

ZR8 SYSTEM DIAGRAM

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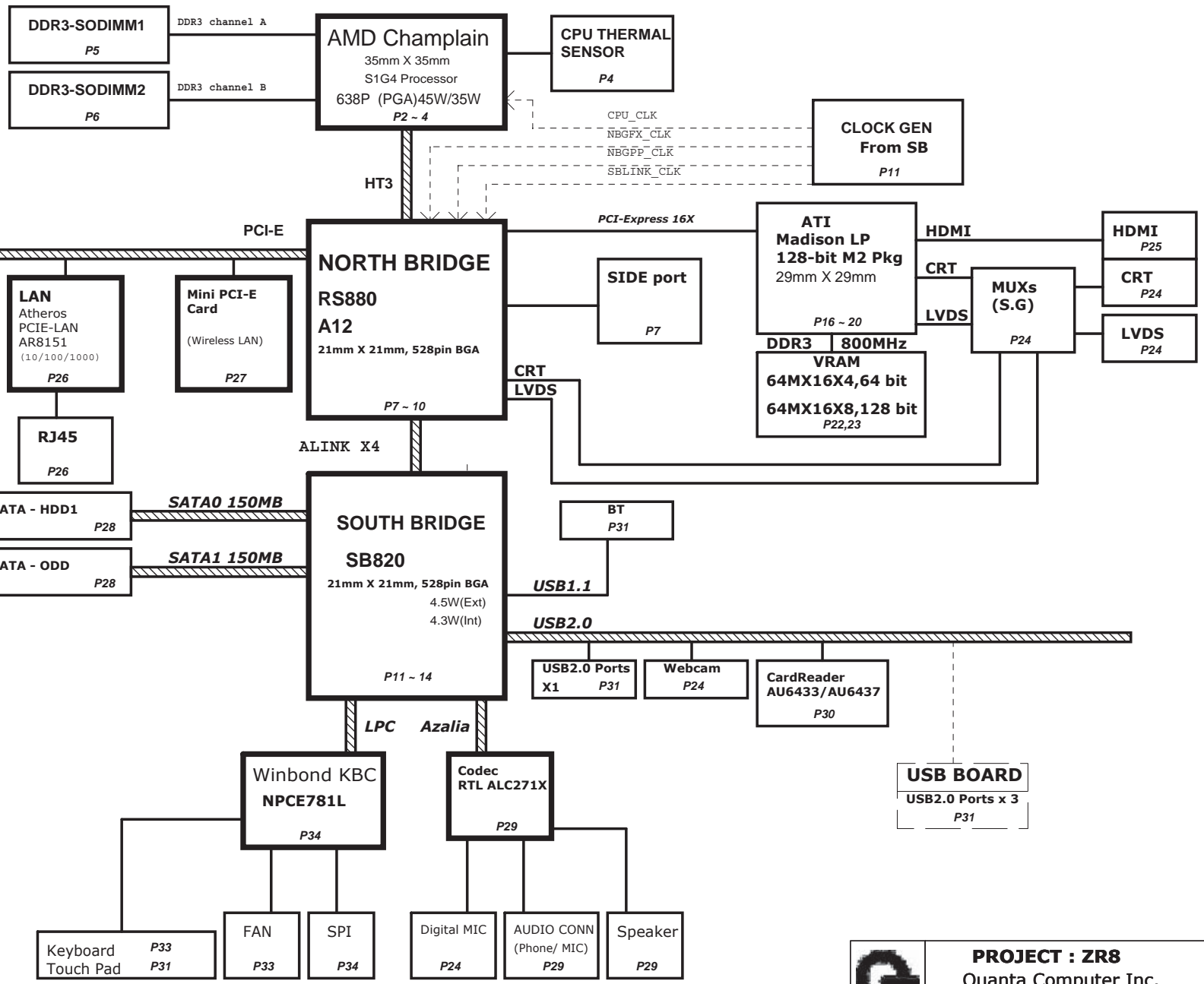


RAMP

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : IN3
 LAYER 7 : GND
 LAYER 8 : BOT

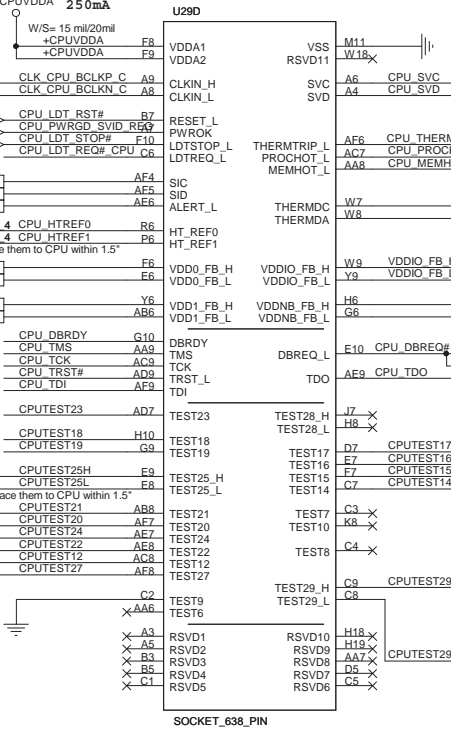
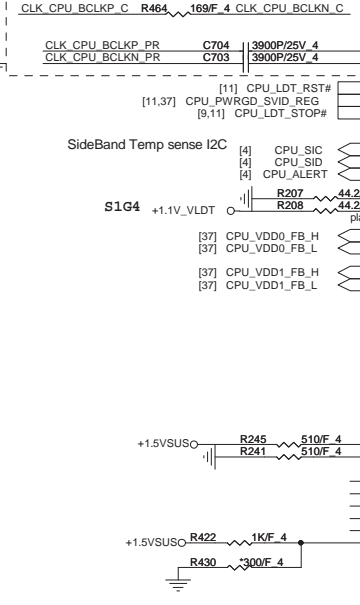
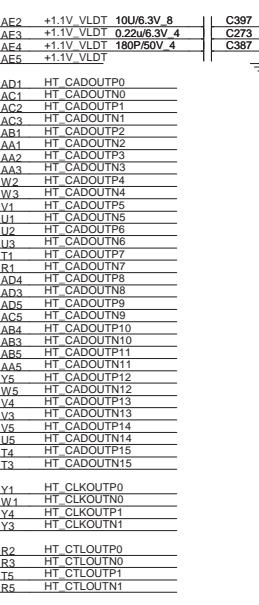
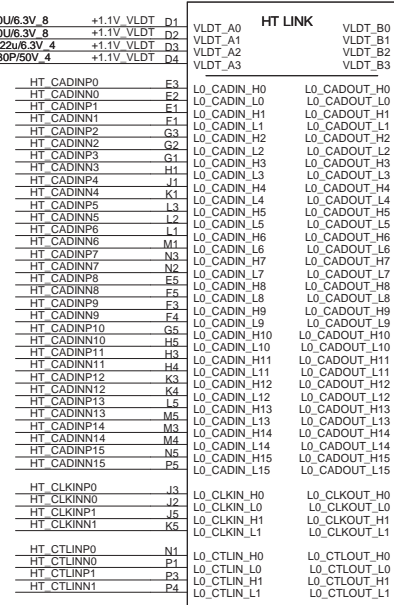
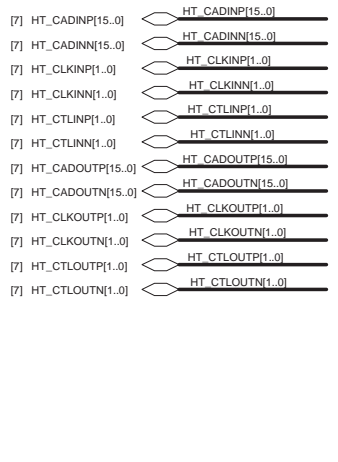
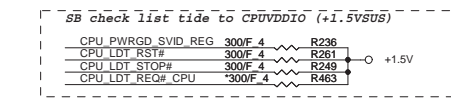
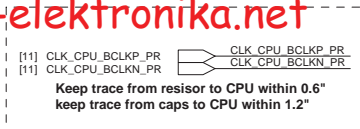
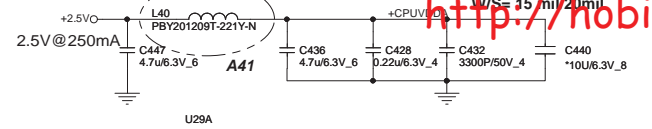
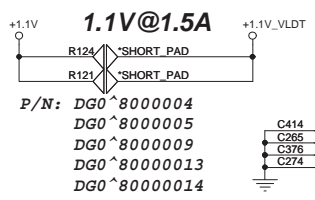
SGN@---->Internal CLK GEN.
 GN@ ---->External CLK GEN.
 IV@ ----> iGPU
 SW@ ----> dGPU
 SP@ ----> iGPU & dGPU notice
 SPE@ ---->Only for dGPU notice
 SIDE@ ----> Side port



- Charger (ISL88731A) P35
- DC/DC (3VPCU / 5VPCU) RT8206B P36
- CPU_VCORE (VCORE) ISL6265A P37
- DC/DC (+1.1V_S5) UP6111AQD P38
- DC/DC (NB_CORE) UP6111AQD P39
- DC/DC (+1.5VSUS) RT8207A P40
- DC/DC (GPU_CORE) MAX8792ETD+T P41
- DC/DC (+1.8V/+1V/+2.5V) HPA00835RTER / RT9018A / RT9025-25PSP P42
- DC/DC (CPU_VDDR) RT9025-25PSP P43

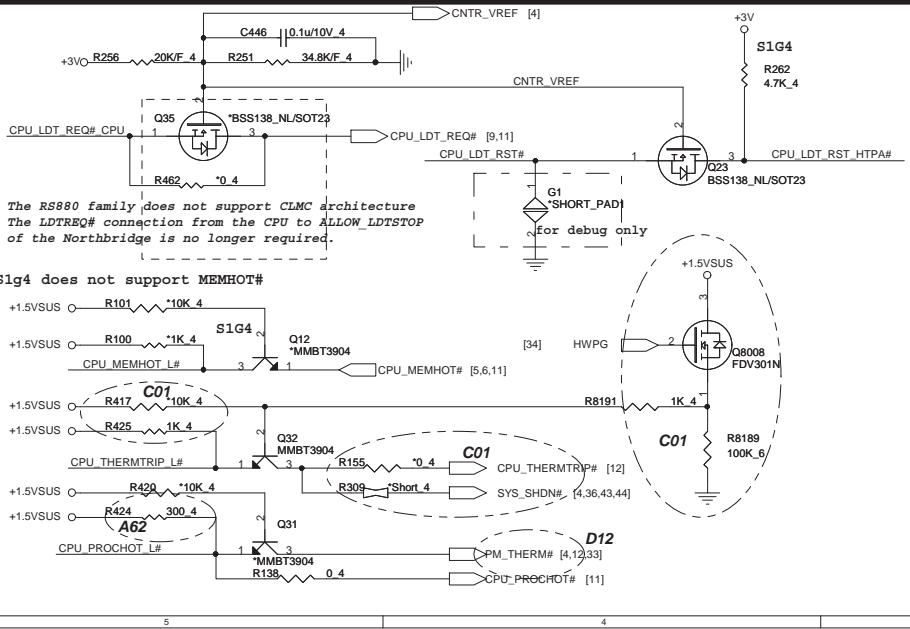
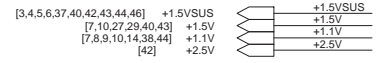
PROJECT : ZR8
 Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date:	Wednesday, May 27, 2009	Sheet 1 of 49

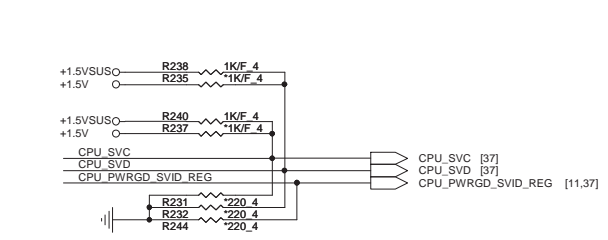


FOX P263826-284R-41F
 DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
 MLX 47296-4131
 DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
 TYC 4-1903401-2
 DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

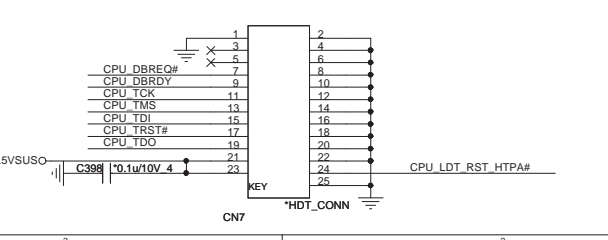
SOCKET_638_PIN



Serial VID



HDT Connector

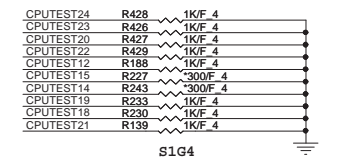


VFIX MODE

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



PROJECT : ZR8
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Size: Document Number: **S1G4 HT,CTL IF 1/3** Rev 1A

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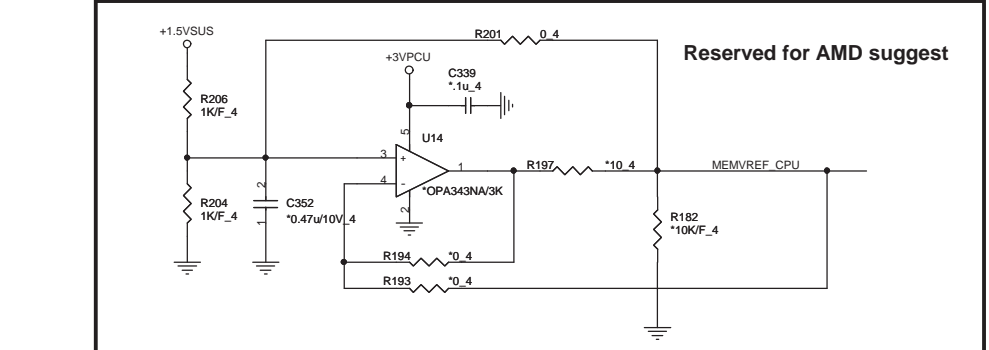
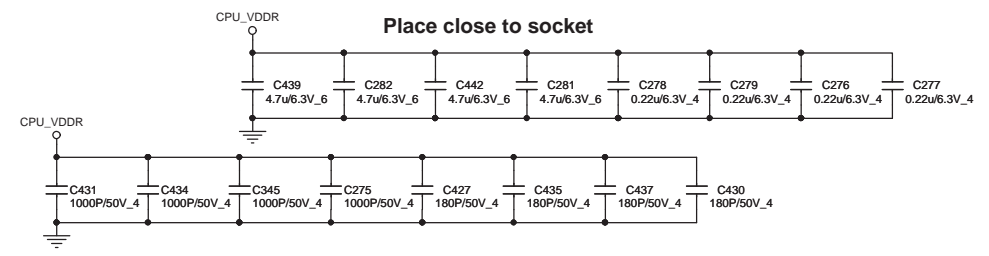
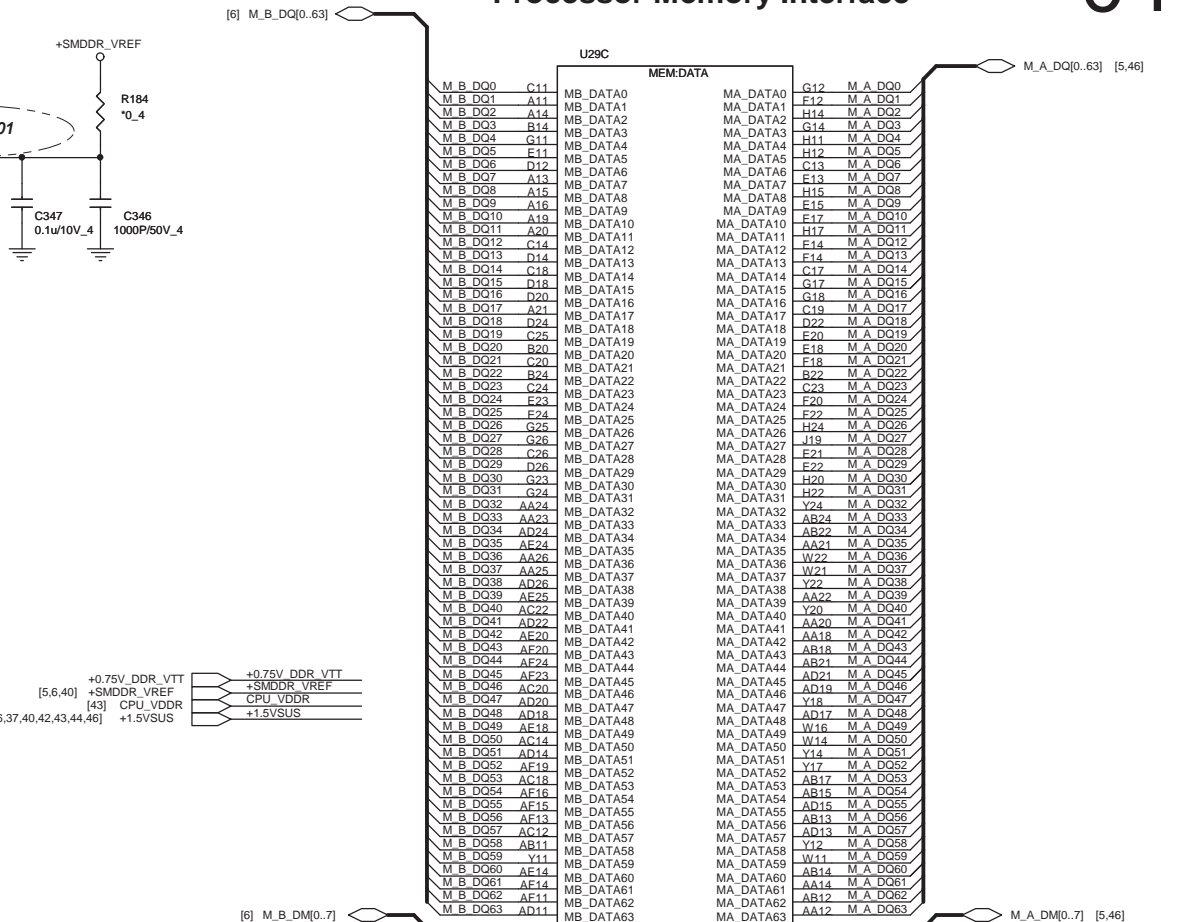
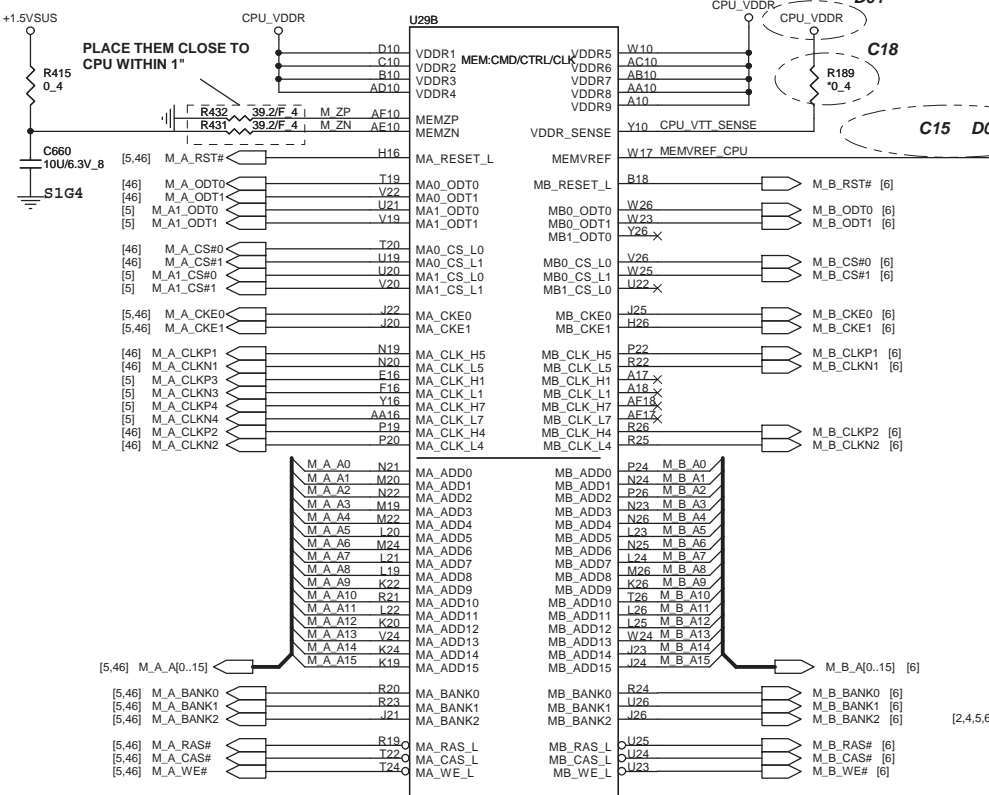
VDDR=>1.75A

VDDR=> 0.9V support 1.65V 300 DR
VDDR=> 1.05V support 1.33 306 800 DR

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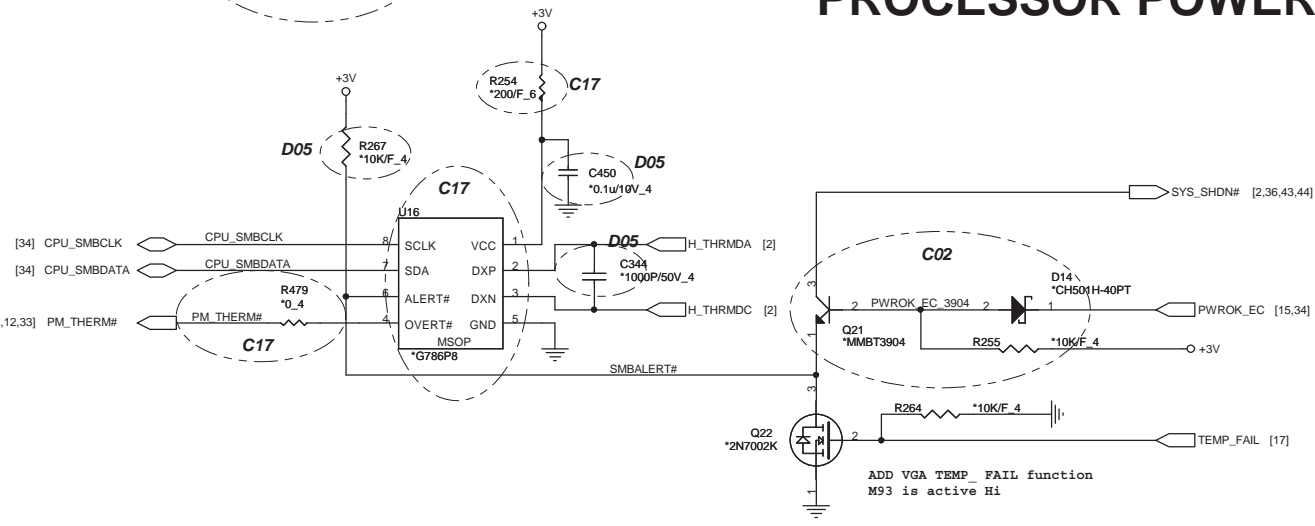
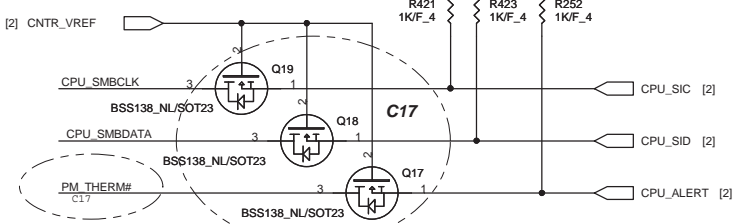
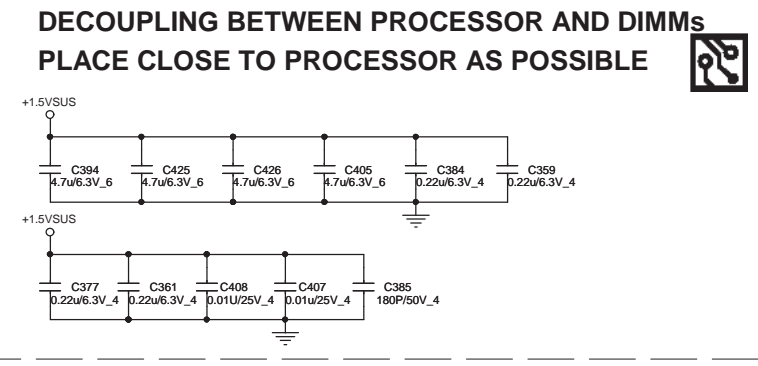
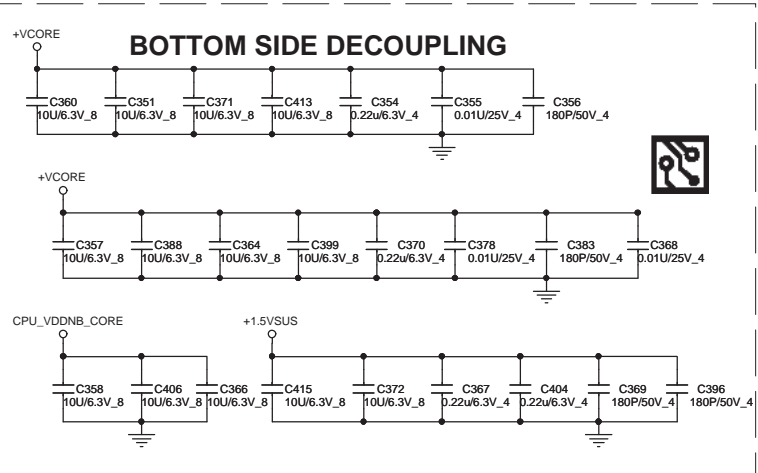
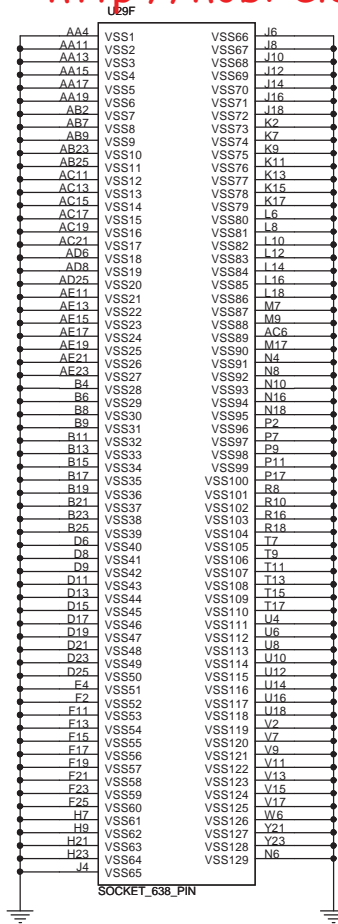
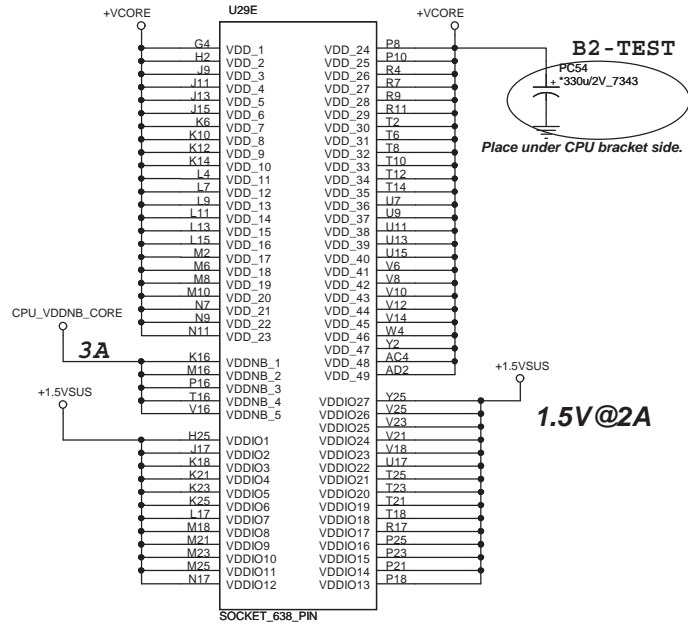
Processor Memory Interface

04



PROJECT : ZR8
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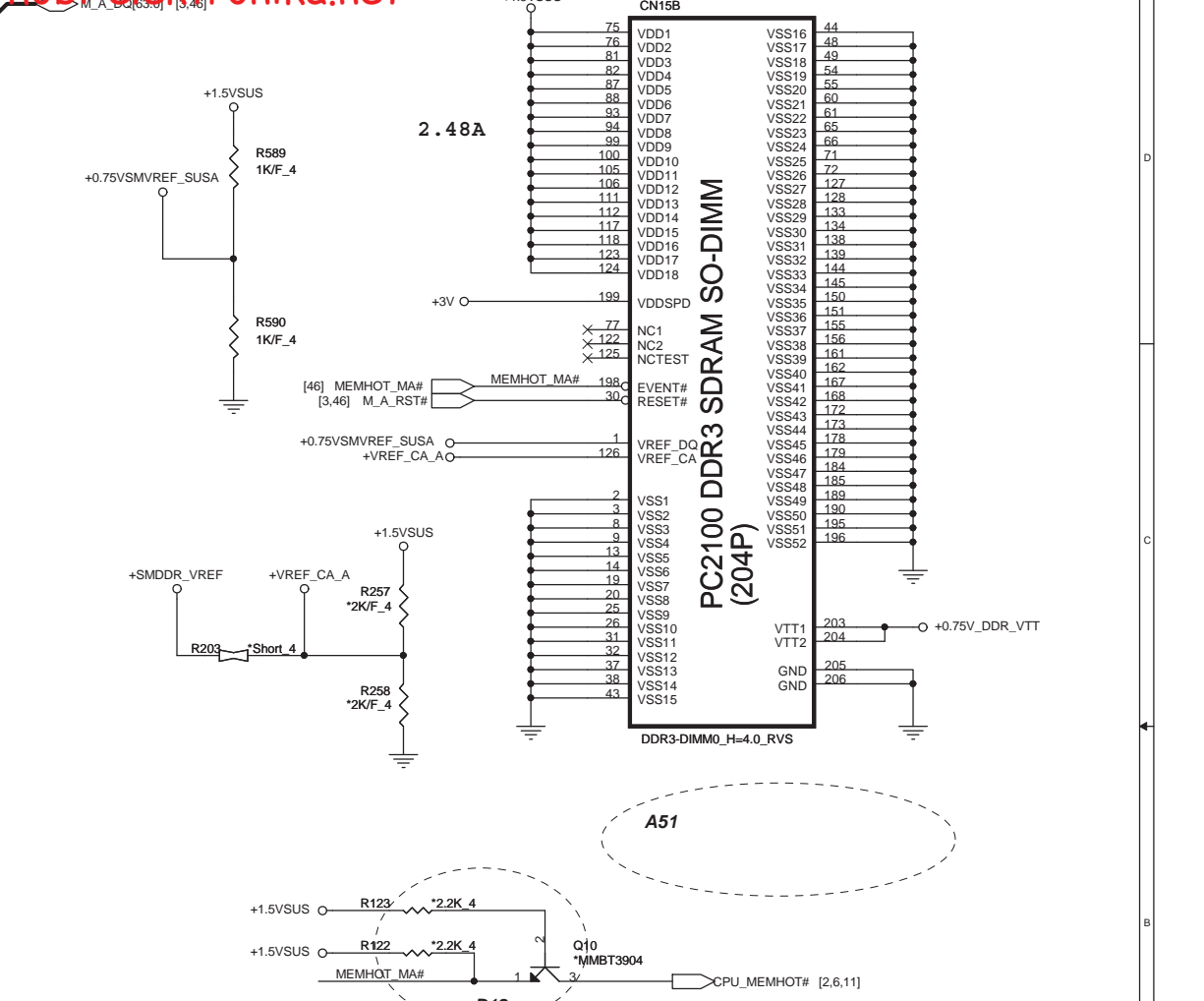
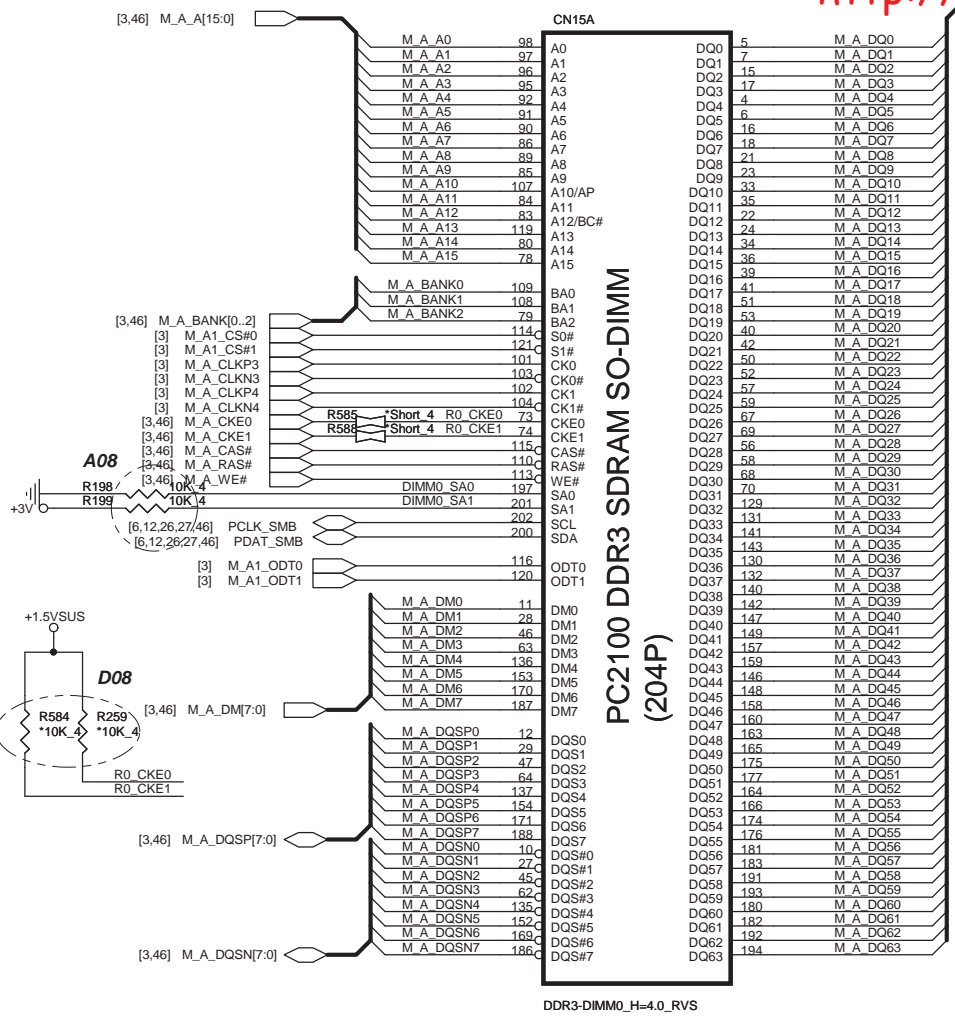
Size	Document Number	Rev
	S1G4 DDRIII MEMORY I/F 2/3	1A
Date:	Wednesday, May 27, 2009	Sheet 3 of 49



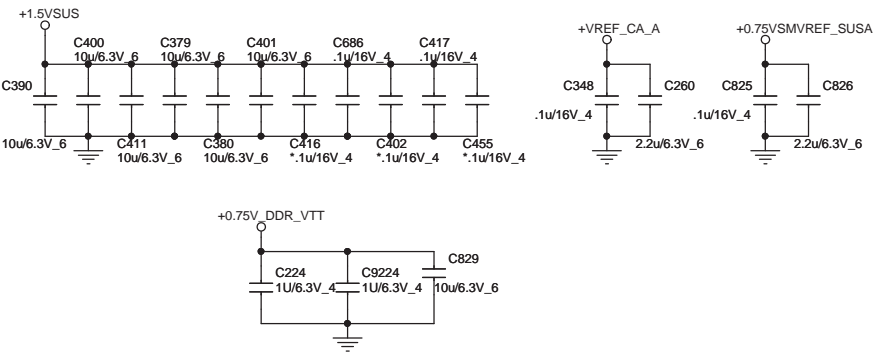
PROCESSOR POWER AND GROUND

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Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date:	Wednesday, May 27, 2009	Sheet 4 of 49

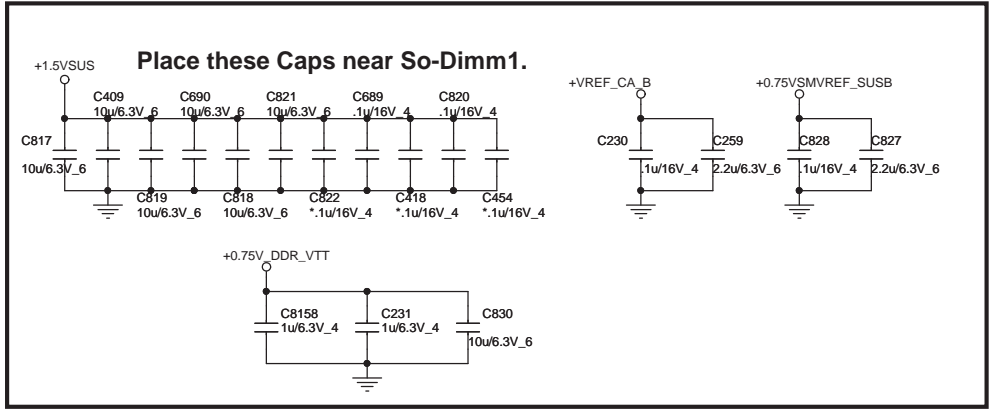
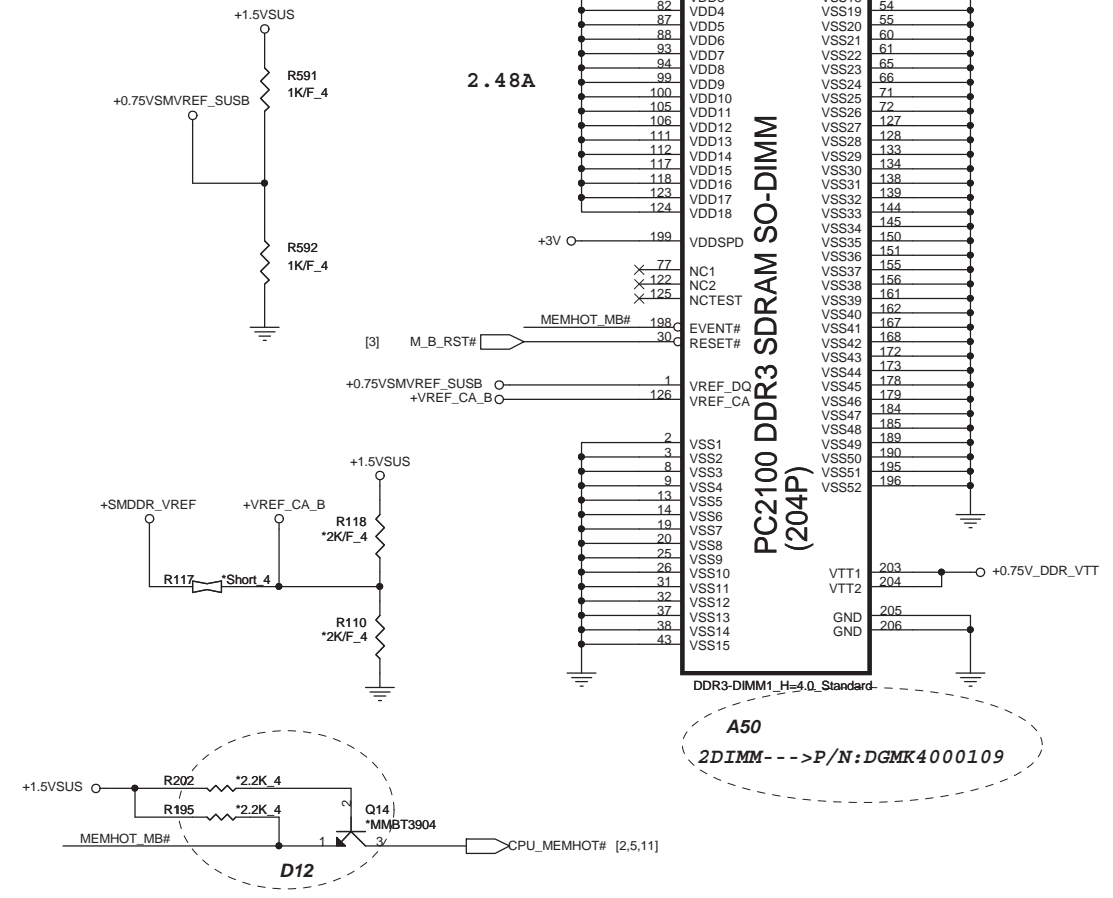
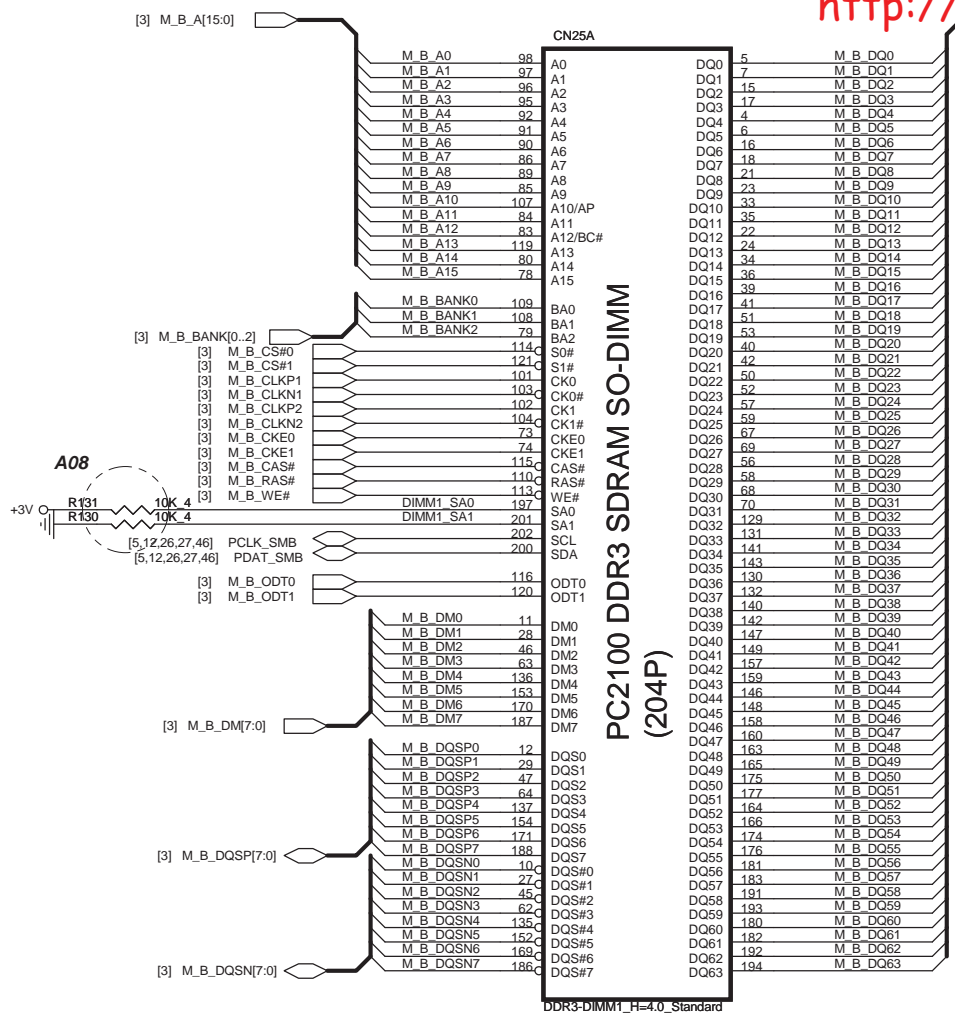


Place these Caps near So-Dimm0.



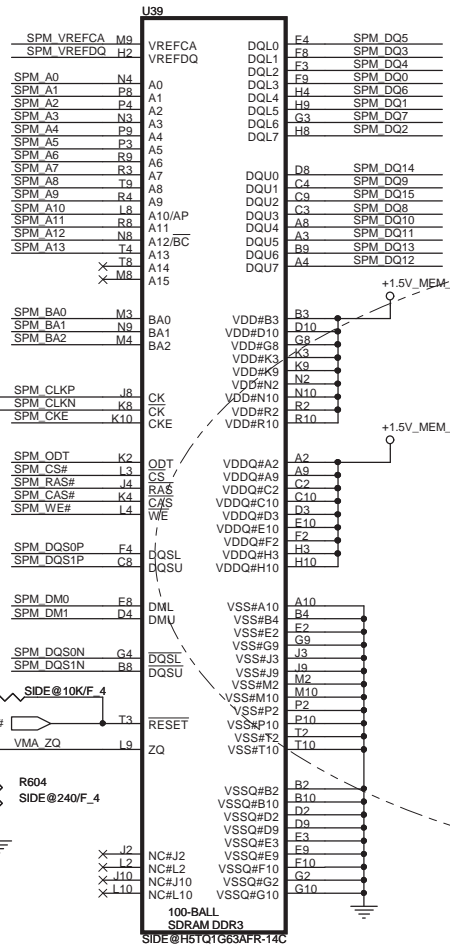
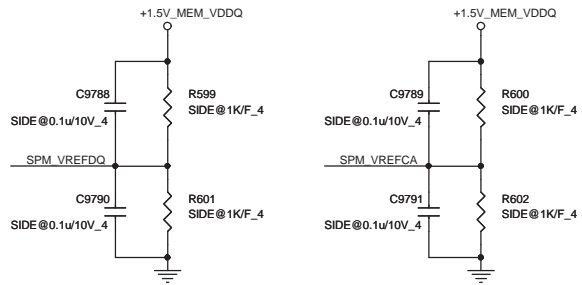
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
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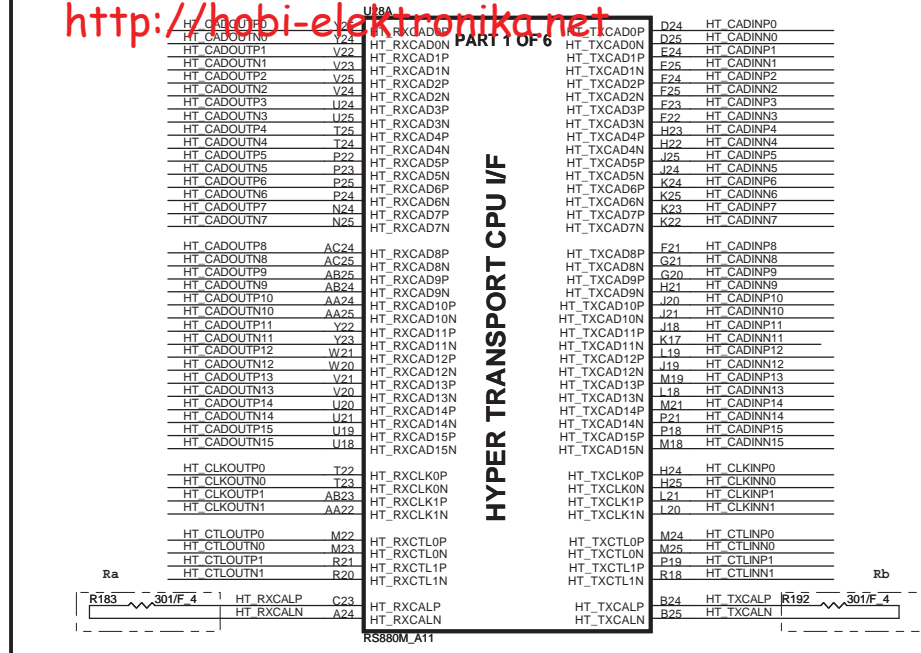


SIDE PORT

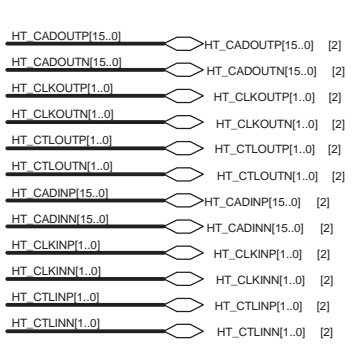
11/4



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HYPER TRANSPORT CPU I/F

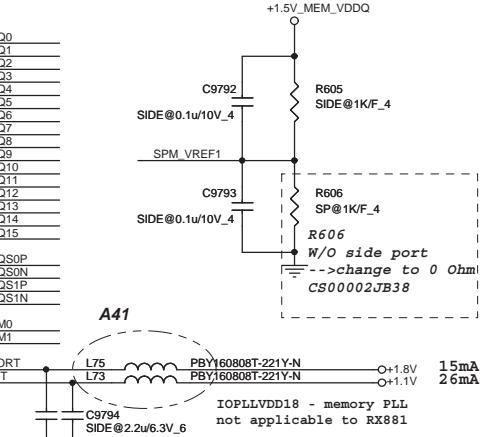
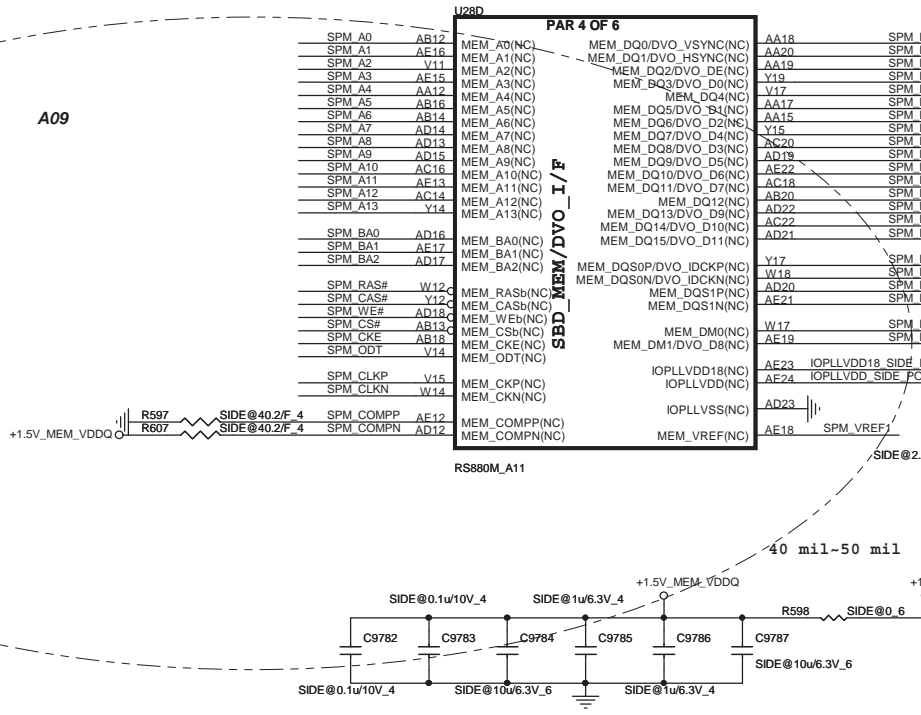


08

Table with 3 columns: signals, R9880, RX880. Rows include HT_TXCALP, HT_RXCALP, HT_TXCALN, HT_RXCALN with resistance values like Ra 301 ohm 1% and Rb 301 ohm 1%.

RES CHIP 1.21K 1/16W +-1% (0402) P/N : CS21212FB18

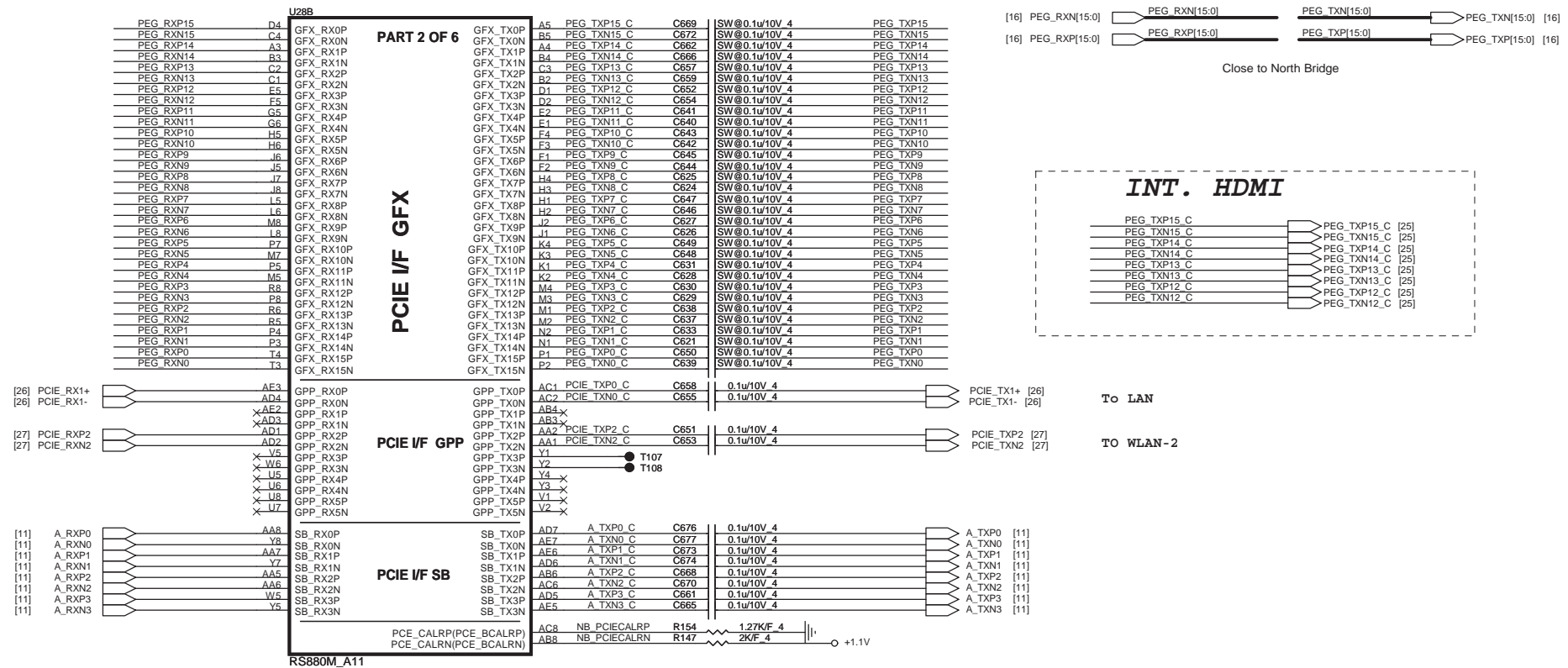
This block is for UMA only , Discrete can remove all component

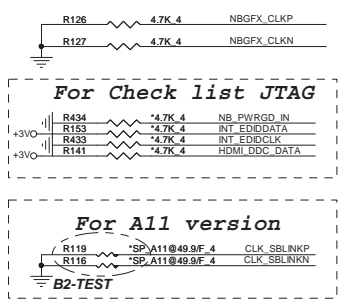


IOPLLVD18 - memory PLL not applicable to RX881

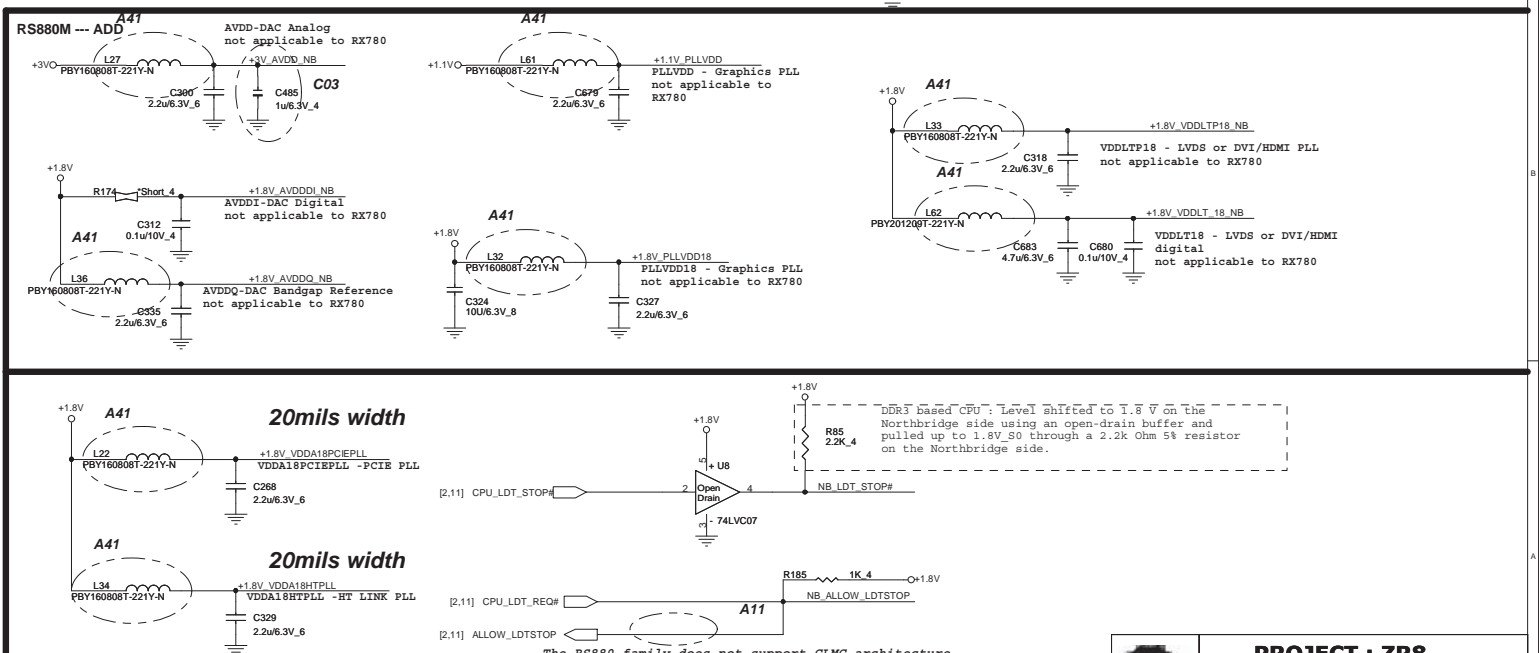
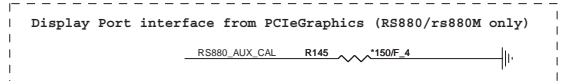
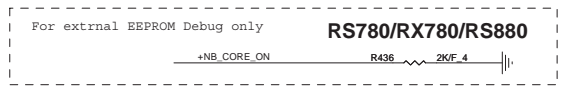
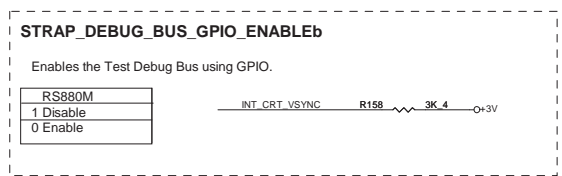
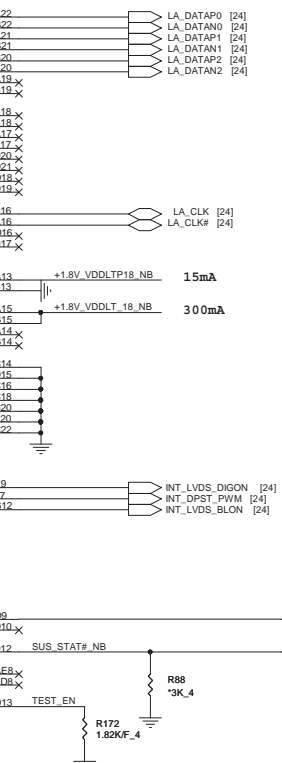
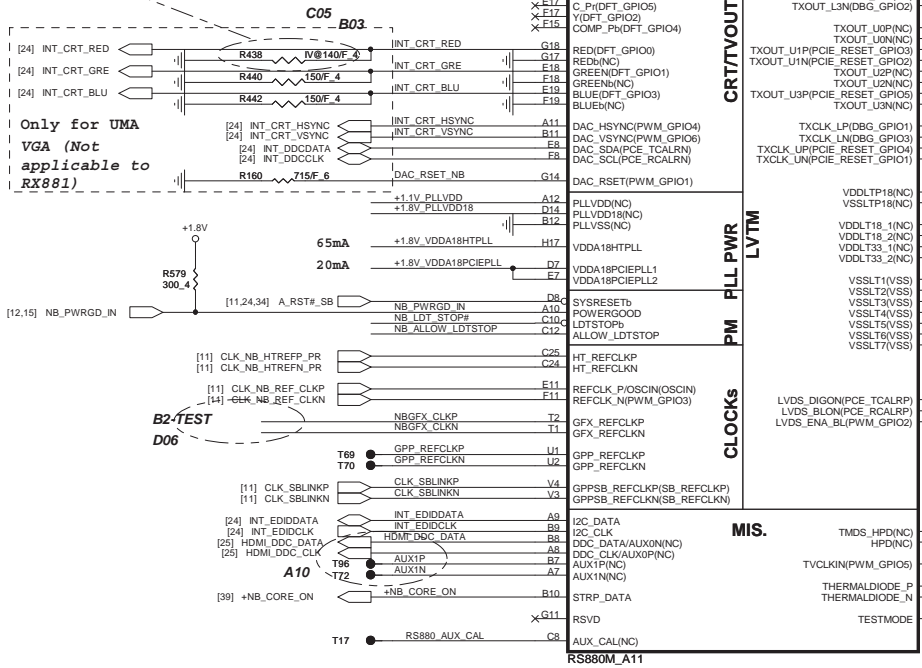


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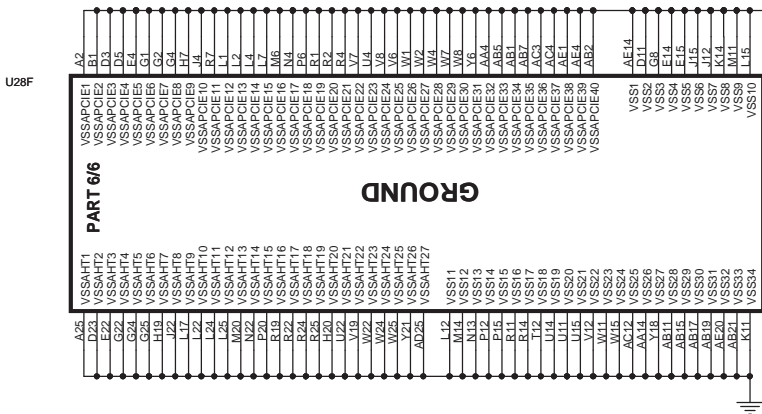


UMA use 140 ohm 1%.
Discrete use 133 ohm 1%.
Note : Only for RS880 series A11 ASIC errata.



DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_{SO} through a 2.2k Ohm 5% resistor on the Northbridge side.

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.



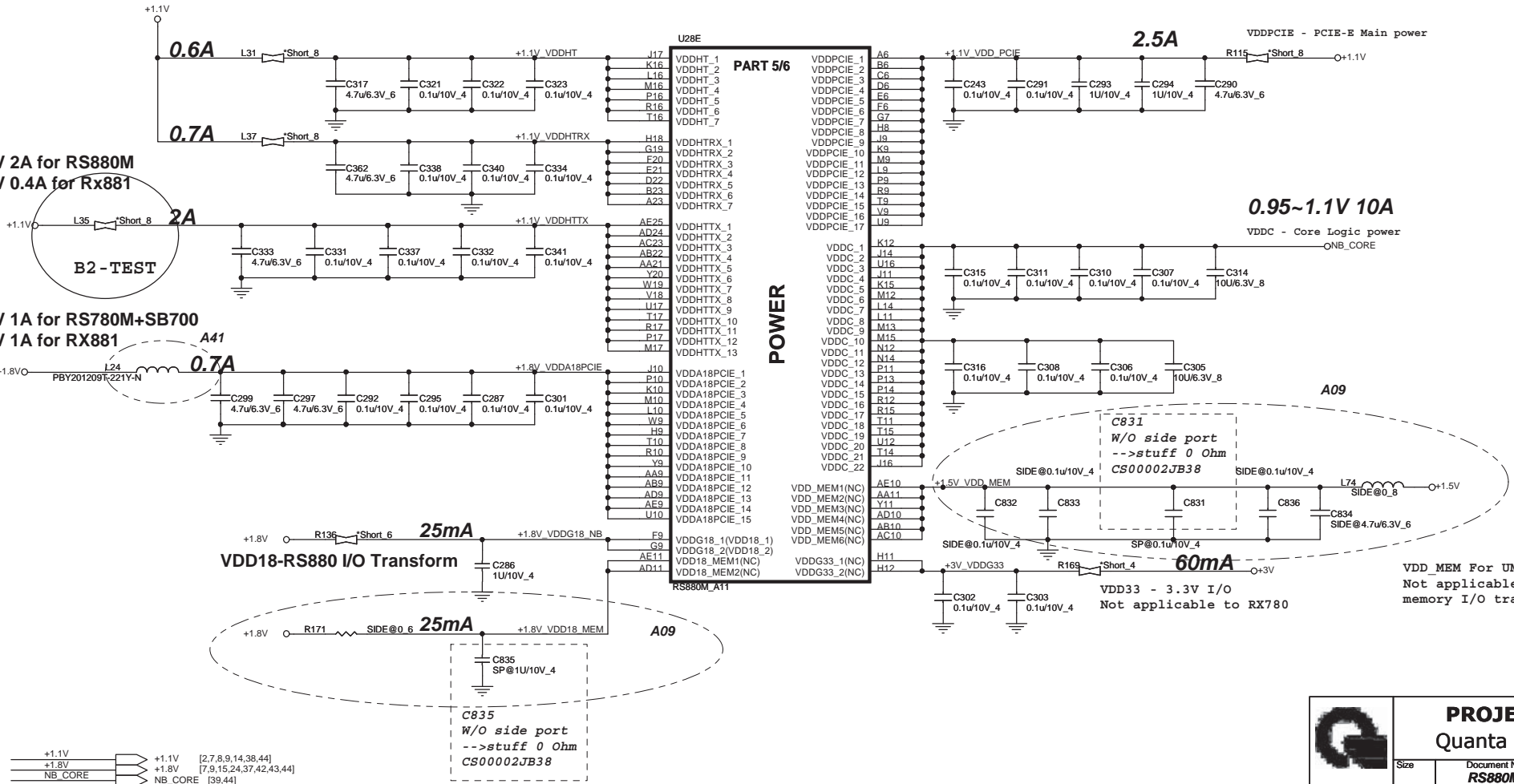
RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLTP18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLTP33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881

+1.1V 2A for RS880M
+1.2V 0.4A for Rx881

+1.8V 1A for RS780M+SB700
+1.8V 1A for RX881



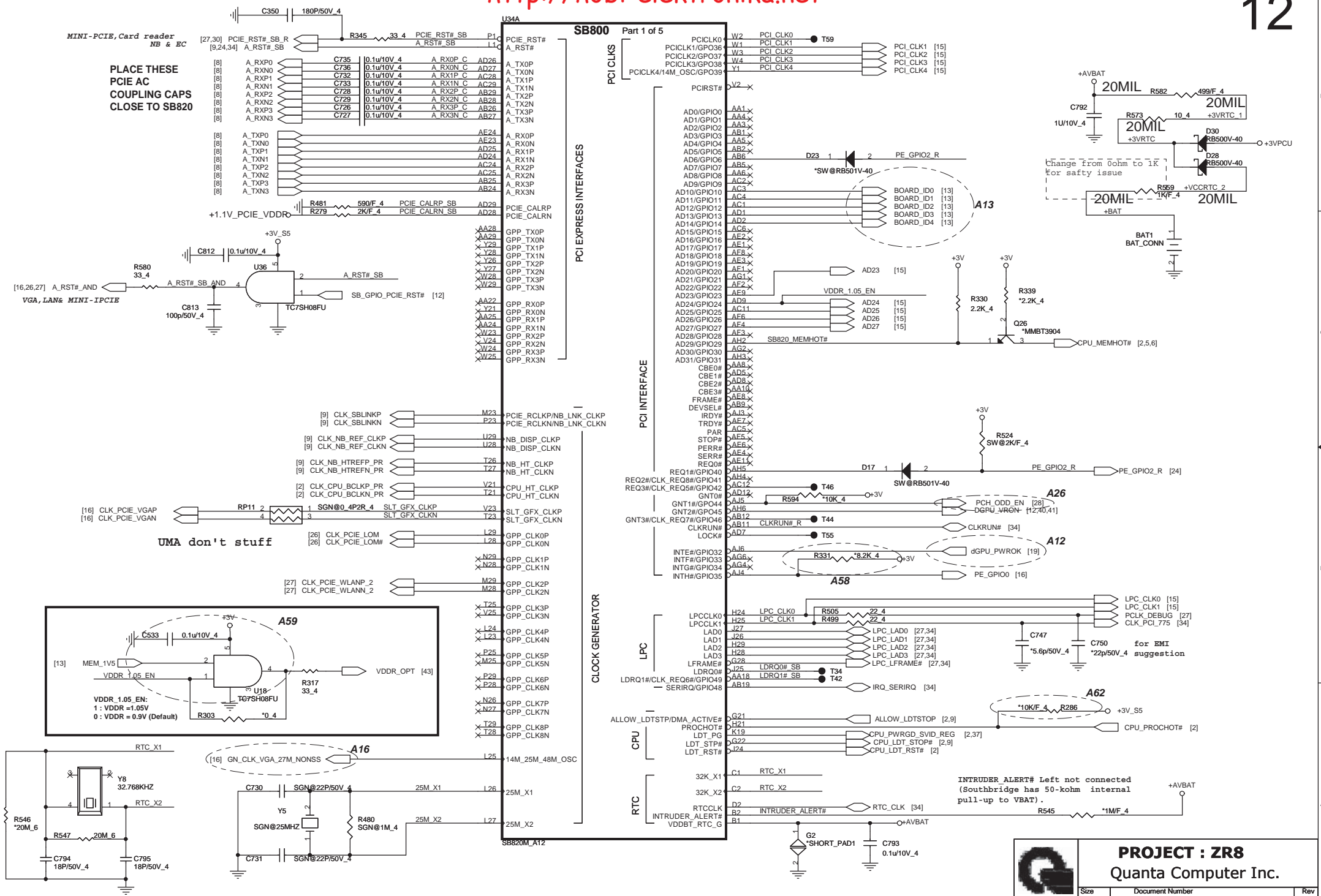
+1.1V → +1.1V [2,7,8,9,14,38,44]
+1.8V → +1.8V [7,9,15,24,37,42,43,44]
NB_CORE → NB_CORE [39,44]

C835
W/O side port
-->stuff 0 Ohm
CS00002JB38

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

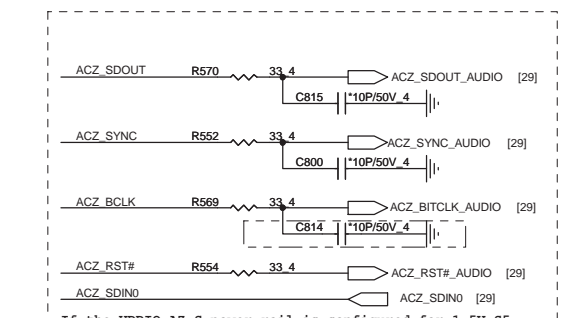
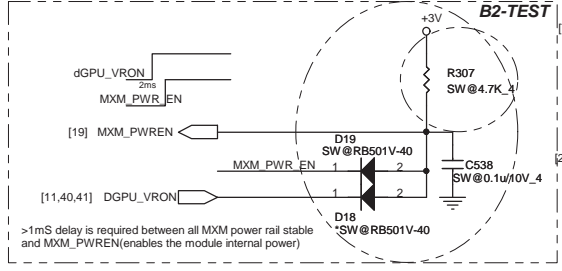
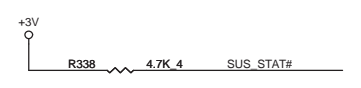
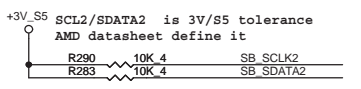
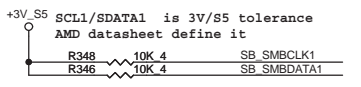
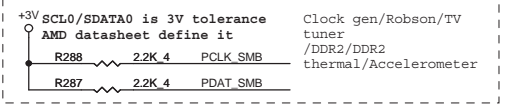
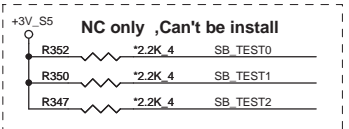


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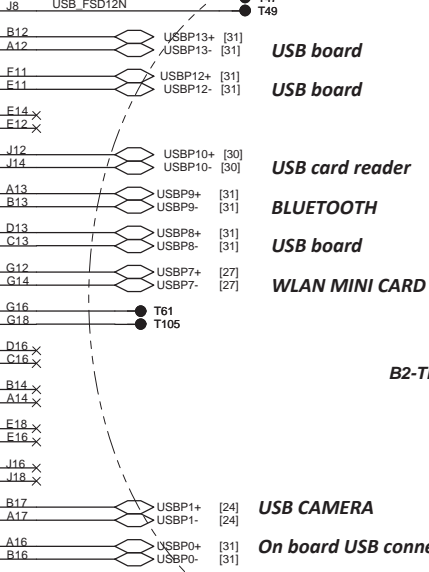
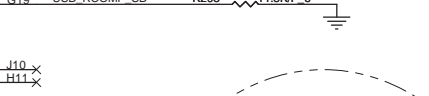
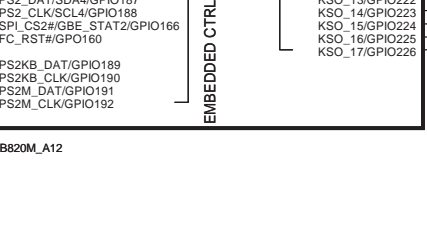
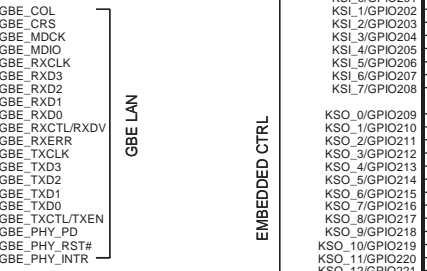
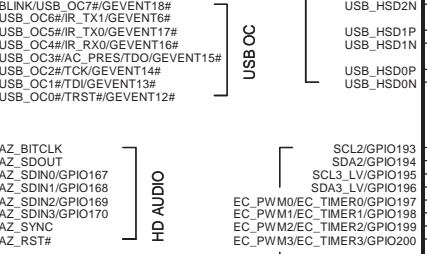
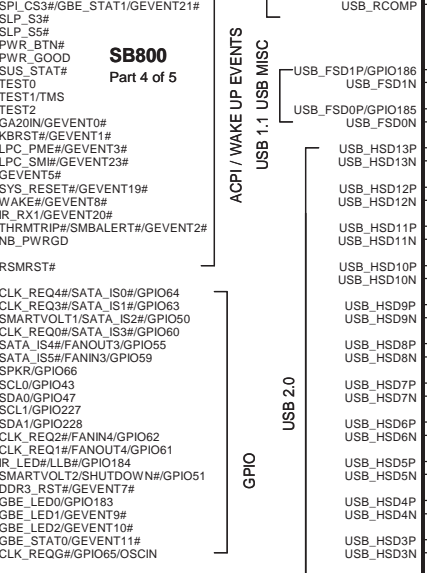
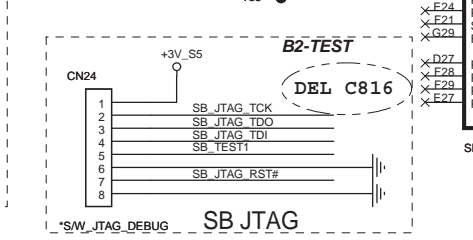
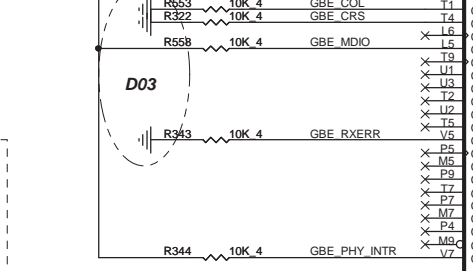
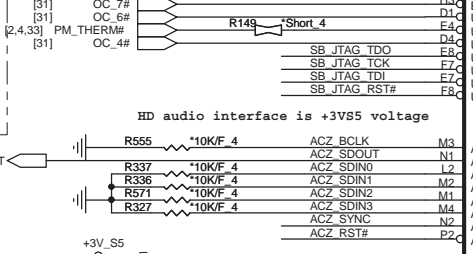
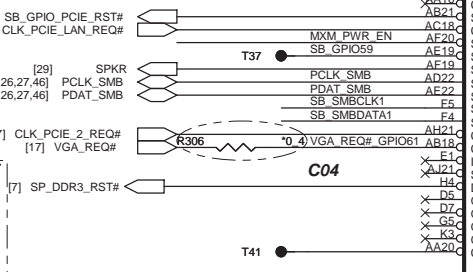
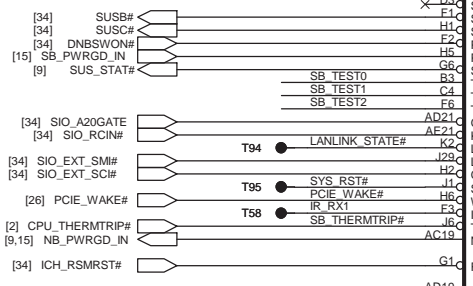


PROJECT : ZR8
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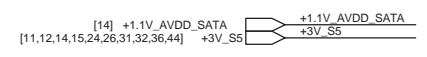
Size	Document Number	Rev
	SB820-PCIE/CPU/LPC 1/4	1A
Date:	Wednesday, May 27, 2009	Sheet 11 of 49



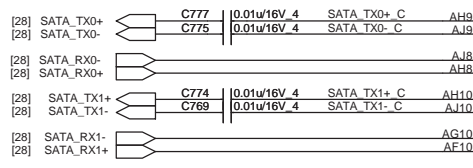
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.



SATA PORT 0,1,2,3
can support AHCI
mode

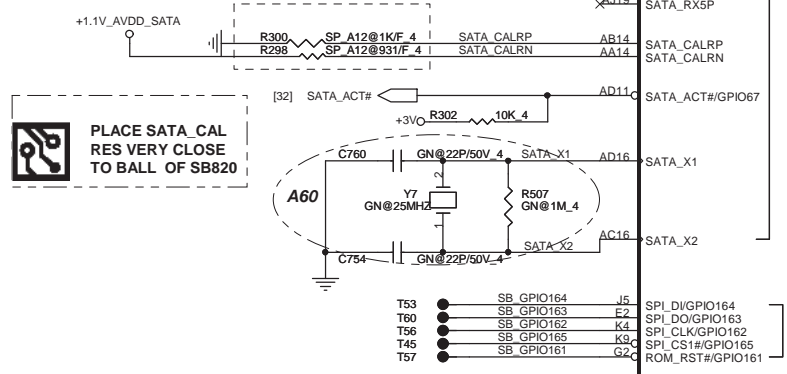


SATA1

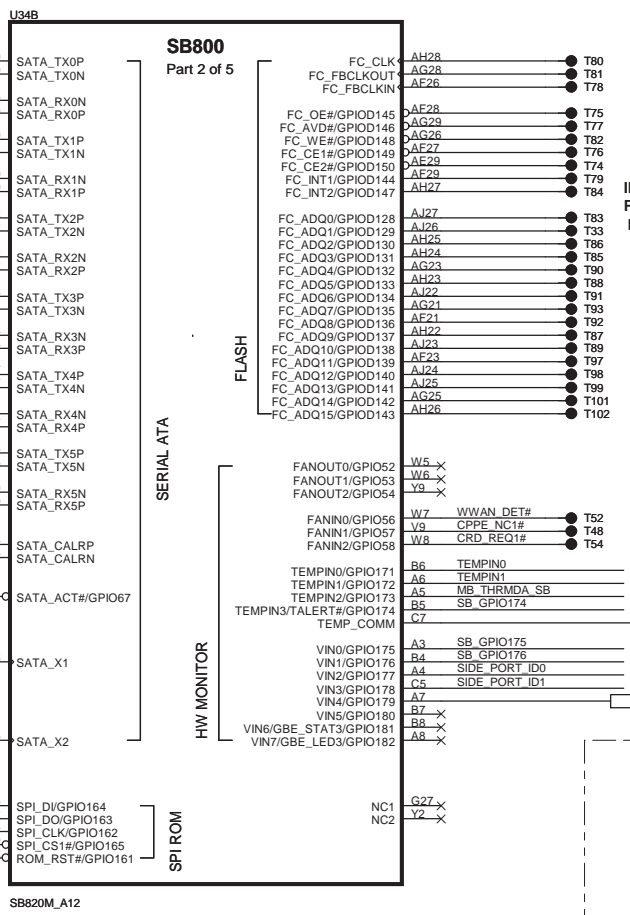


SATA ODD

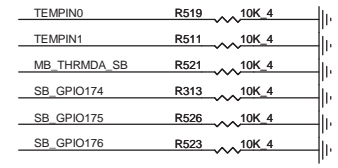
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. P/N:CS18062FB00 (806 Ohm)
SATA_CALRN	SB800 A12: 1k ohm 1% resistor to GND. SB800 A11: 931-? 1% resistor to VDDAN_11_SATA.



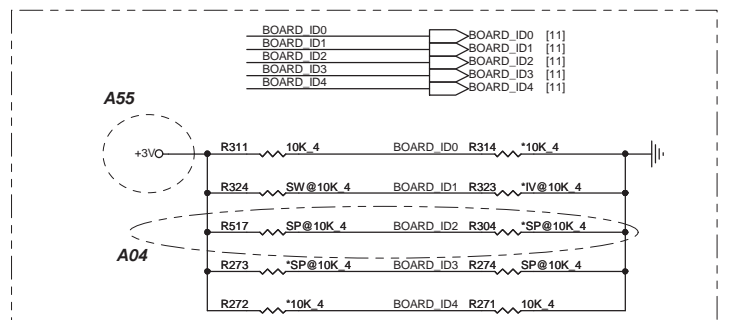
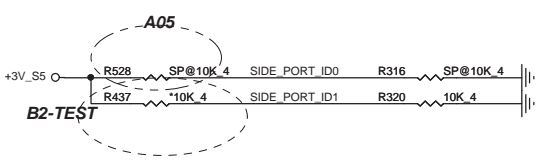
PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820



IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY



	ID1	ID0
HYX	0	0
SAM	0	1
ATI	1	0



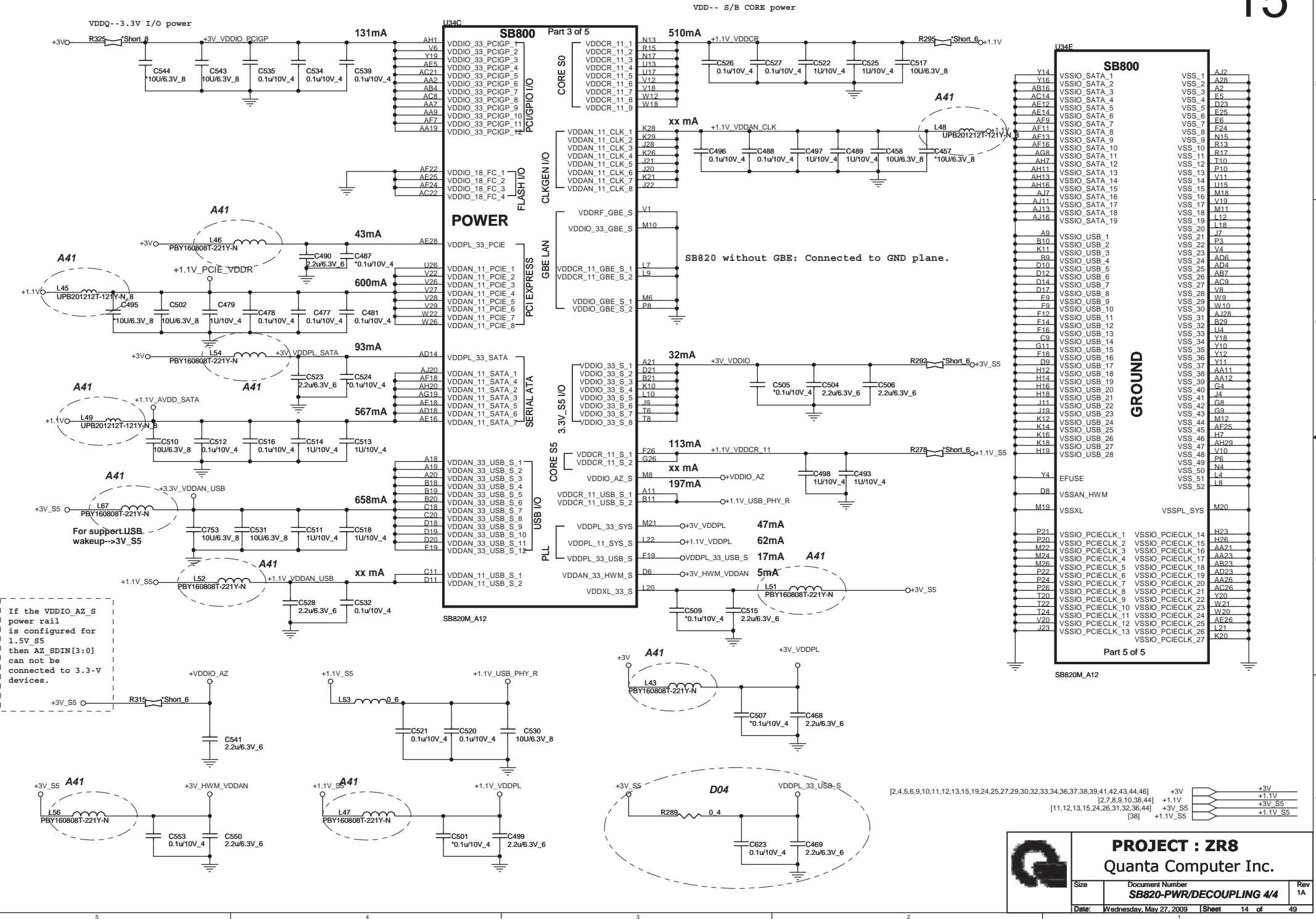
Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A (Default)	JV51-DN (3-DIMM) (Default)	WO/Sideport	UMA	14"
1	N/A	JM51-DN (2-DIMM)	W/Sideport (Default)	Discrete (Default)	15.6" (Default)

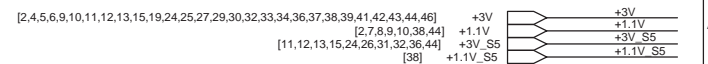
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number SATA/IDE/HWM/SPI 3/4	Rev 1A
Date:	Wednesday, May 27, 2009	Sheet 13 of 49

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET (USE THE BEST POSSIBLE)



If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

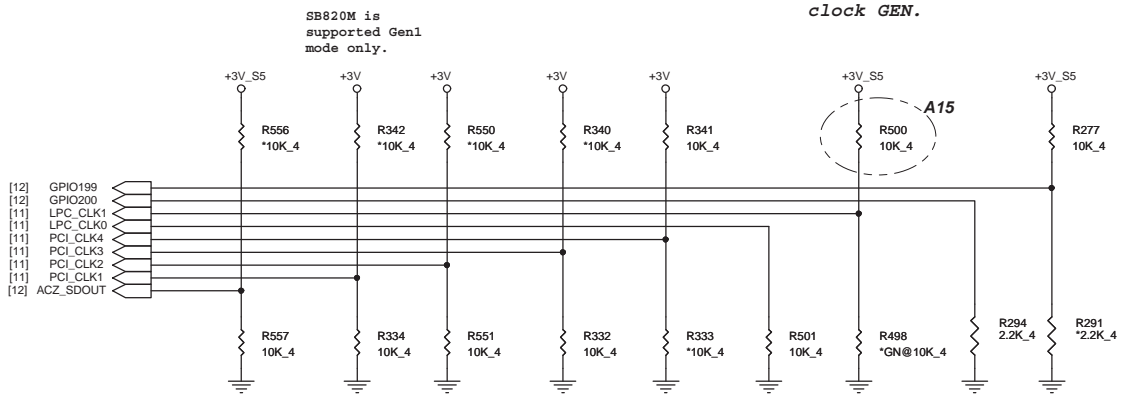


PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/4	1A
Date:	Wednesday, May 27, 2009	Sheet 14 of 49

REQUIRED STRAPS

For internal clock GEN.

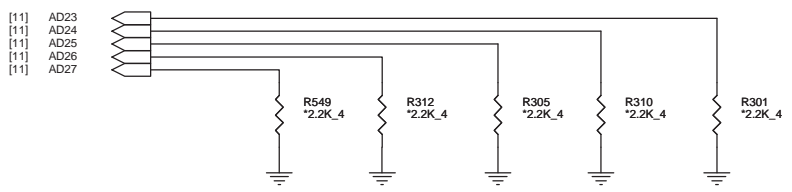


D02	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE DEFAULT	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE DEFAULT	L,H=LPC ROM DEFAULT L, L=FWH ROM	

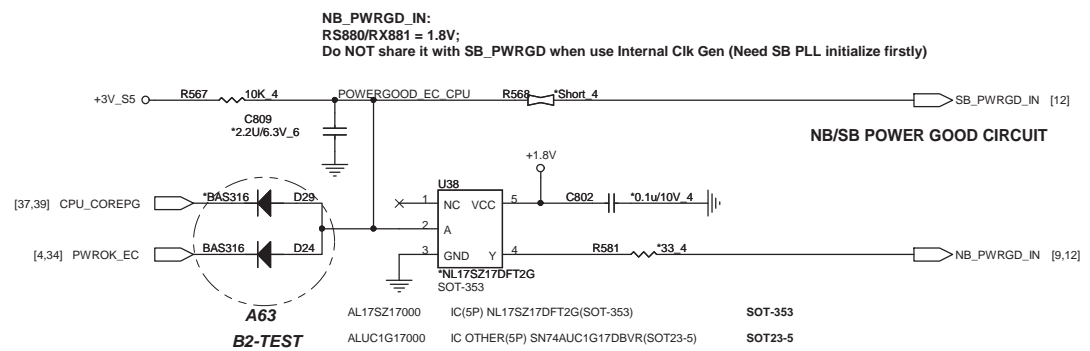
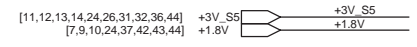
internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



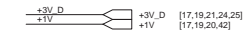
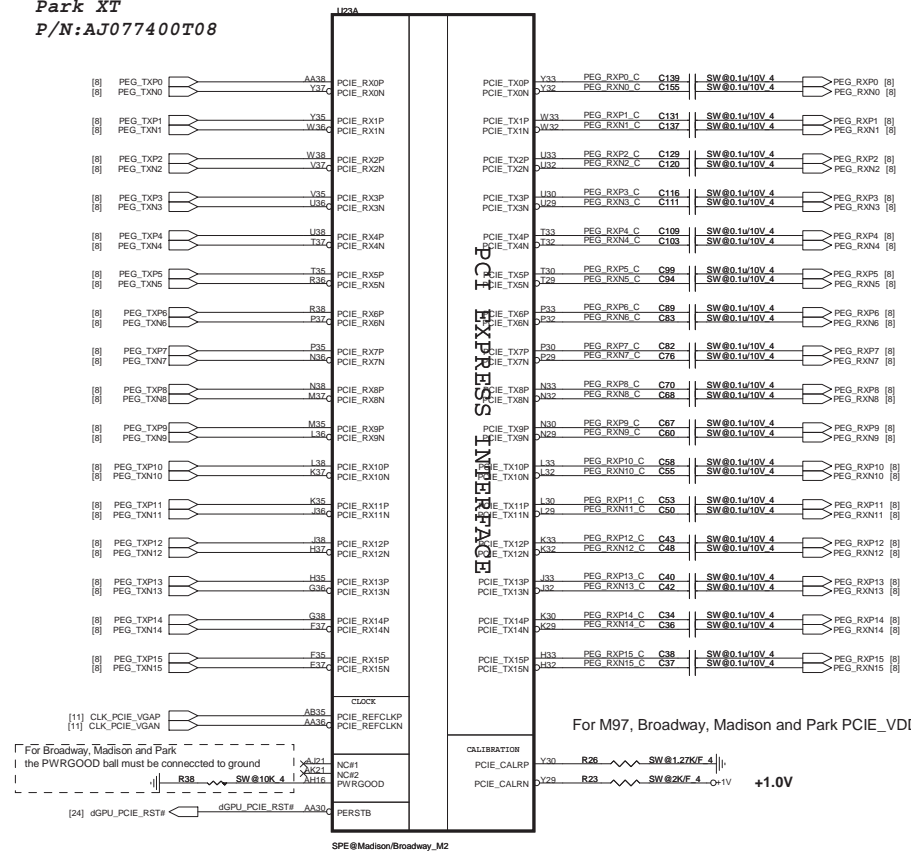
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT



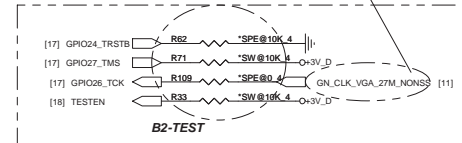
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A
Date:	Wednesday, May 27, 2009	Sheet 15 of 49

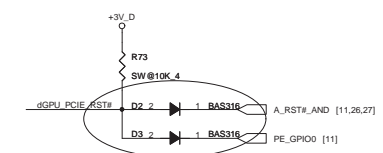
Park XT
P/N: AJ077400T08



Add extra OSC for use SB clock.



SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)

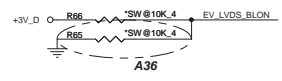


GPU Power-on sequence

- 1 => +3V_D
- 2 => +VGPU_CORE
- 3 => +VGPU_IO
- 4 => +1V
- 5 => +1.5V_GPU
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK

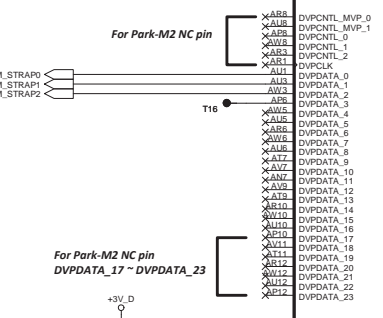
[19,20,21,43] +1.8V_GPU
 [16,18,20,42] +1V
 [16,19,21,24,25] +3V_D

1.8V GPIO

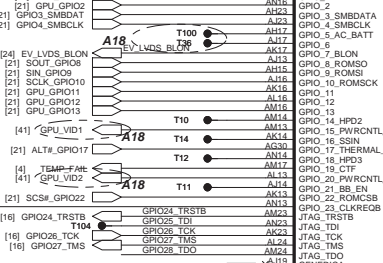


For Park-M2 NC pin

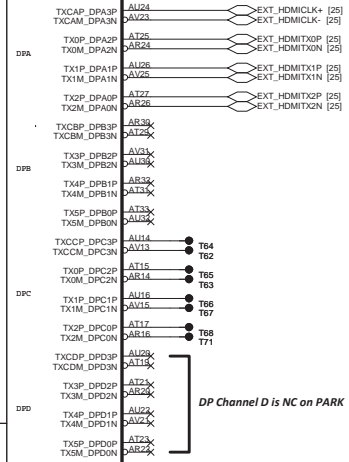
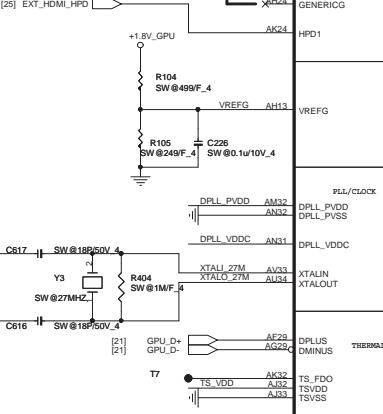
For Park-M2 NC pin DVPDATA_17 ~ DVPDATA_23



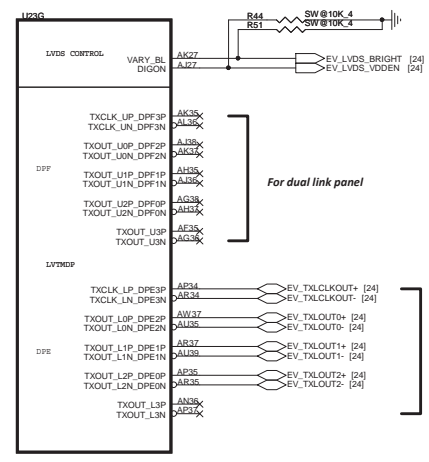
GENERAL PURPOSE I/O



For Park-M2 is NC pin



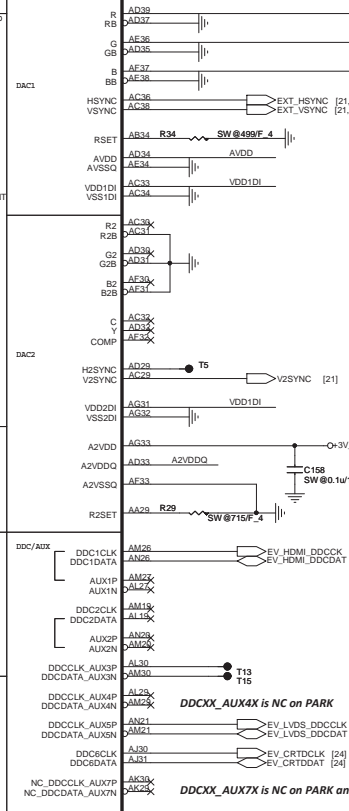
DP Channel D is NC on PARK



For dual link panel

For Single link panel

SPE@Madison/Broadway_M2



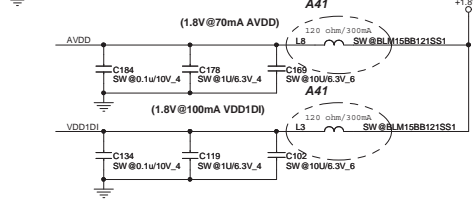
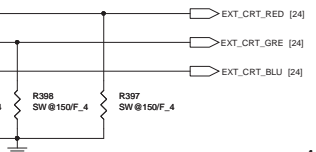
HDMI

LVDS

CRT

DDCX_AUX4X is NC on PARK

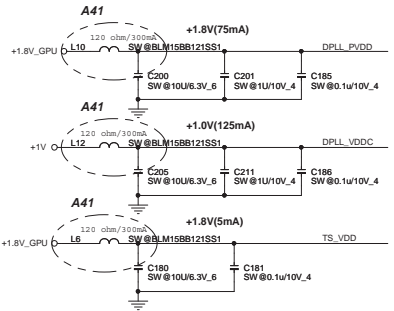
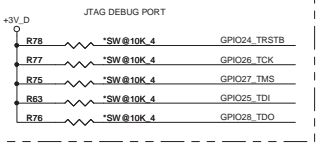
DDCX_AUX7X is NC on PARK and M9X



+1.8V_GPU

+3V_D (3.3V@130mA A2VDD)

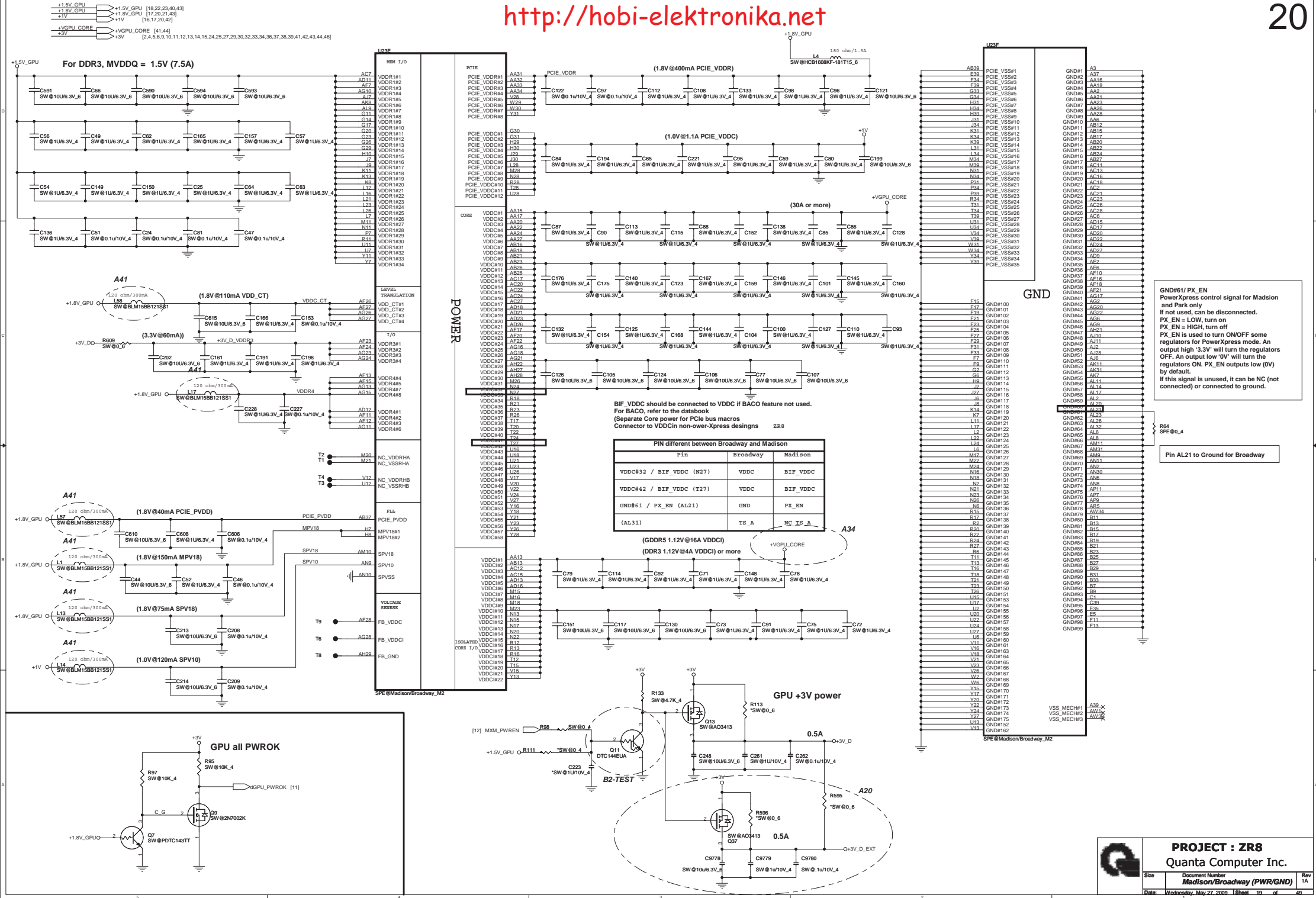
+1.8V_GPU



SPE@Madison/Broadway_M2

PROJECT : ZR8
 Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway-HOST I/F	1A
Date:	Wednesday, May 27, 2009, 18:04:17	of 49



BIF_VDDC should be connected to VDDC if BACO feature not used.
 For BACO, refer to the databook
 (Separate Core power for PCIe bus macros
 Connector to VDDCin non-over-Xpress designs ZR8

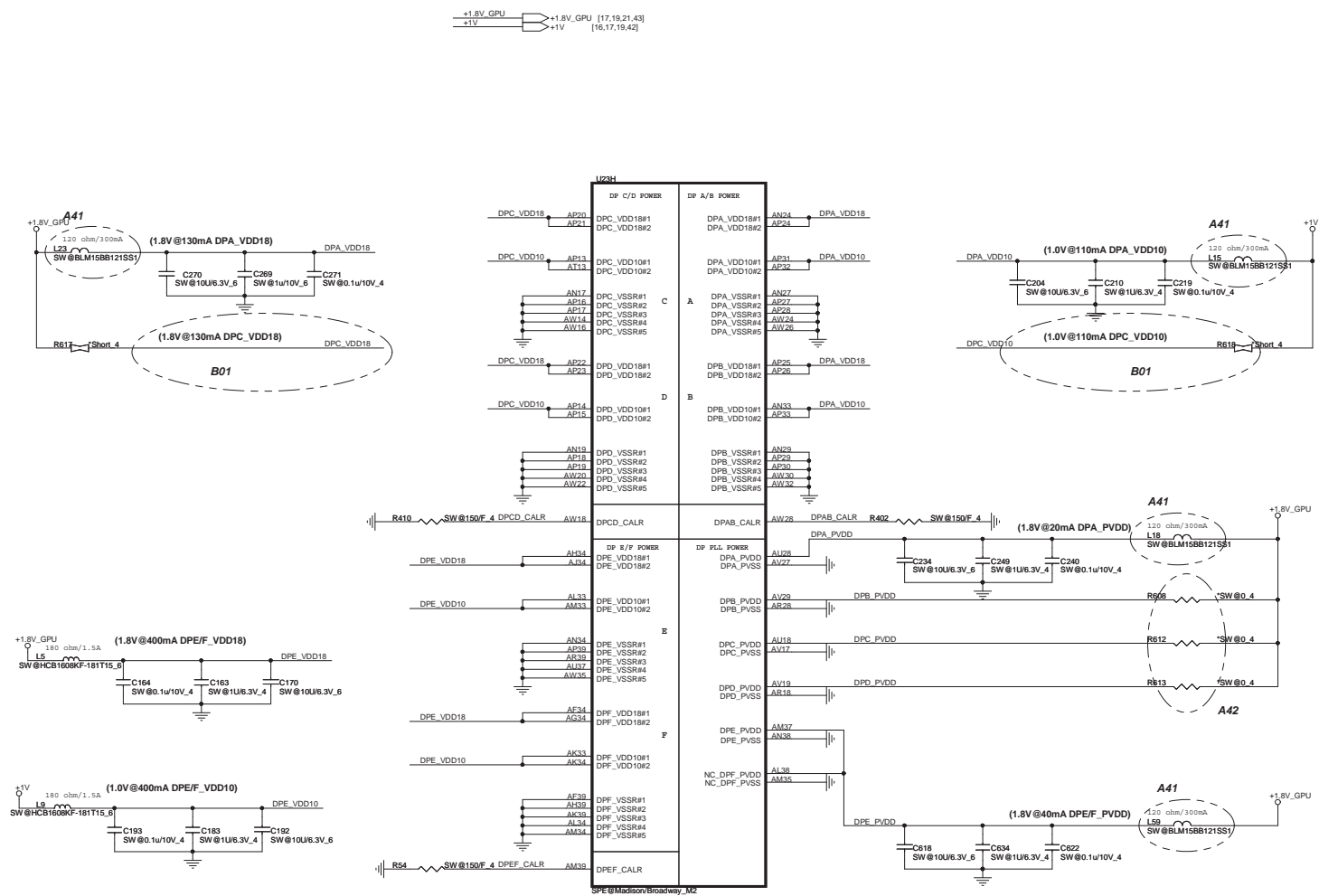
Pin	Broadway	Madison
VDDC#32 / BIF_VDDC (N27)	VDDC	BIF_VDDC
VDDC#42 / BIF_VDDC (T27)	VDDC	BIF_VDDC
GND#61 / P_X_EN (AL2.1)	GND	P_X_EN
(AL3.1)	TS_A	NC TS_A

GND#61/ P_X_EN
 PowerXpress control signal for Madson and Park only
 If not used, can be disconnected.
 P_X_EN = LOW, turn on
 P_X_EN = HIGH, turn off
 P_X_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. P_X_EN output low (0V) by default.
 If this signal is unused, it can be NC (not connected) or connected to ground.

Pin AL21 to Ground for Broadway

PROJECT : ZR8
 Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway (PWR/GND)	
Date:	Wednesday, May 27, 2009, 11:04am	19 of 49

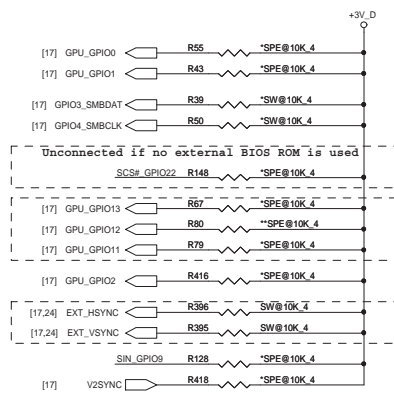


PROJECT : ZRS
Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1/A

Date: Wednesday, May 27, 2009, 15:00:23, 20.04.09

PIN STRAPS



Memory Aperture size

GPIO [13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Function Table

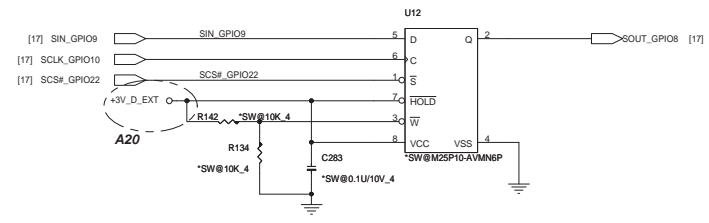
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRs_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
BIOS_ROM_EN	GPIO_22_ROMCSB		0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX_M25P10A:101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0GT/s capability will be controlled by software.)
GPIO_8_ROMSO_H2SYNC_GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1]	HSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

SERIAL ROM

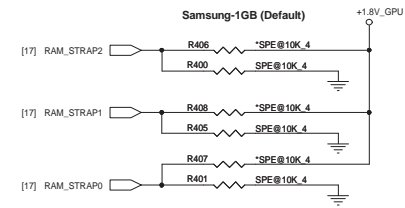
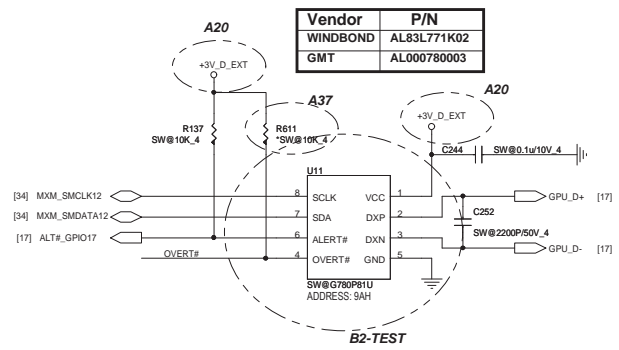


DDR3 Memory Aperture size

DDR3 Memory Aperture size

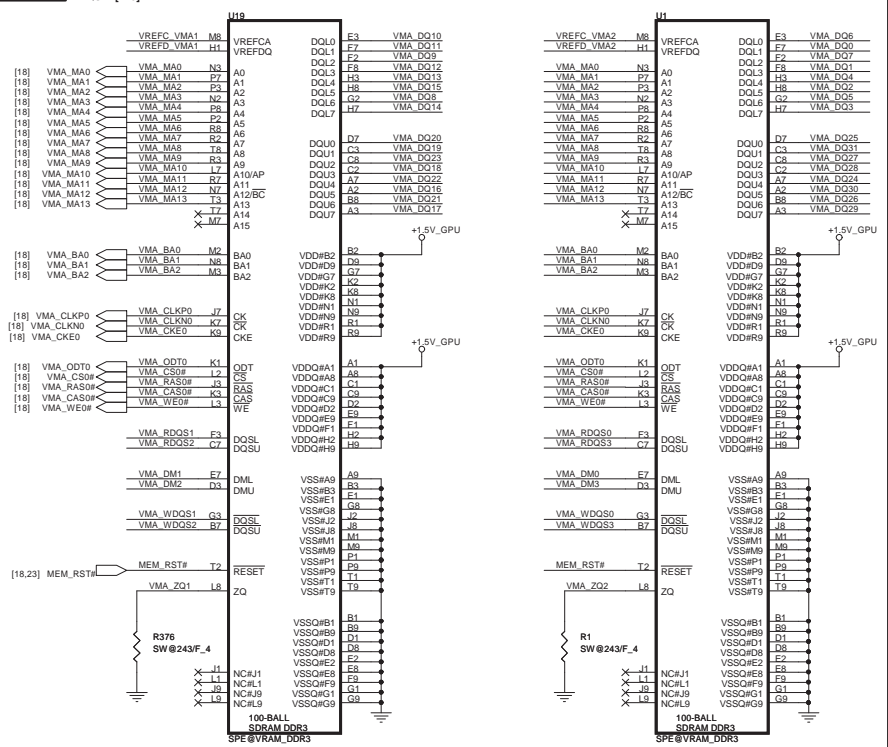
Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Park	1	1	0
			Madison	1	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Park	0	1	0
			Madison	0	0	0
AMD	K4W2G1646B-HC12	AKD5MGGT500	Park	0	0	1
			Madison	1	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	Park	0	1	1
			Madison	1	0	1

Thermal Sensor



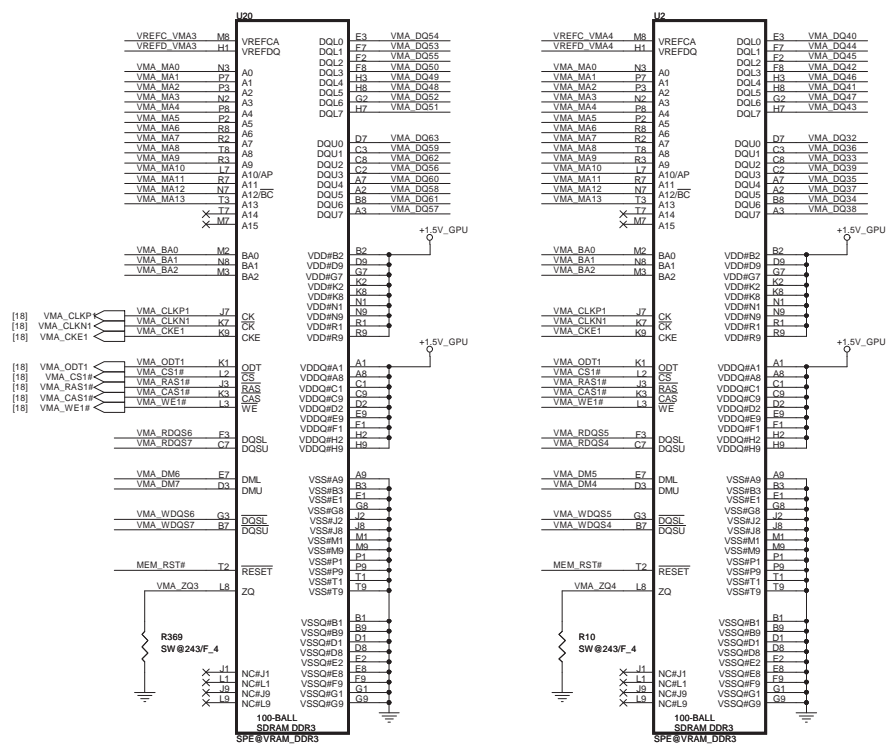
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

- [18] VMA_DQ[63..0] VMA_DQ[63..0]
- [18] VMA_DM[7..0] VMA_DM[7..0]
- [18] VMA_RDQS[7..0] VMA_RDQS[7..0] QSA#[7..0]
- [18] VMA_WDQS[7..0] VMA_WDQS[7..0] QSA#'[7..0]



TOP Left

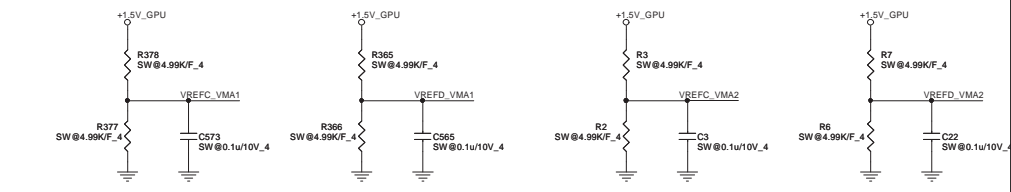
BOT Left



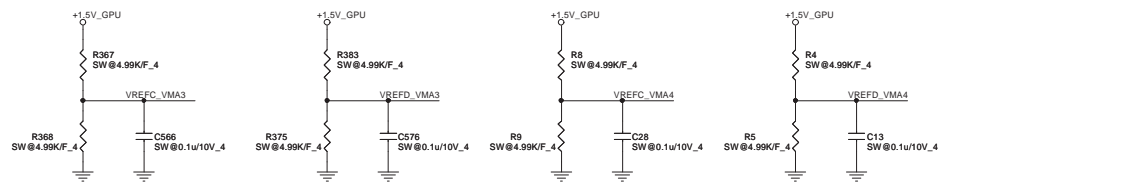
BOT Right

TOP Right

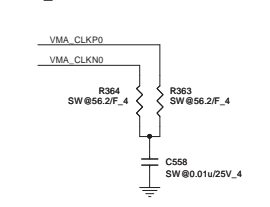
Group-A0 VREF



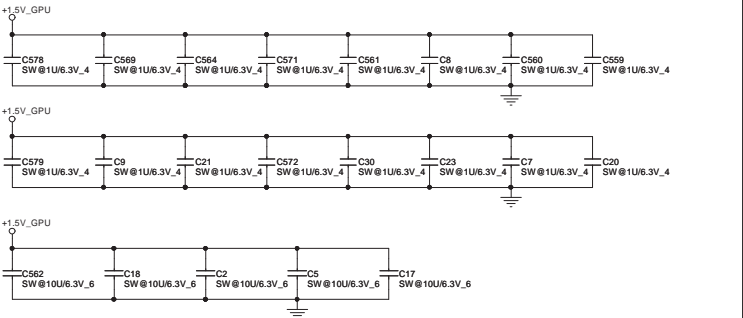
Group-A1 VREF



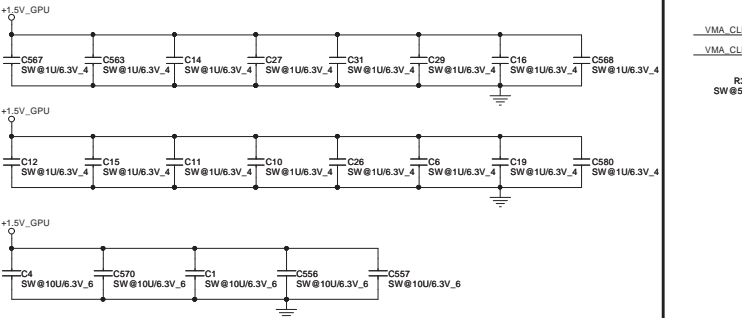
MEM_A0 CLK



Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

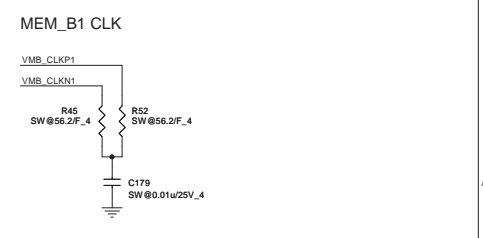
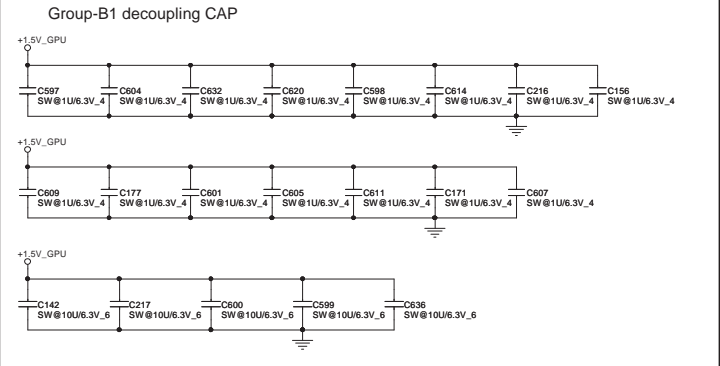
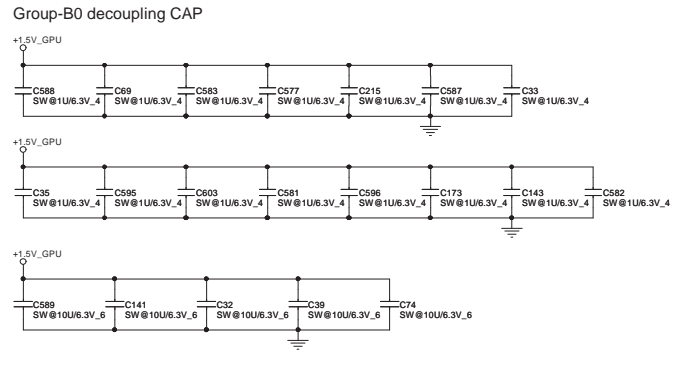
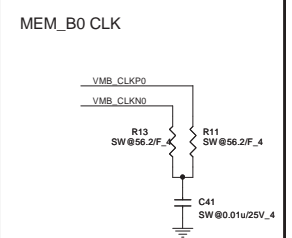
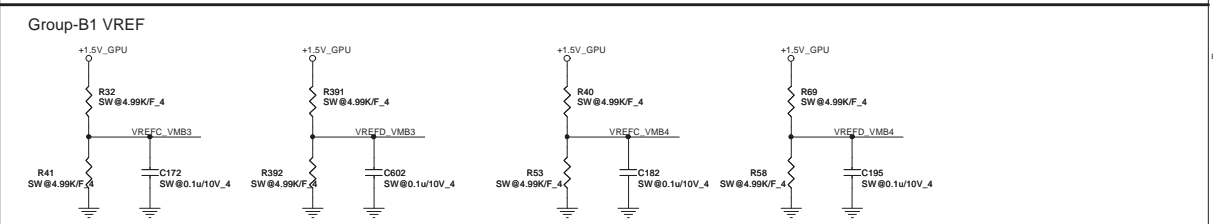
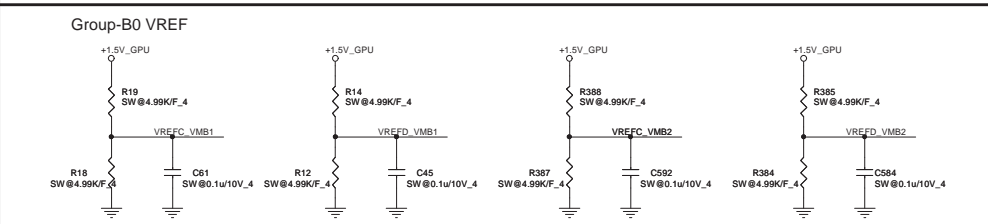
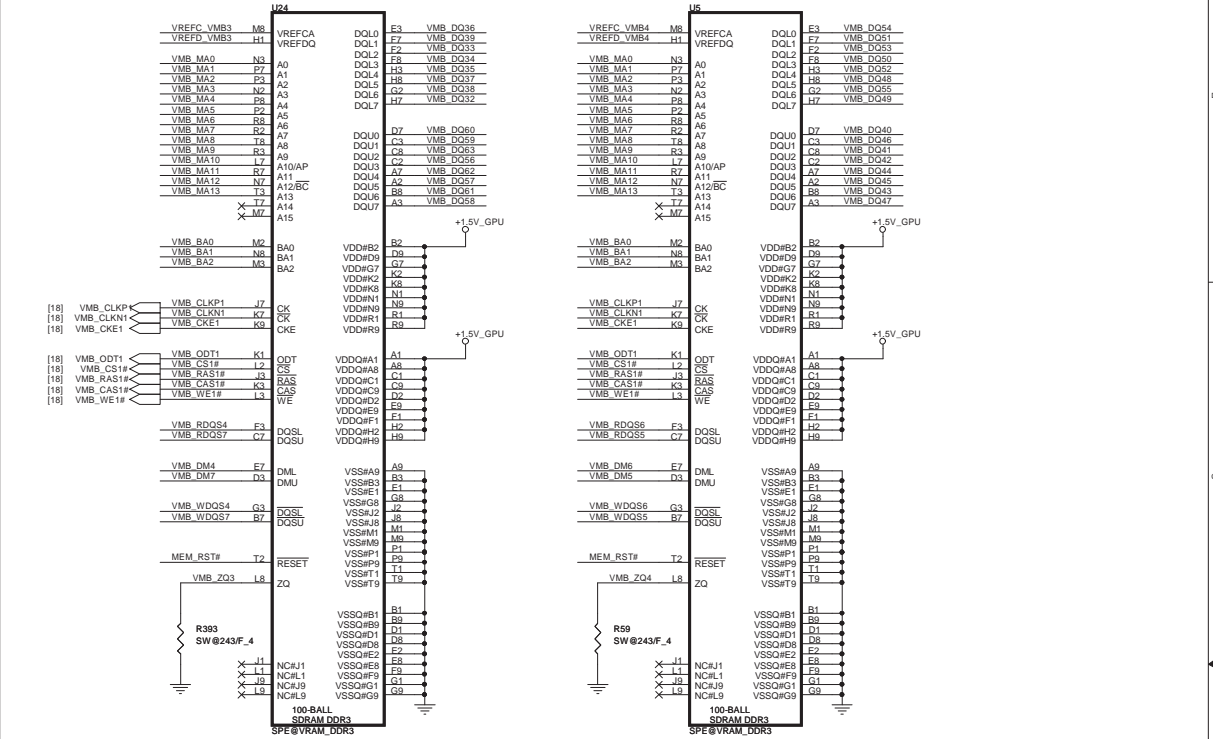
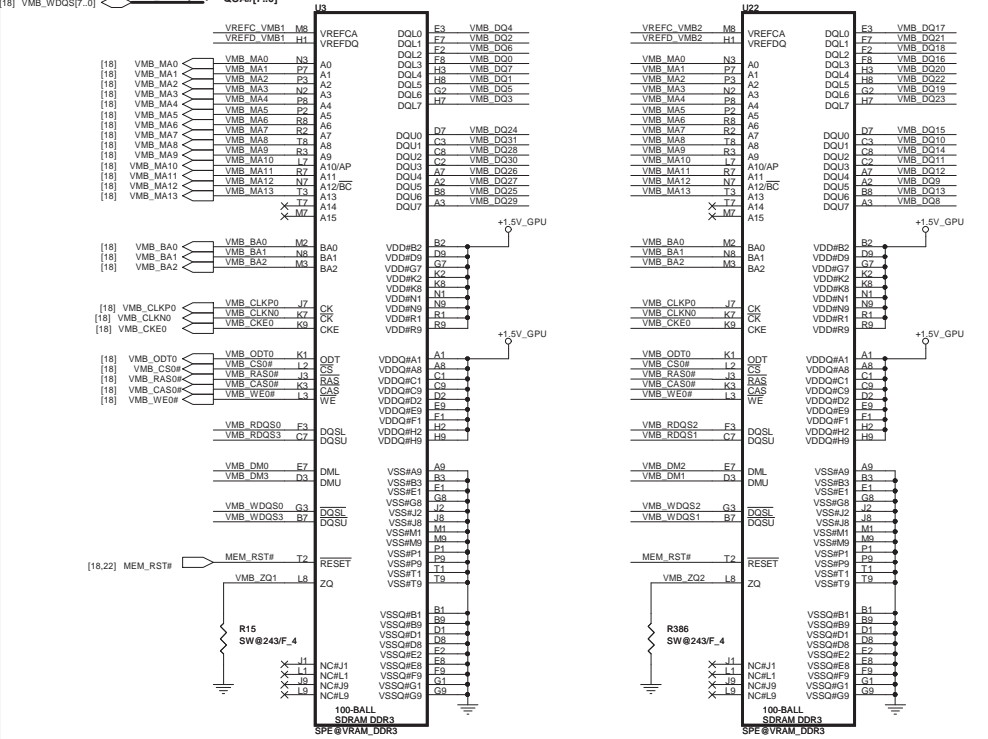


PROJECT : ZR8
Quanta Computer Inc.

Size: _____ Document Number: **MEMORY 1 channel A** Rev 1A
 Date: **Wednesday, May 27, 2009** Sheet 22 of 49

CHANNEL B: VREF, MEM, DR3 & CLK (16*4) net

- [18] VMB_DO[63..0] VMB_DO[63..0]
 - [18] VMB_DM[7..0] VMB_DM[7..0]
 - [18] VMB_RDQS[7..0] VMB_RDQS[7..0]
 - [18] VMB_WDQS[7..0] VMB_WDQS[7..0]
- QSA#[7..0]
- QSA#[7..0]

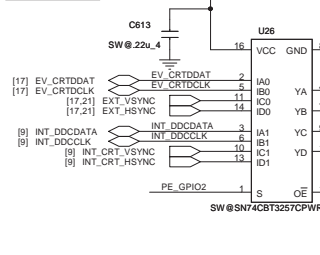
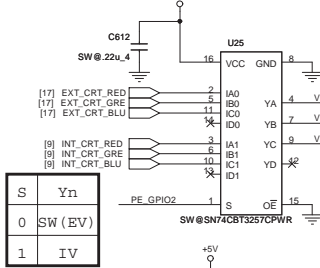


PROJECT : ZR8
Quanta Computer Inc.

Size: Document Number:
MEMORY 2 channel B

Date: Wednesday, May 27, 2009 Sheet 23 of 49

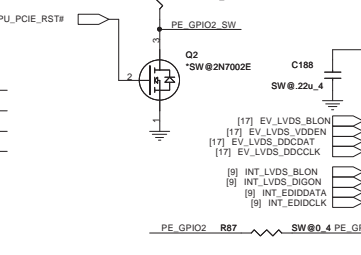
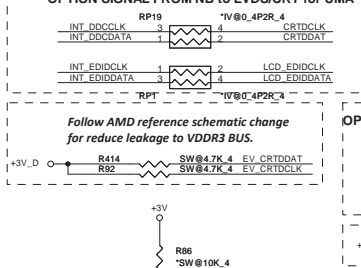
CRT



S	Yn
0	SW (EV)
1	IV

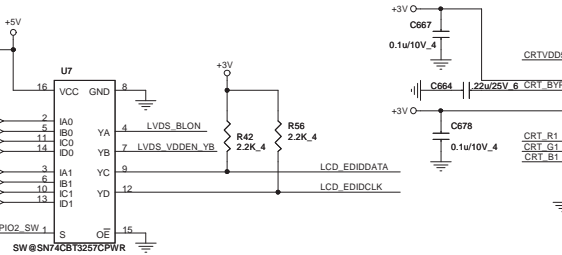
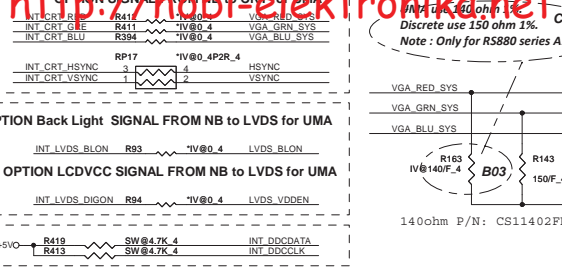
S	Yn
0	SW (EV)
1	IV

OPTION SIGNAL FROM NB to LVDS/CRT for UMA



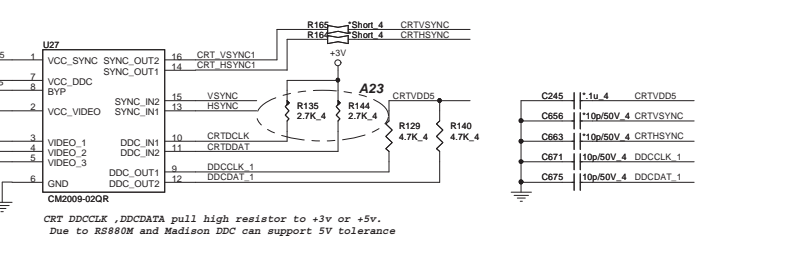
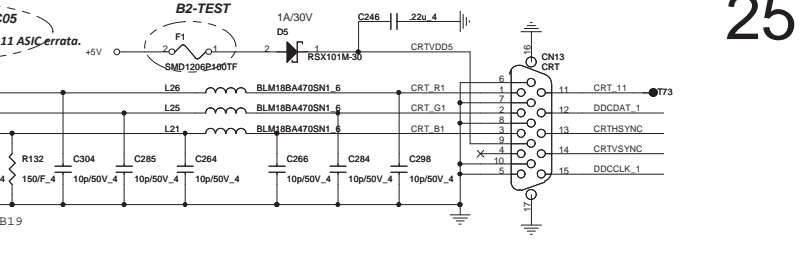
Follow AMD reference schematic change for reduce leakage to VDDR3 BUS.

OPTION SIGNAL FROM NB to CRT for UMA



OPTION Back Light SIGNAL FROM NB to LVDS for UMA
OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

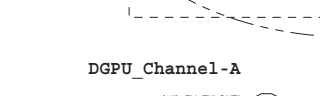
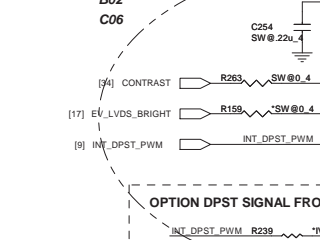
B2-TEST



Discrete use 150 ohm 1%. Note: Only for RS880 series A11 ASIC errata.

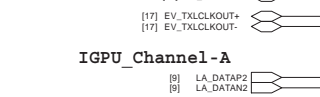
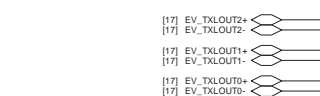
CRT DDCCLK, DDCDATA pull high resistor to +3V or +5V. Due to RS880M and Madison DDC can support 5V tolerance

A22 B02 C06

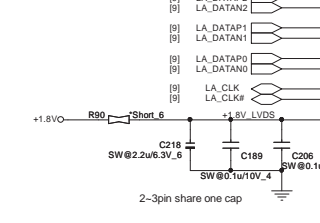


S	Yn
0	SW (EV)
1	IV

OPTION DPST SIGNAL FROM NB to LVDS for UMA



DGPU_Channel-A

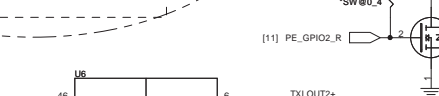
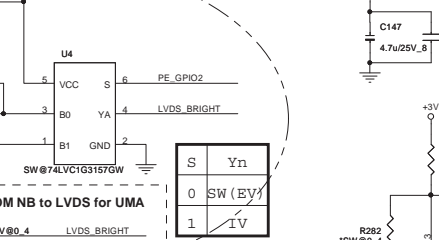


PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



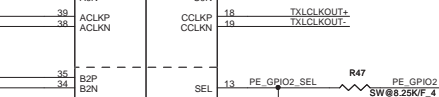
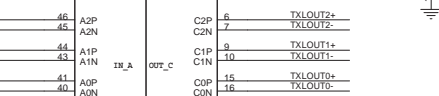
OPTION SIGNAL FROM NB to LVDS for UMA

A35

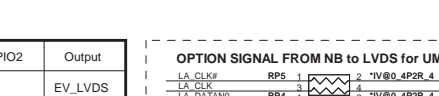
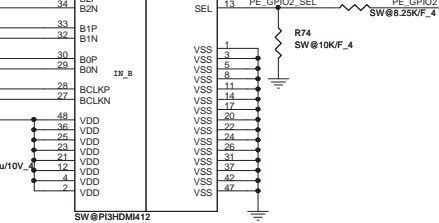


S	Yn
0	SW (EV)
1	IV

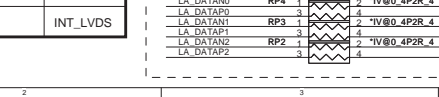
OPTION DPST SIGNAL FROM NB to LVDS for UMA



DGPU_Channel-A

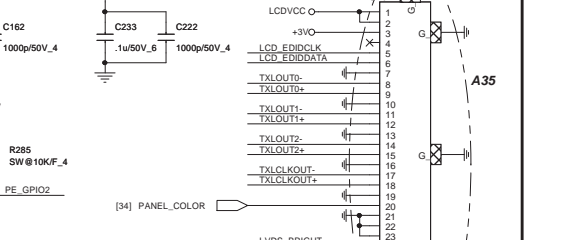


PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



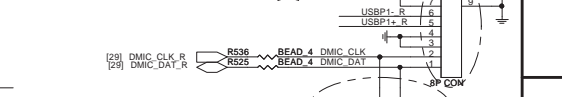
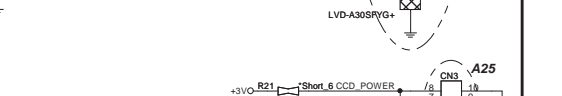
OPTION SIGNAL FROM NB to LVDS for UMA

A24

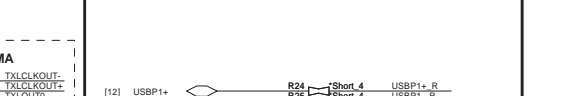
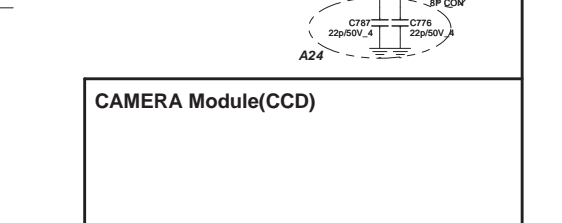


S	Yn
0	SW (EV)
1	IV

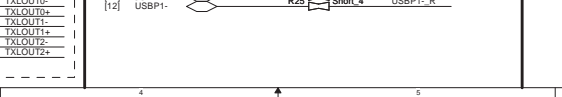
OPTION DPST SIGNAL FROM NB to LVDS for UMA



DGPU_Channel-A

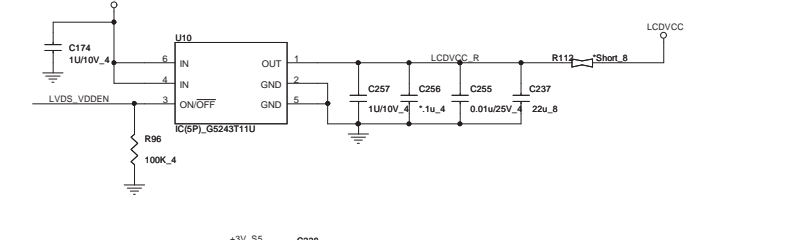


PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



OPTION SIGNAL FROM NB to LVDS for UMA

LCD Power

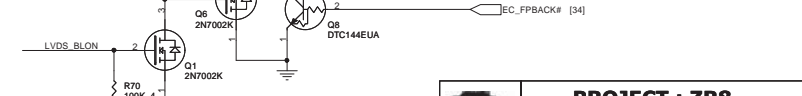
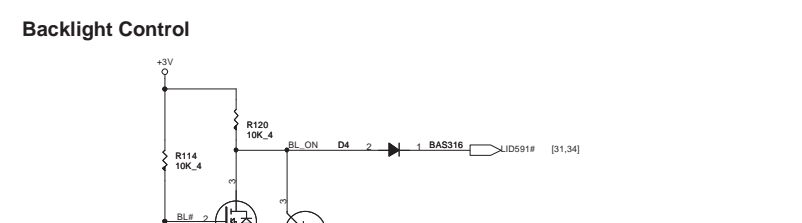


S	Yn
0	SW (EV)
1	IV

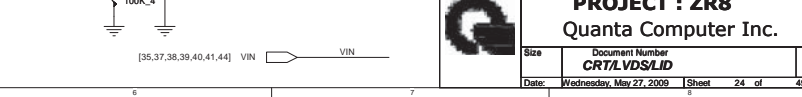
OPTION DPST SIGNAL FROM NB to LVDS for UMA



DGPU_Channel-A

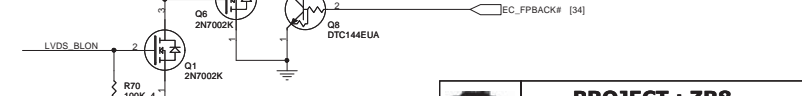
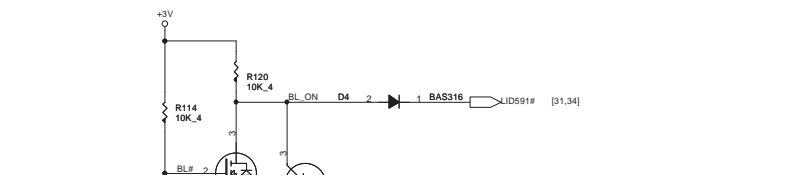


PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



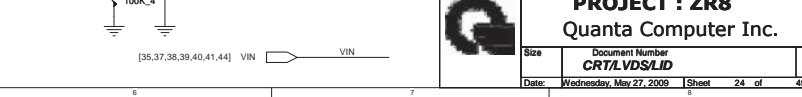
OPTION SIGNAL FROM NB to LVDS for UMA

Backlight Control



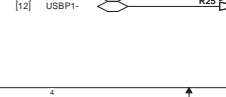
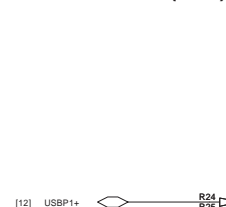
S	Yn
0	SW (EV)
1	IV

PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS

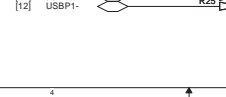


OPTION SIGNAL FROM NB to LVDS for UMA

CAMERA Module(CCD)



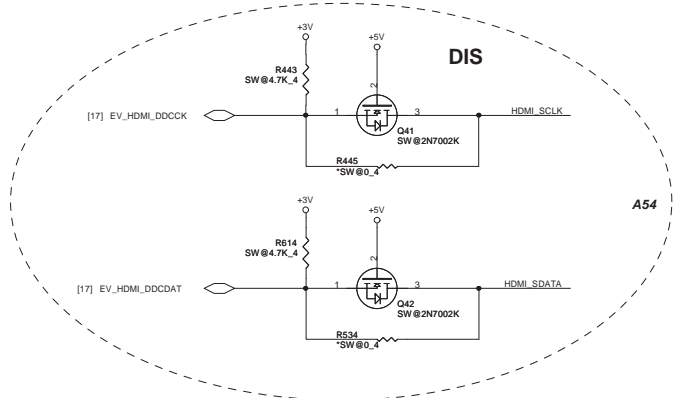
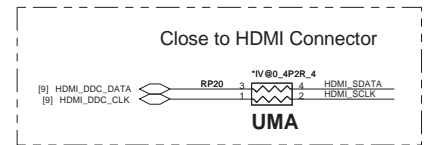
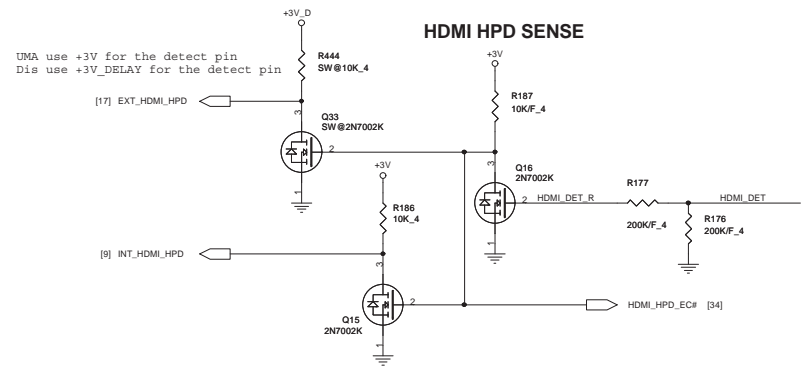
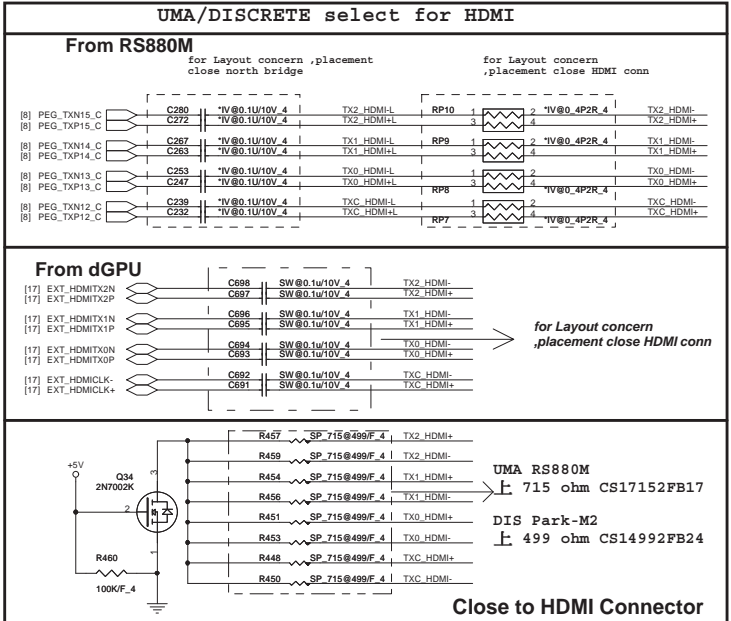
PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



OPTION SIGNAL FROM NB to LVDS for UMA

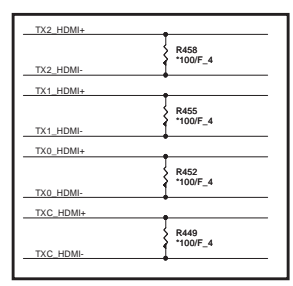
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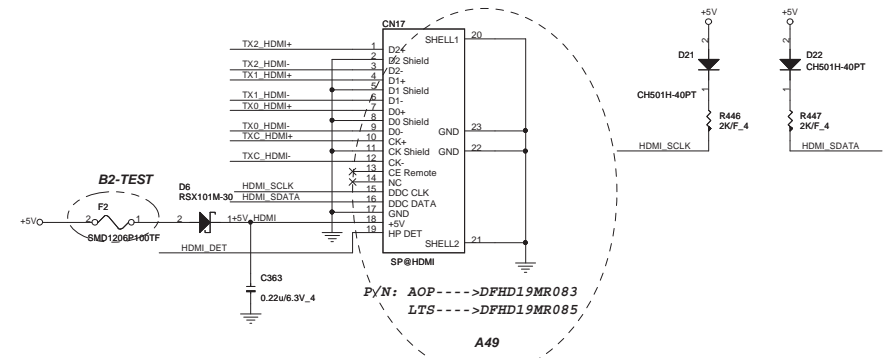


EMI reserve for HDMI(HDM)

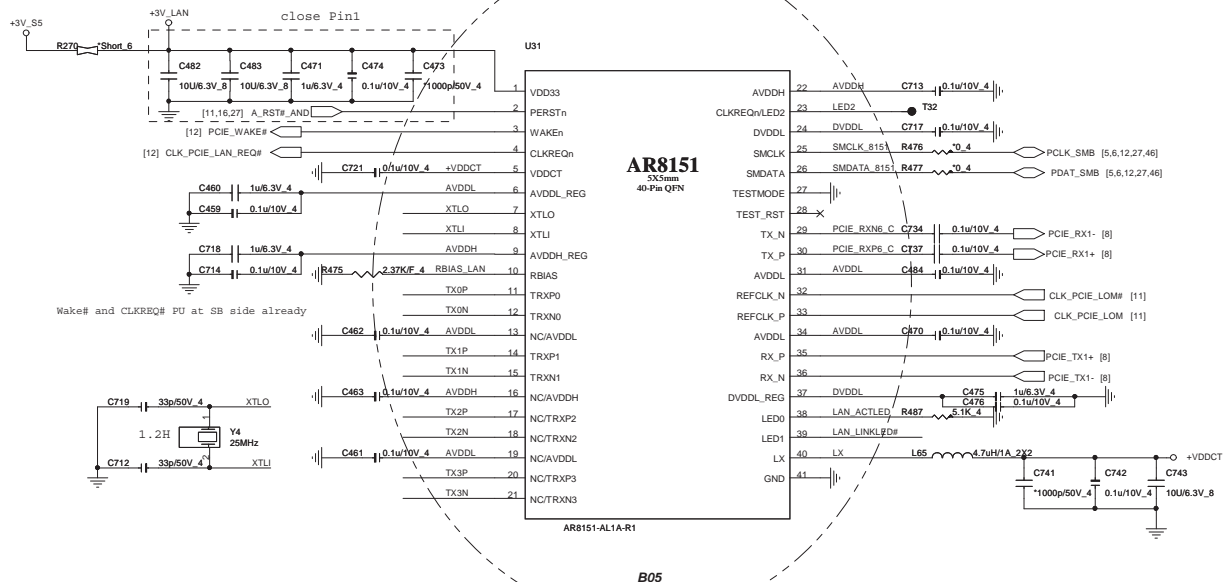
Close connector



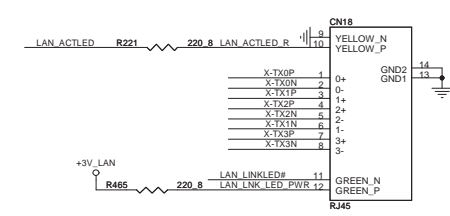
HDMI PORT



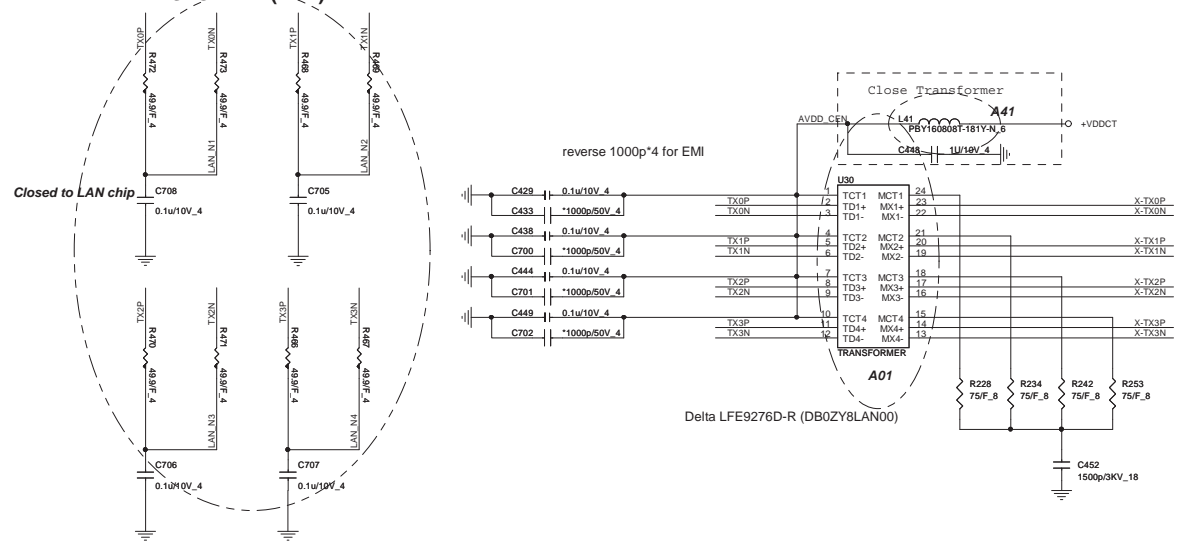
Giga-LAN AR8151



RJ45(LAN)

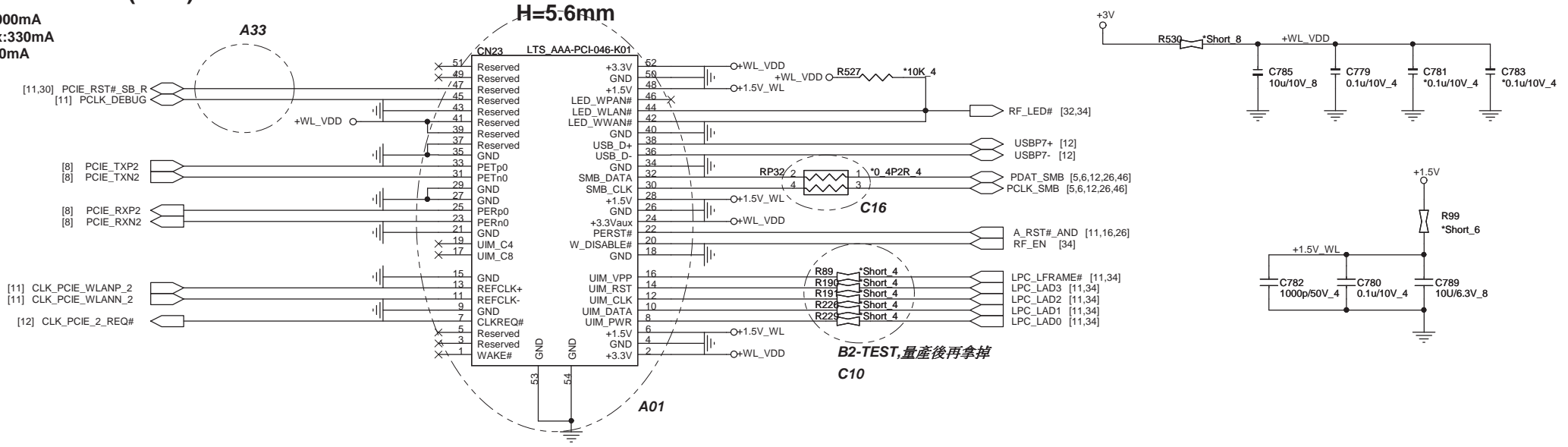


TRANSFORMER(LAN)



MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



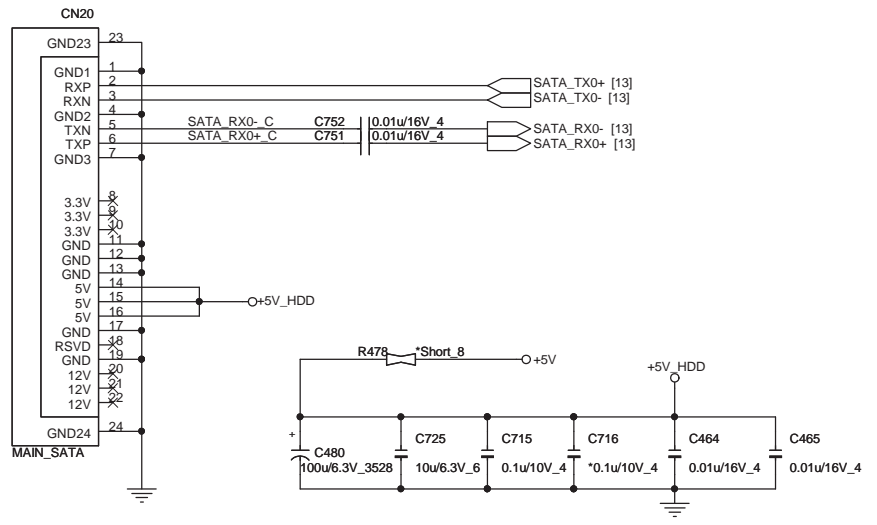
B2-TEST, 量產後再拿掉
C10



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Quanta Computer Inc.

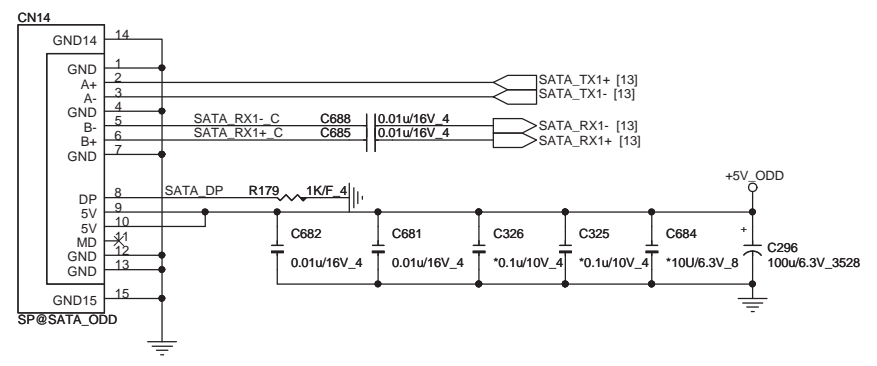
Size	Document Number	Rev
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SATA HDD(HDD)



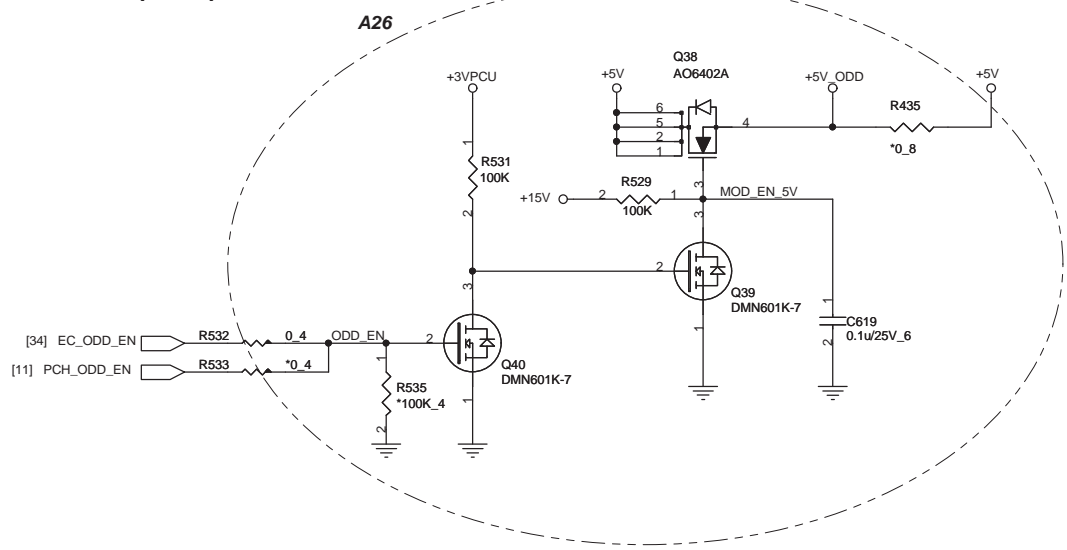
HOLE(OTH)

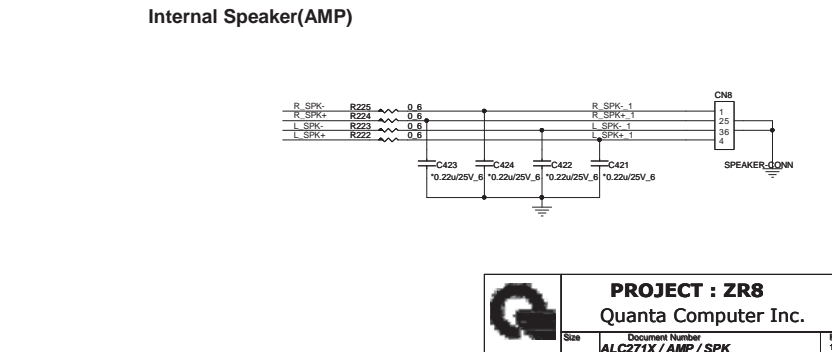
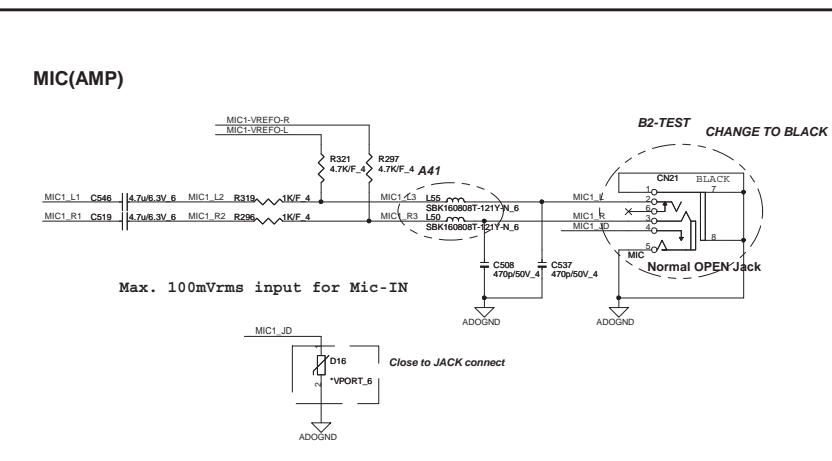
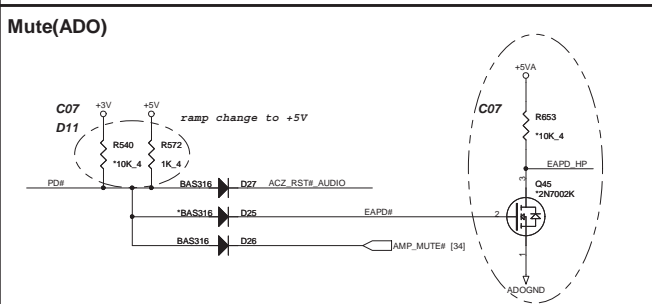
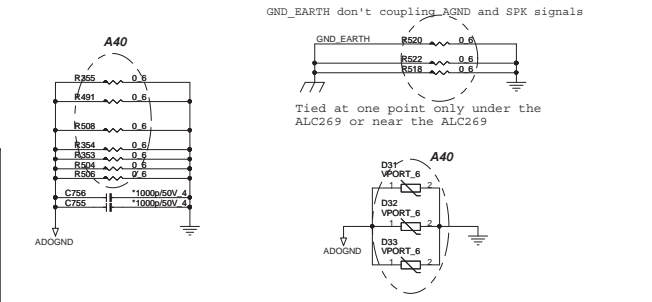
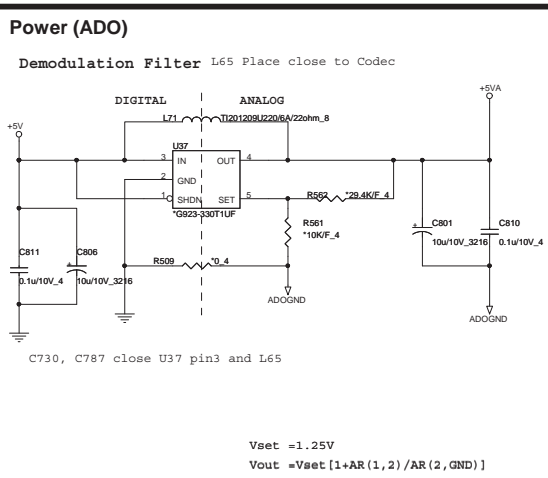
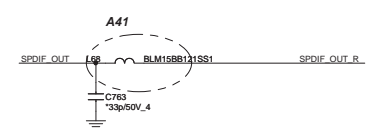
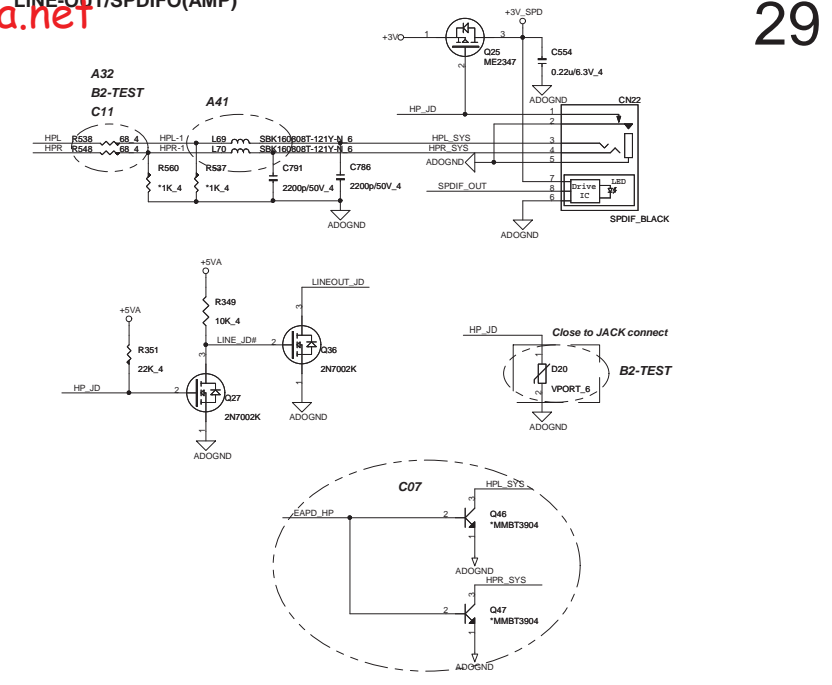
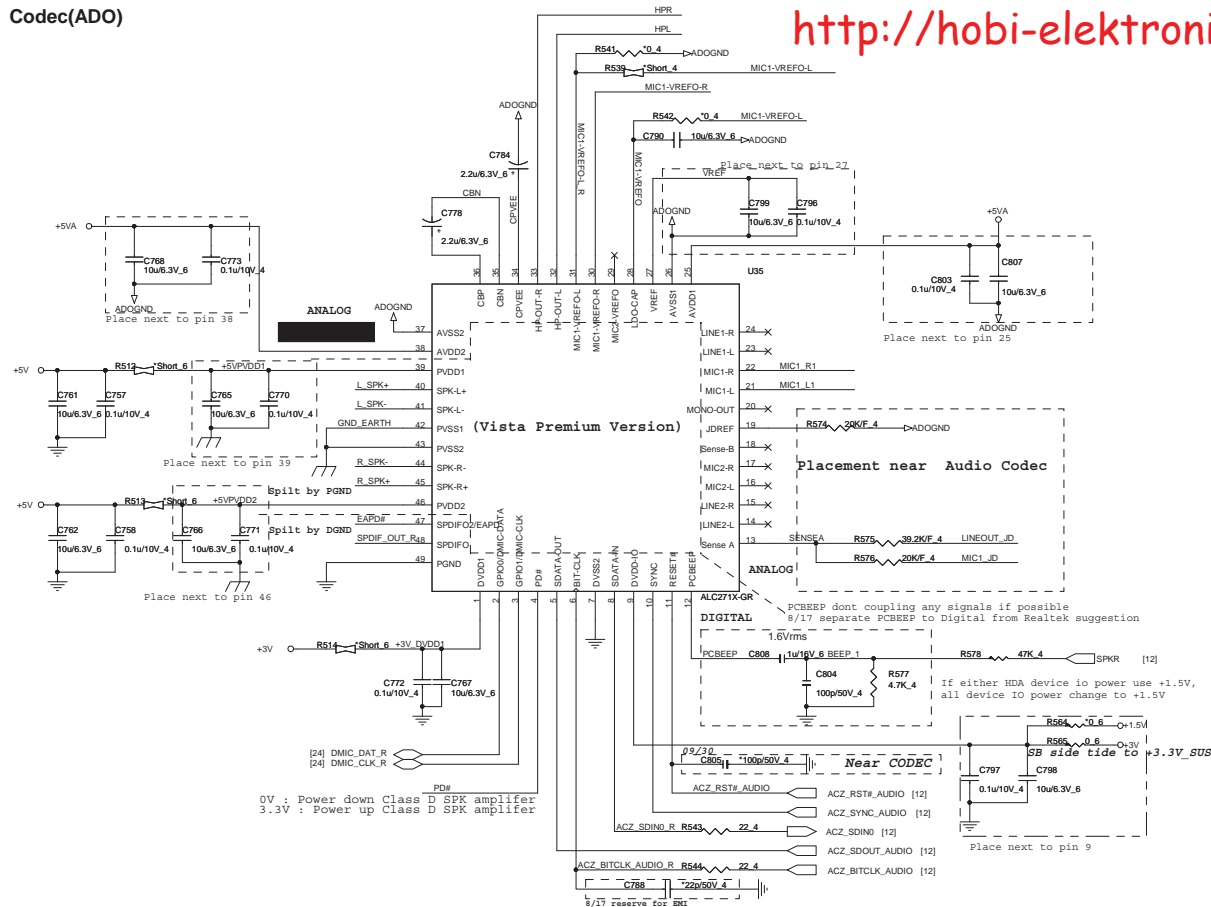
SATA ODD(ODD)



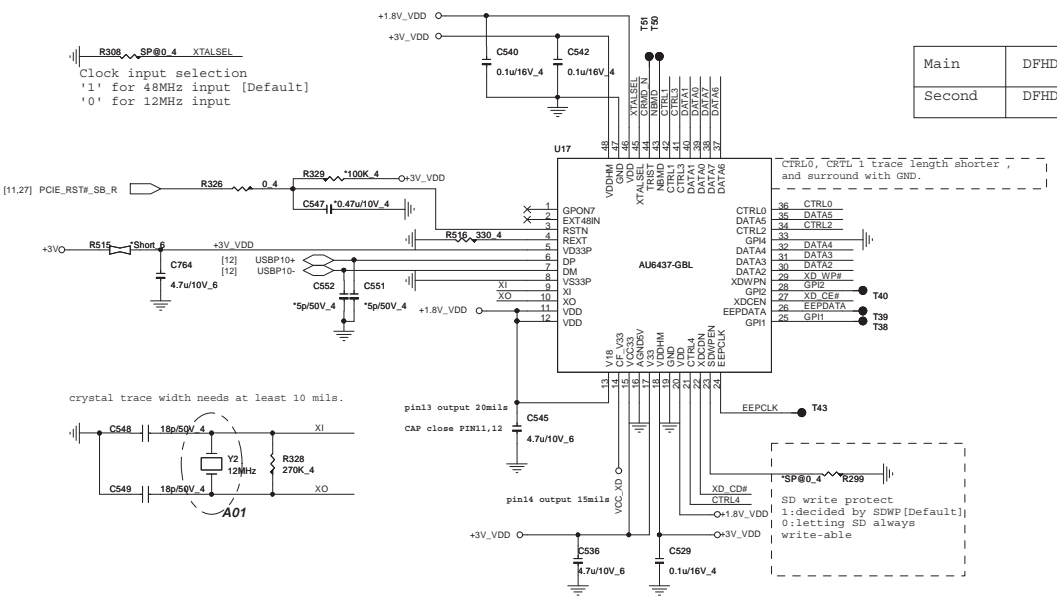
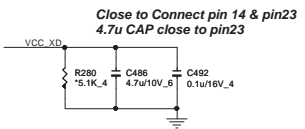
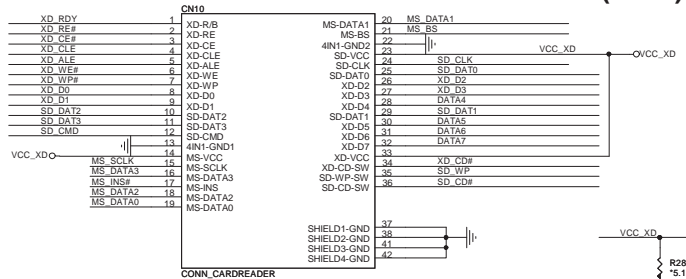
JM51 (2-DIMM) -->CN14 P/N:DFHS13FR075
 JV51 (3-DIMM) -->CN14 P/N:DFHS13FR017
 DFHS13FR022
 DFHS13FR005
 DFHS13FR006

ODD POWER(ODD)

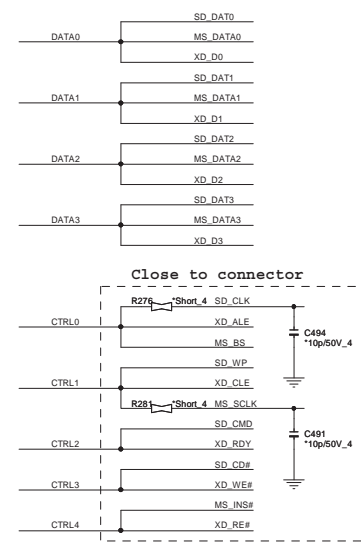




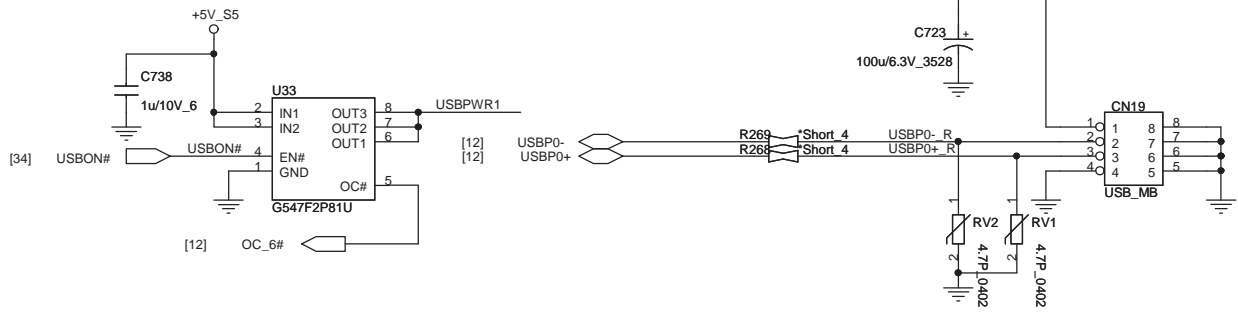
4 IN 1 CARD READER (MMC)



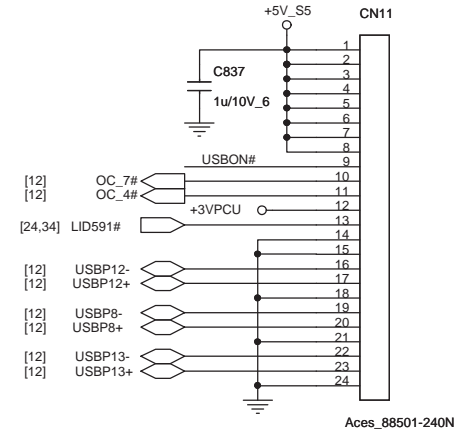
Main	DFHD36MS006
Second	DFHD36MS012



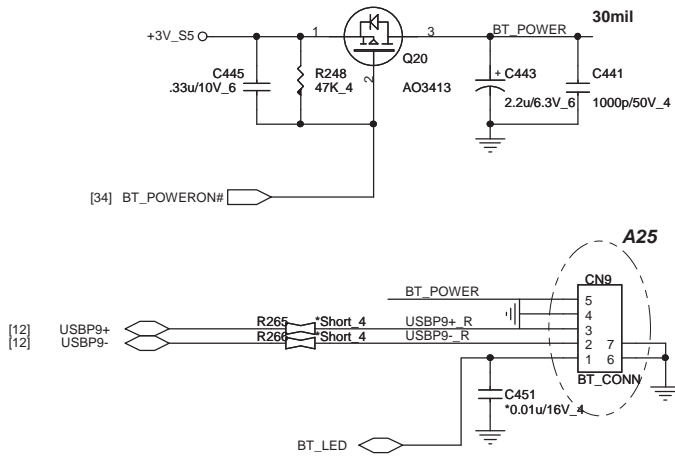
USB PORT(USB)



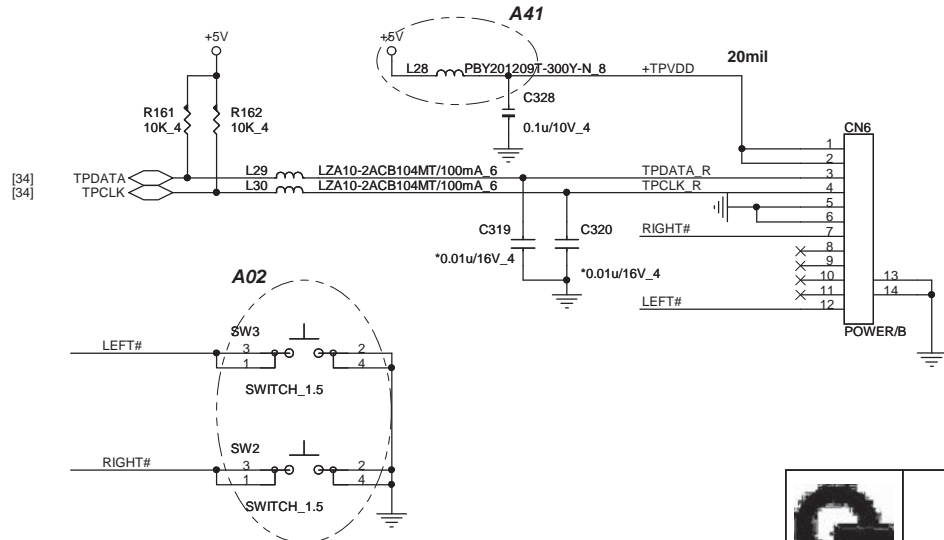
USB BOARD CONN(USB)



BLUETOOTH CONN(BTM)



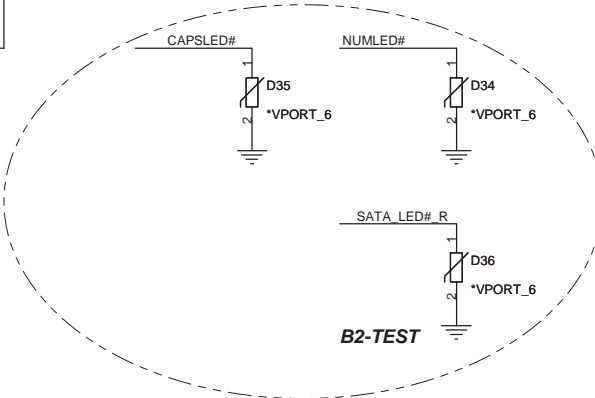
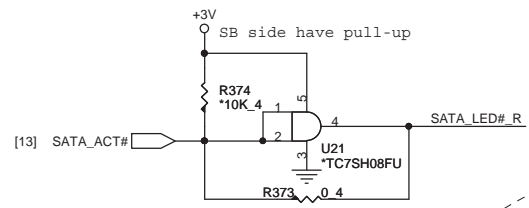
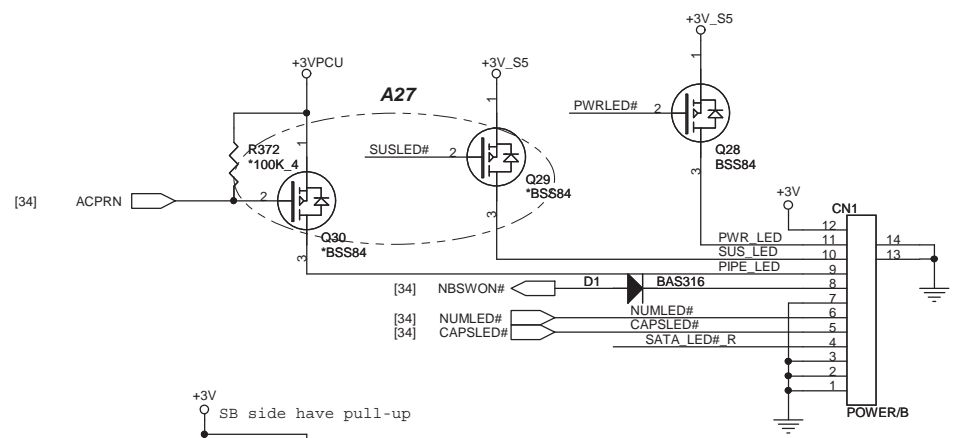
TOUCHPAD BOARD CONN(TPD)



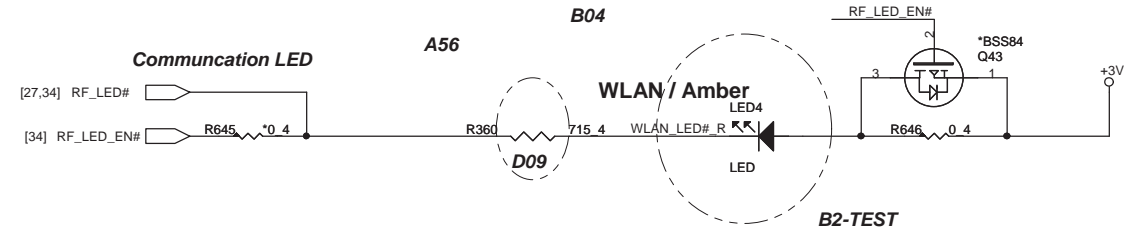
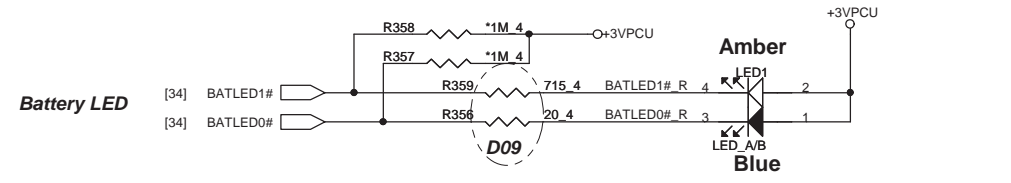
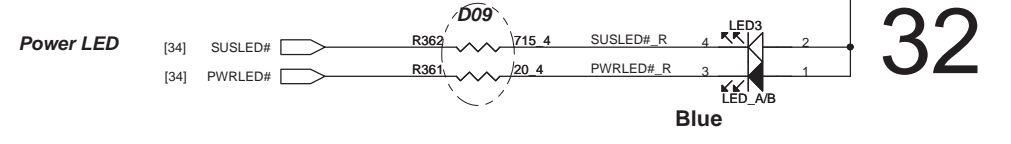
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 Quanta Computer Inc.

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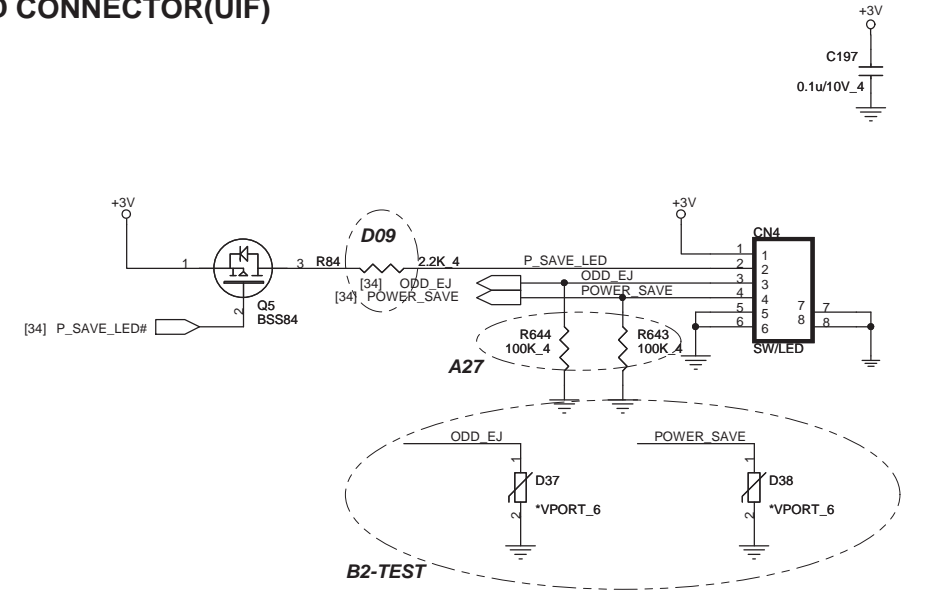
POWER BOARD CONN(UIF)



LED BOARD CONN(UIF)

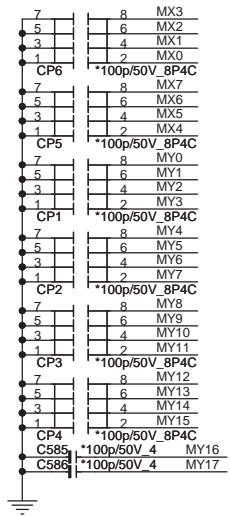


LED BOARD CONNECTOR(UIF)

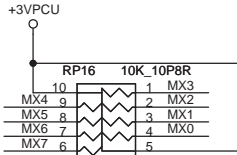
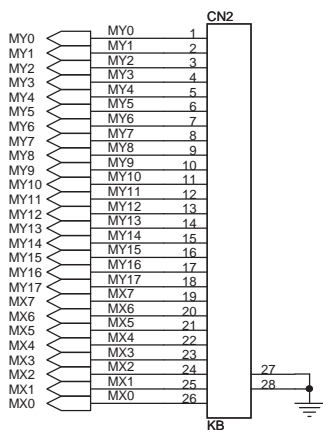


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Quanta Computer Inc.

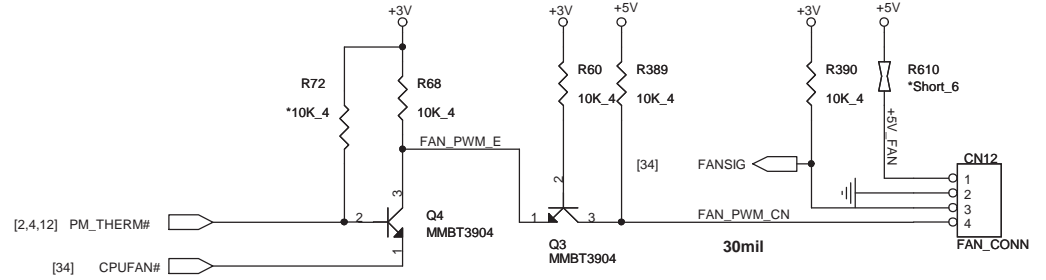
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[34] MY0
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[34] MY2
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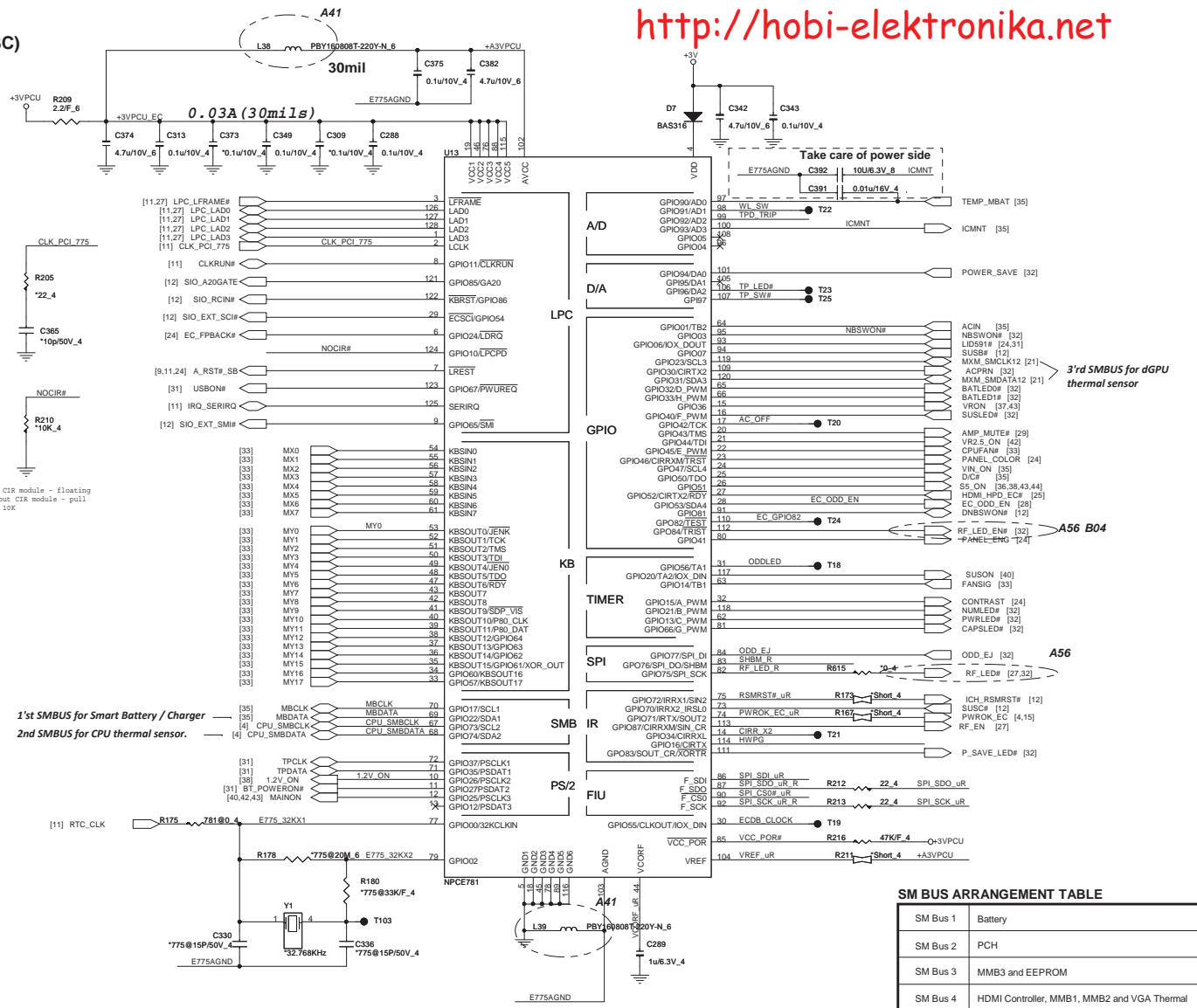
CPU FAN(THM)



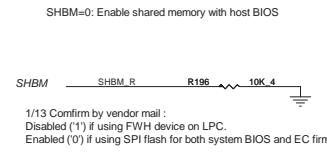
PROJECT : ZR8
Quanta Computer Inc.

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	KB/FAN/EE RETURN CAP	1A
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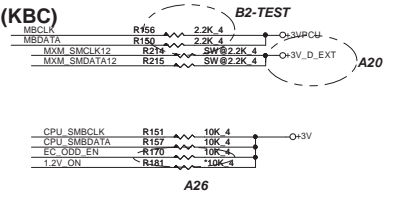
EC(KBC)



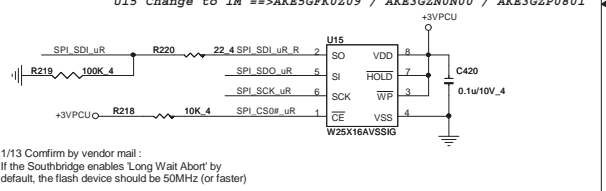
I/O ADDRESS SETTING(KBC)



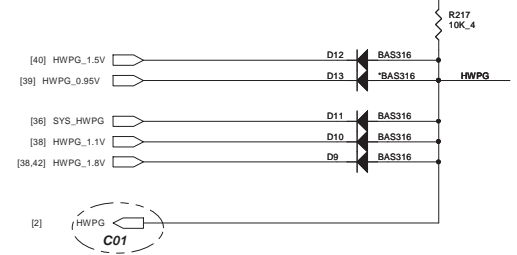
SM BUS PU(KBC)



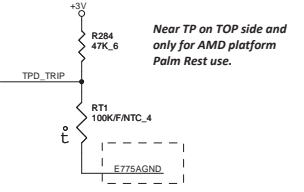
SPI FLASH(KBC)



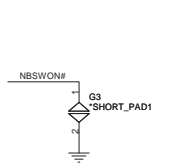
HWPG(KBC)



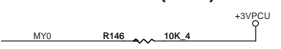
Palm Rest Thermal Sensor(THM)

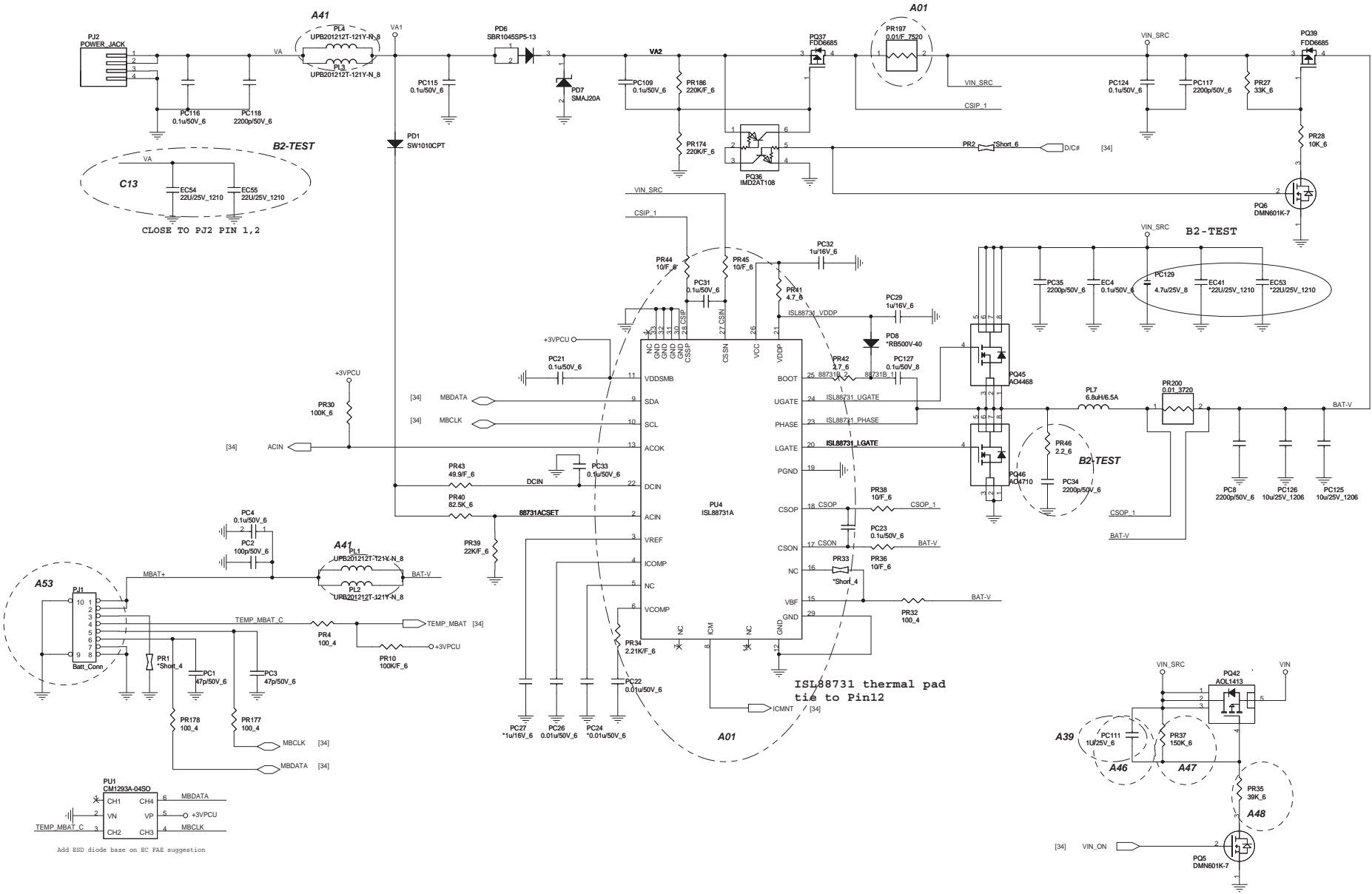


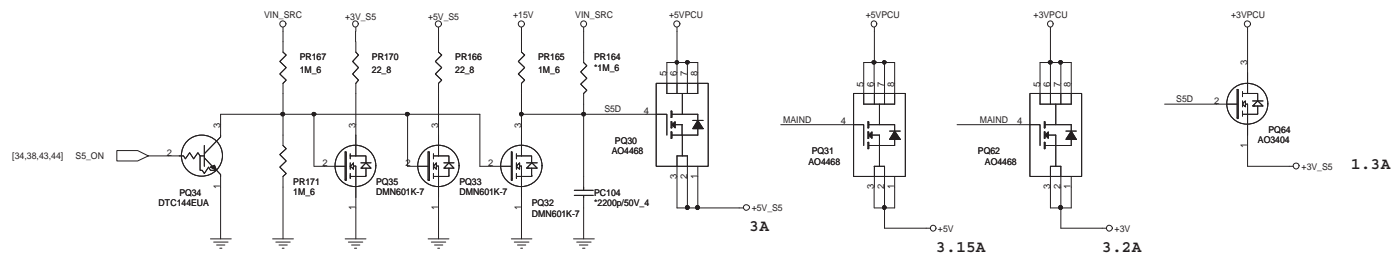
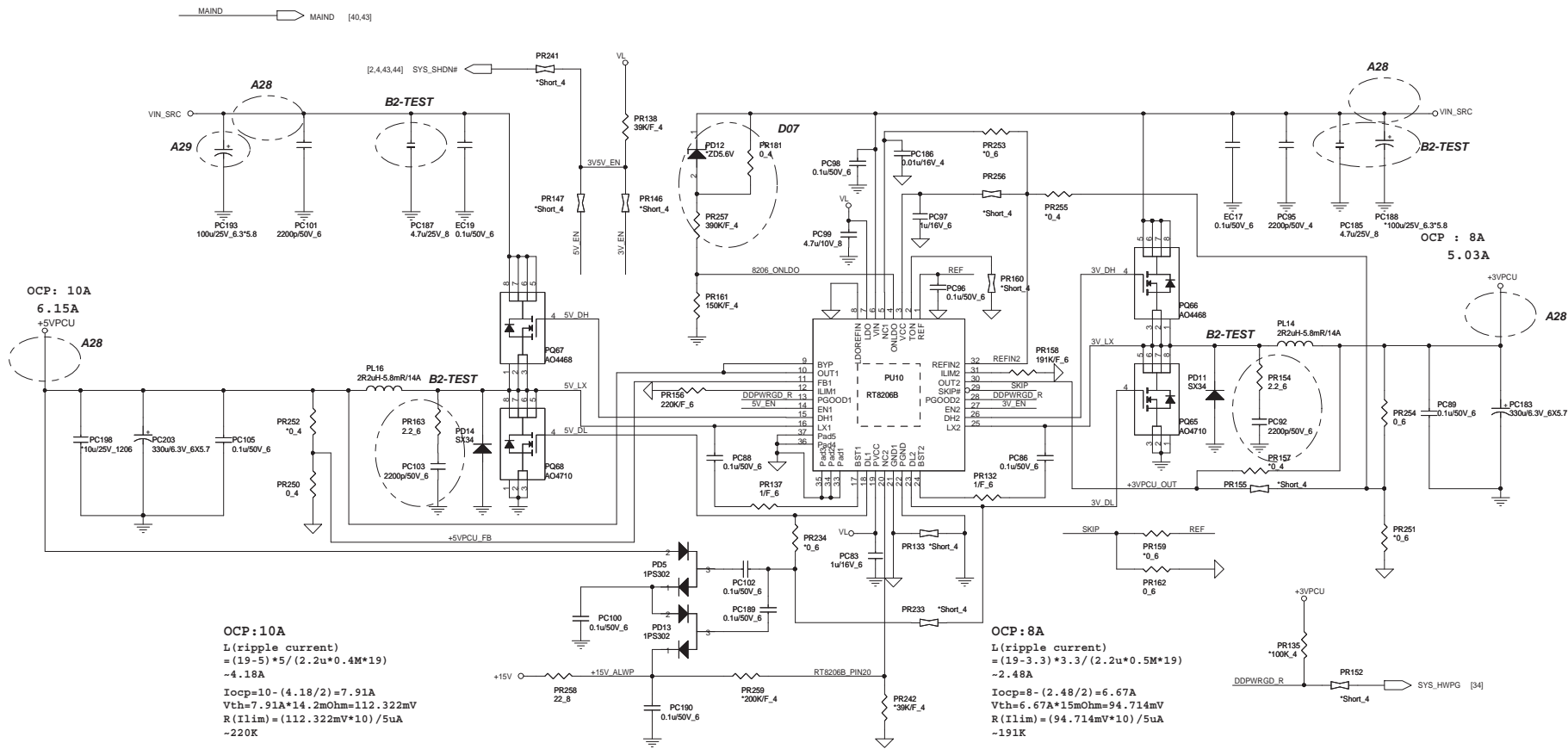
POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)







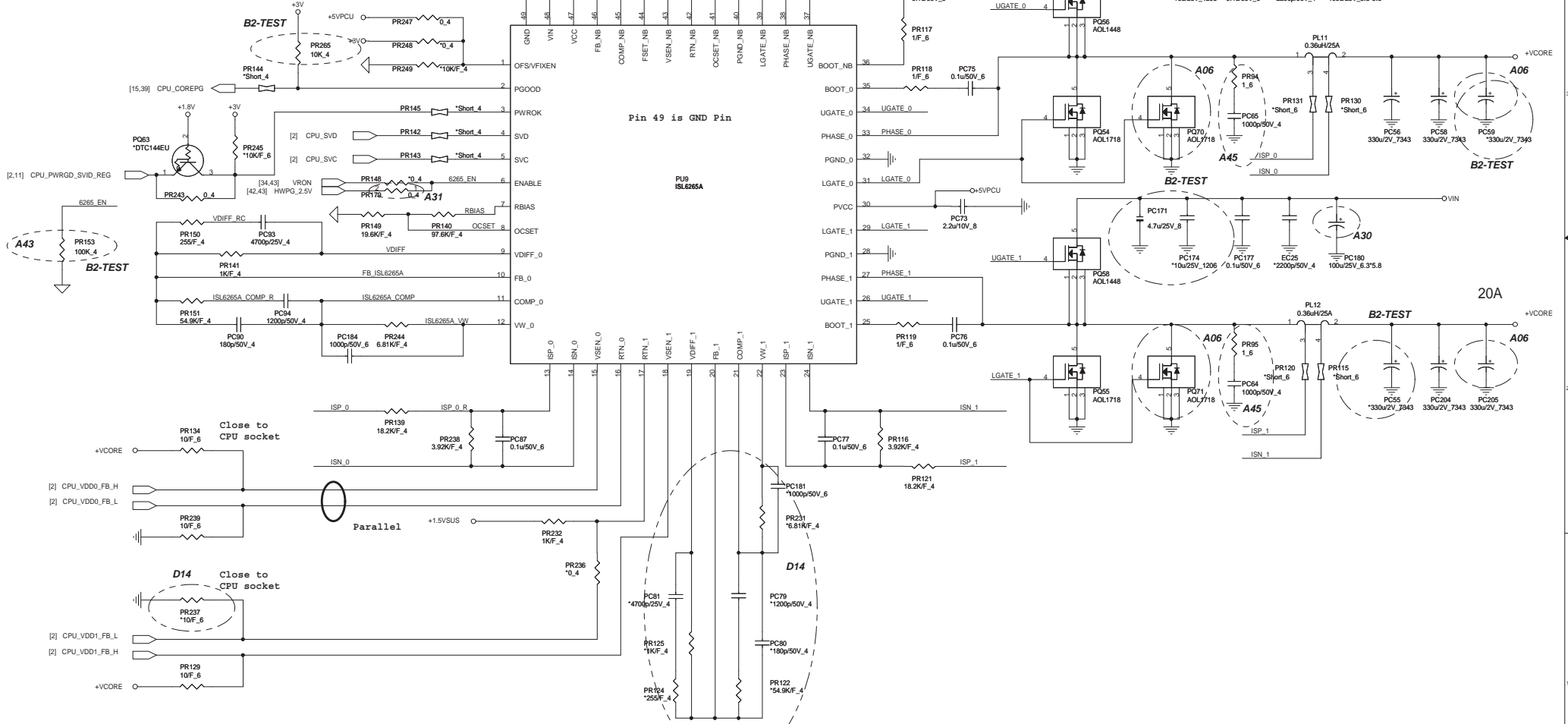
OFS/VFIXEN	Offset & Droop	SVC	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

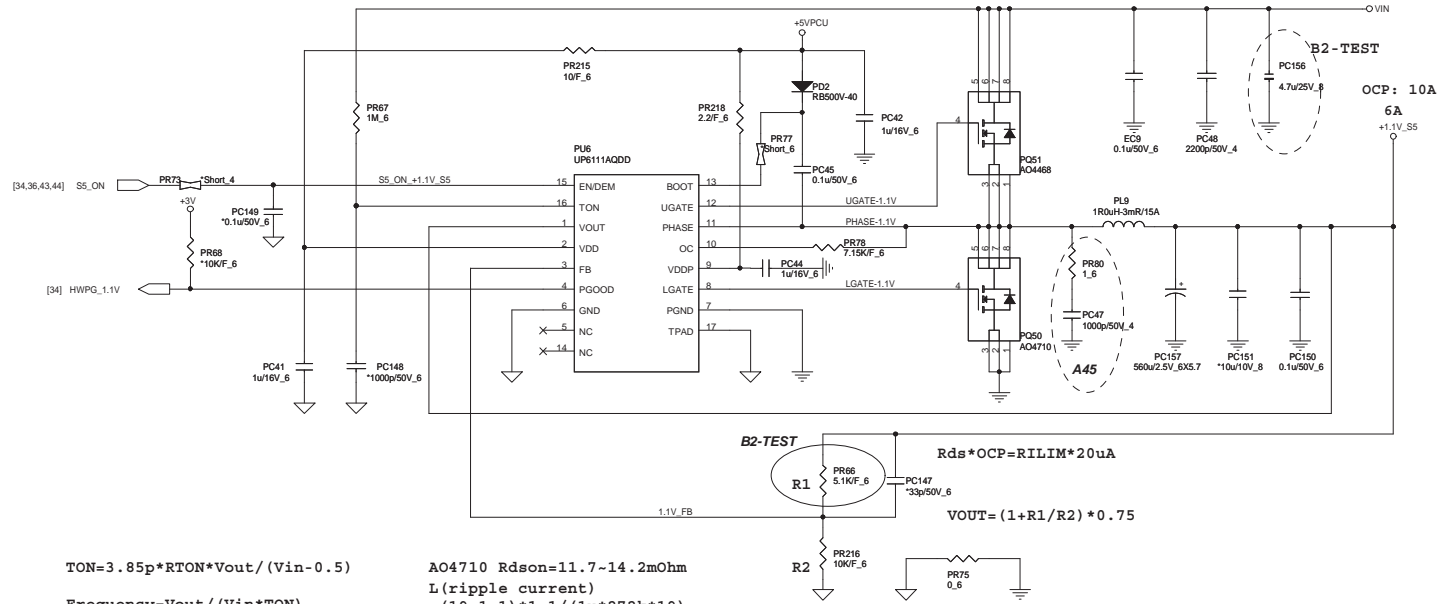
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

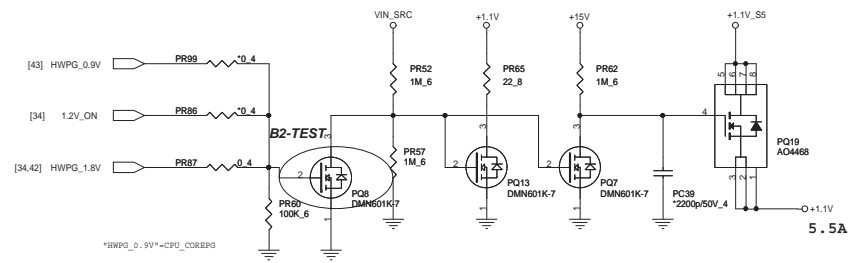
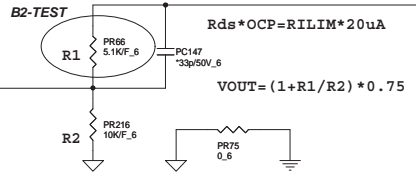


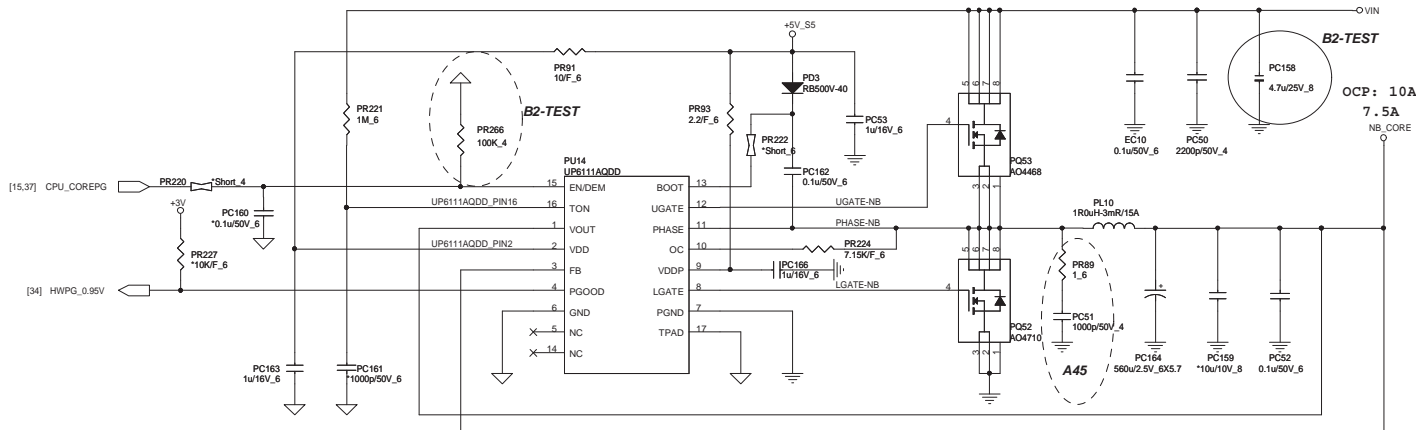
PROJECT : ZR8 Quanta Computer Inc.			
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CPU_CORE			



$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO4710 $R_{ds} = 11.7 - 14.2m\Omega$
 L (ripple current)
 $= (19 - 1.1) * 1.1 / (1u * 272k * 19)$
 $\sim 3.81A$
 $14.2m * 10 = RILIM * 20uA$
 $RILIM = 7.1K - 7.15K$



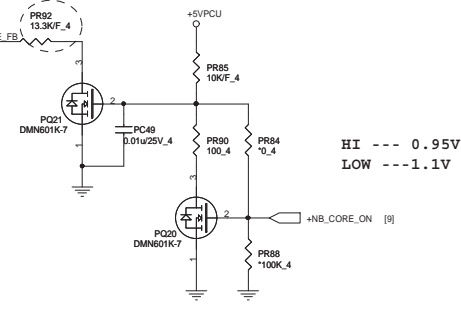


$V_{OUT} = (1 + R1/R2) * 0.75$

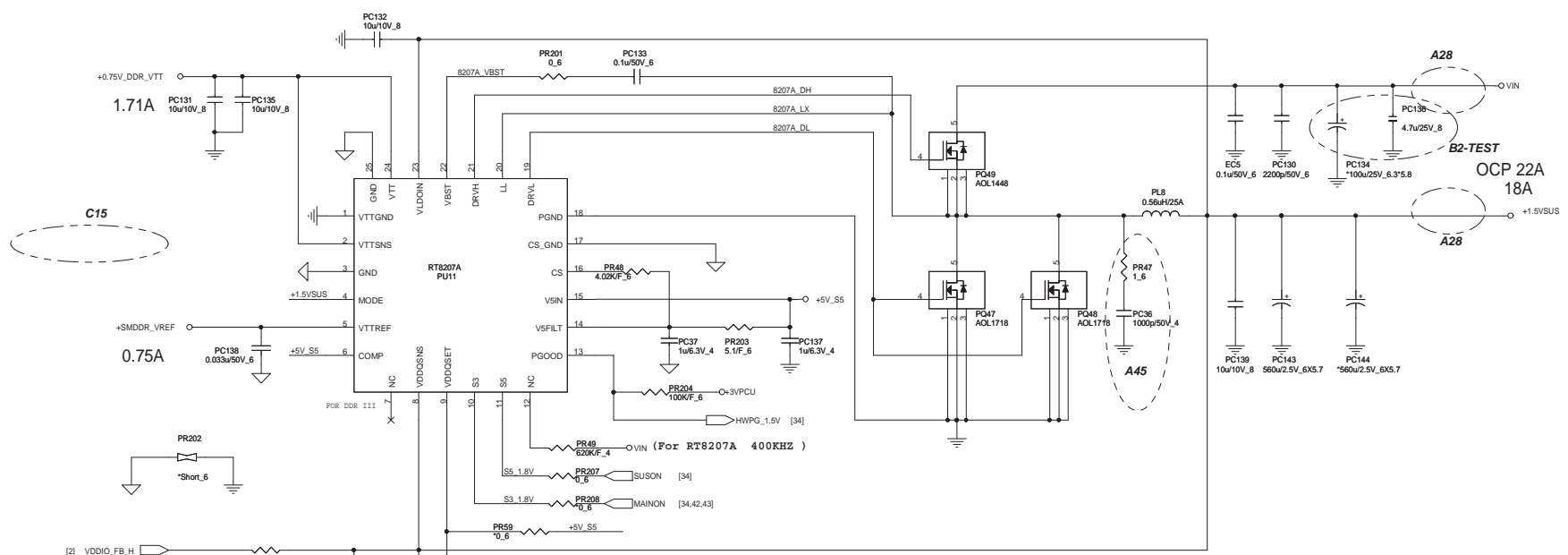
$R_{ds} * OCP = RILIM * 20\mu A$

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO4710 $R_{dson} = 11.7 \sim 14.2m\Omega$
 L (ripple current)
 $= (19 - 1.05) * 1.05 / (1u * 272k * 19)$
 $\sim 3.646\mu A$
 $14.2m * 10 = RILIM * 20\mu A$
 $RILIM = 7.1K \sim 7.15K$

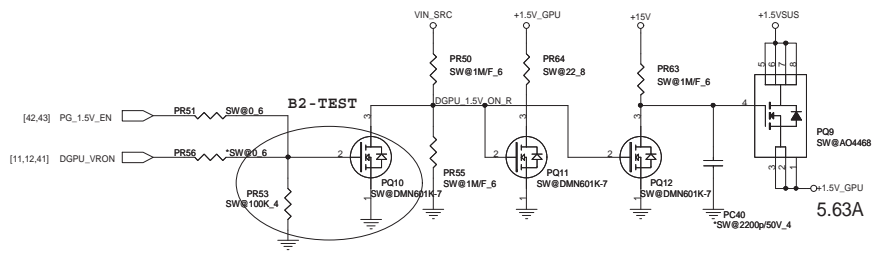
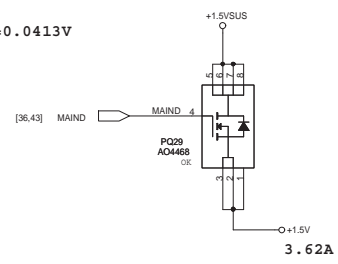


HI --- 0.95V
 LOW --- 1.1V



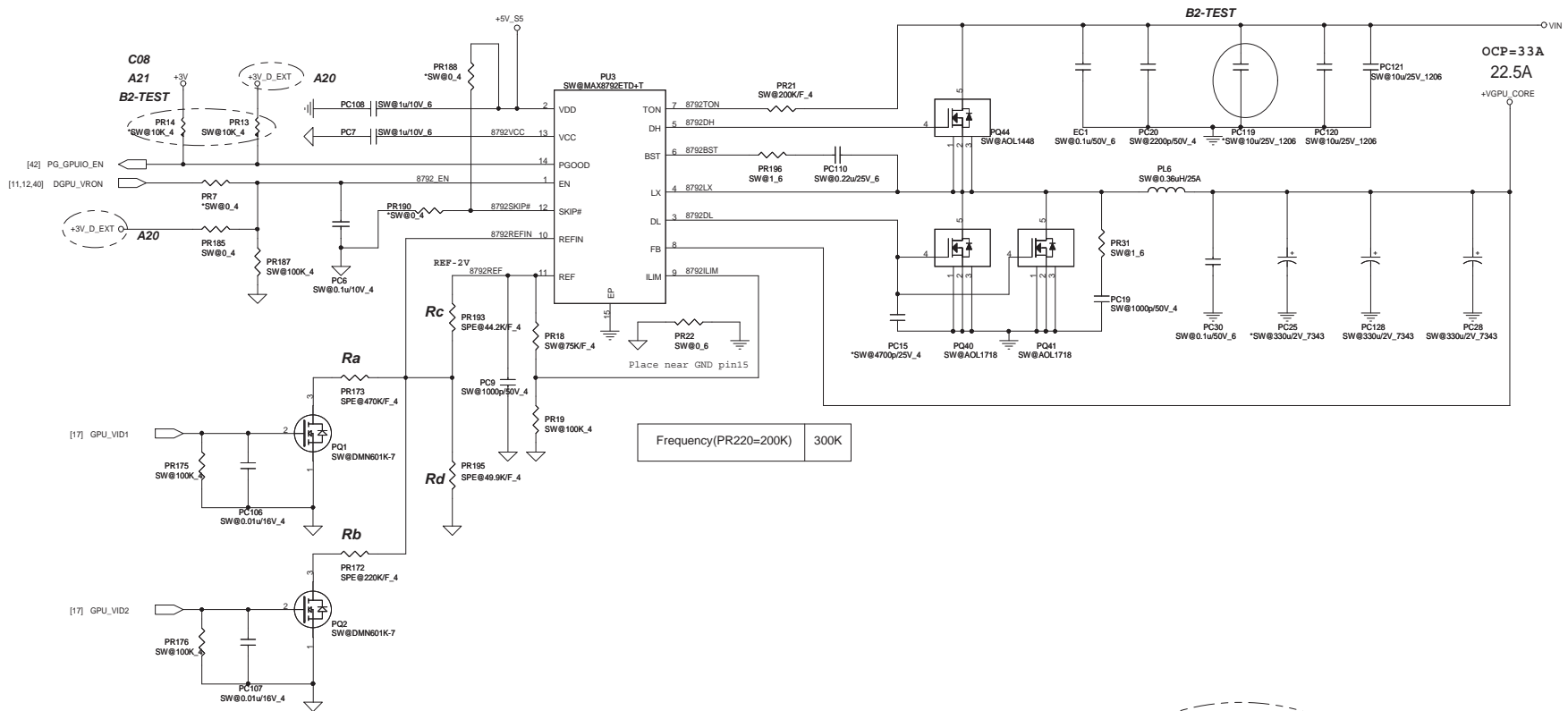
$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1718 $R_{dson} = 3.8 - 4.3 m\Omega$
 L (ripple current)
 $= (9 - 1.5) \times 1.5 / (0.56 \mu \times 400k \times 9)$
 $\sim 5.58 \mu$
 $V_{trip} = (22 - 2.79) \times (4.3 m\Omega / 2) = 0.0413 V$
 $R_{LIM} = V_{trip} / 10 \mu A = 4.13 K$



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Frequency(PR220=200K) 300K

Madison -Pro

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

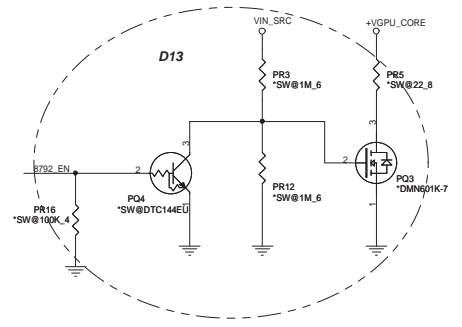
Ra	Rb	Rc	Rd	VREF
470K	220K	44.2K	49.9K	2V

Park -XT

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

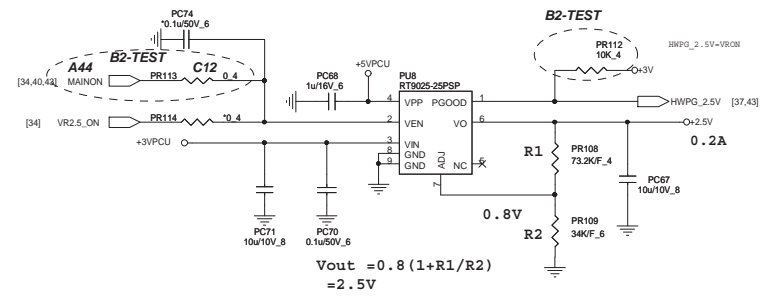
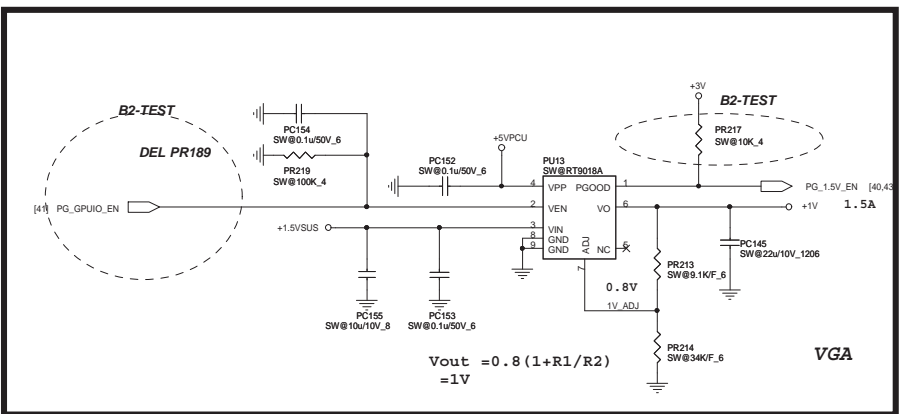
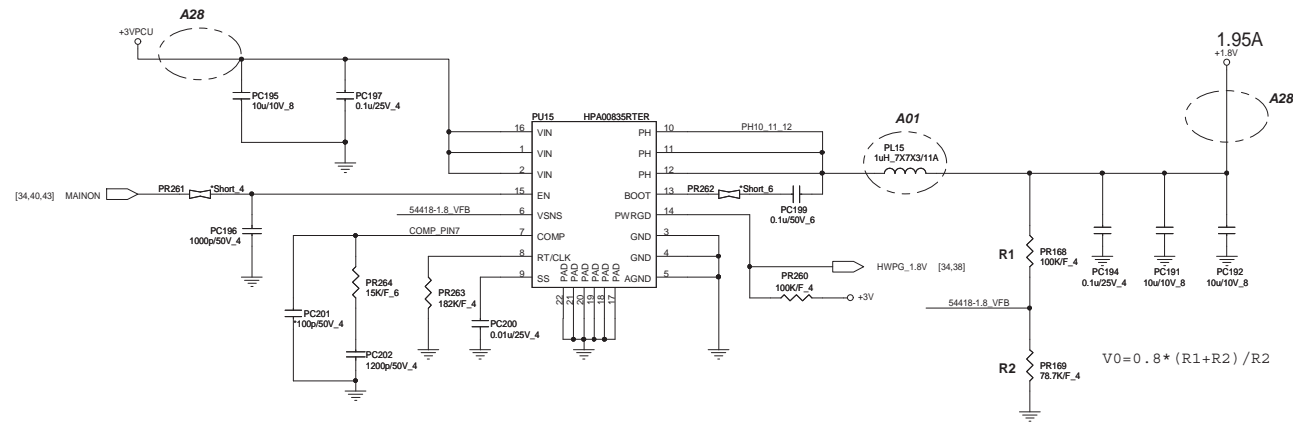
Ra	Rb	Rc	Rd	VREF
332K	130K	39.2K	49.9K	2V

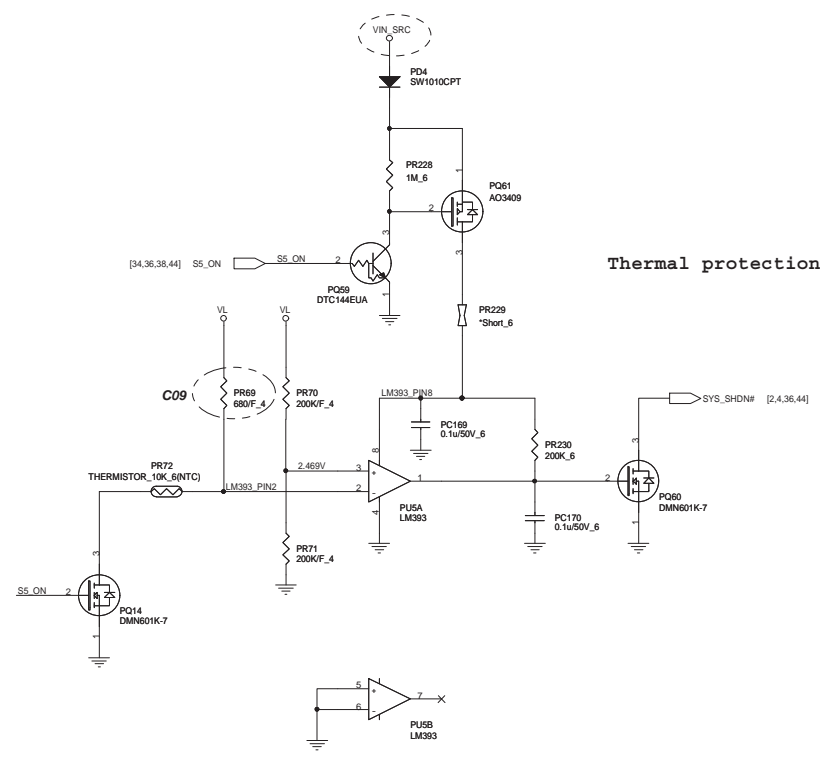
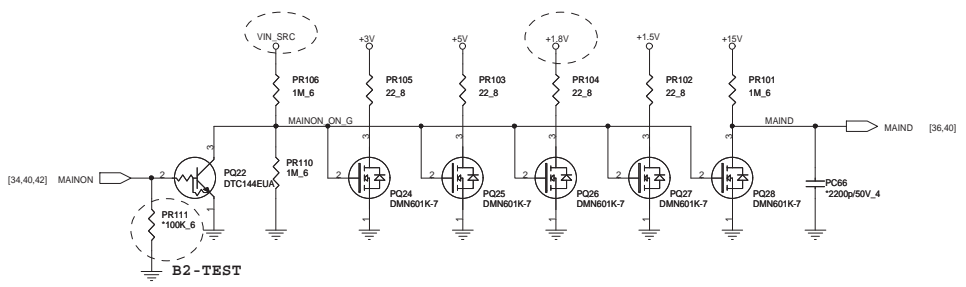
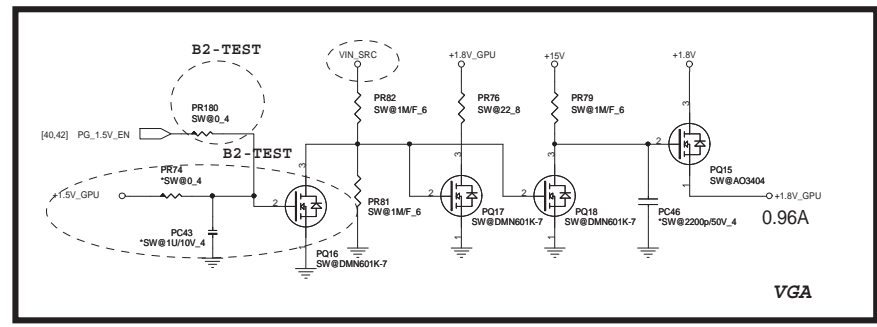
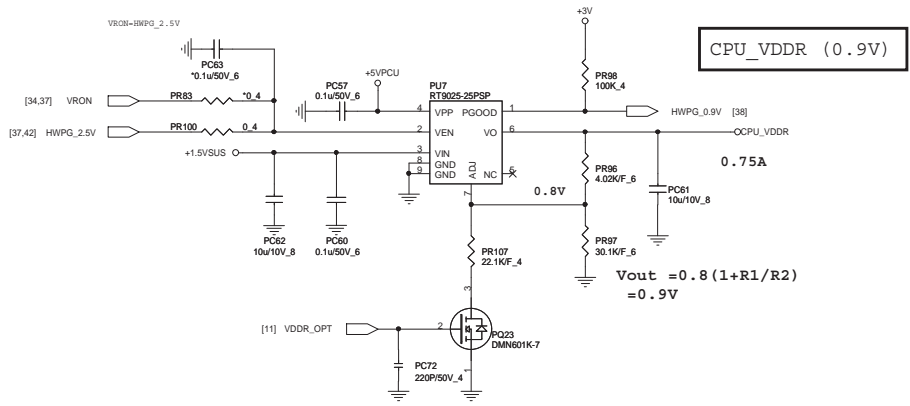
Rc --> 39.2K/F_4 (CS33922FB15)
 Ra --> 332K/F_4 (CS43322FB15)
 Rb --> 130K/F_4 (CS41302FB00)

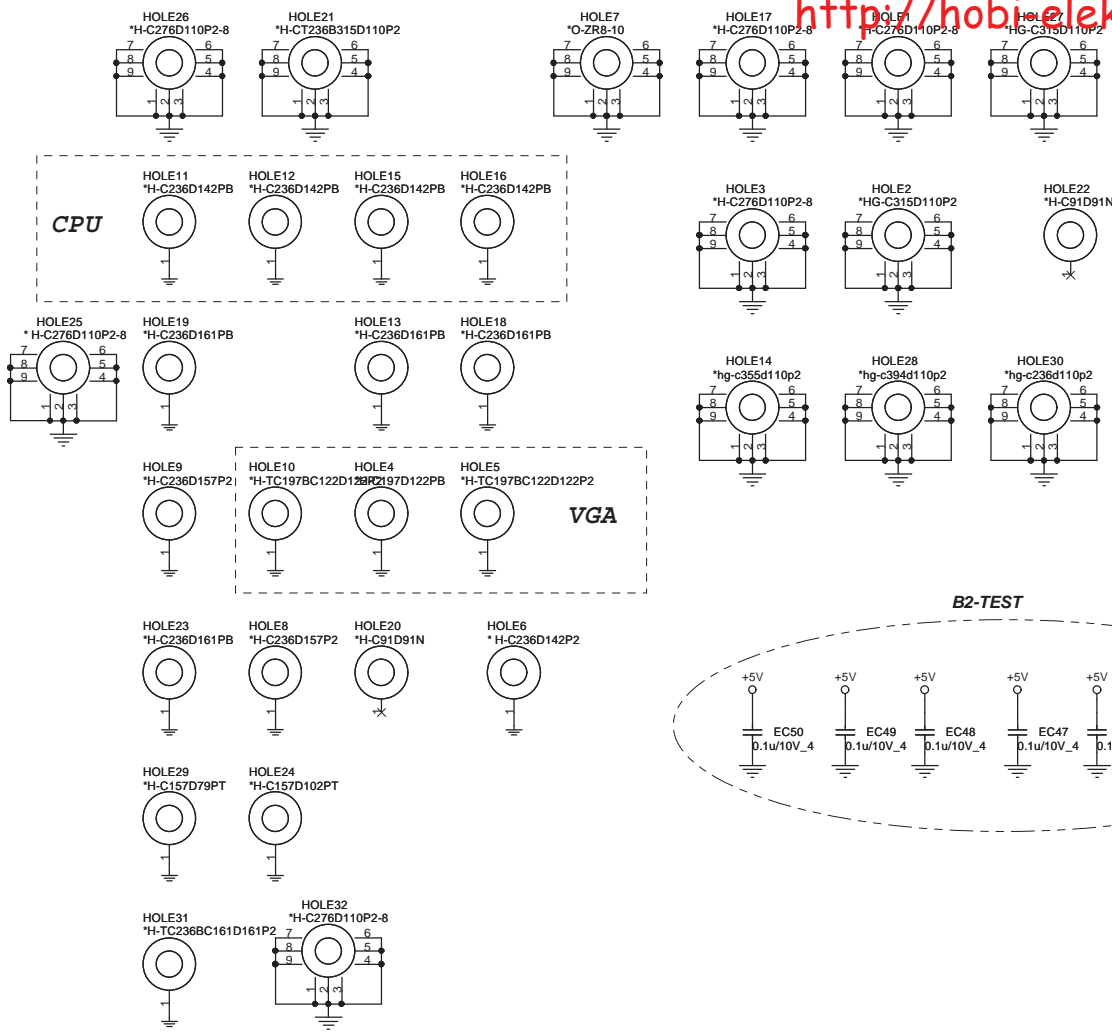


B2-TEST

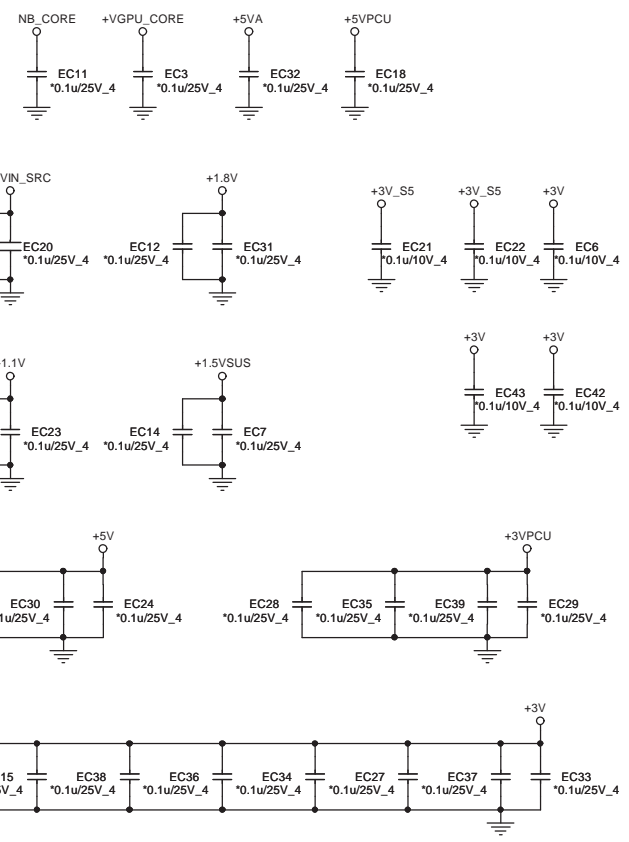
OCP=3.3A
22.5A
+VGPU_CORE



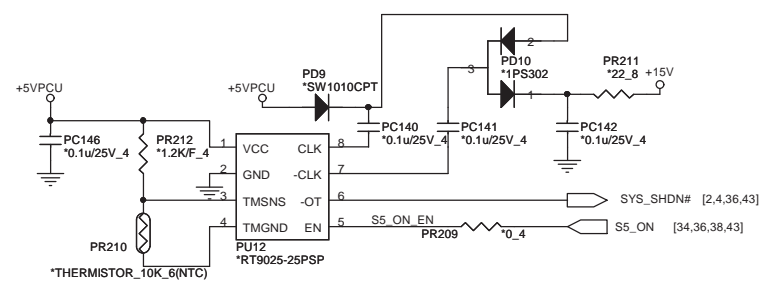




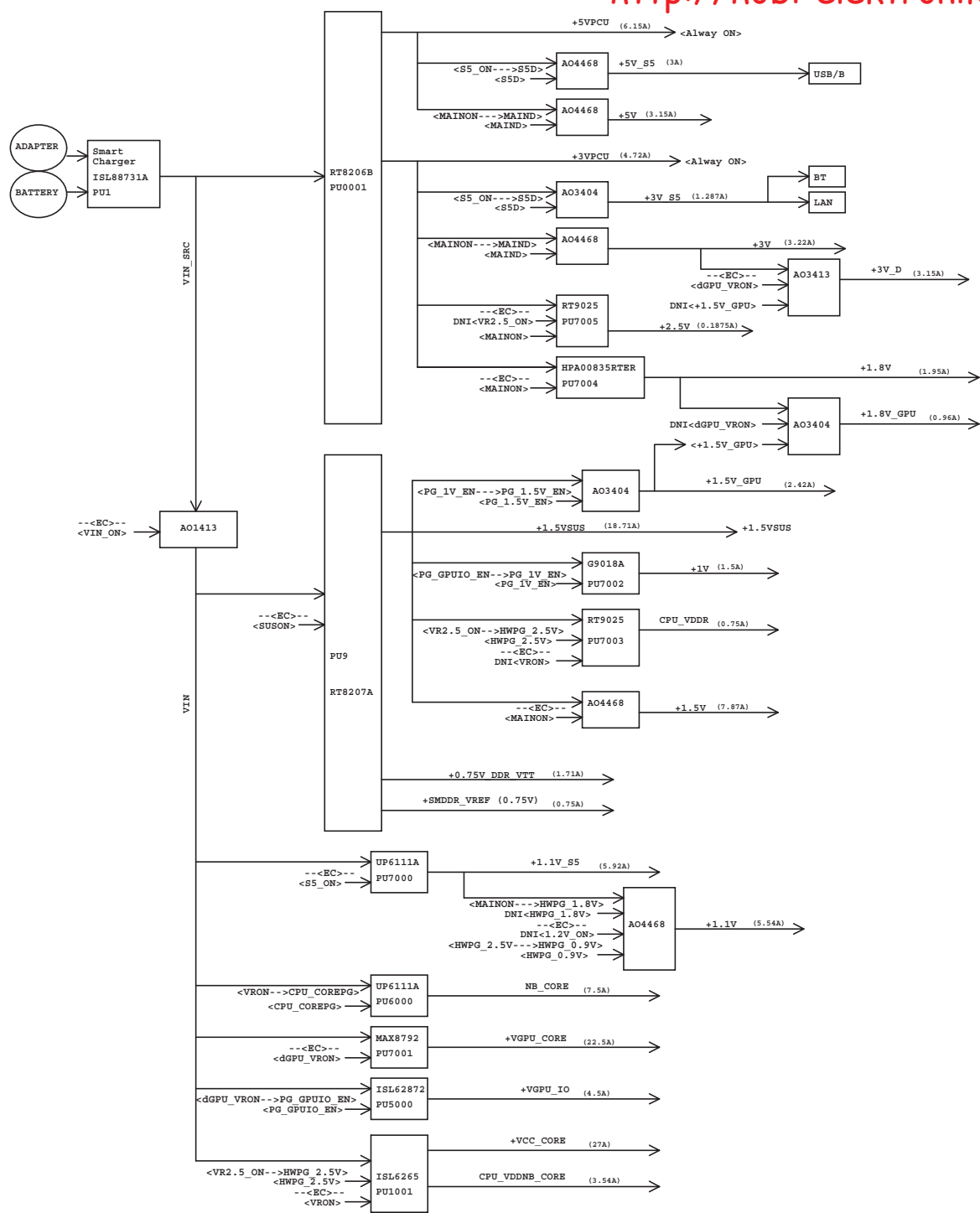
For EMI

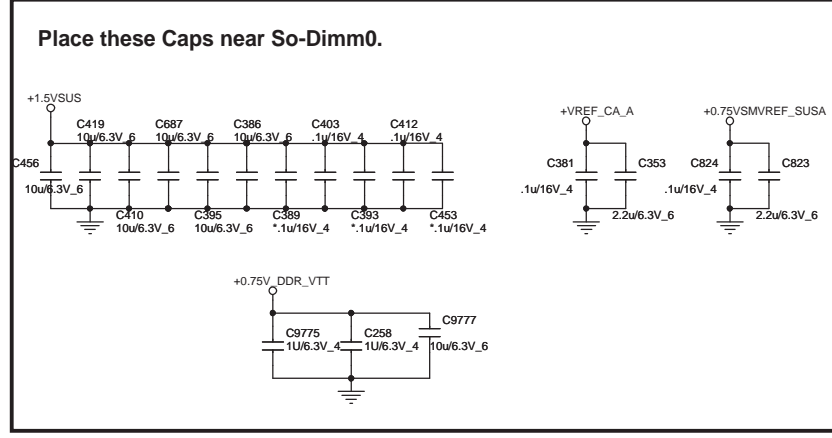
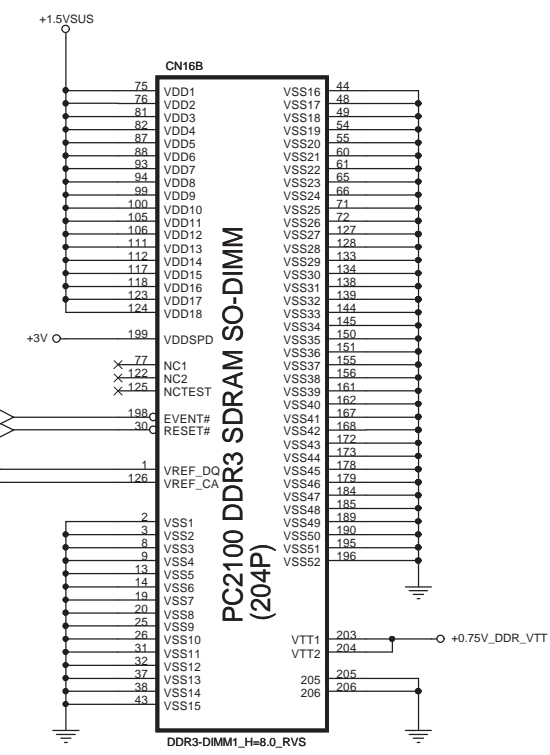
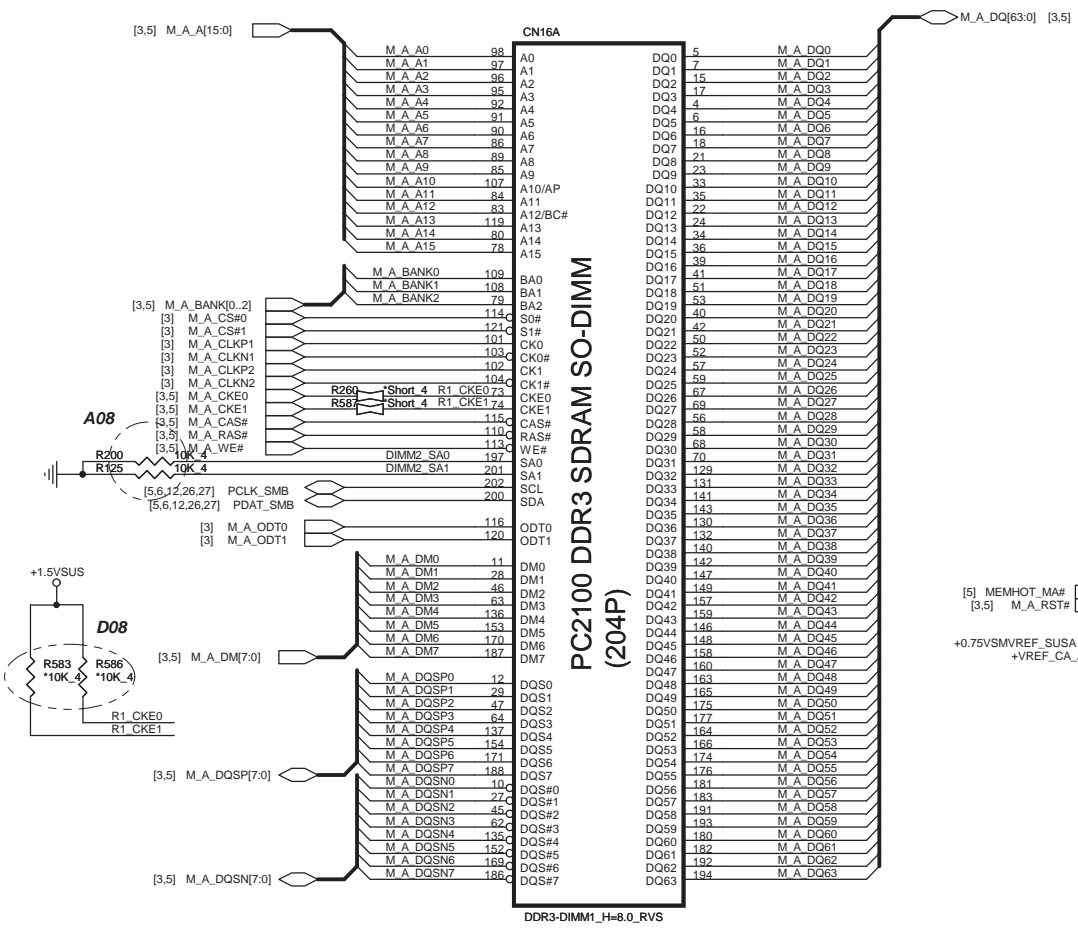


POWER TEST



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A52
2DIMM---->P/N: DGMK4000145



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Size	Document Number DDR3 DIMM-1(H=9.2)	Rev 1A
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- A01 Page25/27/28/31/32/36/38/44 Change footprint , due to SMT open issue highlight.
- A02 Page32 Change T/P switch P/N, due to SMT open issue highlight.
- A03 Page42 Modify Madison-Pro & Park-XT VID table.
- A04 Page14 Modify board ID table and R517,R304 support Side-port function.
- A05 Page14 Add R528 support different Side-port VRAM type.
- A06 Page44 Support CPU 45W solution.
- A07 Page02 Change clock gen to no stuff, due to use internal clock source.
- A08 Page06/07/48 Change SO-DIMM SMBUS address.
- A09 Page08/10/11 Add Side-port function.
- A10 Page10 Chane HDMI DDC CLK/DATA port.
- A11 Page10 Stuff R190.
- A12 Page12 Change dGPU_PWROK from GPIO1 to GPIO32.
- A13 Page12 Change board ID GPIO pin.
- A14 Page13 1. Stuff D19,R307,C538 and no stuff D18. 2. Change pull high power rail from +3V_D to +3V.
- A15 Page16 Change R500 from 0ohm to 10k.
- A16 Page12 Connect 25Mhz for GPU workaround design.
- A17 Page18 Modify GPU Power-on sequence table.
- A18 Page18 Remove GPU_IO VID contron pin and change GPU_CORE GPIO pin to GPIO15/20.
- A19 Page19 Change R107 from 680ohm to 51 ohm and modify design of MEM_RST#. Also change R30 to no stuff.
- A20 Page20/22/35/42 Reserve +3V_D_ZR8 power rail for GPU leakage issue.
- A21 Page18 Reserve VGA_REQ# pin.
- A22 Page25 Delete brightness switch IC control and change to 0ohm solution.
- A23 Page25 Stuff R135,R144 ,due to some CRT monitor can't display.
- A24 Page25 Stuff C776,C787 for EMI request.
- A25 Page25/32 Change connect footprint and P/N.
- A26 Page29/35 Add ODD power switch design and stuff R170.
- A27 Page33 Change Q29,Q30 to no stuff.
- A28 Page37/41/44 Remove jmuper.
- A29 Page37 Change PC193 P/N to low highlimit, due to ME thermal door impact.
- A30 Page38 Change PC179,PC180 from 22uF/25V to 100uF/25V.
- A31 Page38 Change CPU_CORE enable from VRON to HWPG_2.5V.
- A32 Page30 Change R538,R548 from 48ohm to 68ohm for audio performance.
- A33 Page28 Change R572,R563 to short pad for debug use.
- A34 Page20 Change +VGPU_IO power rail to +VGPU_CORE.
- A35 Page25 Connect CN5 LCD connect shielding pin to GND for ESD issue.
- A36 Page18 Change R65 to no stuff.
- A37 Page22 Reserve OVERT# pull high resistor prevent noise.
- A38 Page33 Add pull low 100k ohm for ODD_EJ,POWER_SAVE signal.
- A39 Page36 Reserve cap for power team request.
- A40 Page30 Stuff 0 ohm resistor for ESD protect use.
- A41 Page02/03/10/11/15/18/20/21/27/30/32/35/36 Change bead P/N for EMI request, the reason is cost down and not STD parts.
- A42 Page21 Reserve 0 ohm for PLL power use.
- A43 Page38 Remove PR153 & change to 0402 package
- A44 Page44 Change PR113 from 0 to 10K Ohm & Change enable source to +3V
- A45 Page38/39/40/41 Stuff PR80,PR89,PR94,PR95,PR47 to 1 Ohm & PC47,PC51,PC64,PC65,PC36 of value to 1000p for EMI request
- A46 Page36 Change PC111 of value to 1U/25V
- A47 Page36 Change PR37 of value, from 33K to 150K
- A48 Page36 Change PR35 of value, from 10K to 39K
- A49 Page26 Change HDMI connector PN
- A50 Page7 Change P/N for 3-DIMM H=4.0 STD
- A51 Page6 Change P/N for 3-DIMM H=4.0 RVS
- A52 Page48 Change P/N for 3-DIMM H=8.0 RVS
- A53 Page36 Change battery connector P/N to DFHD08MR099
- A54 Page26 Modify HDMI's I2C for DIS.



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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

- A55 Page14 Change board ID power rail from +3V_S5 to +3V.
- A56 Page33/35 Modify WLAN RF_LED control design.
- A57
- A58 Page12 Remove R331 only for A11 version.
- A59 Page12 Add U18,C533 & remove R303 for power sequence.
- A60 Page14 Remove C760,C754,R507& Y7, due to it's for external clock use.
- A61 Page2 Stuff R474,R486 for LAN & WLAN of REQ#.
- A62 Page3/12 Stuff R424 and no stuff R286, due to CPU_PRPCOT# is +1.5VSUS level.
- A63 Page16 Change D29 package & Add D24.

Note : Change 0ohm to short pad
R276,R281,R415,R443,R445,R531,R532,R533,R534,R535,R539,R566,R174,R512,R513,R263,R437,R439,R441,R99


ZR8 Schematic EC Tracking Record B1 (For B1 TEST) Dec.09 , 2009
EC / Page / Item / Description

- B01 Page21 Remove DP/TMDS Output Driver Analog Supply from port C&D. Due to it's don't to use.
- B02 Page25 Stuff R48 for Discrete platform use.
- B03 Page/10/25 Modify R signal pull low resistor value to 140ohm, due to keep 70 ohm trace impedance.
- B04 Page33 Modify WLAN LED design and change from GPIO82 to GPIO84.
- B05 Page27 Change LAN layout footprint for "SAW" new package.
- B06 Page13/25 Reserve CCD USB host from for Port2, due to CCD issue.
- B07 Page33 Reserve blue LED power source to 5V, due to White/Blue LED max Vf is more than Green/Orange LED.

ZR8 Schematic EC Tracking Record C (For C TEST) Jan.28 , 2010
EC / Page / Item / Description

- C01 Page02/34 Remove "CPU_THERMTRIP#" control from SB820, due to BIOS don't support this function. Add another "SYS_SHDN#" for H/W shutdown function and add HWPG shutdown design.
- C02 Page04 No stuff Q21,D14,R255 for thermal sensor Alert fnction and change to EC or H/W shutdown function.
- C03 Page09 Add 1uF for monitor test noise issue.
- C04 Page12 Add 0ohm to separate VGA_REQ function, due to it's don't support the function and cause by leakage current concern.
- C05 Page24 Modify VGA note text for R signal impedance control.
- C06 Page24 Add brightness switch control by iGPU switch mode. Due to BIOS for C test already support.
- C07 Page29 Reserve EAPD# audio design for "Bo" sound.
- C08 Page41 Change PG_GPUJO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
- C09 Page43 Change PR69 FROM 1.2K to 680ohm , the reason is for SDA high temperature (40 degree/20% humidity) auto shutdown issue.
- C10 Page27 Short LPC signal for debug card use.
- C11 Page29 Change R538,R548 from 56ohm to 68ohm for audio performance test FSOV spec requirement.
- C12 Page42 Change PR113 from 10k to 0ohm.
- C13 Page35 Change EC54,EC55 to stuff for ISN issue.
- C14 Page21 Modify DDR3 Memory Aperture size table.
- C15 Page03/40 Reserve VDDR_SENSE signal to controller IC.
- C16 Page27 Change RP32 to no stuff.
- C17 Page04 Modify CPU thermal control design from EC or BIOS control and change U16,R254 to no stuff ,Q17,Q18,Q19 to stuff.
- C18 Page03 No stuff R189.

Note : Change 0ohm to short pad
R124,R121,R174,L31,L37,L35,R136,R115,R169,R325,R315,R295,R292,R278,R31,R90,R21,R112,R24,R25,R270,R530,R99,R478,R512,R513,R514,R326,R269,R268,R265,R266,R610,PR73,PR220,PR261,PR229

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ZR8 Schematic EC Tracking Record A (For Ramp) Feb.25 , 2010

EC / Page / Item / Description

- D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.
- D02 Page15 Modify text note.
- D03 Page12 Change "GBE_COL" , "GBE_CRS" , "GBE_RXERR" to GND follow SCL V1.04 version.
- D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.
- D05 Page04 No stuff R267,C450,C344.
- D06 Page09 Delete R149,R152 layout pad.
- D07 Page36 No stuff PD12 and add PR181, change PR257 from 1k to 390k. The purpose is for panasonic battery low power protect issue.
- D08 Page05/46 No stuff R584,R259,R583,R586 for CKE signal.
- D09 Page32 Change LED current sense resistor value for LED light measure requirement. (Follow ZR7B)
- D10 Page21 Modify VRAM table.
- D11 Page05/06 Change R123,R122,Q10,R202,R195,Q14 to no stuff, due to S1g4 don't support MEMHOT function.
- D12 Page02 Reserve prohot# for FAN control.
- D13 Page41 No stuff PR16,PQ4,PR3,PR12,PR5,PQ3. Due to MAX8792 had integrate discharge design.
- D14 Page37 Change some component to no stuff, dut to for S1g4 use the same VDD power don't need to compensation difference voltage.

Note : Change 0ohm to hort pad.

R203,117,R585,R588,R260,R587,PR1,PR2,PR33,PR241,PR147,PR146,PR160,PR256,PR133,PR233,PR152,PR155,PR128,PR142,PR143,PR144,PR145,PR130,PR131,PR115,PR120,PR77,PR226,PR222,PR202,PR262.

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