

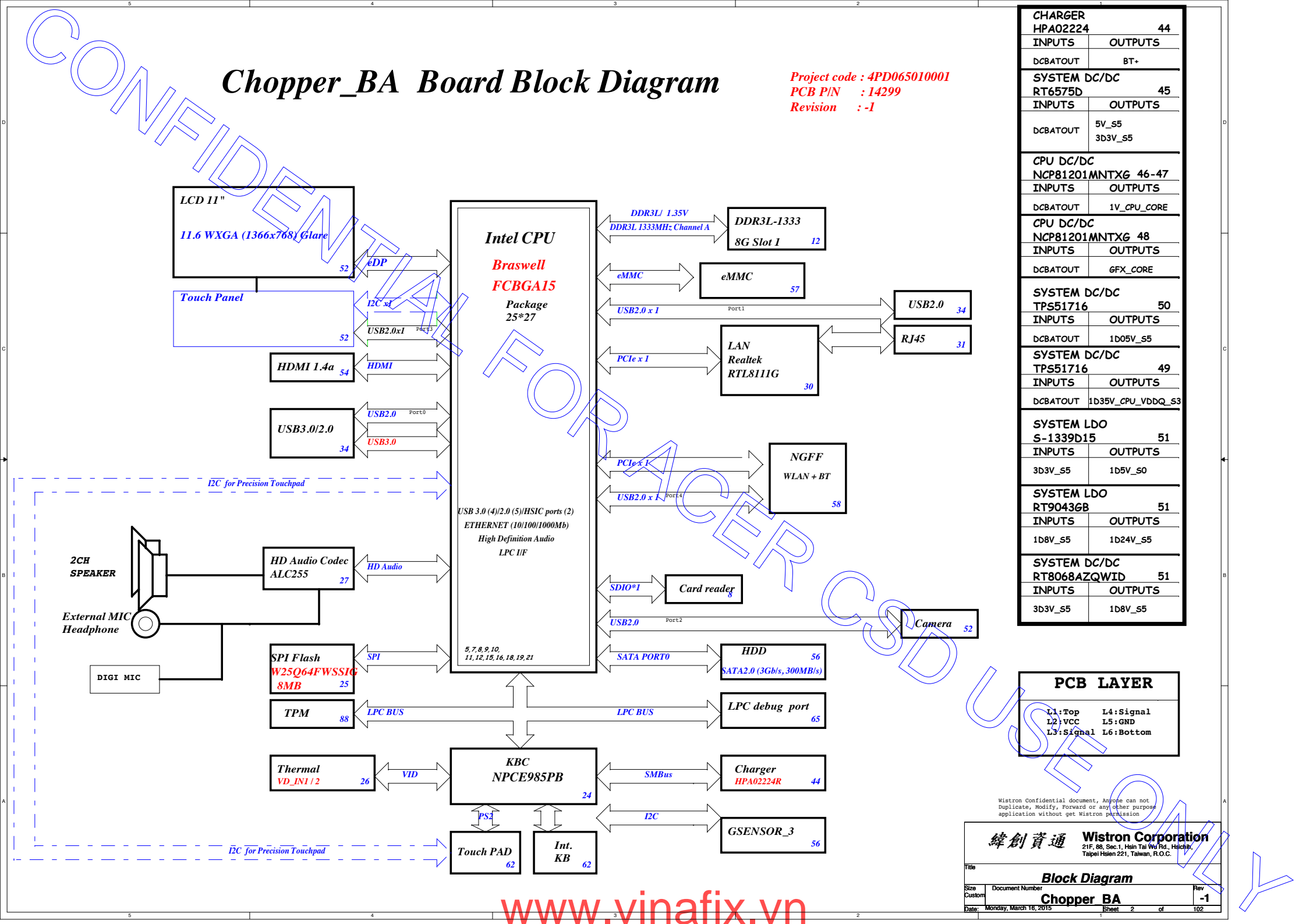
Chopper_BA
Schematics Document

003

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size A4	Document Number Chopper BA		Rev -1
Date: Monday, March 16, 2015		Sheet 1	of 102

Chopper_BA Board Block Diagram

Project code : 4PD065010001
PCB P/N : 14299
Revision : -1



CHARGER	
HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575D	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
DCBATOUT	6FX_CORE
SYSTEM DC/DC	
TPS51716	50
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5
SYSTEM DC/DC	
TPS51716	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_CPU_VBDQ_S3
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
RT9043GB	51
INPUTS	OUTPUTS
1D8V_S5	1D24V_S5
SYSTEM DC/DC	
RT8068AZQWID	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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SSID = CPU

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SSID = CPU

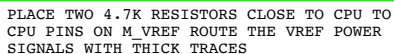
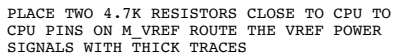
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Title CPU (CFG)			
Size A4	Document Number Chopper BA		Rev -1
Date: Monday, March 16, 2015		Sheet 6	of 102

SSID = CPU

Imax=6.4A (merged VCC0+VCC1) CPU1H
1V_CPU_CORE

1V_CPU_CORE

GFX_CORE

Imax=11A

Imax=0.7A (1D15V_S5)

8 OF 13

BRASWELL

AF36 CORE_VCC1_S0IX3
AG33 CORE_VCC1_S0IX7
AG35 CORE_VCC1_S0IX8
AG36 CORE_VCC1_S0IX9
AG38 CORE_VCC1_S0IX10
AJ33 CORE_VCC1_S0IX14
AJ36 CORE_VCC1_S0IX15
AJ38 CORE_VCC1_S0IX16

AF30 CORE_VCC1_S0IX2
AG27 CORE_VCC1_S0IX4
AG29 CORE_VCC1_S0IX5
AG30 CORE_VCC1_S0IX6
AJ27 CORE_VCC1_S0IX11
AJ29 CORE_VCC1_S0IX12
AJ30 CORE_VCC1_S0IX13
AF29 CORE_VCC1_S0IX1

AD16 DDI_VGG_S0IX1
AD18 DDI_VGG_S0IX2
AD19 DDI_VGG_S0IX3
AF16 DDI_VGG_S0IX4
AF18 DDI_VGG_S0IX5
AF19 DDI_VGG_S0IX6
AF21 DDI_VGG_S0IX7
AF22 DDI_VGG_S0IX8
AJ19 DDI_VGG_S0IX15
AG16 DDI_VGG_S0IX9
AG18 DDI_VGG_S0IX10
AG19 DDI_VGG_S0IX11
AG21 DDI_VGG_S0IX12
AG22 DDI_VGG_S0IX13
AG24 DDI_VGG_S0IX14
AJ21 DDI_VGG_S0IX16
AJ22 DDI_VGG_S0IX17
AJ24 DDI_VGG_S0IX18
AK24 DDI_VGG_S0IX19

AK30 CORE_V1P15_S0IX1
AK35 CORE_V1P15_S0IX2
AK36 CORE_V1P15_S0IX3
AM29 CORE_V1P15_S0IX4

AK33 FUSE_V1P15_S0IX2
AJ35 FUSE_V1P15_S0IX1

AM19 DDI_V1P15_S0IX2
AK21 DDI_V1P15_S0IX1

BRASWELL-GP

UNCORE_VNN_S41
UNCORE_VNN_S42
UNCORE_VNN_S43
UNCORE_VNN_S44
UNCORE_VNN_S45
UNCORE_VNN_S46
UNCORE_VNN_S47
UNCORE_VNN_S48
UNCORE_VNN_S49
UNCORE_VNN_S410
UNCORE_VNN_S411
UNCORE_VNN_S412
UNCORE_VNN_S413
UNCORE_VNN_S414

RSVD#AA30
UNCORE_V1P15_S0IX6
UNCORE_V1P15_S0IX1
UNCORE_V1P15_S0IX2
UNCORE_V1P15_S0IX3
UNCORE_V1P15_S0IX4
UNCORE_V1P15_S0IX5
UNCORE_V1P15_S0IX7
UNCORE_V1P15_S0IX8
UNCORE_V1P15_S0IX9
UNCORE_V1P15_S0IX10

CLK_GND_OFF2
CLK_GND_OFF1

DDR_V1P05A_G31
DDR_V1P05A_G34
DDR_V1P05A_G32
DDR_V1P05A_G35
DDR_V1P05A_G36
DDR_V1P05A_G33

PCI_E_V1P05A_G31#V22
PCI_E_V1P05A_G32

SATA_V1P05A_G32
SATA_V1P05A_G31

USB3_V1P05A_G32
USB3_V1P05A_G31
USBSSIC_V1P05A_G3

FUSE3_V1P05A_G5
FUSE_V1P05A_G3



Imax=1.9A (1D05V_S5)

TP701 Do Not Stuff

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

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Title

CPU (VCC CORE)

Size A4

Document Number

Chopper BA

Rev

-1

Date: Monday, March 16, 2015

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SSID = CPU

HDMI

SRN803
SRN2K2J-1-GP
CRB 2.2k

54 HDMI_CLK_CPU
54 HDMI_DATA_CPU

EDP

52 eDP_TX_CPU_P0
52 eDP_TX_CPU_N0

52 eDP_AUX_CPU_P
52 eDP_AUX_CPU_N

52 eDP_HPD_CPU_N

24 eDP_BLEN_CPU
52 eDP_BLCtrl_CPU
52 eDP_VDDEN_CPU

R801
402R2F-GP

R813

1MR2J-L3-GP

Do Not Stuff

TP803

Do Not Stuff

TP801

Do Not Stuff

TP802

1D8V_S5

R803

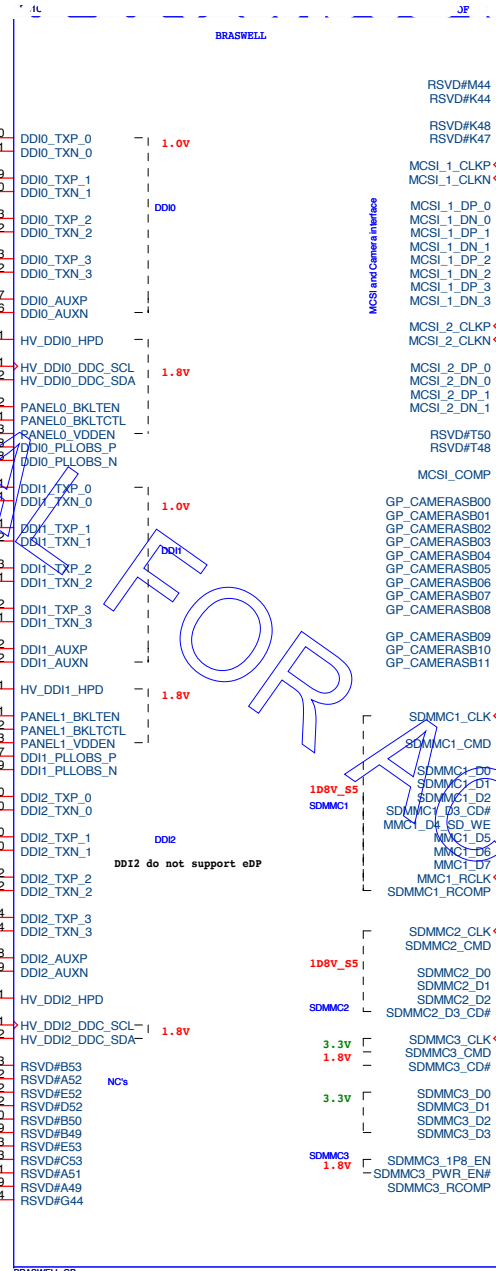
R804

Do Not Stuff

Do Not Stuff

eDP_BLEN_CPU

eDP_BLCtrl_CPU



RSVD#M44
RSVD#K44
RSVD#K48
RSVD#K47
MCSI_1_CLKP
MCSI_1_CLKN
MCSI_1_DP_0
MCSI_1_DN_0
MCSI_1_DP_1
MCSI_1_DN_1
MCSI_1_DP_2
MCSI_1_DN_2
MCSI_1_DP_3
MCSI_1_DN_3
MCSI_2_CLKP
MCSI_2_CLKN
MCSI_2_DP_0
MCSI_2_DN_0
MCSI_2_DP_1
MCSI_2_DN_1
RSVD#T50
RSVD#T48
MCSI_COMP
GP_CAMERASB00
GP_CAMERASB01
GP_CAMERASB02
GP_CAMERASB03
GP_CAMERASB04
GP_CAMERASB05
GP_CAMERASB06
GP_CAMERASB07
GP_CAMERASB08
GP_CAMERASB09
GP_CAMERASB10
GP_CAMERASB11

SDMMC1_CLK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3_CD#
SDMMC1_D4_SD_WE
SDMMC1_D5
SDMMC1_D6
SDMMC1_D7
SDMMC1_RCLK
SDMMC1_RCOMP
SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#
SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#

SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC3_CM#

RSVD#M44
RSVD#K44
RSVD#K48
RSVD#K47
MCSI_1_CLKP
MCSI_1_CLKN
MCSI_1_DP_0
MCSI_1_DN_0
MCSI_1_DP_1
MCSI_1_DN_1
MCSI_1_DP_2
MCSI_1_DN_2
MCSI_1_DP_3
MCSI_1_DN_3
MCSI_2_CLKP
MCSI_2_CLKN
MCSI_2_DP_0
MCSI_2_DN_0
MCSI_2_DP_1
MCSI_2_DN_1
RSVD#T50
RSVD#T48
MCSI_COMP
GP_CAMERASB00
GP_CAMERASB01
GP_CAMERASB02
GP_CAMERASB03
GP_CAMERASB04
GP_CAMERASB05
GP_CAMERASB06
GP_CAMERASB07
GP_CAMERASB08
GP_CAMERASB09
GP_CAMERASB10
GP_CAMERASB11

SDMMC1_CLK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3_CD#
SDMMC1_D4_SD_WE
SDMMC1_D5
SDMMC1_D6
SDMMC1_D7
SDMMC1_RCLK
SDMMC1_RCOMP
SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#
SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#

SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC3_CM#

RSVD#M44
RSVD#K44
RSVD#K48
RSVD#K47
MCSI_1_CLKP
MCSI_1_CLKN
MCSI_1_DP_0
MCSI_1_DN_0
MCSI_1_DP_1
MCSI_1_DN_1
MCSI_1_DP_2
MCSI_1_DN_2
MCSI_1_DP_3
MCSI_1_DN_3
MCSI_2_CLKP
MCSI_2_CLKN
MCSI_2_DP_0
MCSI_2_DN_0
MCSI_2_DP_1
MCSI_2_DN_1
RSVD#T50
RSVD#T48
MCSI_COMP
GP_CAMERASB00
GP_CAMERASB01
GP_CAMERASB02
GP_CAMERASB03
GP_CAMERASB04
GP_CAMERASB05
GP_CAMERASB06
GP_CAMERASB07
GP_CAMERASB08
GP_CAMERASB09
GP_CAMERASB10
GP_CAMERASB11

SDMMC1_CLK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3_CD#
SDMMC1_D4_SD_WE
SDMMC1_D5
SDMMC1_D6
SDMMC1_D7
SDMMC1_RCLK
SDMMC1_RCOMP
SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#
SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD#

SDMMC3_CLK
SDMMC3_CMD
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN#
SDMMC3_RCOMP
SDMMC3_CM#

SDMMC3_CM#

To XDP

MMC1_CLK 57
MMC1_CMD_CPU 57
MMC1_D0_CPU 57
MMC1_D1_CPU 57
MMC1_D2_CPU 57
MMC1_D3_CPU 57
MMC1_D4_CPU 57
MMC1_D5_CPU 57
MMC1_D6_CPU 57
MMC1_D7_CPU 57

RTC_DET# 125

PSW_CLR# 16

SD_CLK 53
SD_DATA1 53
SD_DATA2 53
SD_DATA3 53

SDMMC3_1P8_EN 53
SDMMC3_PWR_EN# 53

SDMMC3_CM#

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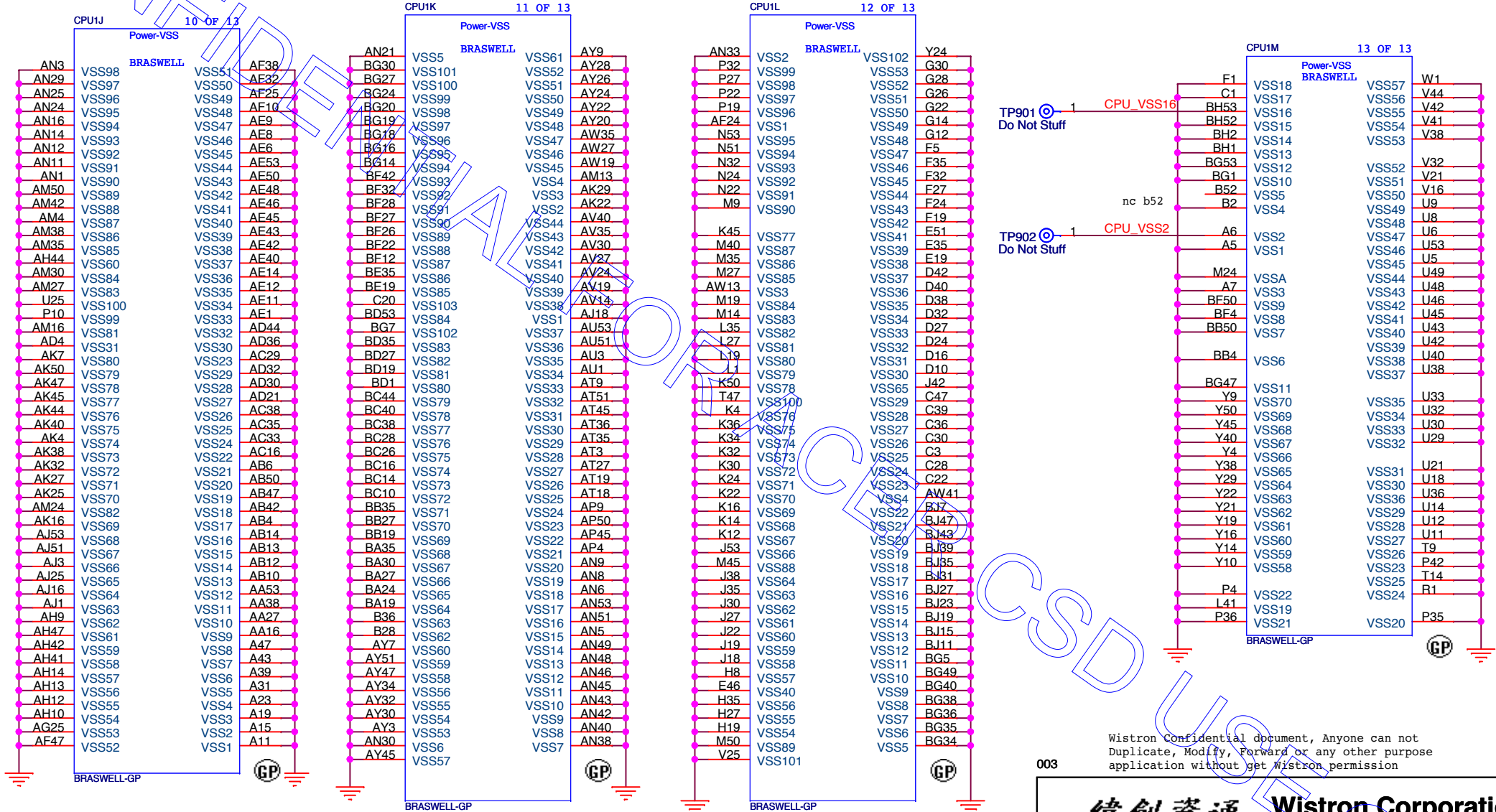
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Title CPU (DDI/EDP/GPIO)
Size A3 Document Number Chopper BA
Date Wednesday, March 25, 2015 Sheet 8 of 102

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SSID = CPU

B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING
recheck



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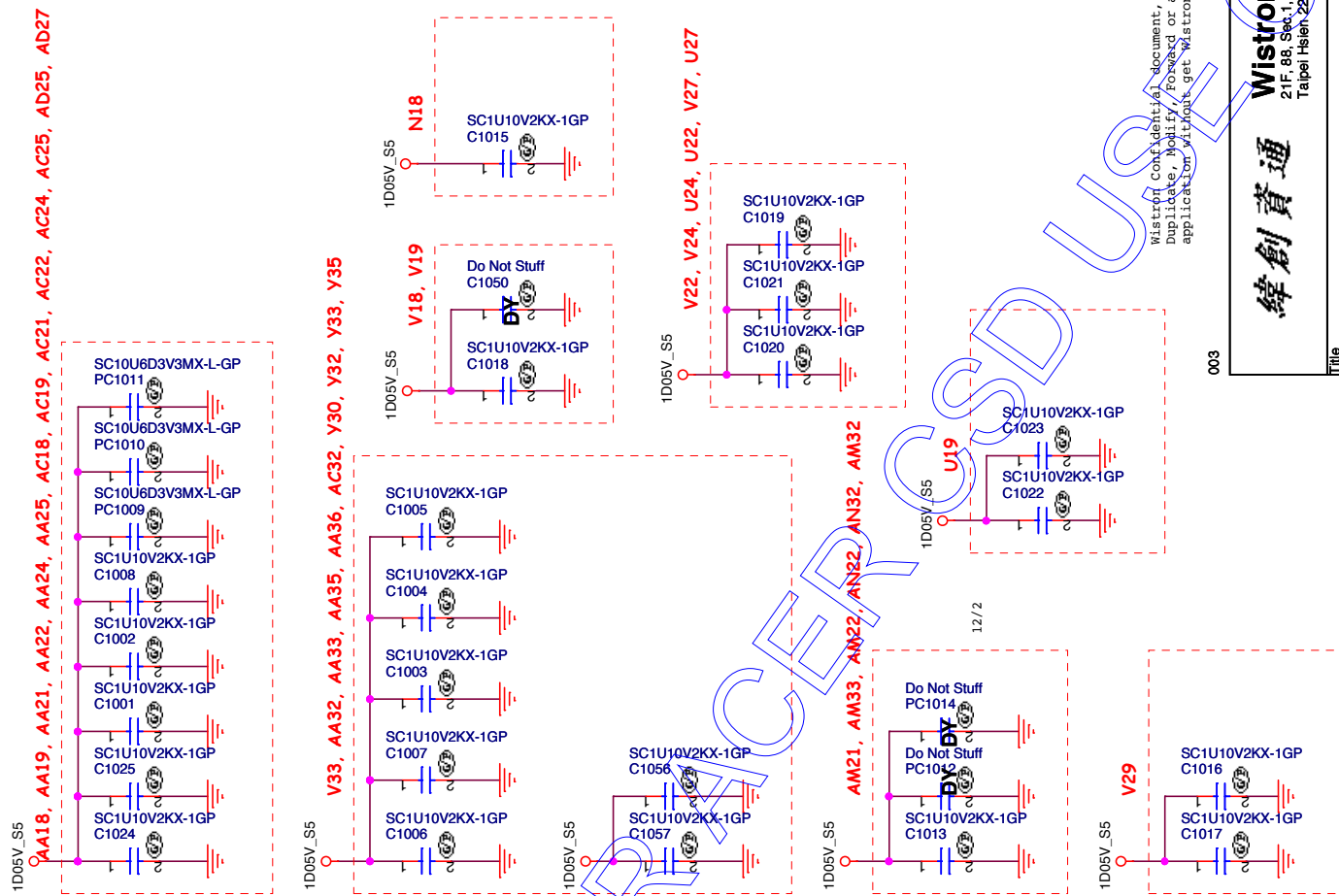
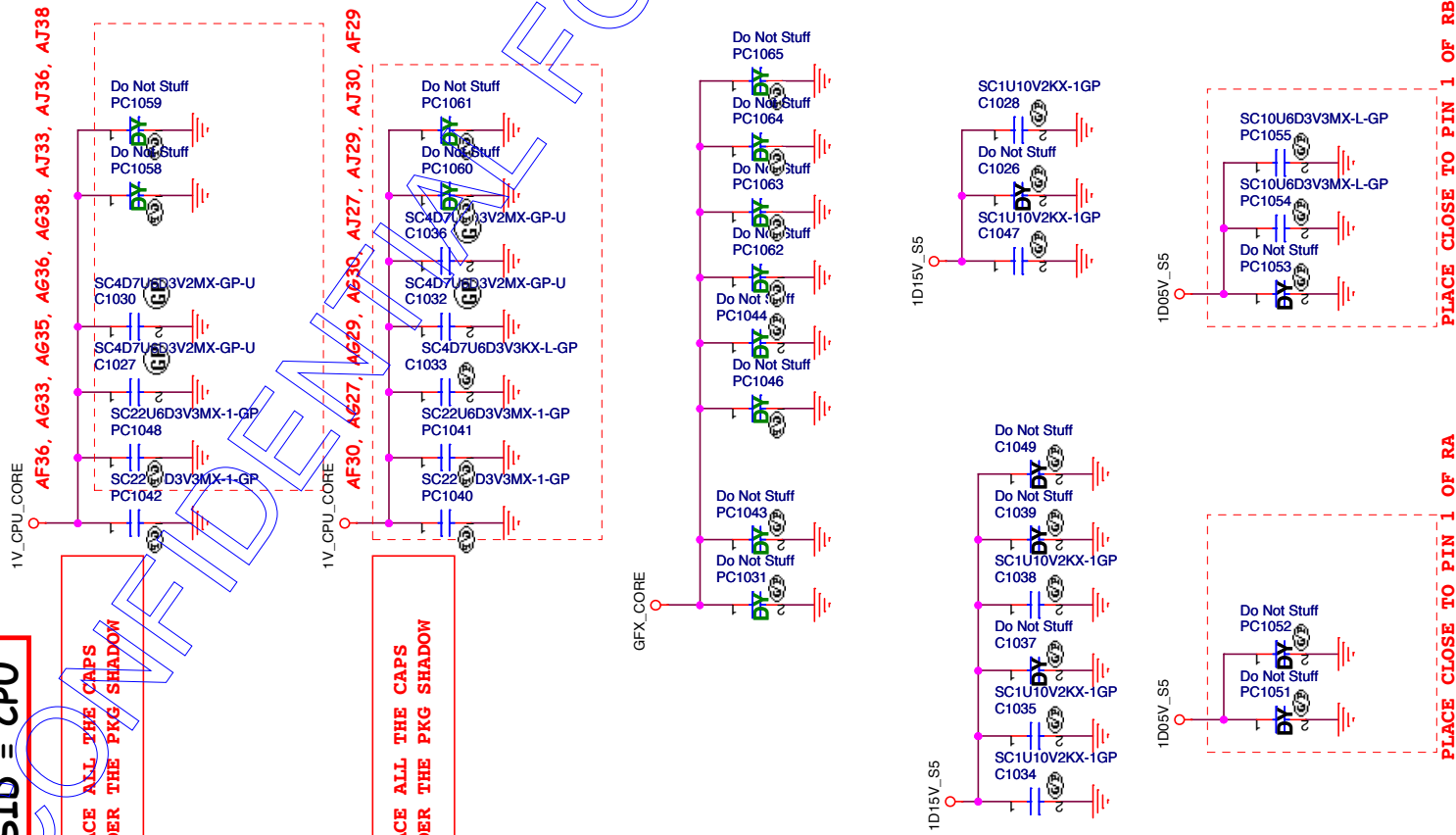
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Title		
CPU (VSS)		
Size	Document Number	Rev
A4	Chopper BA	-1
Date:	Wednesday, March 25, 2015	Sheet 9 of 102

SSID = CPU

**PLACE ALL THE CAPS
UNDER THE PKG SHADOW**

**PLACE ALL THE CAPS
UNDER THE PKG SHADOW**



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Title

CPU (Power CAP1)

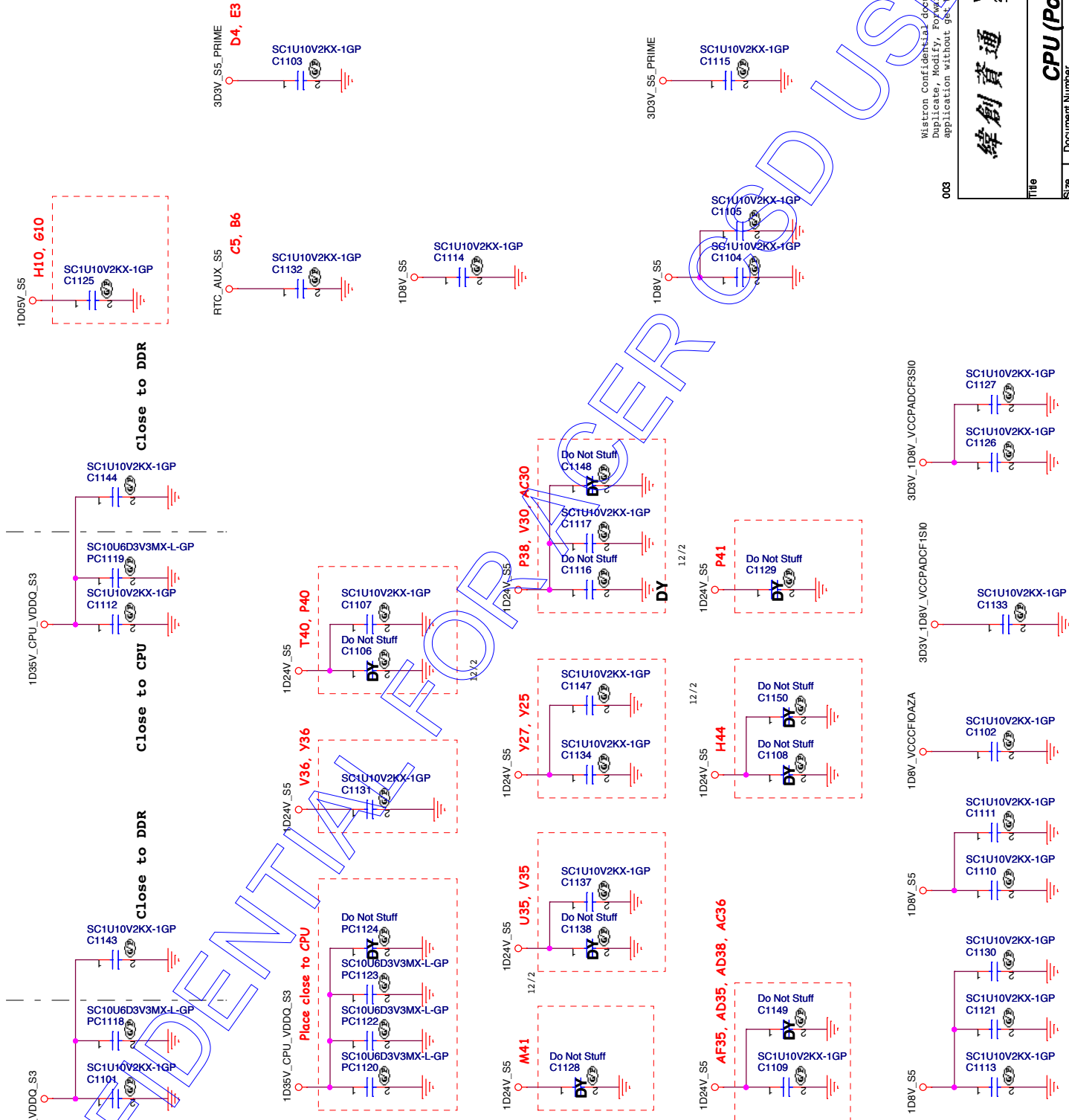
Chopper BA

Rev -1

PLACE CLOSE TO PIN 1 OF RA

----- PLACE CLOSE TO PIN 1 OF RB

SSID = CPU



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Title		CPU (Power CAP2)	
Size	Document Number	Chopper	BA
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SSID = MEMORY

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SSID = CPU

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the finished version of the
PMC_RSMRST_N signal (c. 7.1.1.1)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up	Normal Operation	Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

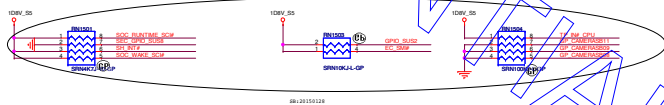


Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name [refer CHV symbol PIN]	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1- Bypass, 0- No bypass	Low

SSID = CPU

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SSID = PCH

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A4		Chopper BA			-1
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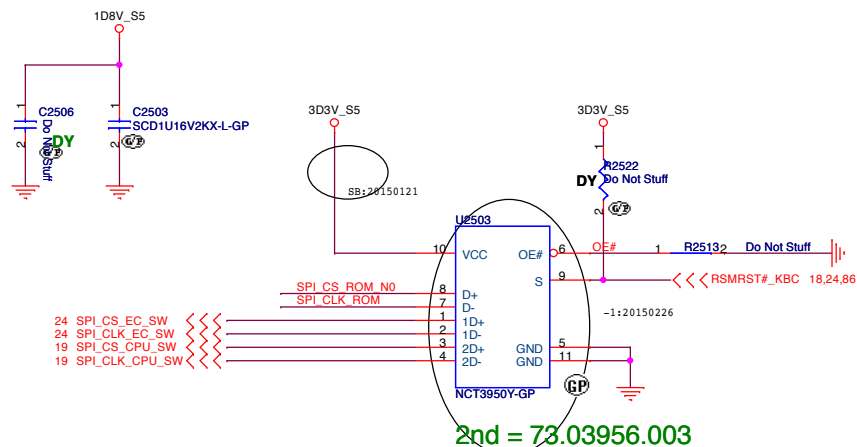
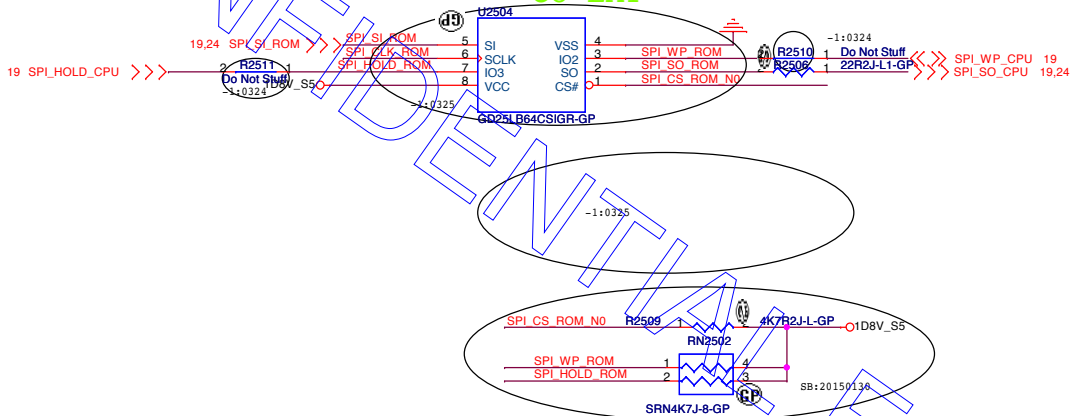
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

072.02564.0A01

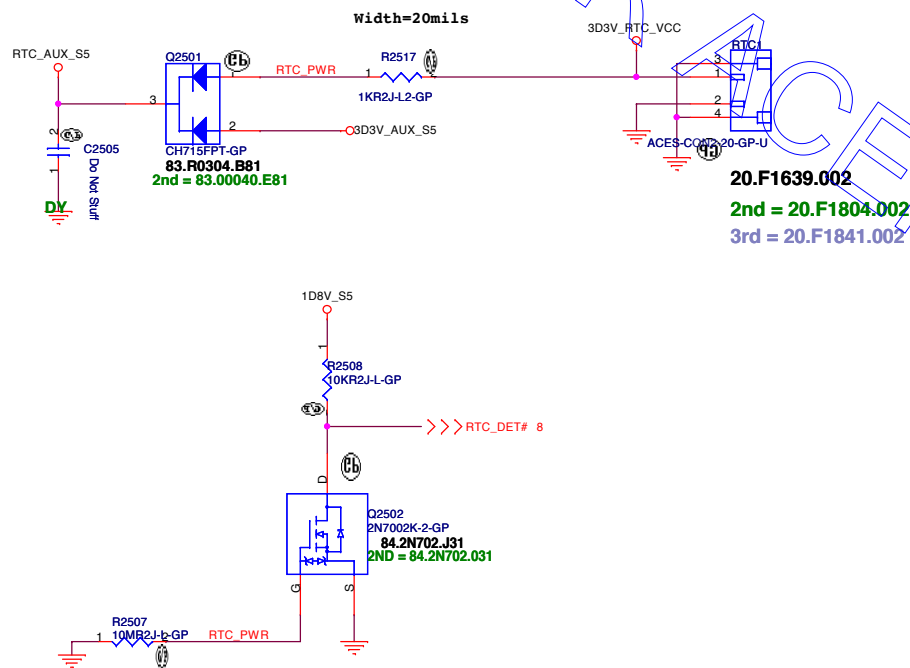
072.25S64.0001

CO-LAY



2nd = 73.03956.003

SSID = RBAT

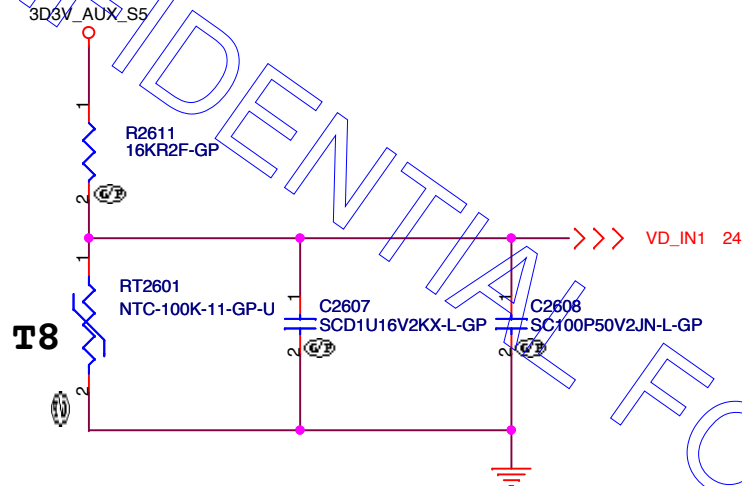


003

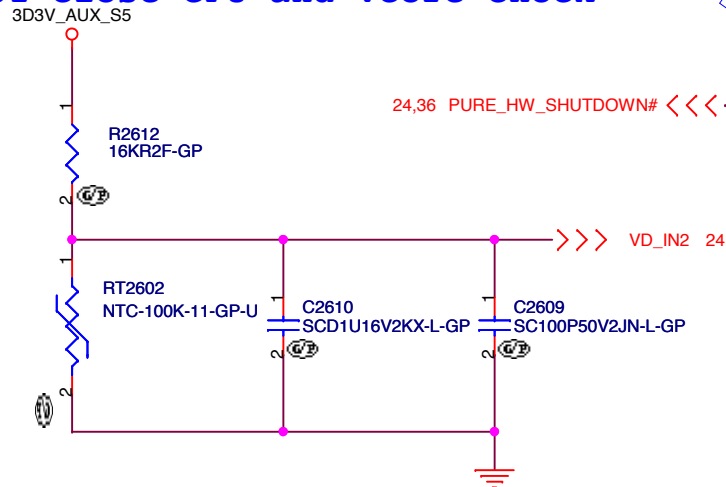
緯創資通 Wistron Corporation
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Title		Flash(KBC+PCH)/RTC	
Size		Document Number	
Custom		Chopper BA	
Date		Wednesday, March 25, 2015	
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SSID = Thermal

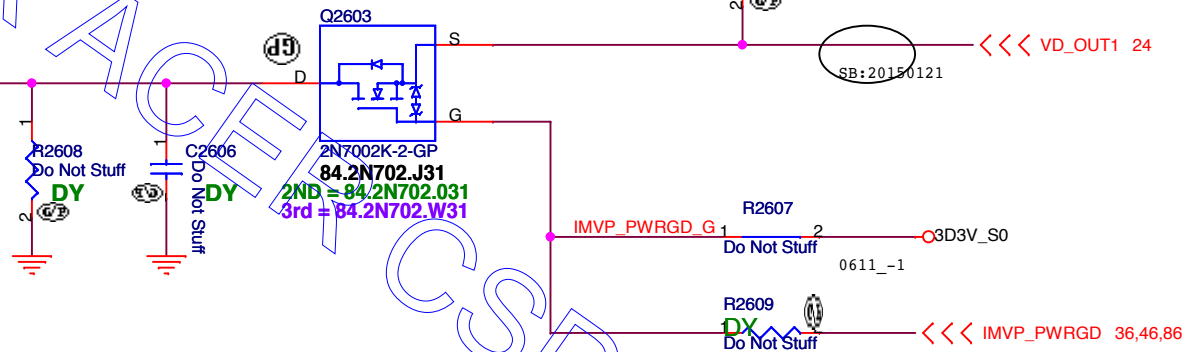


PT2601 close CPU and Vcore chock



PT2602 close CPU and memory

24,36 PURE_HW_SHUTDOWN# <<<



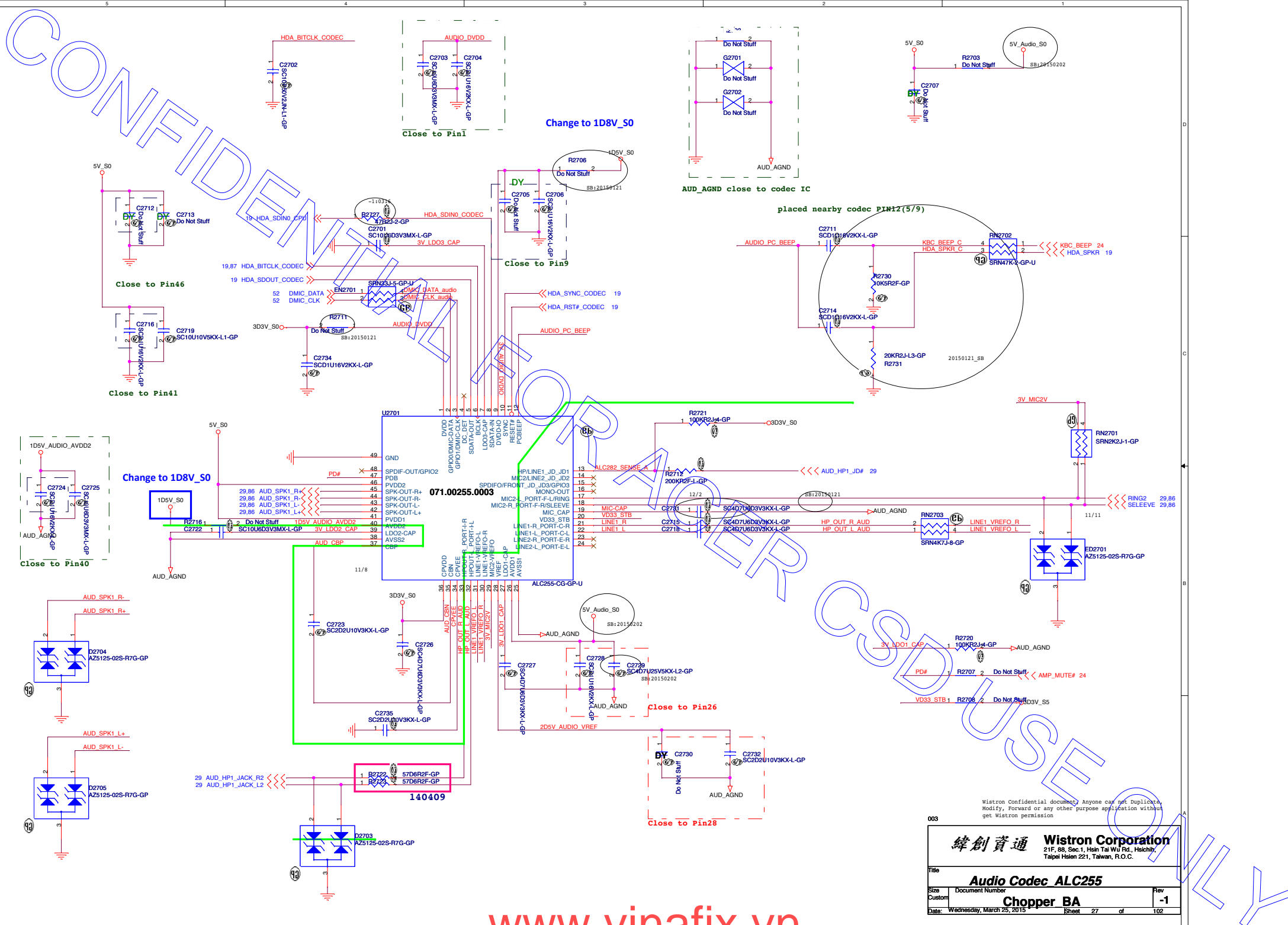
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Title Thermal 7718/Fan Controller P2793

Size A4 Document Number Chopper BA Rev -1

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SSID = AUDIO

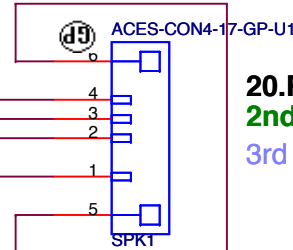
Speaker

27,86 AUD_SPK1_L-
27,86 AUD_SPK1_L+
27,86 AUD_SPK1_R-
27,86 AUD_SPK1_R+

-1+0325

EC2901 1 Do Not Stuff
EC2902 1 Do Not Stuff
EC2903 1 Do Not Stuff
EC2904 1 Do Not Stuff

-1+0324



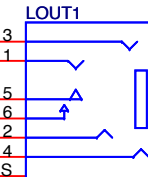
20.F1621.004
2nd = 20.F1937.004
3rd = 020.F0243.0004

Layout Note:
Trace width=40mil

27,86 RING2
27 AUD_HP1_JACK_L2
27 AUD_HP1_JACK_R2
27,86 SELEEVE

EL2901 2 Do Not Stuff
EL2902 2 Do Not Stuff

AUD_HP1_JACK_L1
AUD_HP1_JD#_TYPE
AUD_HP1_JD#_R
AUD_HP1_JACK_R1

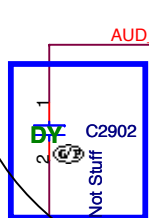


022.10002.0111
2nd = 022.10002.0911

EC2905 1 Do Not Stuff
EC2906 1 Do Not Stuff
EC2907 1 Do Not Stuff
EC2908 1 Do Not Stuff
EC2909 1 Do Not Stuff

AUD_AGND

Combo Jack



AUD_HP1_JD#_R
Do Not Stuff
Do Not Stuff
AUD_AGND

Q2901
Do Not Stuff
2ND = 84.2N702.031

R2910 2 Do Not Stuff
-1+0324

3D3V_S0

R2905 Do Not Stuff

R2906 Do Not Stuff

AUD_AGND

AUD_HP1_JD#_R <<< AUD_HP1_JD#_R 86
AUD_HP1_JACK_R1 <<< AUD_HP1_JACK_R1 86
AUD_HP1_JACK_L1 <<< AUD_HP1_JACK_L1 86

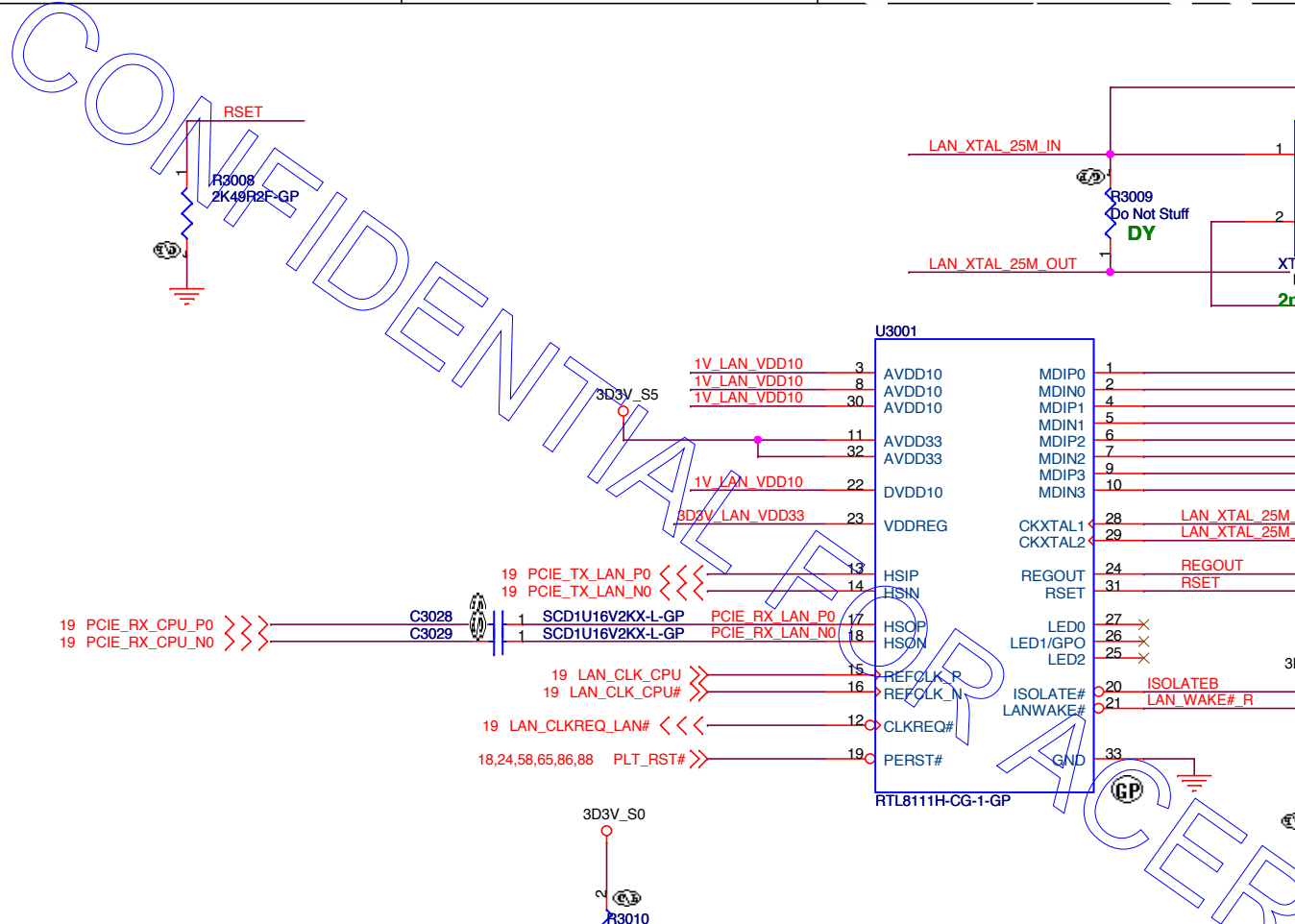
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Title			Audio Jack	
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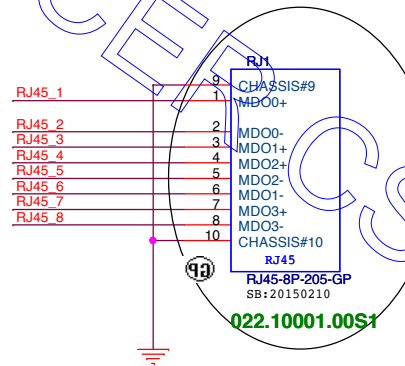
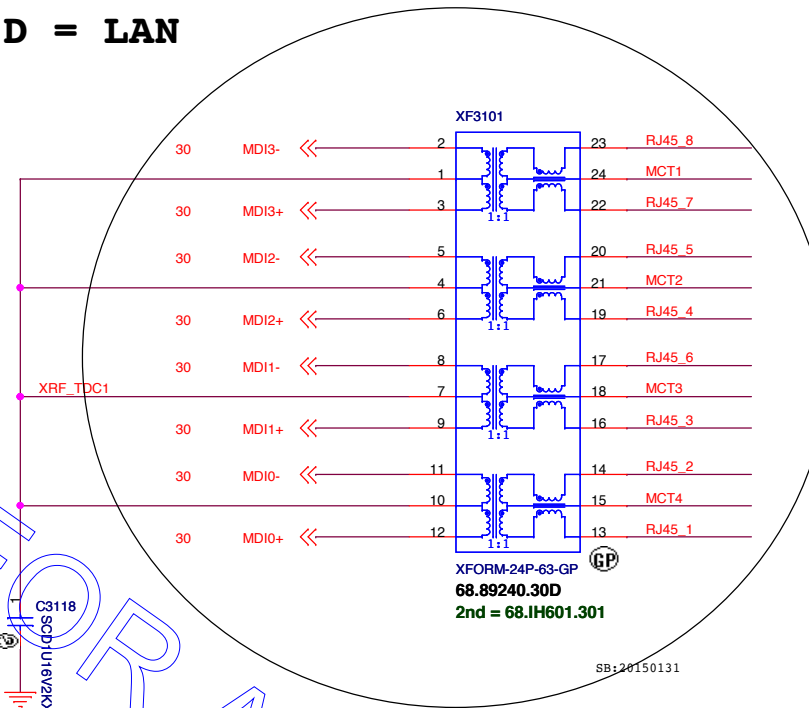
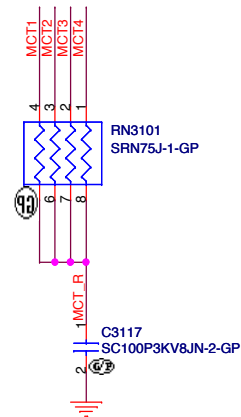
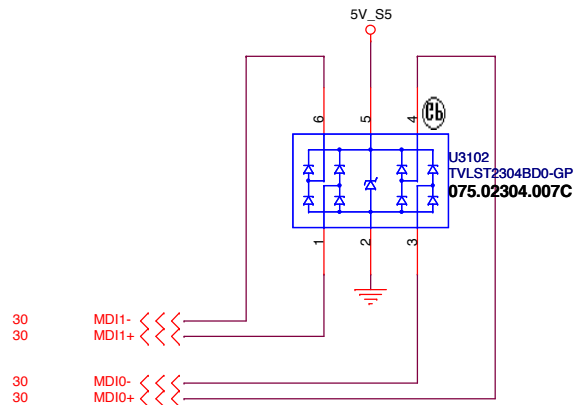
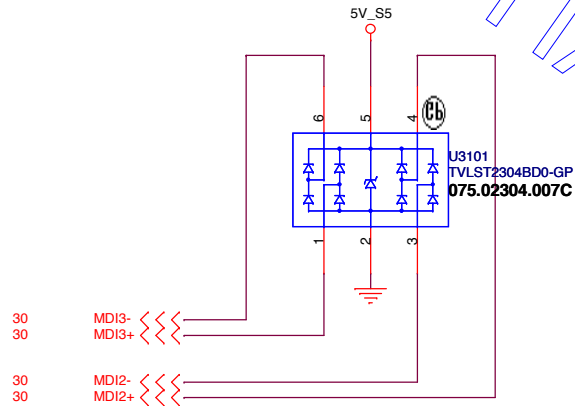
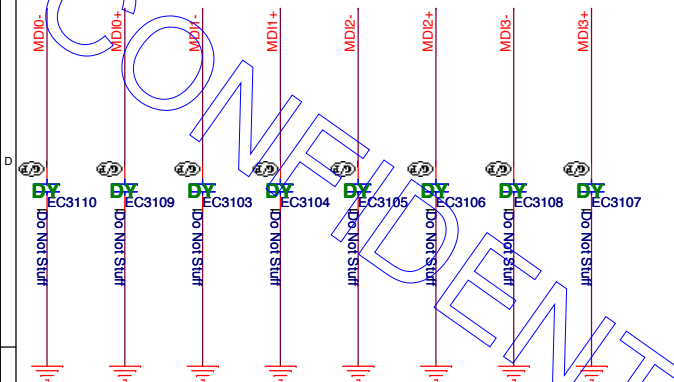
Layout:
For RTL8111G(S)
* Place C3021 to C3024 close to each VDD10 pin--3, 8,

C3024: close to Pin8
C3025: close to Pin30
C3026: close to Pin3
C3027: close to Pin22

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Title LAN(RTL8111)	
Size Custom	Document Number Chopper BA
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SSID = LAN



RJ45_1	RJ45_1	86
RJ45_2	RJ45_2	86
RJ45_4	RJ45_4	86
RJ45_5	RJ45_5	86
RJ45_7	RJ45_7	86
RJ45_8	RJ45_8	86

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Title (LAN+VGA) CONNECTOR	
Size Custom	Document Number Chopper BA
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Title

RTS5170(CARD READER)

Size
A4

Document Number

Chopper BA

Rev
-1

Date: Monday, March 16, 2015

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SSID = SDIO

SD//MS Card Reader

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Title

CARD Reader CONN

Size
A4

Document Number

Chopper BA

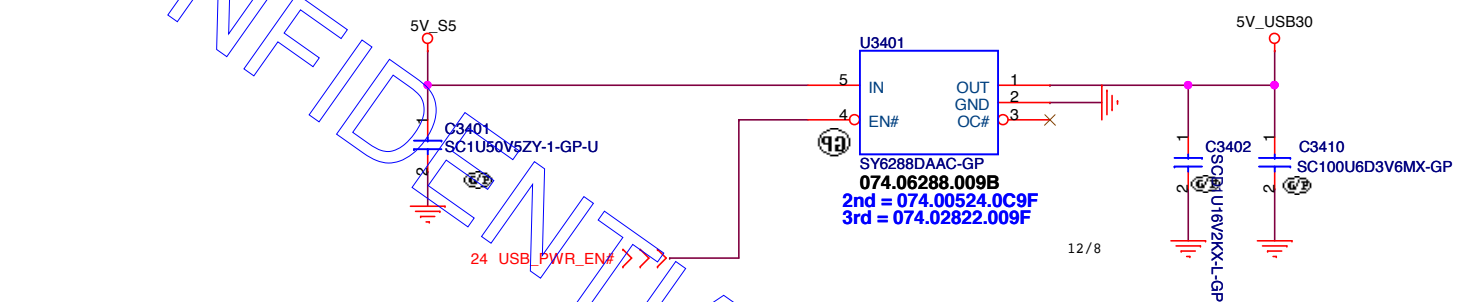
Rev
-1

Date: Monday, March 16, 2015

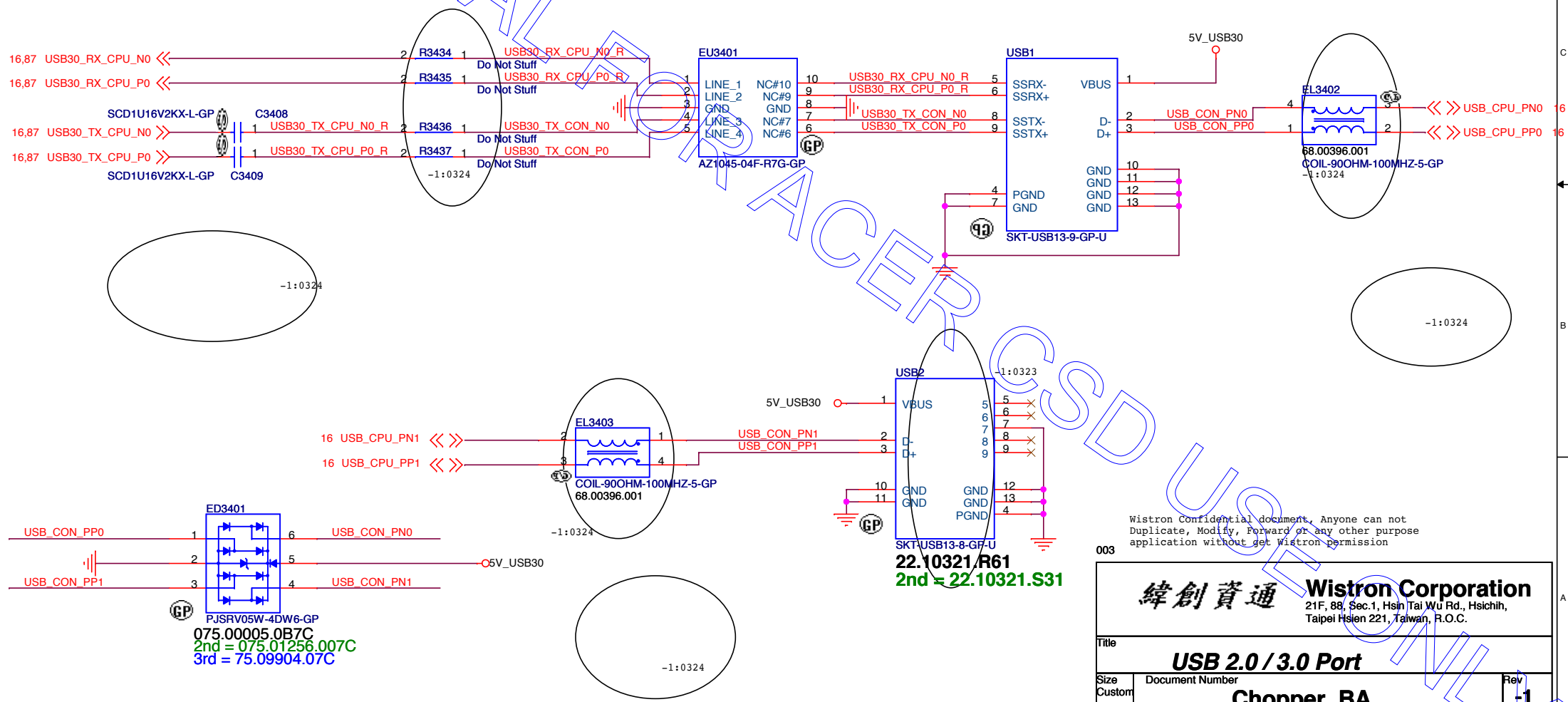
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Low Active 2A



USB 3.0 Connector	
Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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Title

USB 2.0 / 3.0 Port

Size Custom

Document Number

Rev

Date: Friday, March 27, 2015

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Title		
(Reserved)		
Size	Document Number	Rev
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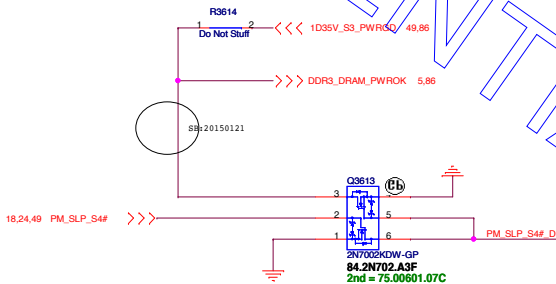
Power Sequence

Table 55- S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

DDR3_DRAM_PWROK

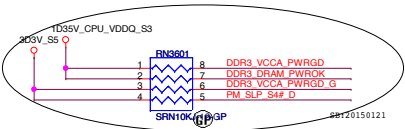
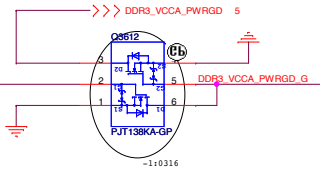
DDR3_VCCA_PWRGD



From EC

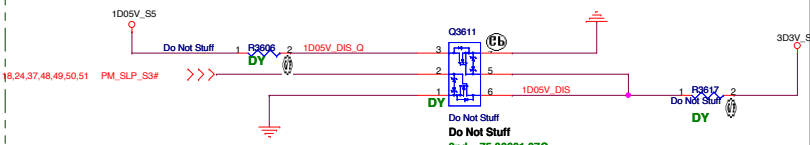
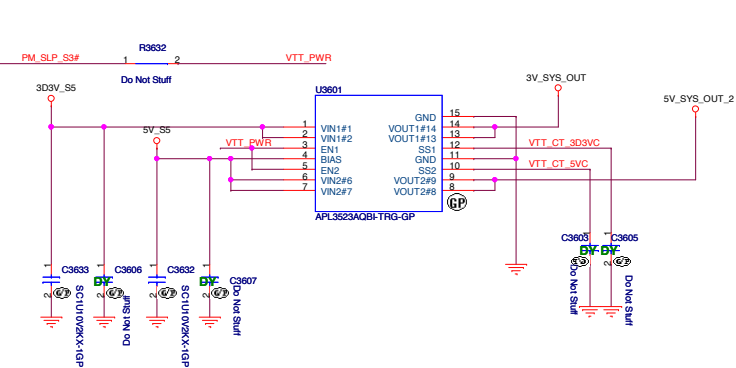
Delay 10ms with ALL_SYS_PWROK

COREPWROK



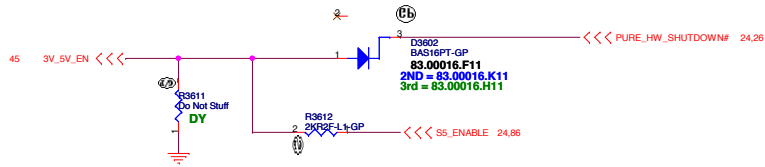
ANNIE Run Power

Discharge circuit



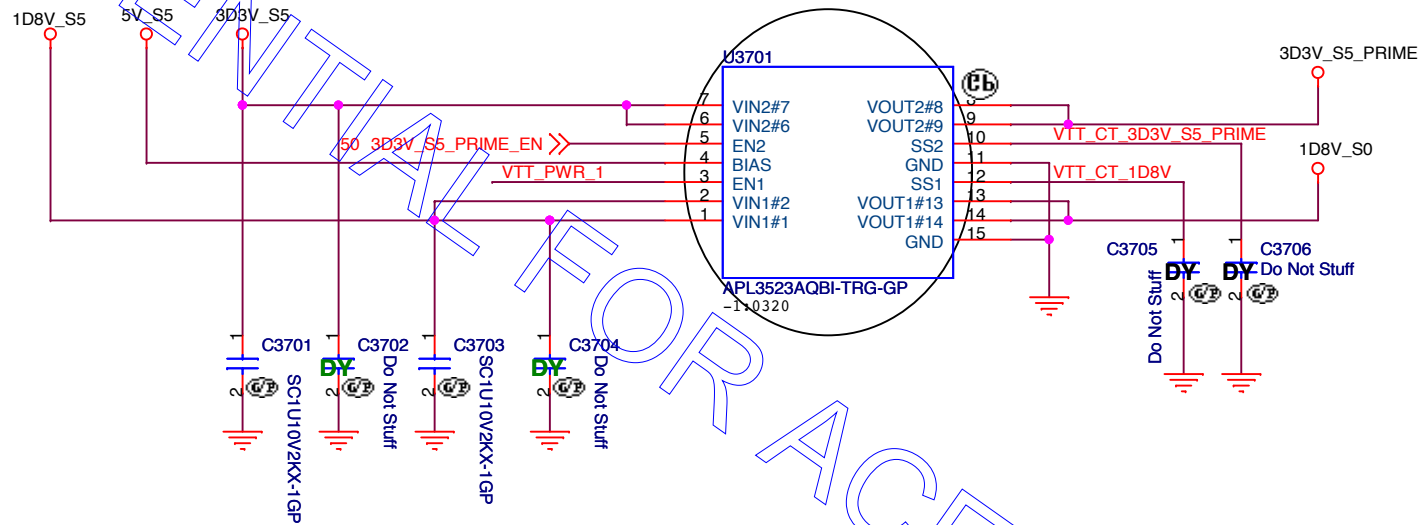
ALL_SYS_PWROK

To EC



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18,24,36,48,49,50,51 PM_SLP_S3# >>> 1 R3701 2 VTT_PWR_1
Do Not Stuff



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Title
ADAPTER OCP / S3 reduction

Size A4 Document Number
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Size
A4

Document Number

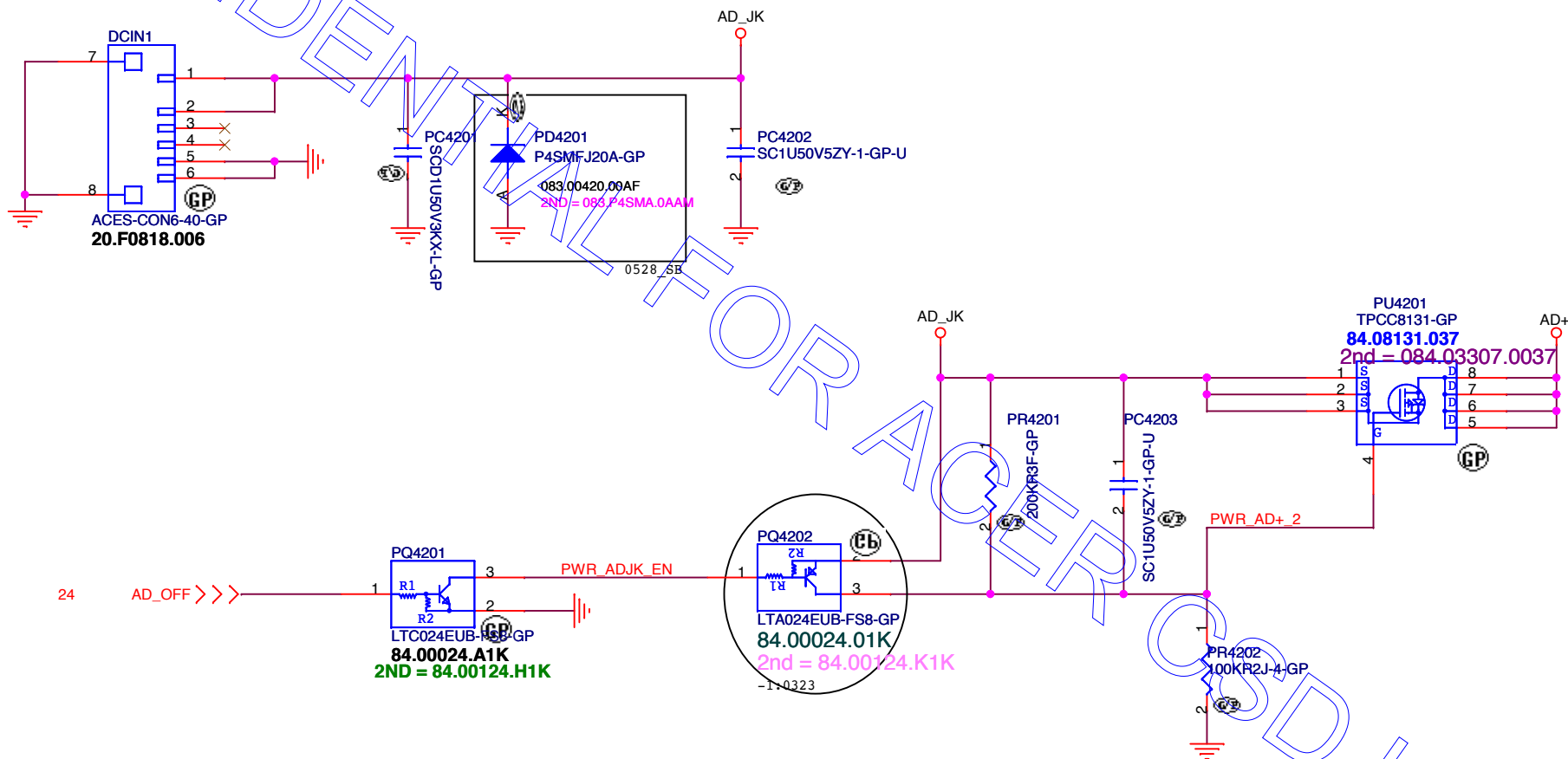
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Adaptor in to generate DCBATOUT



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Title

DCIN JACK

Size
A4

Document Number

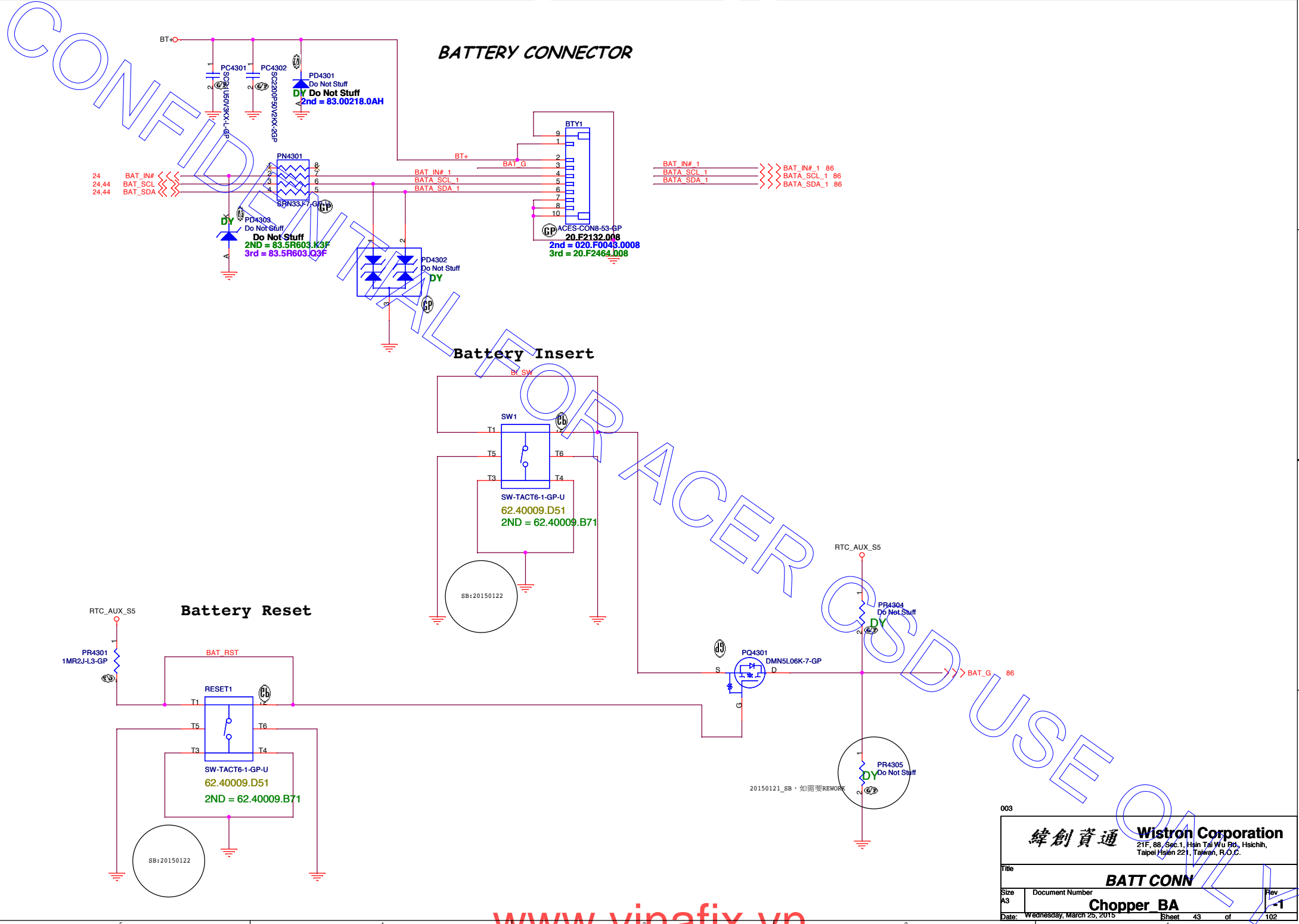
Chopper BA

Rev

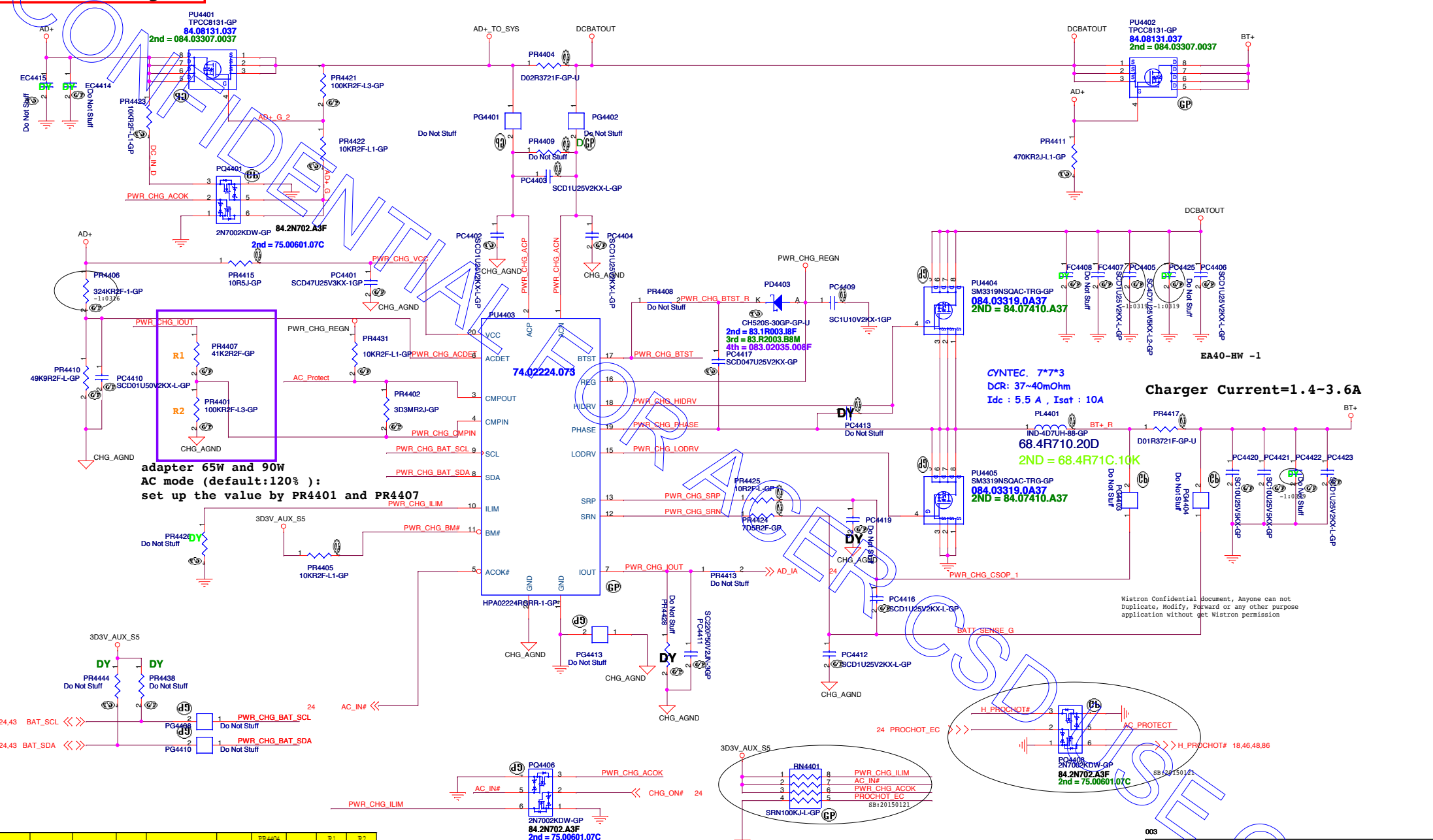
-1

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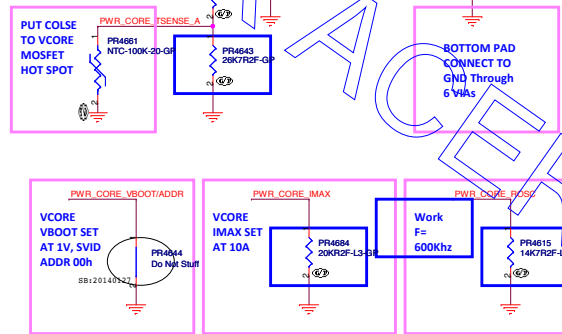
SSID = Charger



	Stat	PM_SLP_A#	Adaptor Current	AC_Protect preset (85% x 120%)	AC_Protect Current	Sense resistor	Current to Wistron	FR4407	FR4401
40W	AC + Battery	High	2.1	102%	2.142	20 mOhm	0.9509	41.2	100
50W	AC + Battery	High	2.61	102%	2.6174	20 mOhm	0.9509	39.4	100
65W	AC + Battery	High	3.42	102%	3.4584	10 mOhm	0.9509	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.9509	60.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10 mOhm	1.2874	115	100
132W	AC + Battery	High	7.1	102%	7.242	10 mOhm	1.4484	180	100

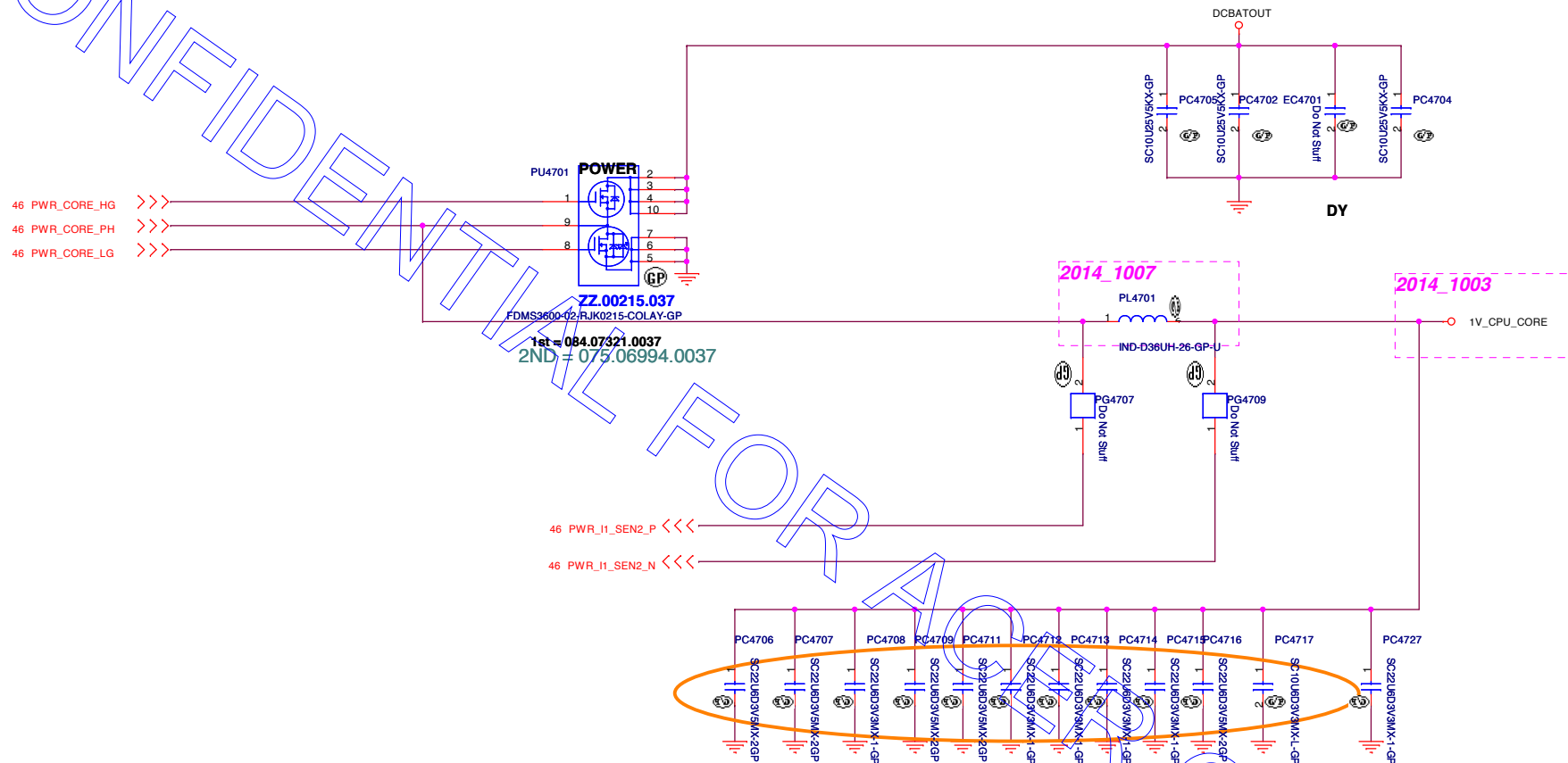
AC adapter detect current :
Ac input current = 20 x (V_{acc} - V_{acn}) / 10mohm

VR12.1 POWER CKT - 1 phase 19Vin



VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
14.0 k	102	140	180	0x0	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

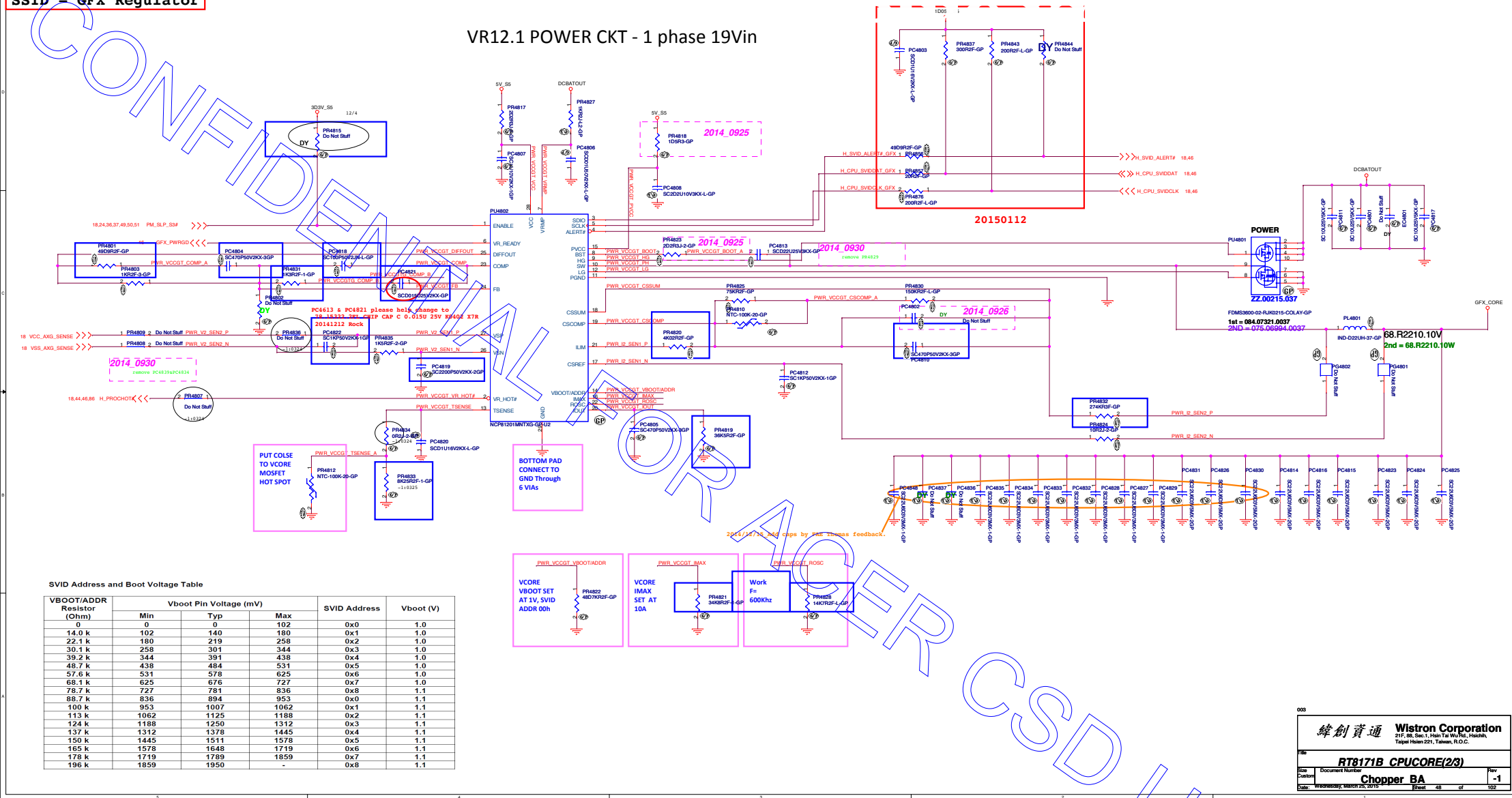
SSID = CPU Regulator



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RT8171B CPUCORE(23)			
Size	Document Number	Rev	
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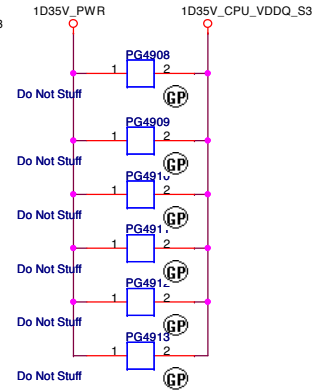
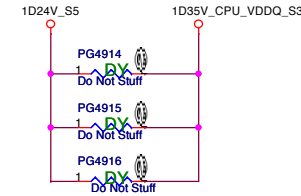
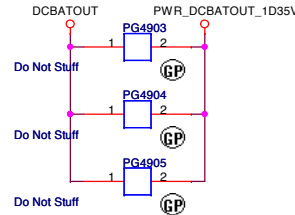
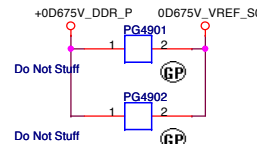
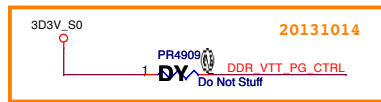
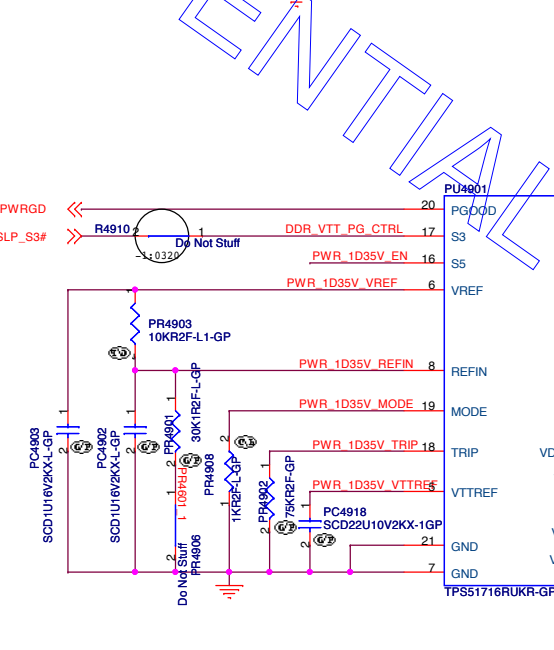
VR12.1 POWER CKT - 1 phase 19Vin



SSID = PWR.Plane.Regulator_1p3Vv0p675V

18,24,36 PM_SLP_S4#

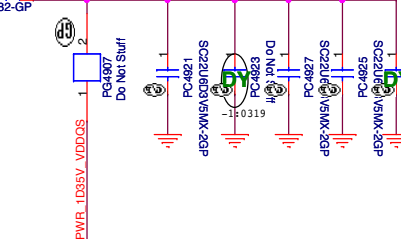
36,86 1D35V_S3_PWRGD
18,24,36,37,48,50,51 PM_SLP_S3#



068.1R010.1111

2ND = 68.1R010.20R

Design Current=4A
OCP<8A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title TPS51716(1.35V_S3/0.675V_S0)	
Size A3	Document Number
Chopper BA	
Date: Wednesday, March 25, 2015	Sheet 49 of 102

TPS51716 for 1D05V_S3

RT8068 PWM for 1D15V

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge	
22k ohm	670kHz		
12k ohm	670kHz		
1k ohm	500kHz	Tracking Discharge	

DCDC 1D05V 1D15V Chopper BA

Wistron Corporation
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DCDC 1D05V 1D15V Chopper BA

Size: 100mm x 100mm
Date: Wednesday, March 25, 2015
Sheet: 50 of 102

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

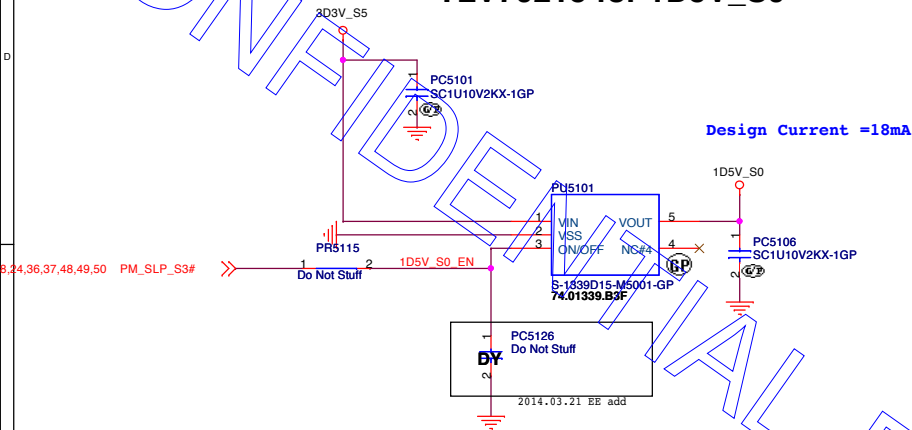
MODE		
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

1D15V
Design current = 0.7A

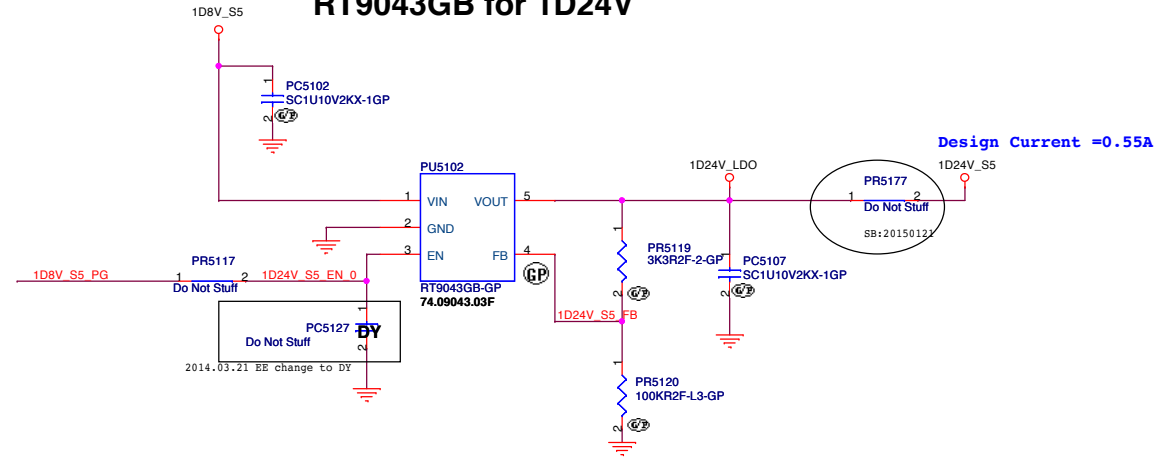
$$V_{out} = 0.6 * ((9.31k + 10k) / 10k) = 1.158$$

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0

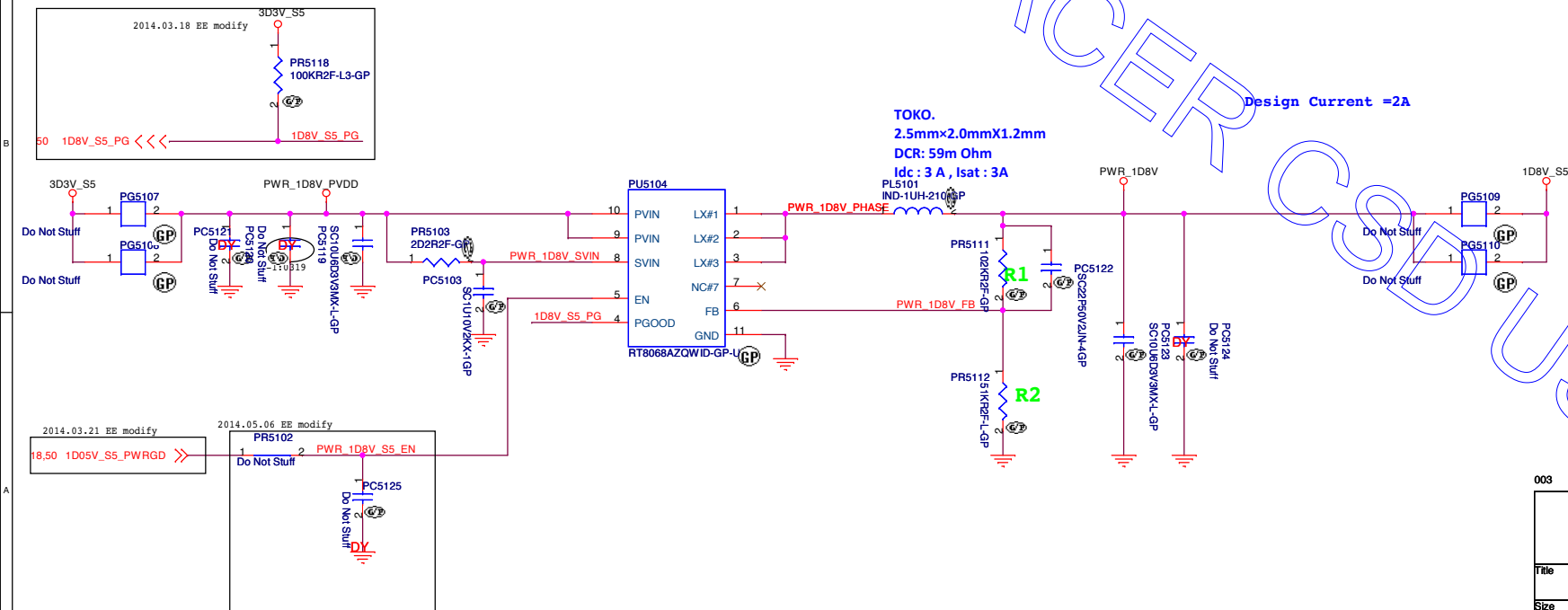


RT9043GB for 1D24V

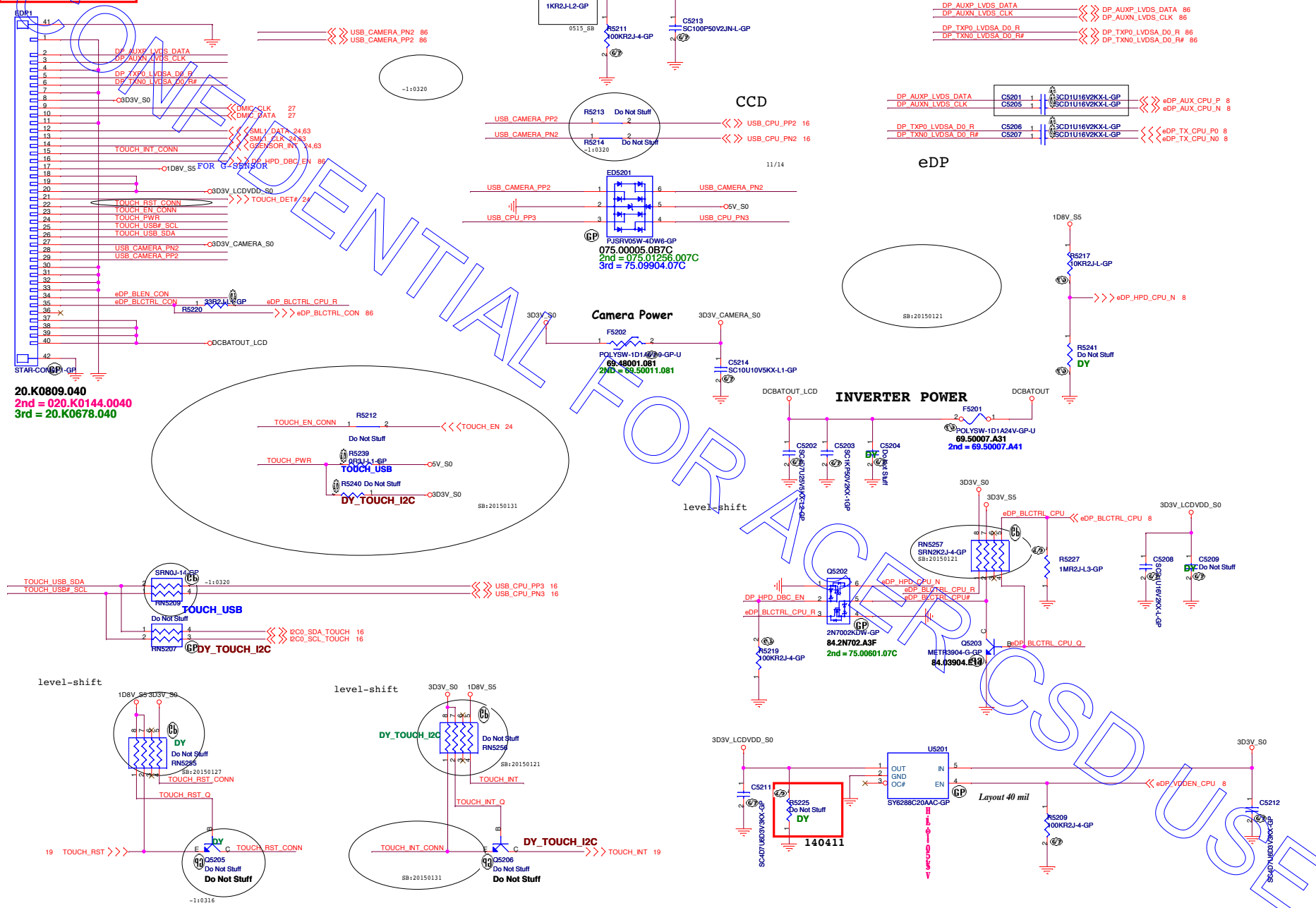


SSID = PWR.Plane.Regulator_1p8v

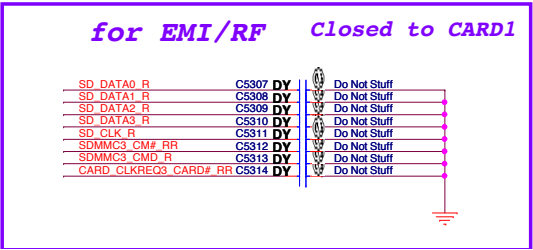
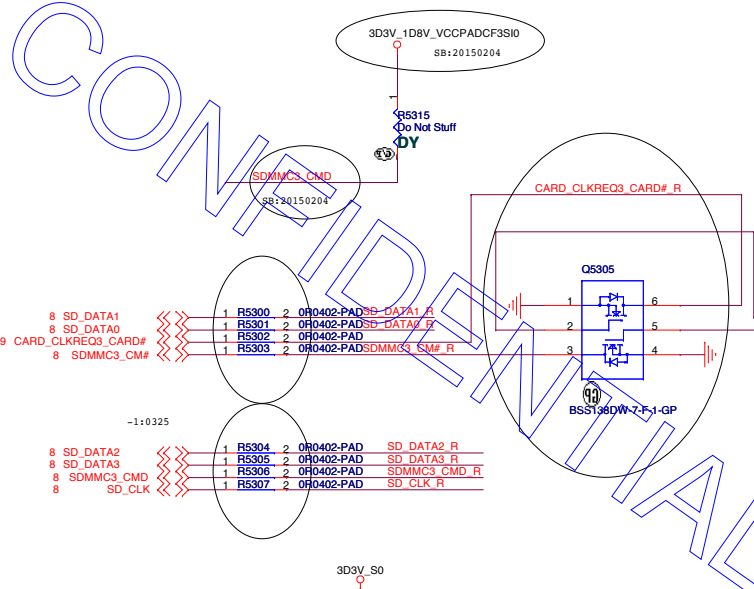
RT8068AZQWID-GP-U for 1D8V_S5



SSID = VIDEO

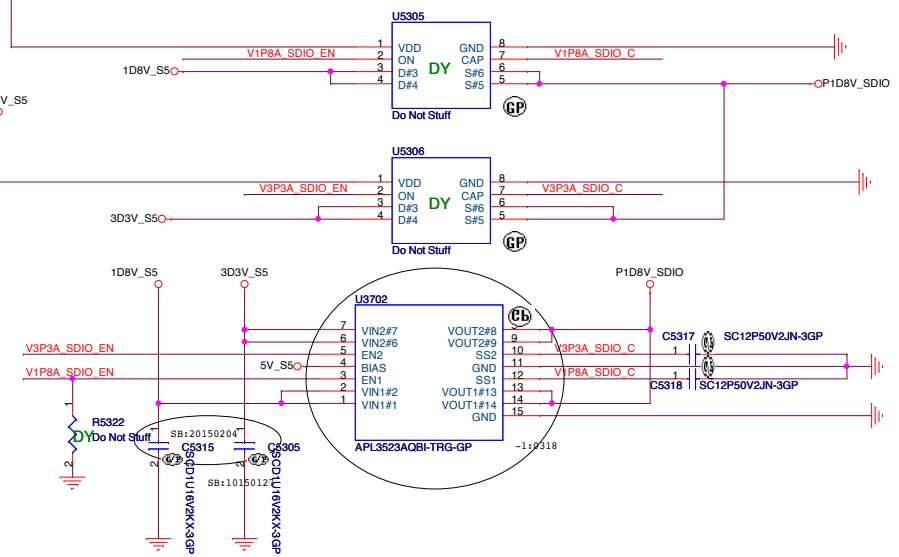
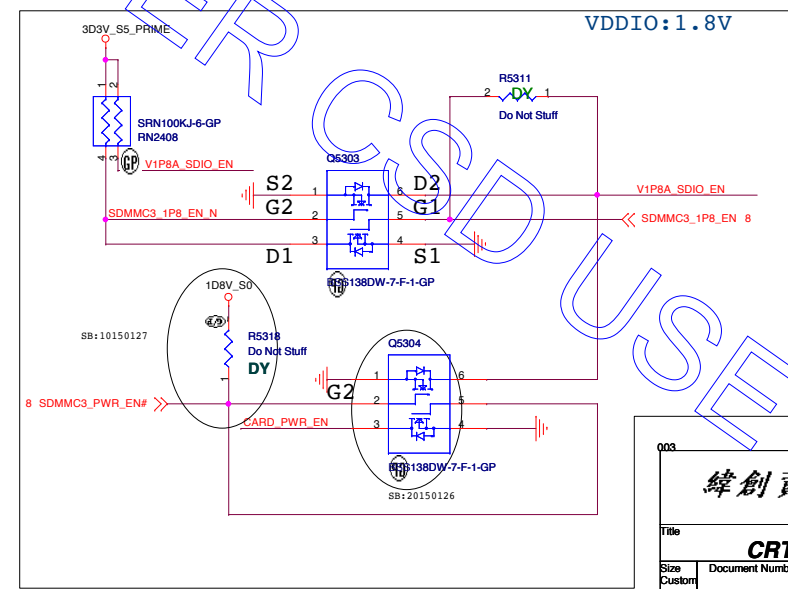
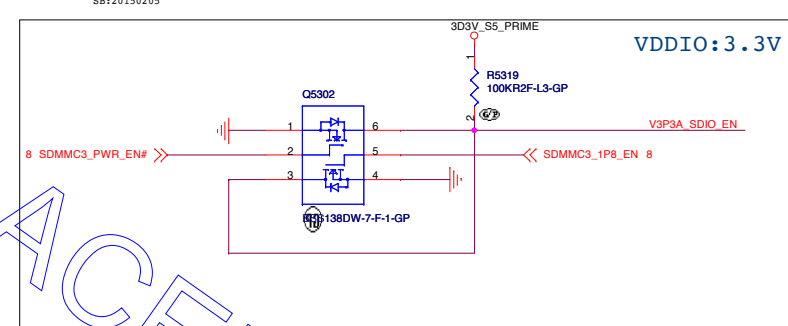
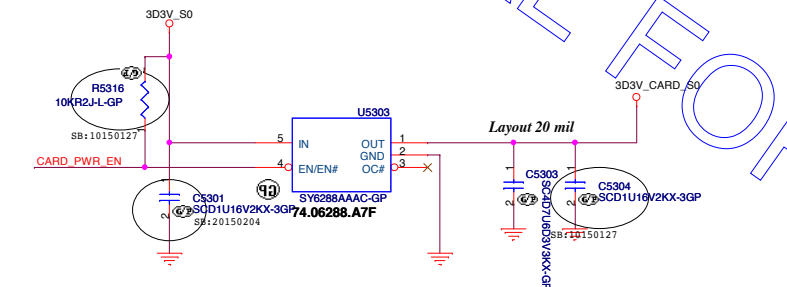


003		003	
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD Connector			
Size	Document Number	How	
Custom	Chopper BA	-1	
Date:	Wednesday, March 2, 2016	Time:	10:27



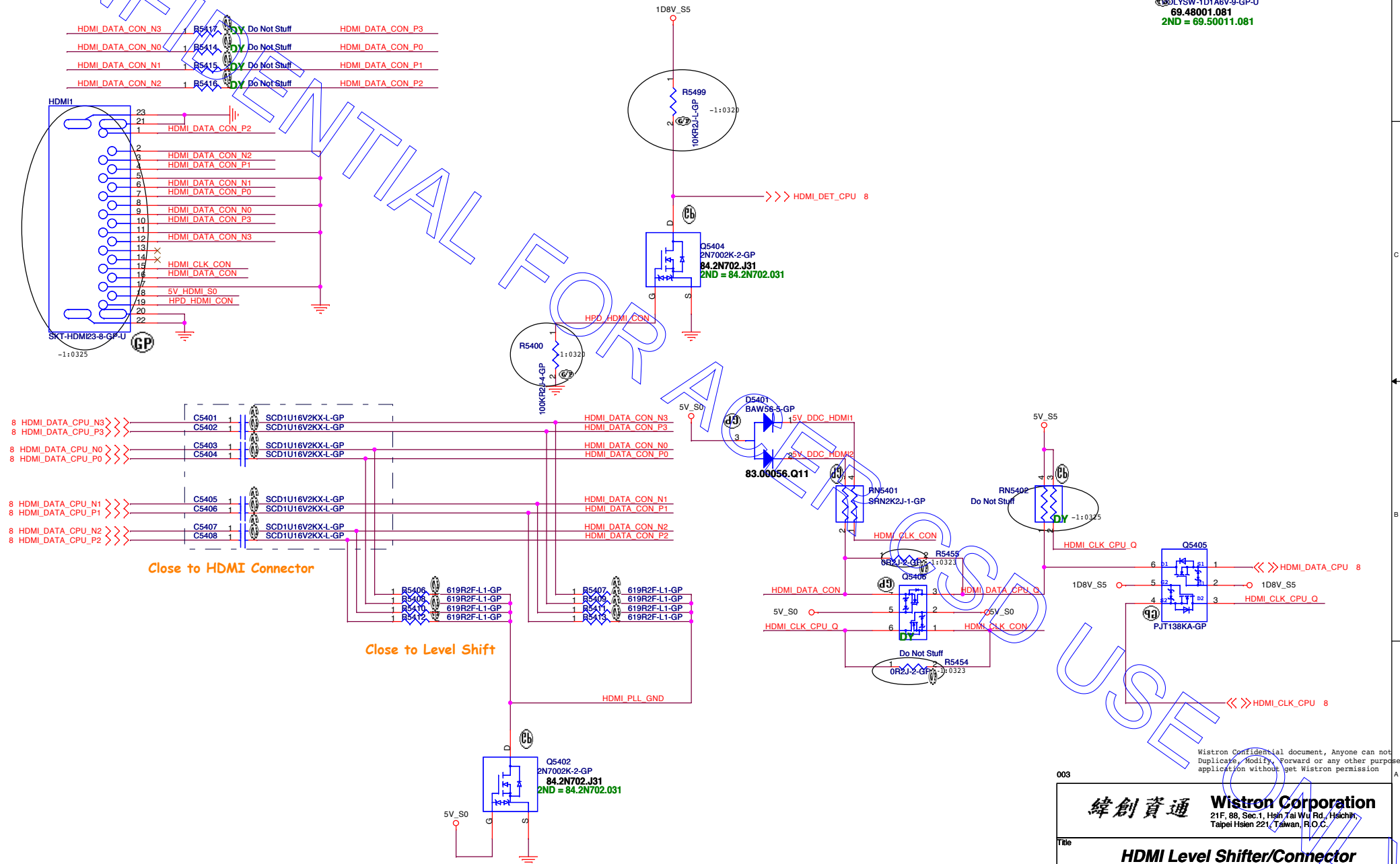
VSDIO VOLTAGE SETTING

SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO (V)
1	0	0V
1	1	0V
0	0	3.3V
0	1	1.8V



SSID = VIDEO *HDMI Level Shifter & CONNECTOR*

HDMI CONN



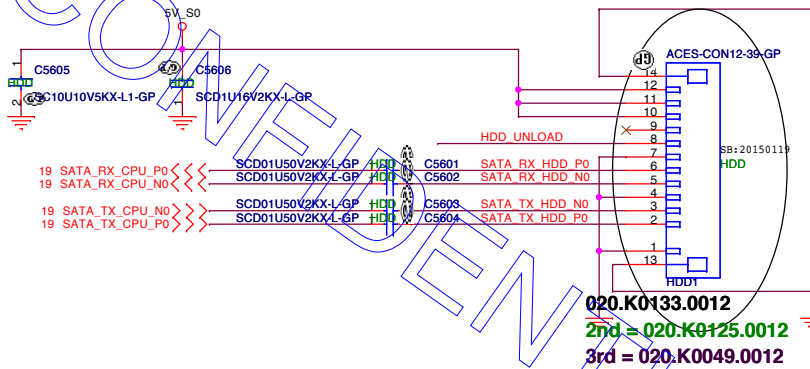
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Title		
Reserved		
Size	Document Number	Rev
A4	Chopper BA	-1
Date:	Monday, March 16, 2015	Sheet 55 of 102

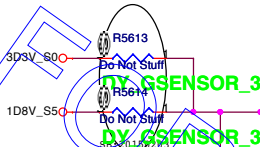
SSID = SATA

SATA HDD Connector



*CS="H"; mode="I2C"
CS="L"; mode="SPI"

SDO="H"; address="3Ah"
*SDO="L"; address="38h"



DY_GSENSOR_3

DY_GSENSOR_3

DY_GSENSOR_3

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DY_GSENSOR_3

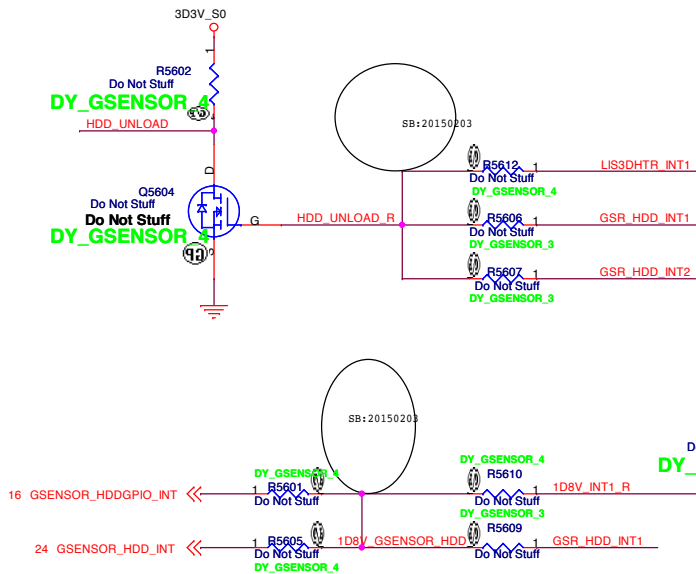
DY_GSENSOR_3

DY_GSENSOR_3

DY_GSENSOR_3

DY_GSENSOR_3

DY_GSENSOR_3



DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

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DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

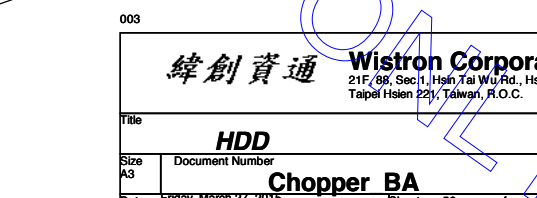
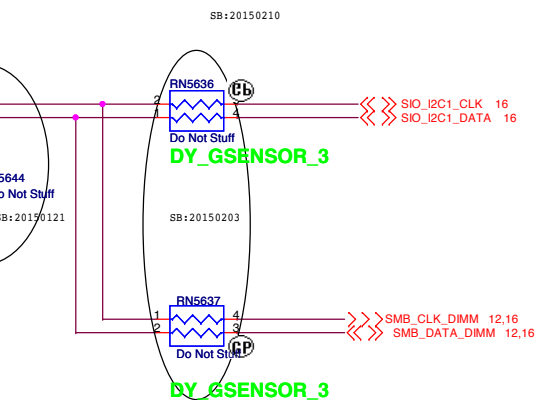
DY_GSENSOR_4

DY_GSENSOR_4

DY_GSENSOR_4

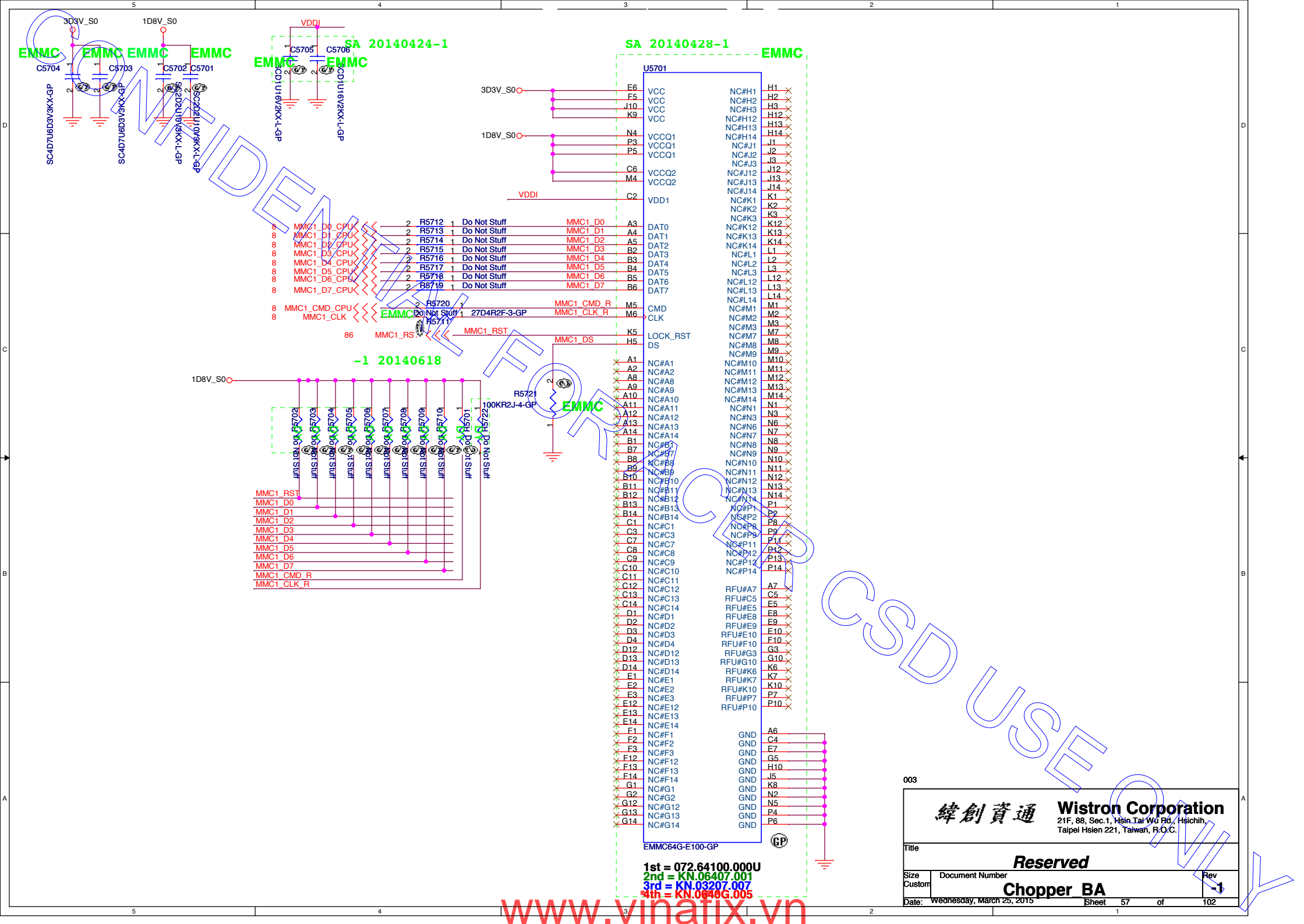
DY_GSENSOR_4

DY_GSENSOR_4

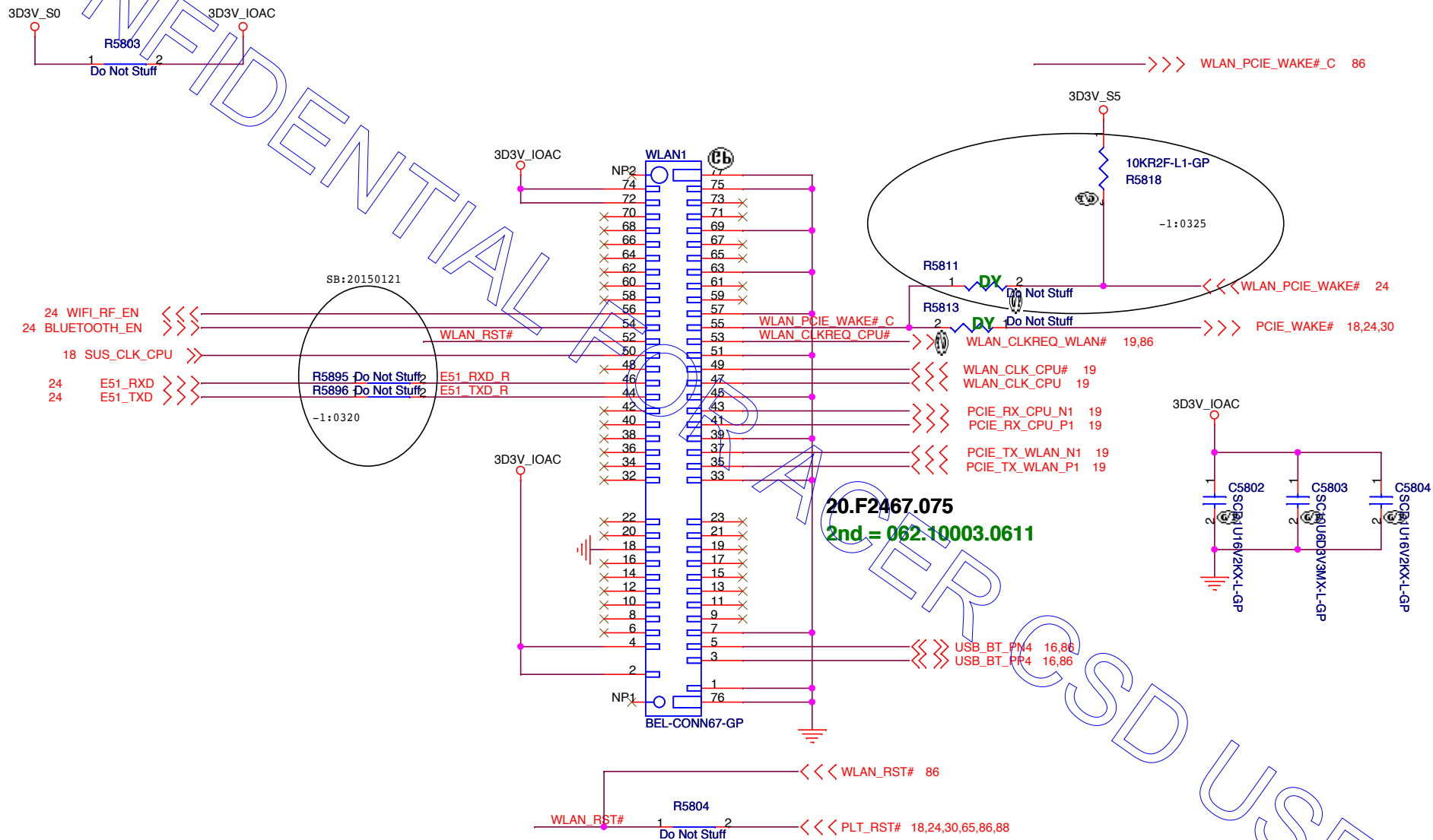


003

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Title HDD	
Size A3	Document Number
Date: Friday, March 27, 2015	
Sheet 56 of 102	
Rev -1	



SSID = Wireless NGFF Connector(802.11a/b/g/n)



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Title			
MINICARD(WLAN)			
Size	Document Number	Rev	
Custom	Chopper BA	-1	
Date:	Wednesday, March 25, 2015	Sheet	58 of 102

SSID = 3G

Mini Card Connector(WWAN)

Blanking

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Title

WWAN CONN

Size
A4

Document Number

Chopper BA

Rev
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SSID = mSATA

Mini Card Connector(mSATA)

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Title

Reserved

Size
A4

Document Number

Chopper BA

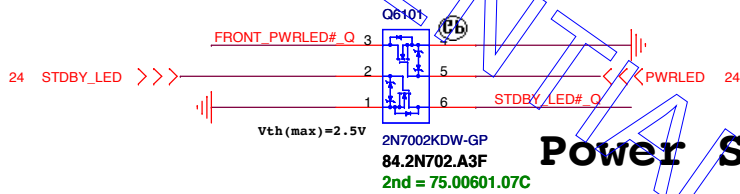
Rev
-1

Date: Monday, March 16, 2015

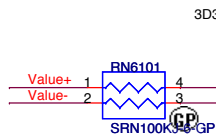
Sheet 60 of 102

SSID = User.Interface

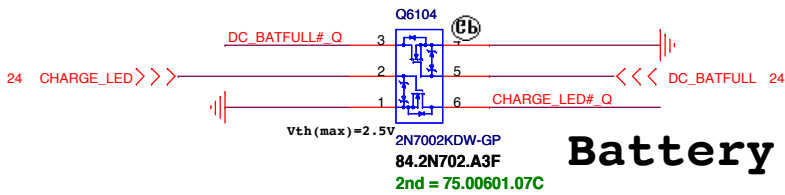
Power button LED



Power STDBY_LED

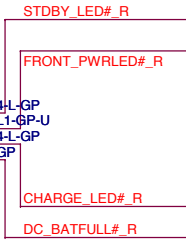
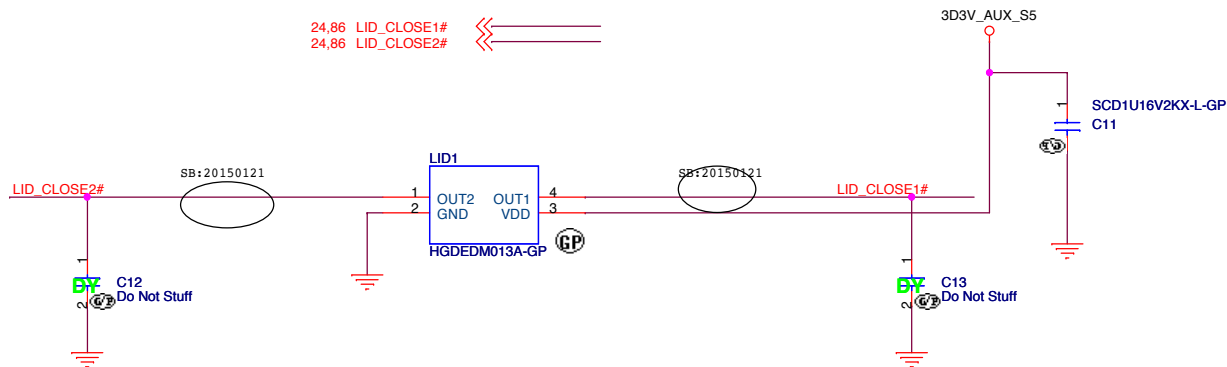


Battery LED2 (DC_BATFULL)

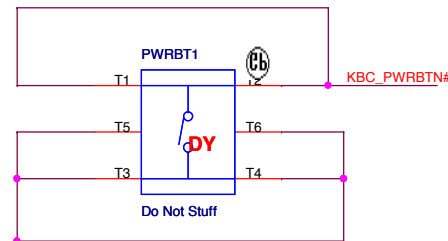
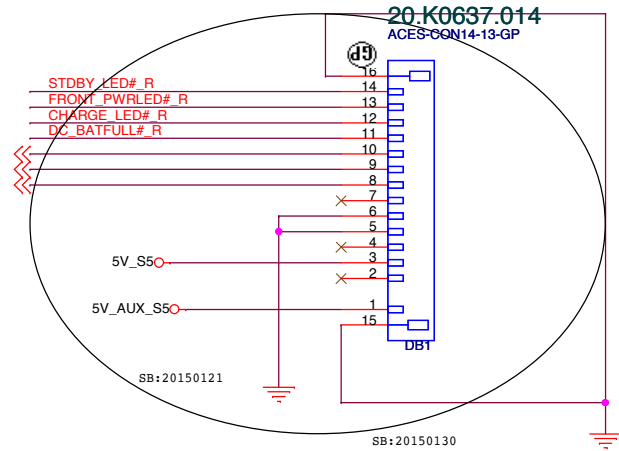


Battery LED1 (CHARGE)

24,86 LID_CLOSE1#
24,86 LID_CLOSE2#



24,86 KBC_PWRBTN#
24 Value+
24 Value-



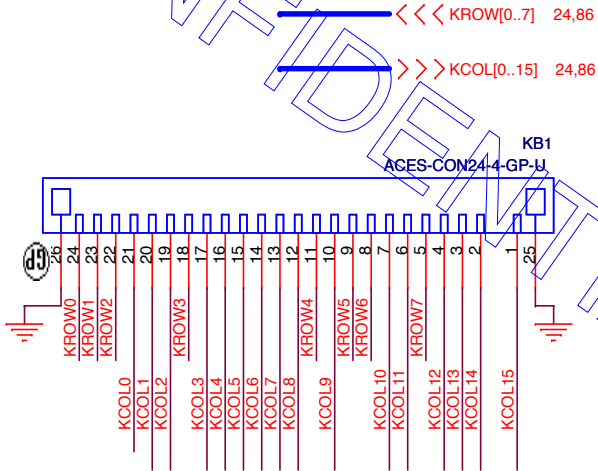
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Title LED Bard/Power Button	
Size Custom	Document Number Chopper BA
Date: Wednesday, March 25, 2015	Sheet 61 of 102
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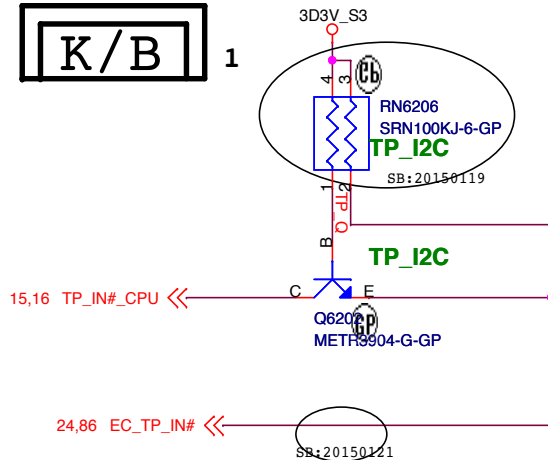
SSID = KBC

Internal Keyboard Connector

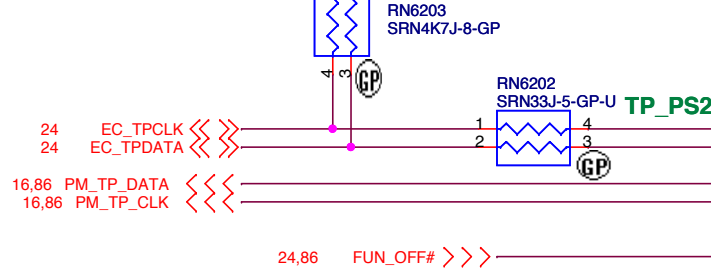


MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

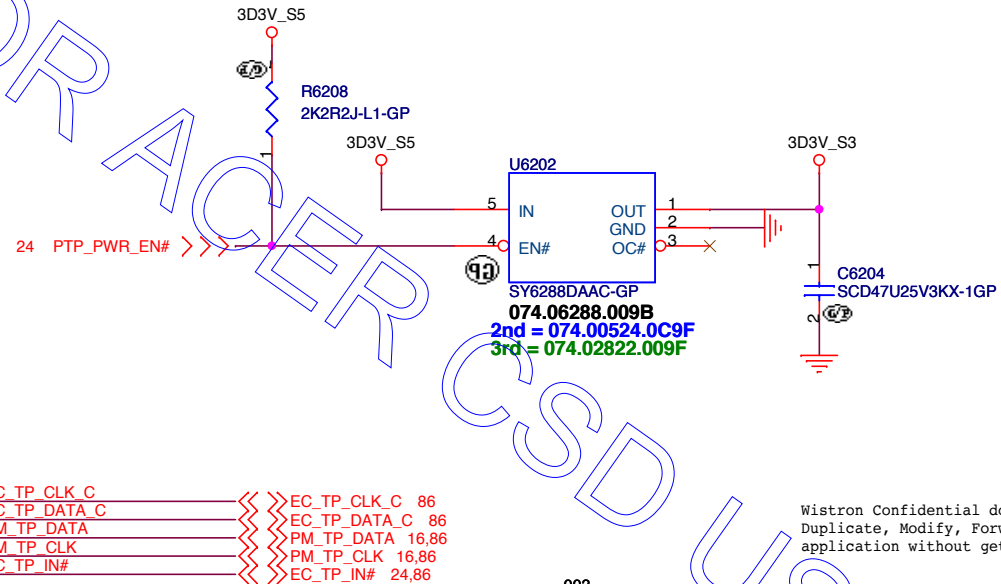
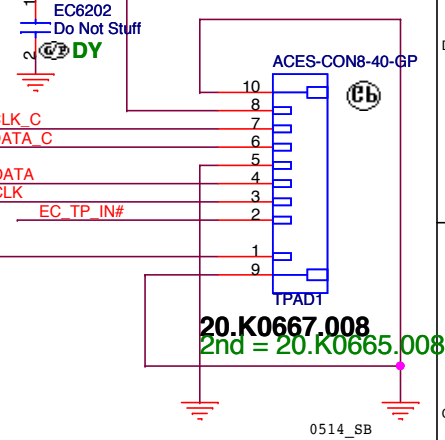
24 **K/B** 1



TP_PS2



TOUCH PAD



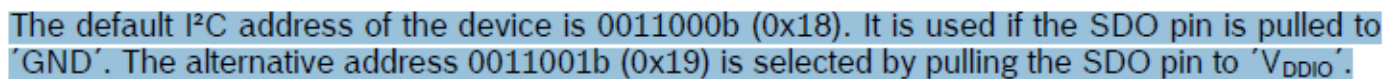
EC_TP_CLK_C 86
EC_TP_DATA_C 86
PM_TP_DATA 16,86
PM_TP_CLK 16,86
EC_TP_IN# 24,86

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Title			
Key Board/Touch Pad			
Size	Document Number	Rev	
Custom	Chopper BA	-1	
Date:	Wednesday, March 25, 2015	Sheet	62 of 102

G Sensor

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



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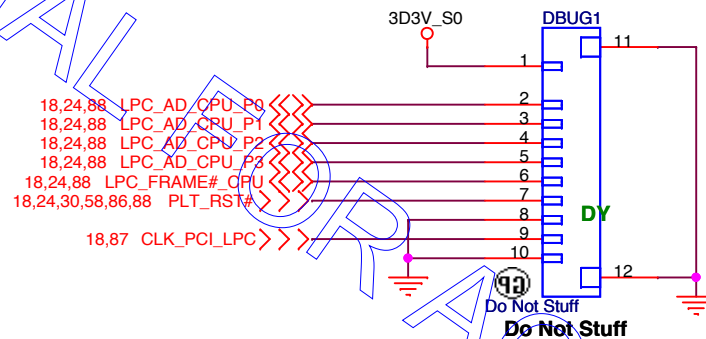
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Title		
Hall Sensor		
Size	Document Number	Rev
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Title

Dubug connector

Size

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Title

Reserved

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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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Title			
G Sensor			
Size A	Document Number		Rev
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Title

Thunderbolt (1/5)

Size
A4

Document Number

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Title

Thunderbolt (2/5)

Size
A4

Document Number

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Title

Thunderbolt (3/5)

Size
A4

Document Number

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Title

Thunderbolt (4/5)

Size
A4

Document Number

Chopper BA

Rev

-1

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Title

Thunderbolt (5/5)

Size
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Title		
GPU(PEG)		
Size	Document Number	Rev
A4	Chopper BA	-1
Date: Monday, March 16, 2015		Sheet 73 of 102

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Title		
GPU (DIGITALOUT)		
Size	Document Number	Rev
A4	Chopper BA	-1
Date: Monday, March 16, 2015		Sheet 74 of 102

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Title		
GPU (VRAM I/F)		
Size	Document Number	Rev
A4	Chopper BA	-1
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Title		
GPU (GPIO/STRAP)		
Size	Document Number	Rev
A4	Chopper BA	-1
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Title		
GPU (POWER/GND)		
Size	Document Number	Rev
A4	Chopper BA	-1
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Title		
GPU-VRAM1,2 (1/4)		
Size	Document Number	Rev
A4	Chopper BA	-1
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Title		
GPU-VRAM3,4 (2/4)		
Size	Document Number	Rev
A4	Chopper BA	-1
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Title		
GPU-VRAM5,6 (3/4)		
Size	Document Number	Rev
A4	Chopper BA	-1
Date:	Monday, March 16, 2015	Sheet 80 of 102

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Title		
GPU-VRAM7,8 (4/4)		
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A4	Chopper BA	-1
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Title		
RT8812A VGA CORE		
Size	Document Number	Rev
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Title		
DISCRETE VGA POWER		
Size	Document Number	Rev
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Title

Switchable GFX LCD(1/2)

Size
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Switchable GFX LCD(2/2)

Size
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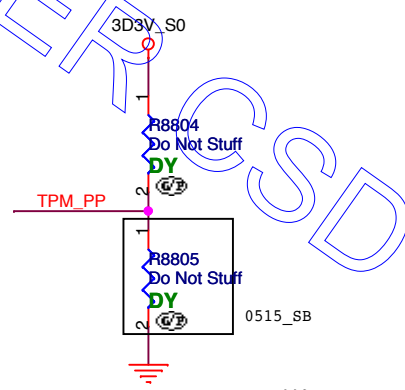
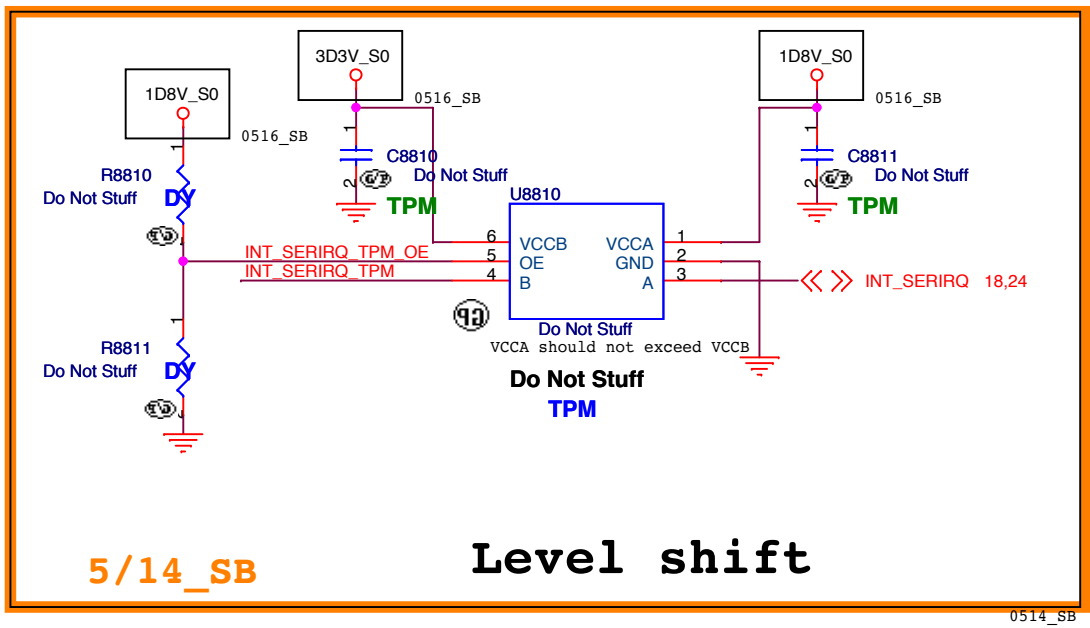
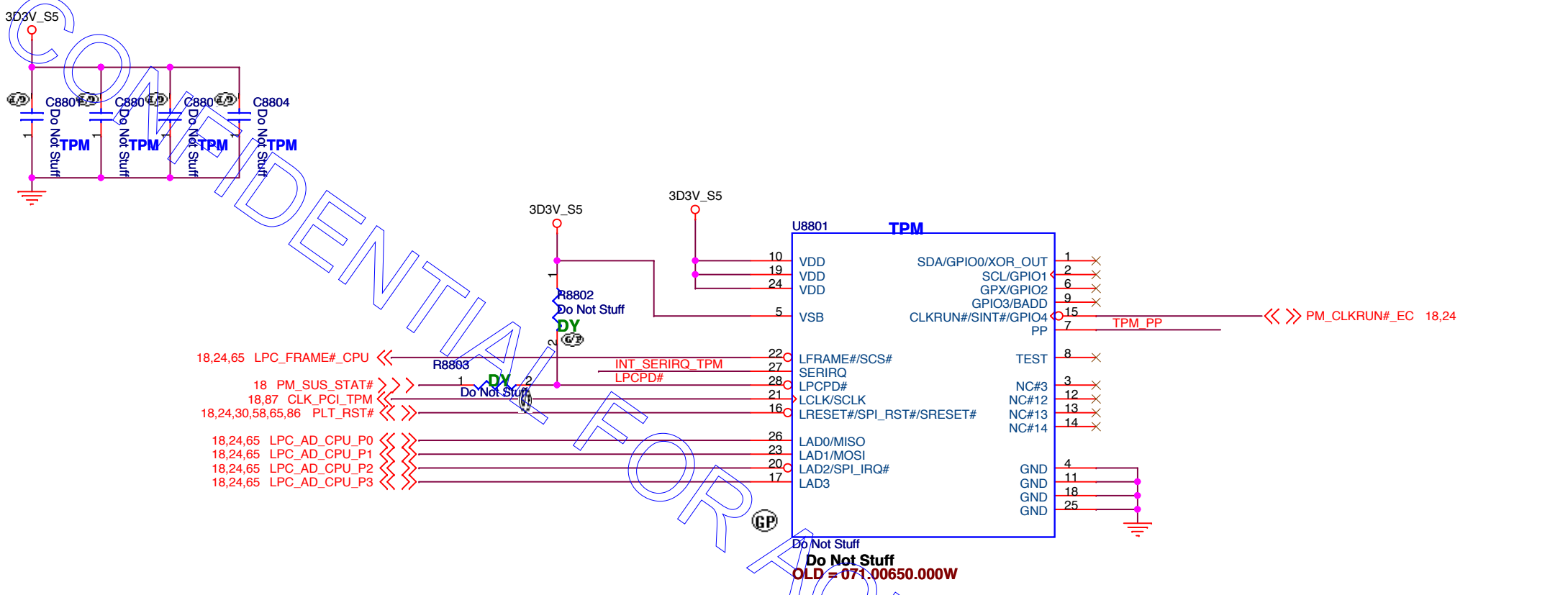
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SSID = Finger Print

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SSID = Smart Card

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SSID = Docking

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SSID = Intel LAN

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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RTIC_R5T# (VRTC)

RTC_RST# (RTEST)

DCBATOUT

3D3V_AUX_55 (-V3P3A_LDO)

S5_ENABLE

SV_55 (+V5A)

3D3V_55 (-V3P3A)

MB_PWR_BTN# (PS_ON_SW_N)

S5SPWRDNACK_SOC_EC

I2DSV_55 (-V1P05A)

I2D1SV_55 (-V1P15A)

I2D4V_55 (-V1P24A)

I2DV_55 (-V1P8A)

3D3V_55_PRIME (-V3P3A_PRIME)

PCH_RSMRST# (RSMRST_N)

AC_PRESENT (PMU_AC_PRESENT)

PMU_PWRSTN#_CPU (PMU_PWRSTN_N)

SIO_SLP_S4# (PMU_SLP_S4_N)

I2DSV_53 (-VDDQ)

DDR_VREF_53 (-VDDQ_VREF)

DDR3_DRAM_PWROK (DDR3_DRAM_PWROK)

SIO_SLP_S3# (PMU_SLP_S3_N)

SV_50

3D3V_50 (-V3P35)

I2DV_50 (-V1P55)

OD67SV_50 (-VDDQ_VTT)

6PX_CORE (-V66)

VCC_CORE0 (VCC0_CPU)

VCC_CORE1 (-VCC1_CPU)

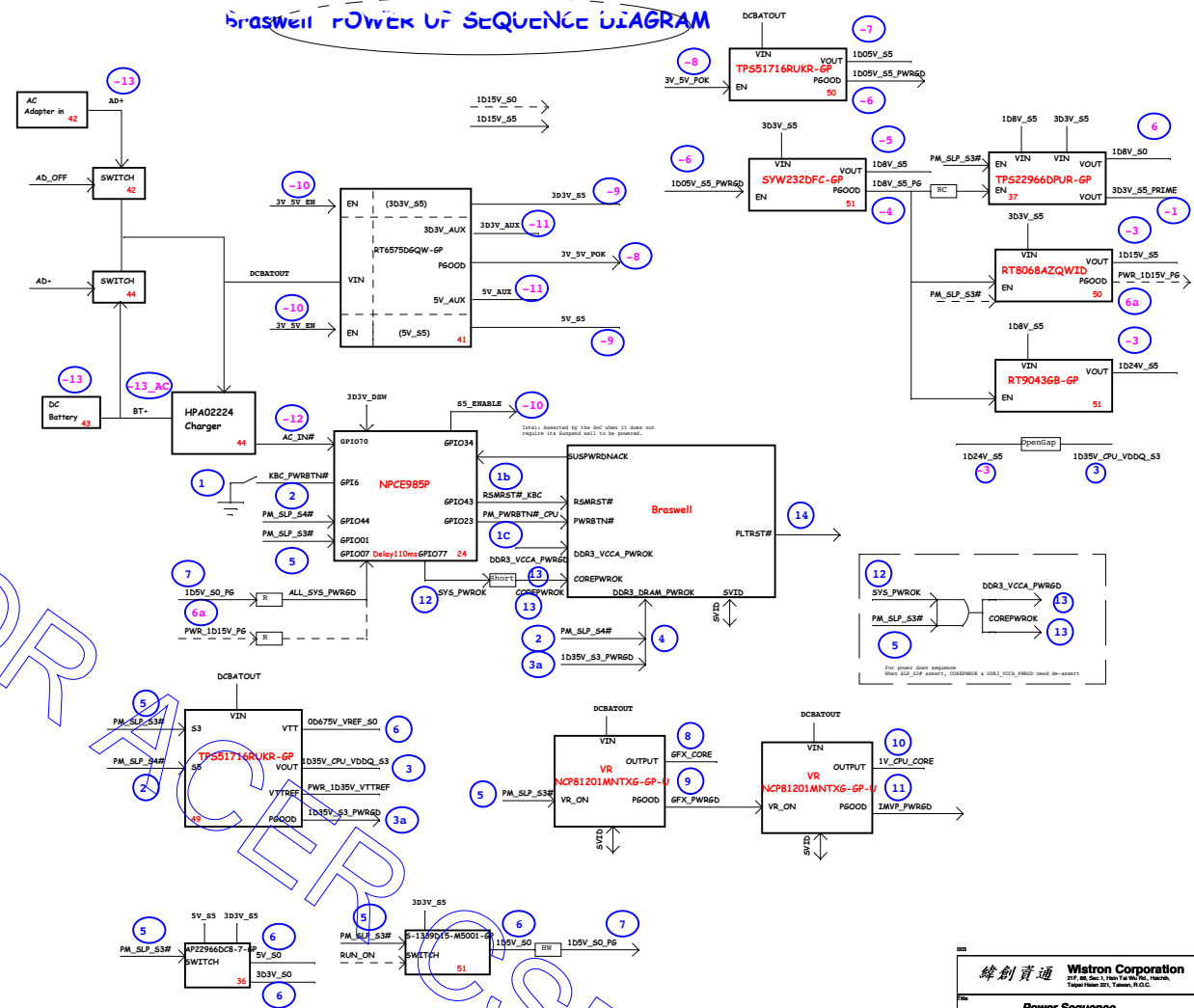
IMVP_PWRGD

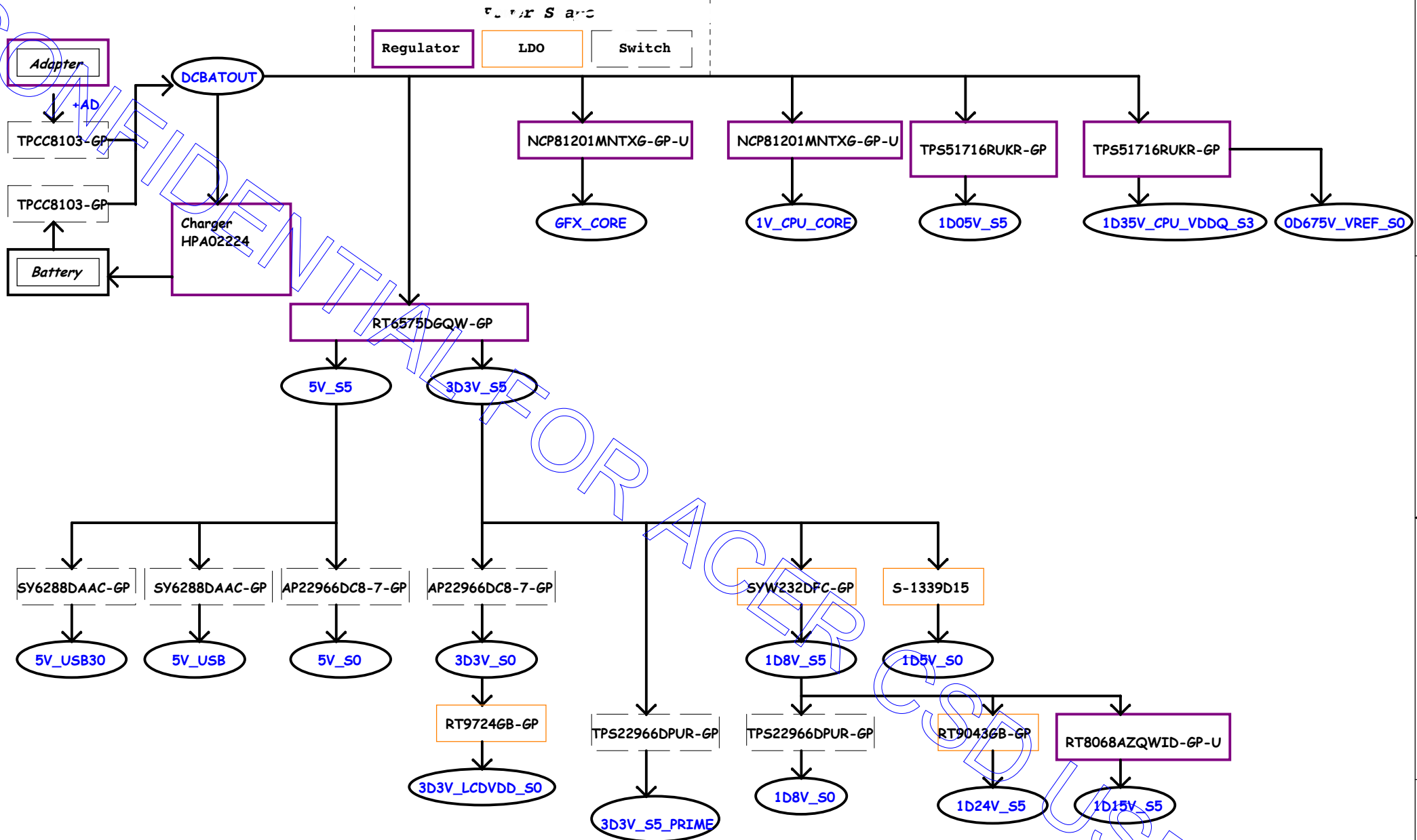
SYS_PWROK (EC_DELAY_ALL_SYS_PWROD)

COREPWROK

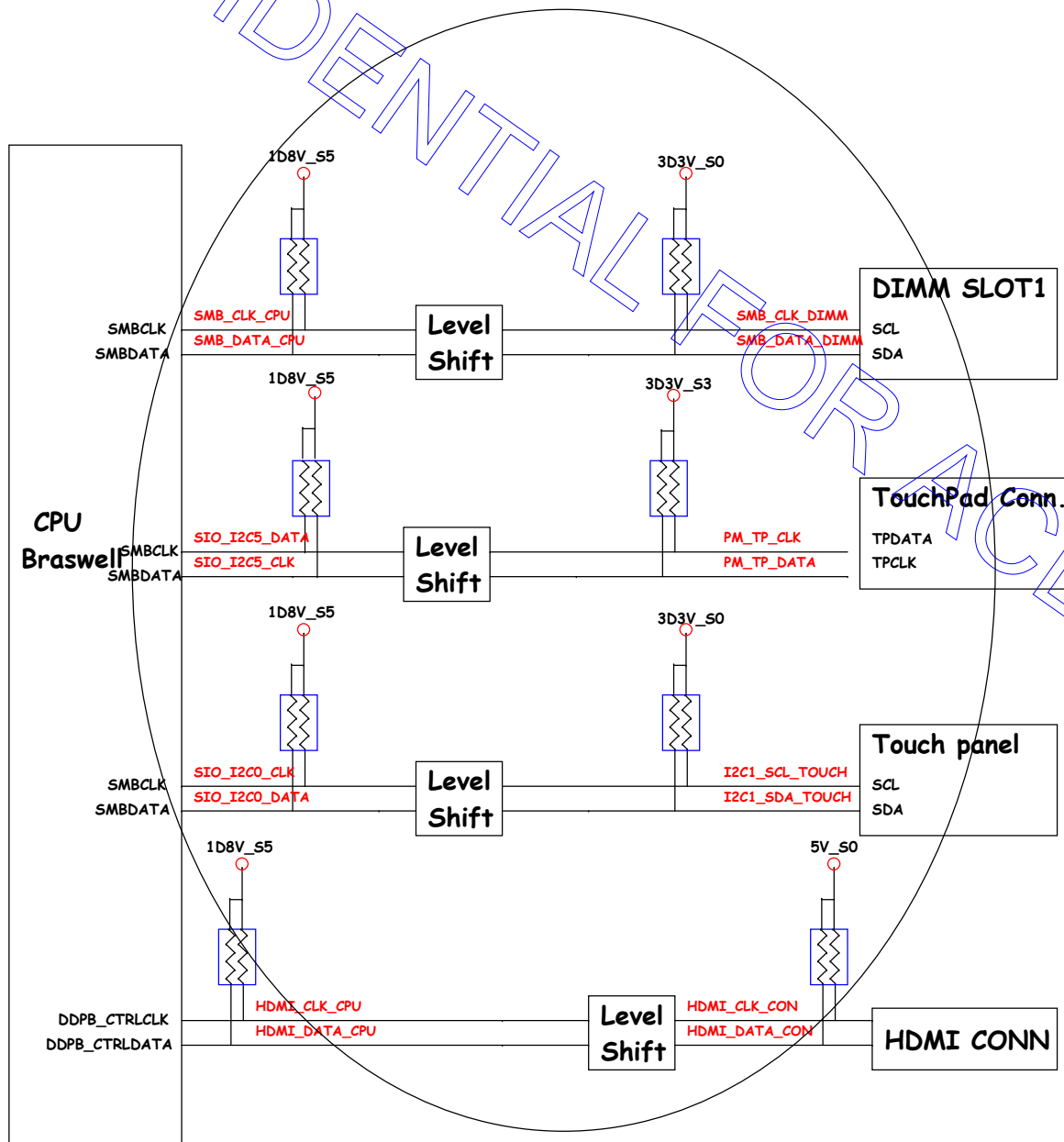
DDR3_VCCA_PWROK

PLT_RST#_CPU

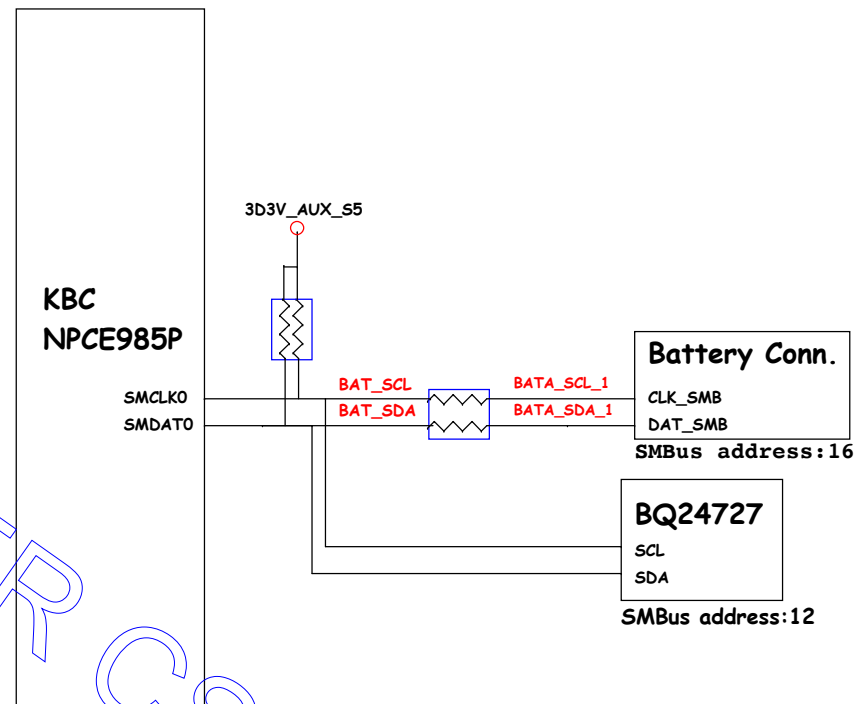




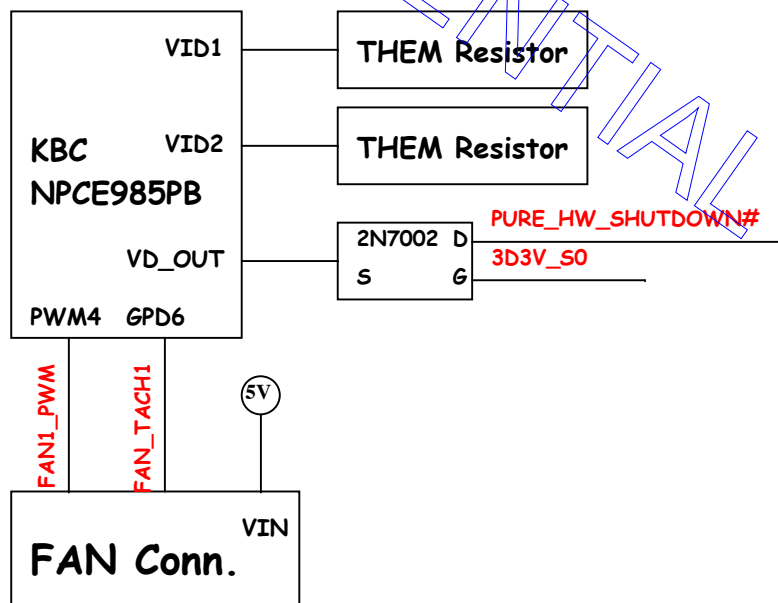
PCH SMBus Block Diagram



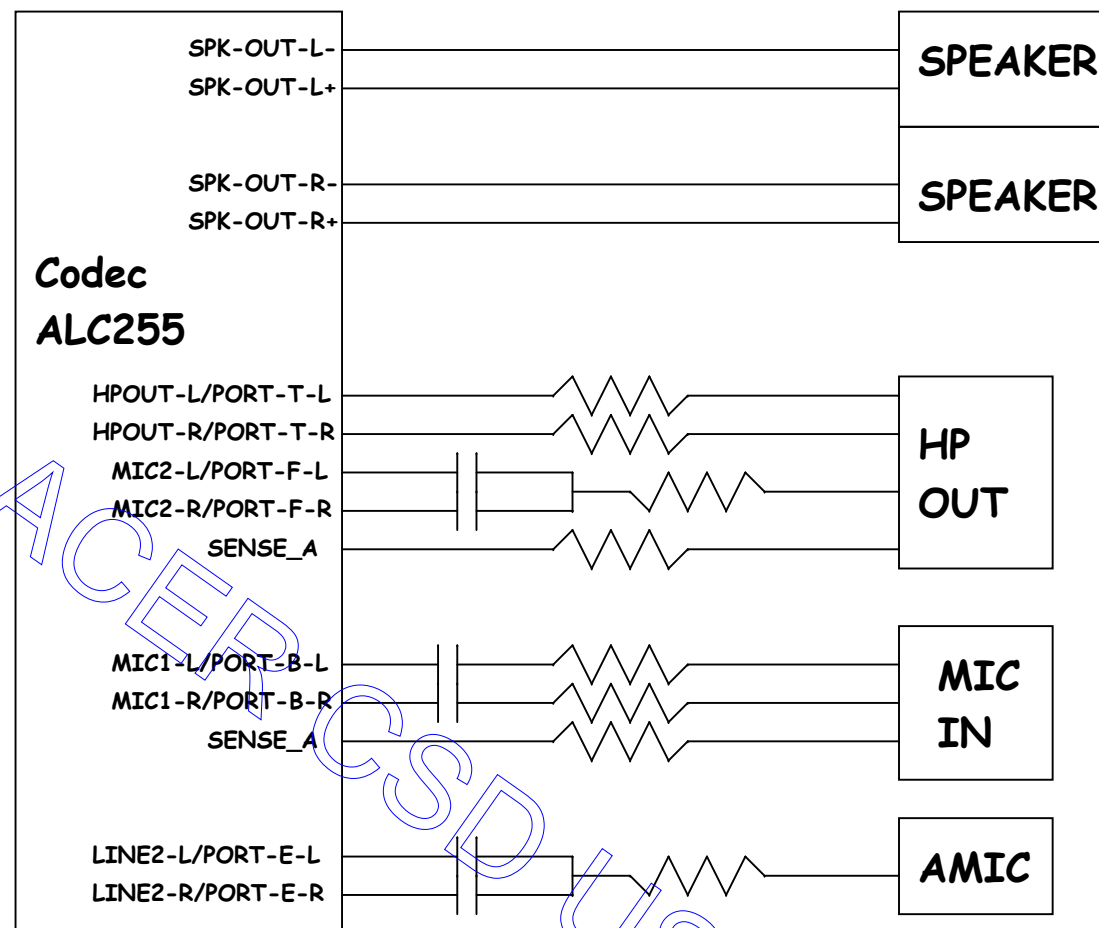
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

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