ACER_BAP31

MAIN BOARD

2008.12.29

DATE	CHANGE NO.	REV
Tuesday, March 10, 2009		X01

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE ACER_JM31

SIZE	CODE	DOC.NUMBER	REV
C	X01	D-CS-1310A284501-ALG	X01

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Montevina Schematic Ver : X01

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8. Adaptor in/Charge
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26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN

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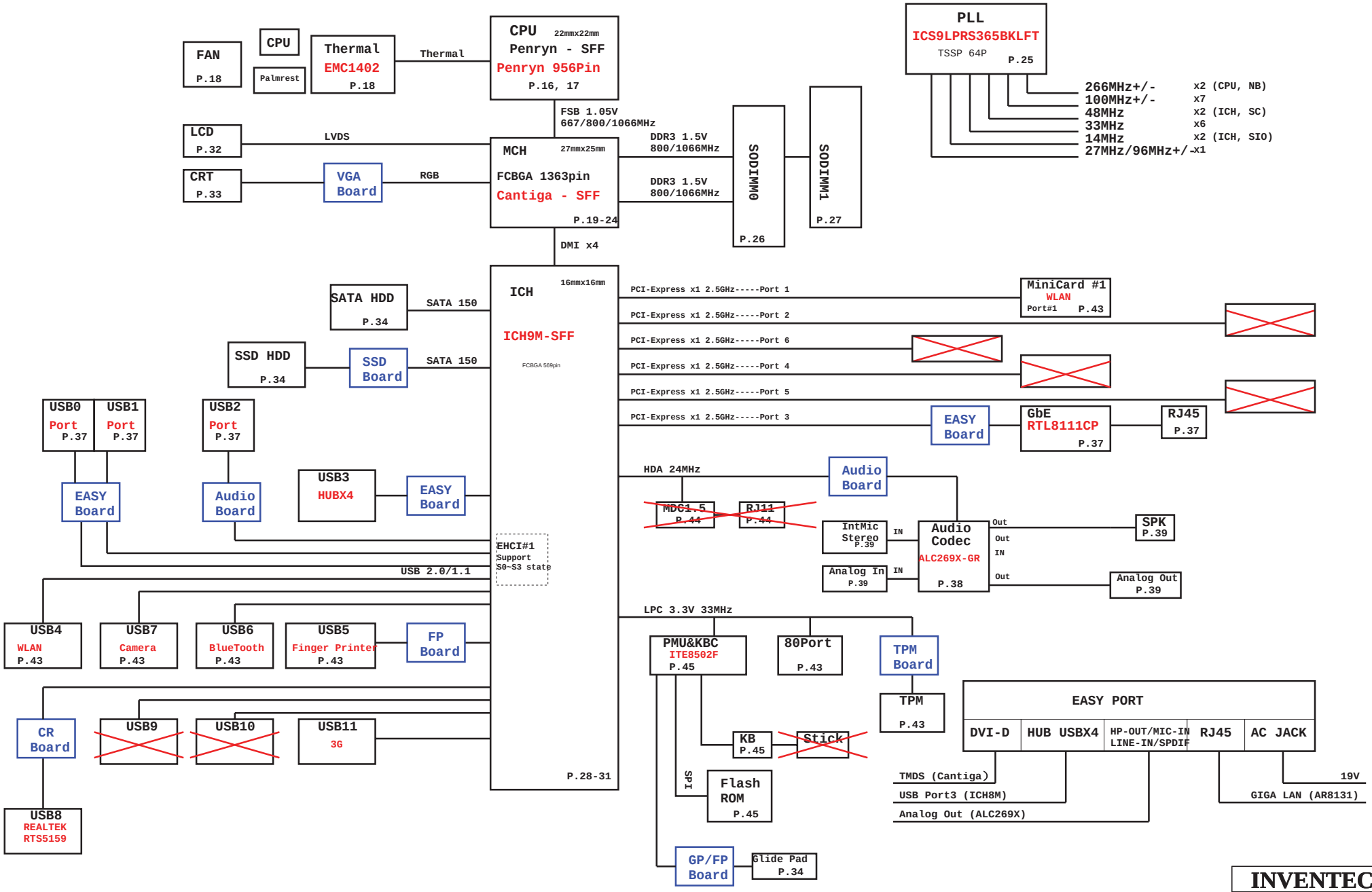
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET 2 of 36

檔

3. Block Diagram :



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INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

INVENTEC

TITLE			
BAP31 (Penryn+Cantiga+ICH9M)SFF ANNOTATIONS			
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miiles Liu DATE Tuesday, March 10, 2009 SHEET 4 of 36

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6.Schematic modify Item and History :

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,
   Modify CN5 -----P28
2. Modify CN20 to 50pin-------P33
3. Move PWR_SWIN# from CN14 to CN20
4. ADD TPM module------P34

2009.0109

1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

2009.0112

1. Change power item: R490,R291,BAT CNN TH PIN

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Schematic Modify

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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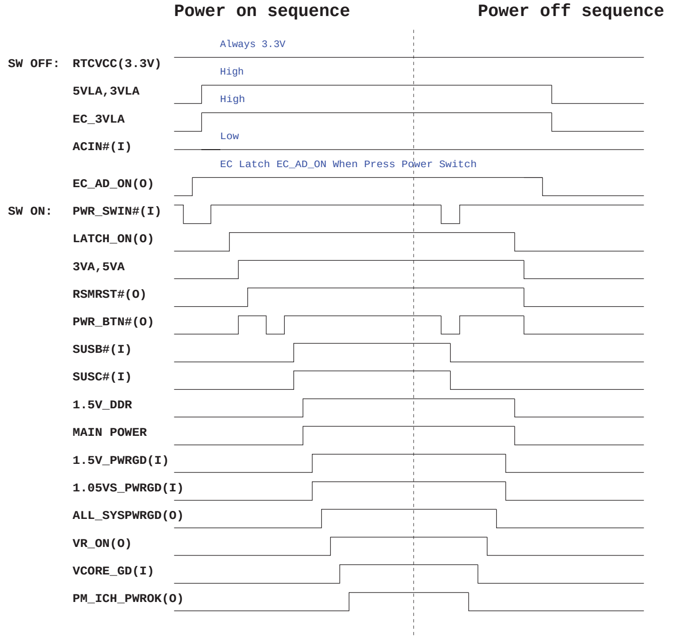
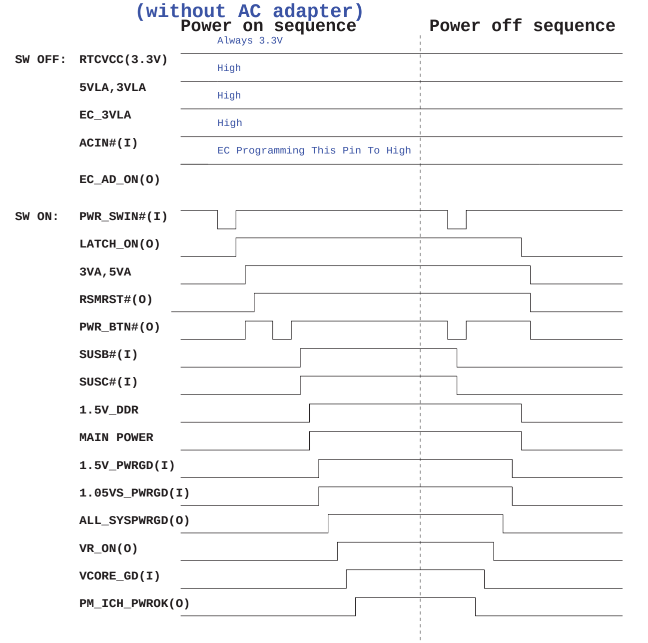
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

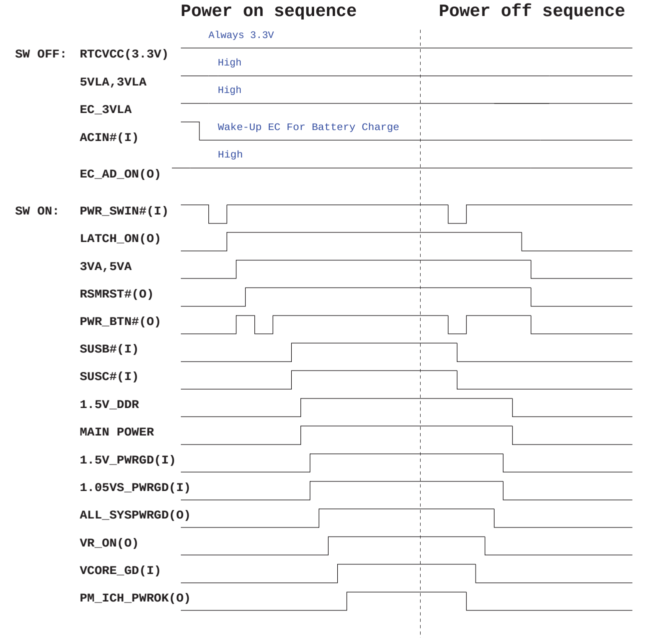
Power on/off sequence AC insert (without Battery Pack)



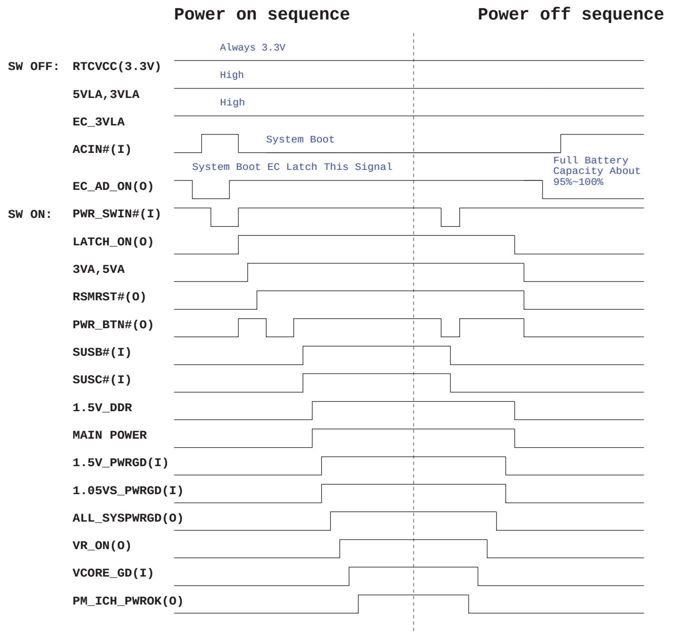
Power on/off sequence Battery insert (without AC adapter)



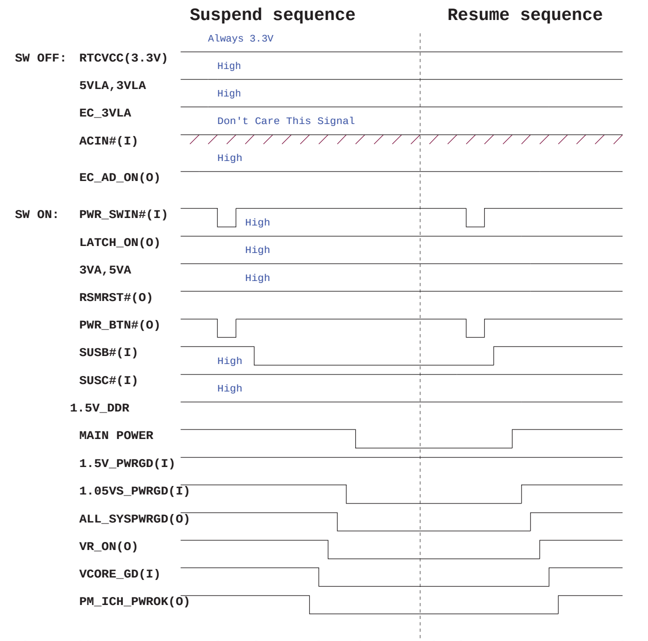
Power on/off sequence AC insert(with charge over 95%)



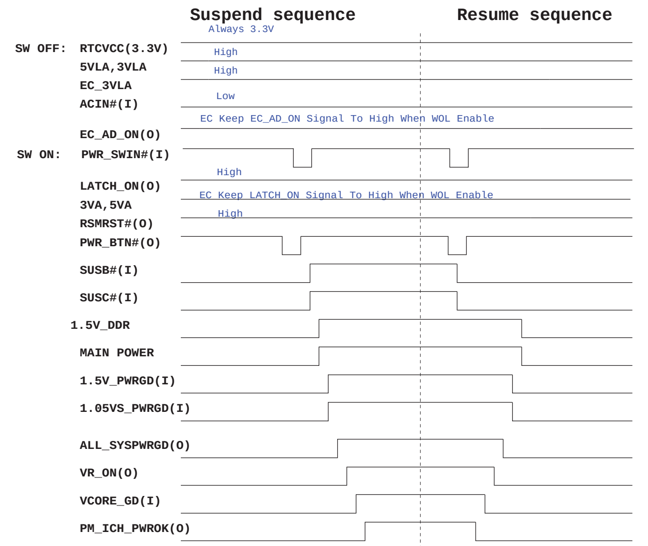
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC			
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF Time Diagram			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
CHANGE by: Miles Liu	DATE: Tuesday, March 10, 2009	SHEET: 6 of 36	

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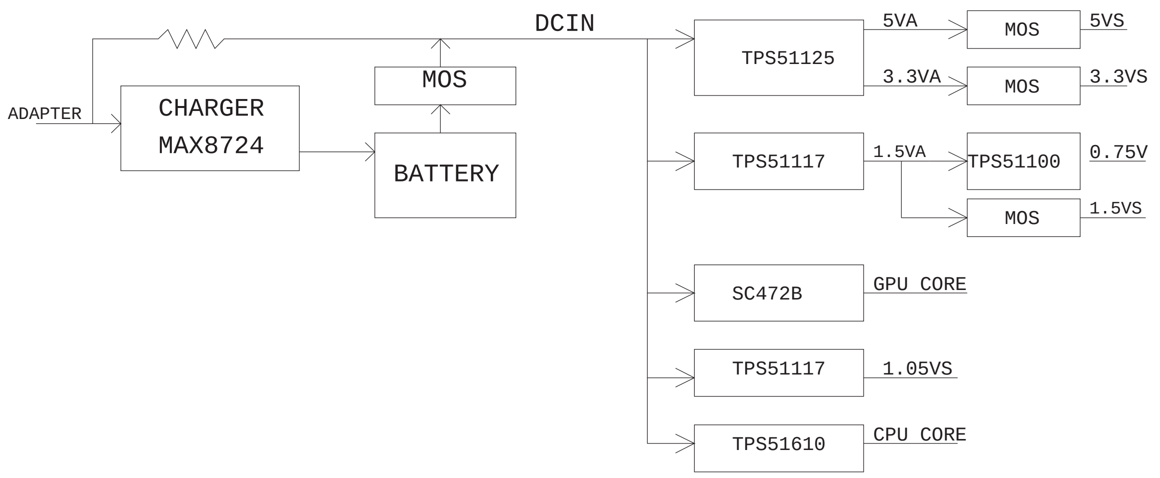
Power Block Diagram :



INVENTEC

TITLE	BAP31 (Penryn+Cantiga+ICH9M)SFF Power Block Diagram		
SIZE C	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
CHANGE by Miiles Liu	DATE Tuesday, March 10, 2009	SHEET 7 of 36	

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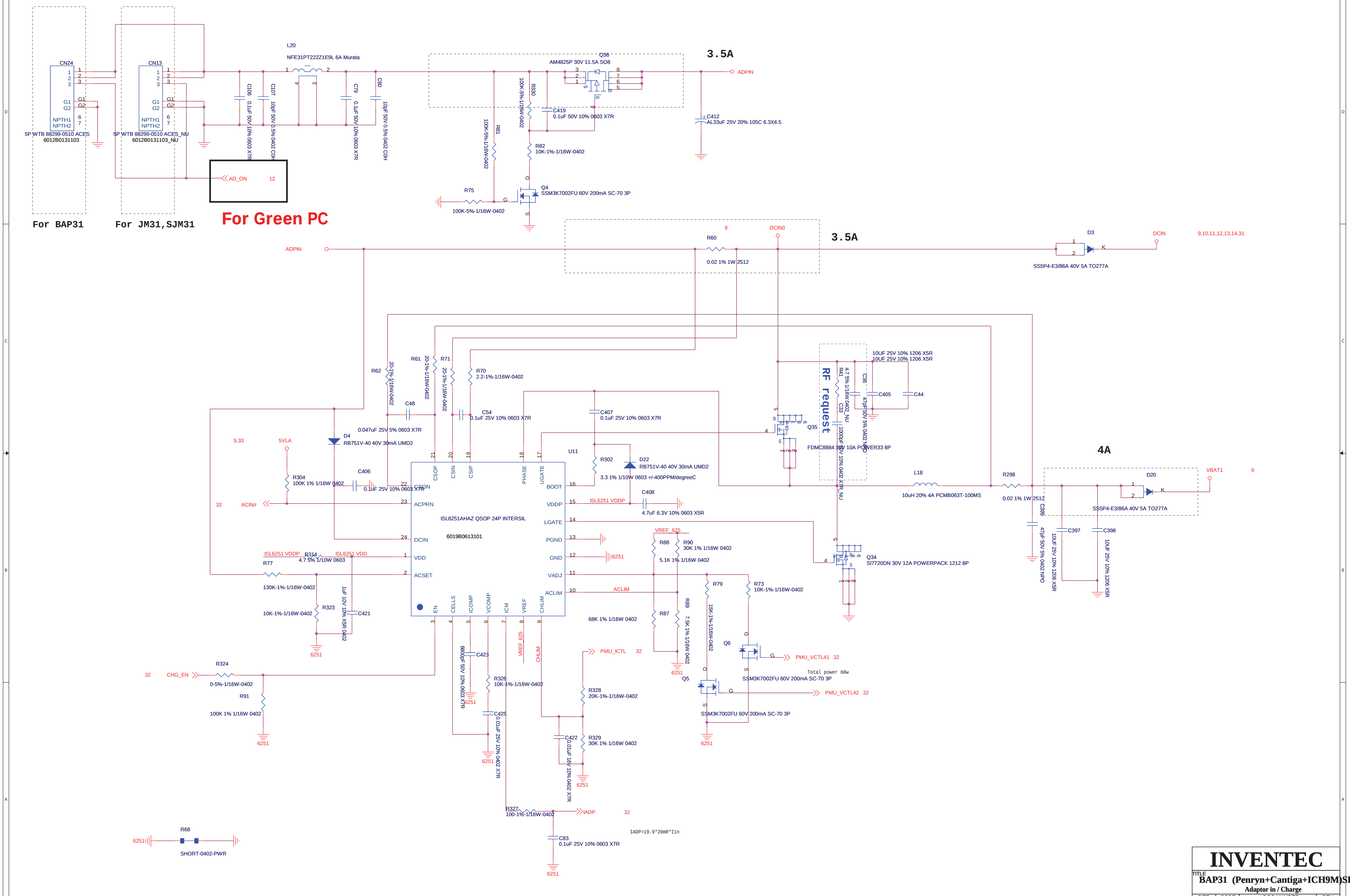

INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
Adaptor in / Charge

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 8 of 36

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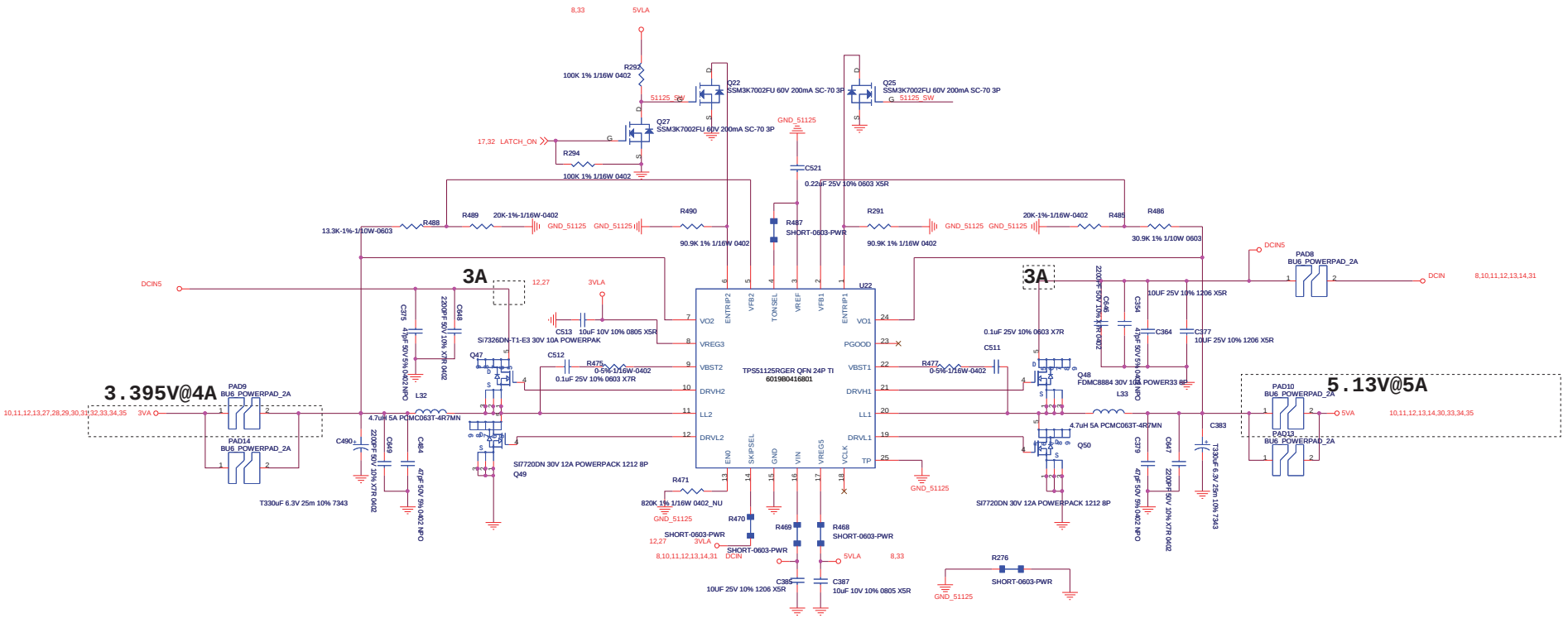
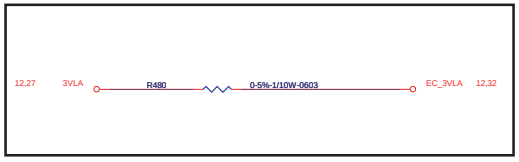
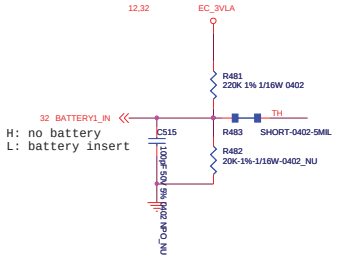
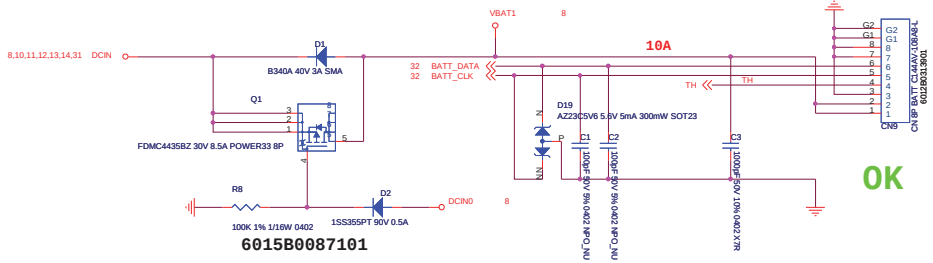


For Green PC







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INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFI
5VLA/5VA/3VLA/3VA

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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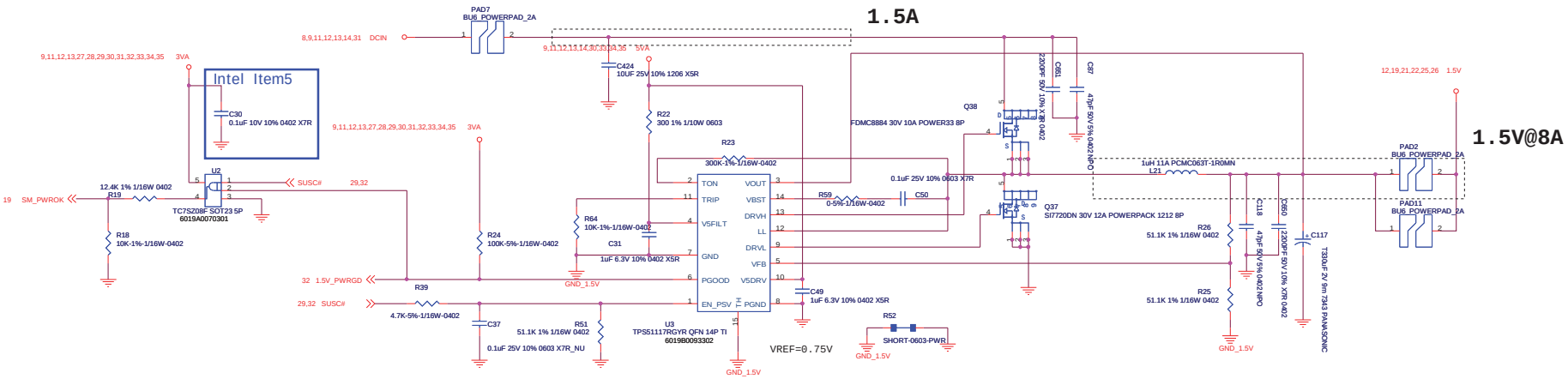

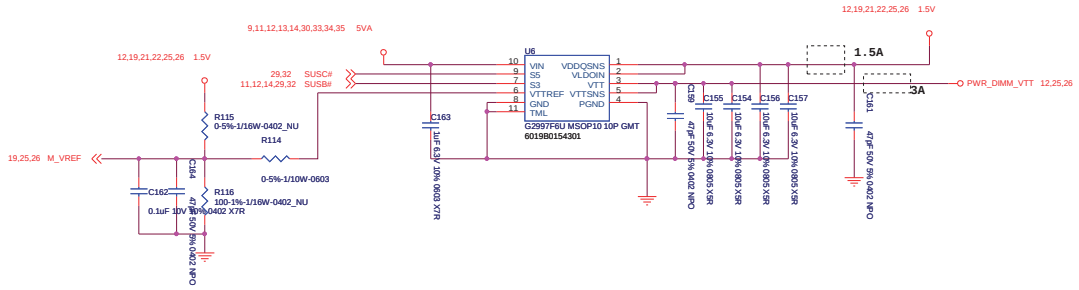

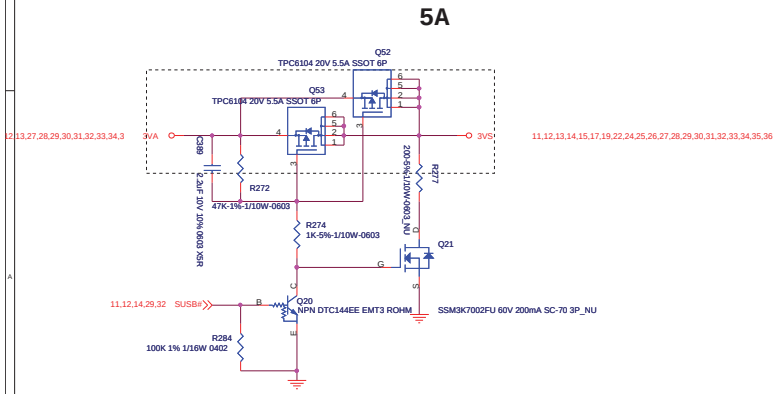

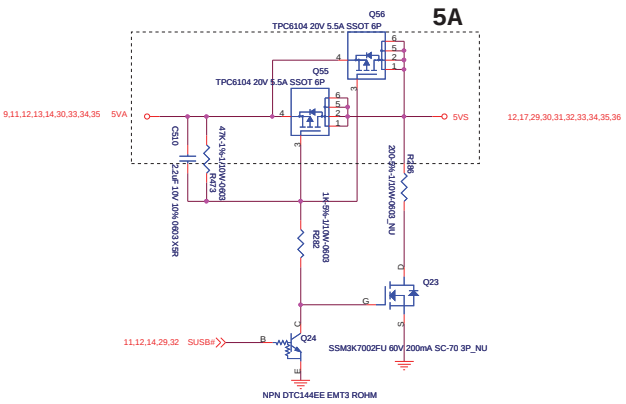

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INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFI
3VS/5VS/1.5V (DDR3)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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CHANGE by Miles Liu DATE Tuesday, March 10, 2009

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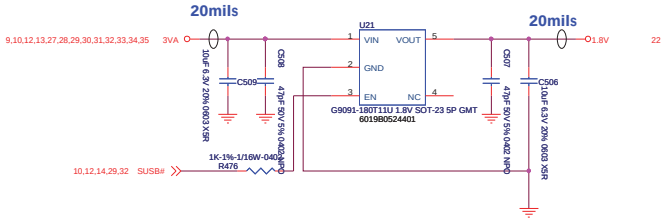

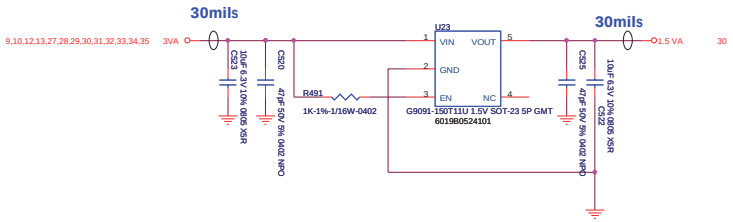

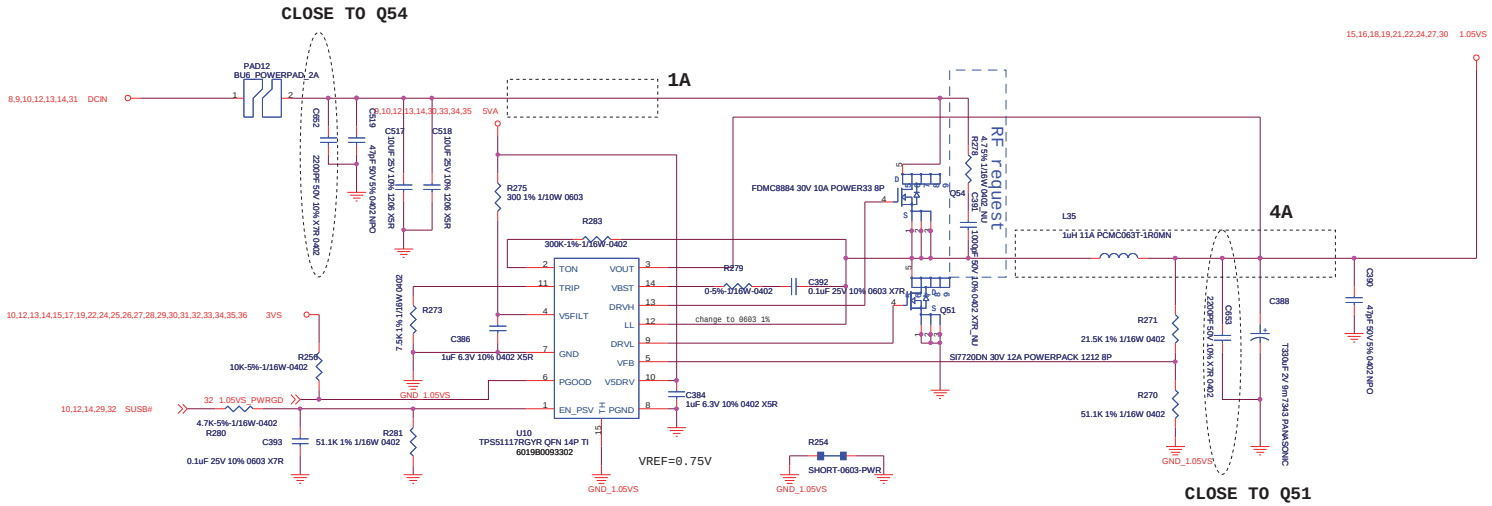

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CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFI
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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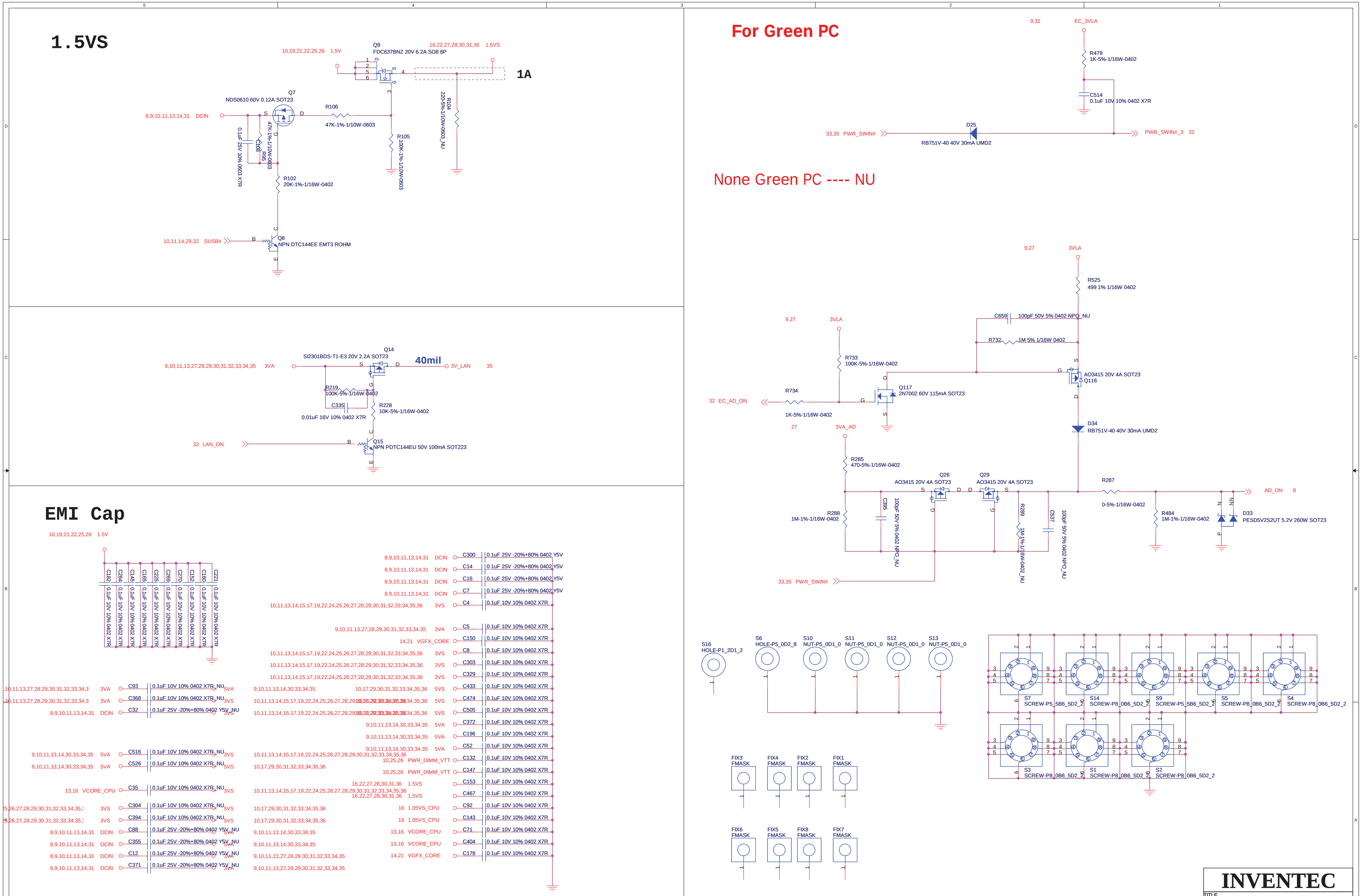

INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
Power on latch

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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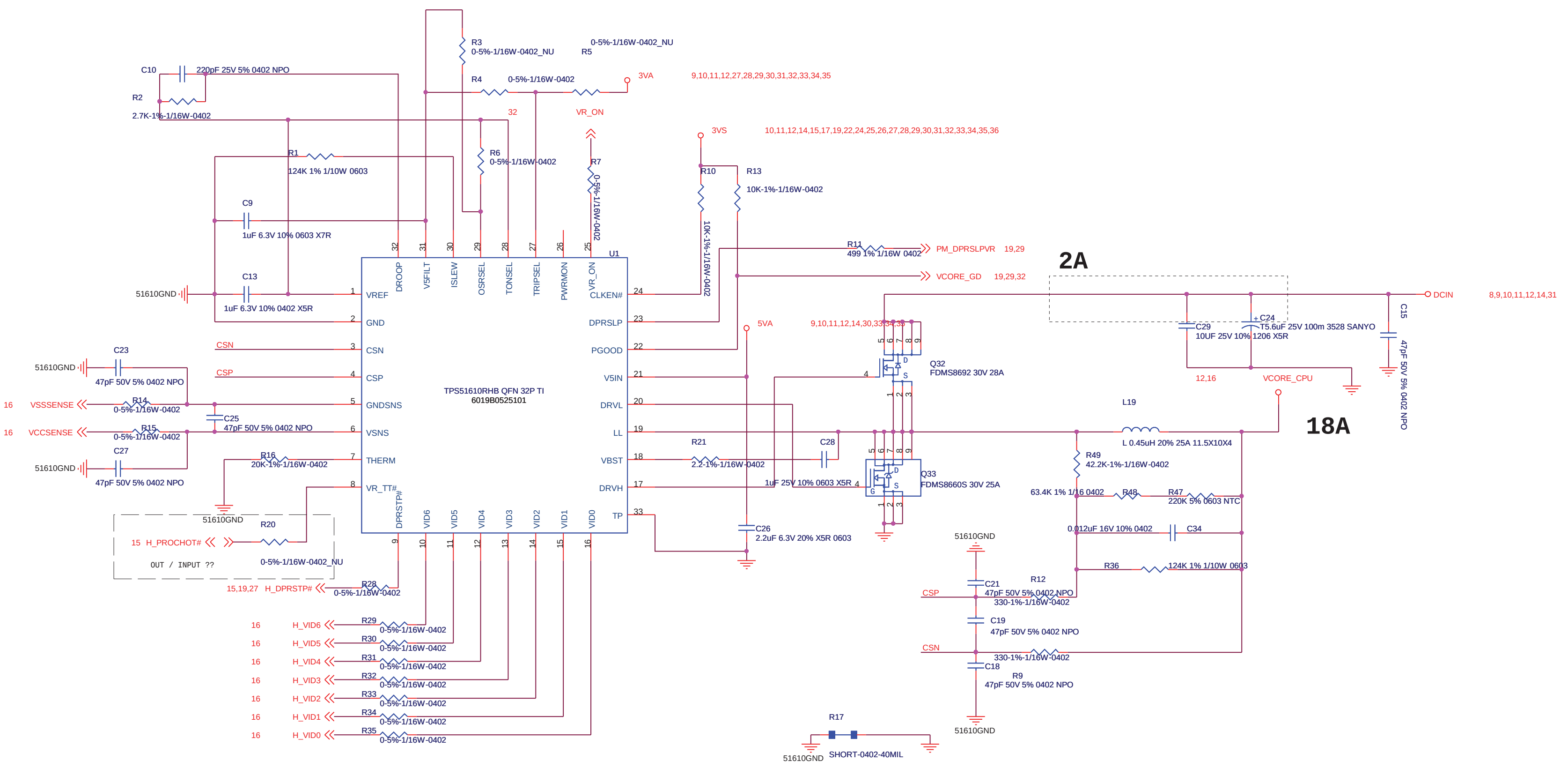

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
CPU Core Power

SIZE	CODE	DOC.NUMBER	REV
C	X01	D-CS-1310A2264501-ALG	X01

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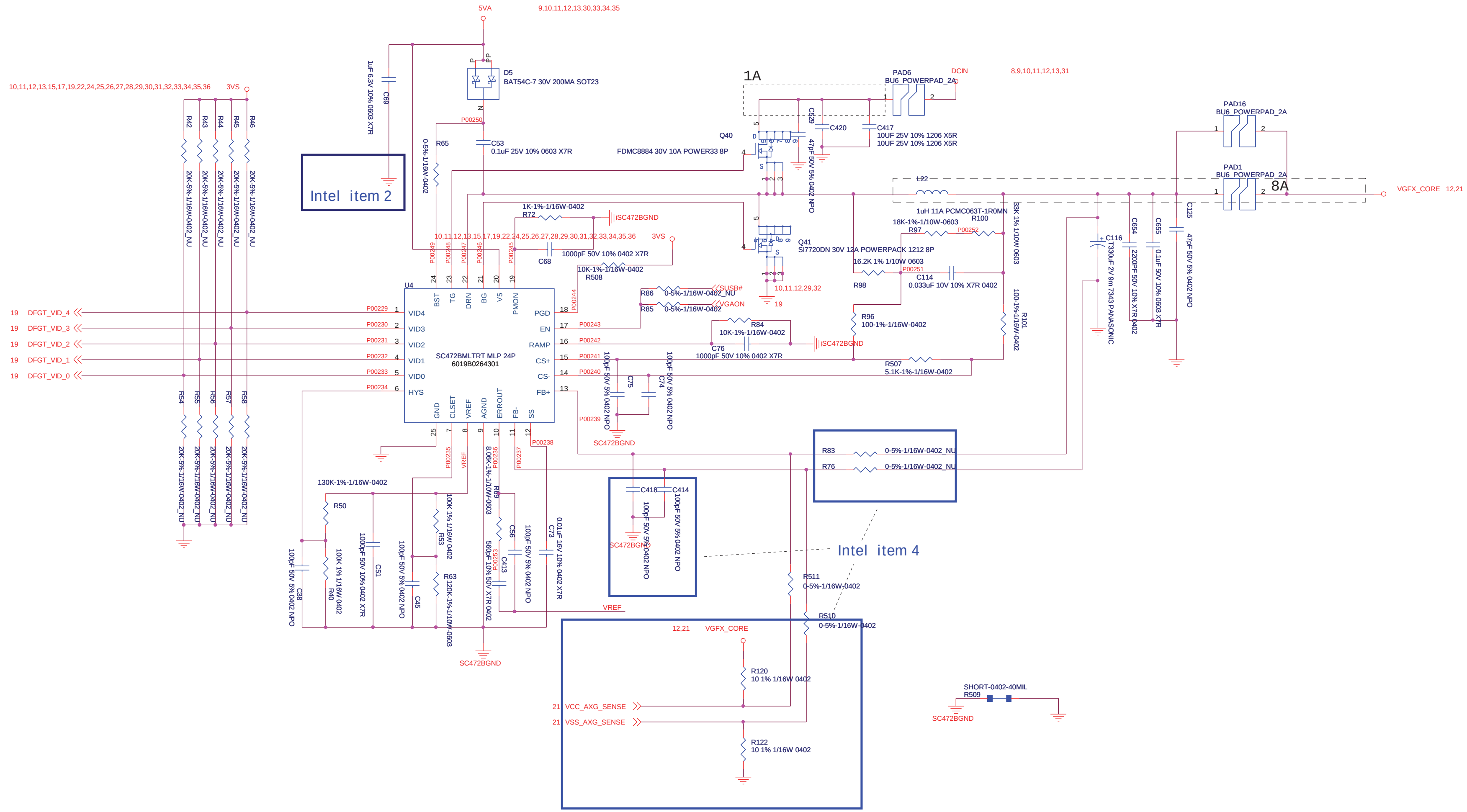

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
GPU CORE

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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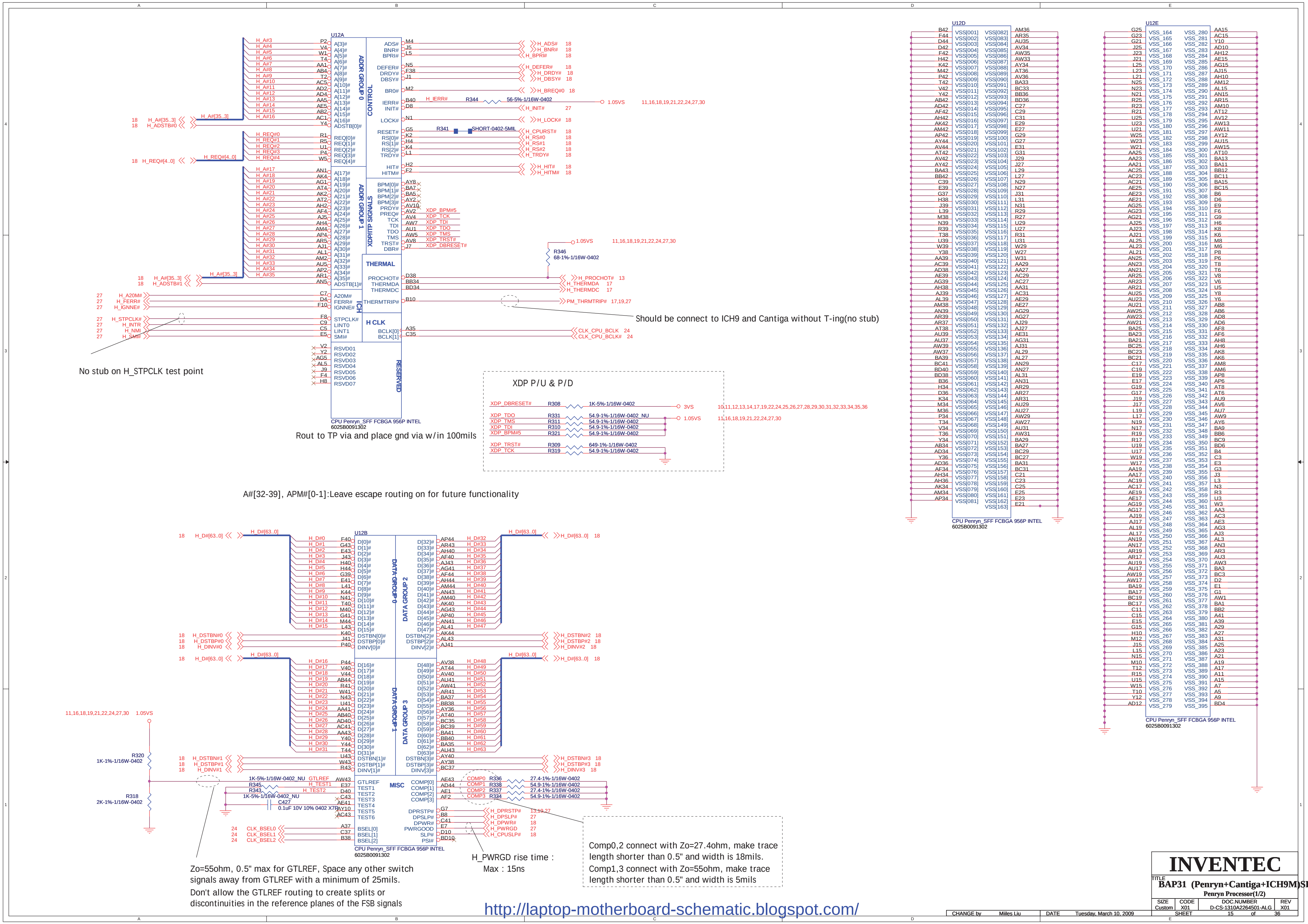

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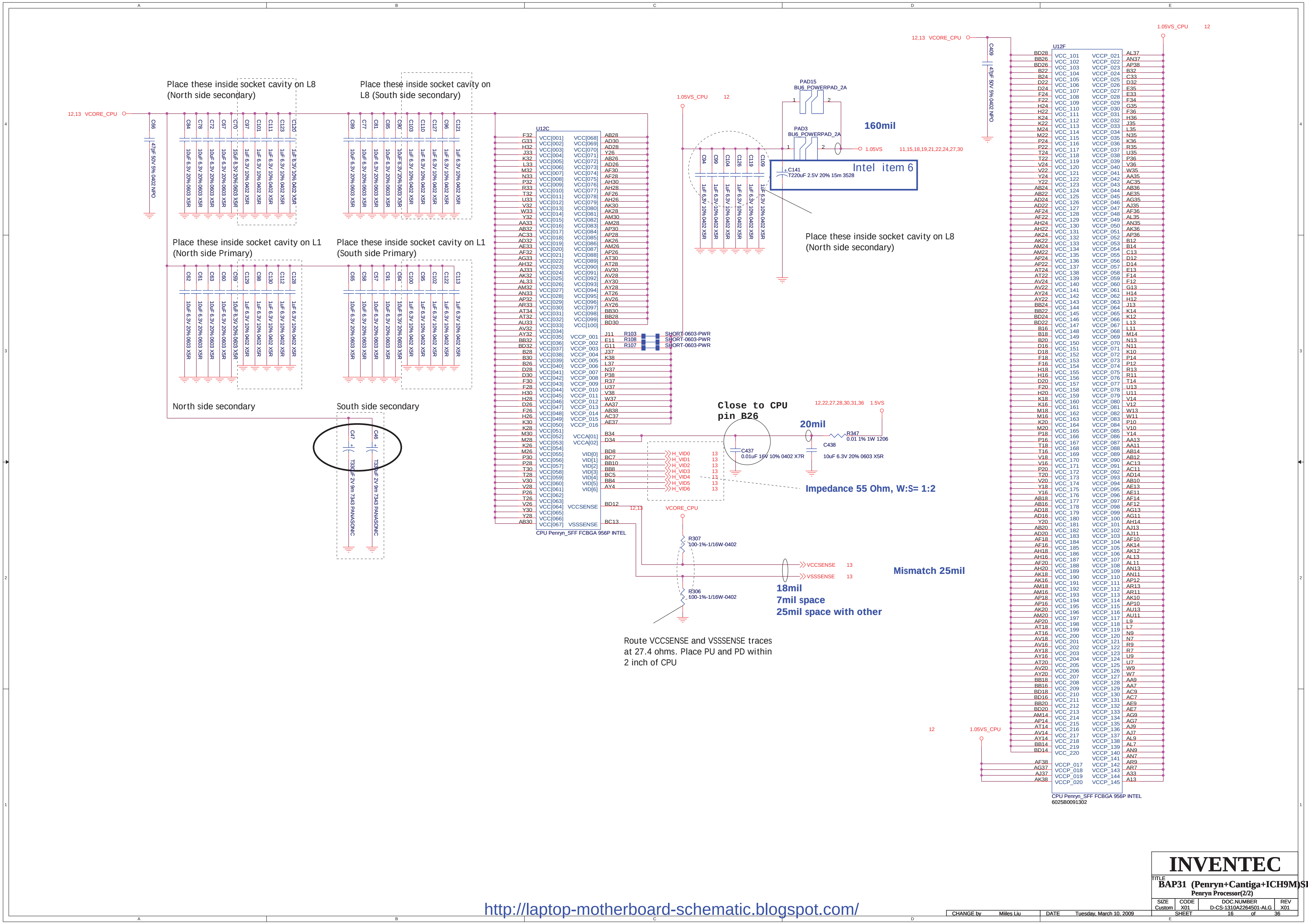

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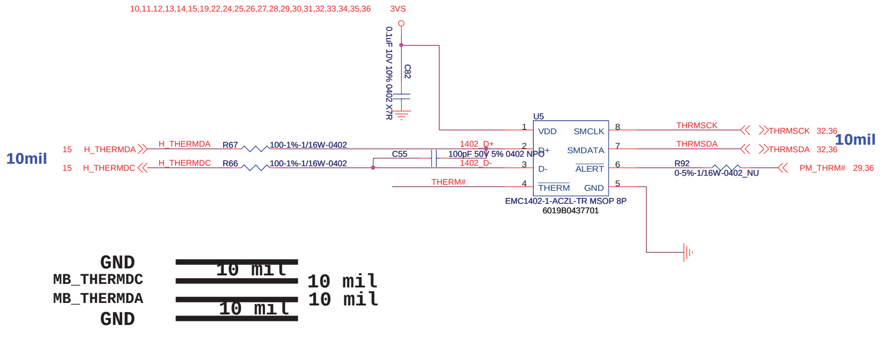
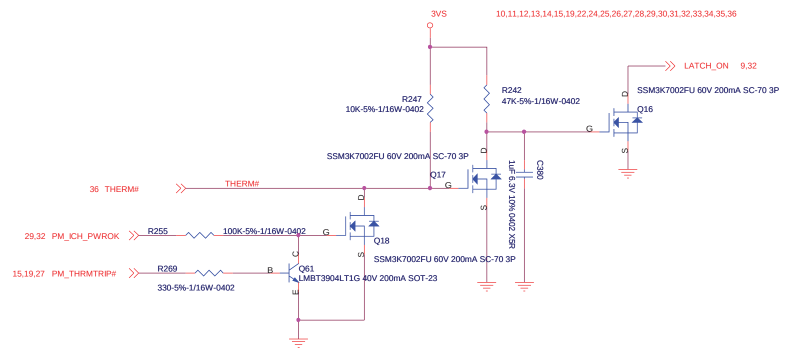
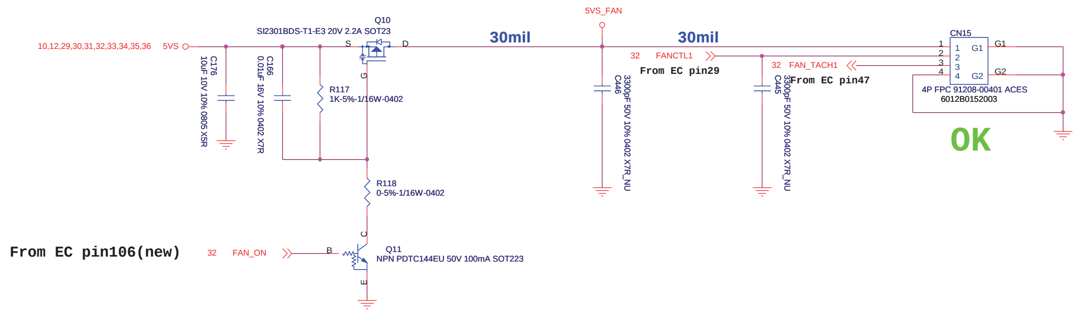
THERMAL SENSOR





Fan control



INVENTEC			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF			
CPU Thermal			
SIZE Custom	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
CHANGE by Miles Liu	DATE Tuesday, March 10, 2009	SHEET 17 of 36	

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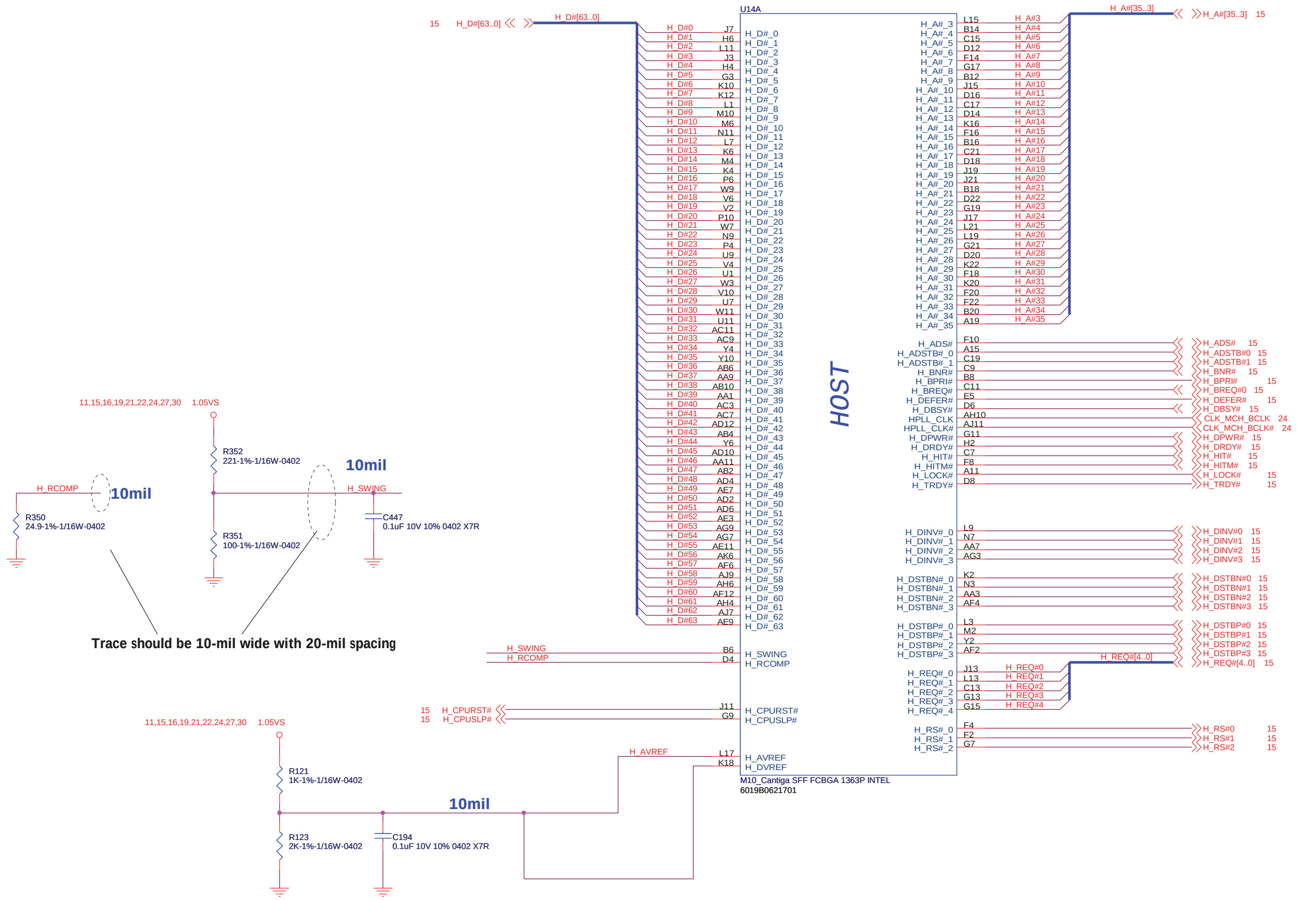
檔案以 製作工廠 試用版建立



INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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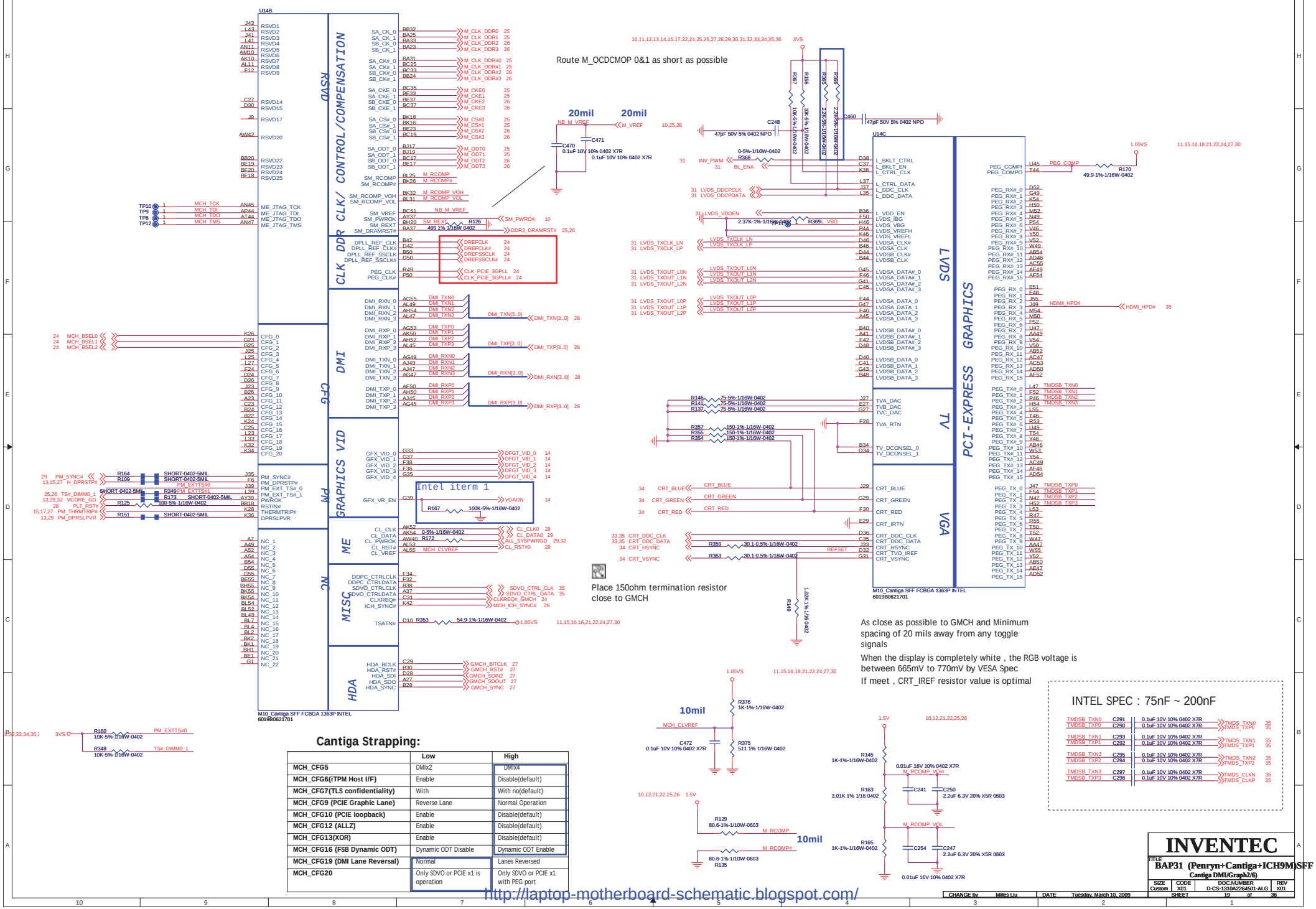
檔案以 製作工廠 試用版建立



Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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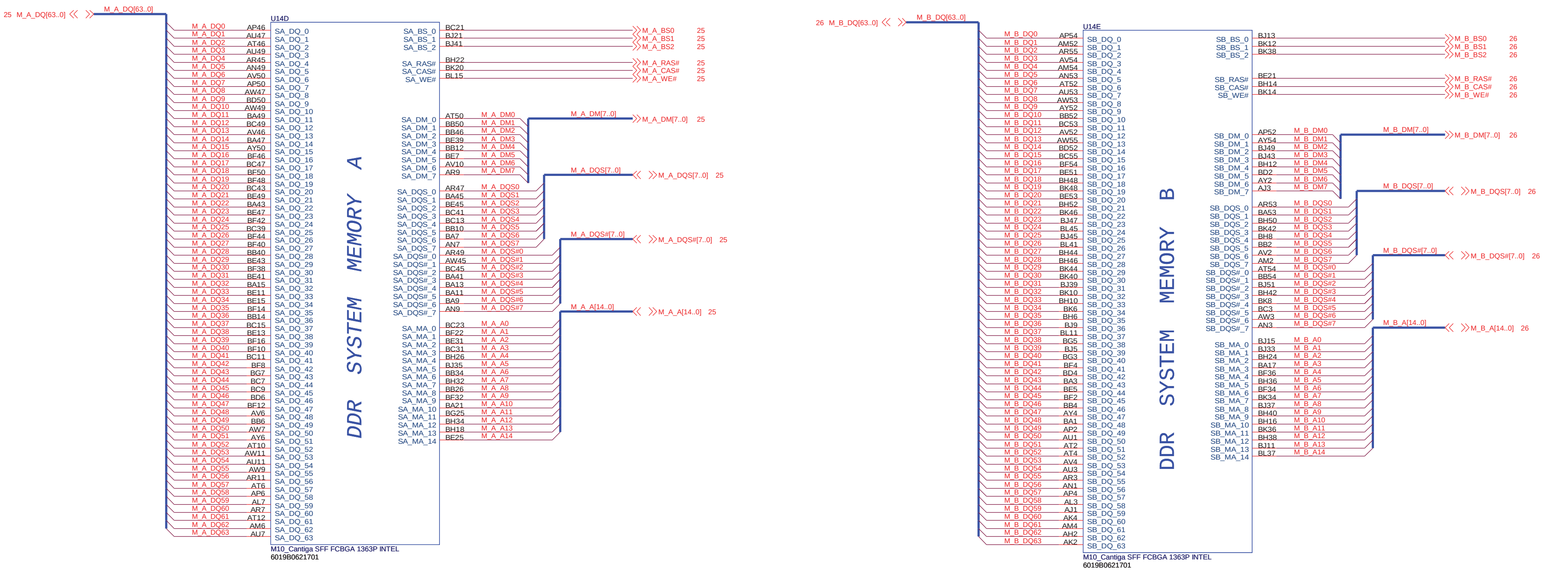
•••檔案以••••製作工廠••試用版建立•••••••••••••••••



INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF

Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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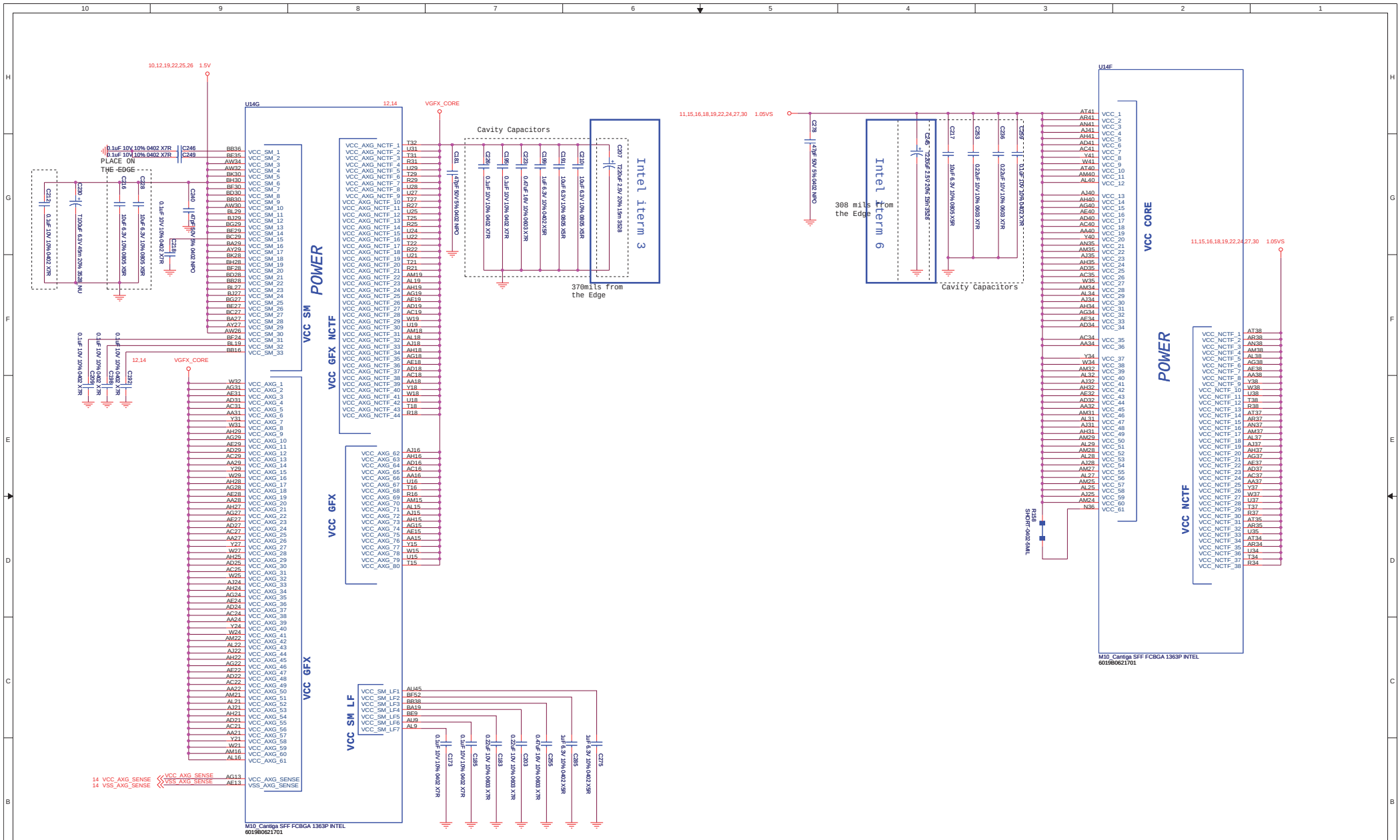

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Power(4/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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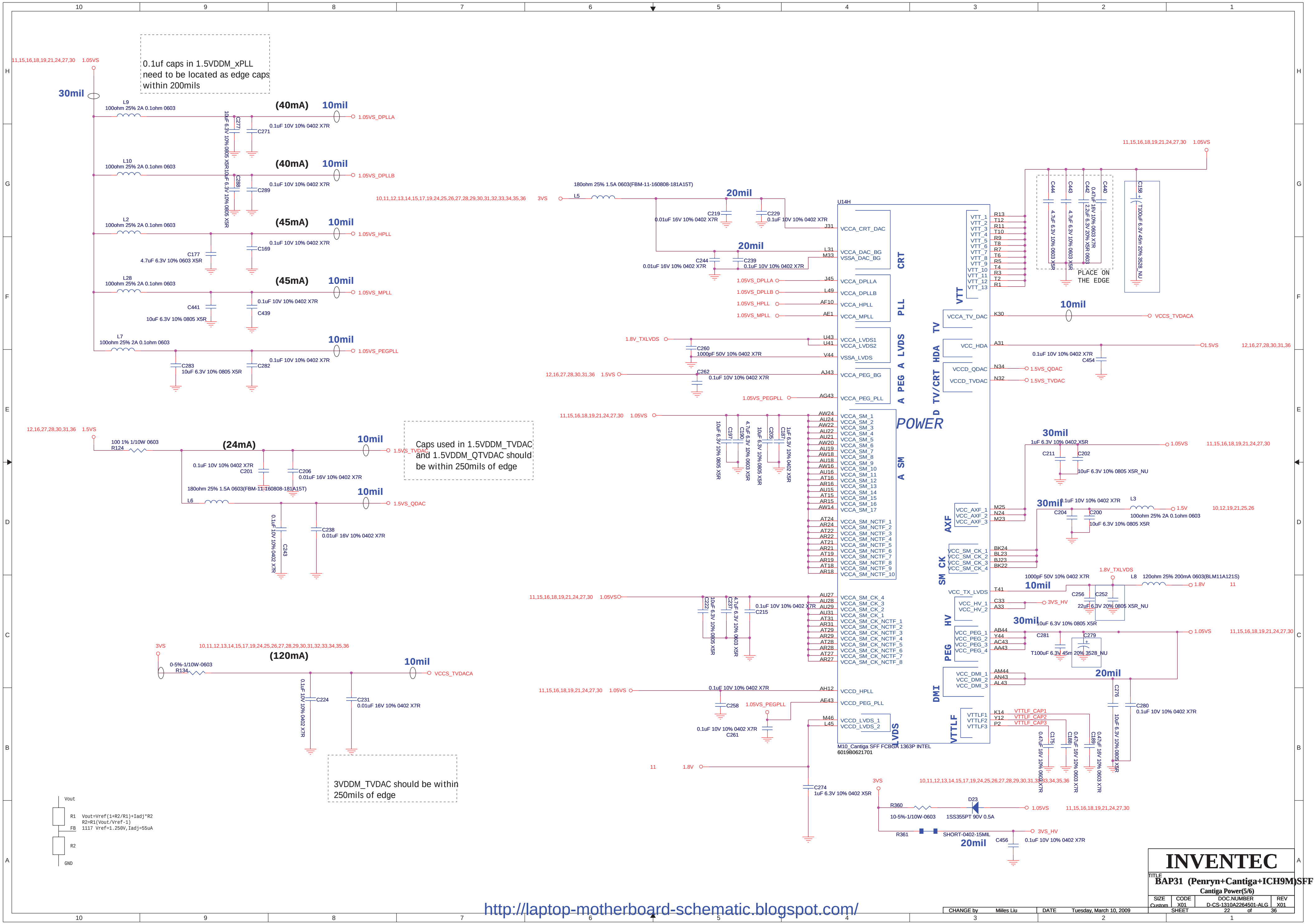

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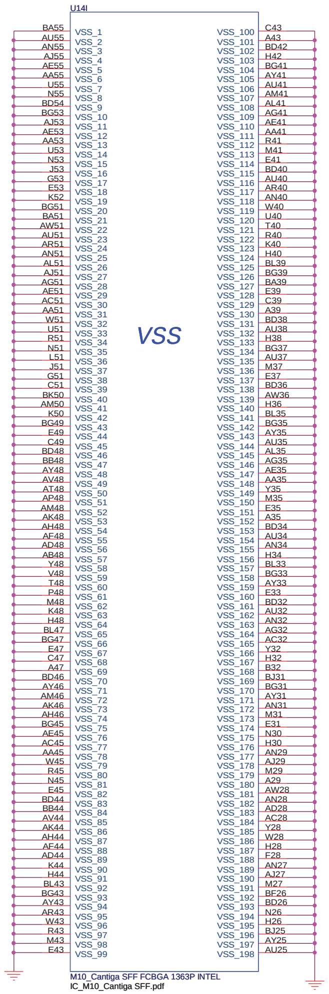
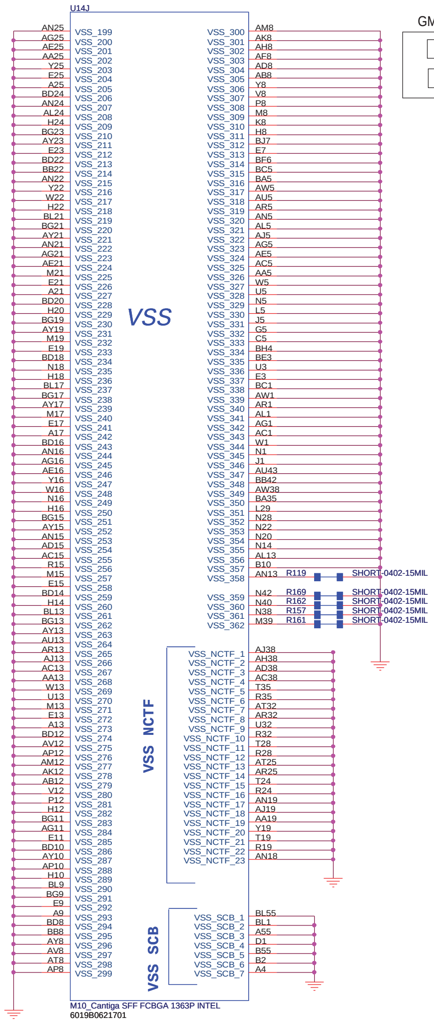
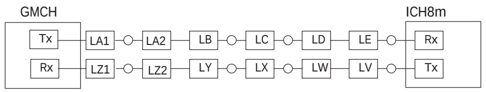




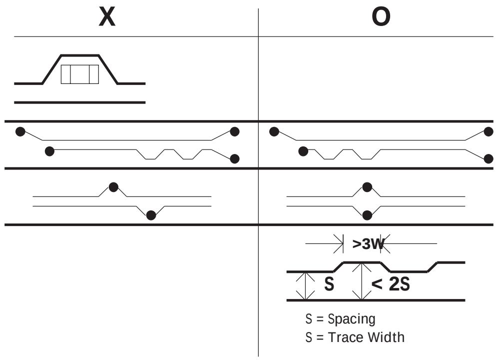
DMI Routing Guideline



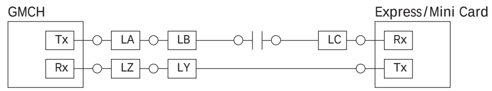
Breakout/in **LA/LZ**	Main Route **LB/LY**		Breakout/in **LE/LV**
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



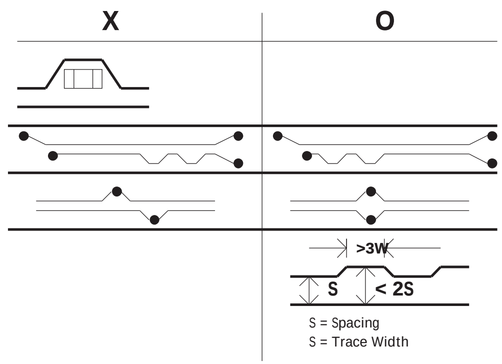
PCIE Routing Guideline



Breakout/in **LA/LZ**	Main Route **LB/LC/LY**	Main Route **LD/LW**	Breakout/in **LE/LV**
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



INVENTEC
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 23 of 36

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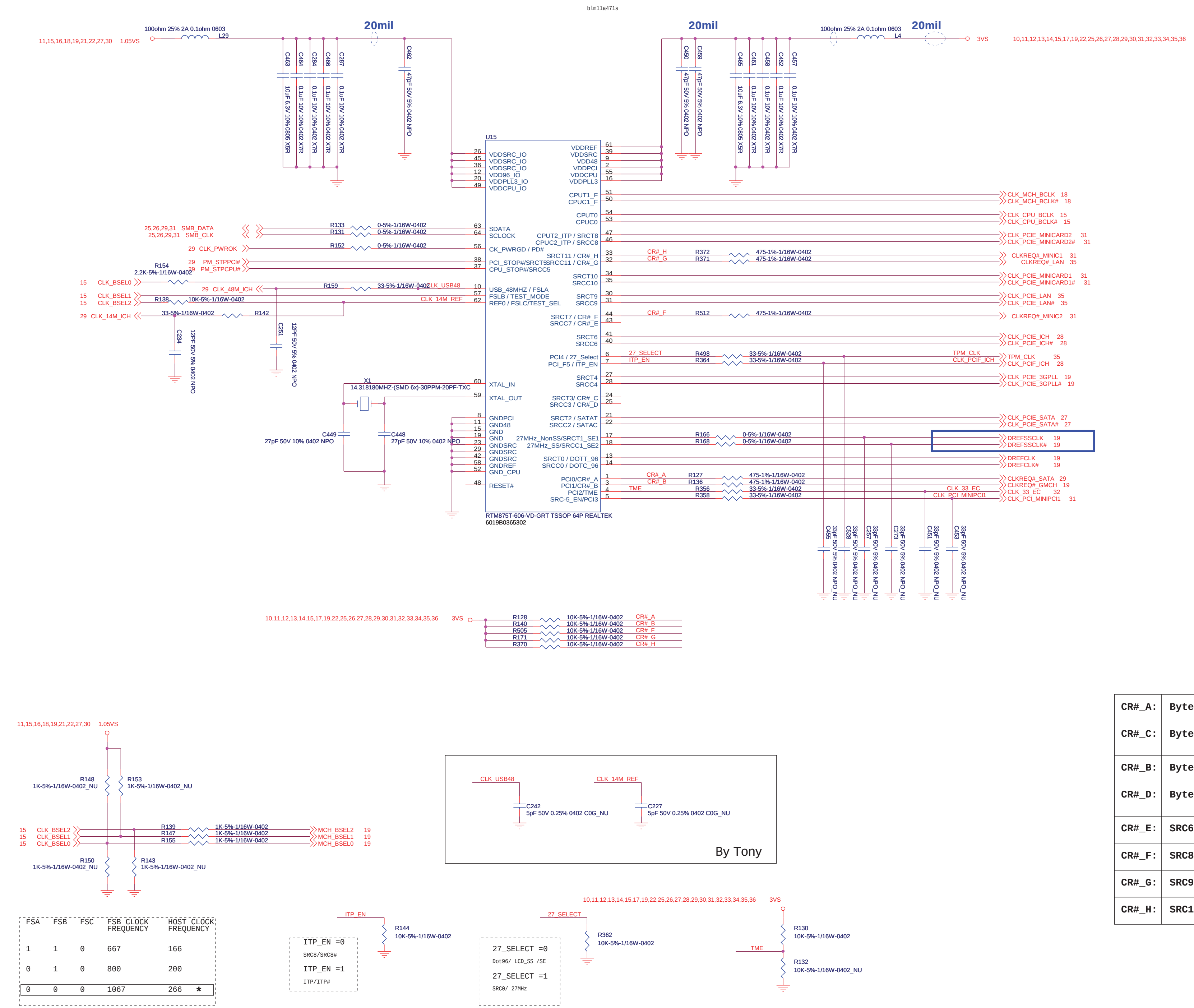

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *

CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF

Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 24 of 36

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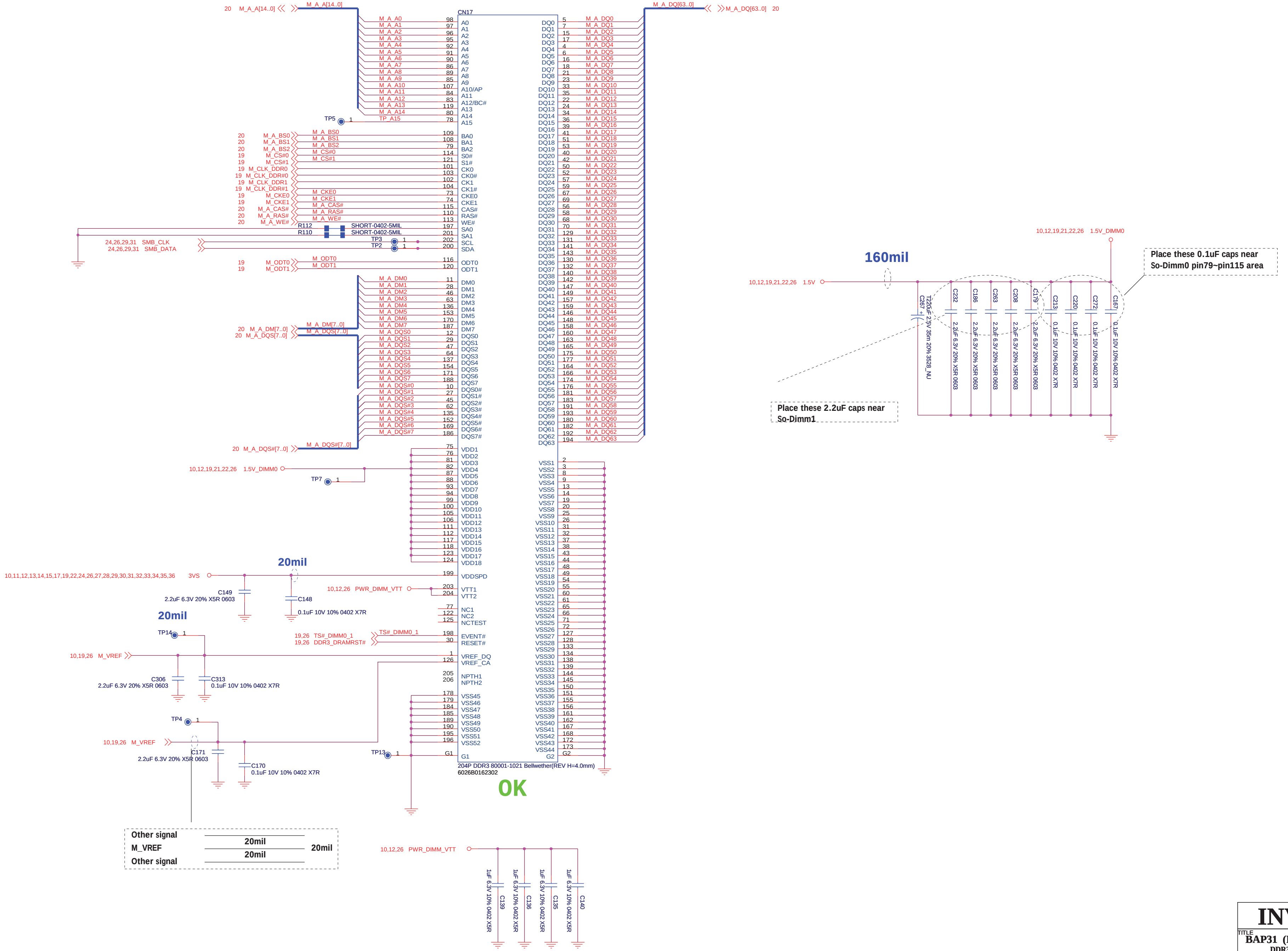
SO-DIMM0



INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF

DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 25 of 36

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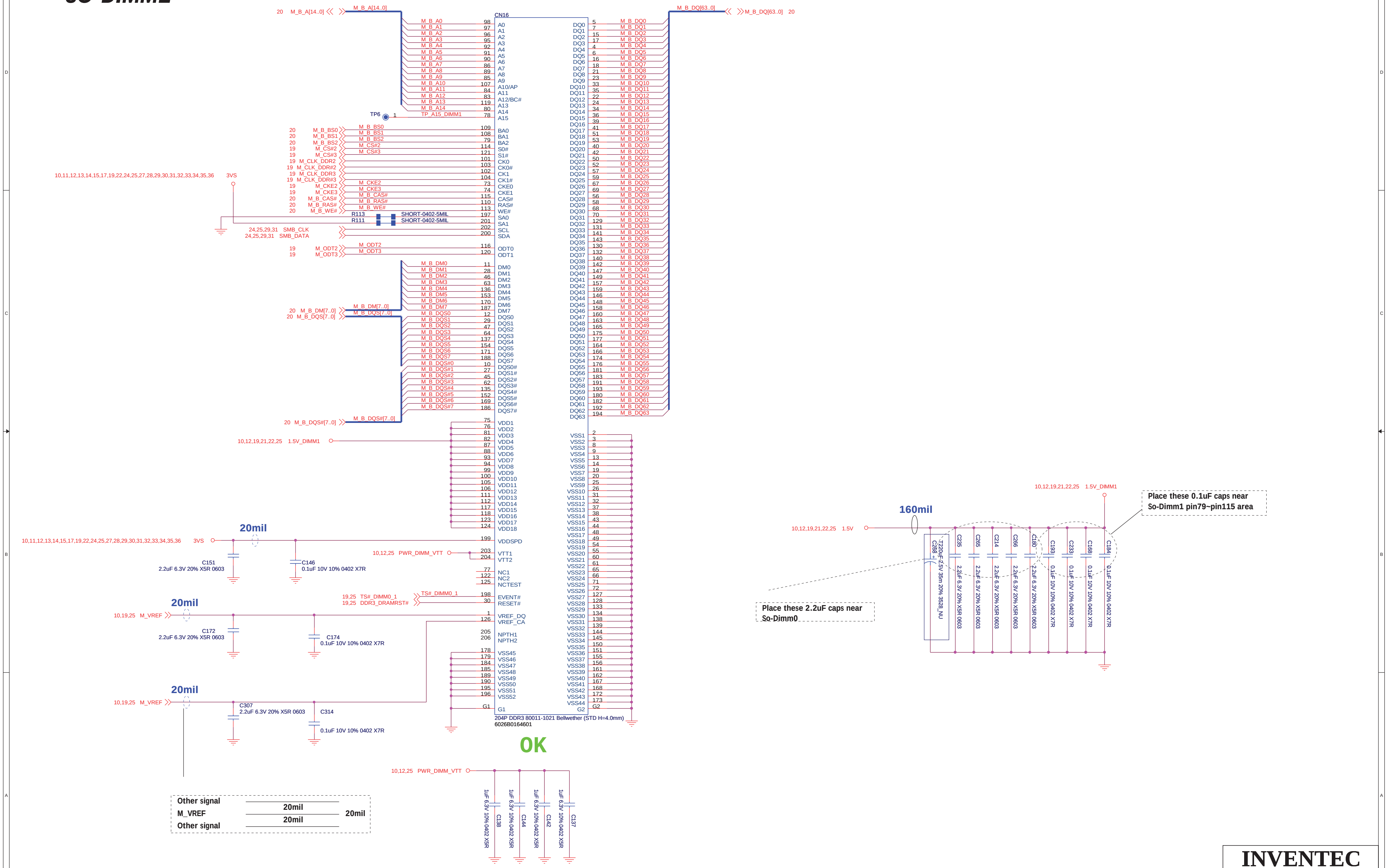
SO-DIMM1



INVENTEC

TITLE	BAP31 (Penryn+Cantiga+ICH9M)SFF		
	DDR3 SDRAM SO-DIMM1		
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
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CHANGE by Miles Liu DATE Tuesday, March 10, 2009

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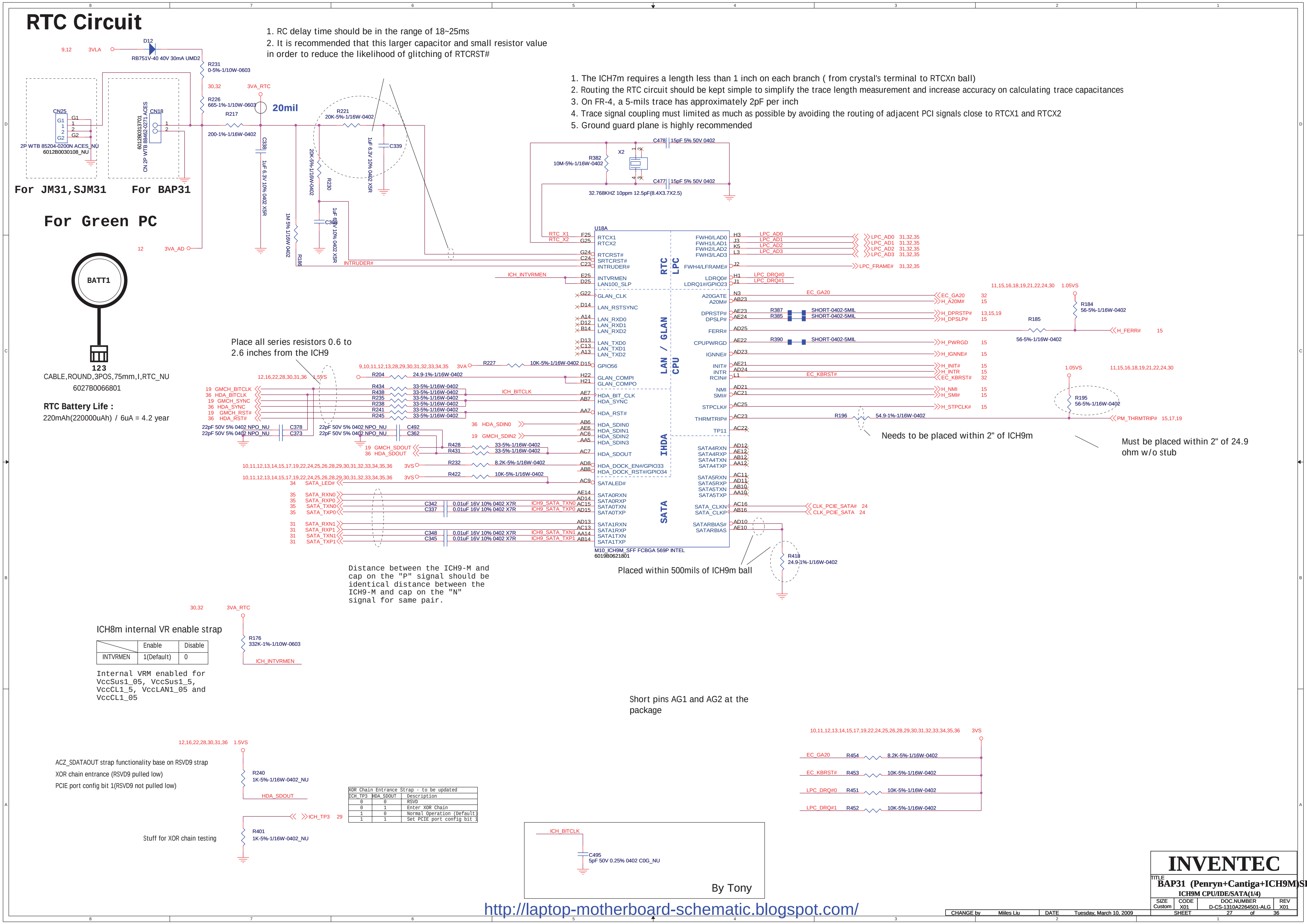
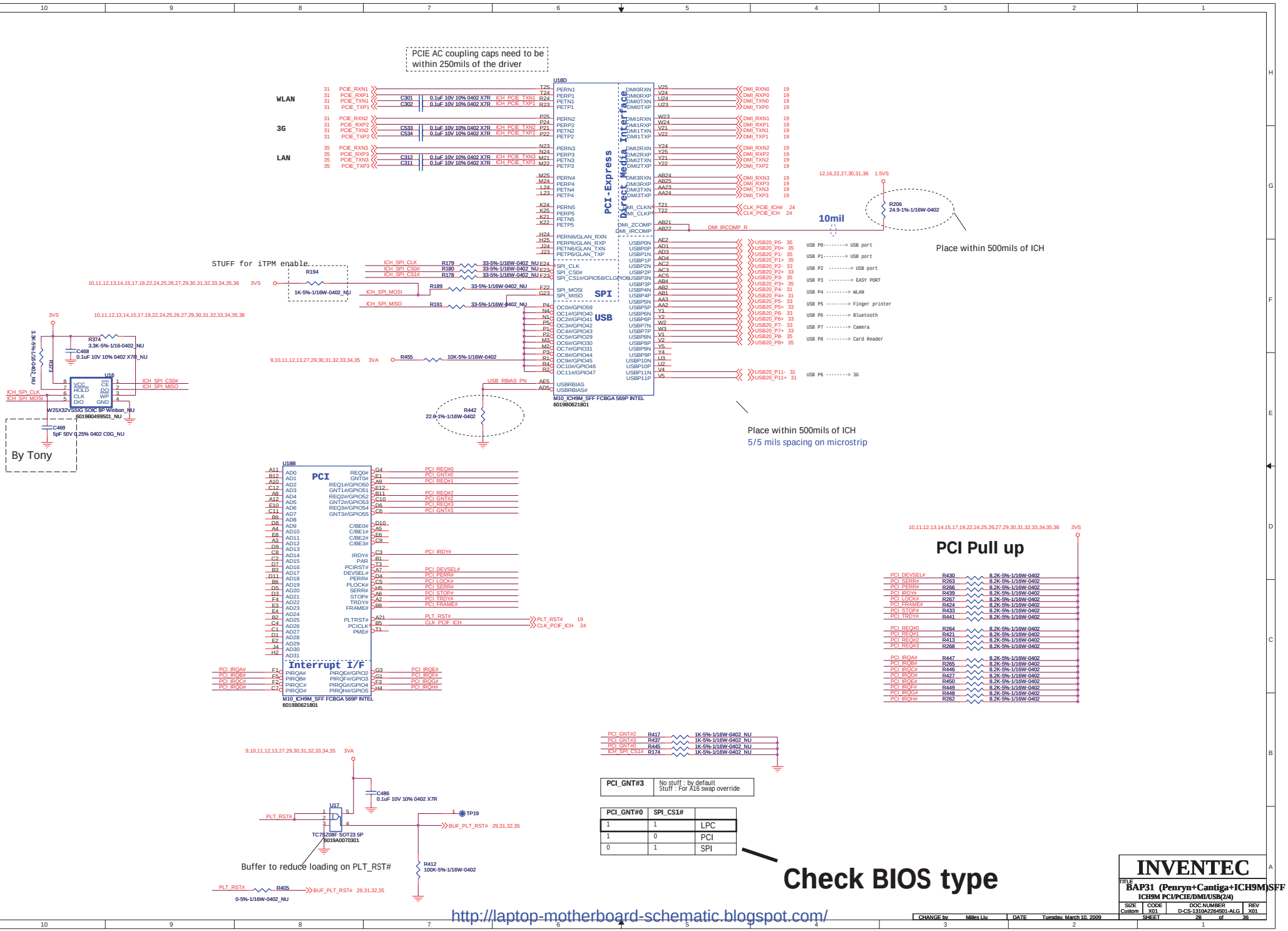
檔案以 製作工廠 試用版建立



http://laptop-motherboard-schematic.blogspot.com/

檔案以 製作工廠 試用版建立



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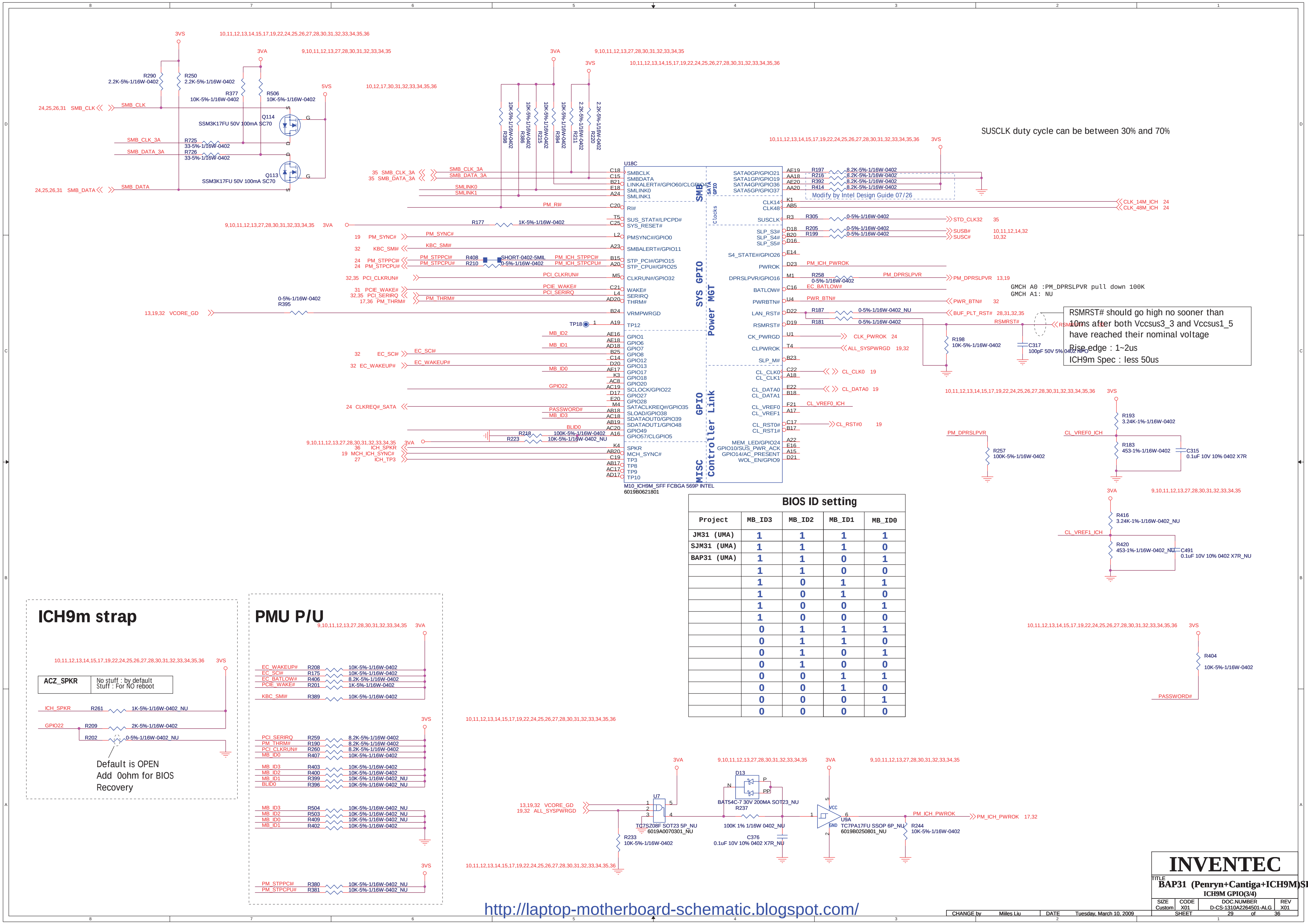

BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0

INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF

ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 29 of 36

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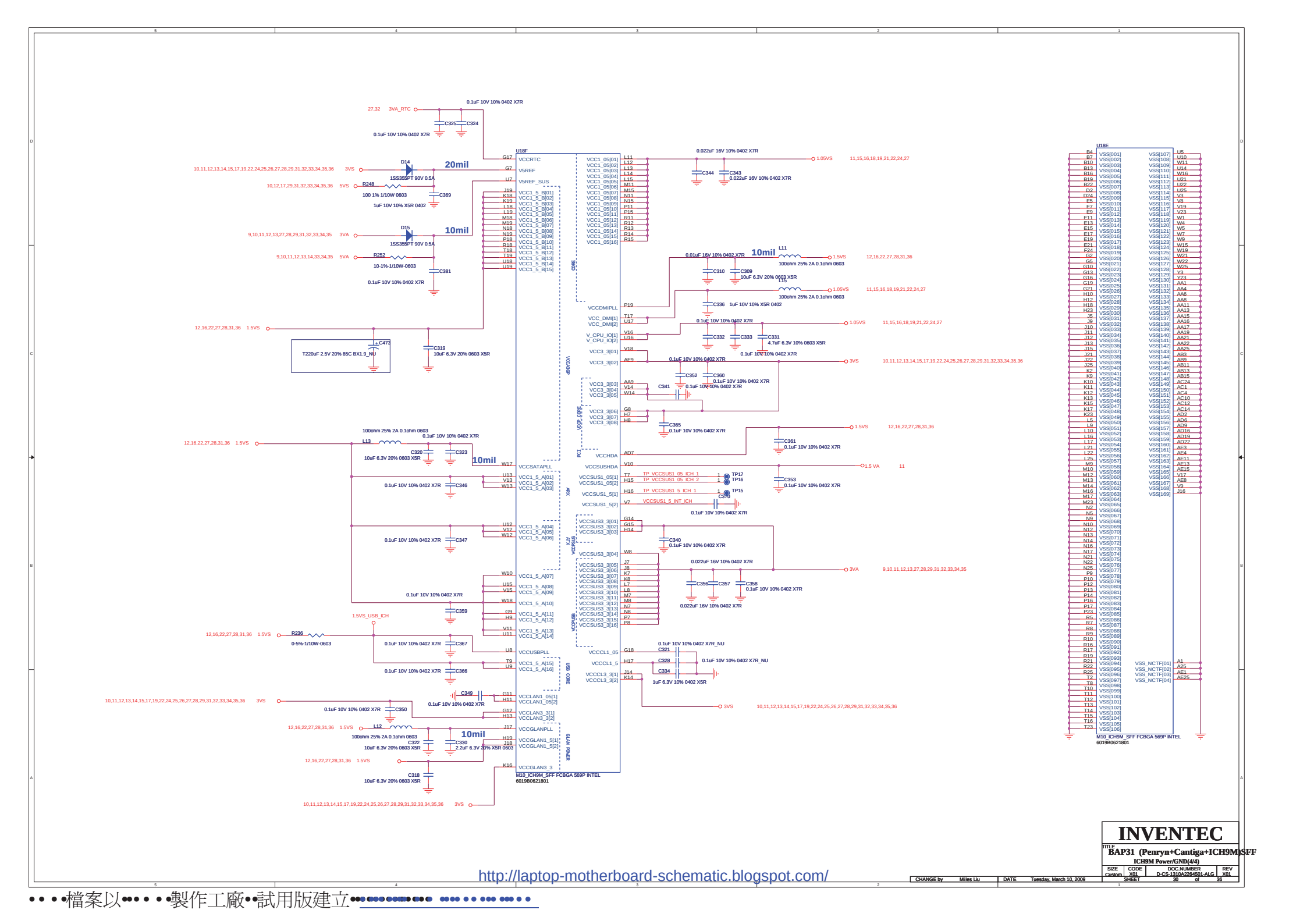
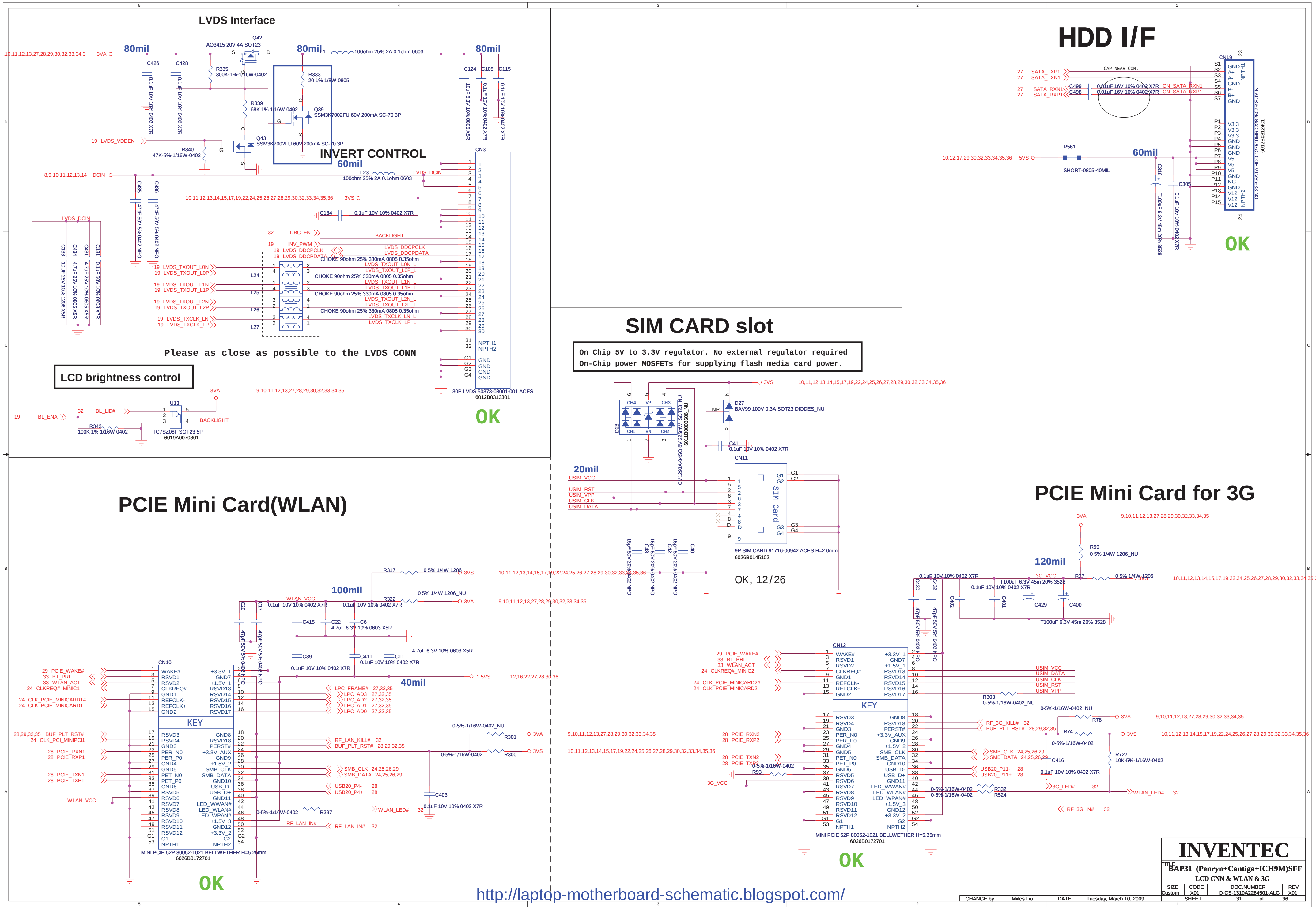

U18F
U18E
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
ICH9M Power/GND(4/4)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
SHEET 30 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
http://laptop-motherboard-schematic.blogspot.com/
檔案以製作工廠試用版建立



http://laptop-motherboard-schematic.blogspot.com/

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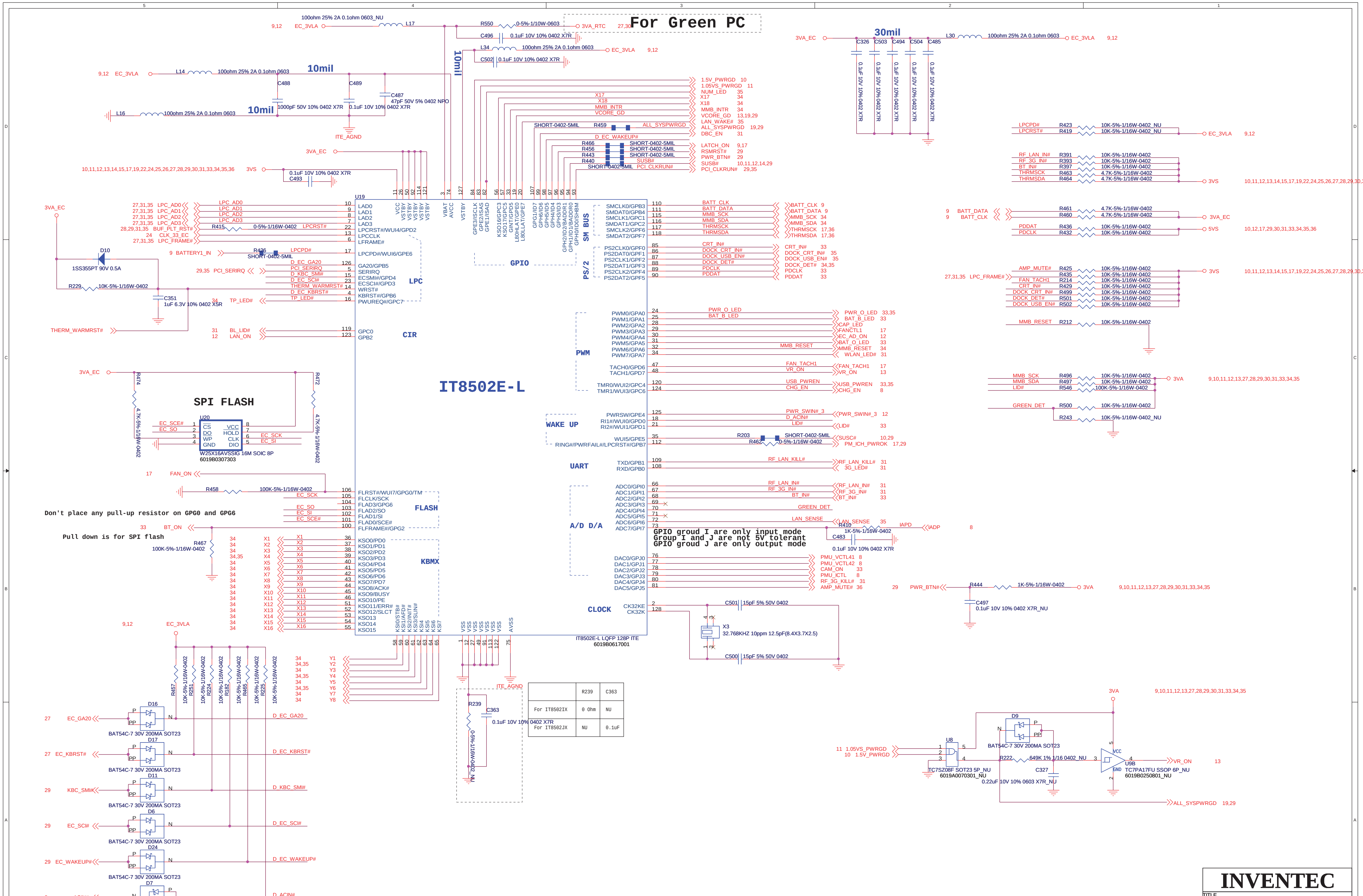


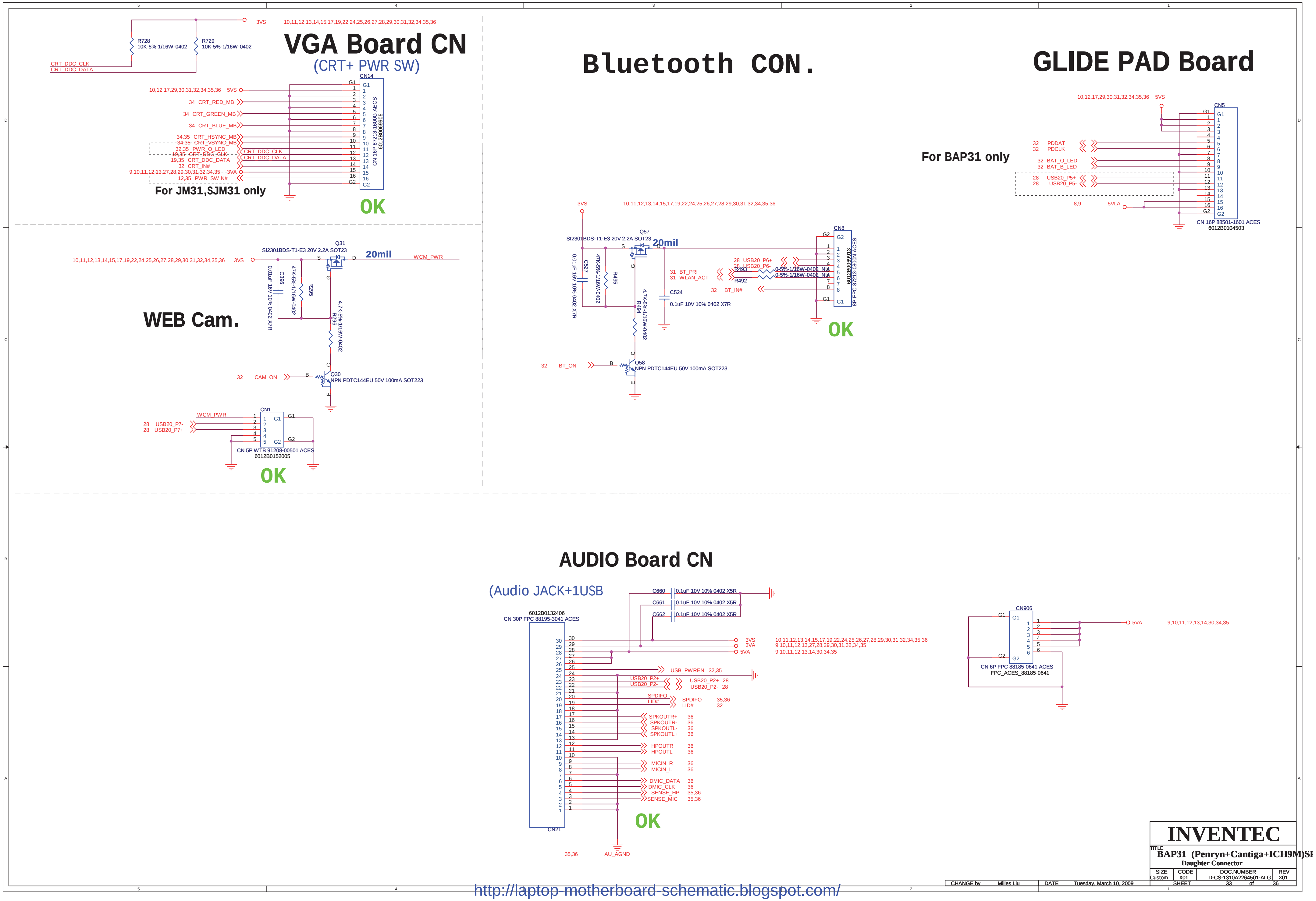
	R239	C363
For IT8502IX	0 Ohm	NU
For IT8502JX	NU	0.1uF

INVENTEC

TITLE	BAP31 (Penryn+Cantiga+ICH9M)SF
	KBC ITE8512F
SIZE	Custom
CODE	X01
DOC.NUMBER	D-CS-1310A2264501-ALG
REV	X01
CHANGE by	Milles Liu
DATE	Tuesday, March 10, 2009
SHEET	32 of 36

http://laptop-motherboard-schematic.blogspot.com/

檔案以 製作工廠 試用版建立



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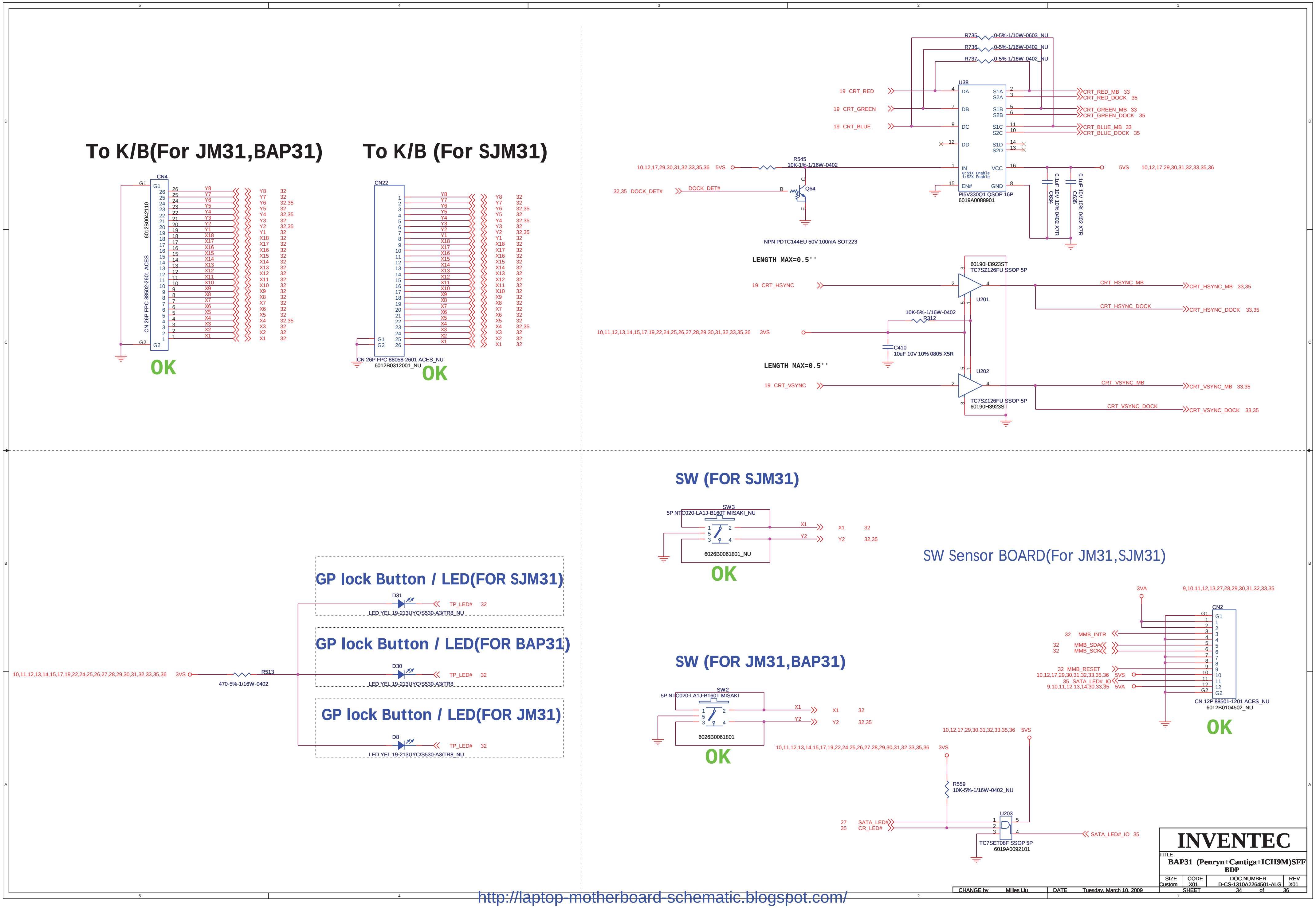

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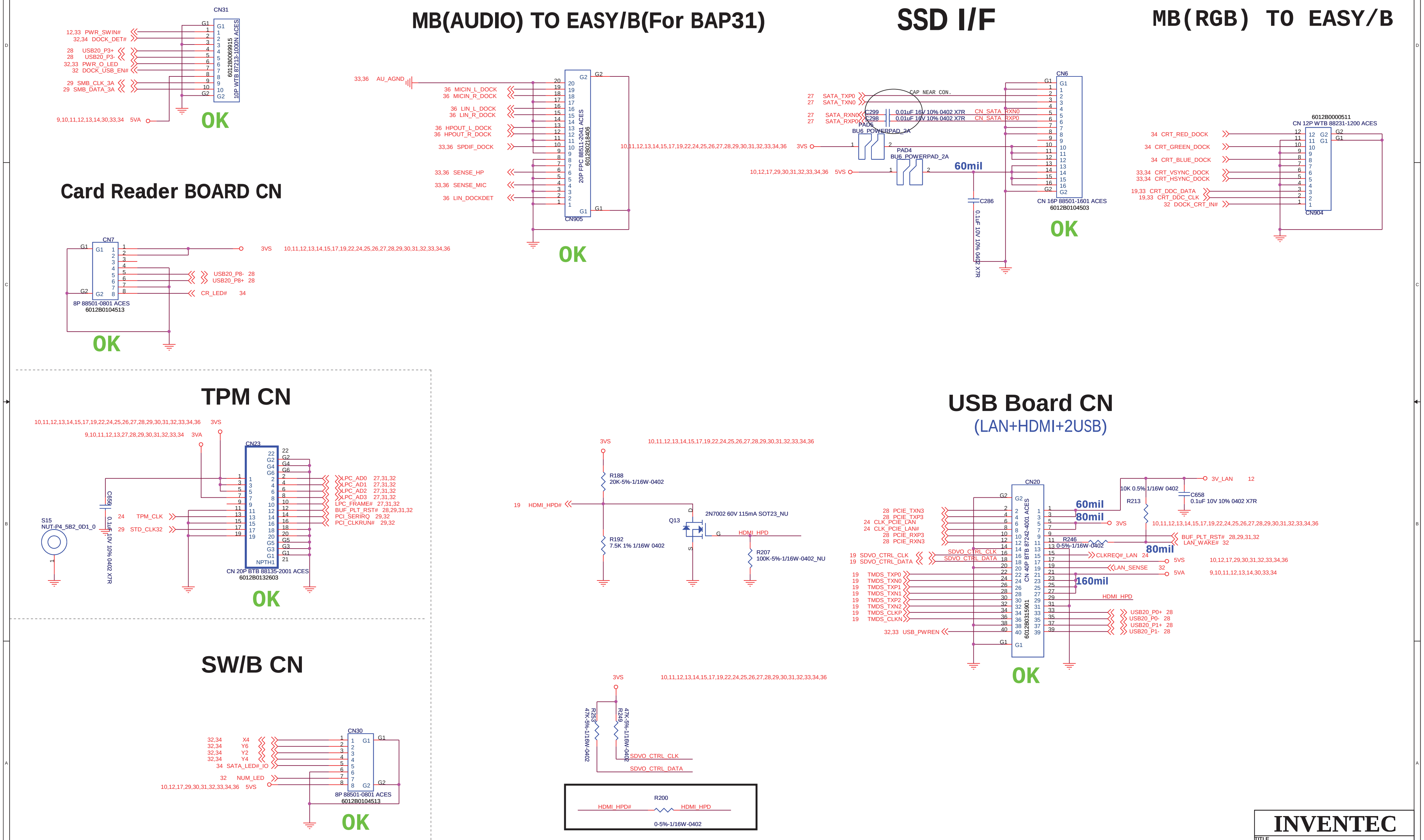
For BAP31(EASY/B)



INVENTEC

TITLE	BAP31 (Penryn+Cantiga+ICH9M)SFF BDP		
SIZE Custom	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
CHANGE by Miiles Liu	DATE Tuesday, March 10, 2009	SHEET 35 of 36	

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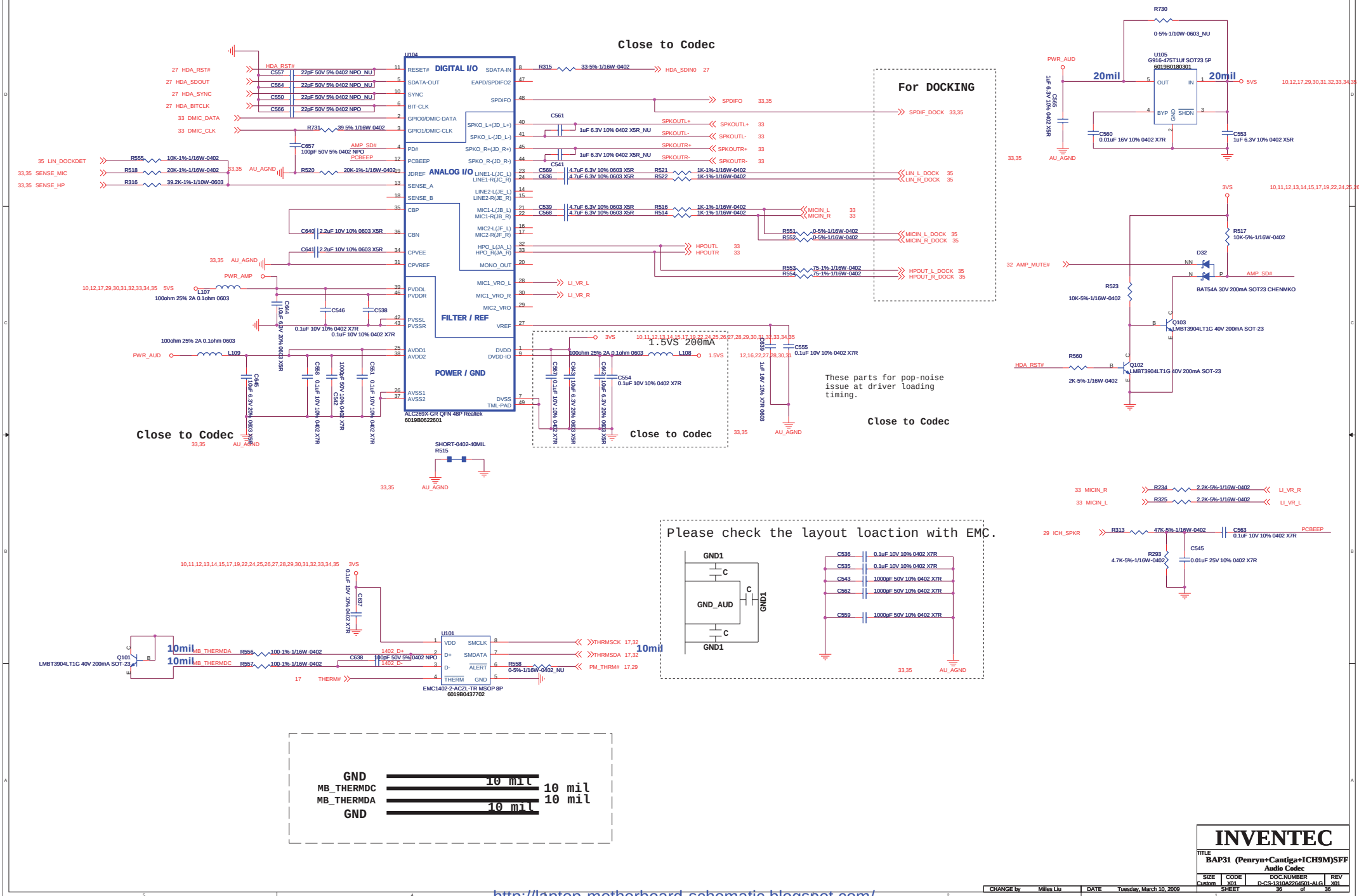

CHANGE by	Milles Liu
DATE	Tuesday, March 10, 2009

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Audio Codec

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
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