

Compal Confidential

KAV10 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

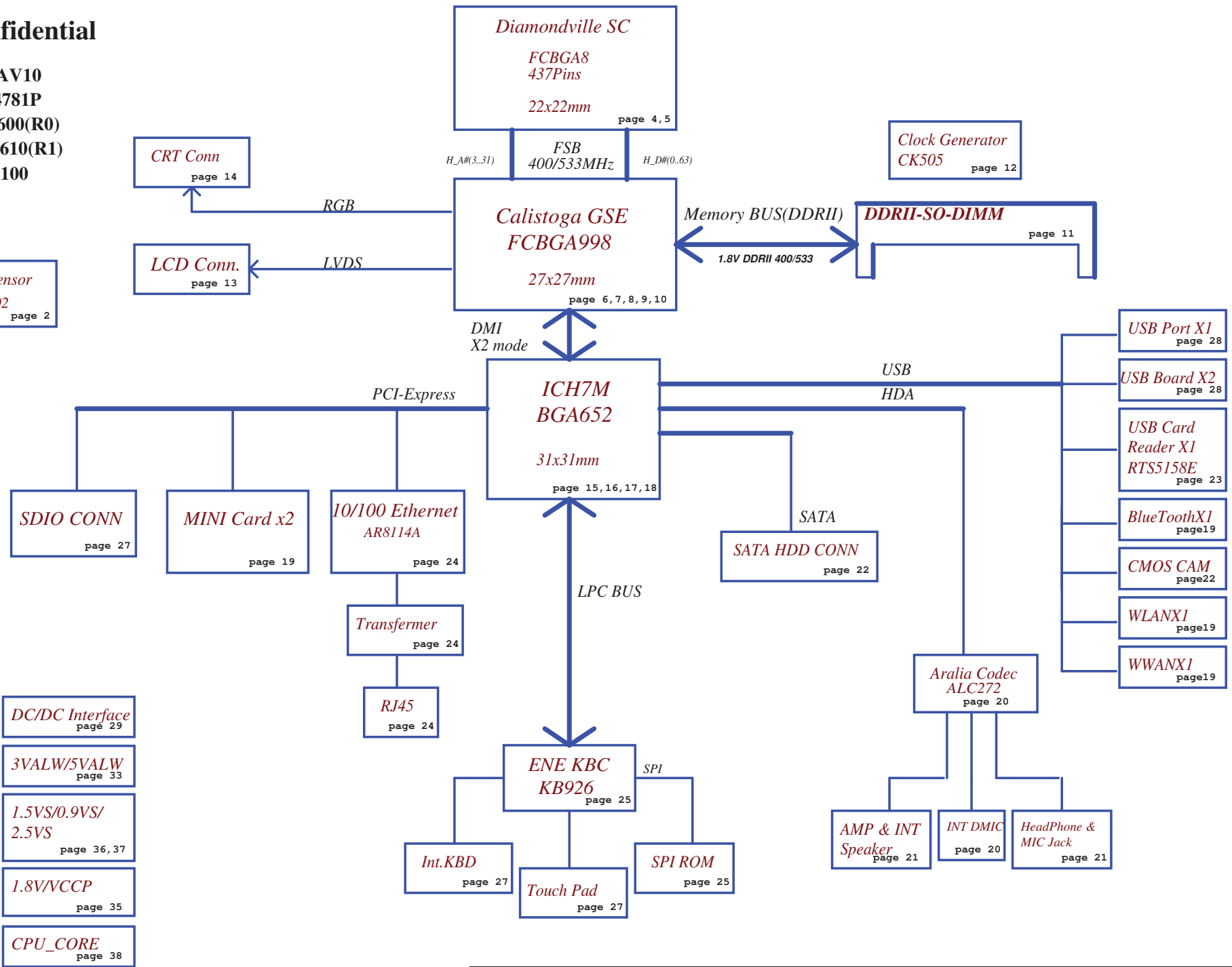
2008-12-30

REV: 1.0

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Model Name : KAV10
 File Name : LA-4781P
 P/N : DA60000A600(R0)
 DA60000A610(R1)
 DAZ06F00100



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SIGNAL						
		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

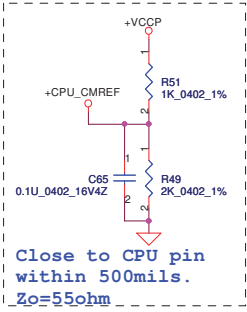
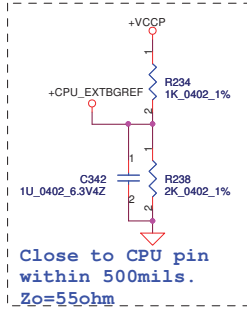
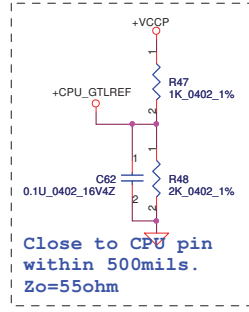
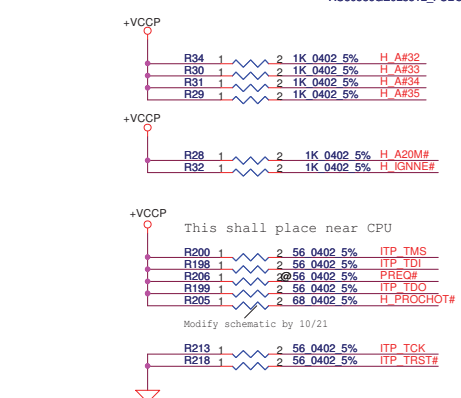
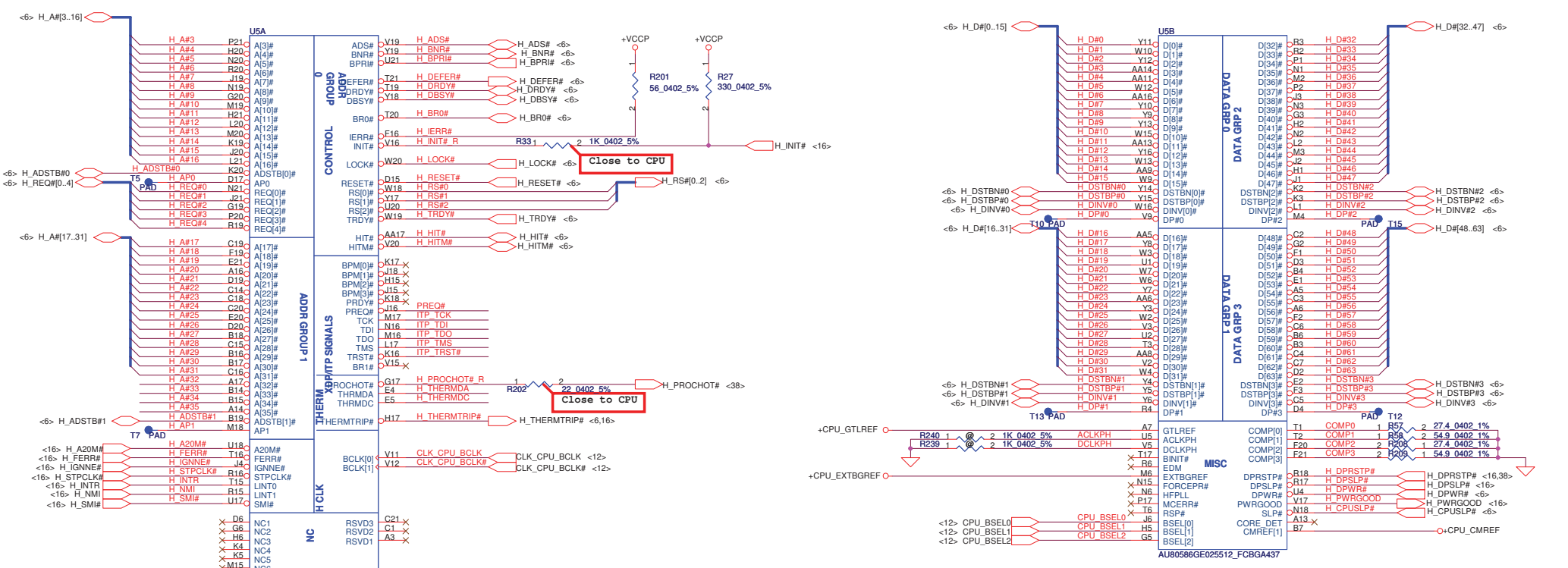
EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b
EEPROM(24C16/02)	1010 000X b		

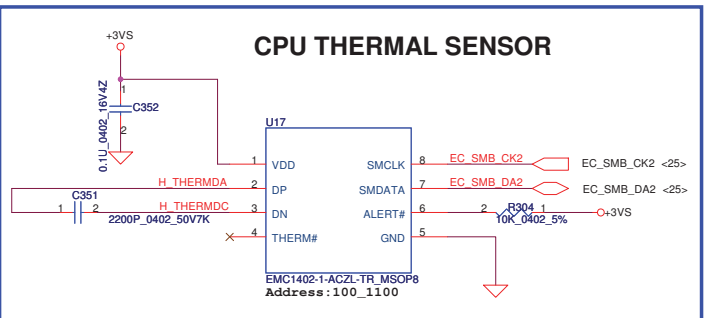
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb



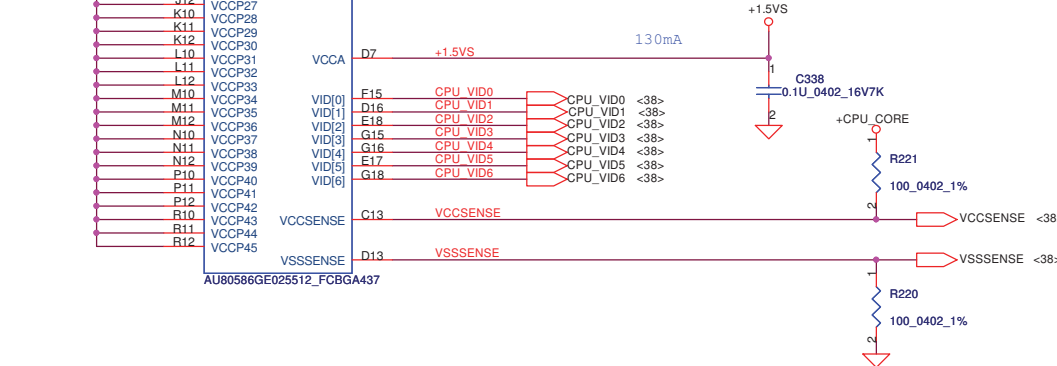
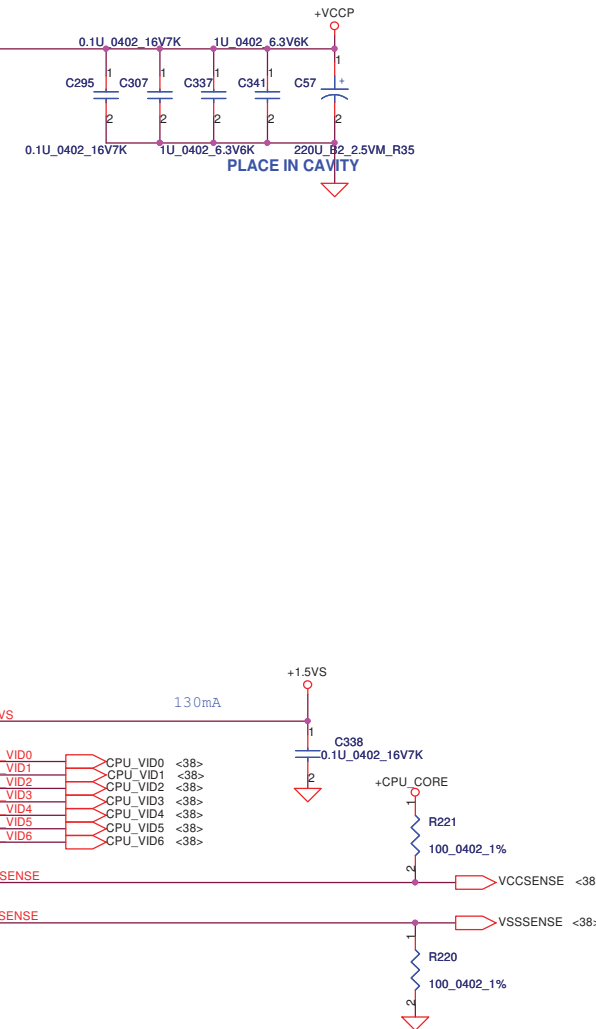
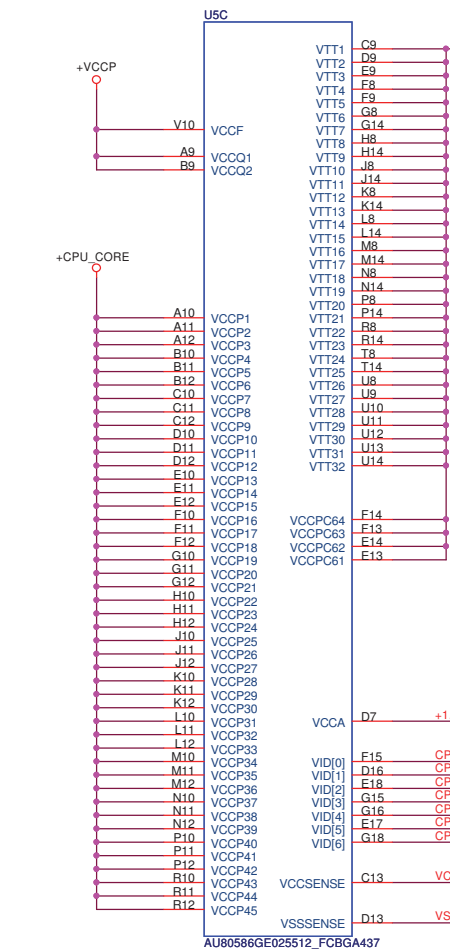
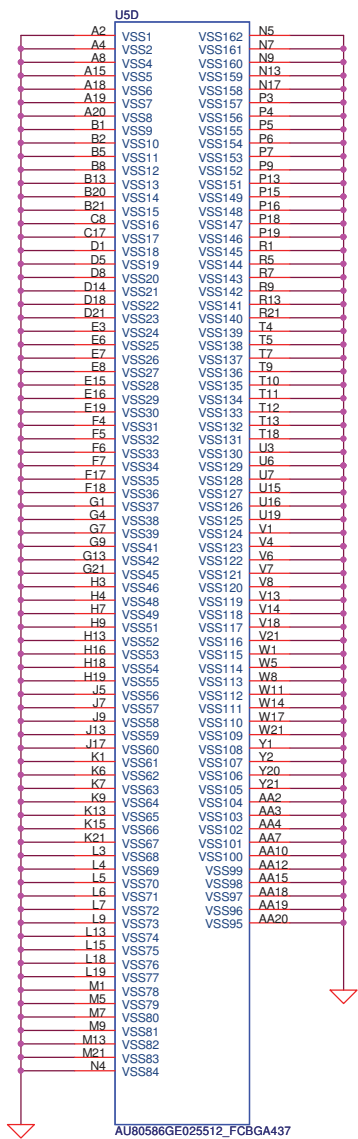
Layout note:
 COMP0,2 connect with $Z_0=27.4\text{ohm} \pm 15\%$, make trace length shorter than 0.5"
 COMP1,3 connect with $Z_0=55\text{ohm} \pm 15\%$, make trace length shorter than 0.5"

H_THERMDA, H_THERMDC routing together.
 Trace width / Spacing = 10 / 10 mil

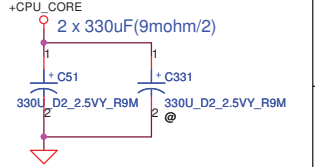
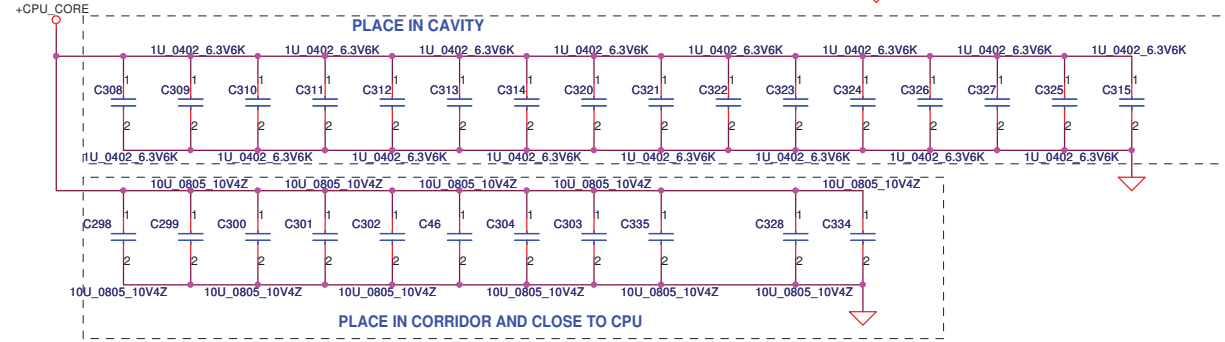


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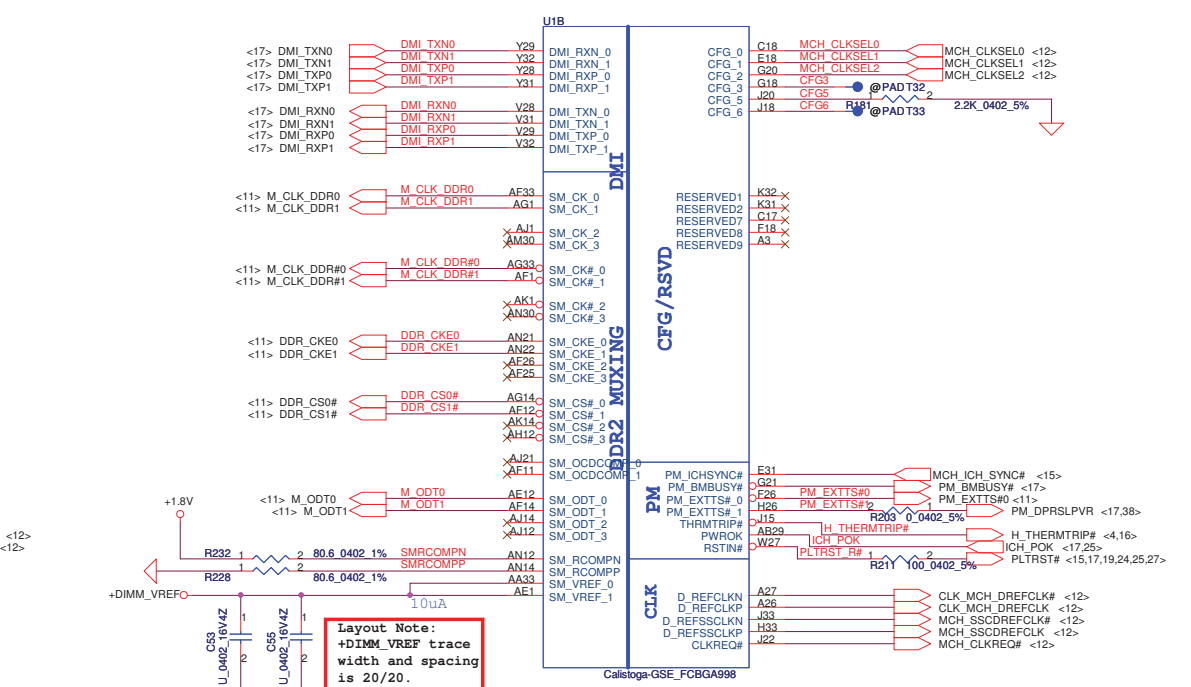
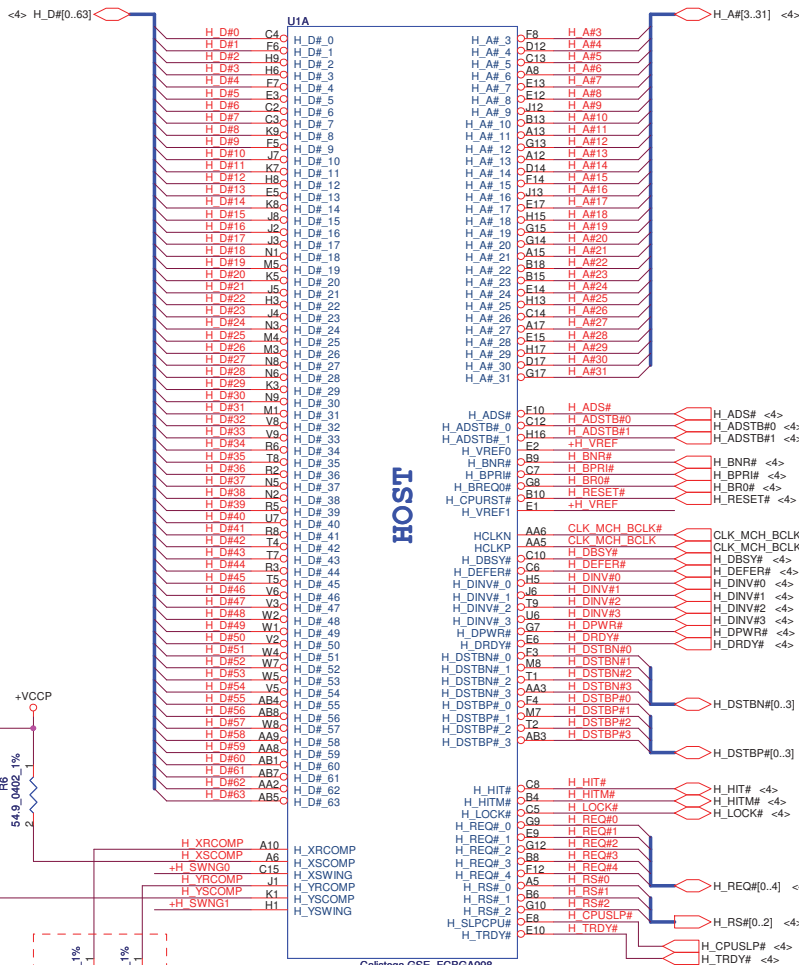


Length match within 25 mils
The trace space 7 mils,
 $Z_0=27.4\text{ohm}$



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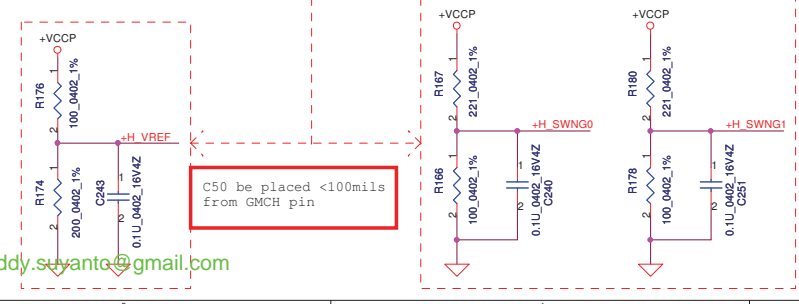


Layout Note:
+DIMM_VREF trace width and spacing is 20/20.

Strap Pin Table

CFG5	Low = DMI x 2 *
	High = DMI x 4

Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

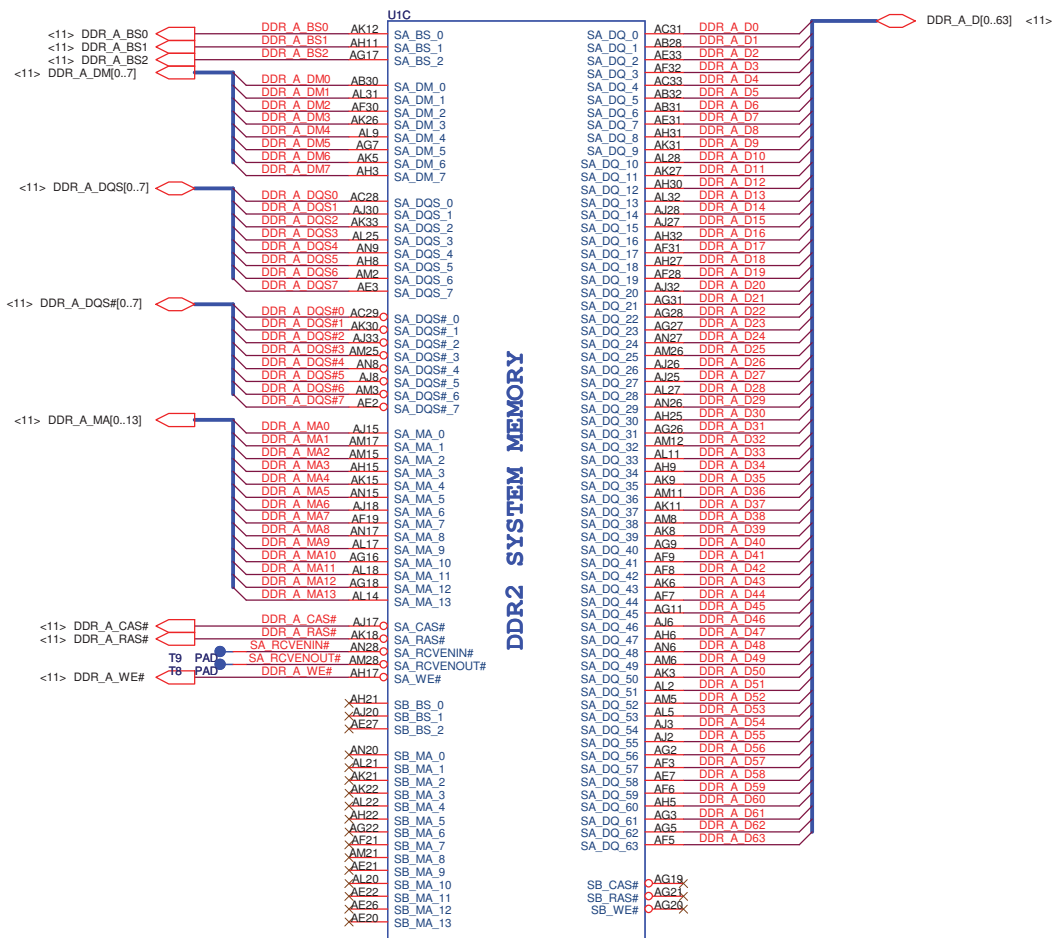


C50 to be placed <100mils from GMCH pin

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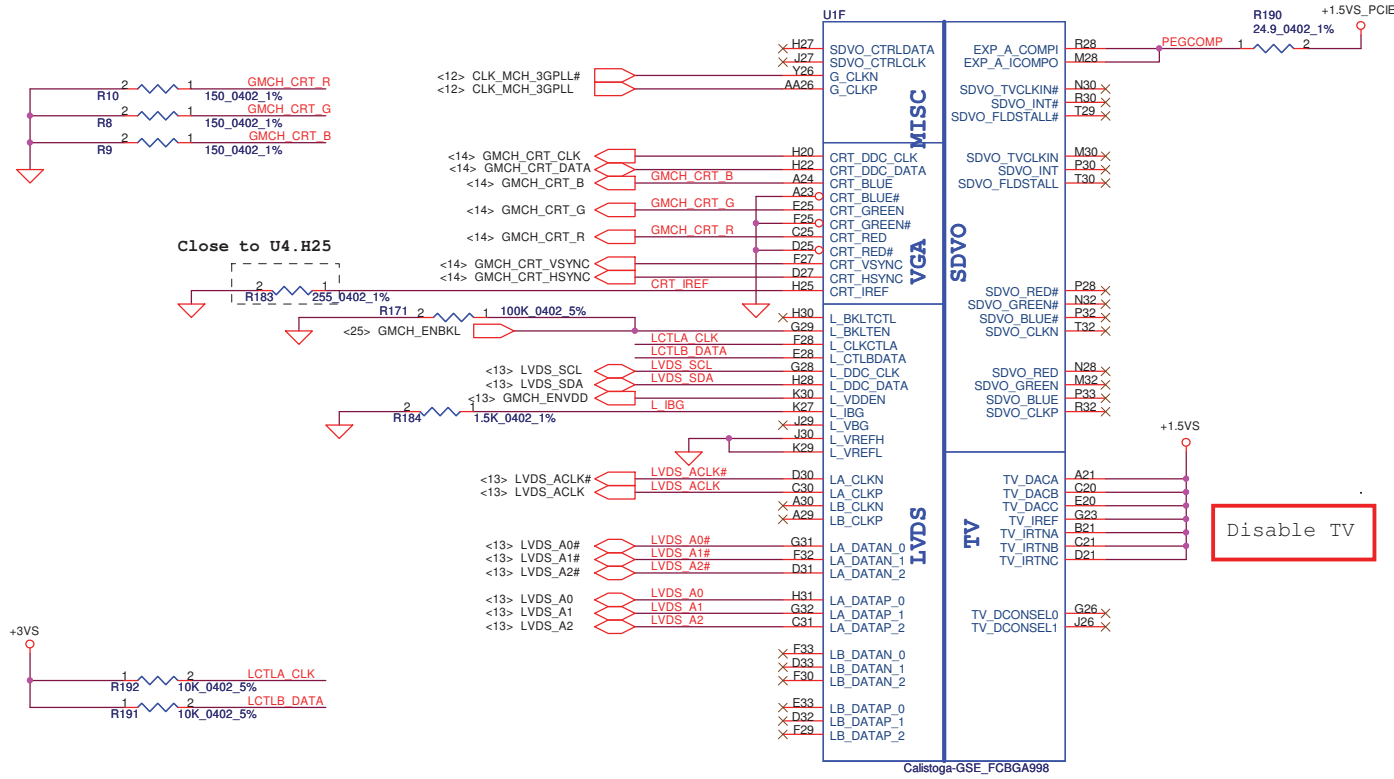
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Calistoga(1/5)-GTL/DMI/DDR			
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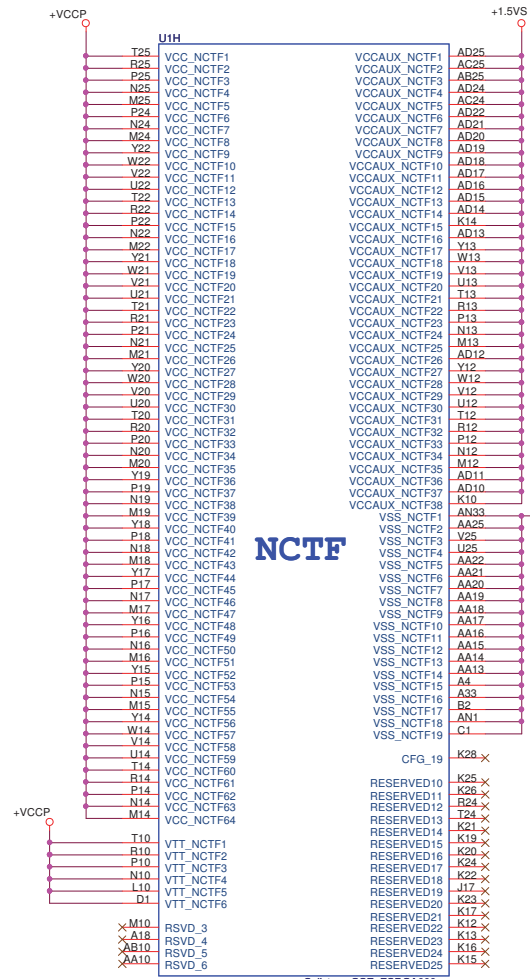
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Disable TV

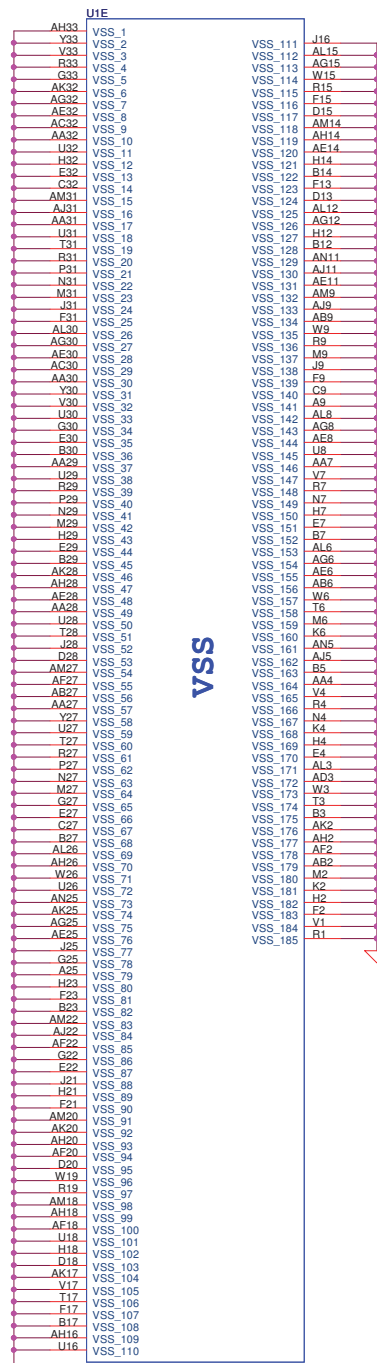
Calistoga-GSE_FCBGA998

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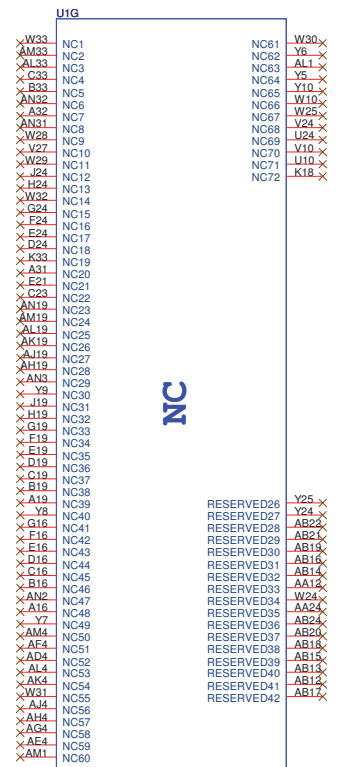
NCTF

Calistoga-GSE_FCBGA998



VSS

Calistoga-GSE_FCBGA998



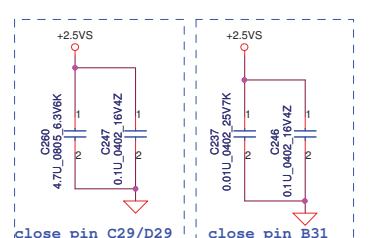
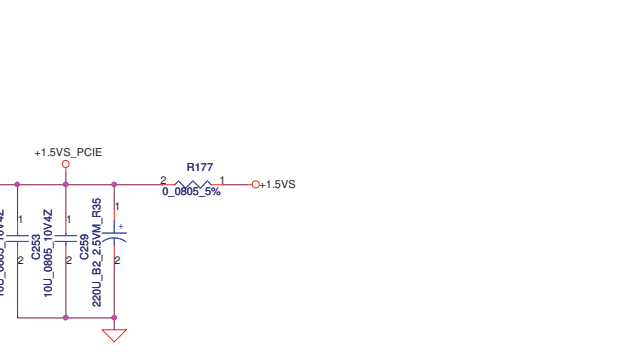
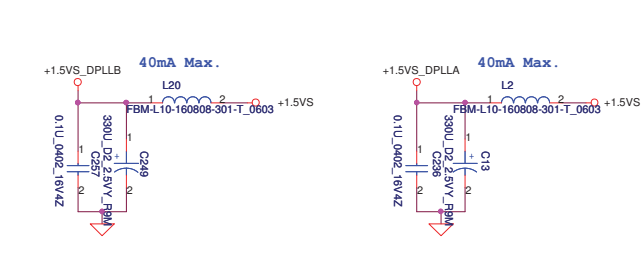
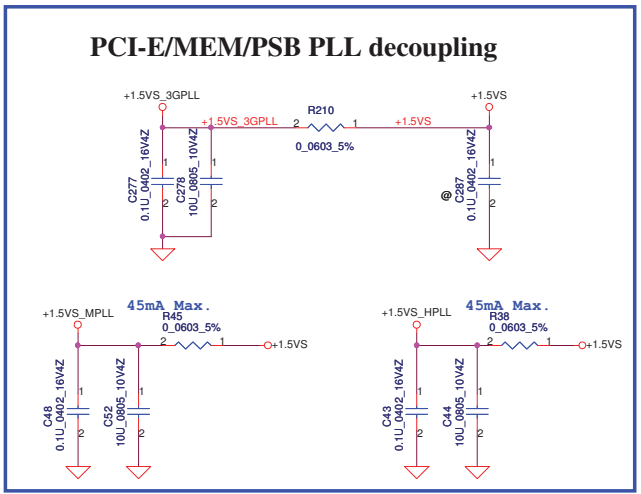
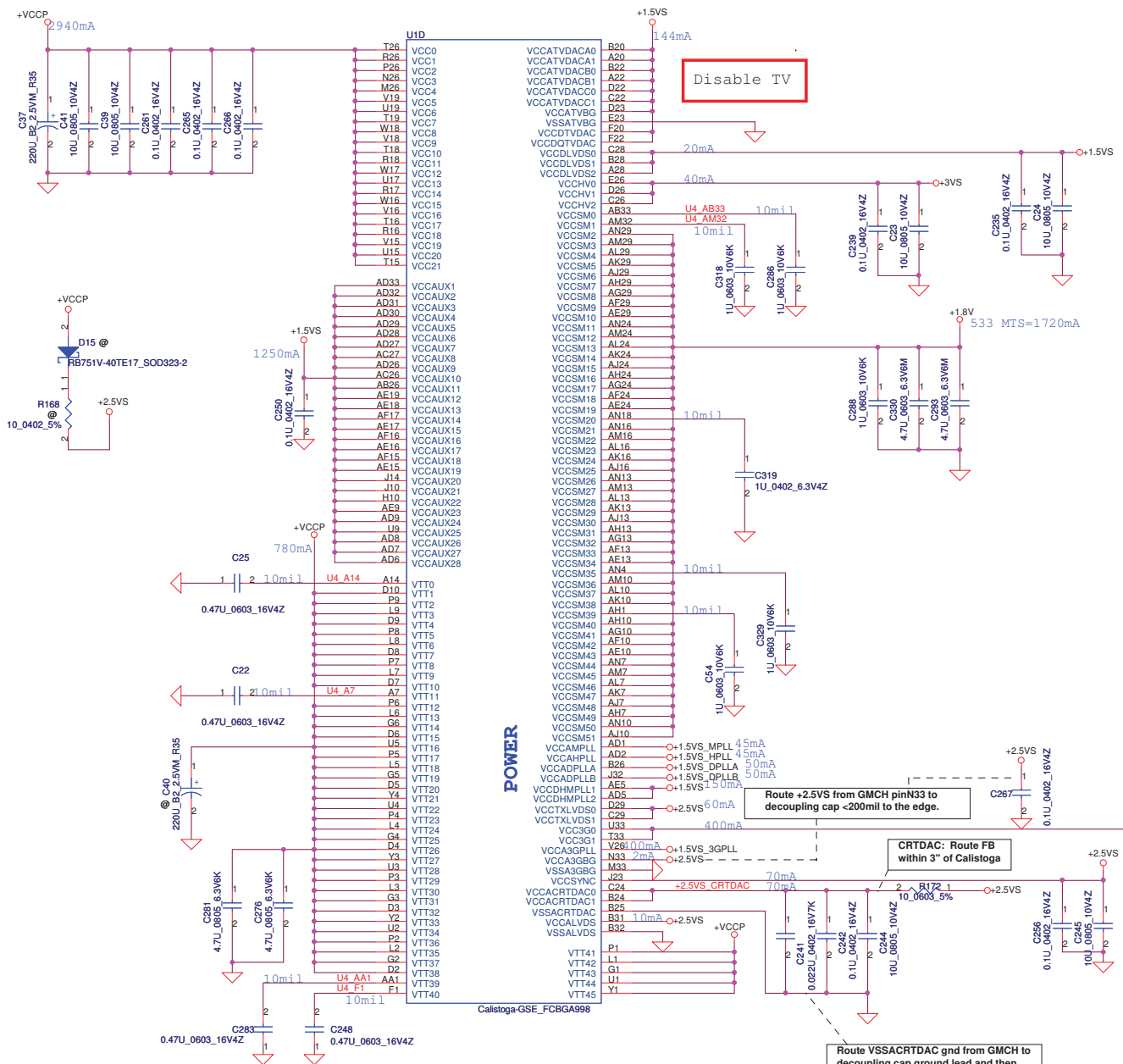
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Calistoga-GSE_FCBGA998



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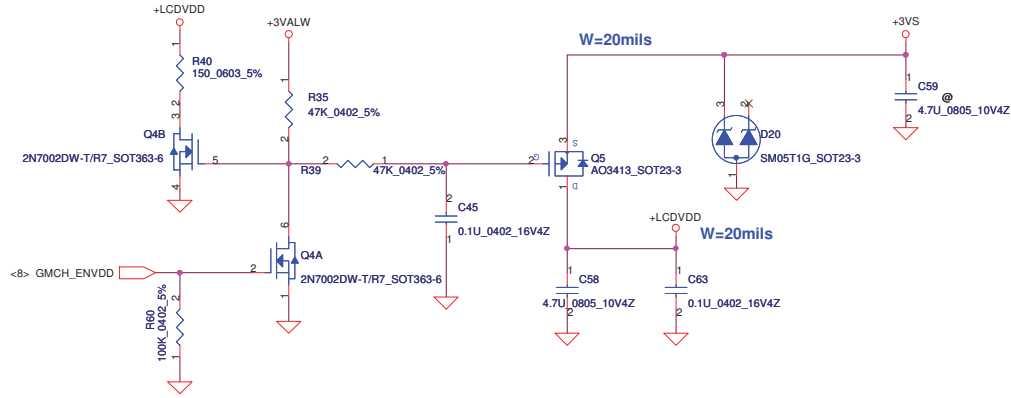


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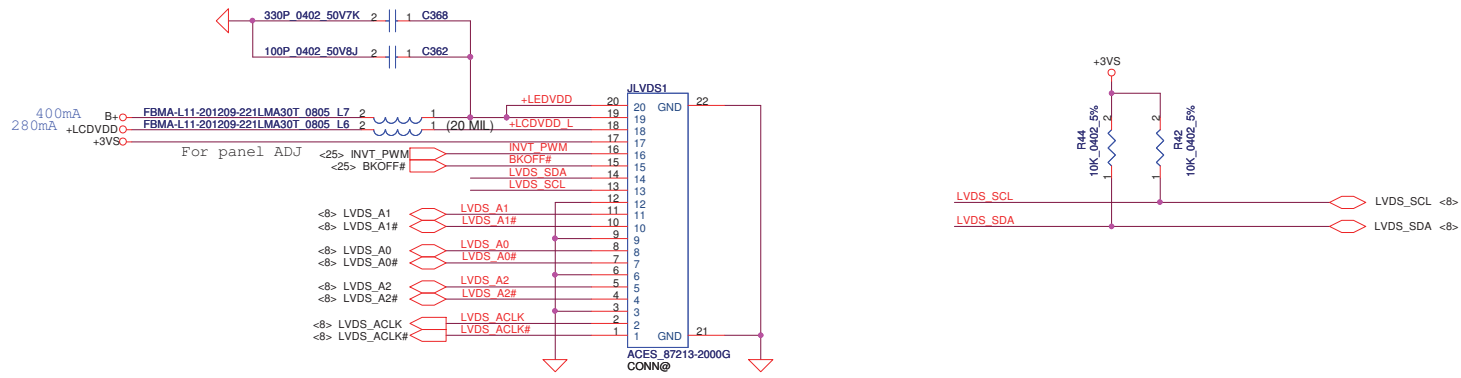
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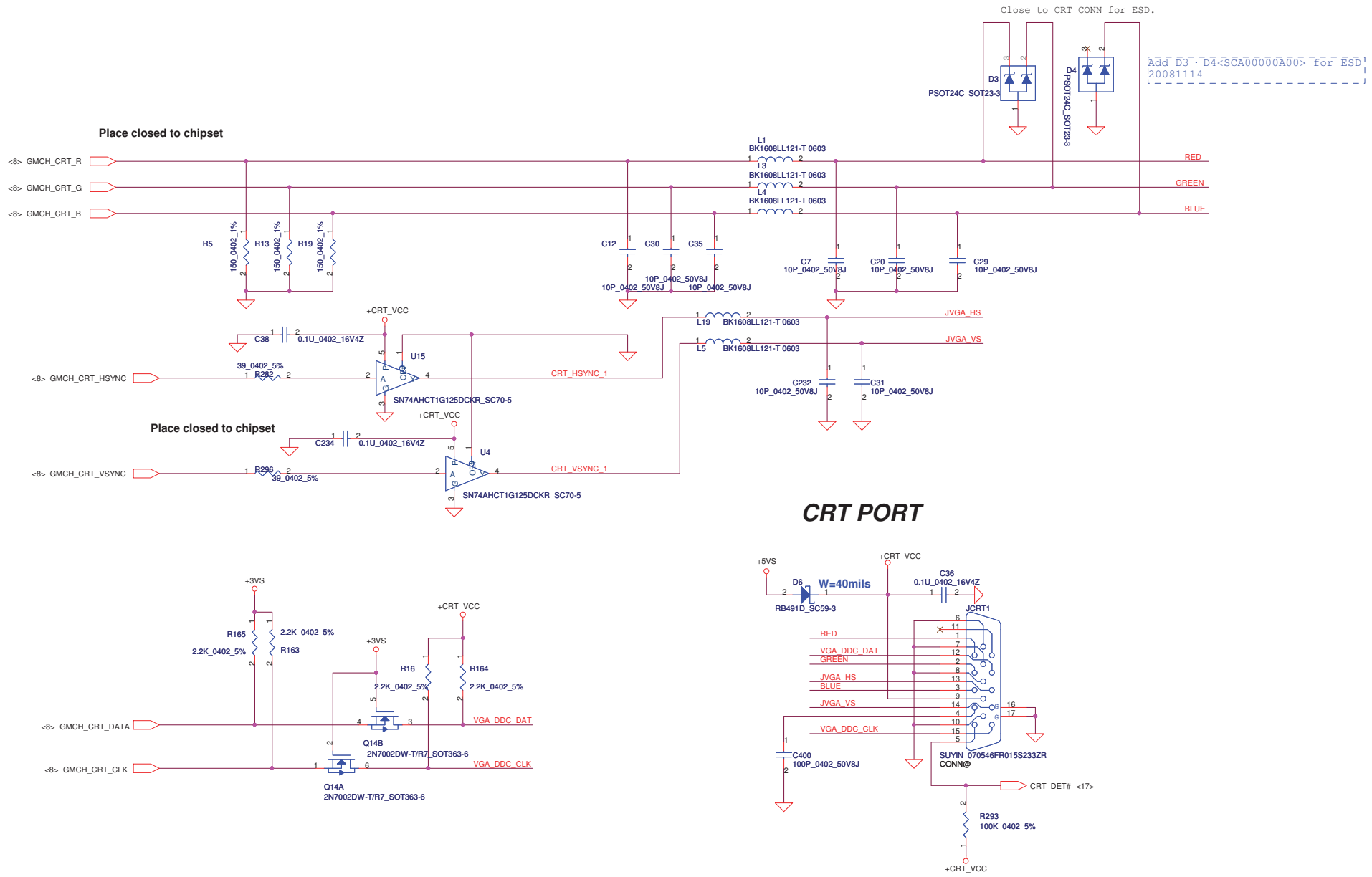
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



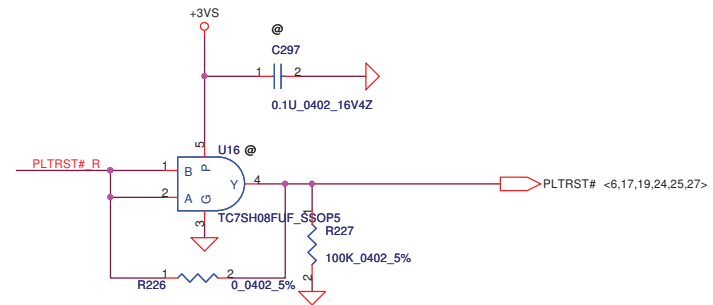
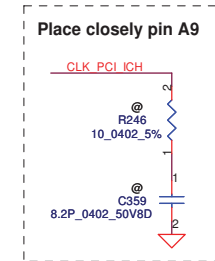
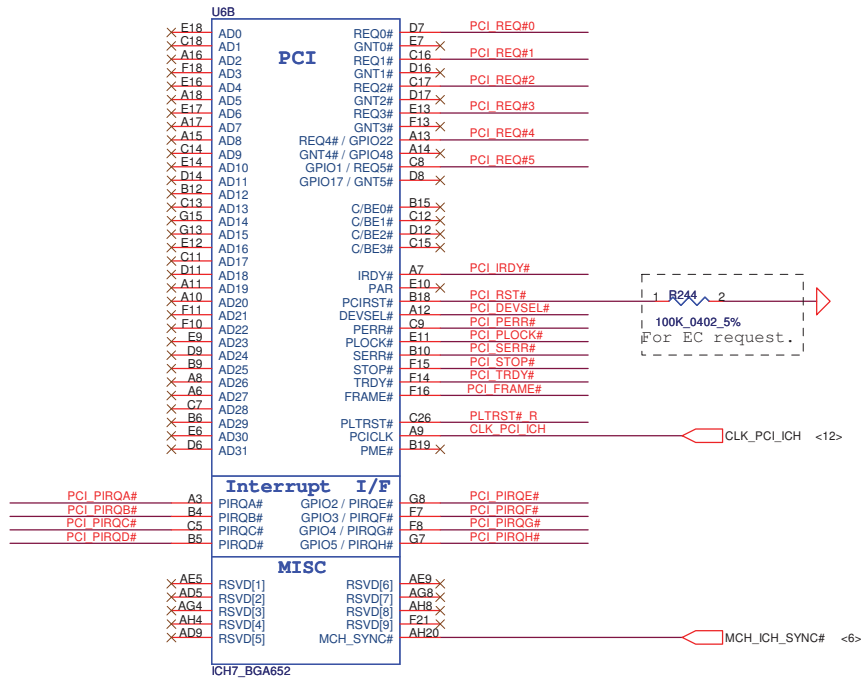
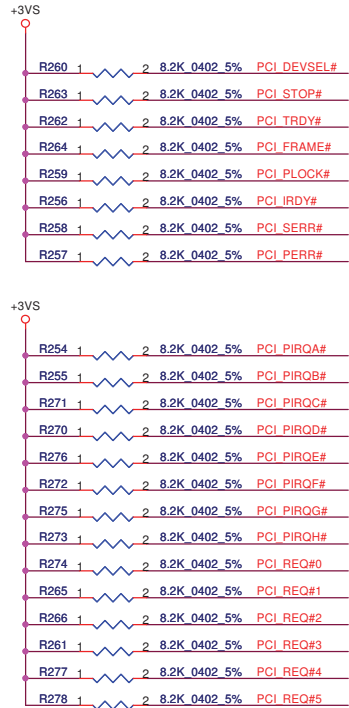
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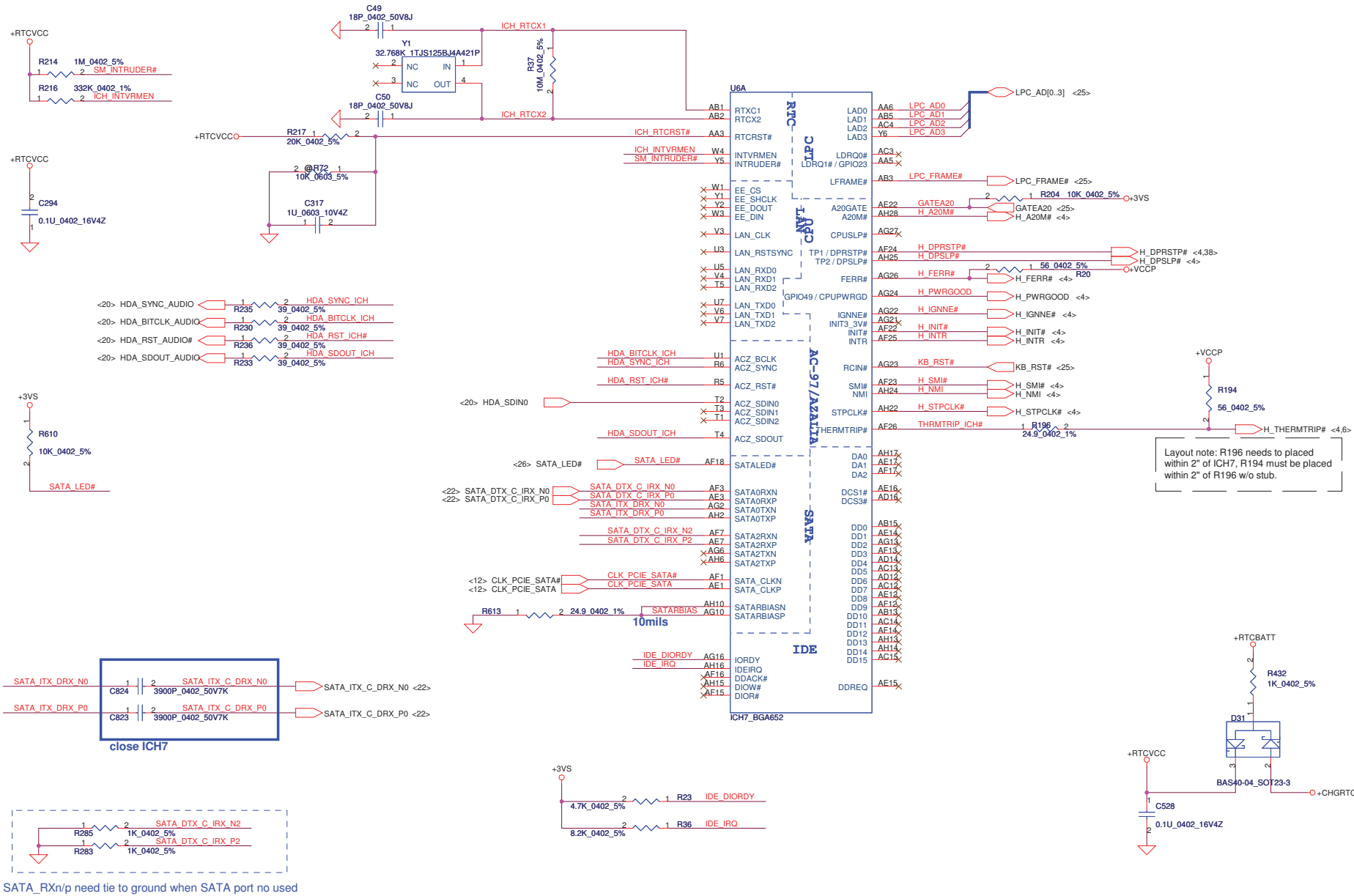
CRT PORT

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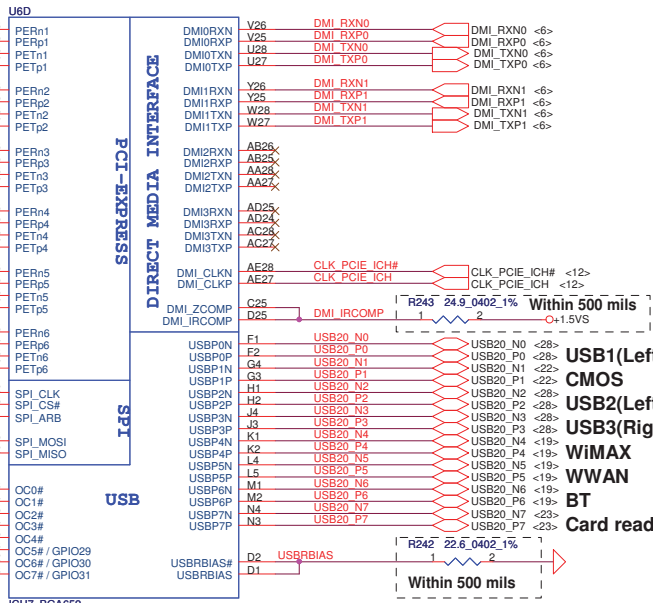
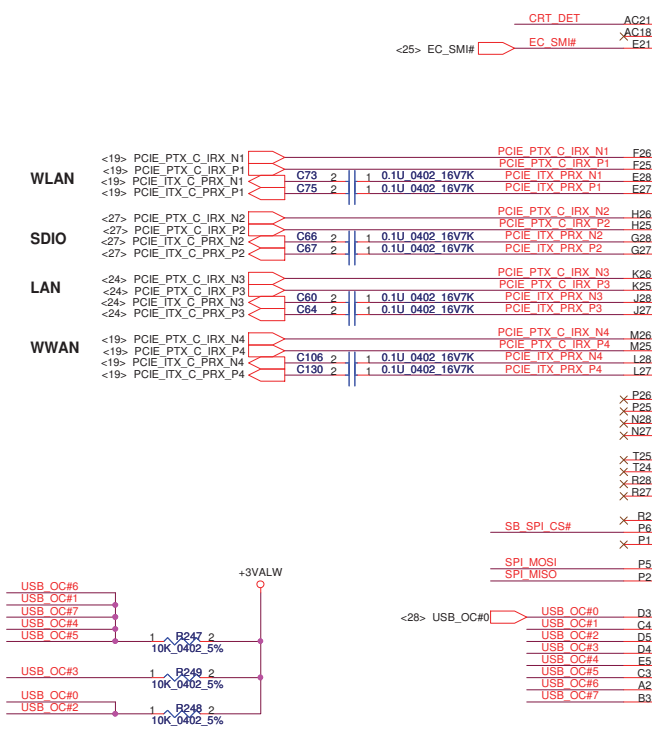
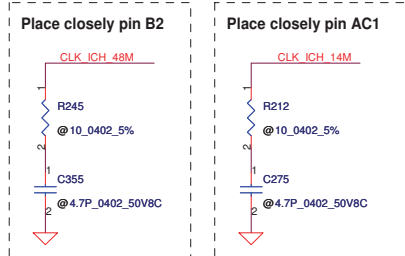
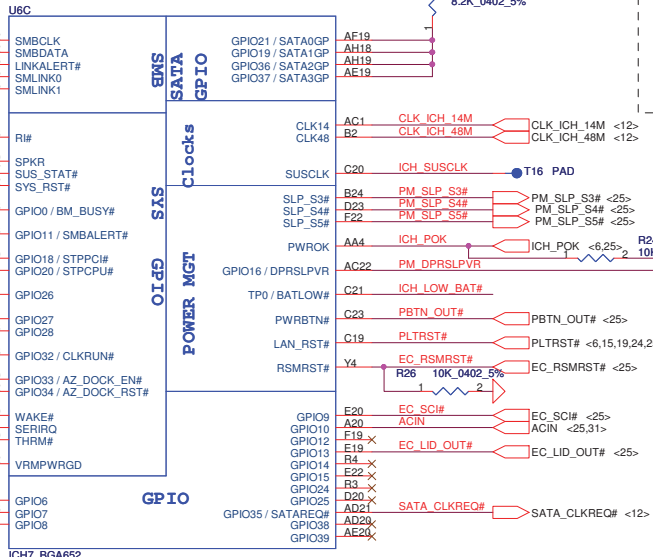
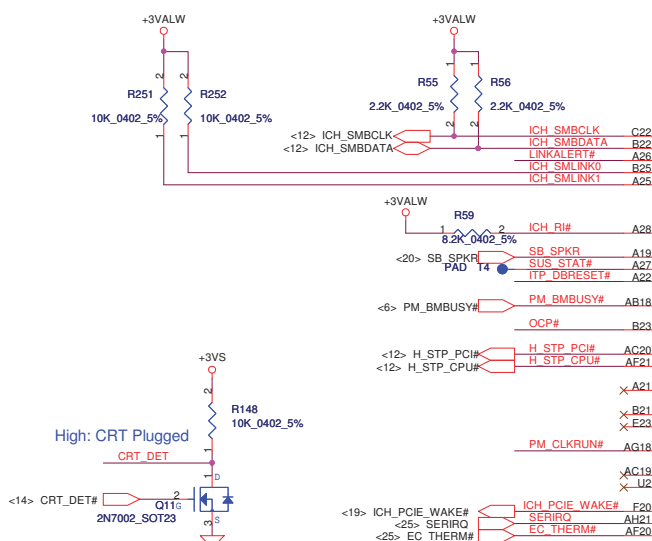
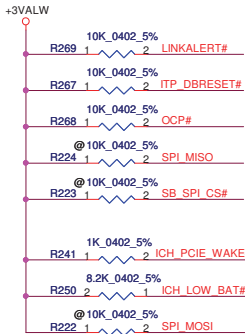
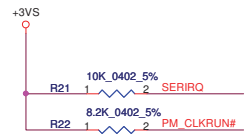


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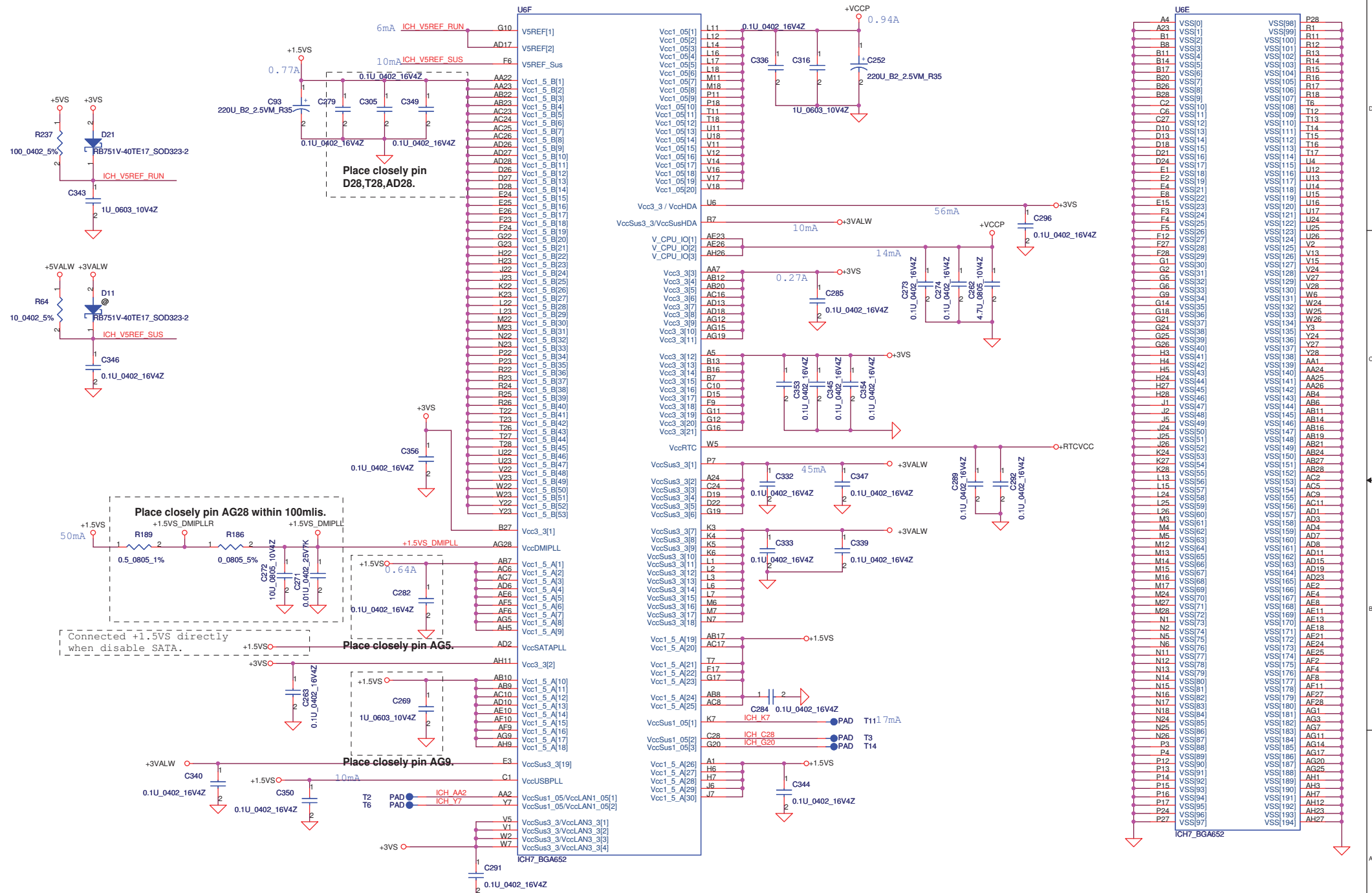
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- USB1(Left)
- CMOS
- USB2(Left)
- USB3(Right)
- WIMAX
- WWAN
- BT
- Card reader

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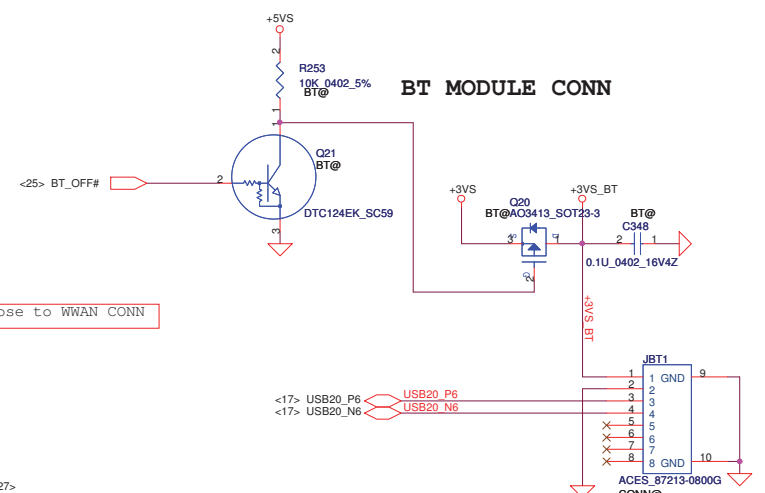
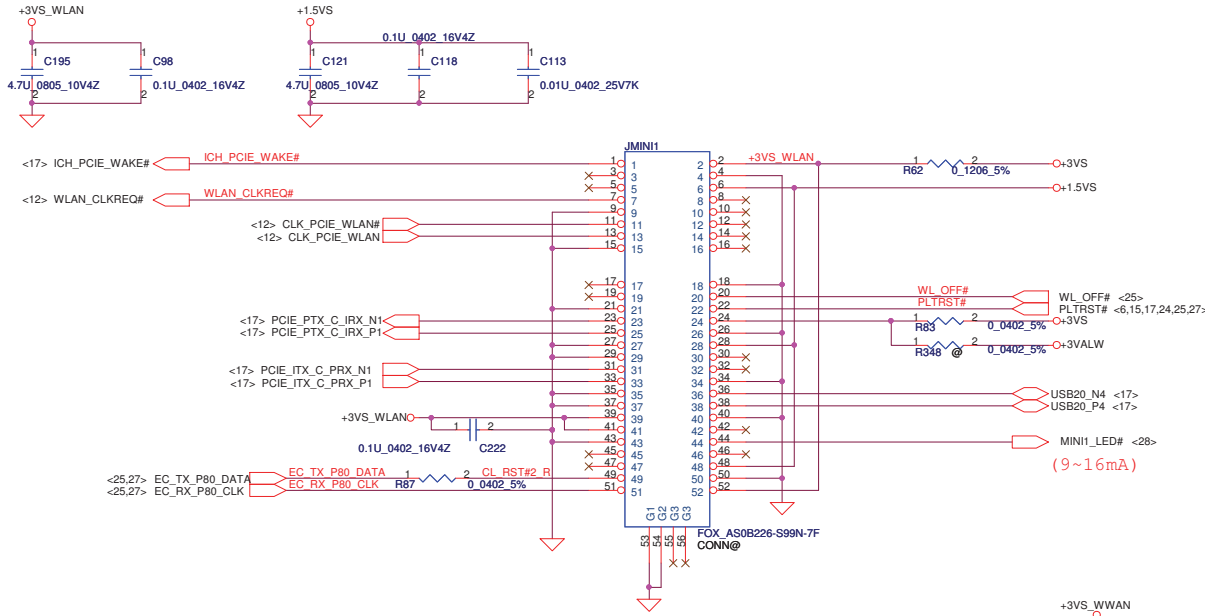
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	ICH7M(3/4)USB,GPIO,PCIE	
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Size	Document Number	KAV10 LA-4781P		Rev	1.0
Date:	Tuesday, December 30, 2008	Sheet	17	of 40	



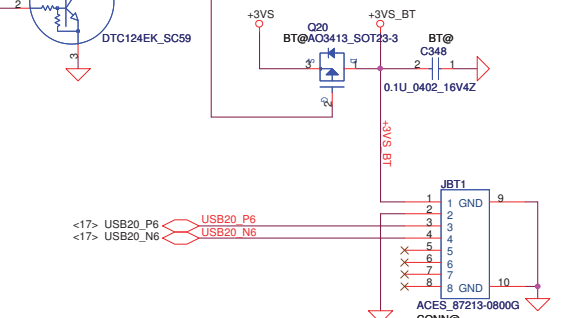
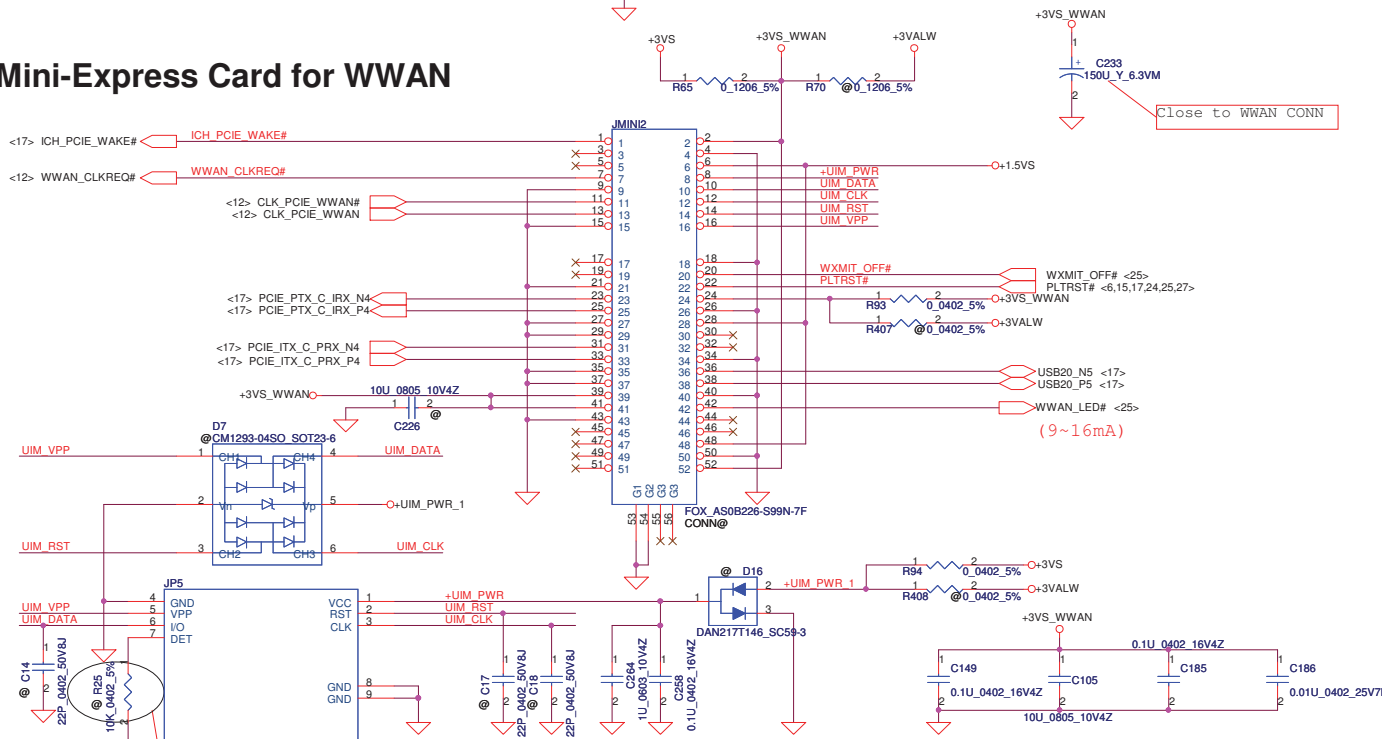
deddy.suyanto@gmail.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH7M(4)POWER/GND
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Date:	Tuesday, December 30, 2008	Sheet	18	of	40

Mini-Express Card for WLAN

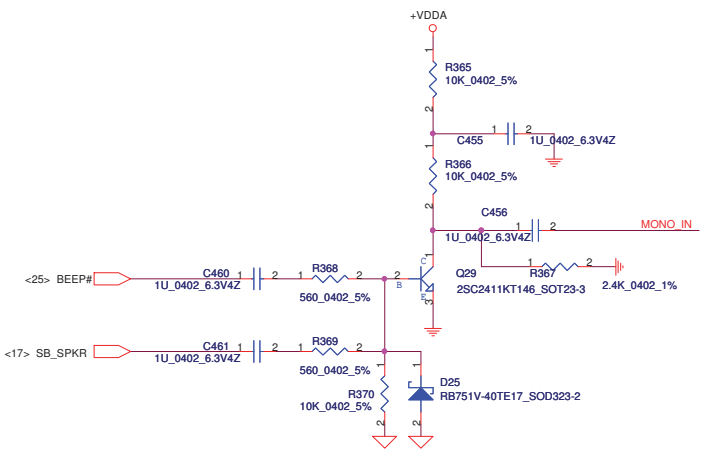


Mini-Express Card for WWAN

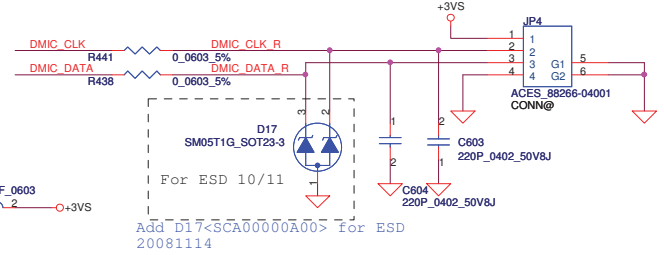
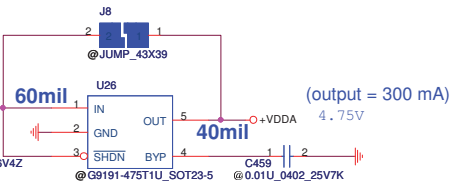
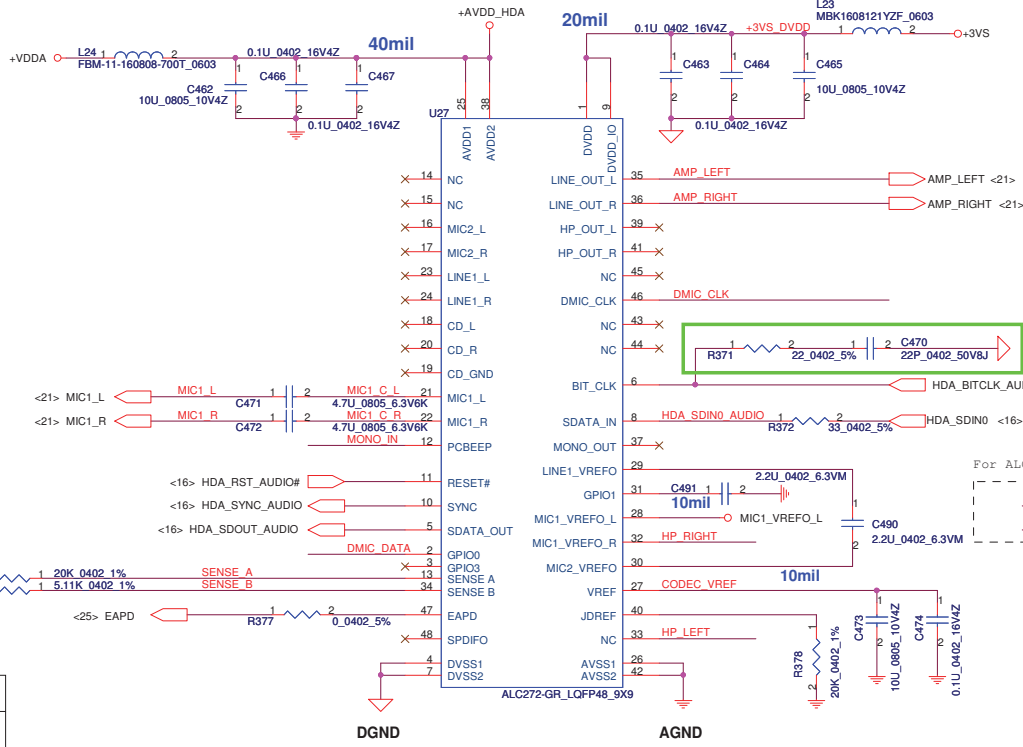


Reserve for SIM card does not meet rise time and pull-up is needed.
deddy.suyanto@gmail.com

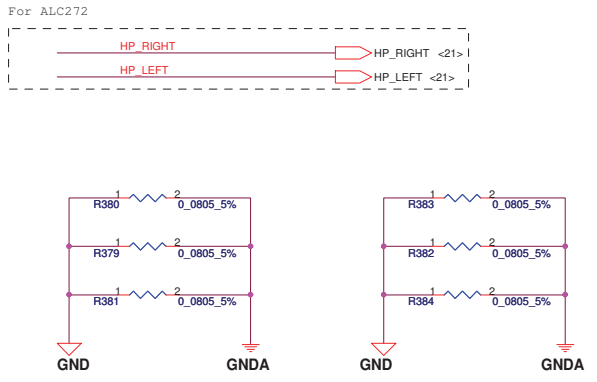
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	Mini-Card/BT CONN	
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HD Audio Codec



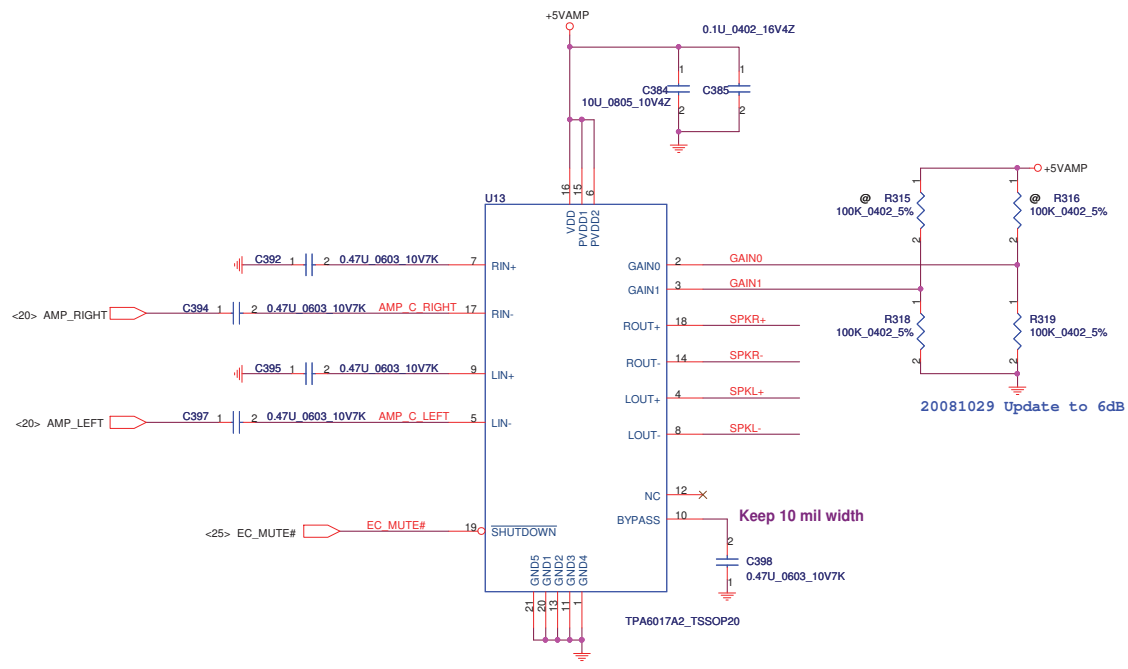
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



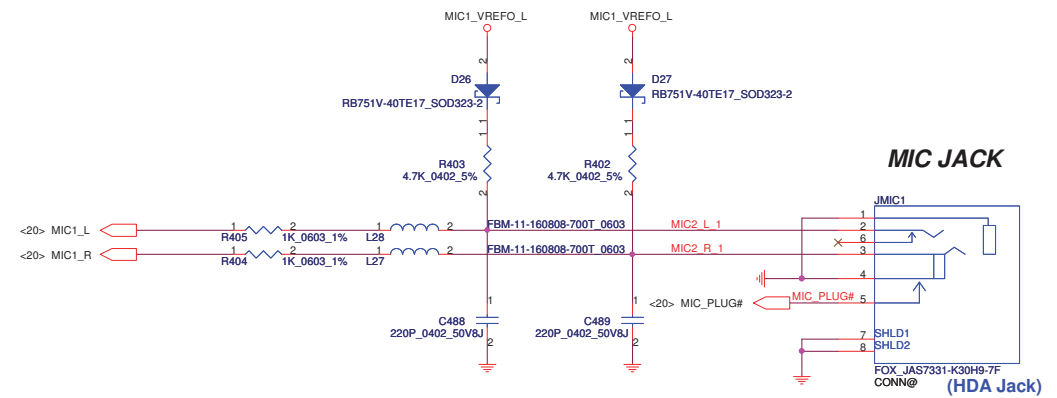
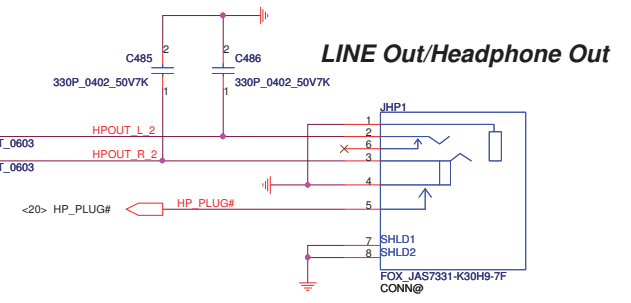
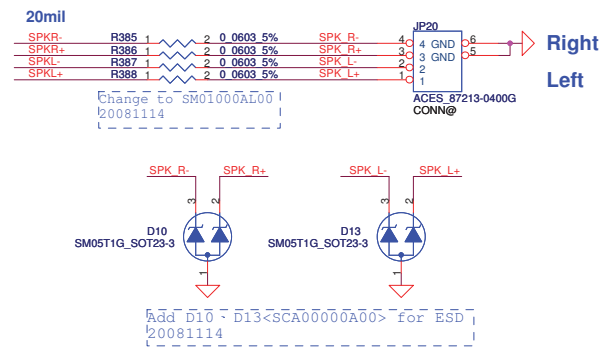
Change to SA00002C120 ALC272X-GR 20081204

daddy.suyanto@gmail.com

Security Classification		Compal Secret Data		Title	
Issued Date	2006/12/25	Deciphered Date	2007/8/18	HD Audio Codec ALC272	
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				Date: Tuesday, December 30, 2008	Sheet 20 of 40



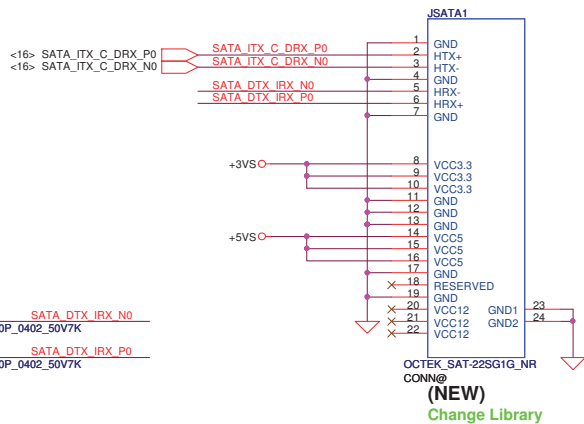
Int. Speaker Conn.



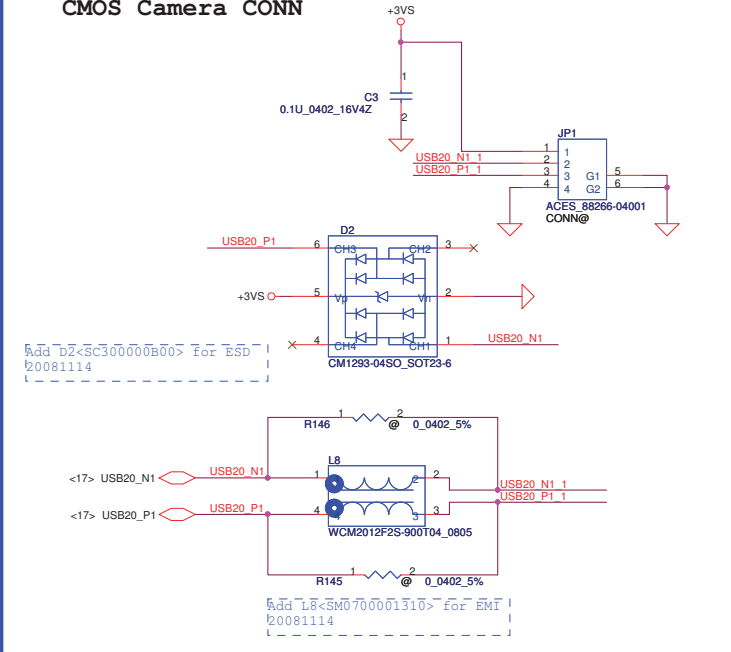
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Security Classification		Compal Secret Data		Title	
Issued Date	2006/12/25	Deciphered Date	2007/8/18	Amplifier & Audio Jack	
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SATA HDD Conn.

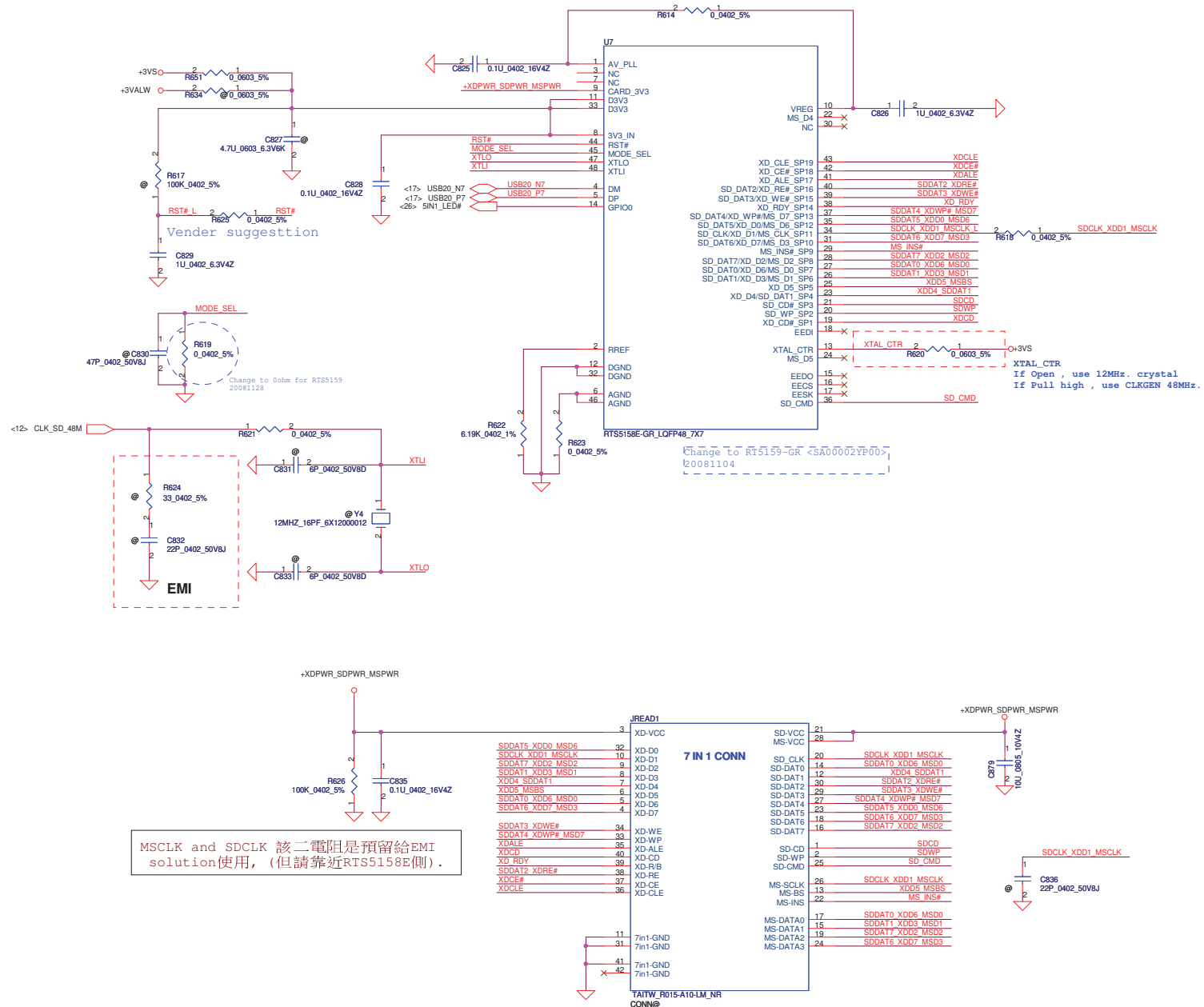


CMOS Camera CONN



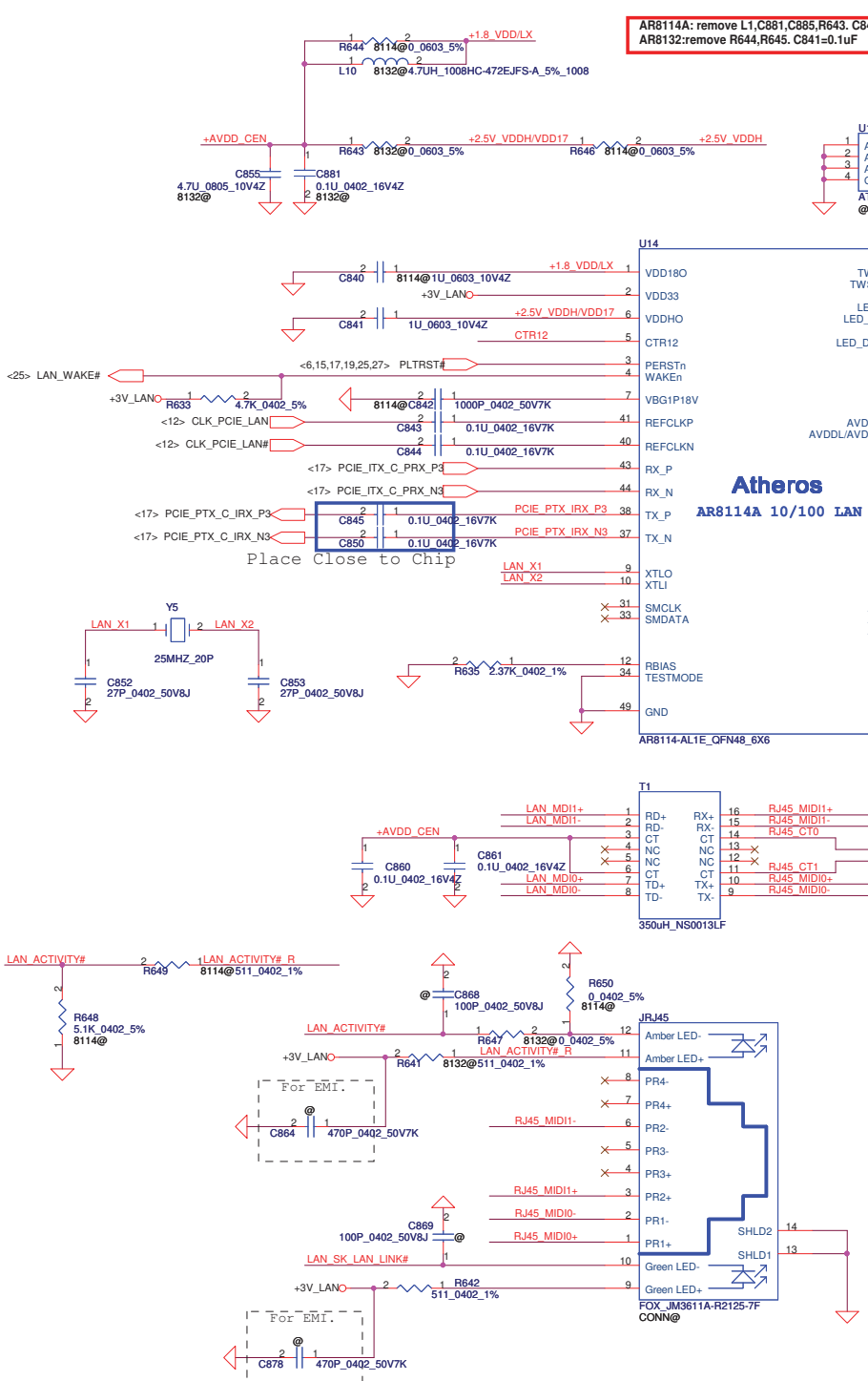
deddy.suyanto@gmail.com

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				SATA HDD/SSD	
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				KAV10 LA-4781P	
				Date:	Tuesday, December 30, 2008
				Sheet	22 of 40
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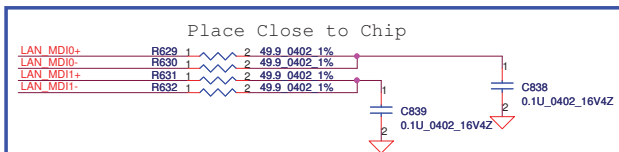


MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).

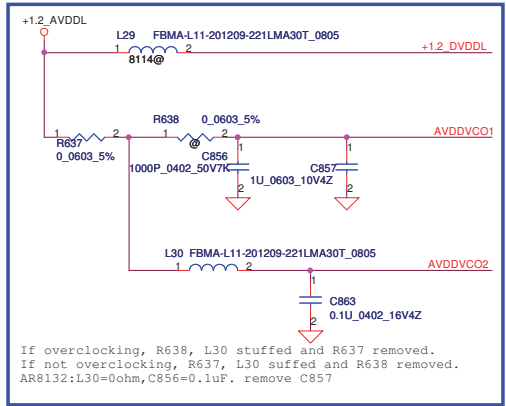
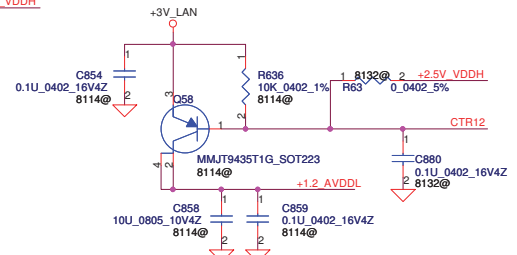
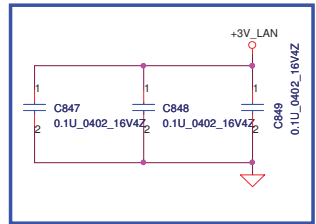
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2007/8/18	5 in 1 Card reader
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Date: Tuesday, December 30, 2008				Sheet 23 of 40



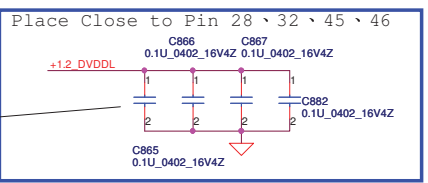
AR8114A: remove L1, C881, C885, R643. C841=1uF
 AR8132: remove R644, R645. C841=0.1uF



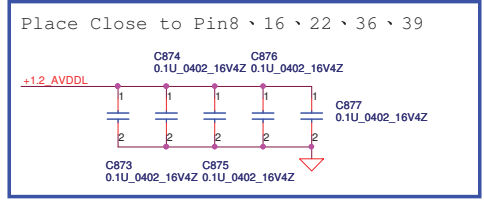
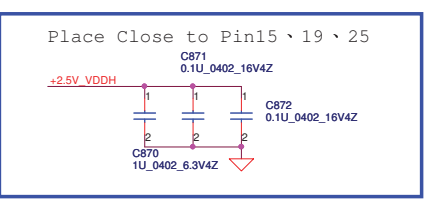
Layout Notice : Place as close chip as possible.



If overclocking, R638, L30 stuffed and R637 removed.
 If not overclocking, R637, L30 stuffed and R638 removed.
 AR8132: L30=0ohm, C856=0.1uF. remove C857

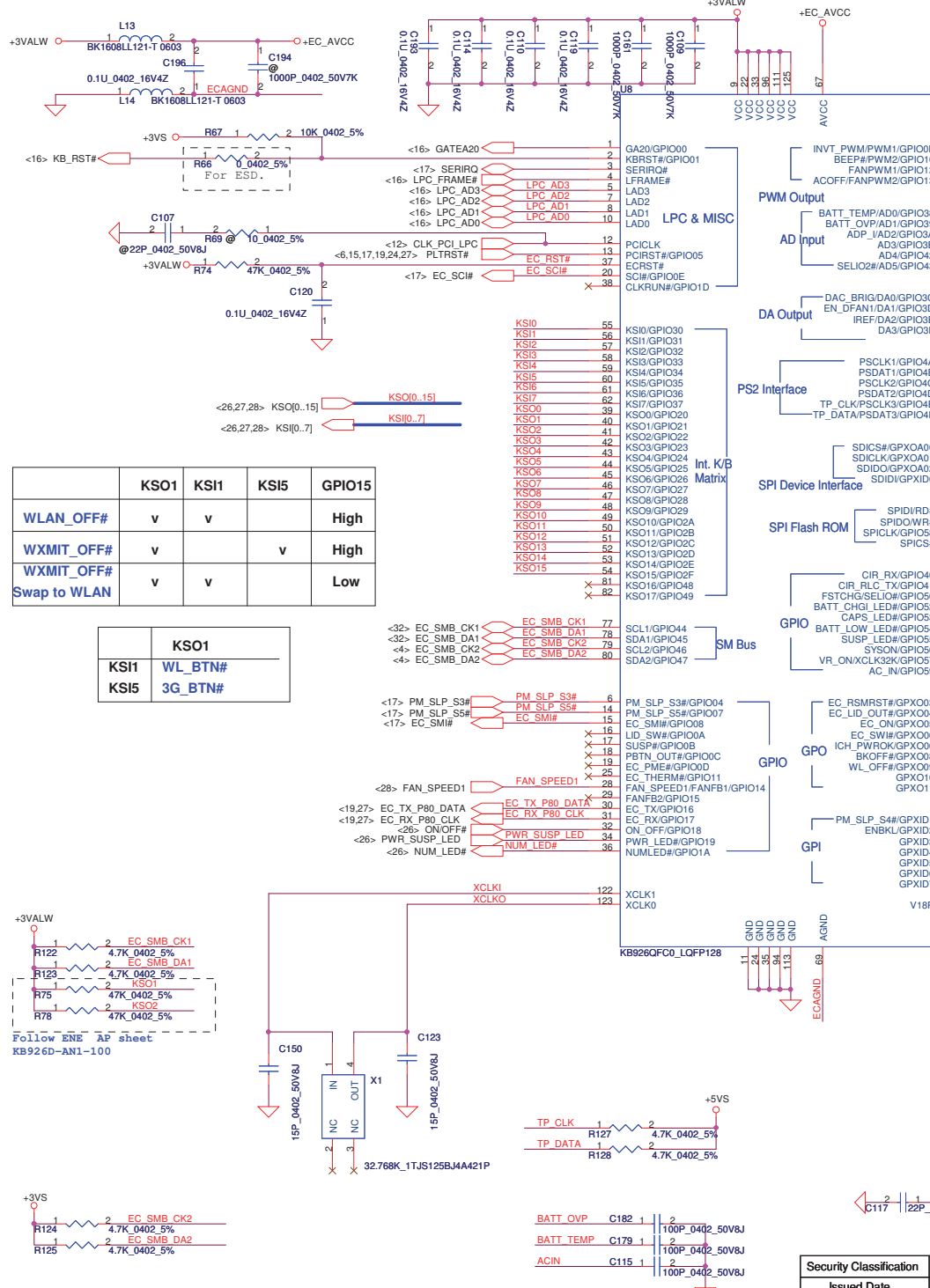


C865 close to Pin46
 AR8114A: C865=0.1uF
 AR8132: C865=1uF



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Issued Date	2006/08/04	Deciphered Date	2007/8/18	AR8114	
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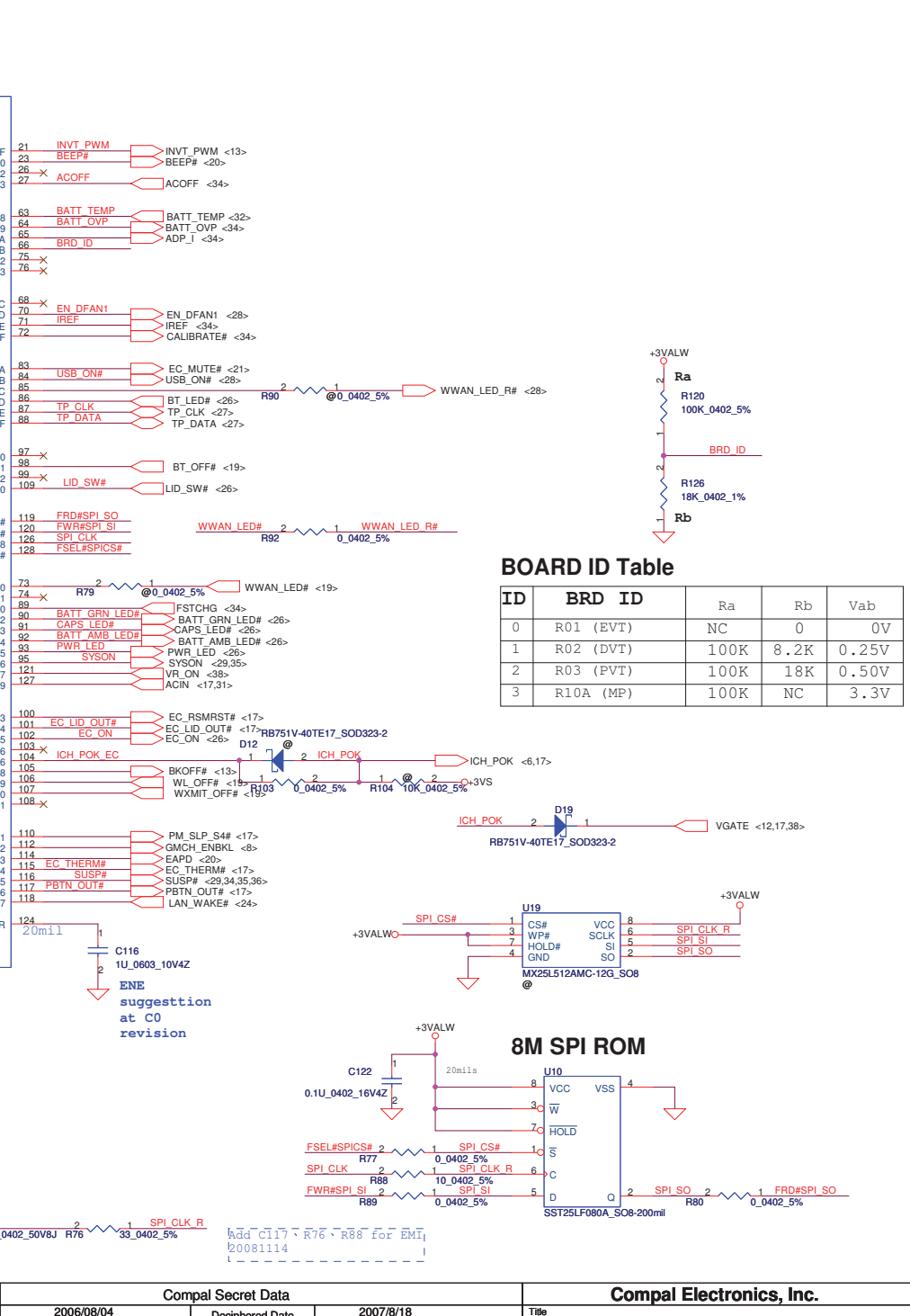


	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

KSO1	
KSI1	WL_BTN#
KSI5	3G_BTN#

Follow ENE AP sheet
KB926D-AN1-100

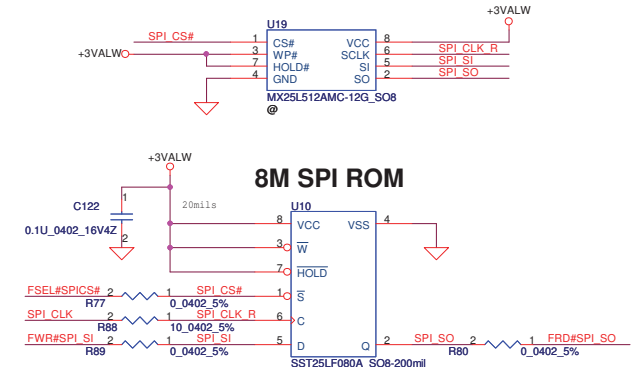
deddy.suyanto@gmail.com



BOARD ID Table

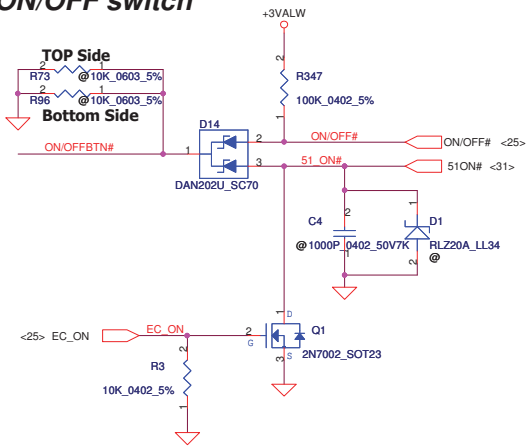
ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

8M SPI ROM

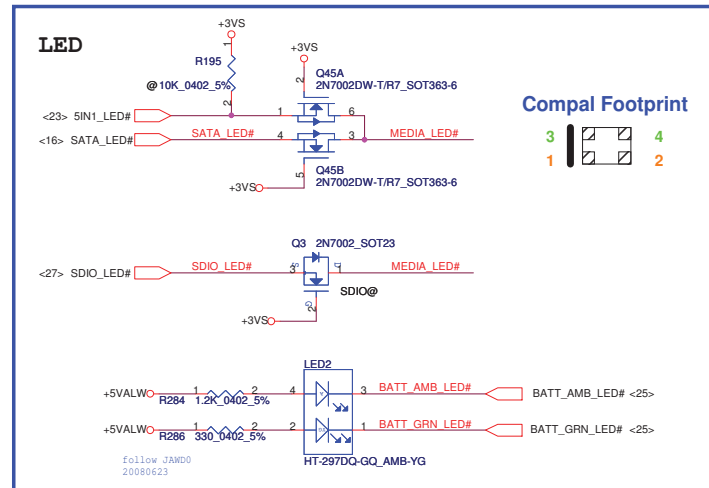
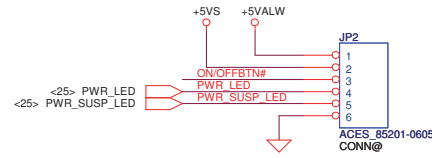


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Size	Document Number	Rev		Date	
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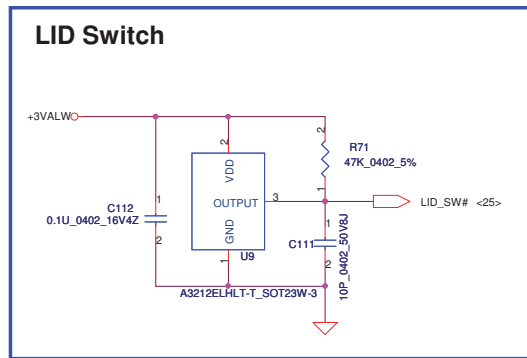
ON/OFF switch



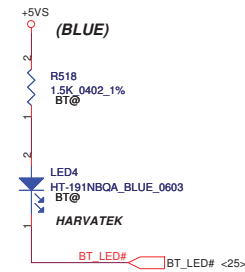
To PWR/B Conn.



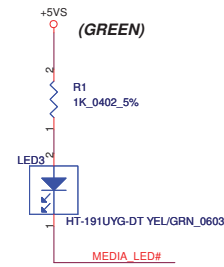
LID Switch



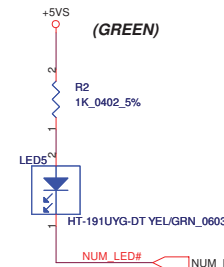
Bluetooth LED



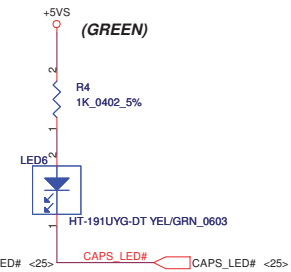
MEDIA_LED



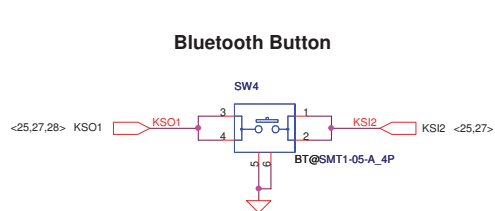
NUM_LED



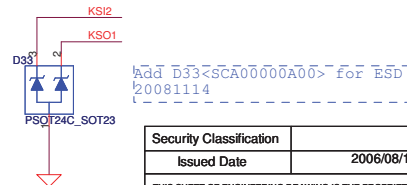
CAPS_LED



Bluetooth Button

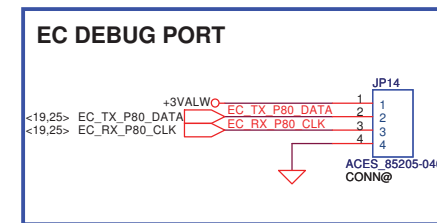
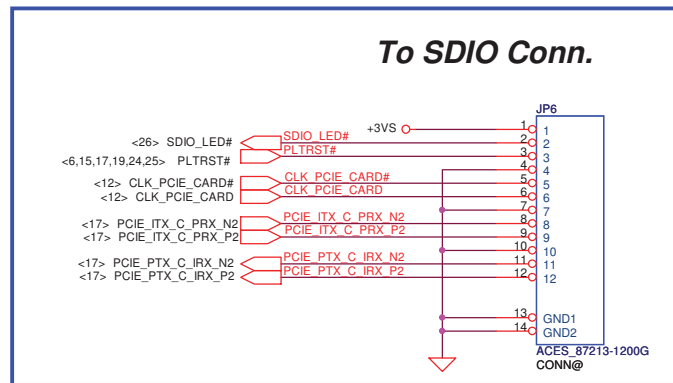
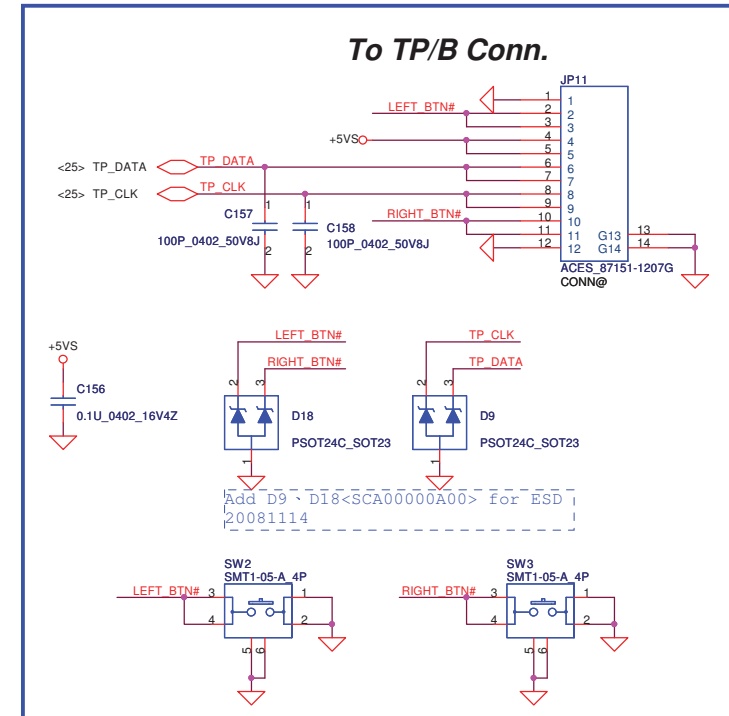
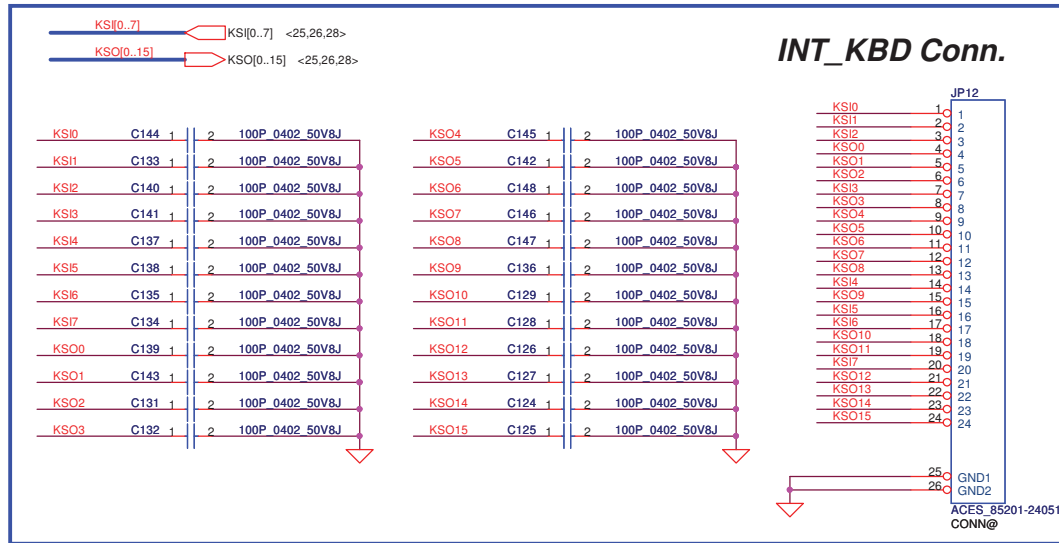


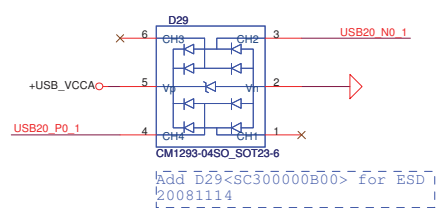
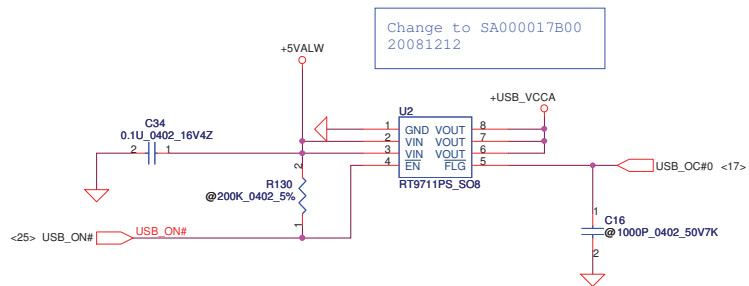
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KSI2	BT_BTN#



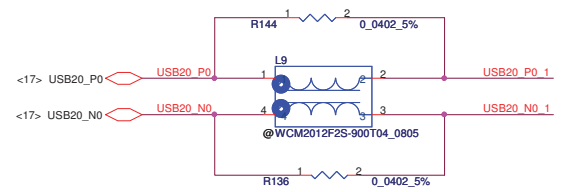
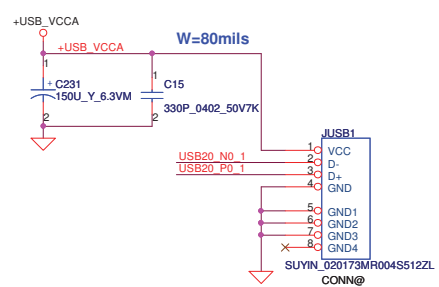
deddy.suyanto@gmail.com

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Issued Date		Deciphered Date		Title	
2006/08/18		2007/8/18		LID SW/LED/CMOS	
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Size B	Document Number			Rev	
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Tuesday, December 30, 2008		26		40	





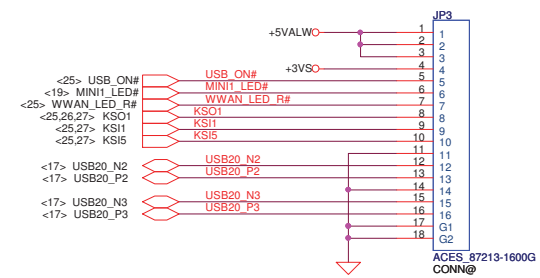
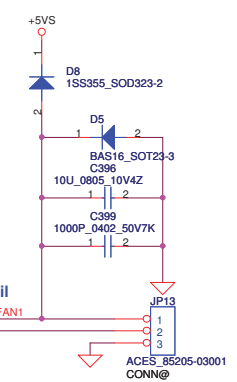
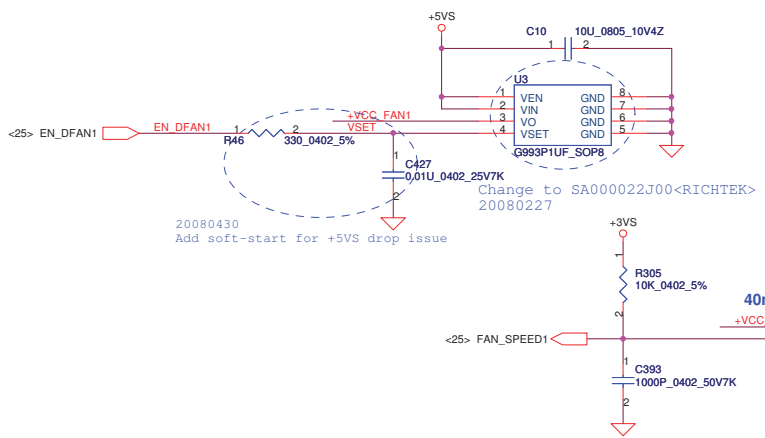
USB CONN. 1



To USB/B Conn.

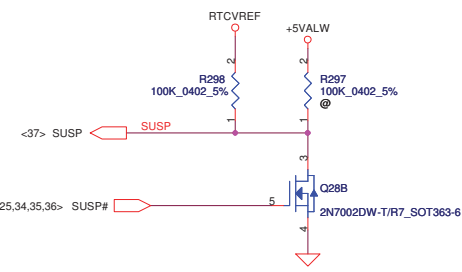
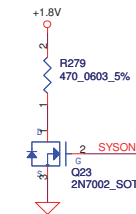
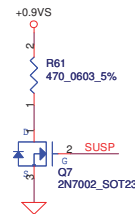
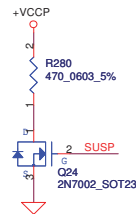
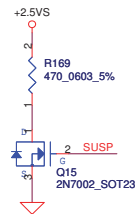
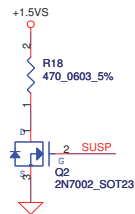
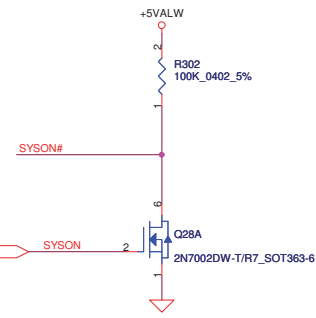
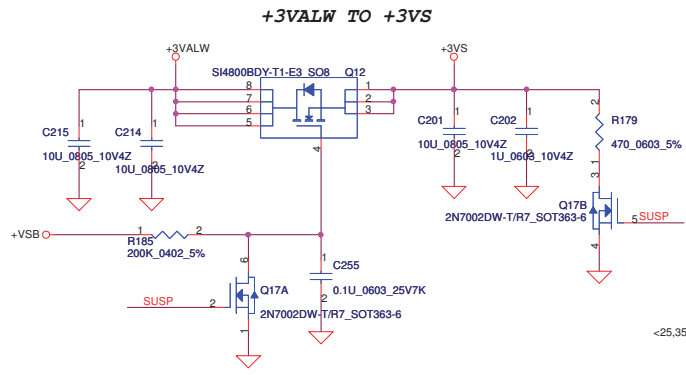
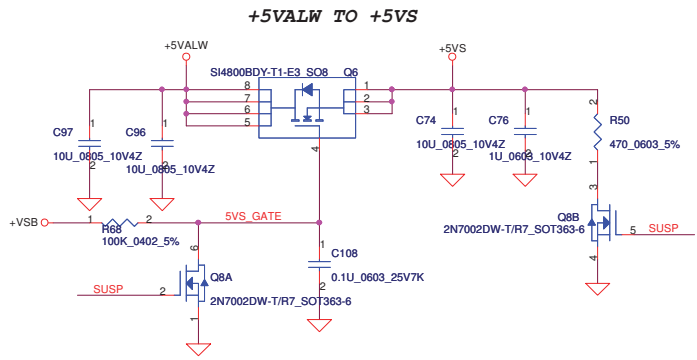
	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

FAN1 Conn



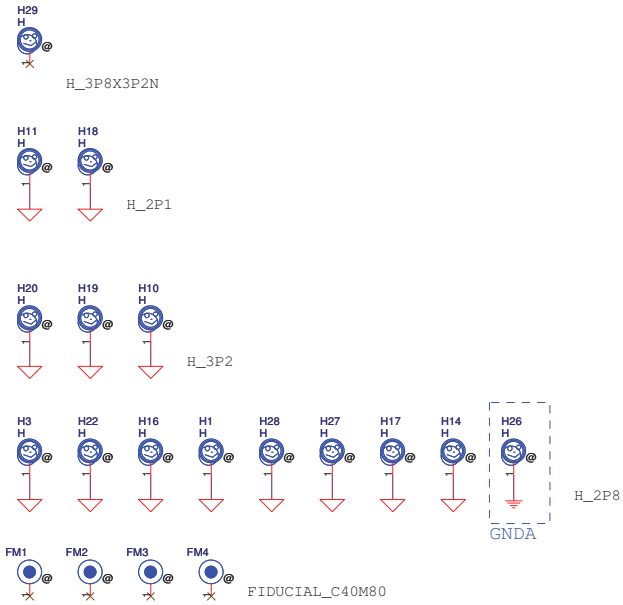
deddy.suyanto@gmail.com

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
				USB PORTS/FAN		
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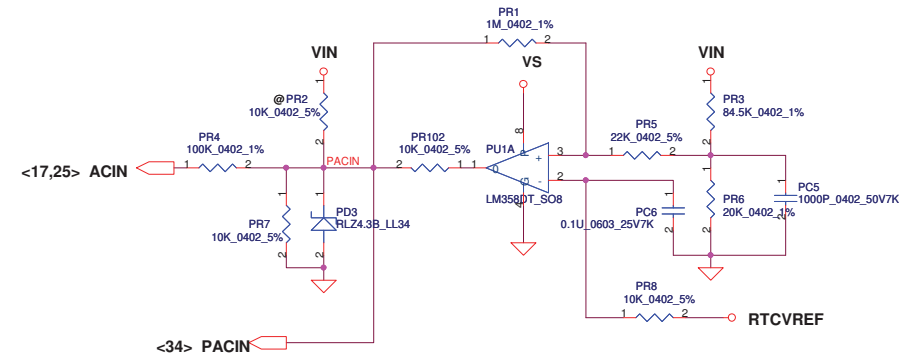
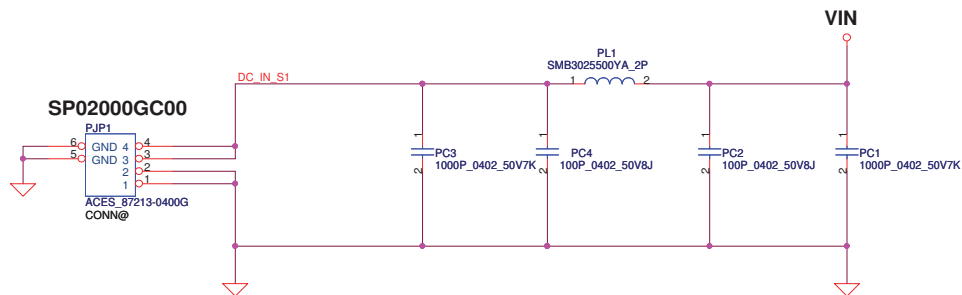


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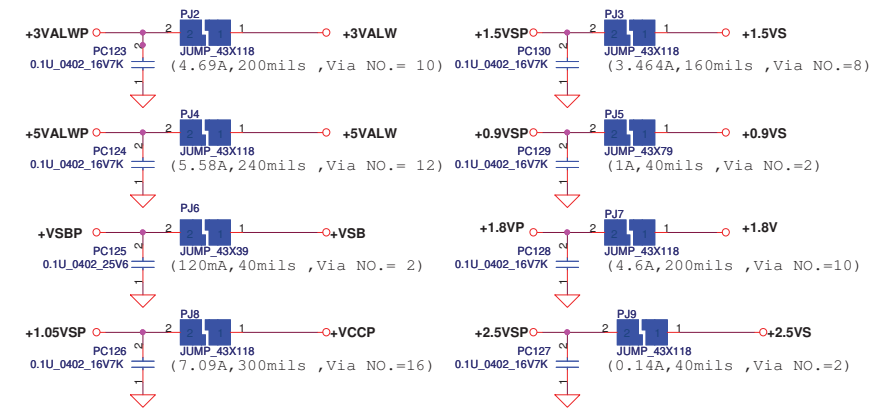
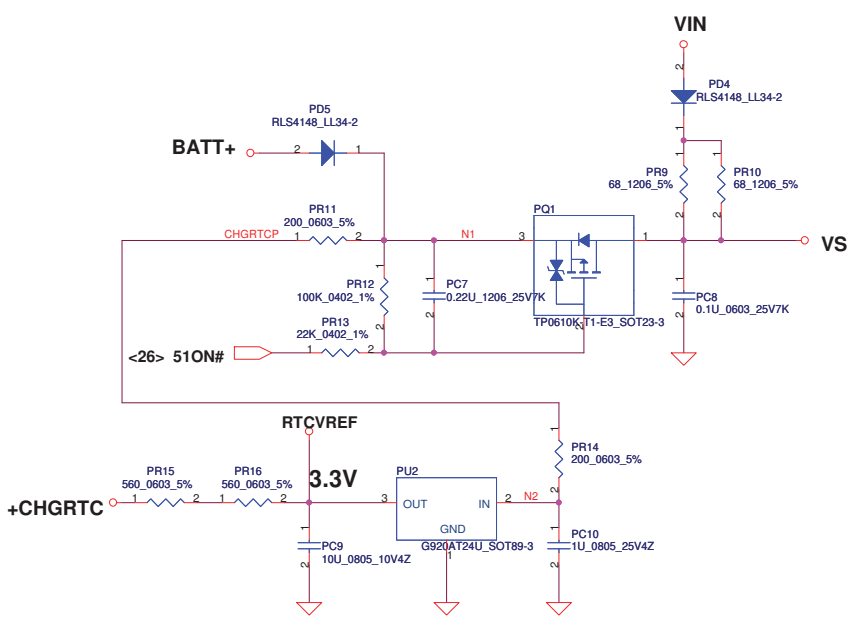
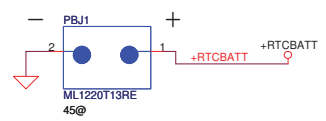
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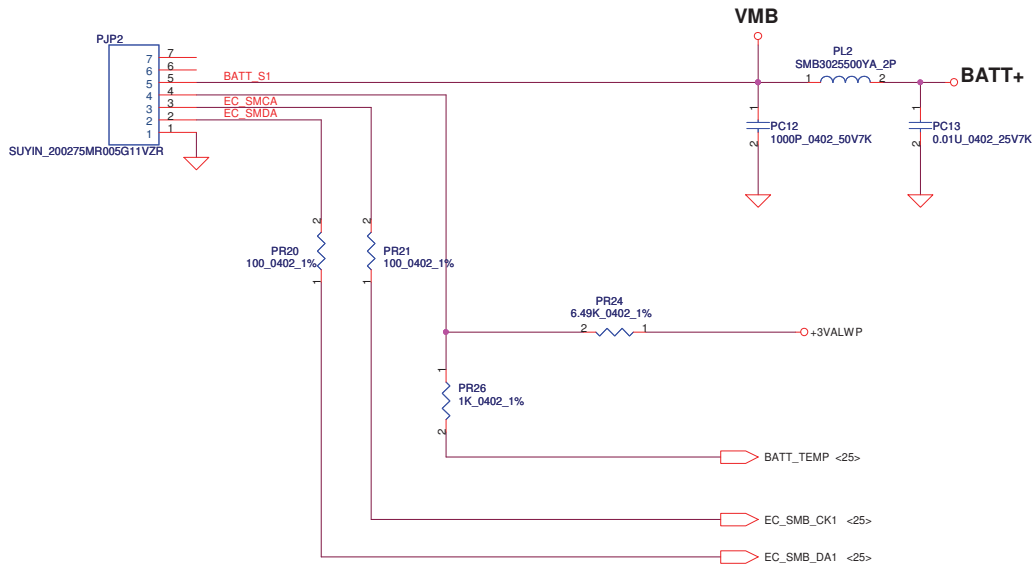


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



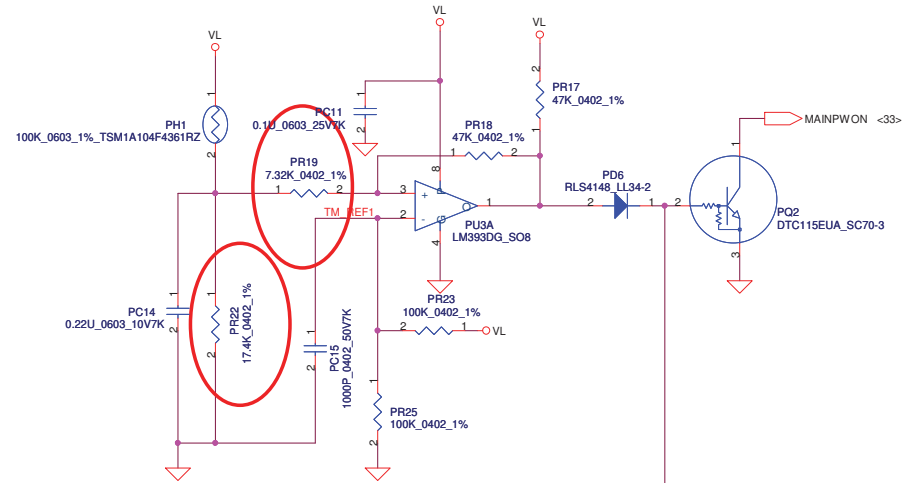
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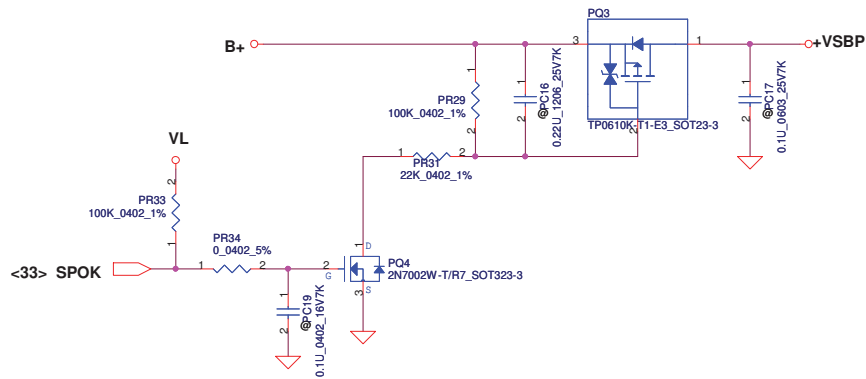
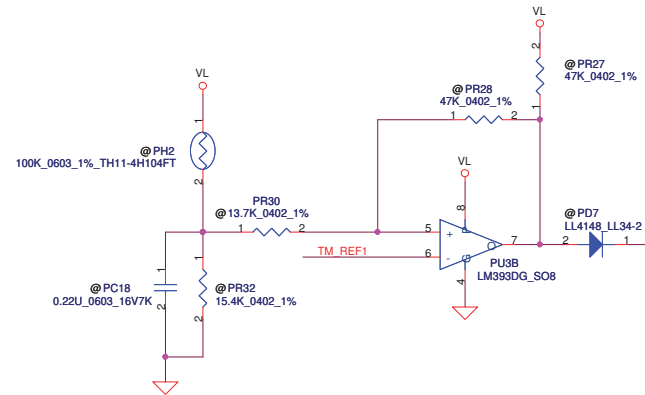
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



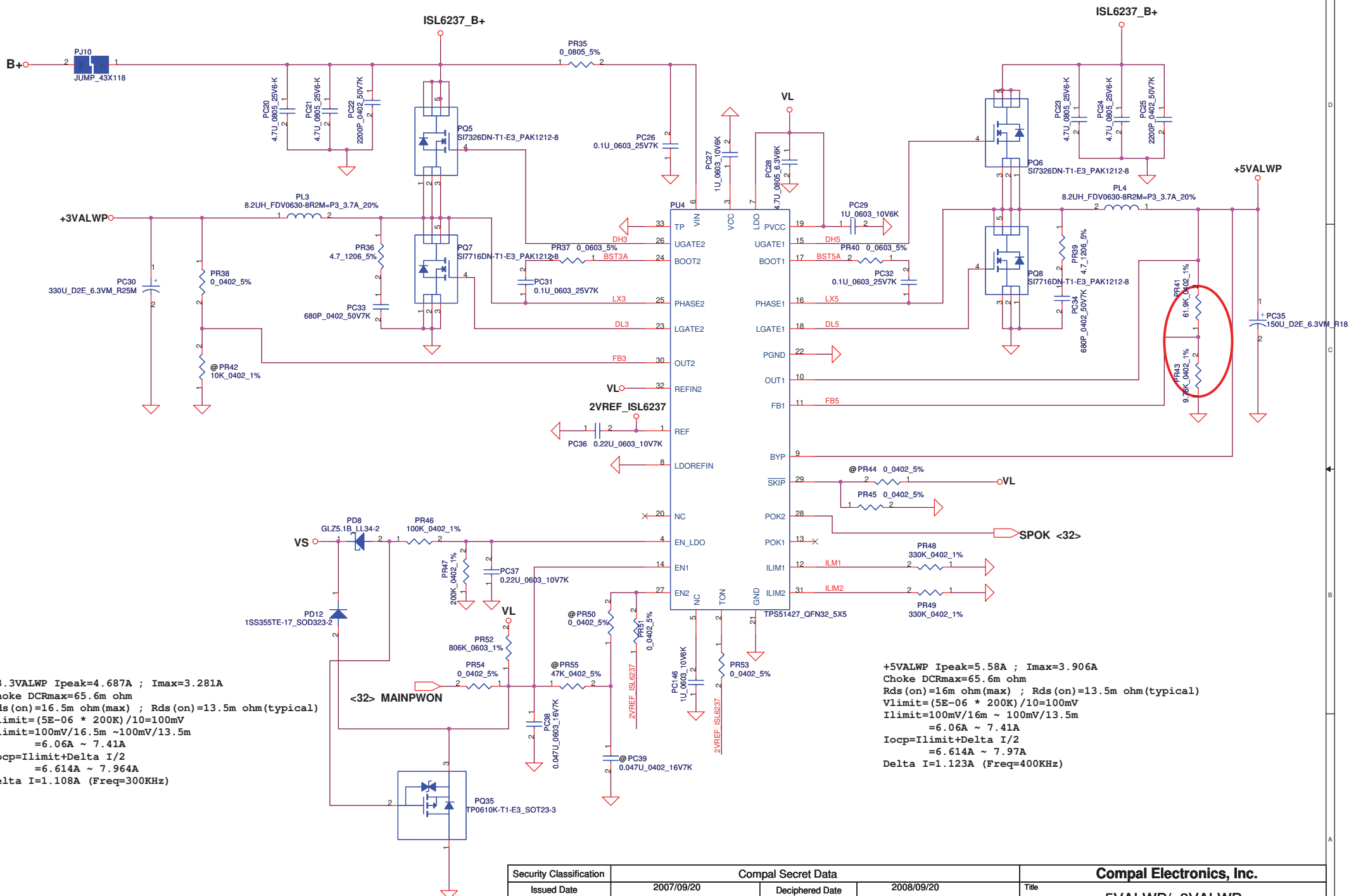
PH2 near main Battery CONN :

BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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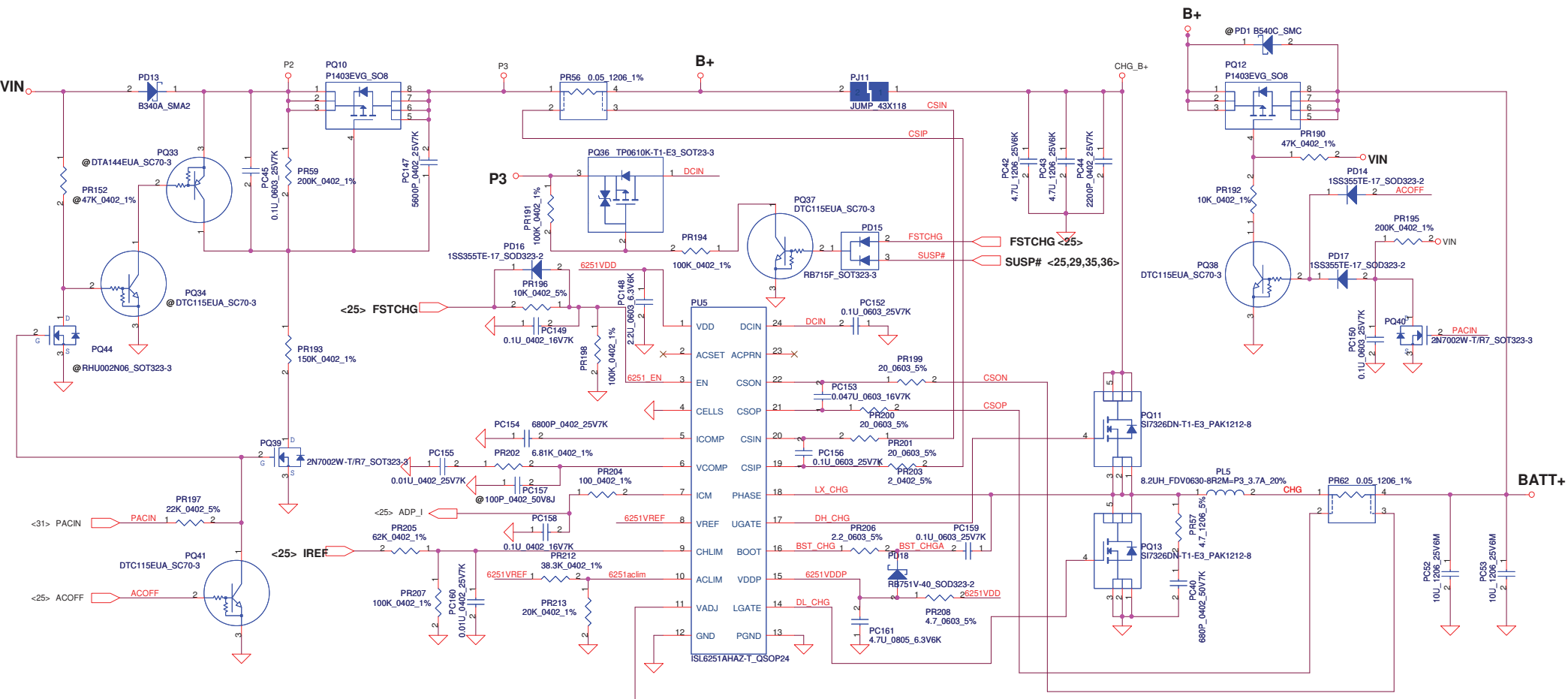


+3.3VALWP Ipeak=4.687A ; Imax=3.281A
 Choke DCRmax=65.6m ohm
 Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
 Vlimit=(5E-06 * 200K)/10=100mV
 Ilimit=100mV/16.5m ~100mV/13.5m
 =6.06A ~ 7.41A
 Iocp=Ilimit+Delta I/2
 =6.614A ~ 7.964A
 Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=5.58A ; Imax=3.906A
 Choke DCRmax=65.6m ohm
 Rds(on)=16m ohm(max) ; Rds(on)=13.5m ohm(typical)
 Vlimit=(5E-06 * 200K)/10=100mV
 Ilimit=100mV/16m ~ 100mV/13.5m
 =6.06A ~ 7.41A
 Iocp=Ilimit+Delta I/2
 =6.614A ~ 7.97A
 Delta I=1.123A (Freq=400KHz)

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				+5VALWP/+3VALWP	
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Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
 $V_{aclim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1/0.05) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 0.8199V$, $I_{input} = 1.343A$

CC=0.3~1.76A
 IREF=1.62*Icharge
 IREF=0.486V~2.85V
 3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

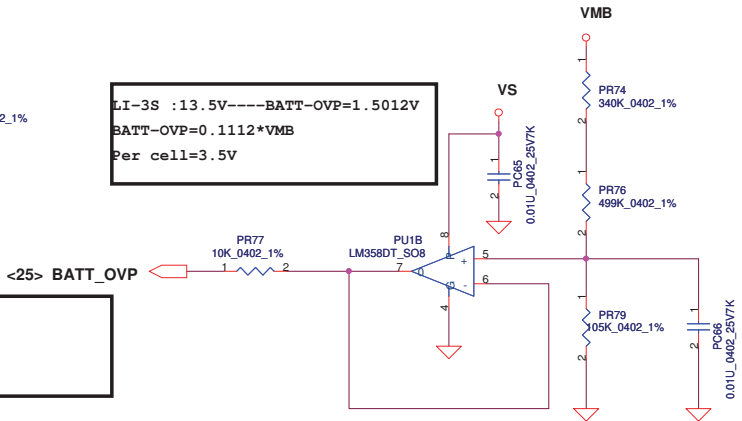
<25> CALIBRATE#

CALIBRATE#	Pre Cell
H	4.35V
L	3.99V

VADJ-->VREF-->4.41V
 VADJ-->Ground-->3.39V
 Vcell=(0.175*VADJ+3.99)

LI-3S :13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=3.5V

Charger ADJ	Calibrate#	PR211	PR220
4.2V	N/A	@	@
3.99V	L	301K	499K
4.35V	H	301K	499K

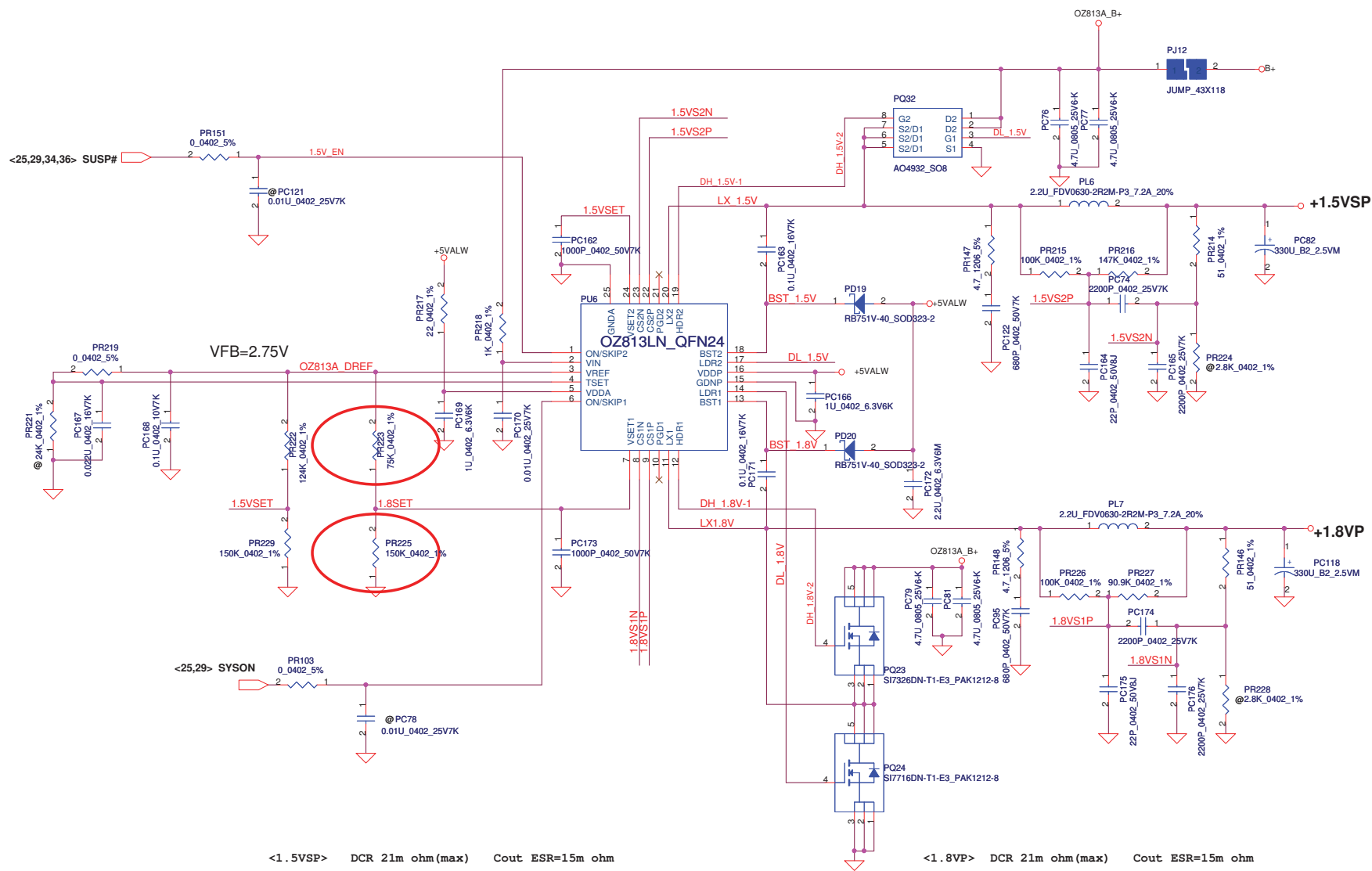


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CHARGER			
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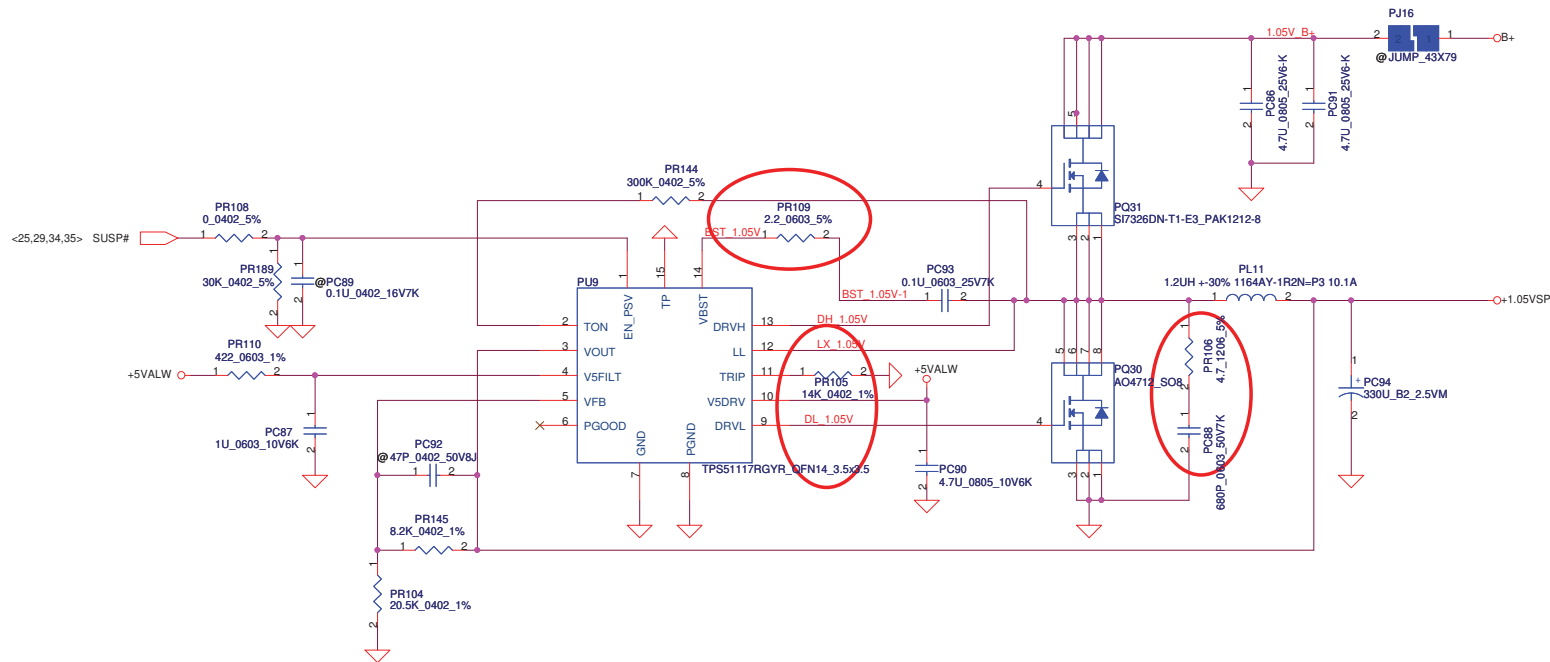
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				1.5VSP / 1.8VP	
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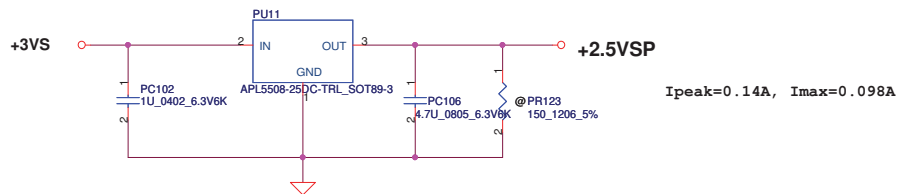
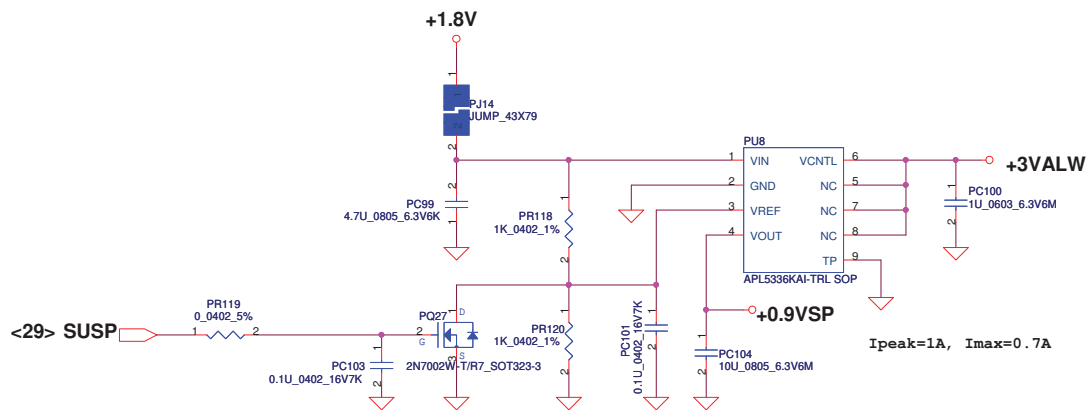


<Vo=1.05V> VFB=0.75V
 Vo=VFB*(1+PR145/PR104)=0.75*(1+8.2K/20.5K)=1.05V
 Fsw=261KHz

Cout ESR=15m ohm Rds(on)(max)=16.5m Rds(on)(typical)=13.5m
 Ipeak=7.09A, Imax=4.963A, Iocp=8.51A
 Delta I=((19-1.05)*(1.05/19))/(1.5u*261K)=2.53A
 =>1/2DeltaI=1.265A
 Vtrip=Rtrip*10uA=14K*10uA=0.14V
 Iocpmin=Vtrip/(Rds(on)(max)*1.2)+1.265
 =0.14/(0.0165*1.2)+1.265=8.34A
 Iocpmax=(0.14/(0.0135*1.2))+1.265=9.91A
 Iocp=8.34A~9.91A

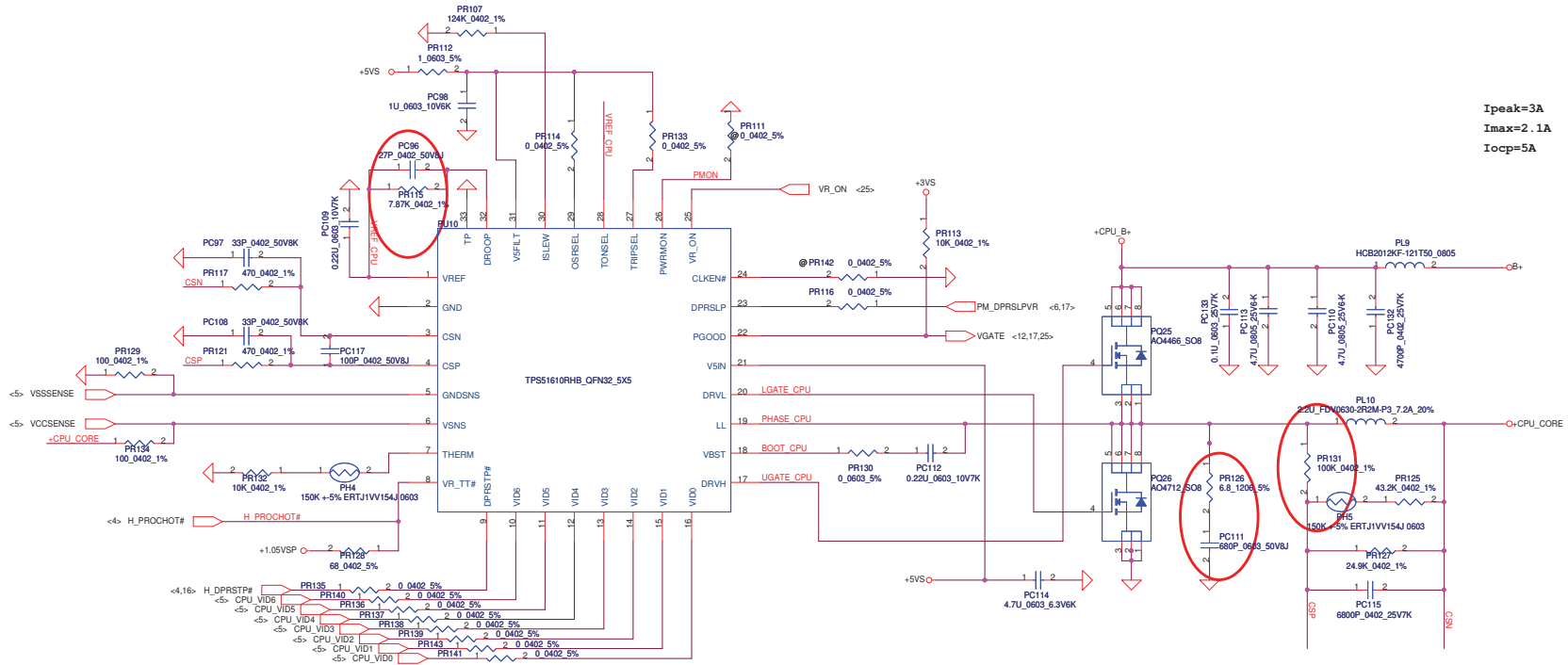
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I_{peak}=3A
 I_{max}=2.1A
 I_{ocp}=5A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify CPU_CORE VR_TT# circuit	circuit error	0.1	38	Change PR128 to SD028680A80 (S RES 1/16W 68 +-5% 0402)	08/10/27	DVT
2	Diode modify	BOM error	0.1	31	Change PD3 to SC4LZ4380T4 (S ZEN DIO RLZ4.3B (LL-34))	08/10/27	DVT
3	Diode modify	BOM error	0.1	31	Change PD4 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
4	Diode modify	BOM error	0.1	31	Change PD5 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
5	Diode modify	BOM error	0.1	32	Change PD6 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
6	Add 3/5V, charger, 1.8/1.5V snubber	For ESD solution	0.1	33	Add PR36 PR39 PR57 PR147 PR148 to SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC33 PC34 PC40 PC122 PC95 to SE074681K80 (S CER CAP 680P 50V K X7R 0402)	08/10/27	DVT
7	Add CPU snubber	For ESD solution	0.1	33	Add PR126 to SD011680B80 (S RES 1/4W 6.8 +-5% 1206) Add PC111 to SE024681J80 (S CER CAP 680P 50V J NPO 0603)	08/10/27	DVT
8	Add CPU_CORE input capacitance	For ESD solution	0.1	38	Add PC133 SE042104K80 (S CER CAP .1U 25V K X7R 0603) Add PC132 SE074222K80 (S CER CAP 2200P 50V K X7R 0402)	08/10/27	DVT
9	Add CPU_CORE input capacitance	For ESD solution	0.1	31	Add PC123 PC124 PC126 PC127 PC128 PC129 PC130 to SE076104K80 (S CER CAP .1U 16V K X7R 0402) Add PC125 to SE072104K80 (S CER CAP 0.1U 25V K Y5V 0402)	08/10/27	DVT
10	Modify 1.05V LMOS	cost down	0.1	31	change PQ30 to SB00000AJ00 (S TR AO4712 1N S08)	08/10/27	DVT
11	Modify 1.05V choke	cost down	0.1	31	change PL11 to SH00000FQ00 (S COIL 1.2UH +-30% 1164AY-1R2N=P3 10.1A)	08/10/27	DVT
12	Modify charger input capacitance size	BOM error	0.1	31	change PC42 PC43 to SE142475K80 (S CER CAP 4.7U 25V K X5R 1206 H1.6)	08/10/29	DVT
13	Modify charger VADJ circuit	circuit error					
14	Modify DIODE BOM (remove ROHN)	BOM error					
15	Modify ACIN circuit	EVT issue solution	0.1	31	change PR4 SD02800008 to SD034100380(100K)	08/11/13	DVT
16	Modify 3/5V circuit	Modify 5V voltage for HW request	0.1	33	change PR43 to SD034976180 (S RES 1/16W 9.76K +-1% 0402) add PR41 SD034619280 (S RES 1/16W 61.9K +-1% 0402)	08/12/26	PVT
17	Modify 1.8V circuit	Modify 1.8V voltage for HW request	0.1	35	change PR223 to SD034750280 (S RES 1/16W 75K +-1% 0402) change PR225 to SD034150380 (S RES 1/16W 150K +-1% 0402)	08/12/26	PVT
18	Modify 1.05V circuit	add snubber for SED 3G solution	0.1	36	add PC88 SE025681K80 (S CER CAP 680P 50V K X7R 0603) add PR106 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	08/12/26	PVT
19	Modify 1.05V circuit	add boost for 1.05v issue	0.1	36	change PR109 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	08/12/26	PVT
20							
21							
22							
23							

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A-TEST Change

- <8/25>
- 1. Update Power SCH
- <8/26>
- 1. Update Power SCH
- 2. Change
D7 SC300000D00 to SC300000000
- 3. Change
C49、C50 SE071180K80 to SE071180J80
- <8/27>
- 1. Updata Power SCH
- 2. Modify
RJ45 temp footprint FOX_JM3611A-R4122-7F_12P-T
- <8/28>
- 1. Updata Power SCH
- <9/1>
- 1. Updata Screw
- <9/5>
- 1. SWAP USB20_1 Signal.
- <9/10>
- 1. Remove Mini card pin55、pin56 的GND。
- 2. Change JREAD1.42、H26 to GNDA。
- <9/12>
- 1. Swap 3G ESD pin neme。
- <9/15>
- 1. Update Audio Jack footprint
- 2. Chcnge R641、R642 300ohm to 511ohm for Arthros。
- 3. Update L footprint。
- <9/16>
- 1. Update POWER SCH.
- <9/17>
- 1. Update POWER SCH.
- 2. ADD R380、R383 for ESD.
- <9/18>
- 1. Update ATHEROS 10/100 LAN <AR8132/AR8114>
- <9/24>
- 1. Change C870 0.1u to 1u.
- <9/26>
- 1. R88 change to 0ohm.

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Pre PVT-TEST Change

- <10/21>
- 1. Remove C389 for Audio can't detect issue on page 16
- 2. Add KS01/KSO2 PU +3VALW on page25
- 3. Add R205 for schematic mistake on page 04
- 4. Change EC RST to PLTRST on page 25
- 5. Add J8 to cost down Audio LDO on page 20
- 6. Add R72 to reserve +3VALW for 3G on page 19
- 7. Reserve C238 for CRTDAC on page 10
- 8. Add R87 for Debug card on page 19
- 9. Change C108/C255 to 0.1uF for random hang issue
- 10. Change JP3 pin assignment on page 28
- <10/21>
- 1. Update Power SCH
- <10/29>
- 1. Audio AMP 10dB update to 6dB
- <11/3>
- 1. Update Power SCH
- <11/4>
- 1. Change R373、R374 to 56.2 ohm for DA-HP FSOV
- 2. Add C834、C851 for 3G noise
- 3. Change KB926 C1 to D2
- 4. Card reader RT5158E change to RT5159-GR
- <11/5>
- 1. Swap D7 pin define
- <11/10>
- 1. EC add R79、R90、R92 for SMS wakeup。

PVT-TEST Change

- <11/28>
- 1. Reserve C40、C46、C47、C233
- 2. R617 change to 0ohm for RTS5159
- 3. R68 200K change to 100K for sequence
- 4. Remove C47
- 5. Add D30 for LVDS
- 6. Add C55 0.1U
- 7. U2 Change to SA000017B00
-because RT9715 Can't protect
- <12/30>
- 1. Update power MP SCH

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