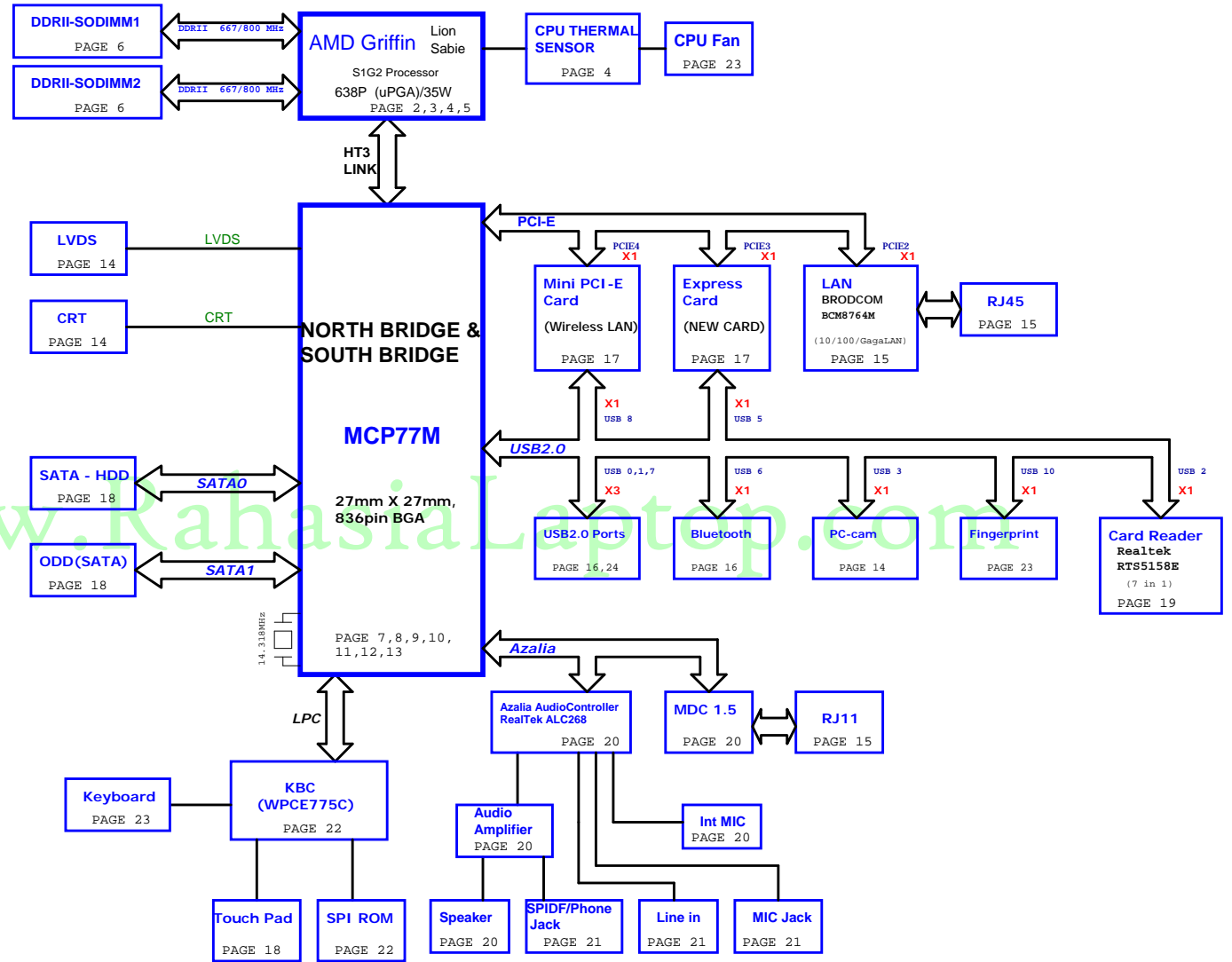


# Z05 SYSTEM BLOCK DIAGRAM



- CPU CORE / VDDNB (ISL6265A) PAGE 26
- NB\_CORE +1.1V (RT8202) PAGE 28
- +1.1V\_NB (RT8202) PAGE 27
- DDR II SMDDR\_VTERM 1.8VSUS(TPSS51116REG) PAGE 29
- SYSTEM POWER (ISL6237) PAGE 25
- SYSTEM CHARGER (ISL6251A) PAGE 24



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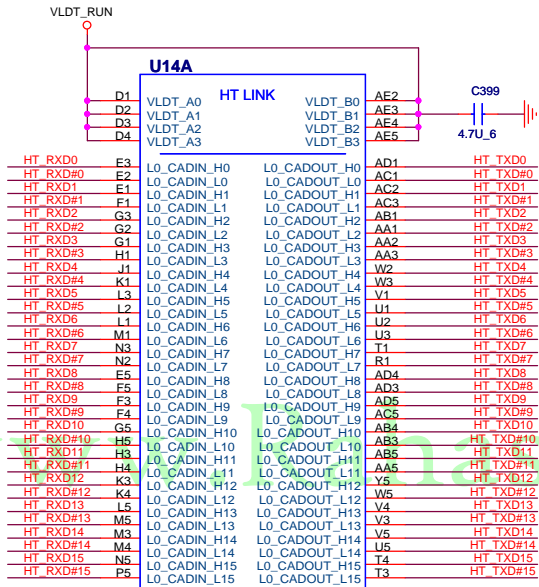
## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

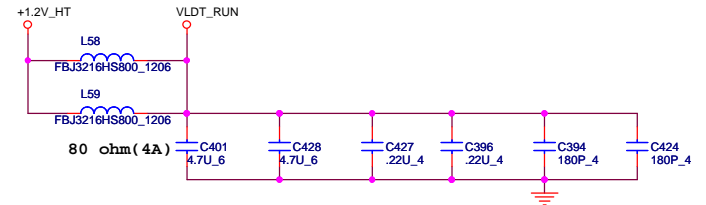


### PROCESSOR HYPERTRANSPORT INTERFACE

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

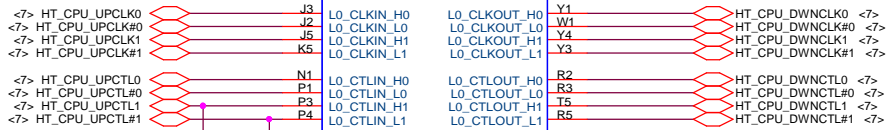


Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



### LAYOUT: Place bypass cap on topside of board

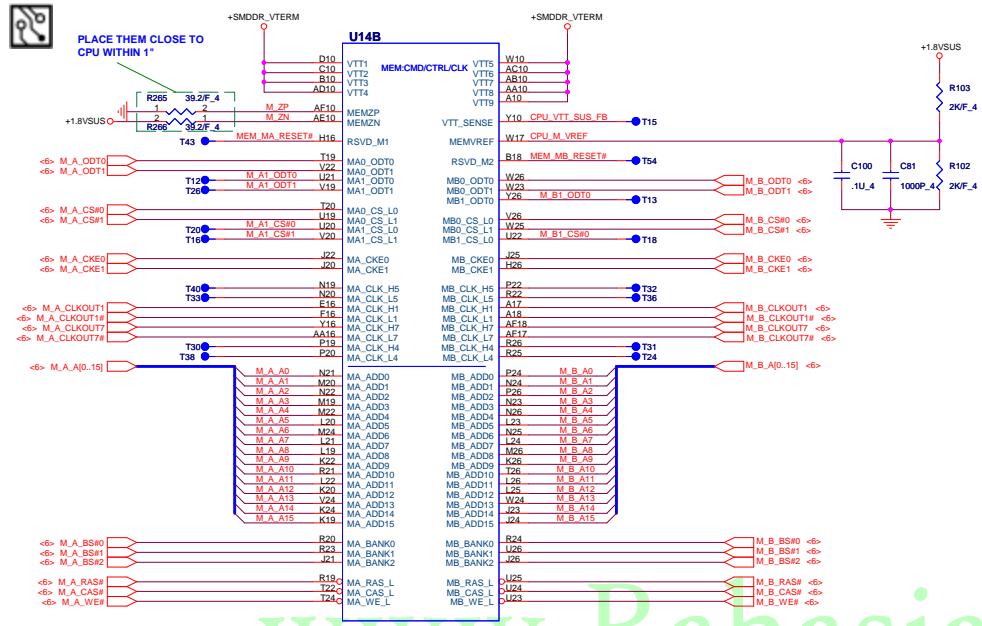
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS. PLACE CLOSE TO VLDT0 POWER PINS



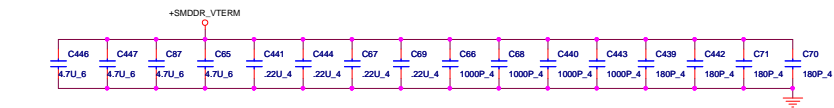
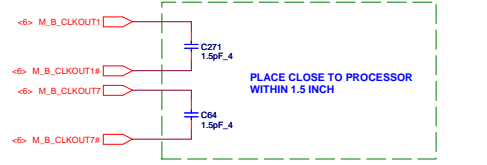
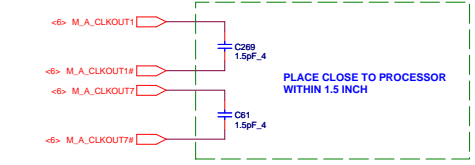
**Quanta Computer Inc.**  
PROJECT : Z05

Size	Document Number	Rev
	<b>AMD Griffin HT I/F</b>	1A
Date:	Mondsy, February 25, 2008	Sheet 2 of 34

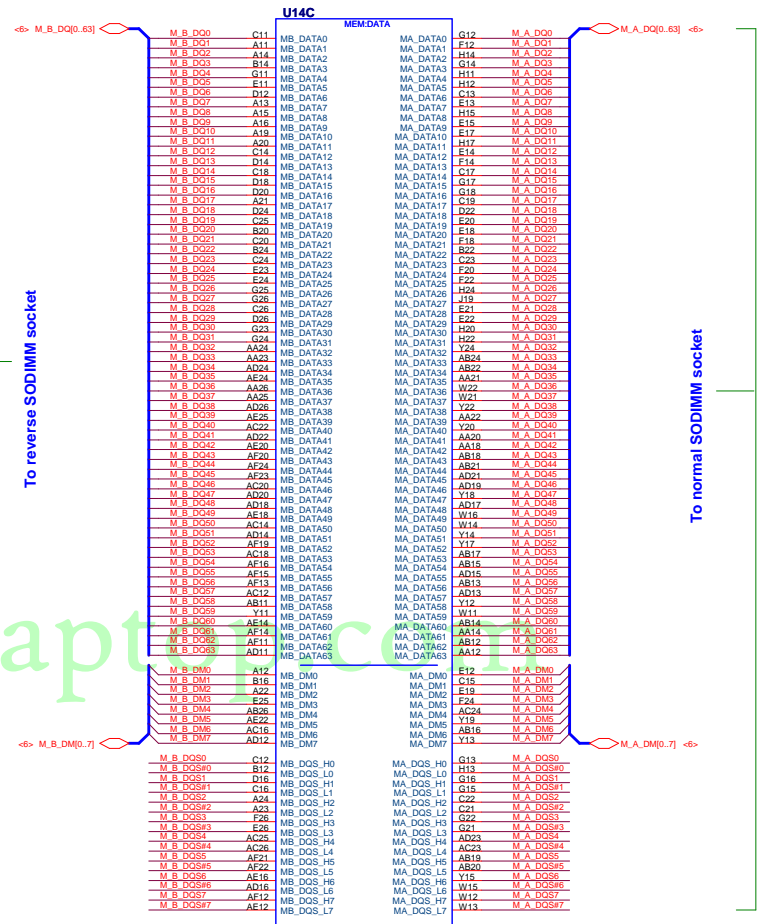
VDD\_VTT\_SUS\_CPU IS CONNECTED TO THE VDD\_VTT\_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1g2 SOCKET\_638\_PIN  
Athlon 64 S1g2 Processor Socket  
SOCKET\_638\_PIN



### Processor DDR2 Memory Interface



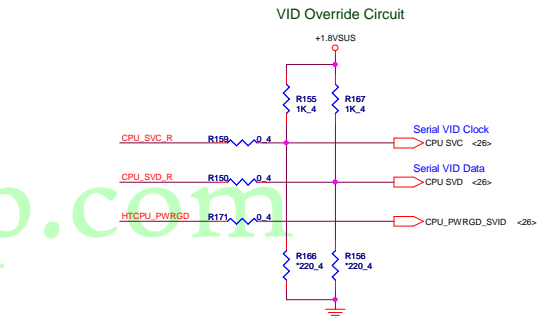
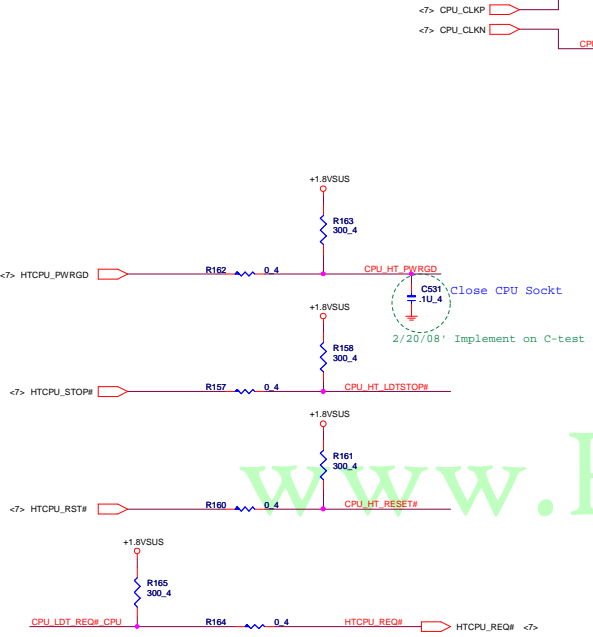
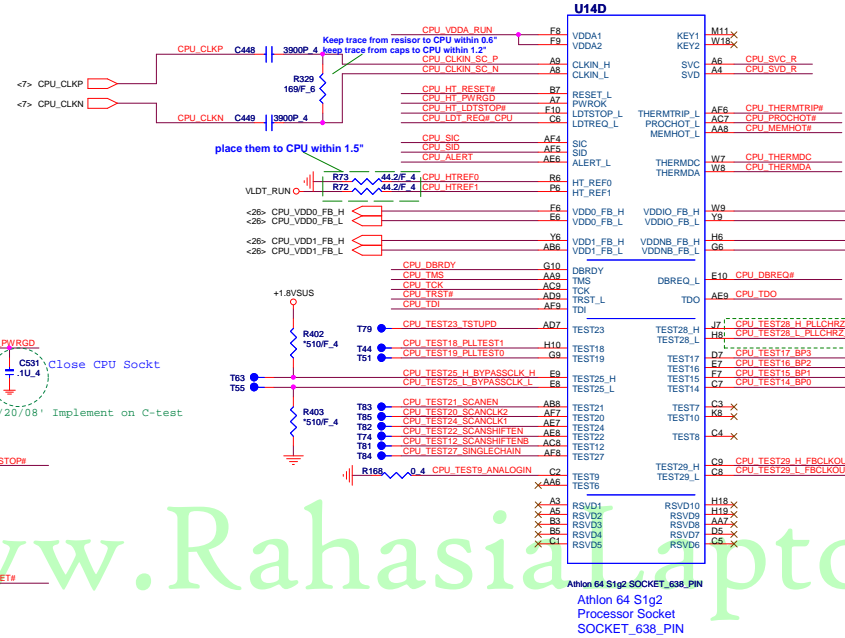
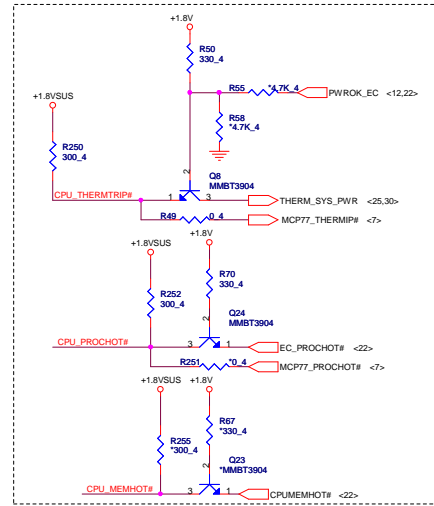
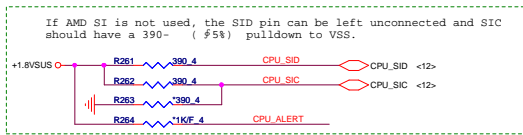
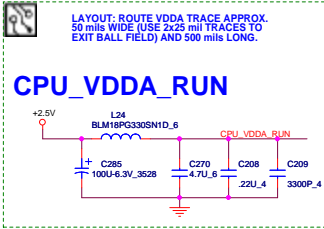
To reverse SODIMM socket

To normal SODIMM socket



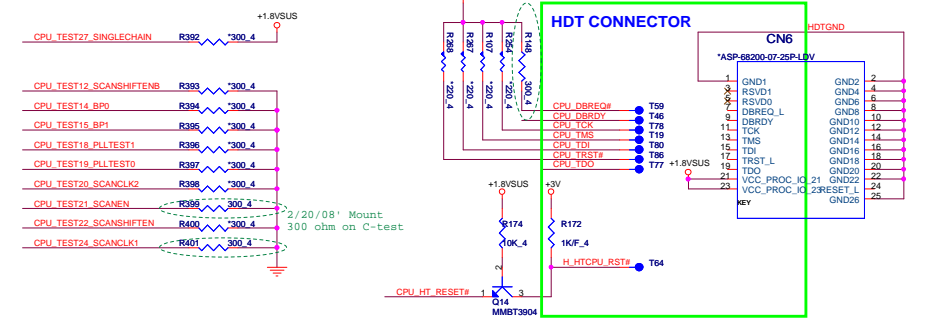
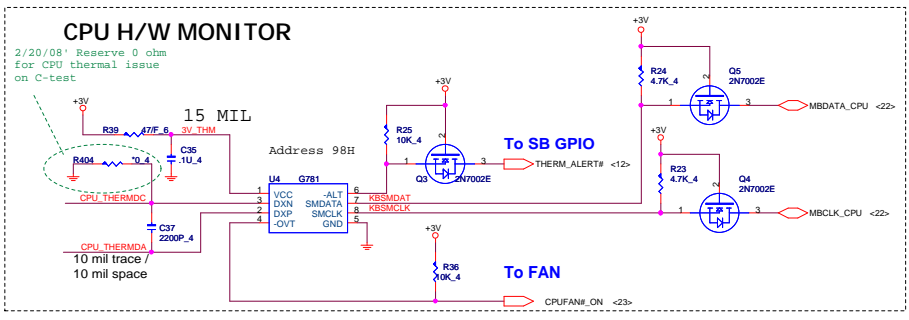
Athlon 64 S1g2 SOCKET\_638\_PIN  
Athlon 64 S1g2 Processor Socket  
SOCKET\_638\_PIN

# ATHLON Control and Debug

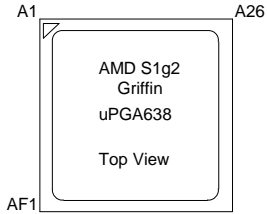
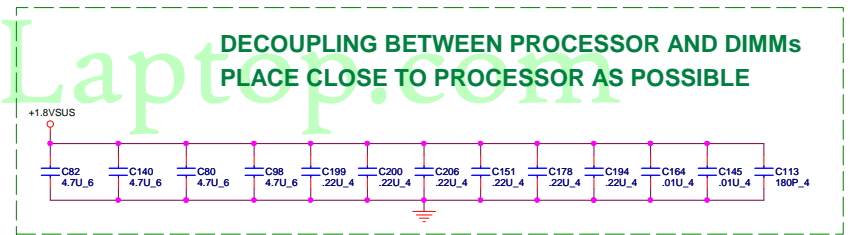
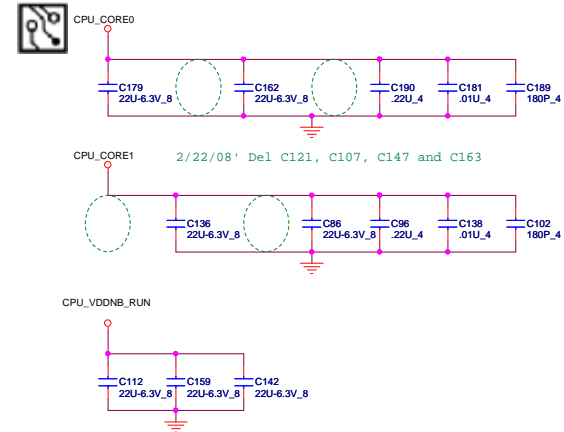
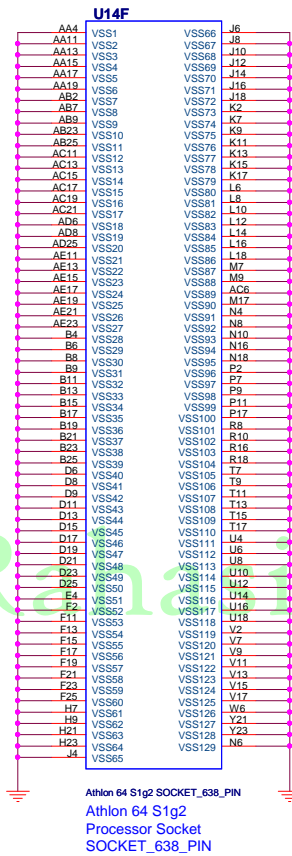
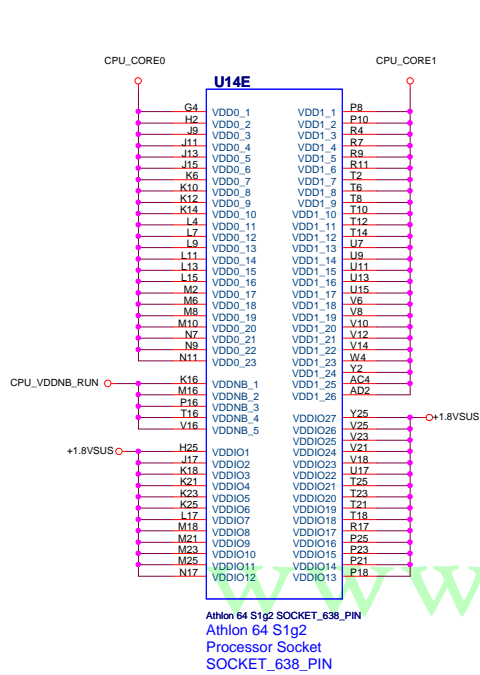


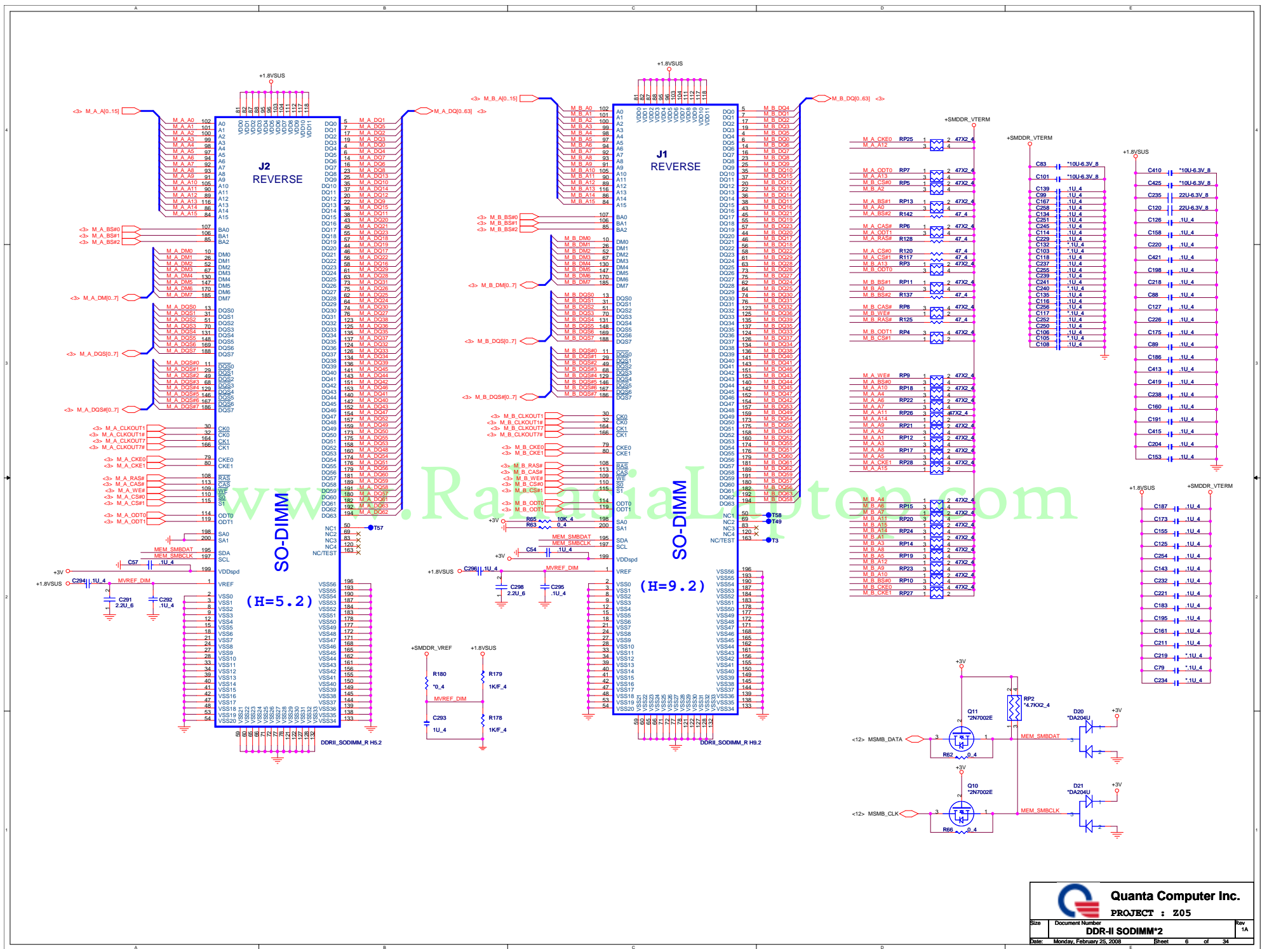
VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



# PROCESSOR POWER AND GROUND





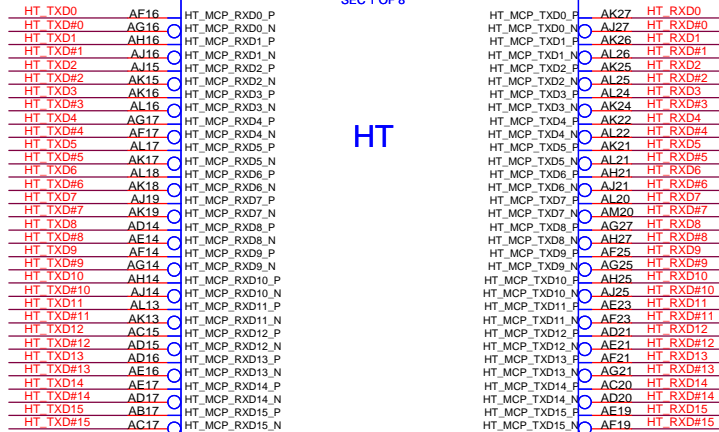
<2> HT\_TXD[15..0] <2>  
 <2> HT\_TXD#[15..0]

HT\_RXD[15..0] <2>  
 HT\_RXD#[15..0] <2>

**U15A**  
 FCBGA836-NVIDIA-MCP67 AJMCP770T02

SEC 1 OF 8

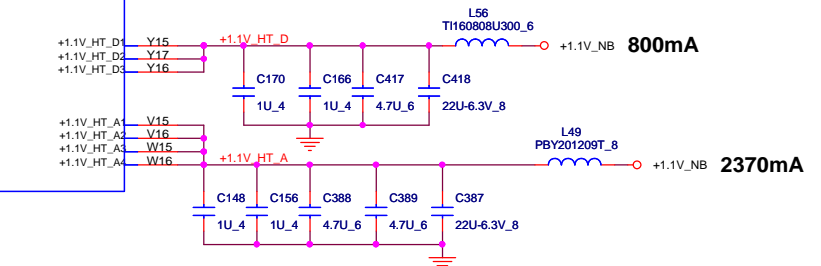
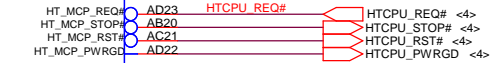
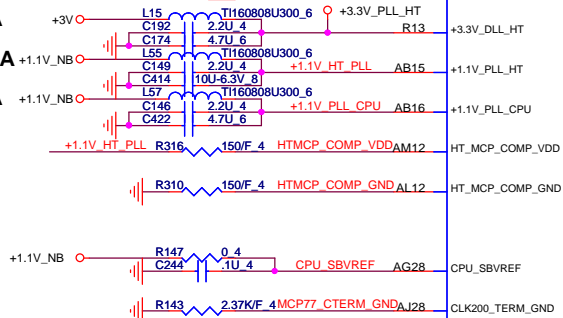
HT



**70mA**

**128mA**

**17mA**



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 PROJECT : Z05

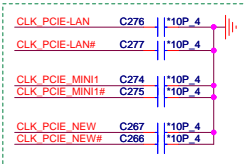
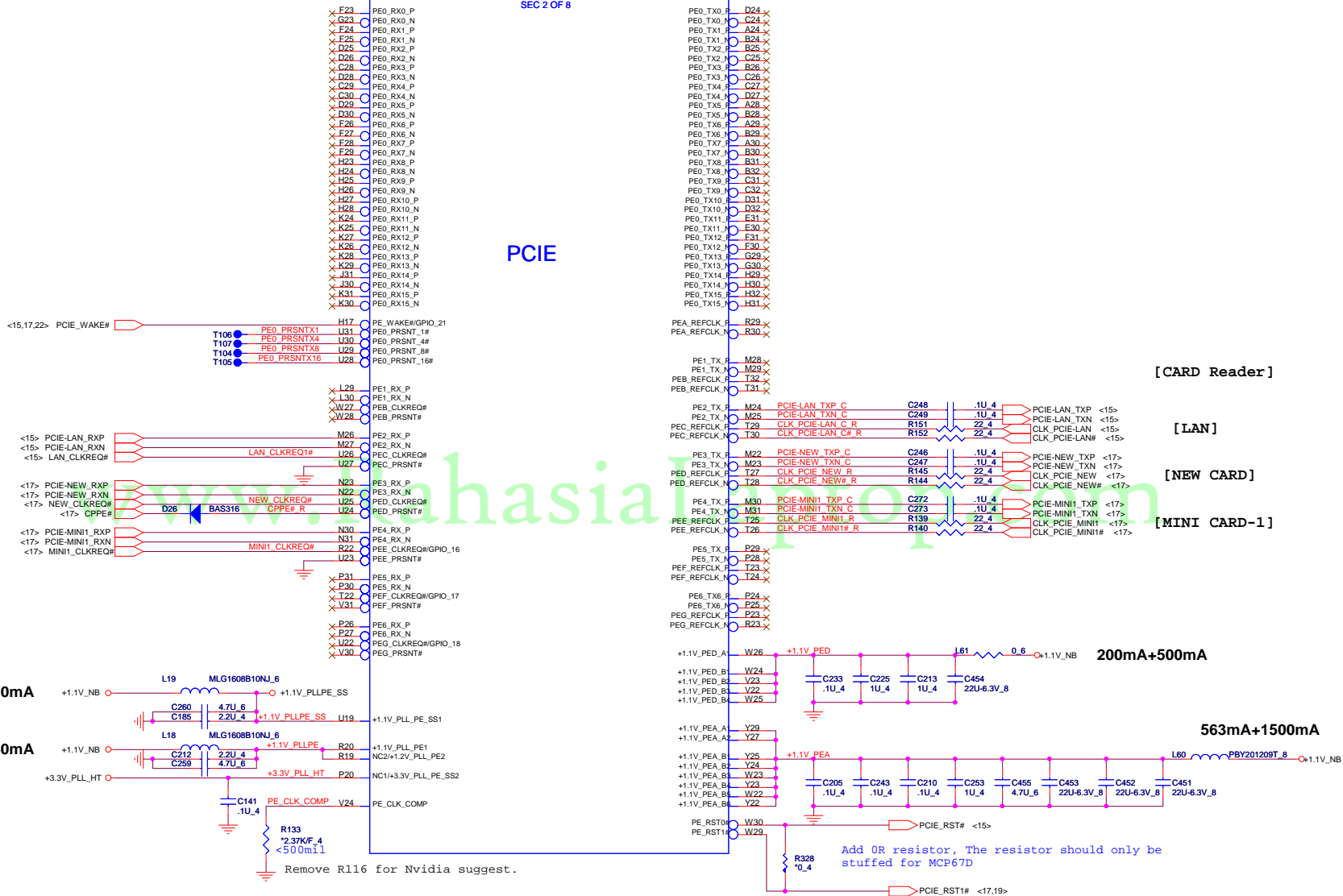
Size	Document Number	Rev
	<b>MCP77 HyperTransport Bus</b>	1A
Date:	Monday, March 10, 2008	Sheet 7 of 34



**U15B**  
FCBG836-NVIDIA-MCP67

SEC 2 OF 8

**PCIE**





U15D

FCBG836-NVIDIA-MCP67

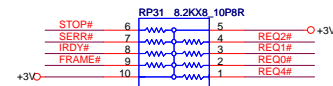
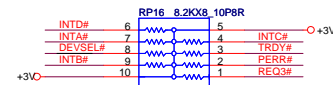
MCP77  
SEC 4 OF 8

PCI

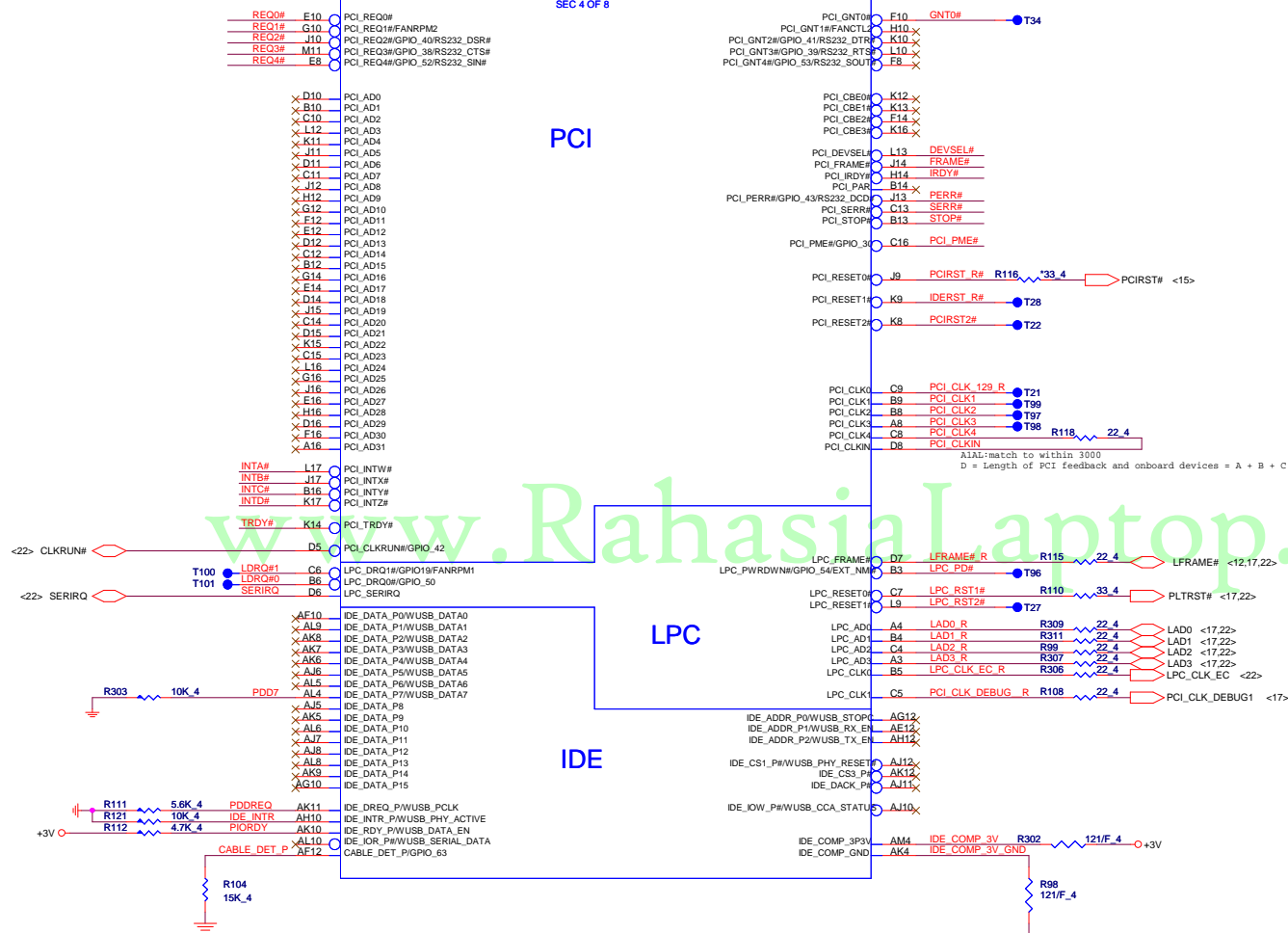
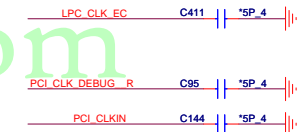
LPC

IDE

PCI/LPC PULL-UP



CLOCK BYPASS



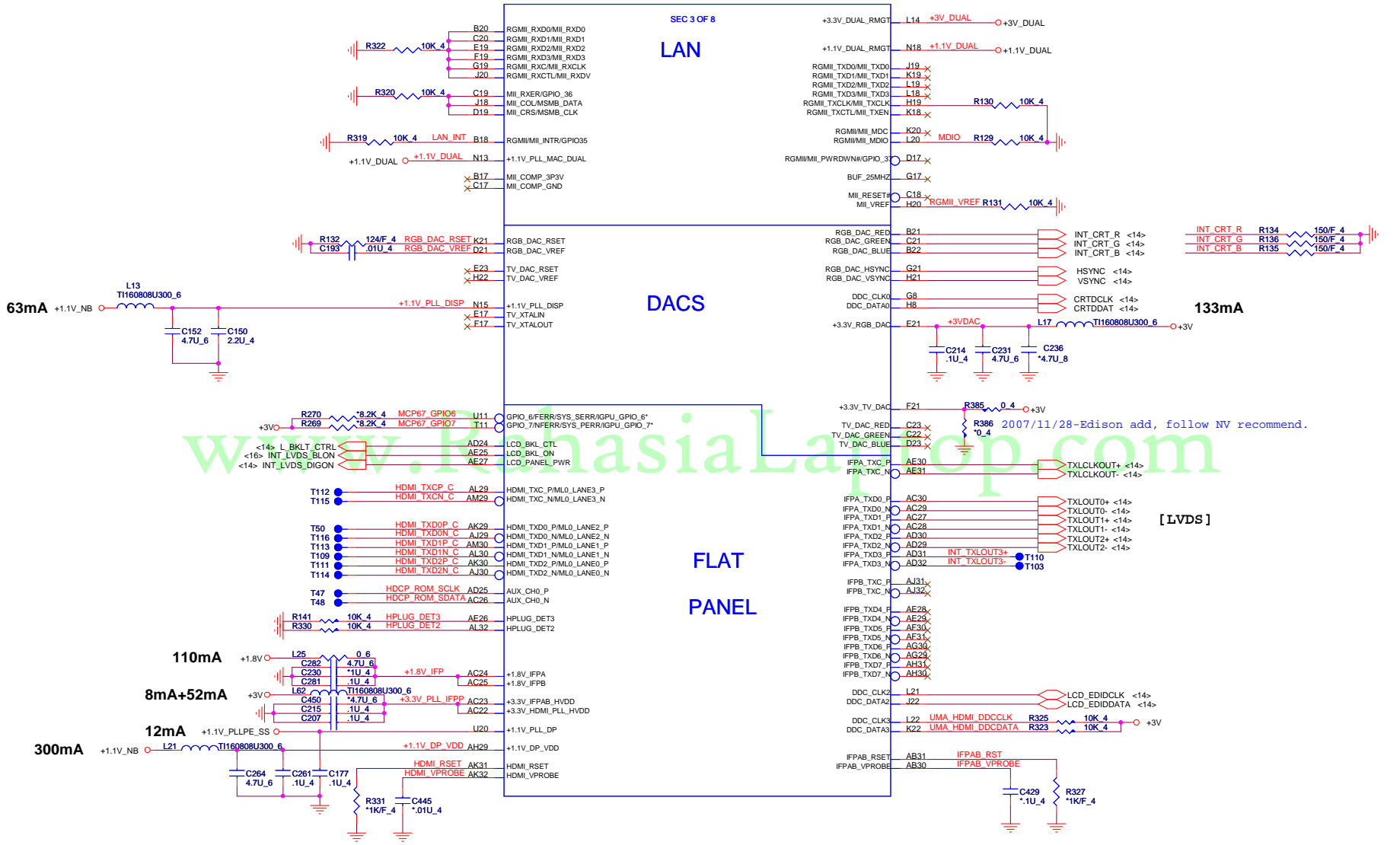
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**U15C**  
FCBGA836-NVIDIA-MCP67

**LAN**

**DACS**

**FLAT PANEL**

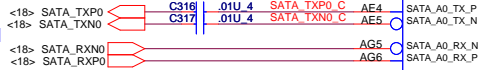


U15E  
FCBG836-NVIDIA-MCP67

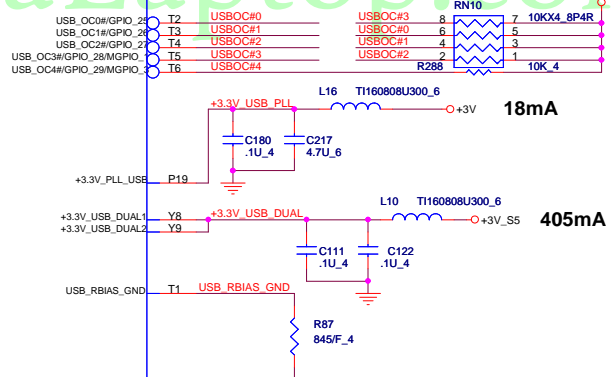
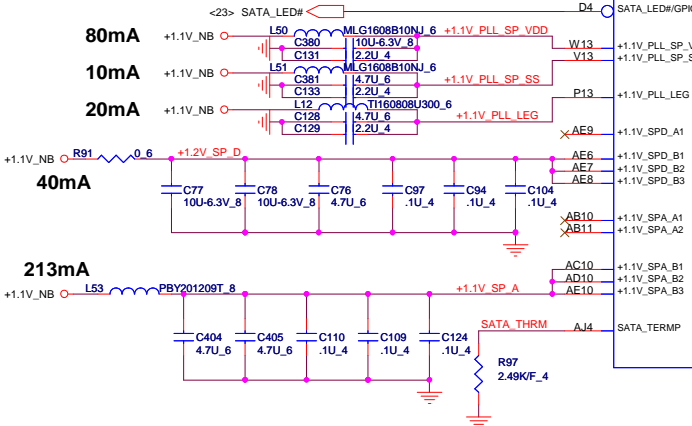
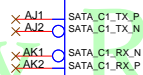
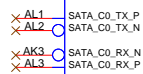
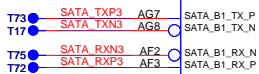
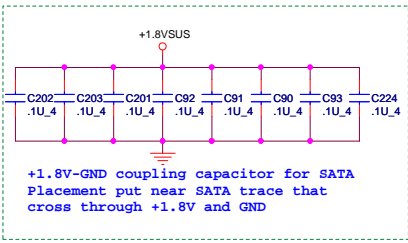
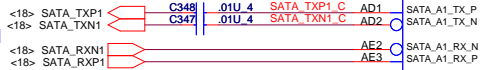
SEC 5 OF 8

SATA USB

[SATA HDD]



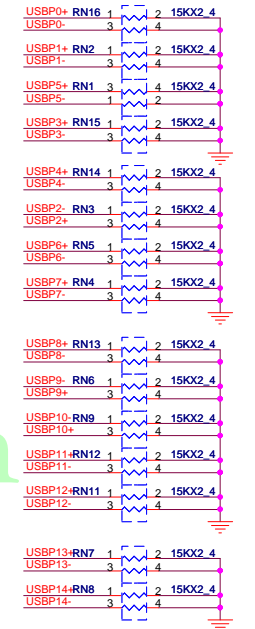
[SATA ODD]



2007/11/29: Pagell the resistor R87 from 909ohm change to 845ohm(follow NV suggest)

- INT LEFT USB-1
- INT LEFT USB-2
- Card Reader
- CCD
- NEW CARD
- BLUETOOTH
- EXT USB(PJ2)
- MINI CARD-1
- Fingerprint

USB PULL-DOWN



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 PROJECT : Z05

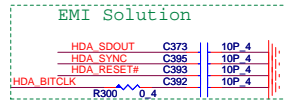
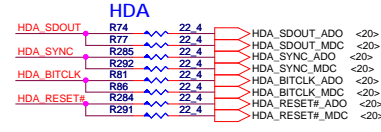
Size	Document Number	Rev
	<b>MCF77 SATA and USB</b>	1A
Date:	Sunday, March 09, 2008	Sheet 11 of 34

**U15F**  
FCBGA836-NVIDIA-MCP67

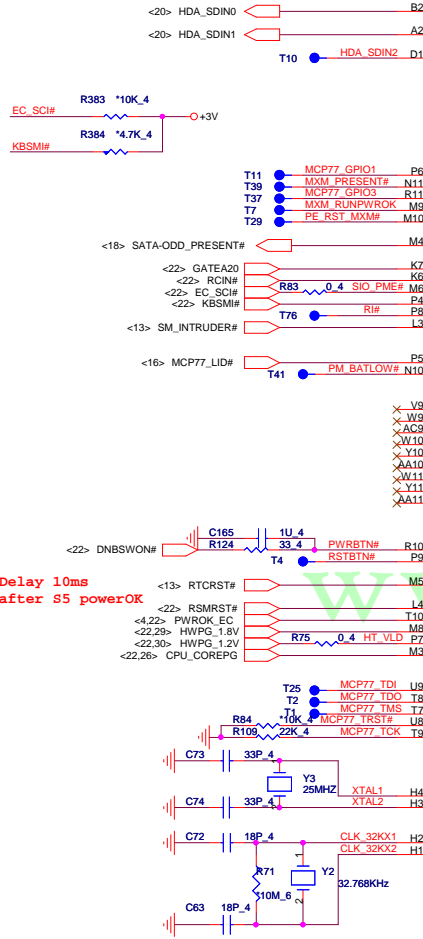
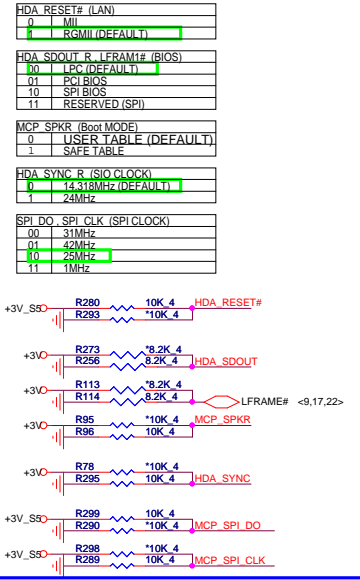
**SEC 6 of 8**

**HDA**

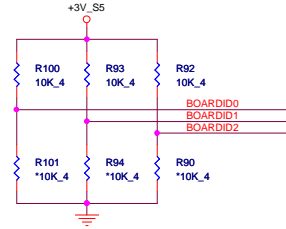
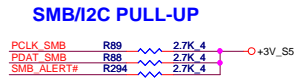
**MISC**



**MCP77 STRAPPING**



Delay 10ms after S5 powerOK

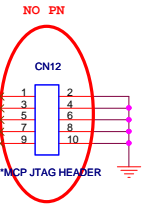
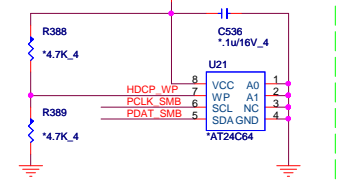


**M/B ID for 14"/17"**

ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	14" Dual Core CPU & MXM
1	1	0	14" Dual Core CPU & UMA
1	1	1	14" Single Core CPU & UMA

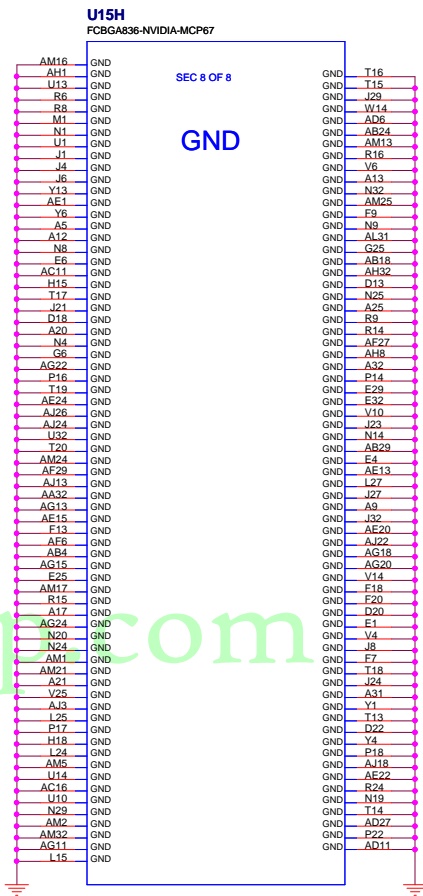
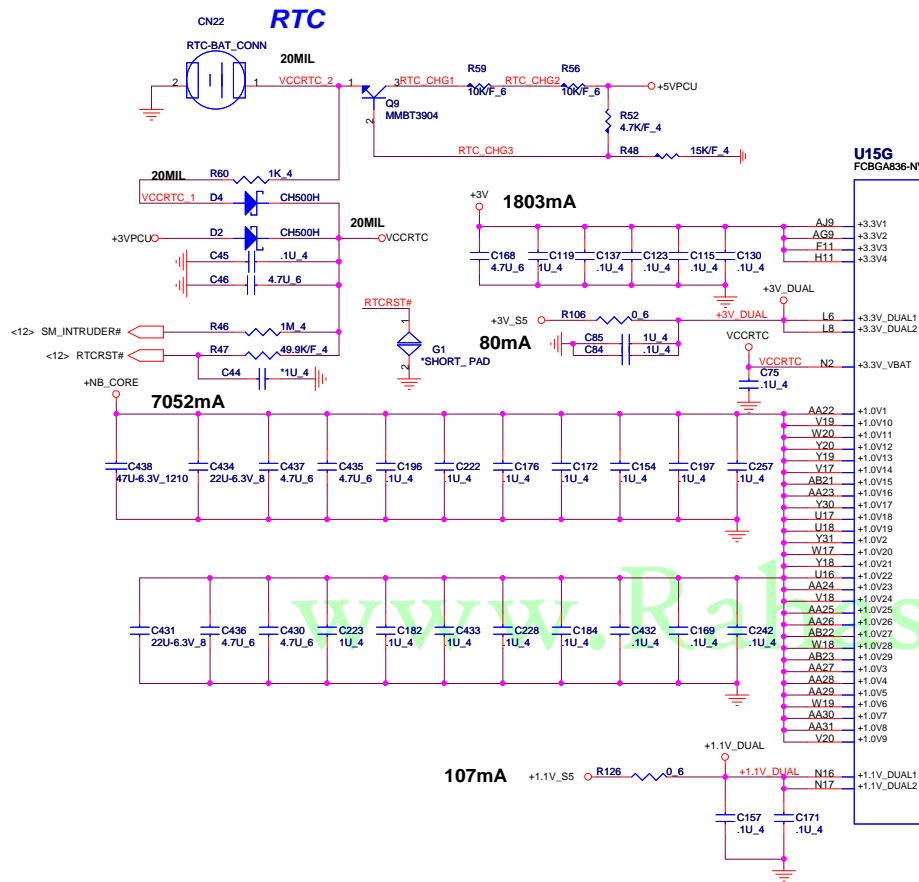
**Acer Suggest Reserve HDCP EEPROM 2007/12/05**

**HDCP EEPROM**



2007/11/28-Edison: Removethese part  
R315, R317, R326, R324, C423, Q28, Q29

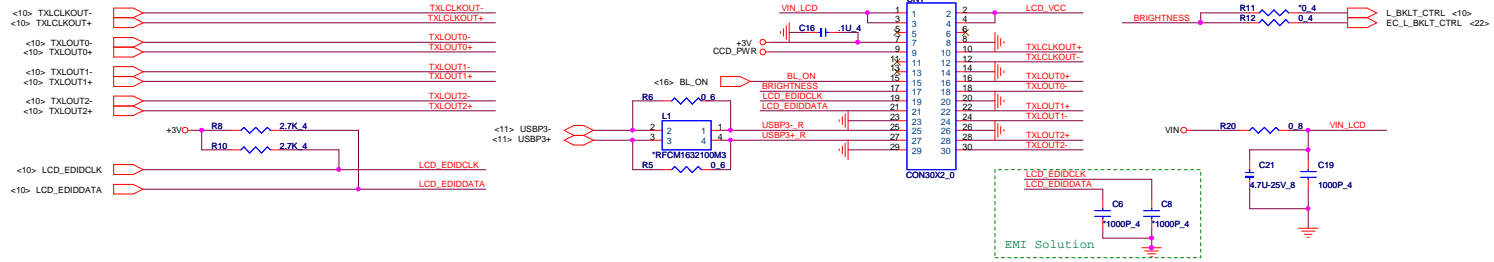
# MCP77 POWER PLANE/GND & BYPASS



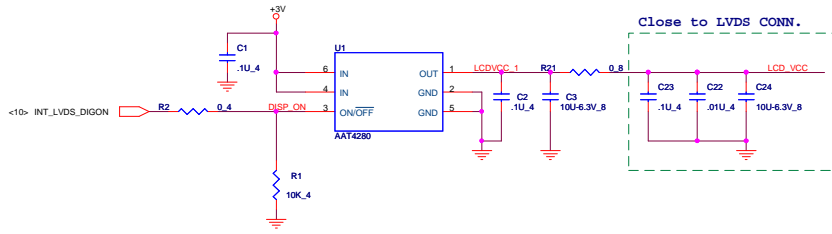
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# LVDS

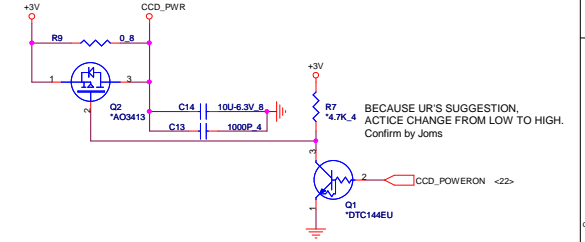
SINGLE\_CH



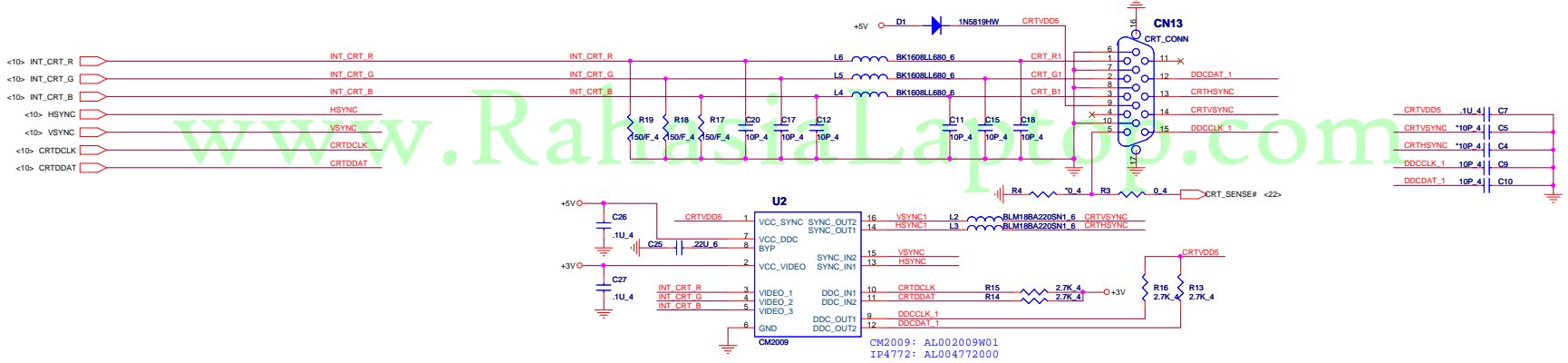
# LCD POWER



# CAMERA MODULE POWER



# CRT

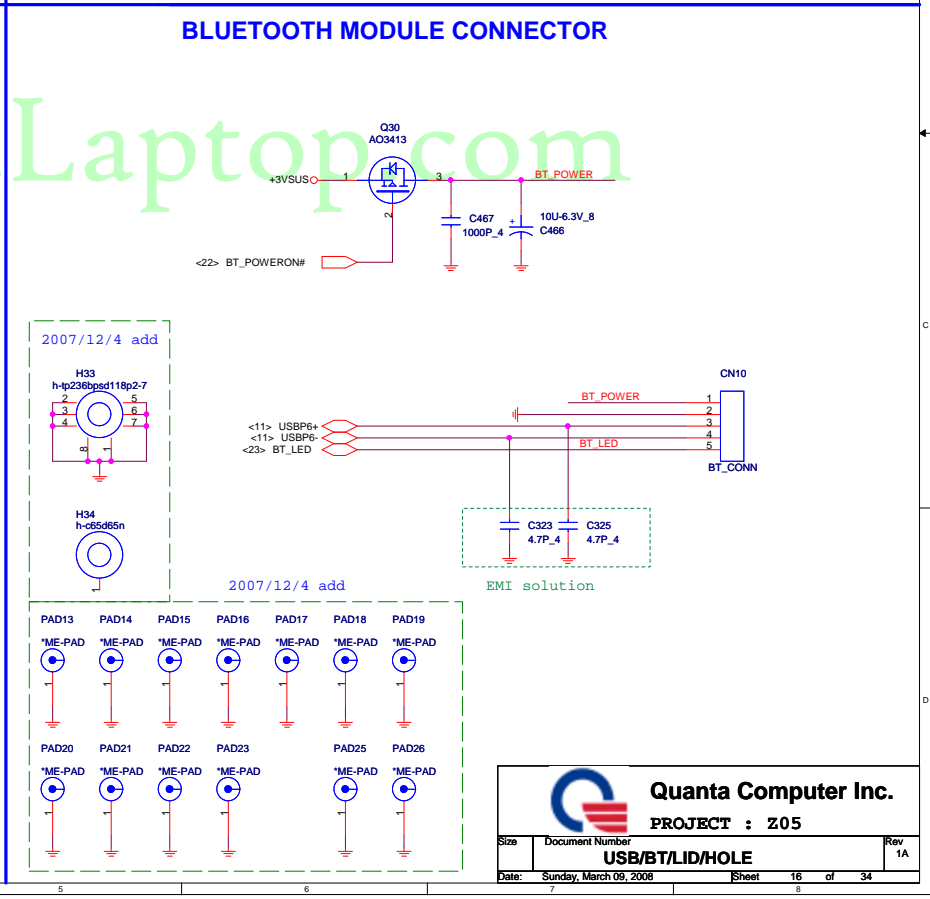
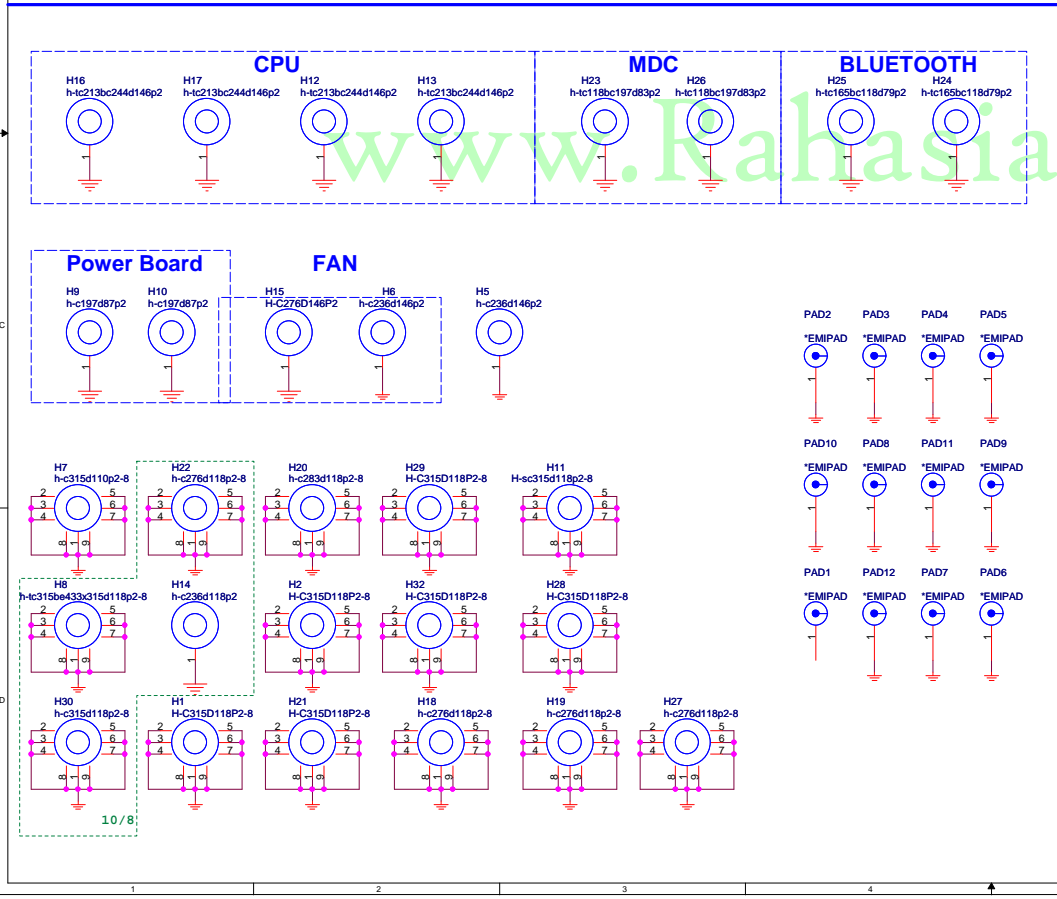
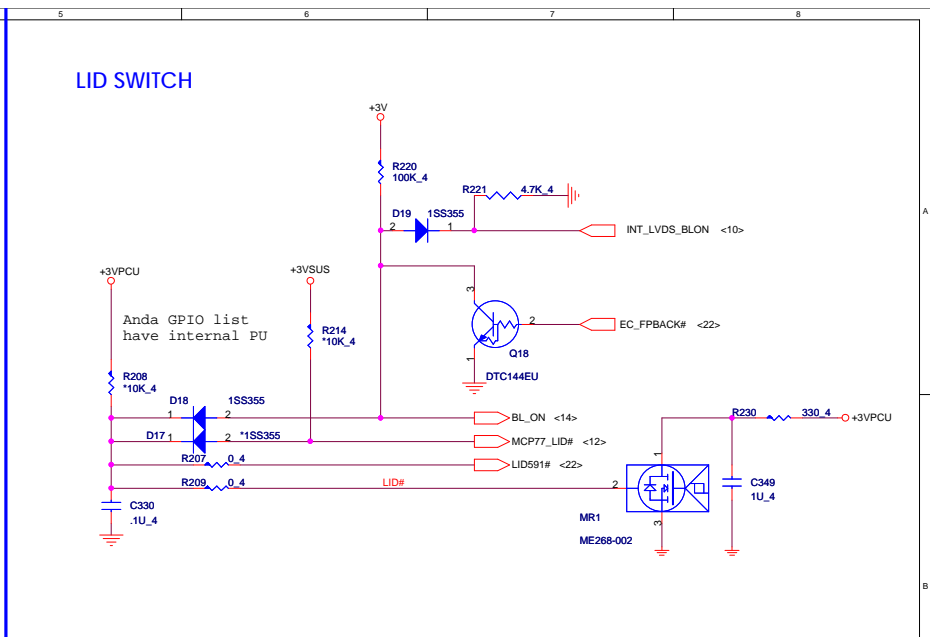
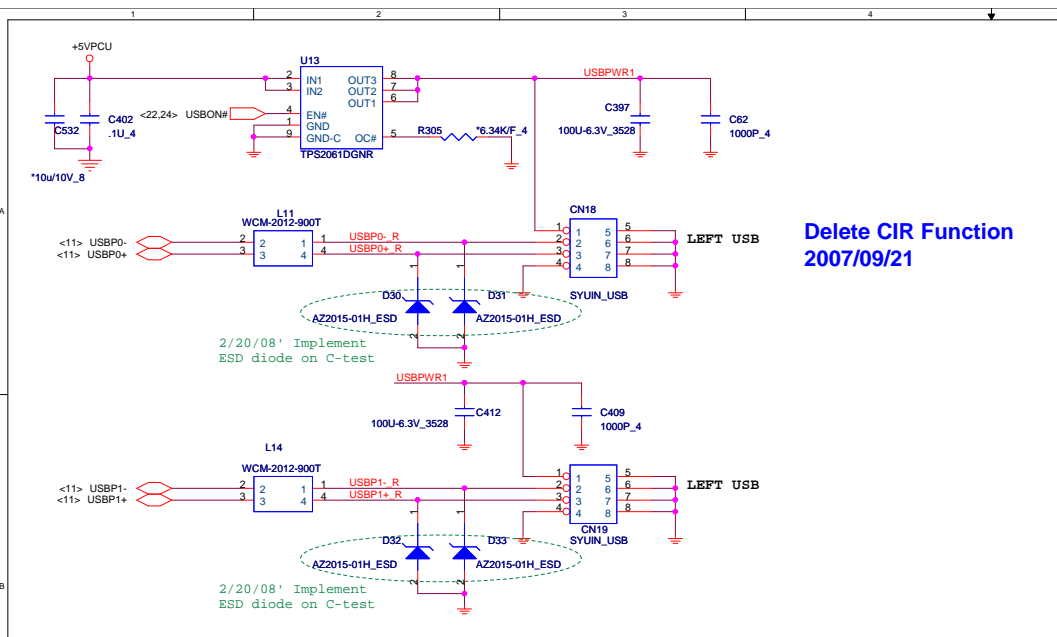


# TV Out (SVHS) MiniDIN 7-pin

Delete TVOUT MiniDIN

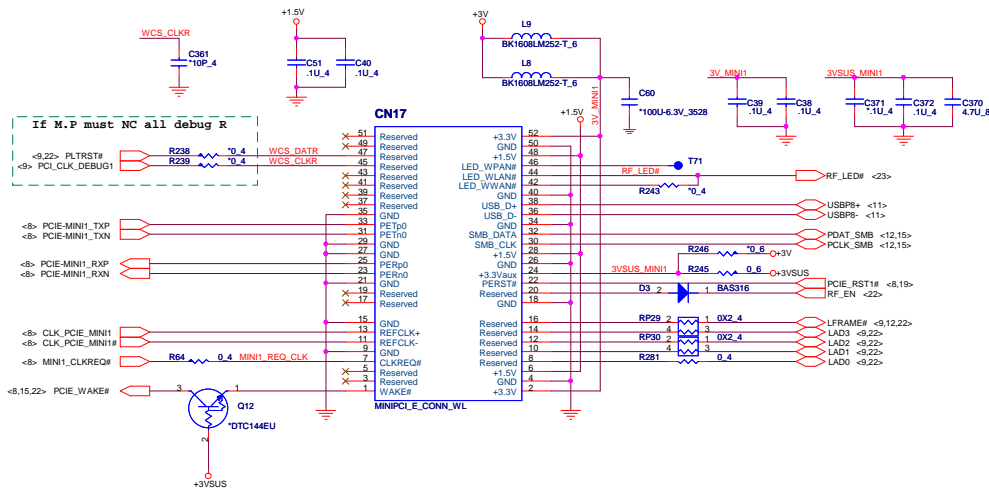






# MINI-Card

## MINI-Card Port-1

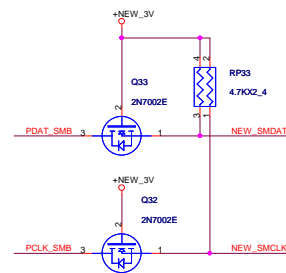
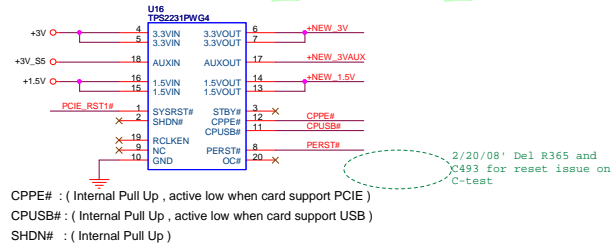
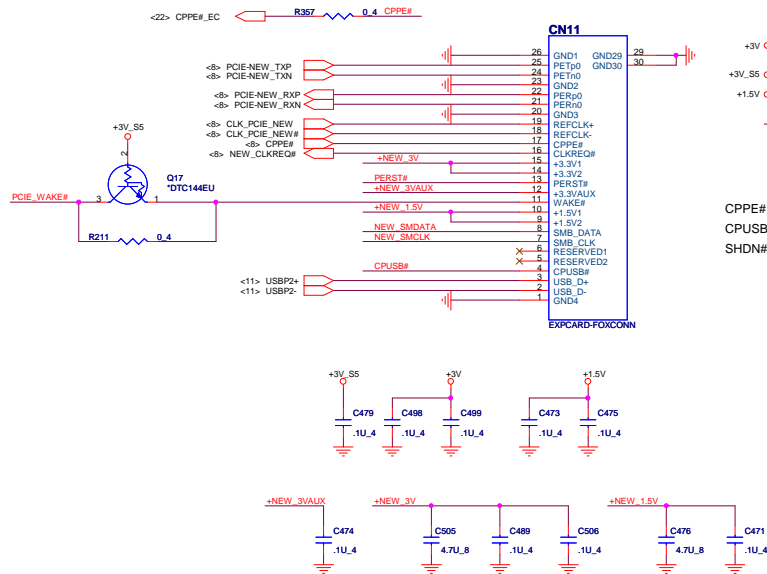


Delete MINI-Card Port-2

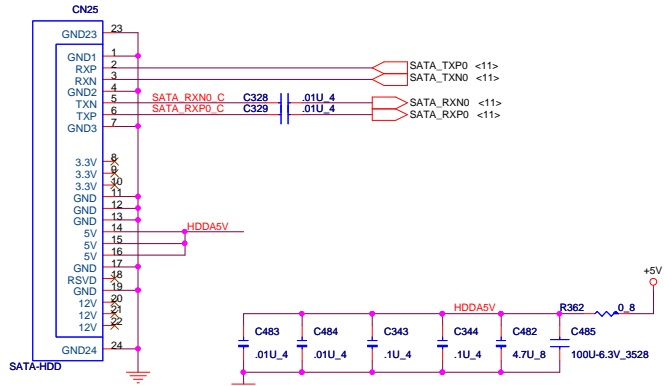
## New card

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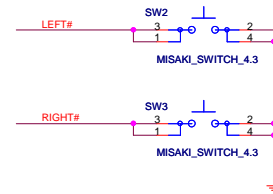
NEW CARD'S POWER SWITCH



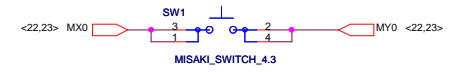
### SATA HDD



### TP SWITCH

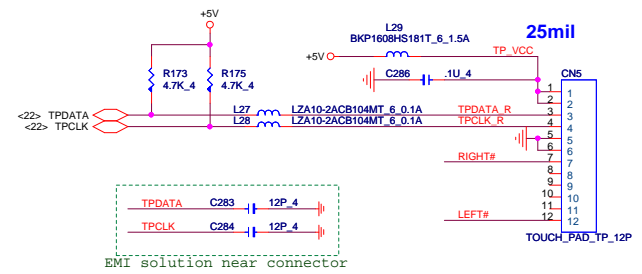


### E-KEY



MX0 MY0:E-Key

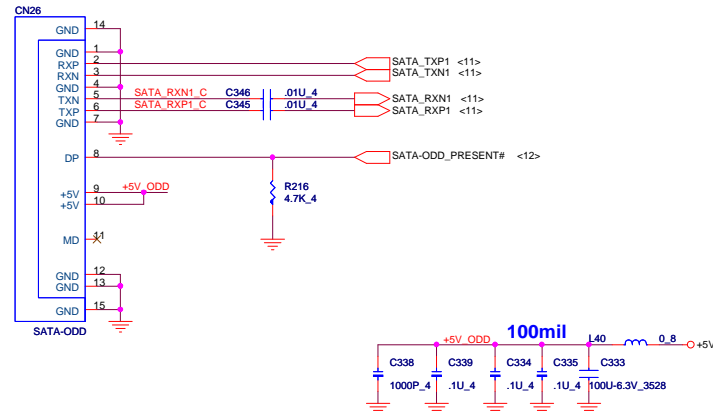
### TP CONN

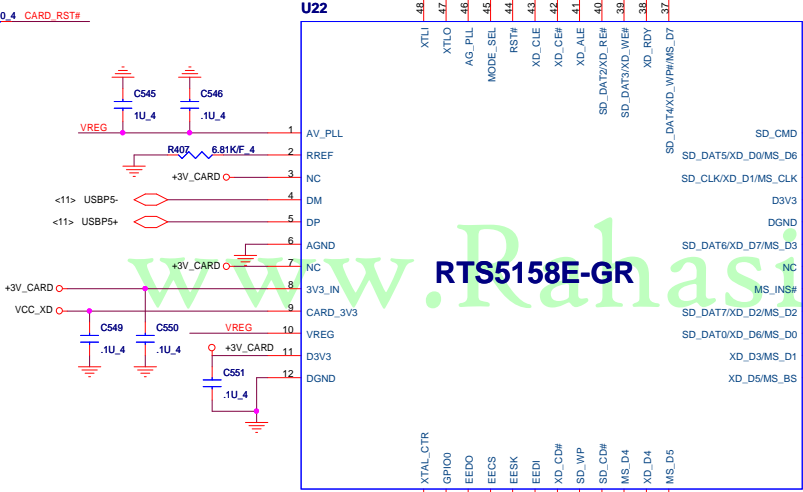
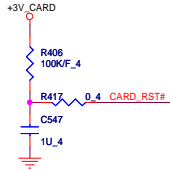
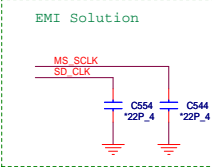
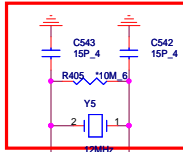
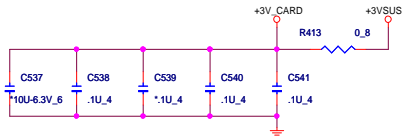


EMI solution near connector

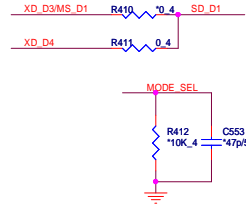
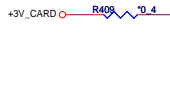
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### ODD (SATA)



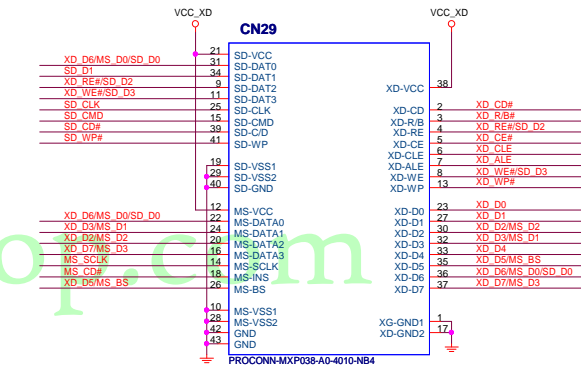
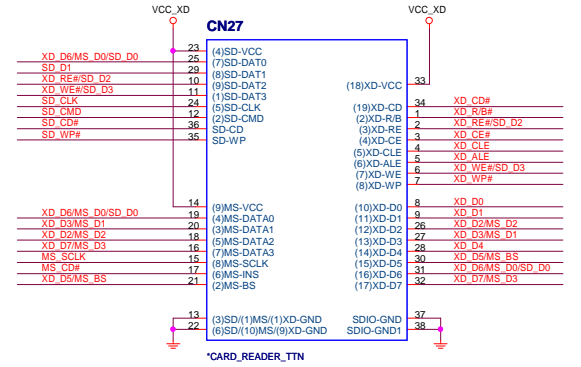


RTS5158E-GR

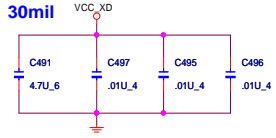


R412/C553 = 10K/47pF => R410 Reside  
R412/C553 = NC / NC => R411 Reside

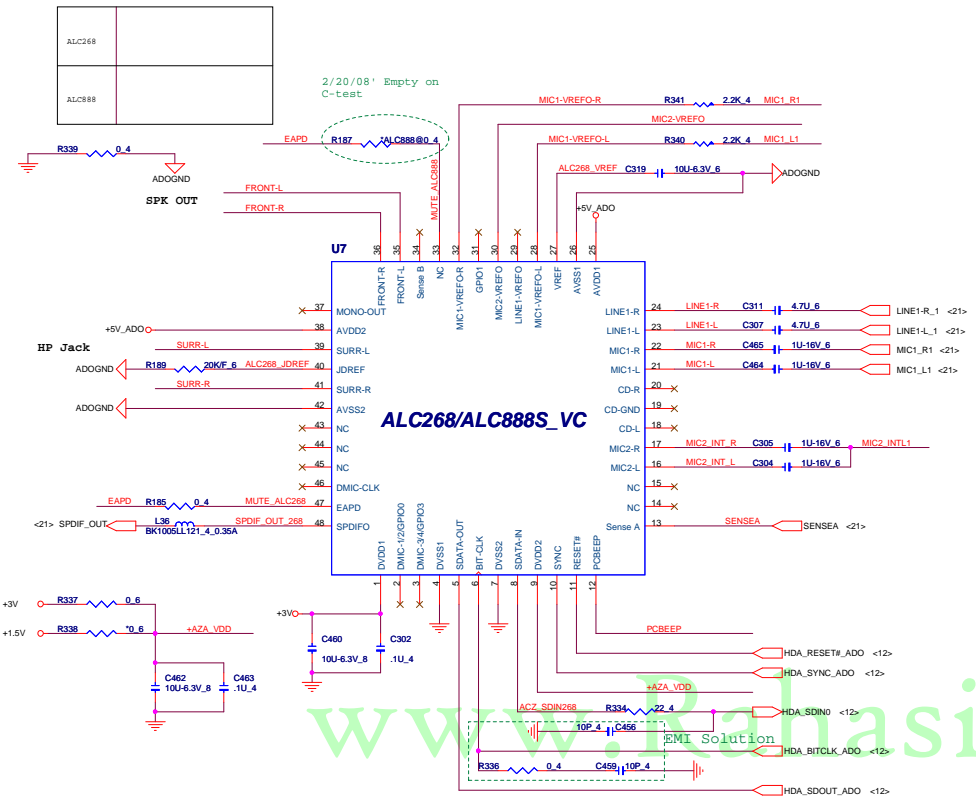
## 7 IN 1 CARD READER



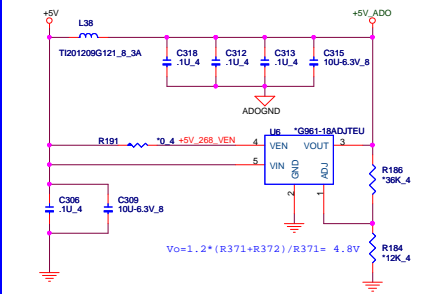
## CARDREADER POWER



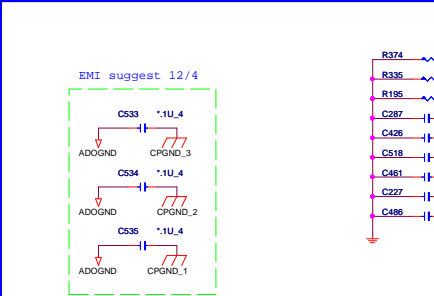
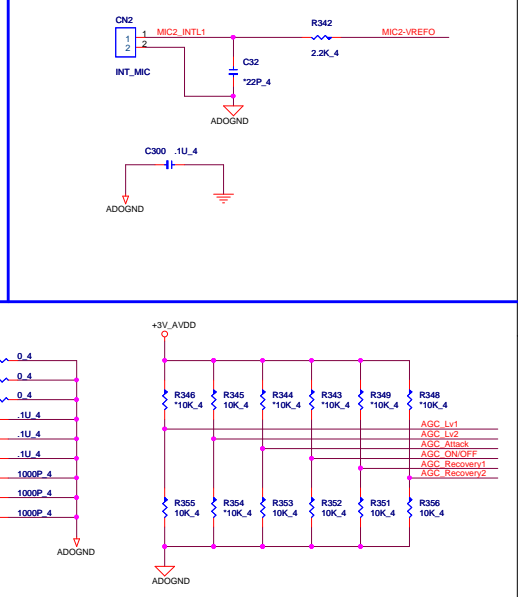
### CODEC (ALC268/ALC888S-VC)



### CODEC (ALC268) Power



### INT MIC array



**AGC-attack-time selection**

AGC_Attack (4 pin)	Attack time
LOW	1 ms
HI	2 ms

**AGC ON/OFF selection**

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
HI	OFF

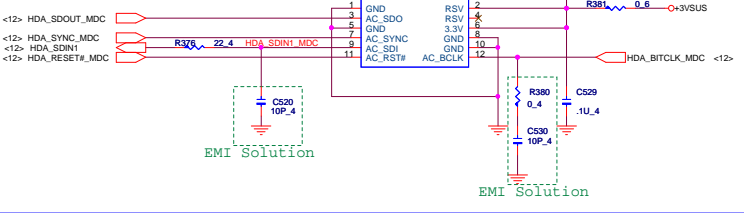
**AGC-recovery-time selection**

AGC_Recovery1 (10 pin)	AGC_Recovery2 (11 pin)	Recovery time
LOW	LOW	1.0 s
LOW	HI	2.0 s
HI	LOW	4.0 s
HI	HI	8.0 s

**AGC-on-level selection**

AGC_Lv1 (2 pin)	AGC_Lv2 (3 pin)	AGC_ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	HI	9.8 dBV	1.0 W
HI	LOW	8.1 dBV	0.9 W
HI	HI	6.0 dBV	0.5 W

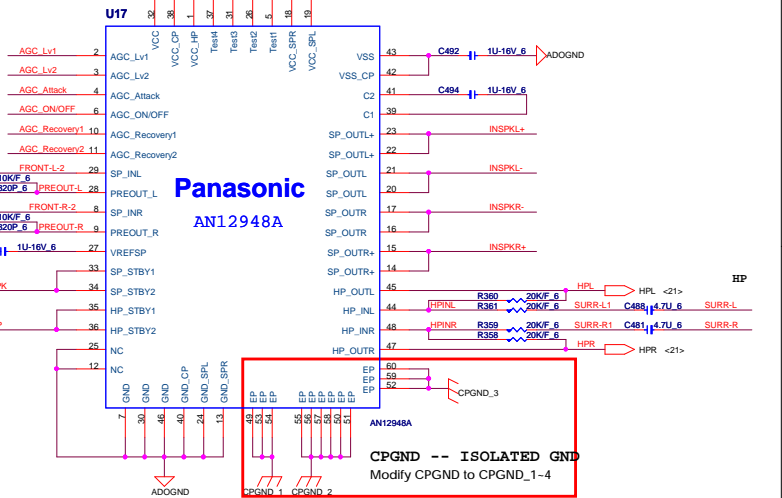
### MDC



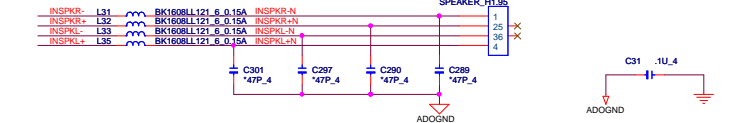
**SP\_STBY ON/OFF & HP\_STBY ON/OFF**

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF CN
LOW	LOW	OFF
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

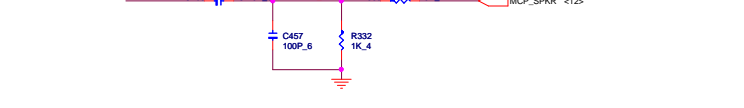
HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF



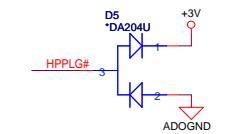
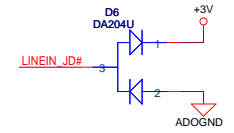
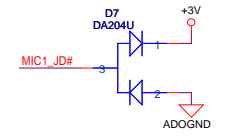
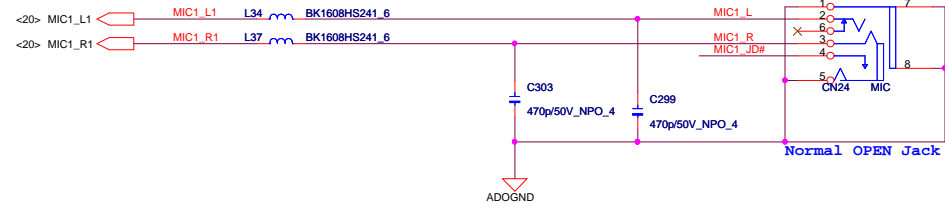
### SPK



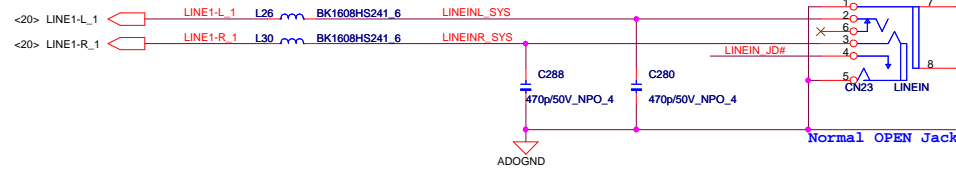
### Beep



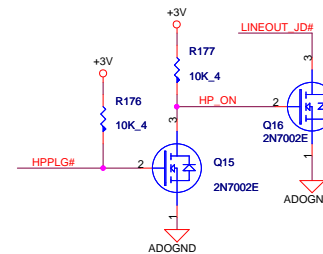
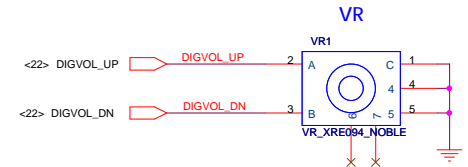
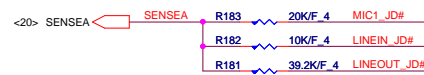
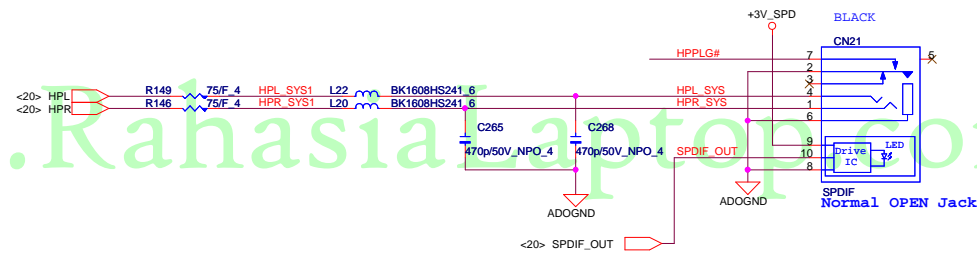
## MIC



## LINE IN

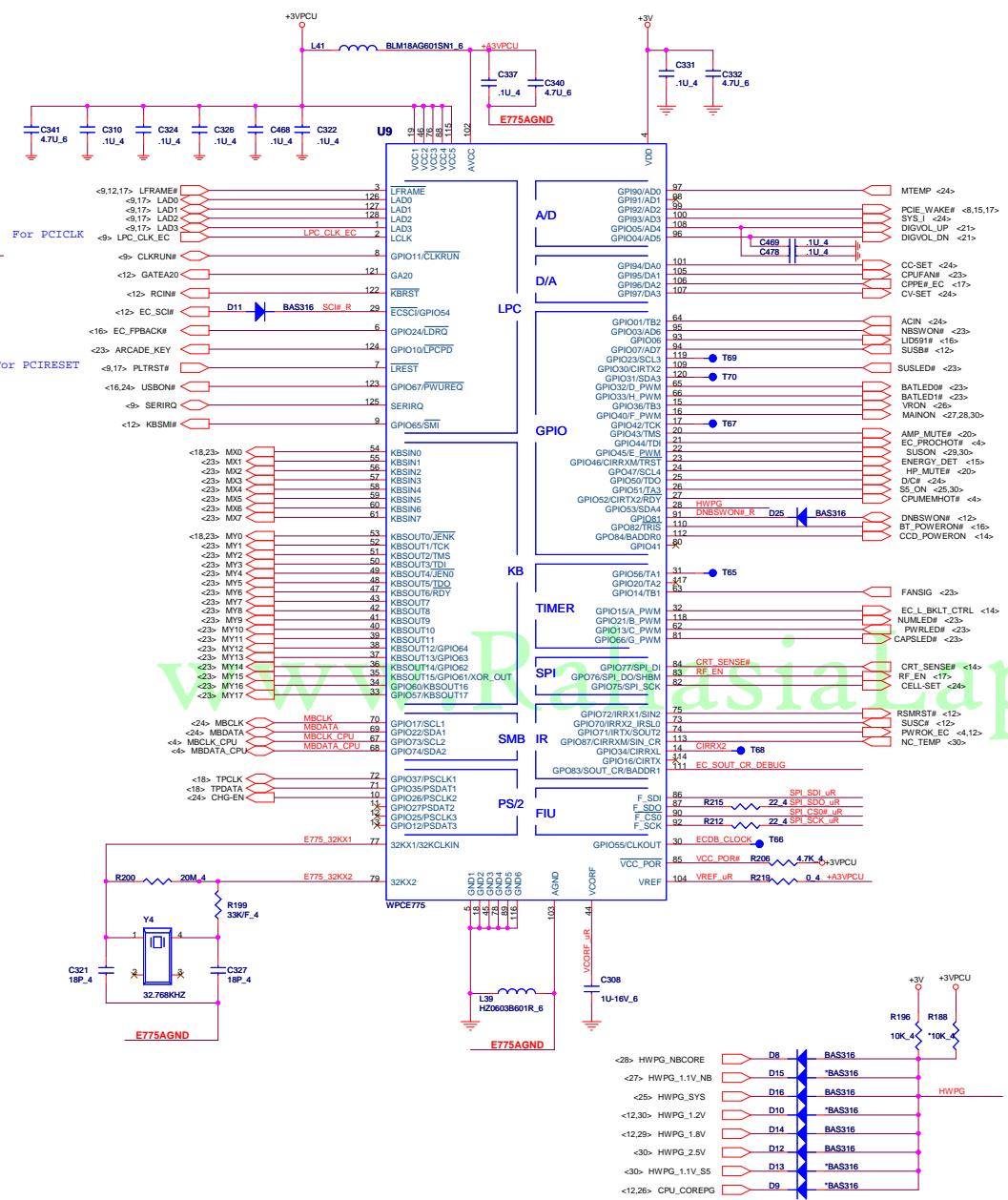


## HeadPhone OUT/SPDIF



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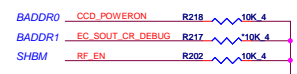
WPCE775C



I/O ADDRESS SETTING

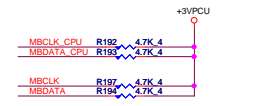
I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

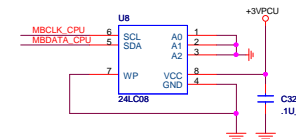


Disabled (\*) if using FW-H device on LPC.  
Enabled (\*) if using SPI flash for both system BIOS and EC firmware

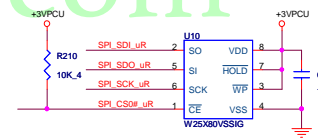
SMBUS PULL-UP



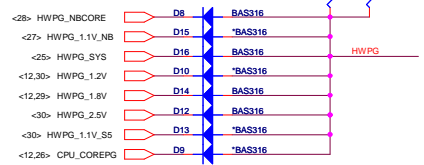
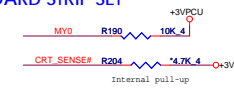
ACER ID



SPI FLASH



INTERNAL KEYBOARD STRIP SET

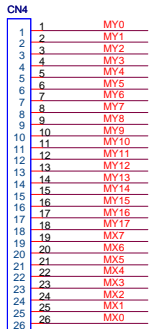


**Quanta Computer Inc.**  
PROJECT : Z05

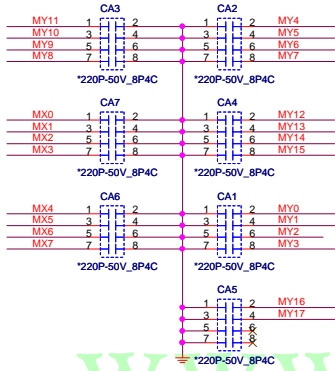
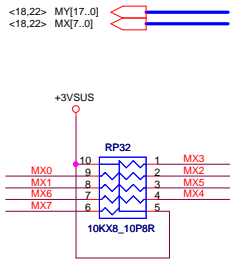
Size: Document Number  
Rev: 1A  
Date: Monday, February 26, 2008 Sheet: 22 of 34



### INT K/B

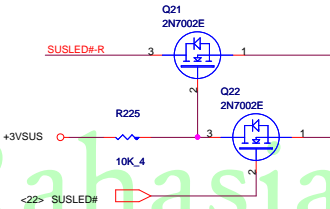
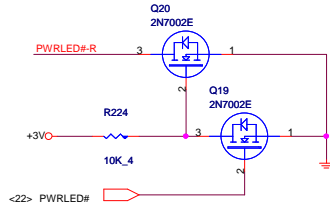
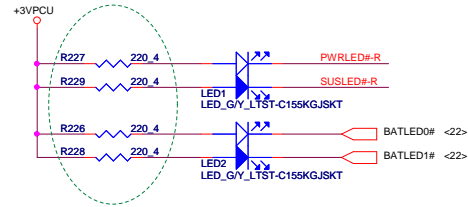


FFC\_26P\_KB

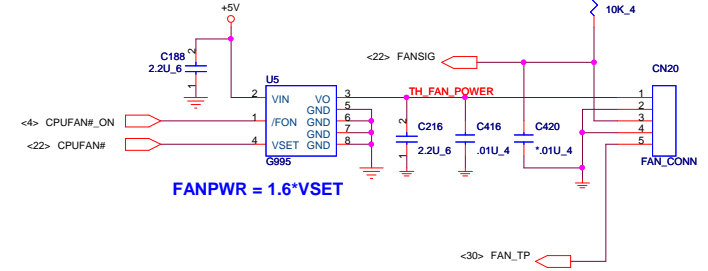


### LED

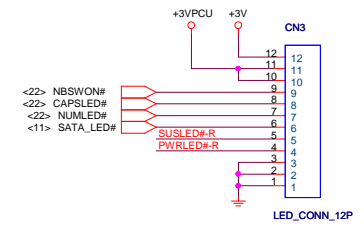
2/21/08' Change from 330ohm to 220ohm on C-test



### CPU FAN



### LED BOARD CONN.



### Debug

Delete Debug Port(PCI & IDE)

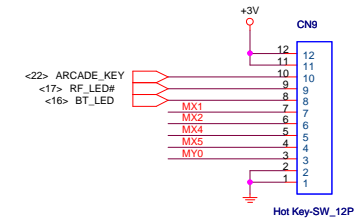
### Fingerprint BOARD CONN.

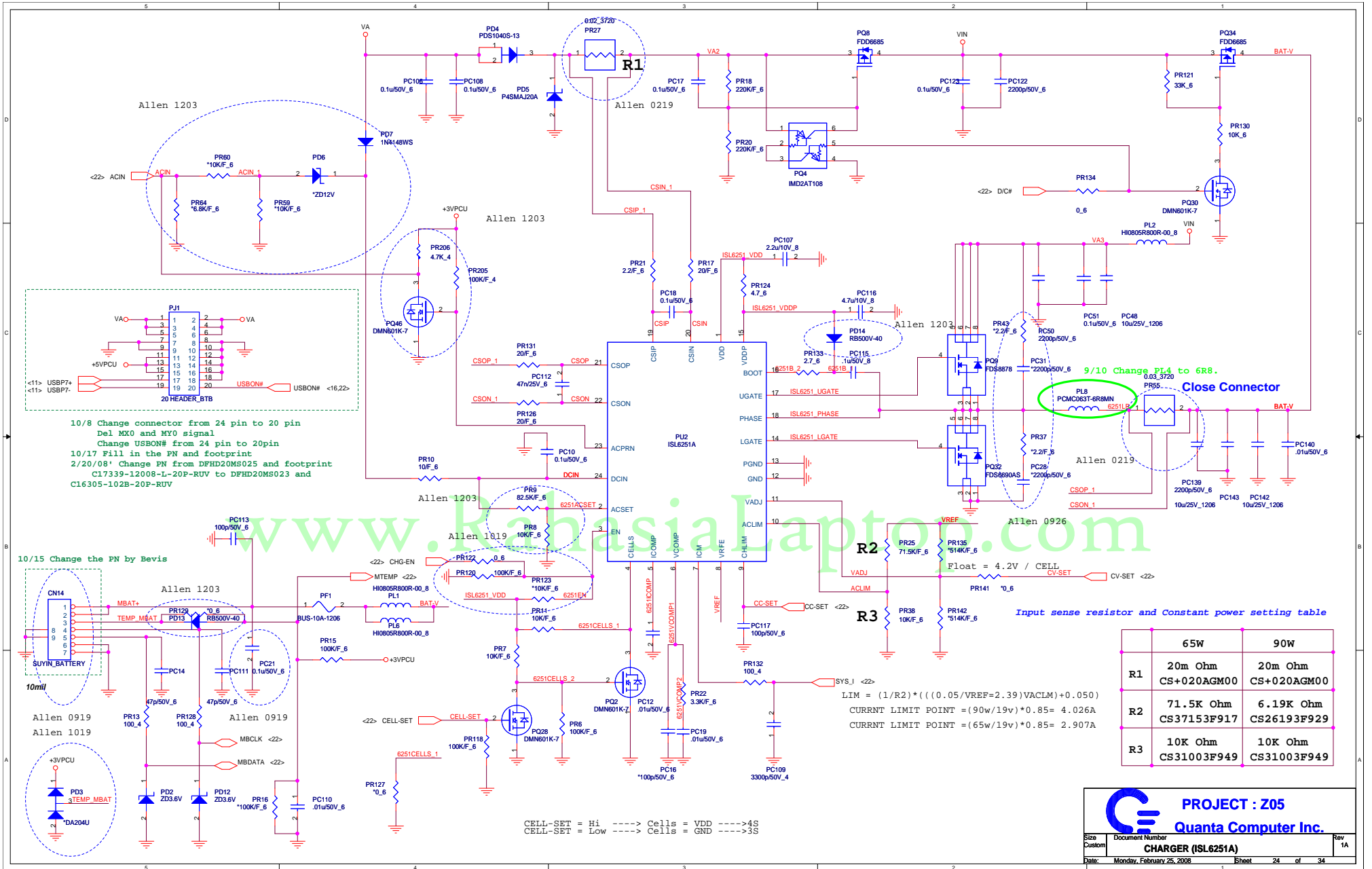


### Button BOARD CONN.

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH





10/8 Change connector from 24 pin to 20 pin  
 Del MX0 and MY0 signal  
 Change USBON# from 24 pin to 20pin  
 10/17 Fill in the PN and footprint  
 2/20/08 Change PN from DFHD20MS025 and footprint  
 C17339-12008-L-20P-RUV to DFHD20MS023 and  
 C16305-102B-20P-RUV

10/15 Change the PN by Bevis

9/10 Change PL4 to 6R8.

Close Connector

$$LIM = (1/R2) * (((0.05/VREF=2.39)VA(ACLIM)+0.050))$$

$$CURRNT\ LIMIT\ POINT = (90w/19v) * 0.85 = 4.026A$$

$$CURRNT\ LIMIT\ POINT = (65w/19v) * 0.85 = 2.907A$$

CELL-SET = Hi ----> Cells = VDD ---->4S  
 CELL-SET = Low ----> Cells = GND ---->3S

	65W	90W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

**PROJECT : Z05**  
**Quanta Computer Inc.**

Size Custom Document Number **CHARGER (ISL6251A)** Rev 1A  
 Date: Monday, February 25, 2008 Sheet 24 of 34



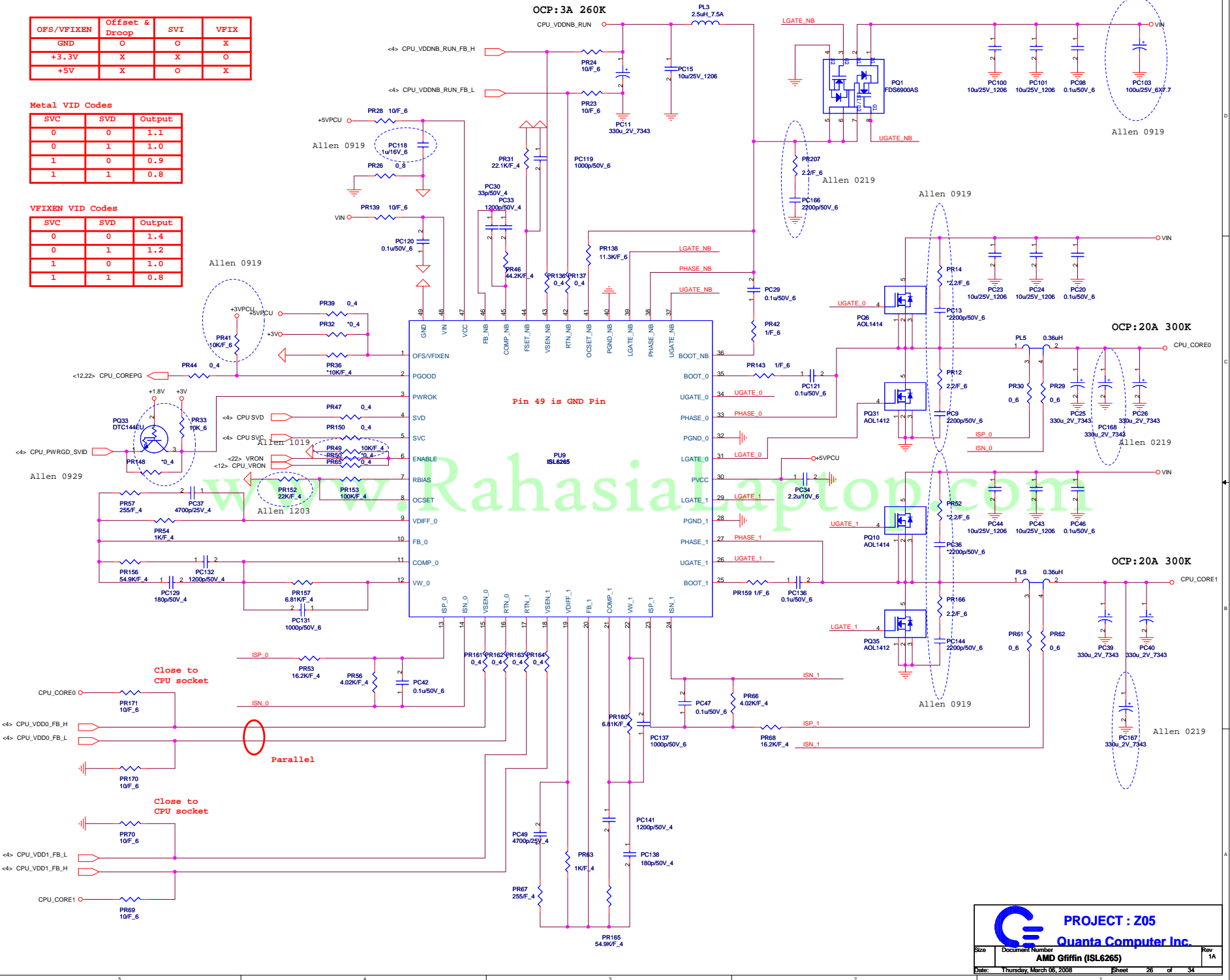
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

**Metal VID Codes**

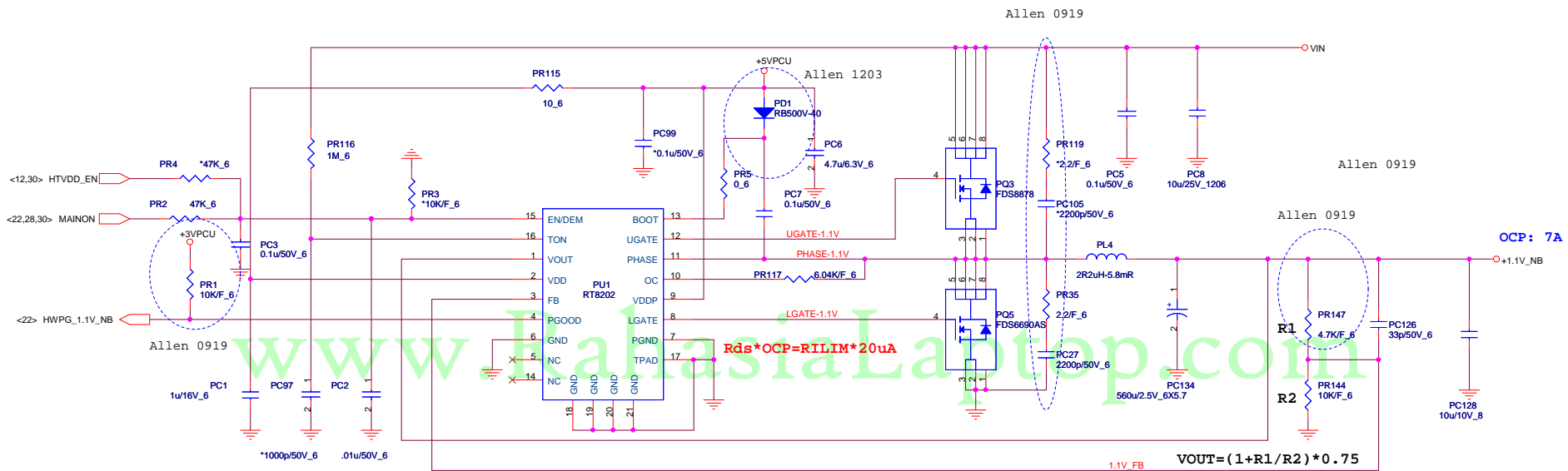
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

**VFIXEN VID Codes**

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



**PROJECT : Z05**  
**Quanta Computer Inc.**  
 Size Document Number  
**AMD Gffinn (ISL6265)** Rev 1A  
 Date: Thursday, March 06, 2008 Sheet 26 of 34



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS Rds=12-15mOhm

OCP=7-0.8A

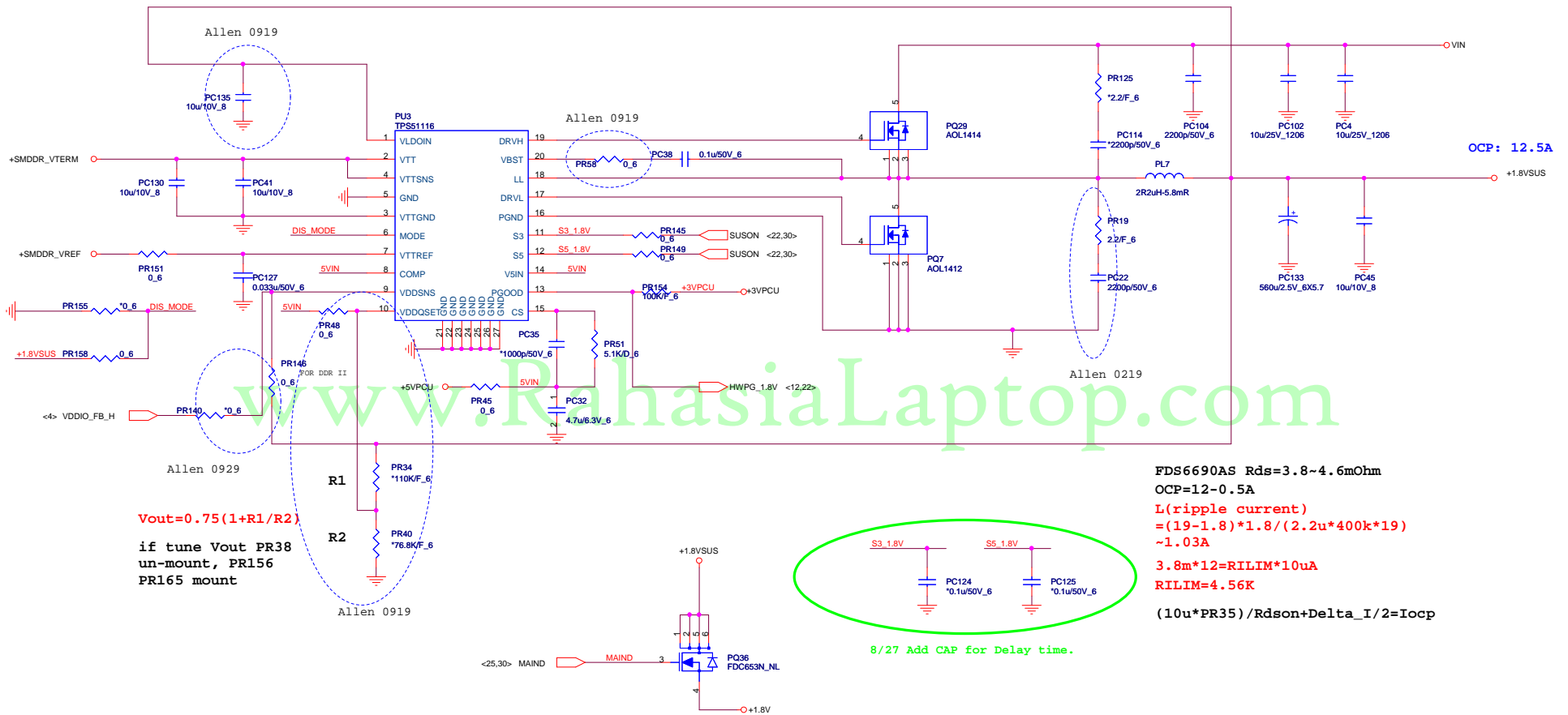
L(ripple current)  
 $= (19-1) * 1 / (2.2u * 272k * 19)$   
 ~1.58A

$12m * 6 = RILIM * 20uA$   
 RILIM=3.6K (2.5~8K)

$$Rds * OCP = RILIM * 20uA$$

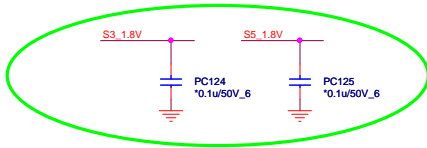
$$VOUI = (1 + R1/R2) * 0.75$$





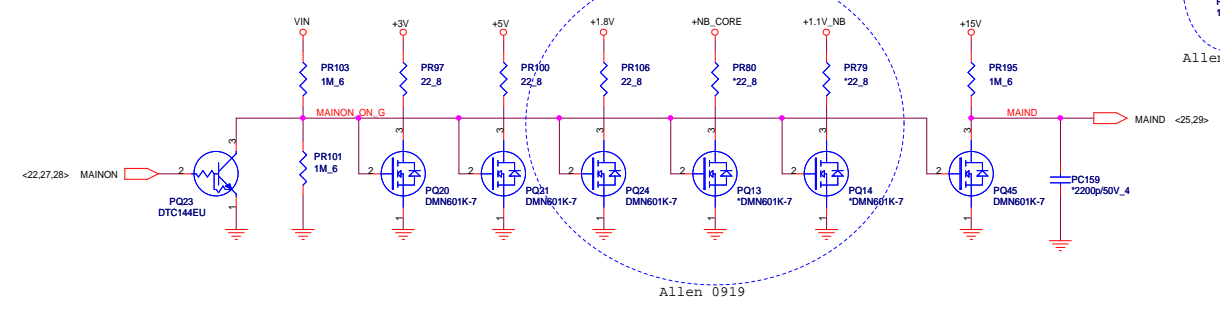
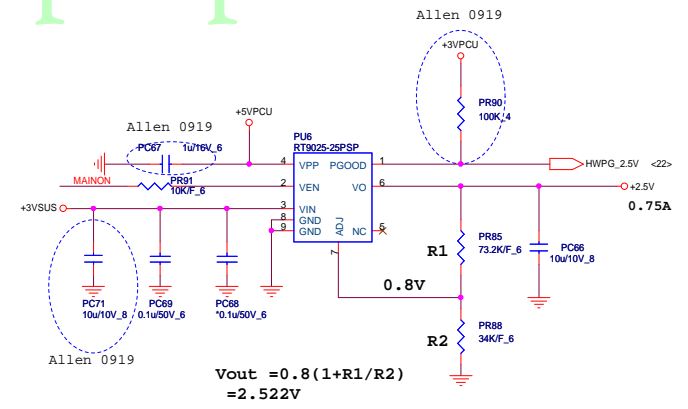
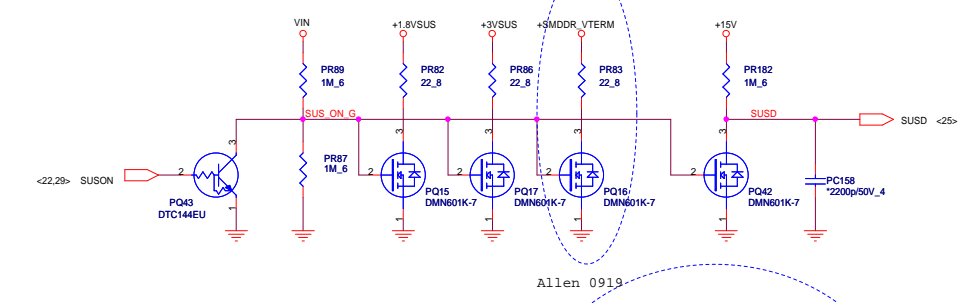
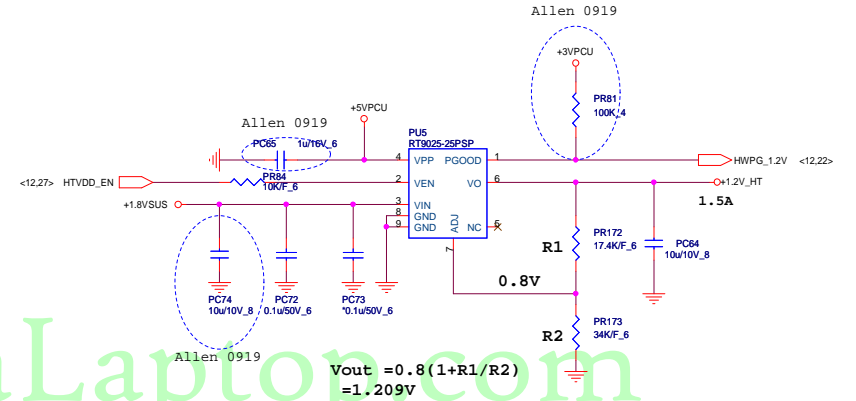
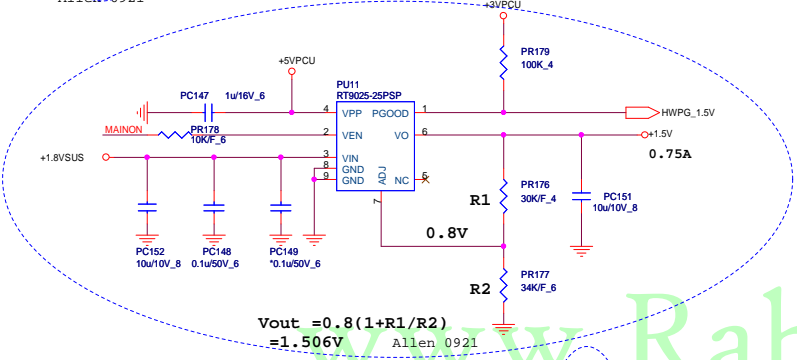
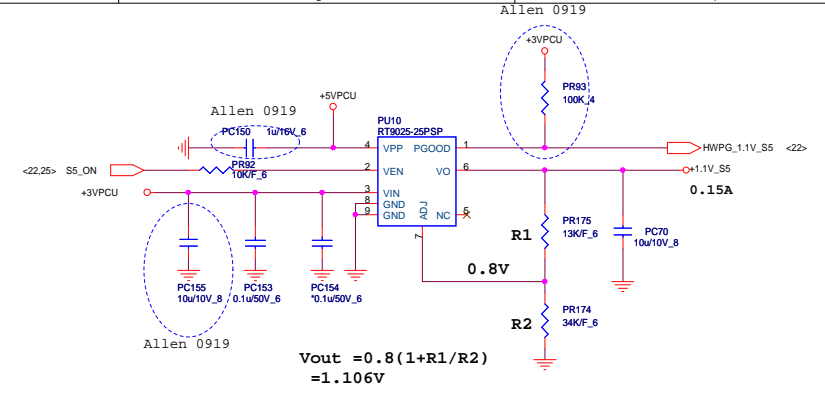
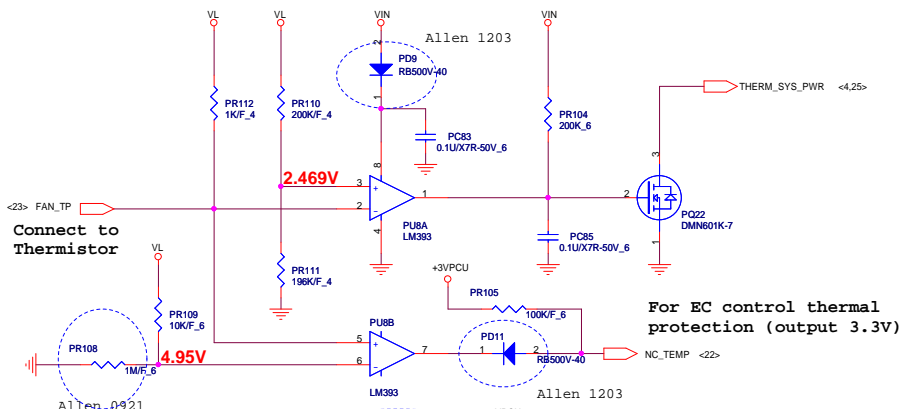
$V_{out} = 0.75(1 + R1/R2)$   
 if tune  $V_{out}$  PR38  
 un-mount, PR156  
 PR165 mount

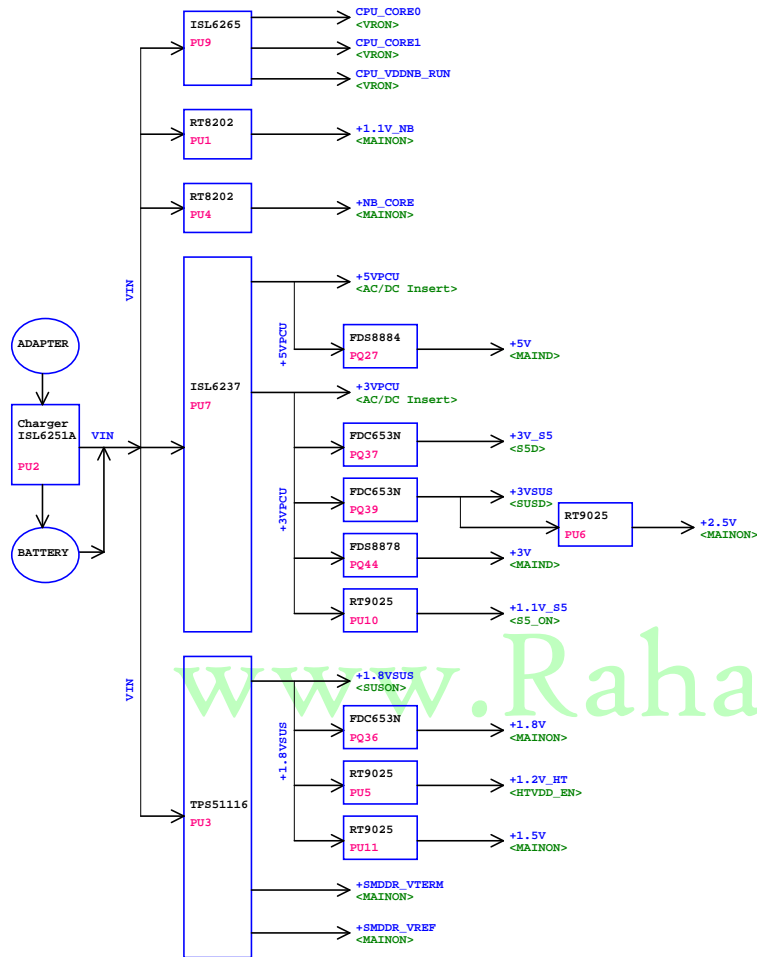
FDS6690AS  $R_{ds} = 3.8 \sim 4.6 \text{ m}\Omega$   
 OCP = 12-0.5A  
 $L(\text{ripple current}) = (19-1.8) * 1.8 / (2.2\mu * 400k * 19) \sim 1.03A$   
 $3.8m * 12 = RILIM * 10\mu A$   
 $RILIM = 4.56K$   
 $(10\mu * PR35) / R_{ds(on)} + \Delta I / 2 = I_{ocp}$



8/27 Add CAP for Delay time.







1. +1.1V\_S5MCP77M Power(+1.1V\_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V\_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C,SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VPCU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VPCU VDDA
9. +3V\_LANLAN Power(BCM5764M)
10. +1.2V\_LANLAN Power(BCM5764M)
11. +2.5V\_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDDR\_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V\_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB\_COREMCP77M Core Power
18. +1.2V\_HTCPU HT Power
19. CPU\_CORE0 CPU Power
20. CPU\_CORE1 CPU Power
21. CPU\_VDDNB\_RUNCPU NB Power
- 22.