

Compal Confidential

NDWGO Schematics Document

AMD S1g3/ RS880M/ SB710

2009 / 09 / 22

LA-5991P

Rev:0.1

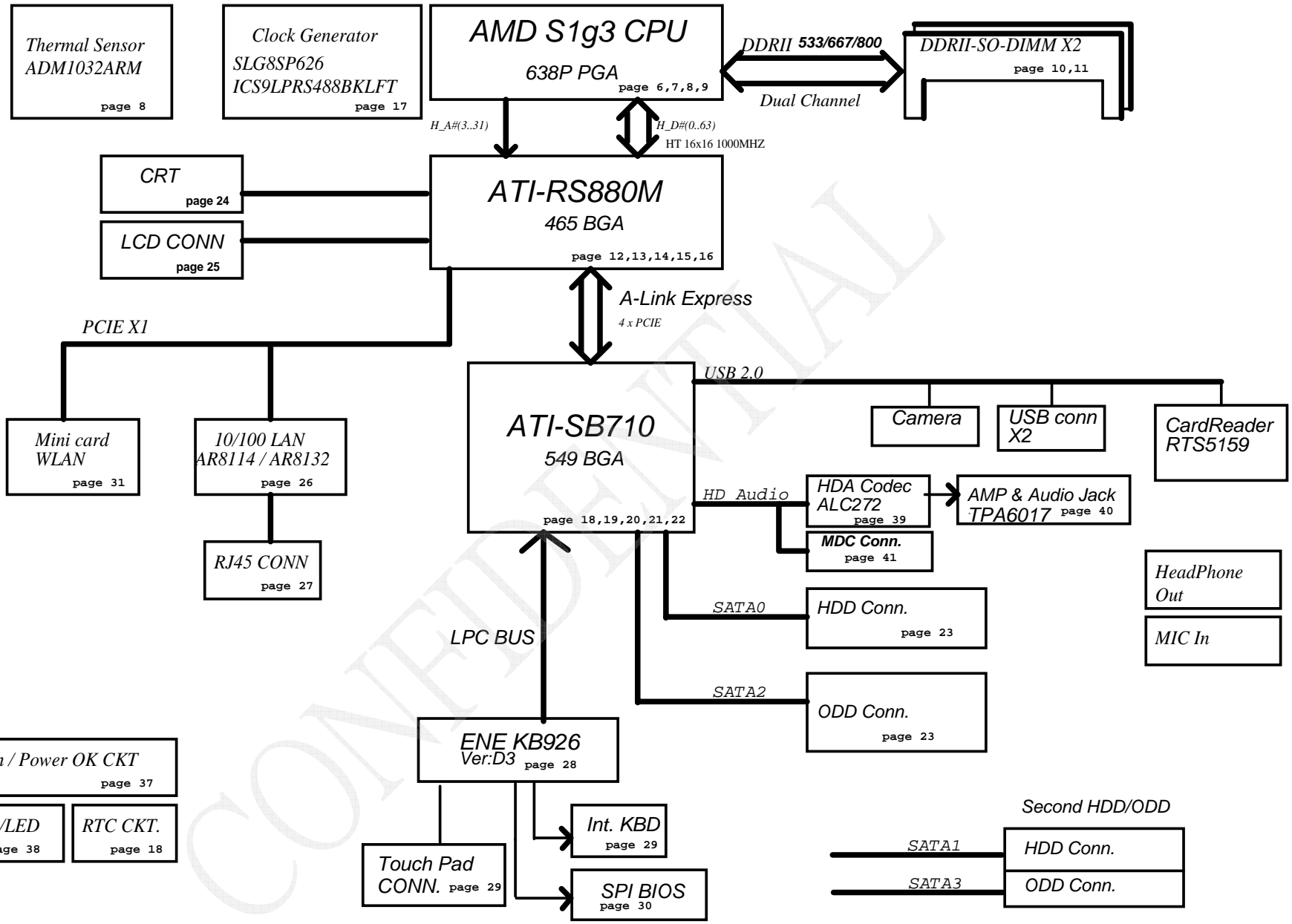
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Project Code: NDWG0/H0

File Name : LA-5991P



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DC/DC Interface CKT. page 41

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Voltage Rails

Power Rail	Description	ON	OFF	ON*
VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

EC SM Bus2 address

SB600 SM Bus 1 address

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

SB600 SM Bus 2 address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

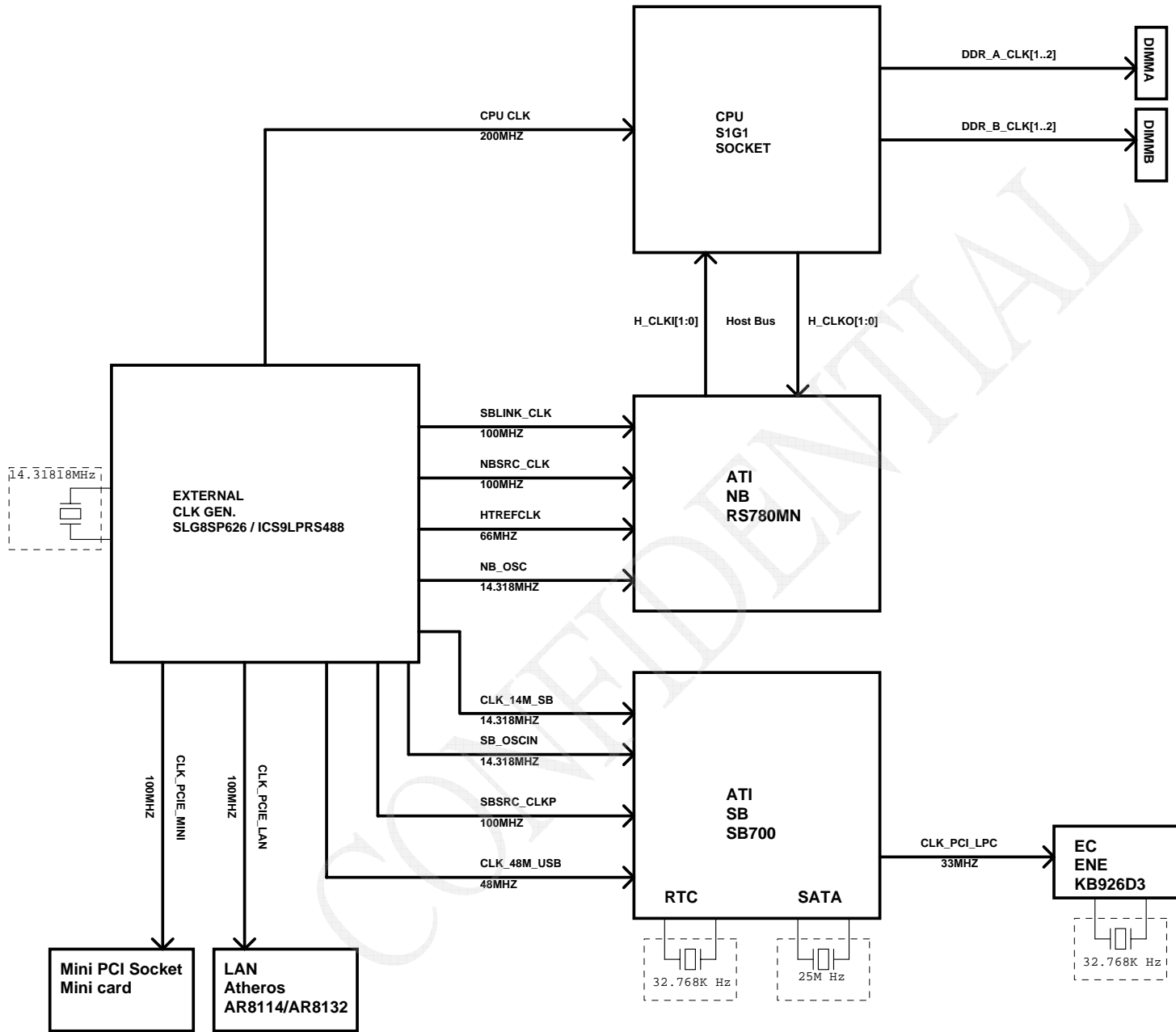
BTO Option Table

BTO Item	BOM Structure
10/100 Lan	8114@
GIGA Lan	8132@
17" ID	17@
15" ID	15@
Support VaryBright	VARY@

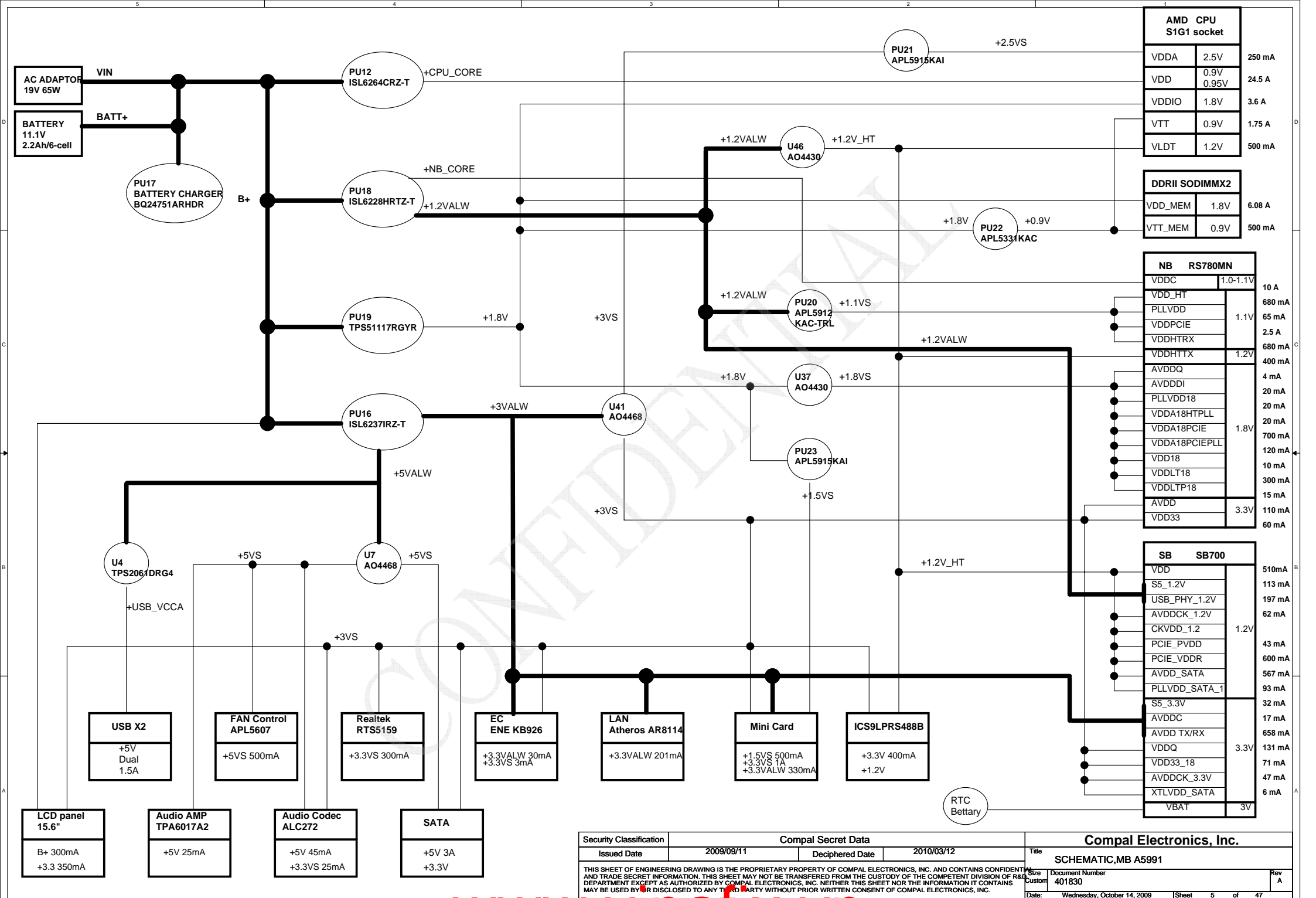
PROJECT ID Table

SKU ID	SKU
0	NCWGO
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

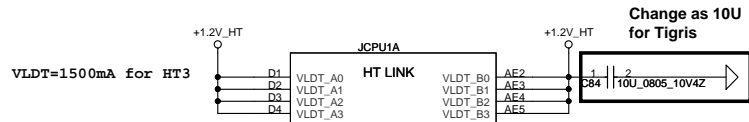
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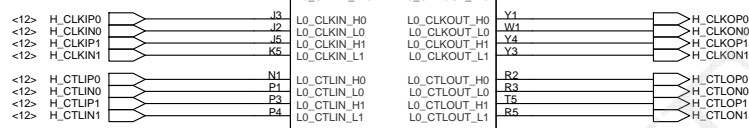


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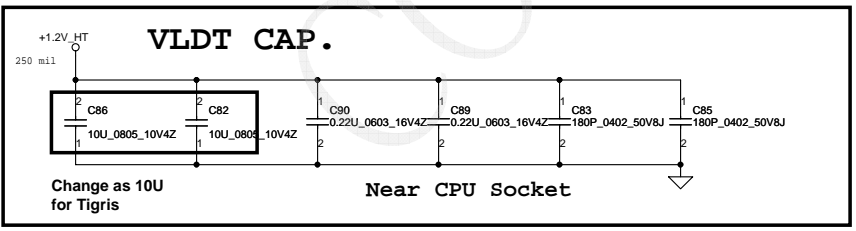
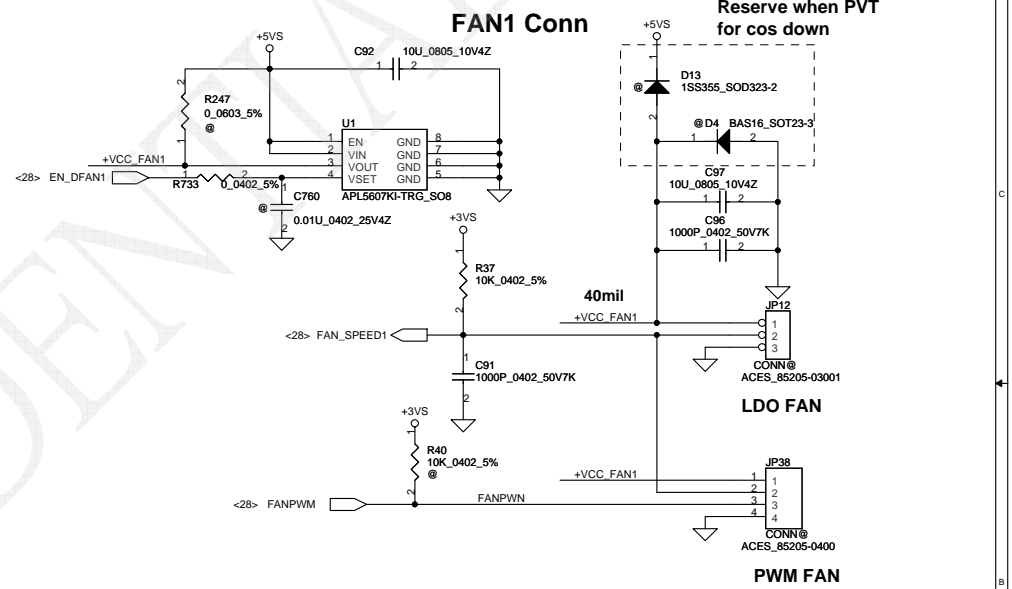


HT LINK		HT LINK	
VLDT_A0	D1	VLDT_B0	AE2
VLDT_A1	D2	VLDT_B1	AE3
VLDT_A2	D3	VLDT_B2	AE4
VLDT_A3	D4	VLDT_B3	AE5

H_CADIP		L0_CADIN		L0_CADOUT		H_CADOP		H_CADON	
H_CADIP0	E3	L0_CADIN_H0	L0	L0_CADOUT_H0	L0	AD1	H	AC1	H
H_CADIN0	F2	L0_CADIN_L0	L0	L0_CADOUT_L0	L0	AC4	H	AC2	H
H_CADIP1	F1	L0_CADIN_H1	L0	L0_CADOUT_H1	L0	AC3	H	AC3	H
H_CADIN1	F1	L0_CADIN_L1	L0	L0_CADOUT_L1	L0	AB1	H	AA1	H
H_CADIP2	G3	L0_CADIN_H2	L0	L0_CADOUT_H2	L0	AA2	H	AA2	H
H_CADIN2	G2	L0_CADIN_L2	L0	L0_CADOUT_L2	L0	AA3	H	AA3	H
H_CADIP3	G1	L0_CADIN_H3	L0	L0_CADOUT_H3	L0	W2	H	W2	H
H_CADIN3	H1	L0_CADIN_L3	L0	L0_CADOUT_L3	L0	W3	H	W3	H
H_CADIP4	J1	L0_CADIN_H4	L0	L0_CADOUT_H4	L0	W1	H	W1	H
H_CADIN4	K1	L0_CADIN_L4	L0	L0_CADOUT_L4	L0	L11	H	L11	H
H_CADIP5	L3	L0_CADIN_H5	L0	L0_CADOUT_H5	L0	L12	H	L12	H
H_CADIN5	L2	L0_CADIN_L5	L0	L0_CADOUT_L5	L0	L13	H	L13	H
H_CADIP6	I1	L0_CADIN_H6	L0	L0_CADOUT_H6	L0	T1	H	T1	H
H_CADIN6	M1	L0_CADIN_L6	L0	L0_CADOUT_L6	L0	R1	H	R1	H
H_CADIP7	N3	L0_CADIN_H7	L0	L0_CADOUT_H7	L0	AD4	H	AD4	H
H_CADIN7	N2	L0_CADIN_L7	L0	L0_CADOUT_L7	L0	AD3	H	AD3	H
H_CADIP8	E5	L0_CADIN_H8	L0	L0_CADOUT_H8	L0	AD5	H	AD5	H
H_CADIN8	F3	L0_CADIN_L8	L0	L0_CADOUT_L8	L0	AC5	H	AC5	H
H_CADIP9	F3	L0_CADIN_H9	L0	L0_CADOUT_H9	L0	AB4	H	AB4	H
H_CADIN9	F4	L0_CADIN_L9	L0	L0_CADOUT_L9	L0	AB3	H	AB3	H
H_CADIP10	G5	L0_CADIN_H10	L0	L0_CADOUT_H10	L0	AB5	H	AB5	H
H_CADIN10	H5	L0_CADIN_L10	L0	L0_CADOUT_L10	L0	AA5	H	AA5	H
H_CADIP11	H3	L0_CADIN_H11	L0	L0_CADOUT_H11	L0	Y5	H	Y5	H
H_CADIN11	H4	L0_CADIN_L11	L0	L0_CADOUT_L11	L0	W5	H	W5	H
H_CADIP12	K3	L0_CADIN_H12	L0	L0_CADOUT_H12	L0	V4	H	V4	H
H_CADIN12	K4	L0_CADIN_L12	L0	L0_CADOUT_L12	L0	V3	H	V3	H
H_CADIP13	L5	L0_CADIN_H13	L0	L0_CADOUT_H13	L0	L15	H	L15	H
H_CADIN13	M5	L0_CADIN_L13	L0	L0_CADOUT_L13	L0	T4	H	T4	H
H_CADIP14	M3	L0_CADIN_H14	L0	L0_CADOUT_H14	L0	T3	H	T3	H
H_CADIN14	M4	L0_CADIN_L14	L0	L0_CADOUT_L14	L0				
H_CADIP15	N5	L0_CADIN_H15	L0	L0_CADOUT_H15	L0				
H_CADIN15	P5	L0_CADIN_L15	L0	L0_CADOUT_L15	L0				



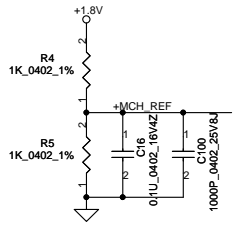
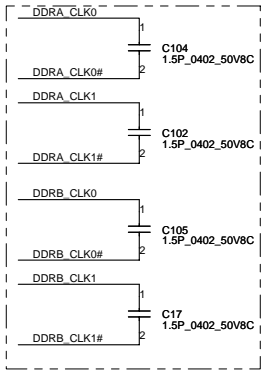
6090022100G_B
Athlon 64 S1
Processor Socket



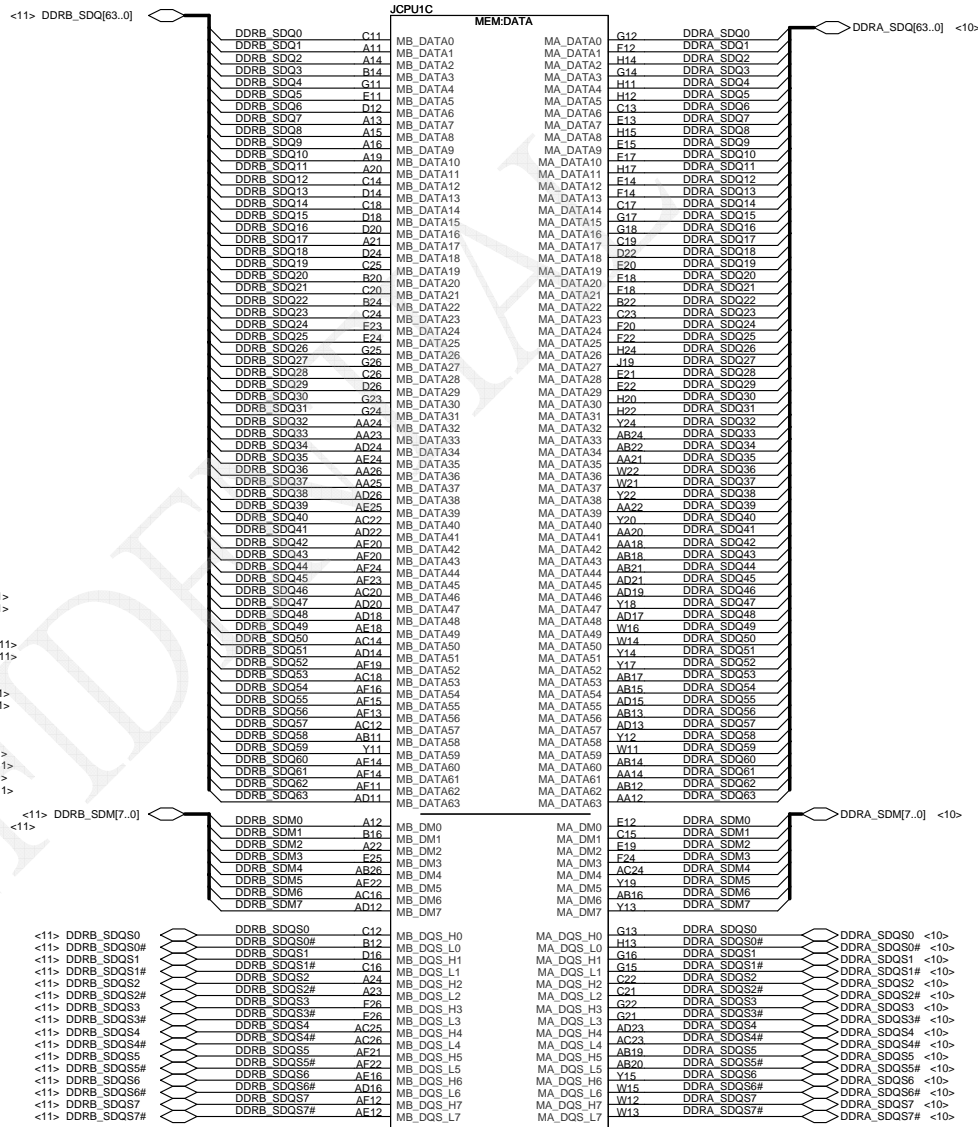
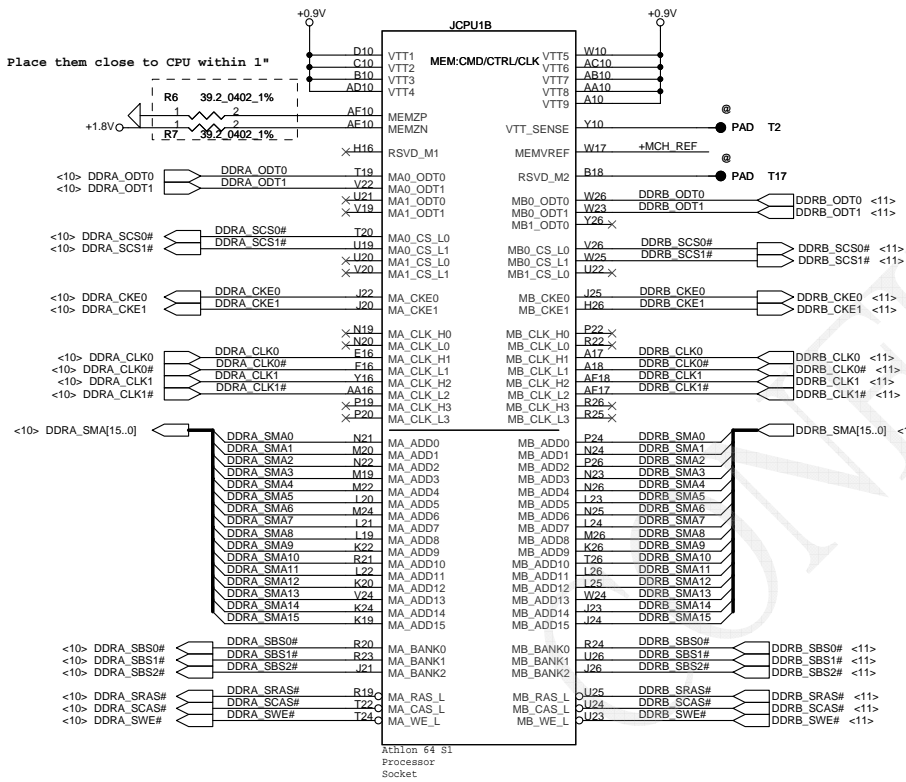
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PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

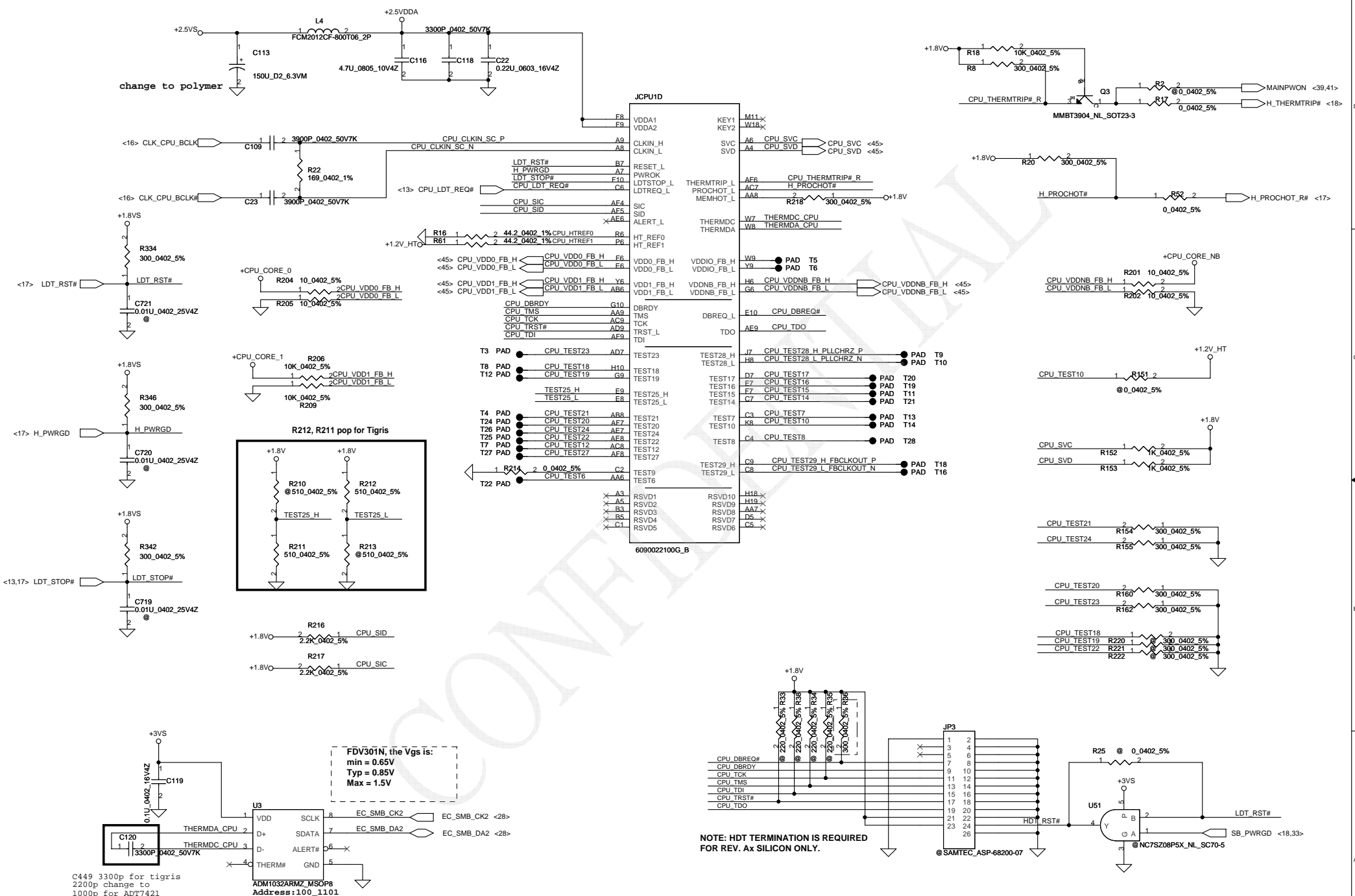


Processor DDR2 Memory Interface



6909022100G_B
Athlon 64 S1 Processor Socket

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C449 3300p for tigris
2200p change to
1000p for ADT7421

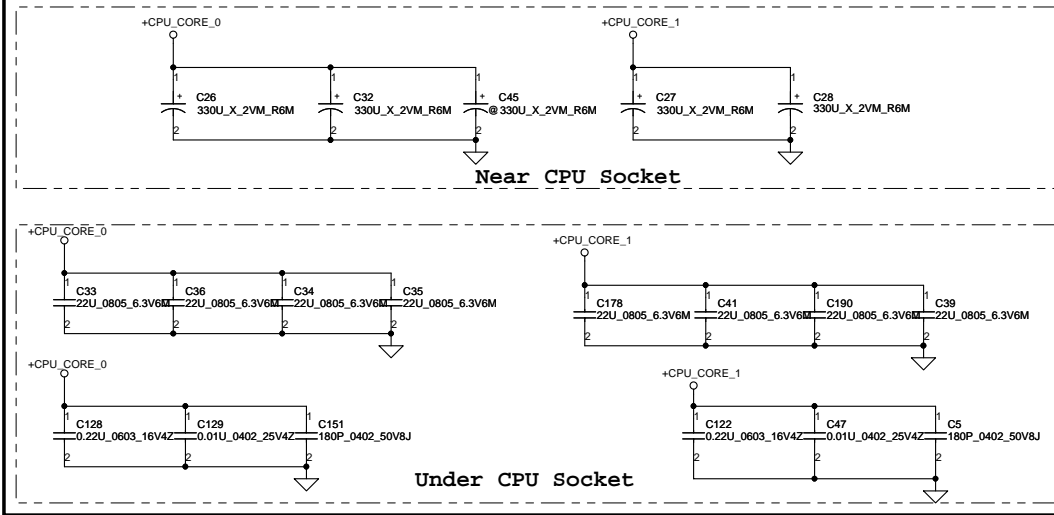
FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

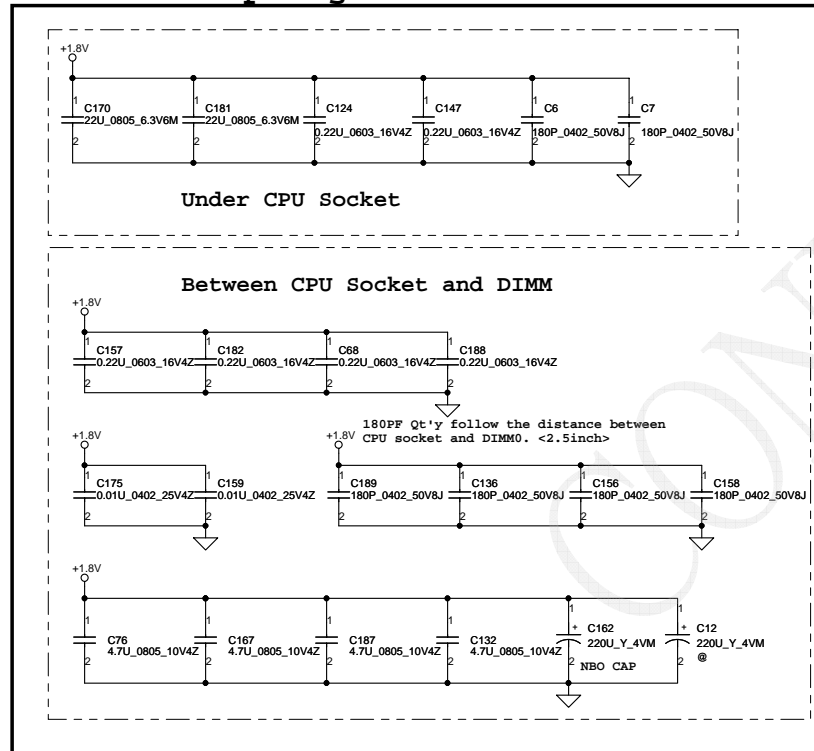
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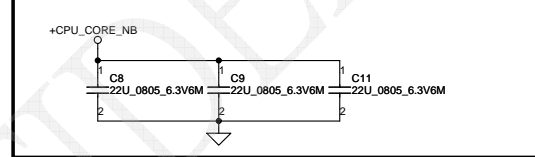
VDD(+CPU_CORE) decoupling.



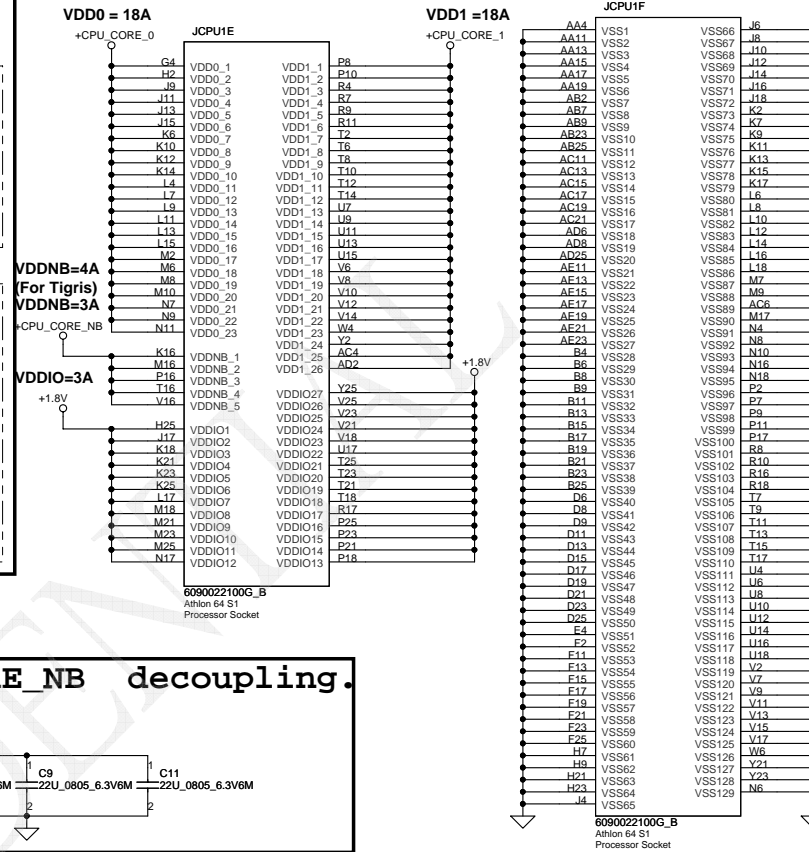
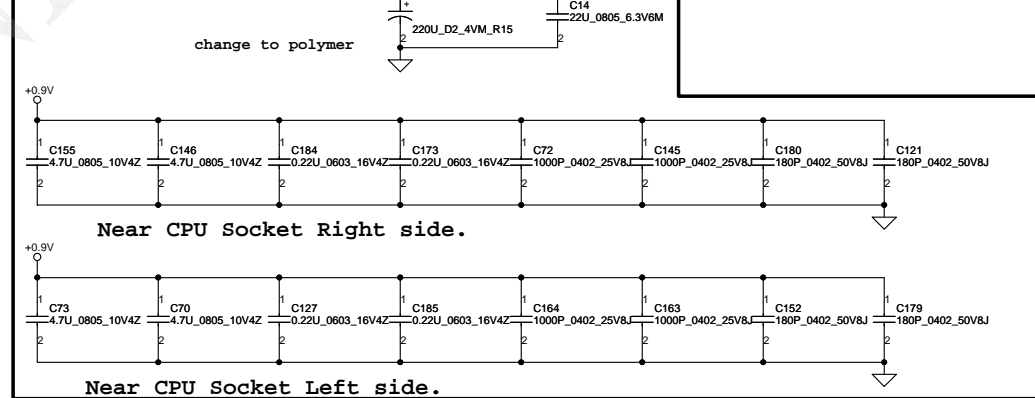
VDDIO decoupling.



+CPU_CORE_NB decoupling.

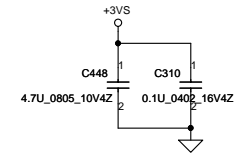
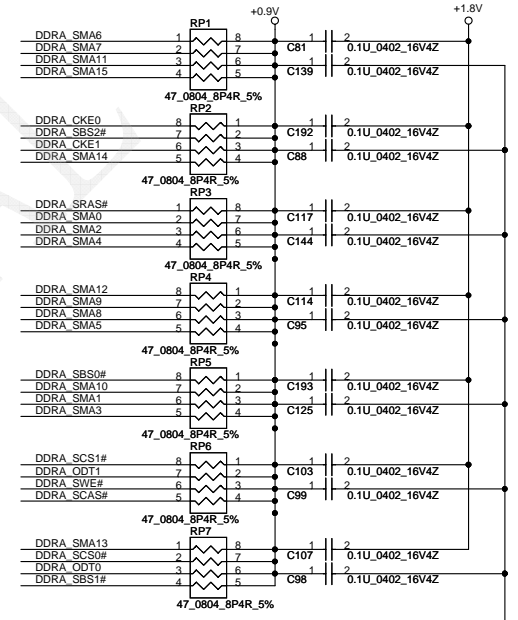
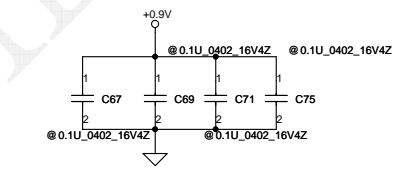
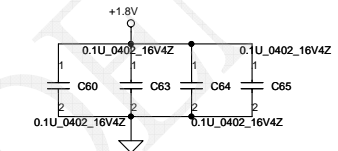
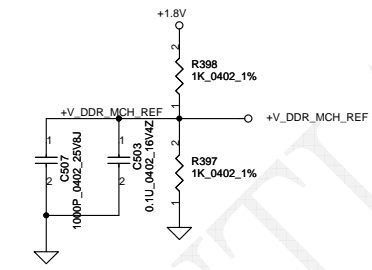
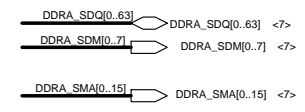
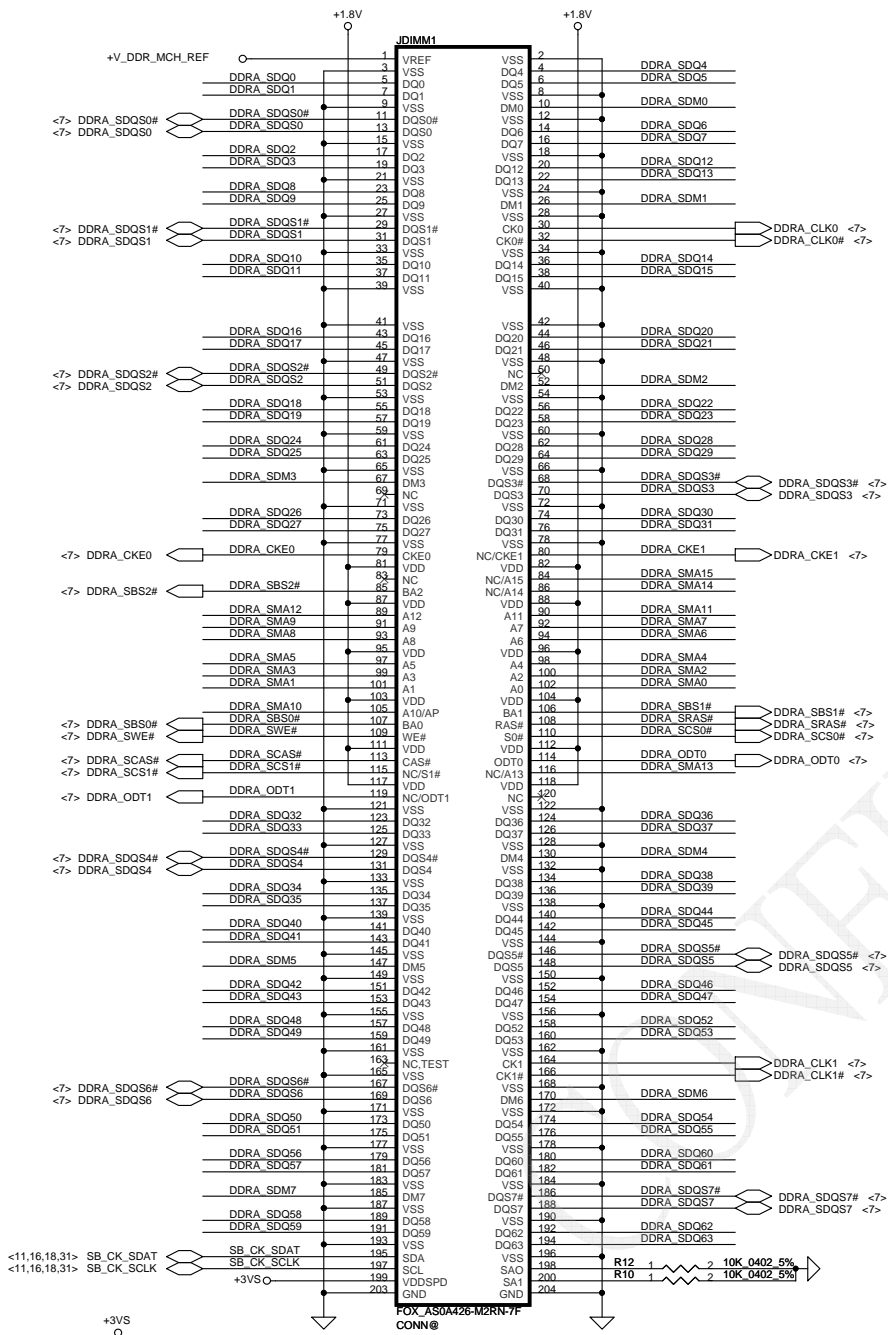


VTT decoupling.



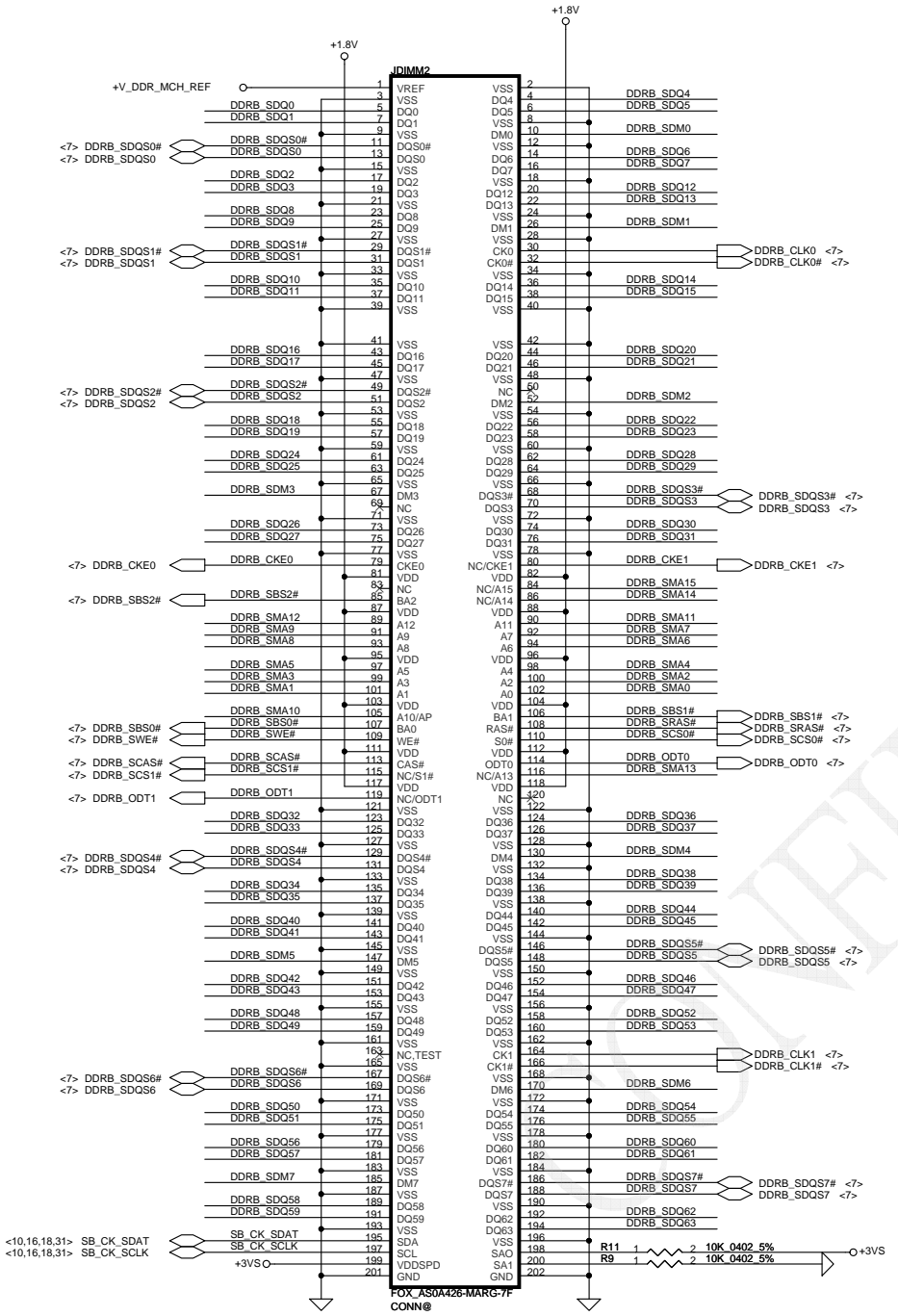
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RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT

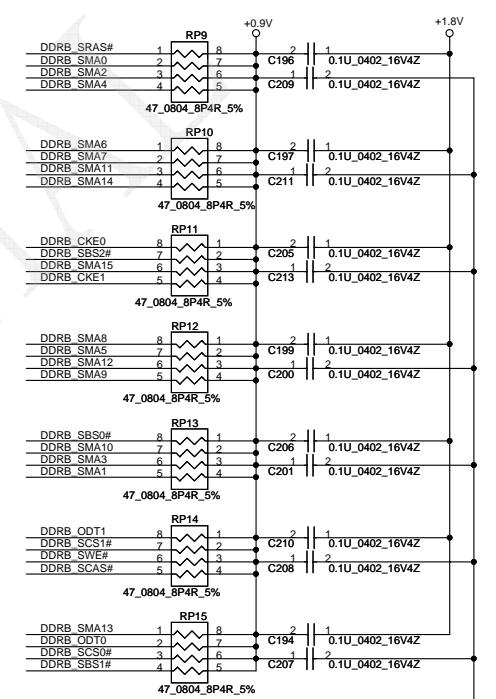
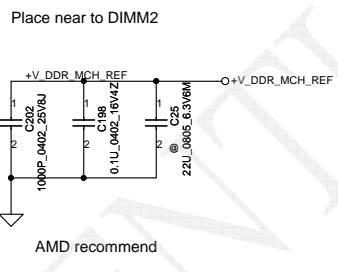
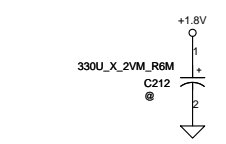
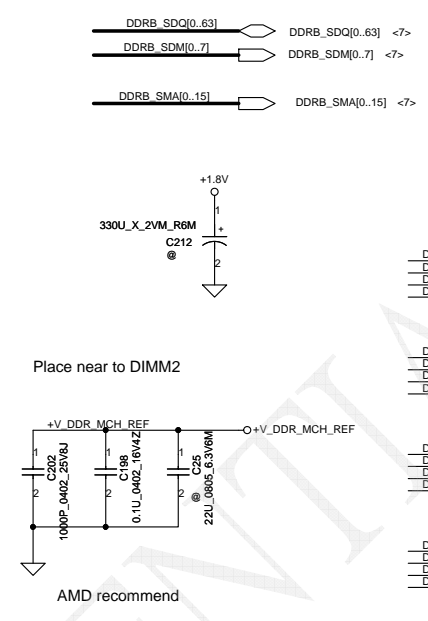


DIMM1 REV H:5.2mm (BOT)

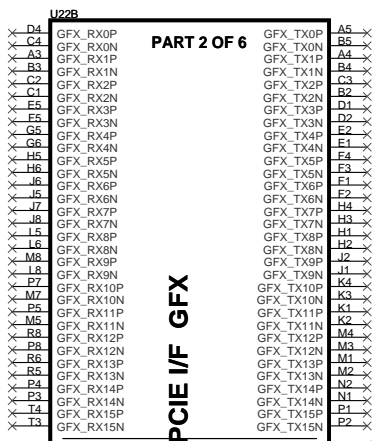
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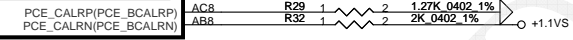
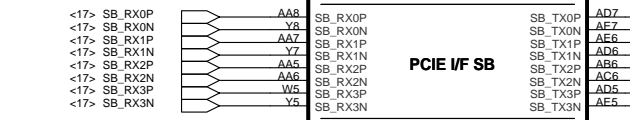
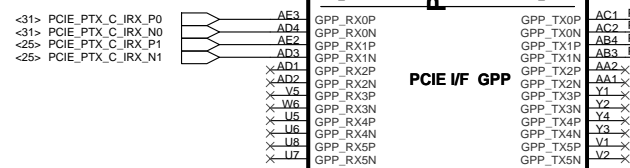
DIMM1 REV H:9.2mm (BOT)



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Check SW Routing
AN_RS780MN1. Only suggest pair0-3 can use for power save.

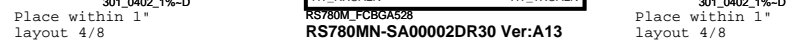
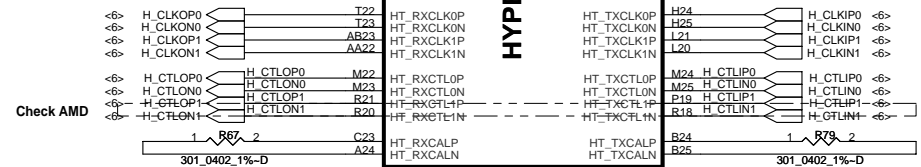
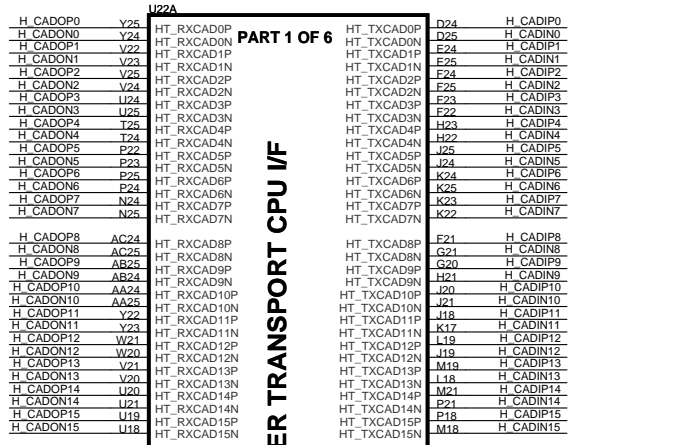


RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

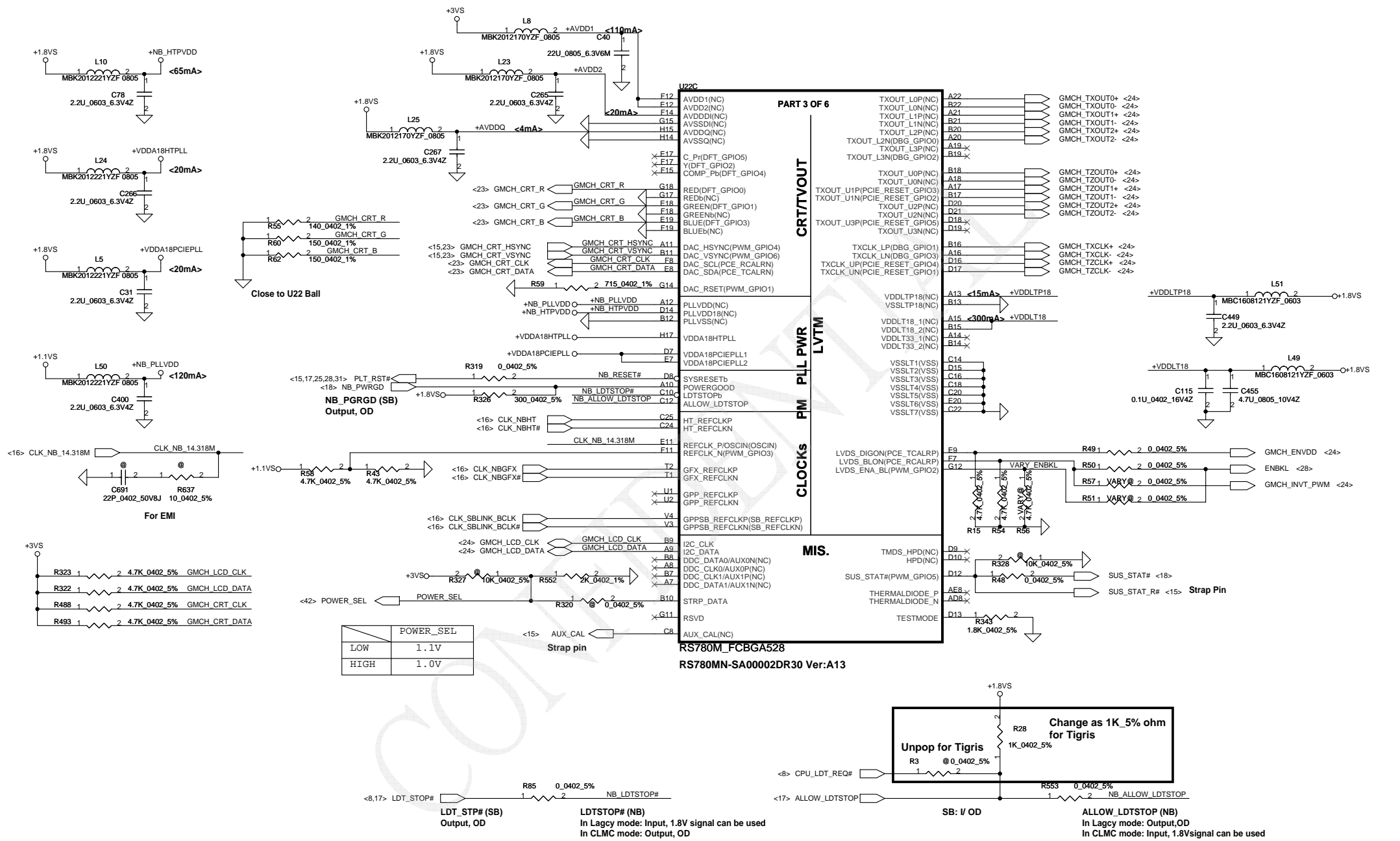
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

HT Link
When tune trace length, must keep 1:4 on self-trace

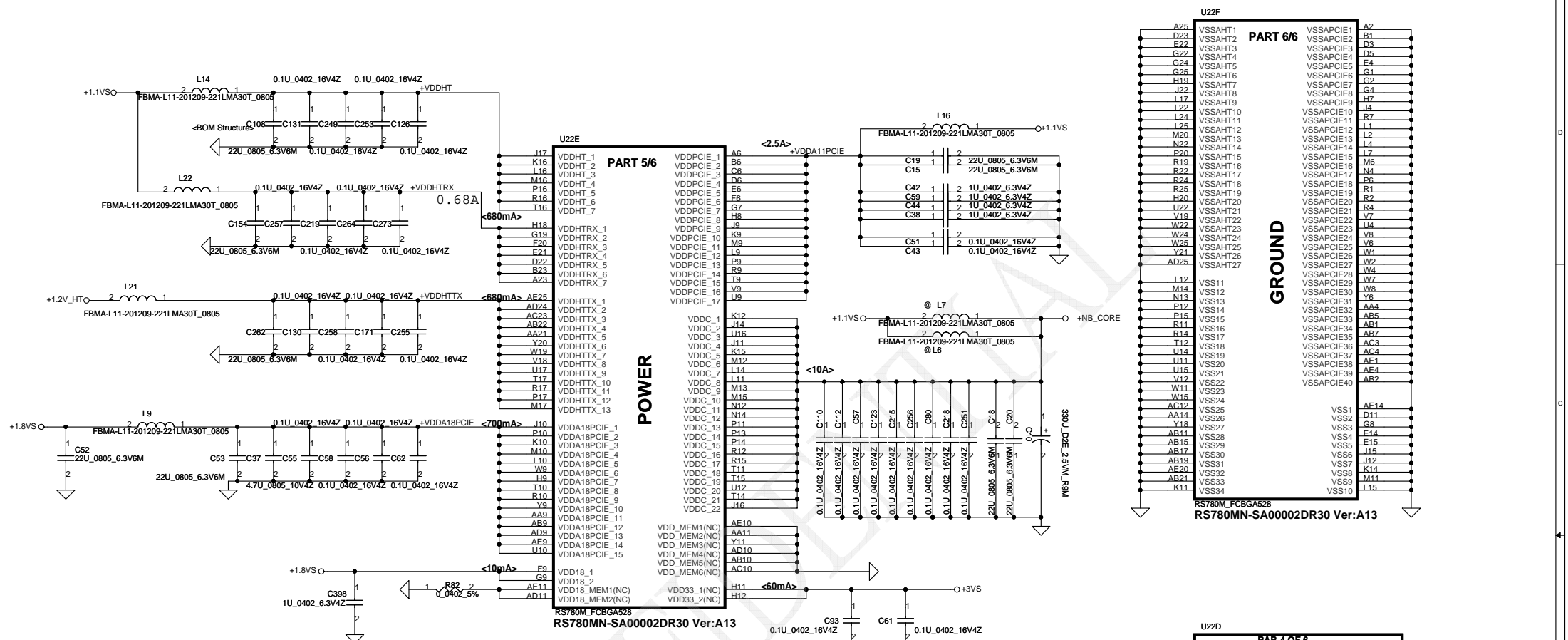


RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

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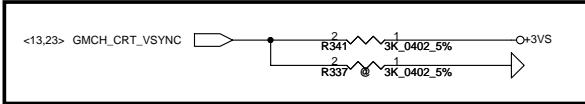
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				13 of 47



COMPAL

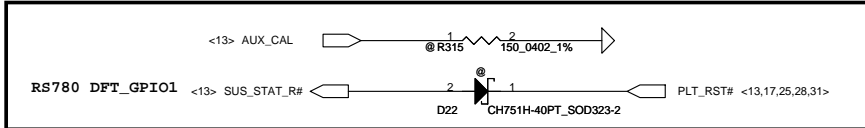
RS780M_FCBA528
RS780MN-SA0002DR30 Ver:A13

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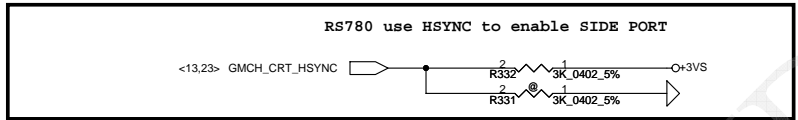
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



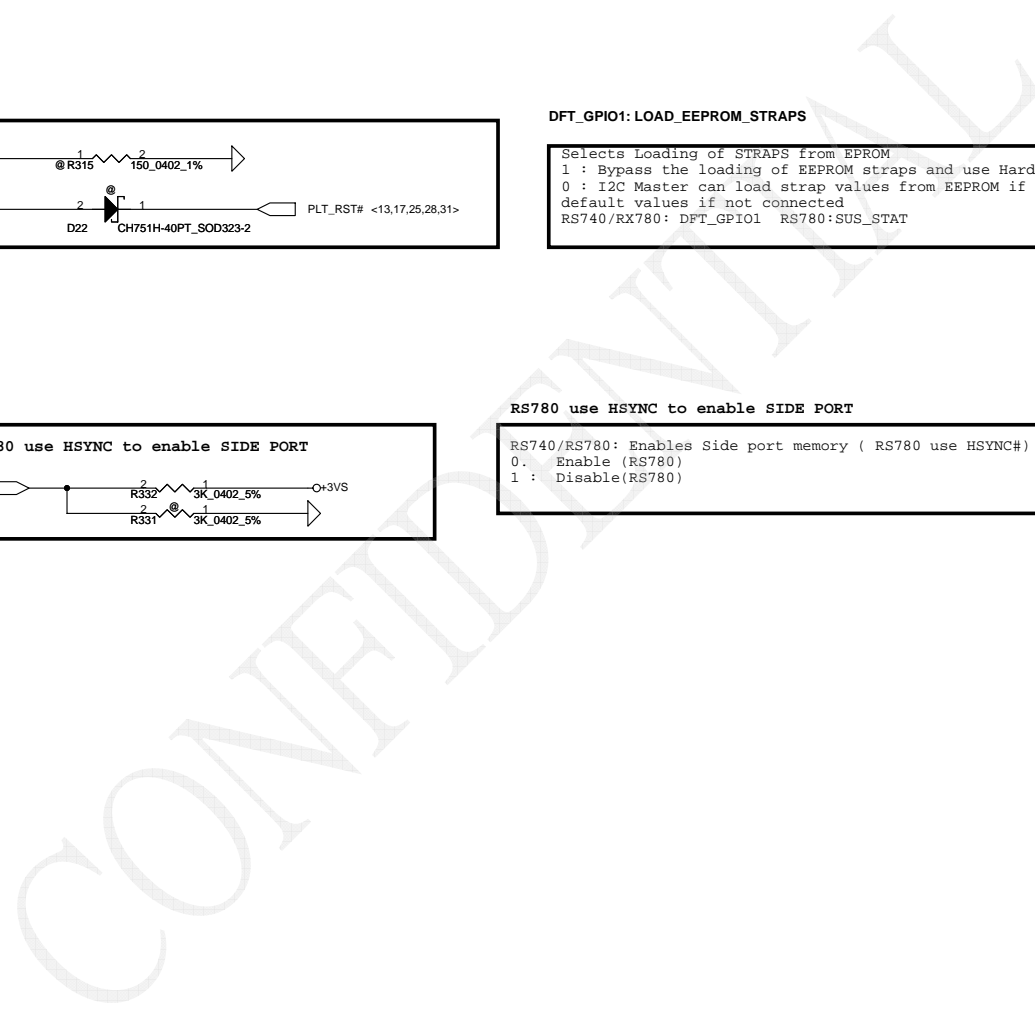
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

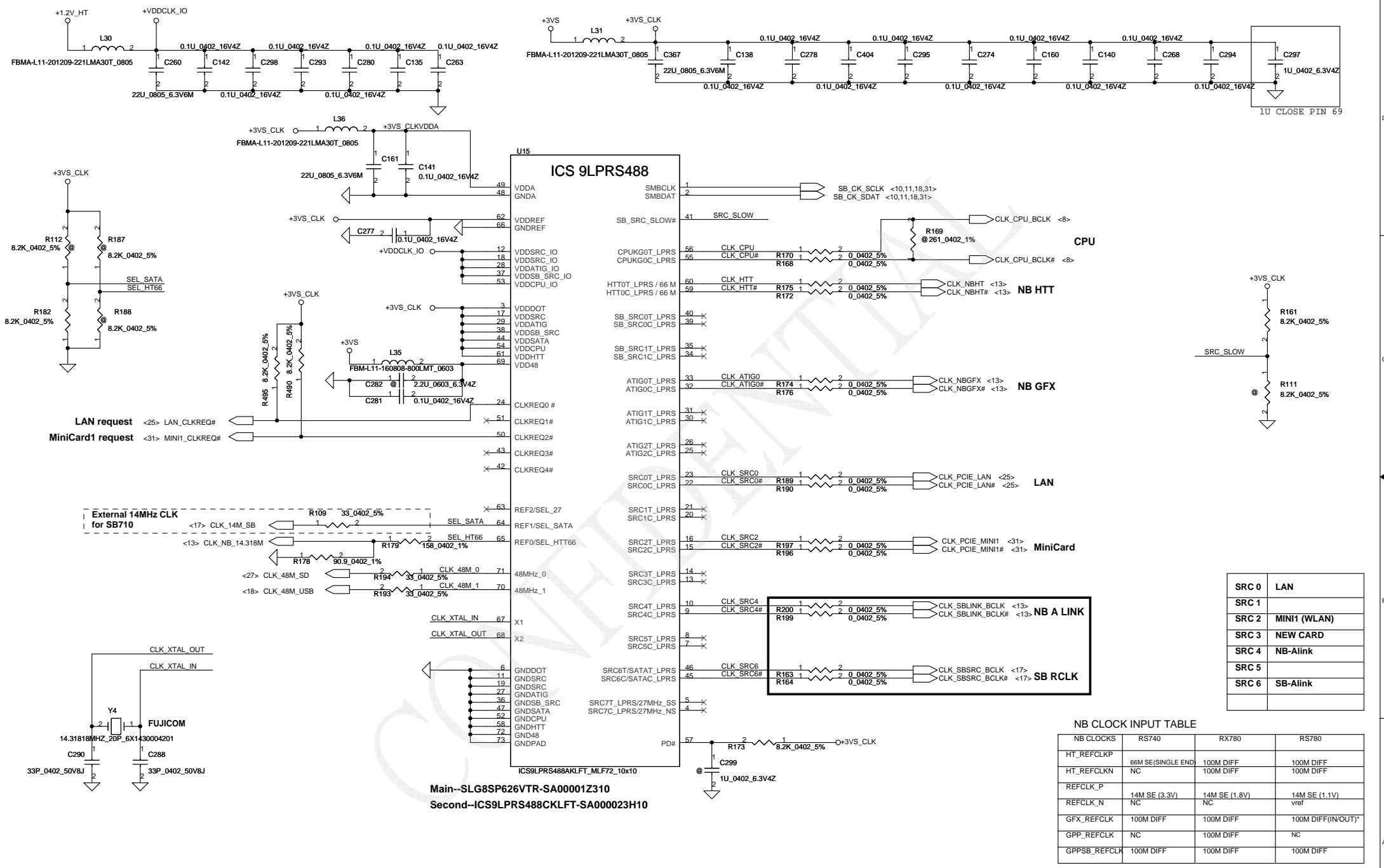


RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS780)
 1 : Disable(RS780)



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Main-SLG8SP626VTR-SA00001Z310
 Second-ICS9LPRS488CKLFT-SA000023H10

SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

NB CLOCK INPUT TABLE

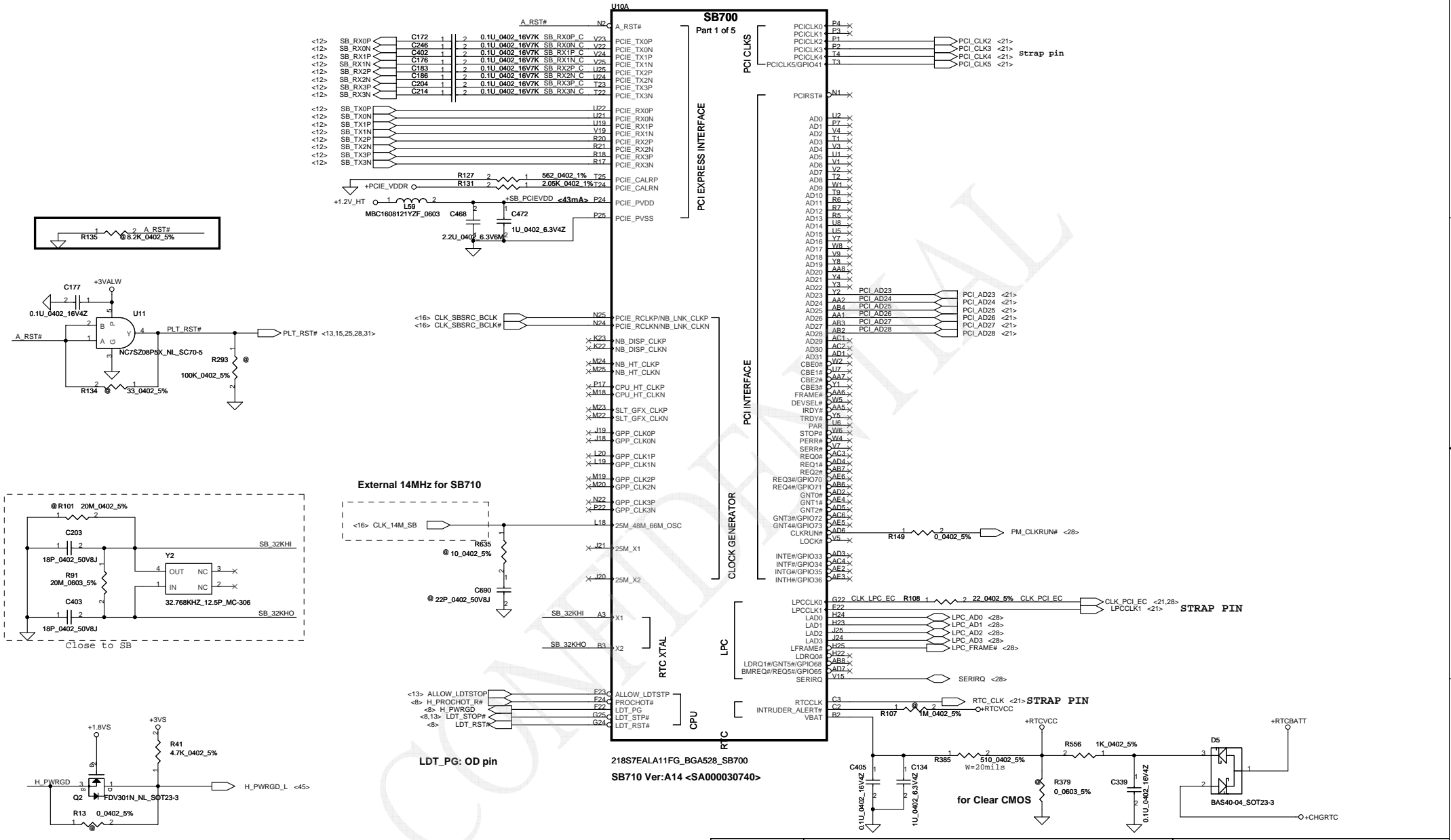
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P			
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

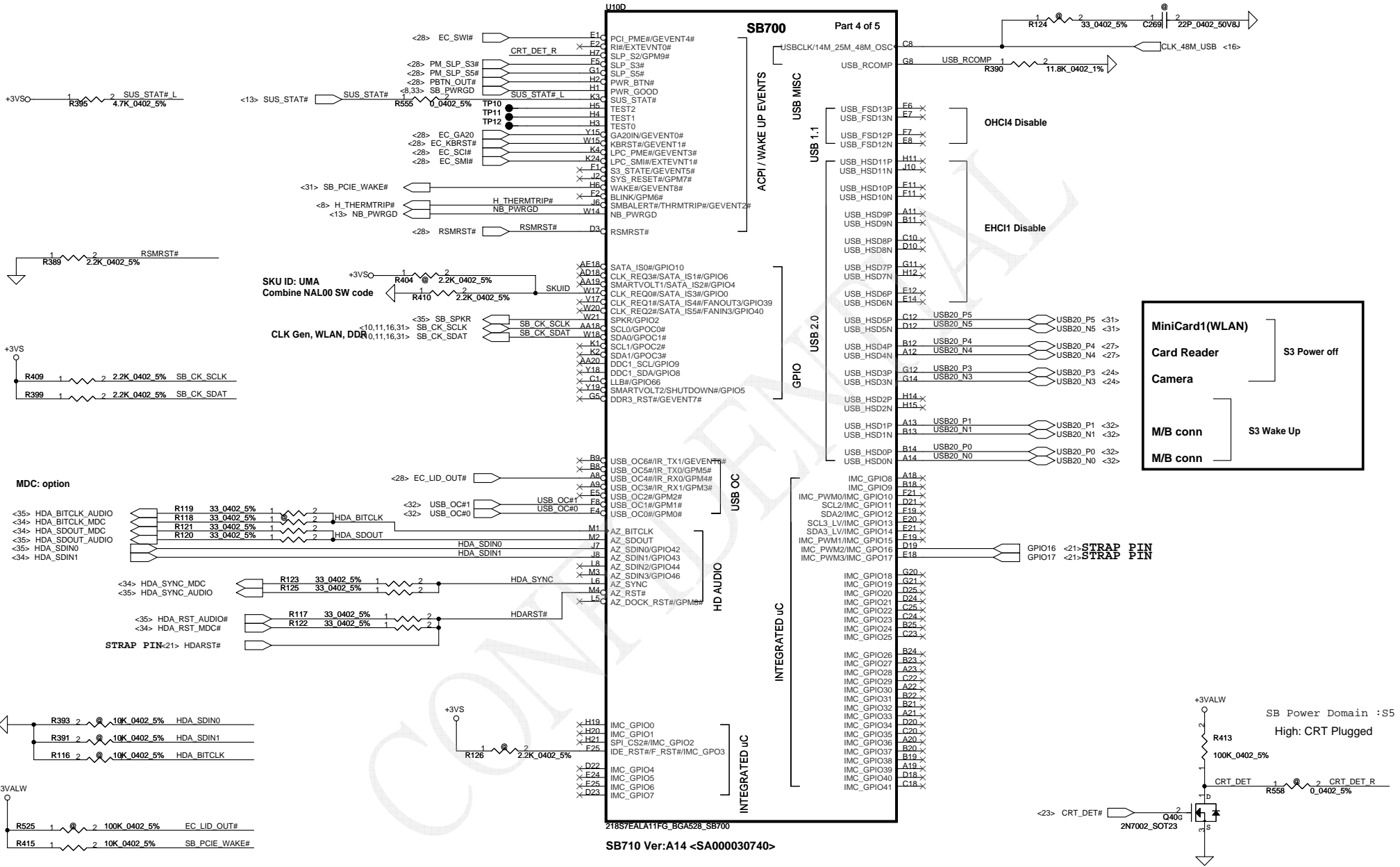
SEL_27M	1	configure as 27M and 27M_SS output
No used	0	configure as SRC_7 output

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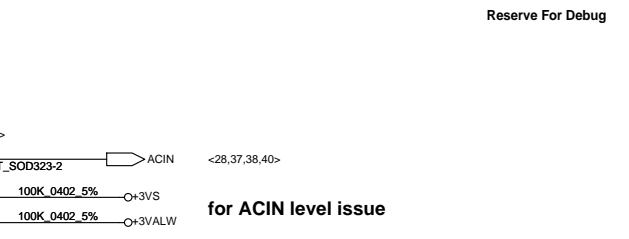
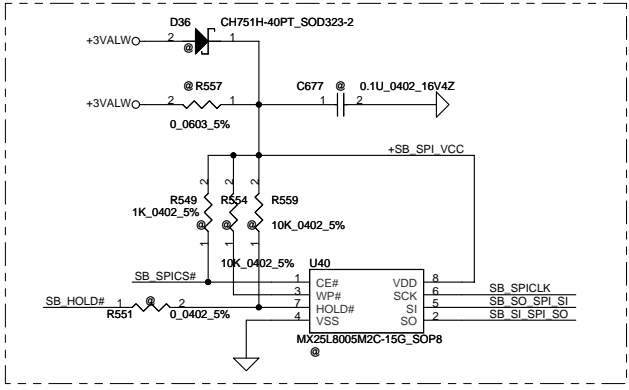
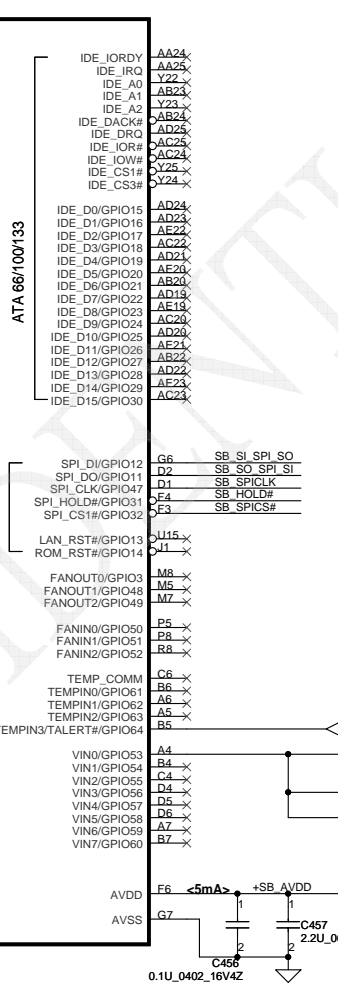
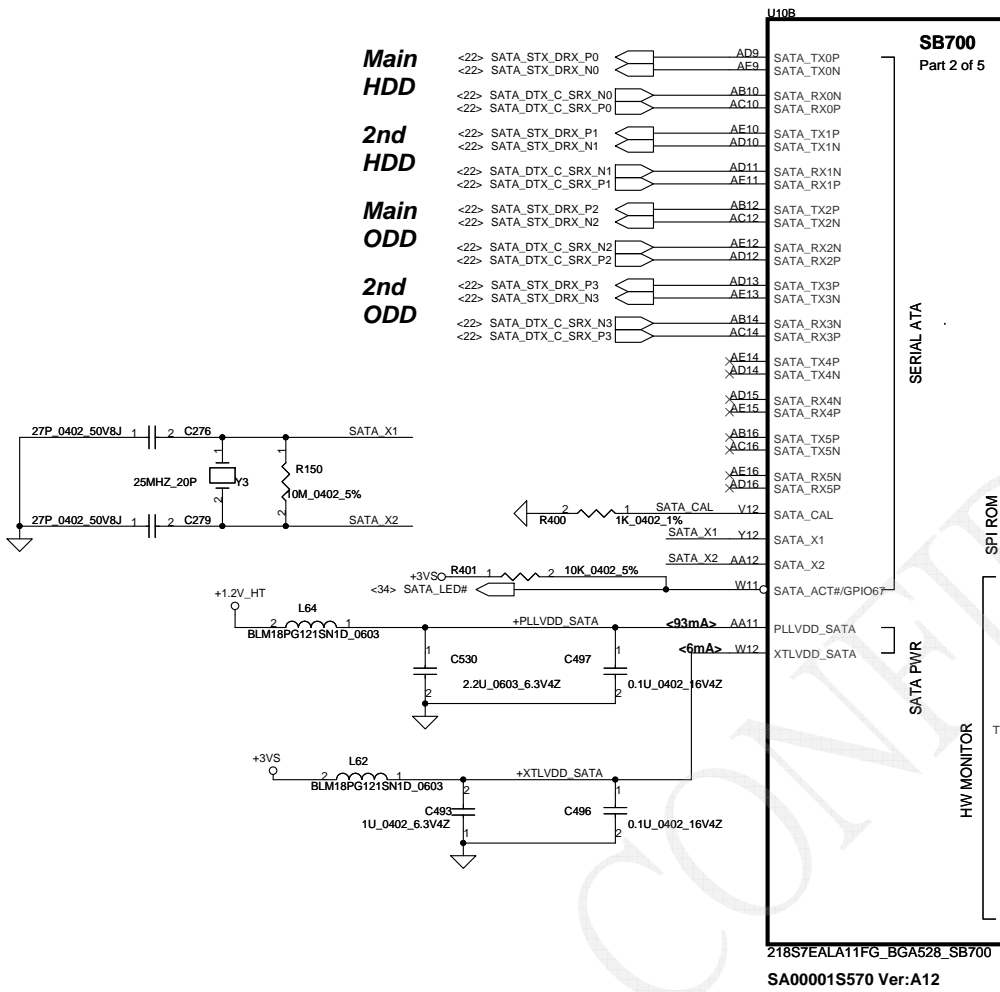
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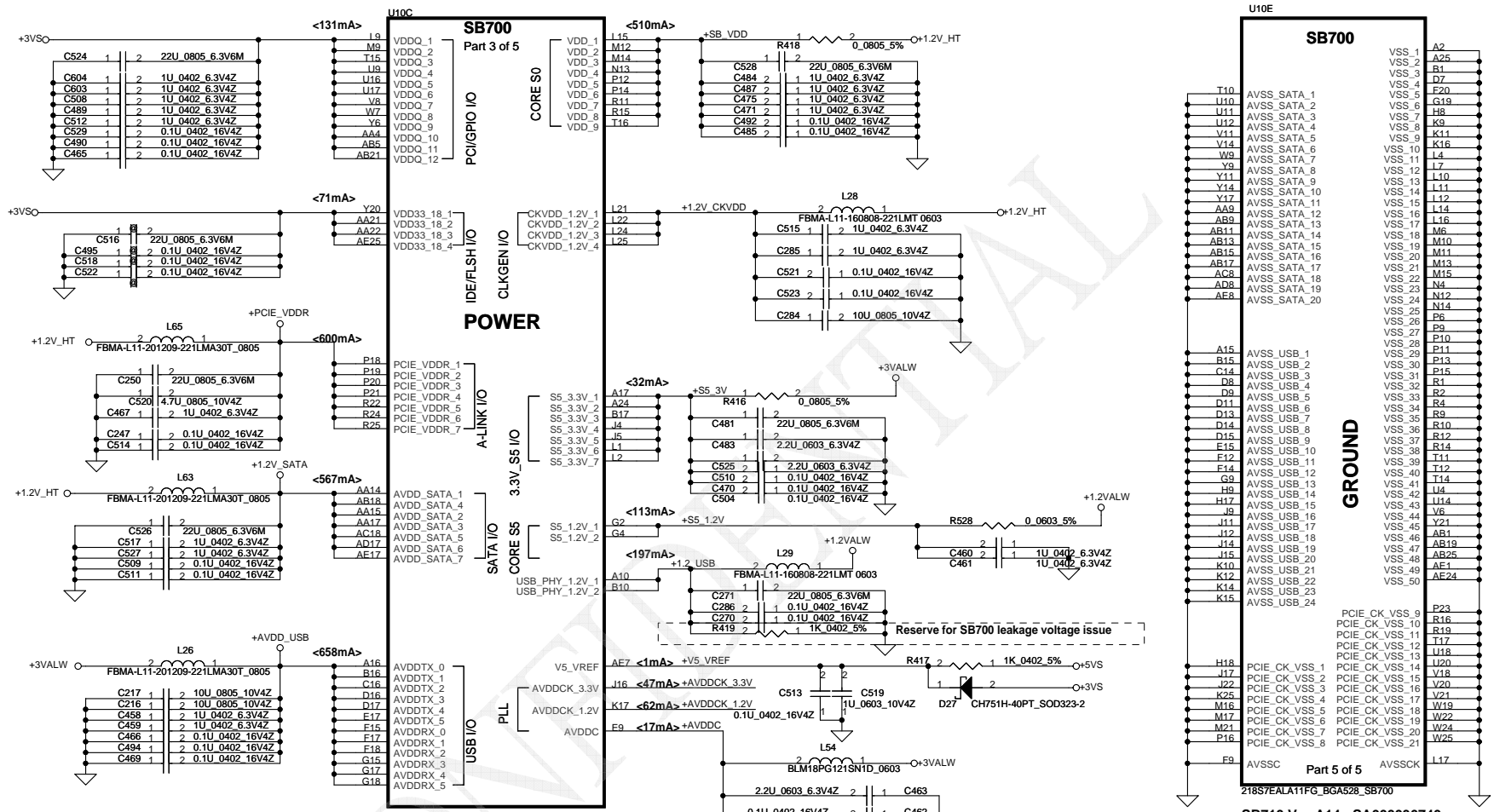


Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

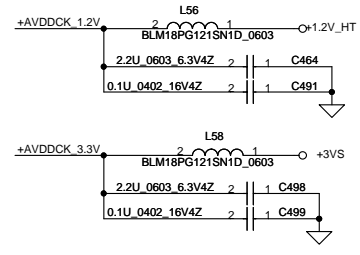


218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12

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218S7EAL11FG_BGA528_SB700
SB710 Ver:A14 <SA000030740>

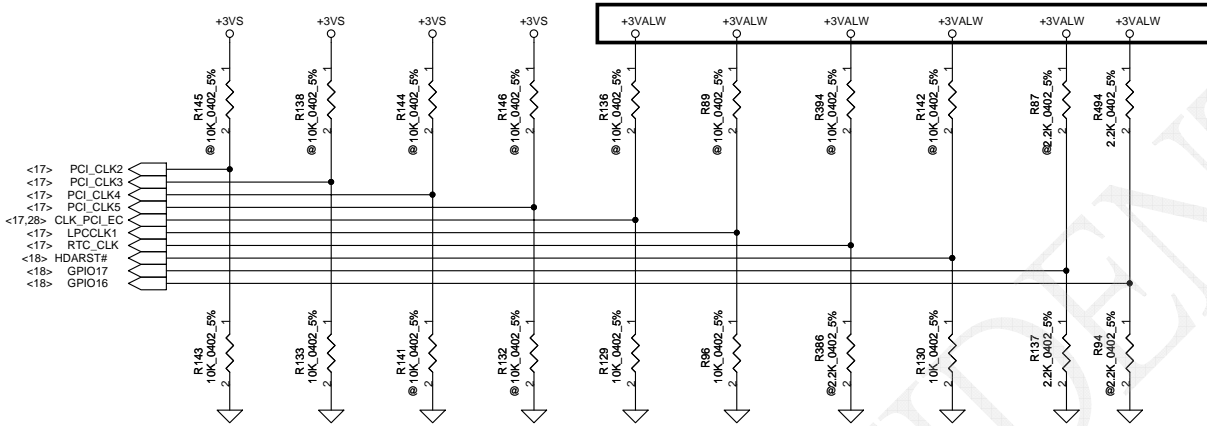


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	

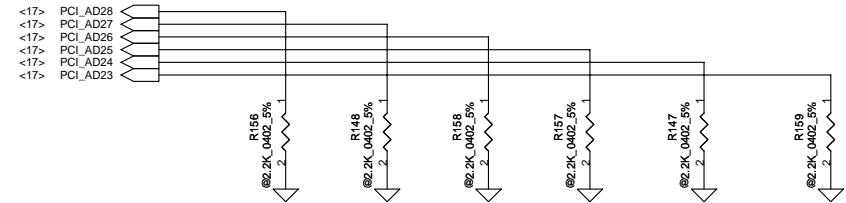


DEBUG STRAPS

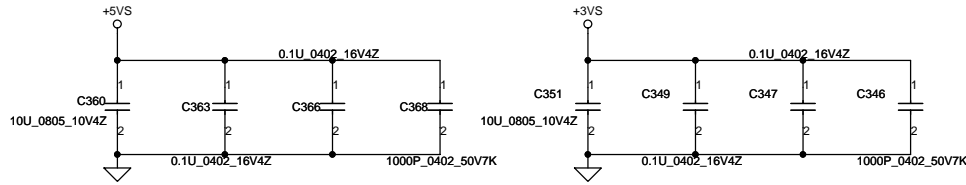
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

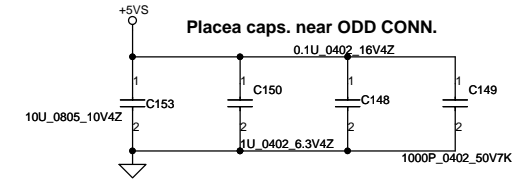
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



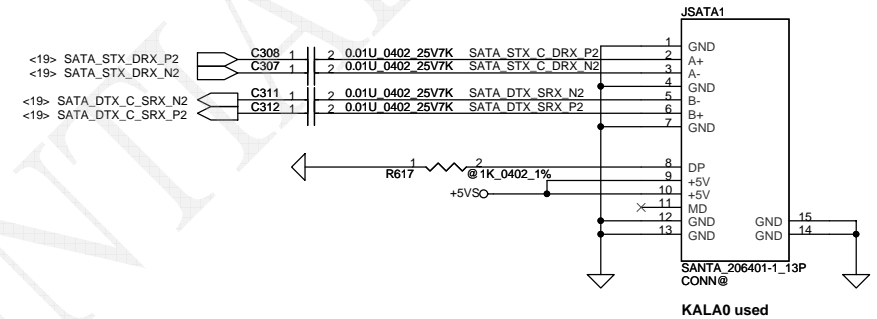
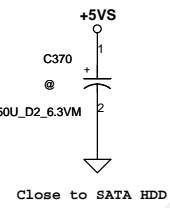
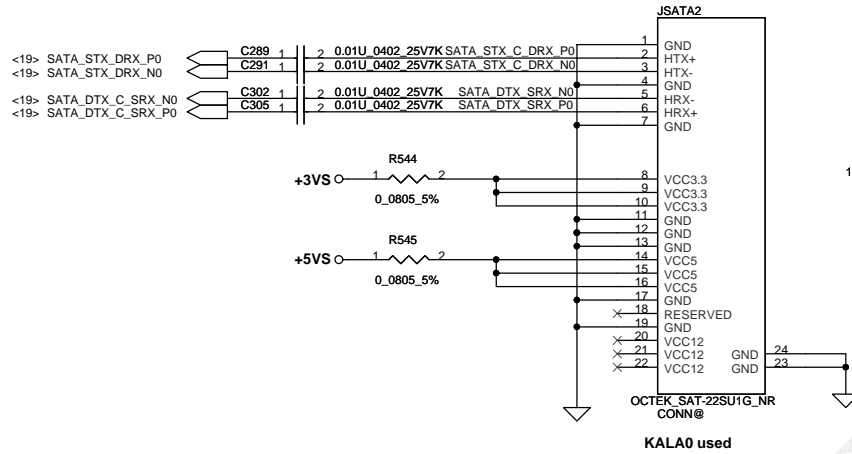
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SATA HDD CONN

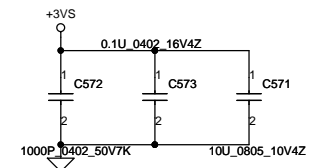
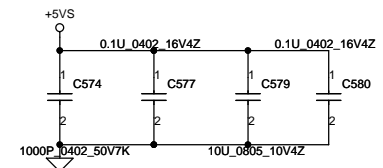
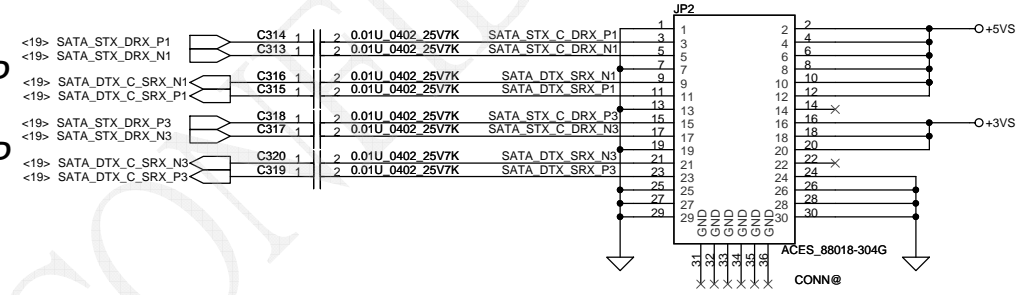


SATA ODD CONN



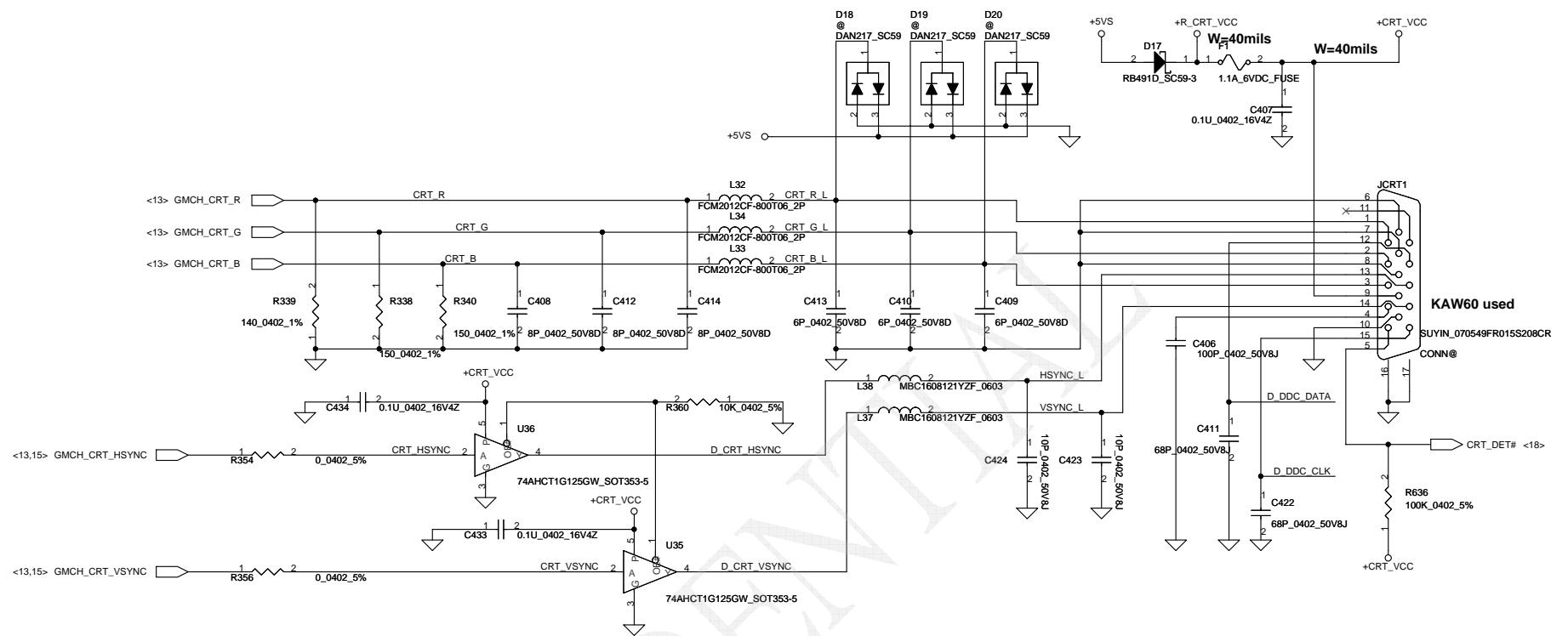
Second HDD

Second ODD

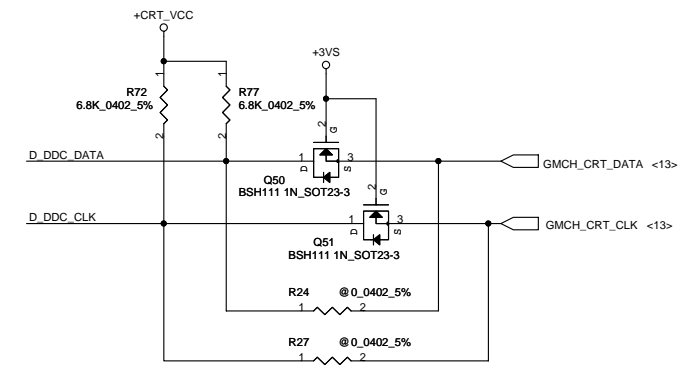


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CRT Connector



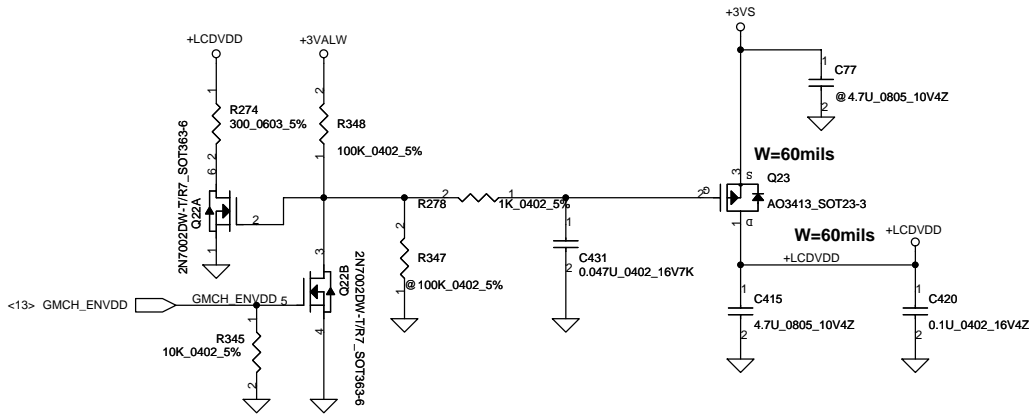
Close to Conn side



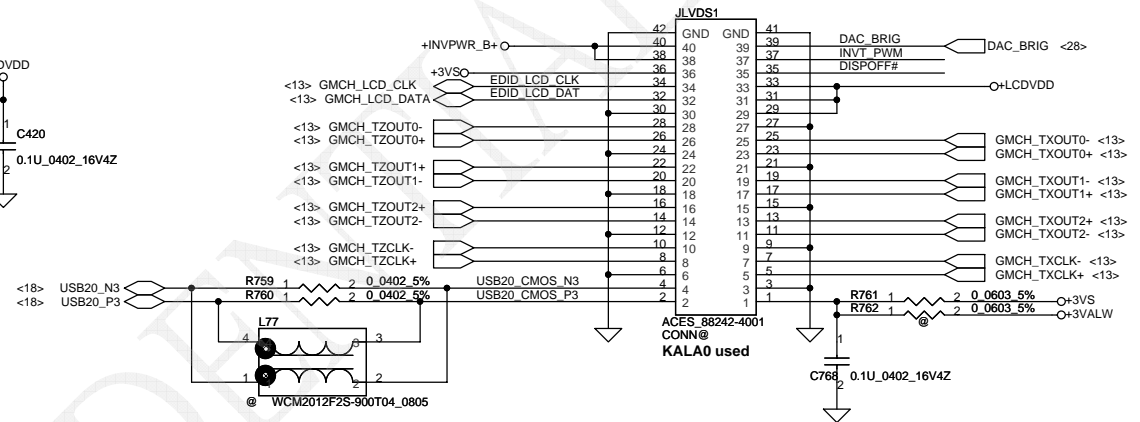
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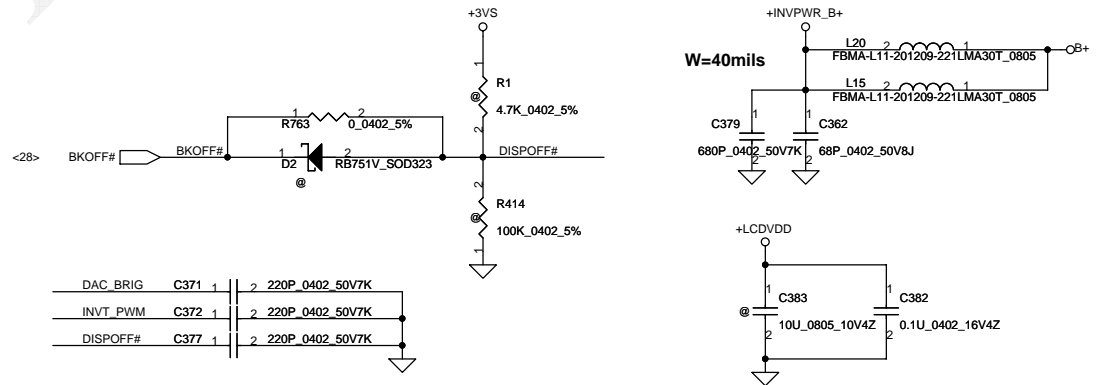
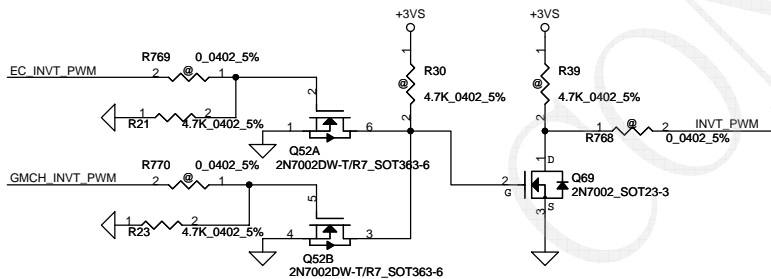
LCD POWER CIRCUIT



LCD/PANEL CONN.

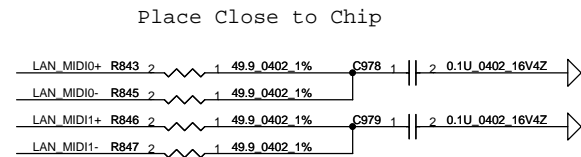
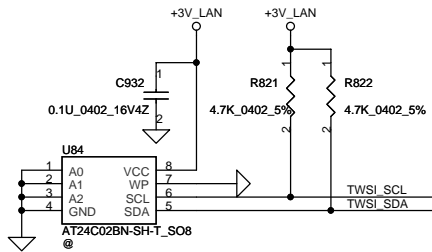
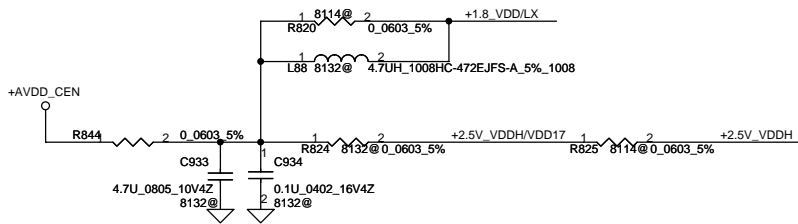


VARYBRIGHT FUNCTION

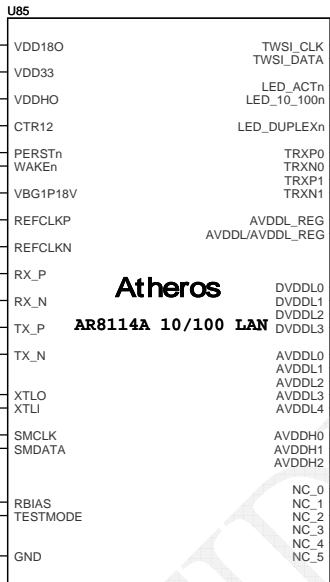
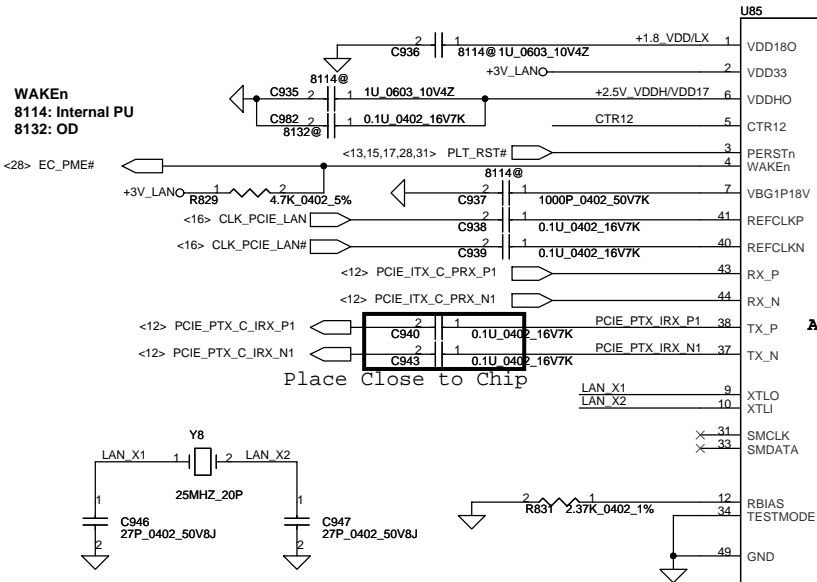


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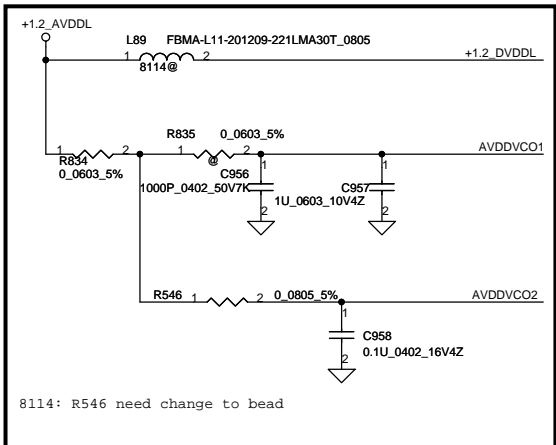
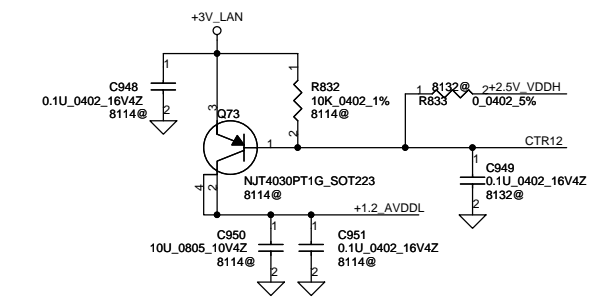
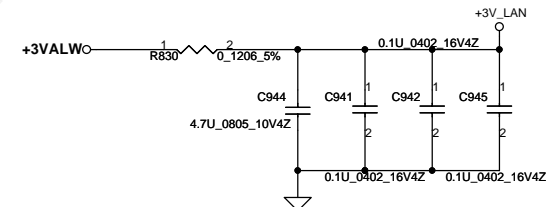
WAKEn
8114: Internal PU
8132: OD



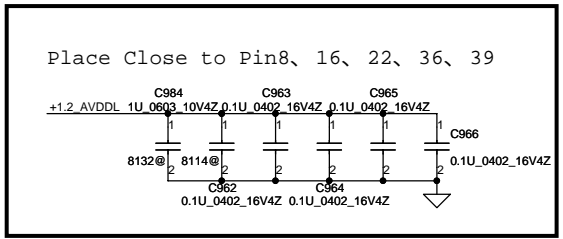
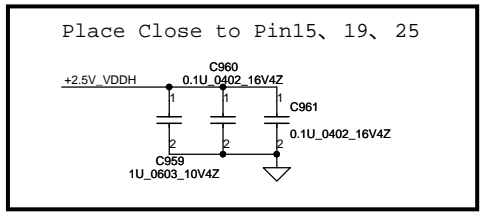
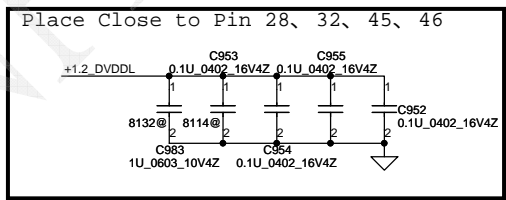
change to AR8132L-AL1E

Place Close to Chip

Layout Notice : Close to chip

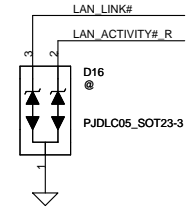
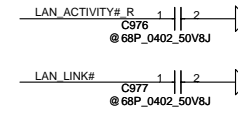
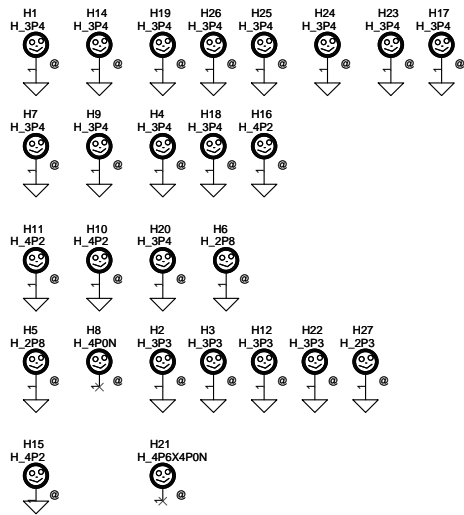
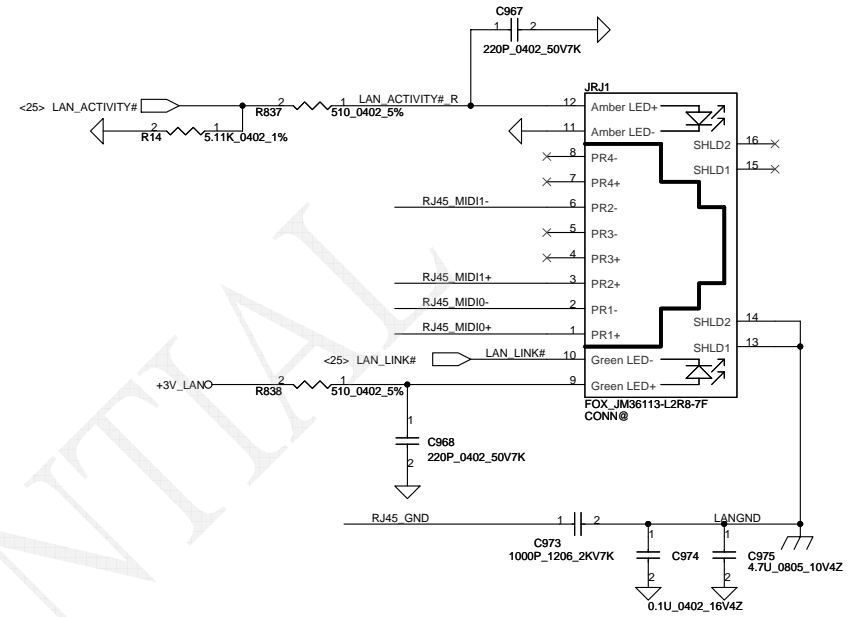
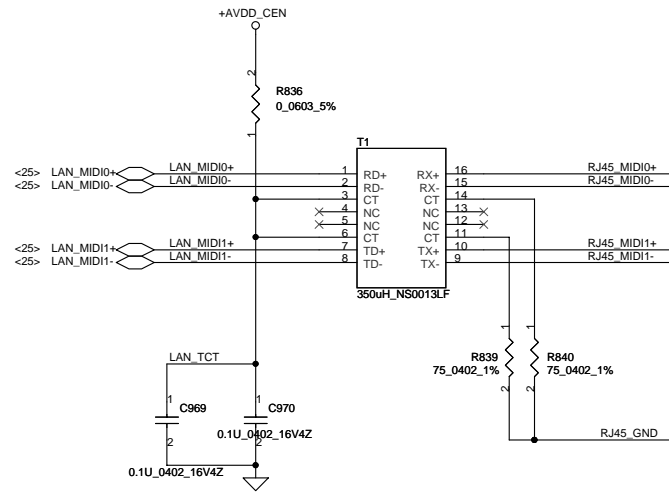


8114: R546 need change to bead

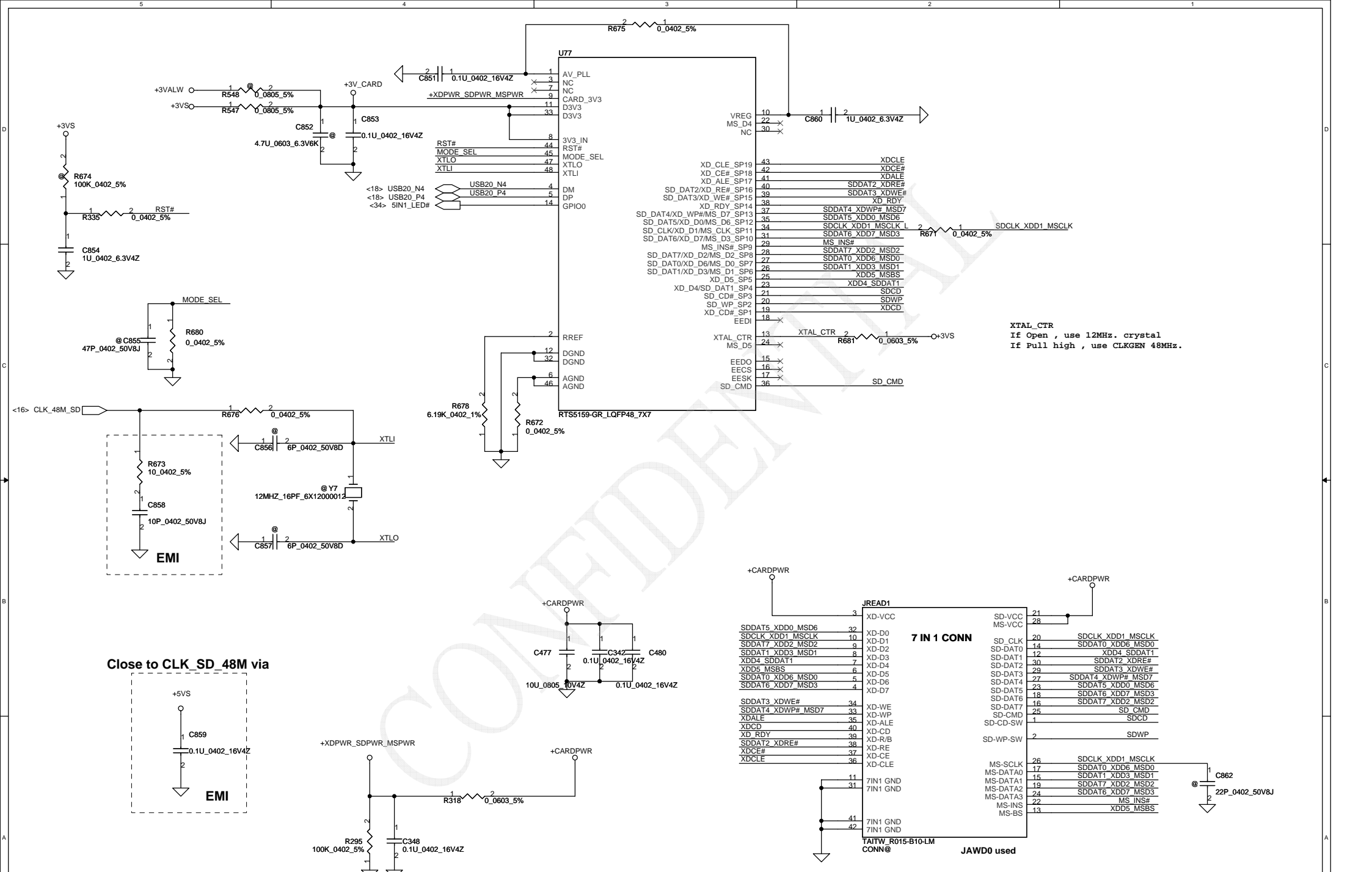


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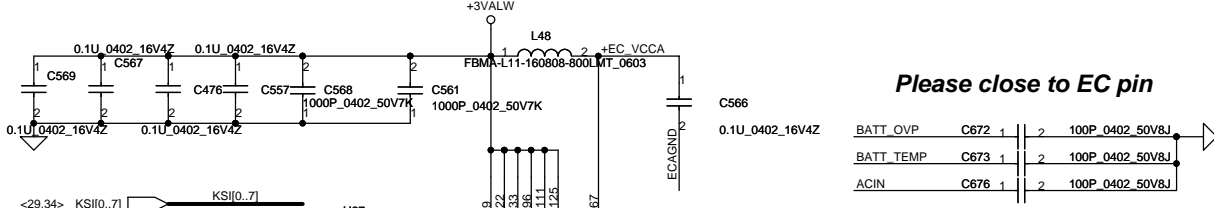
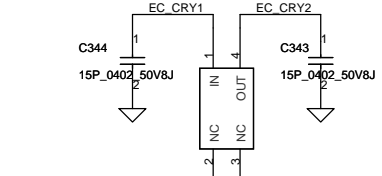
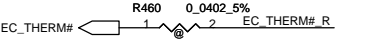
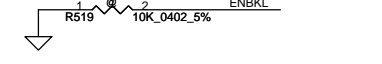
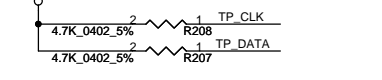
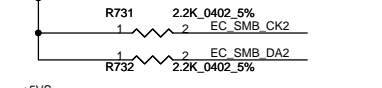
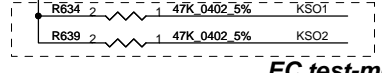
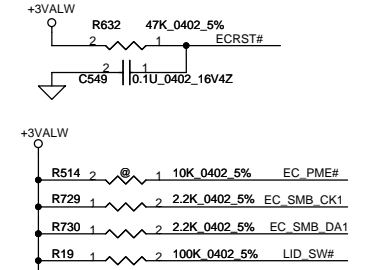
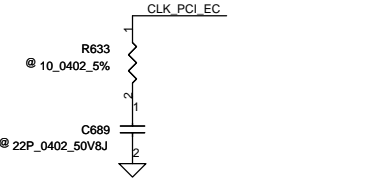
XTAL_CTR
If Open, use 12MHz. crystal
If Pull high, use CLKGEN 48MHz.

Close to CLK_SD 48M via

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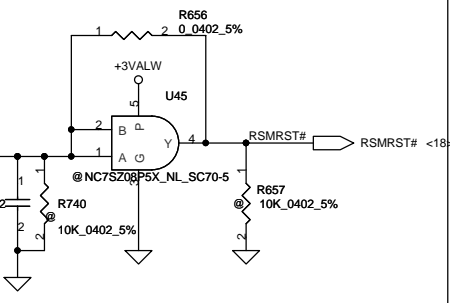
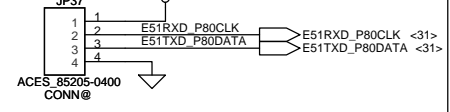
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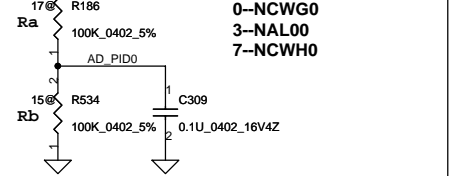
Please close to EC pin

For EC Tools

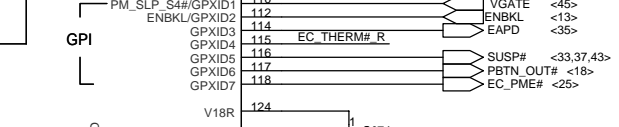
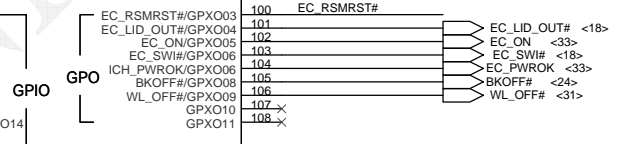
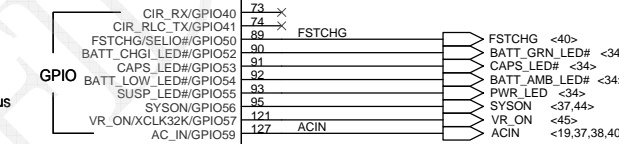
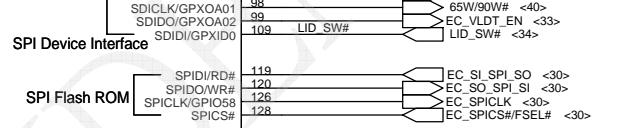
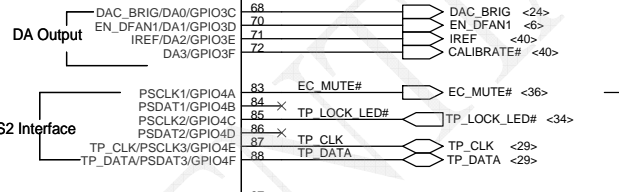
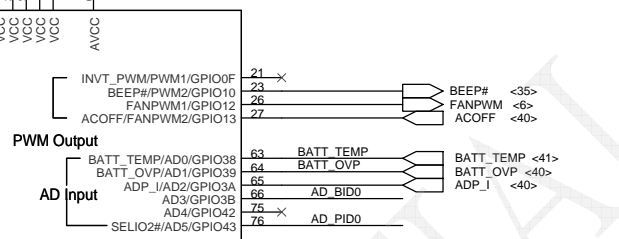
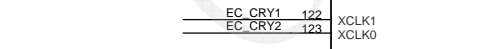
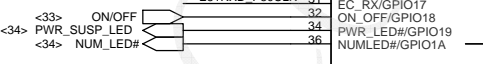
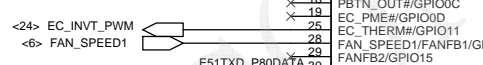
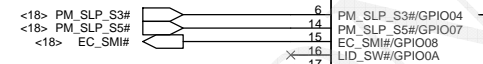
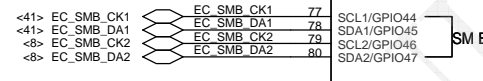
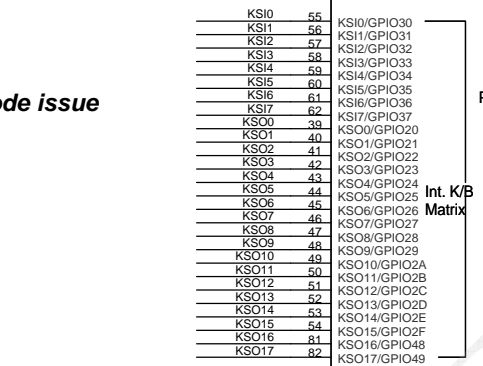
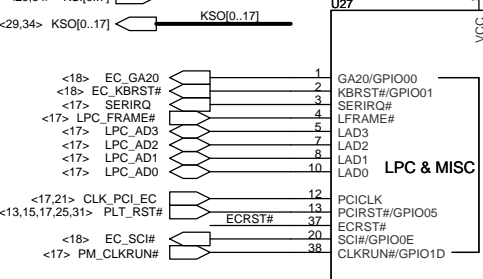
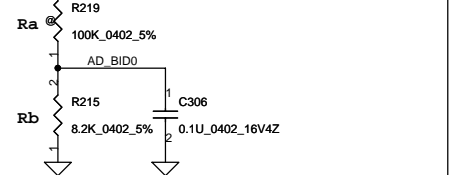
Place on MiniCard



Project ID
Please see page 3.



Board ID <VB support>
Please see page 3.

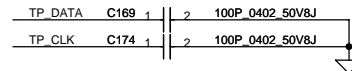
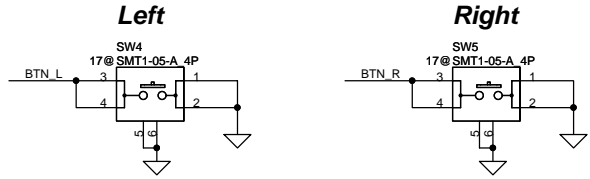


Chagne to D3 version

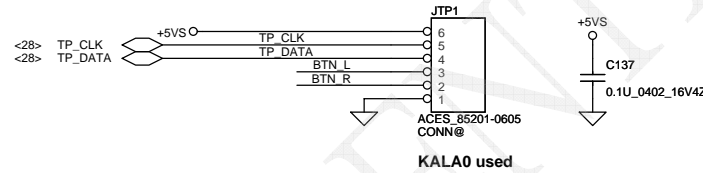
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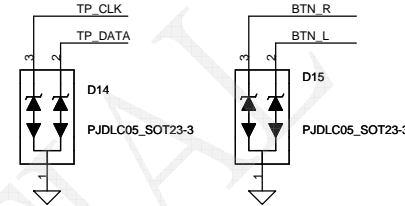
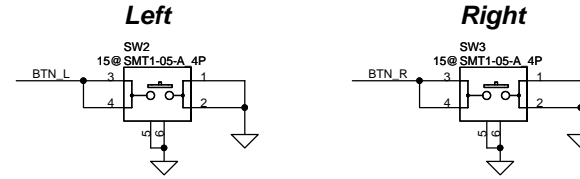
For 17"



To TP/B Conn.

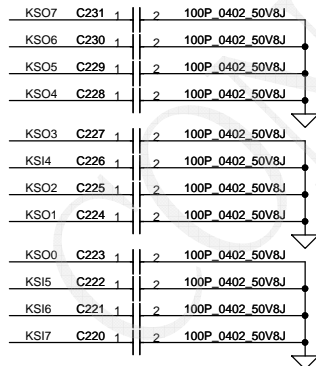
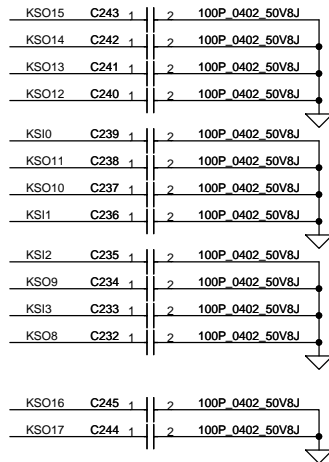


For 15"

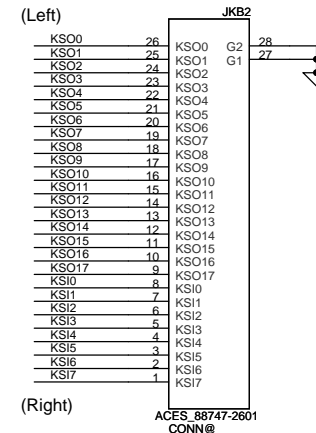
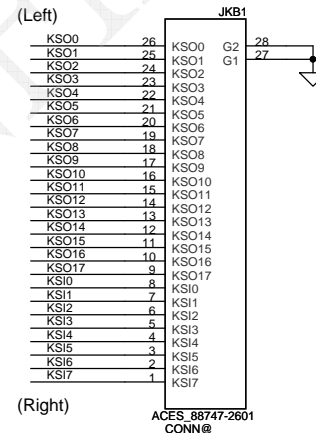


Change to SCA00000200

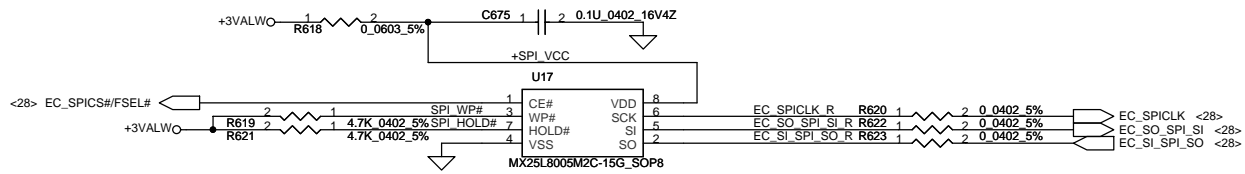
INT_KBD Conn.



KB1 for 15"
KB2 for 17"

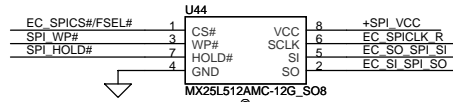
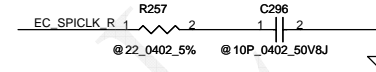


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SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

ONLY MXIC used in this project (66MHz)

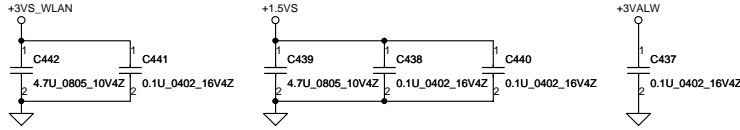


Reserved for BIOS simulator.
 Footprint SO8
 SPI ROM Footprint 150mil

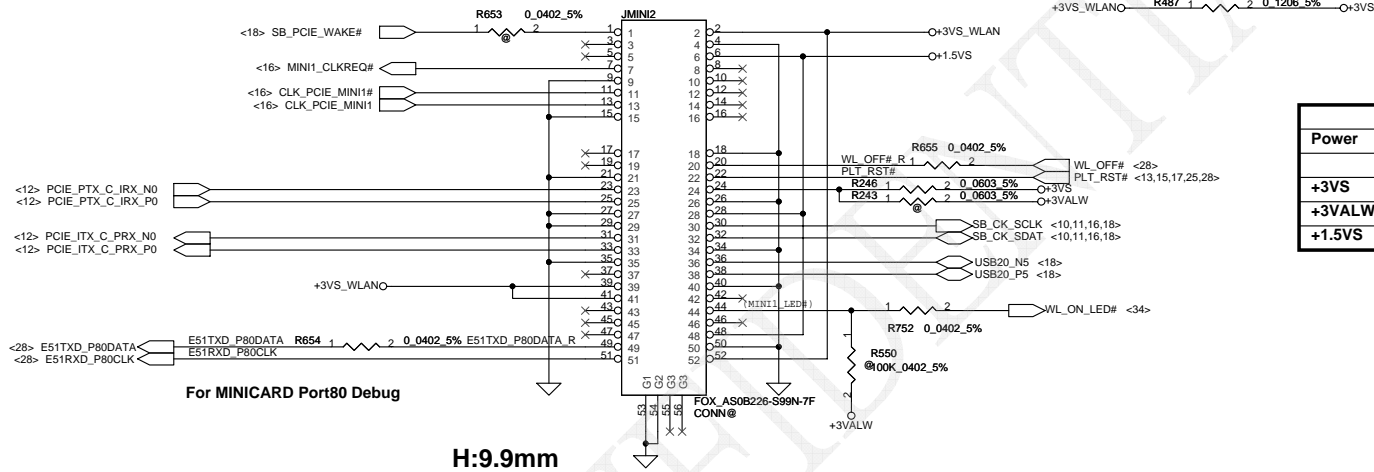
CONFIDENTIAL

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For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

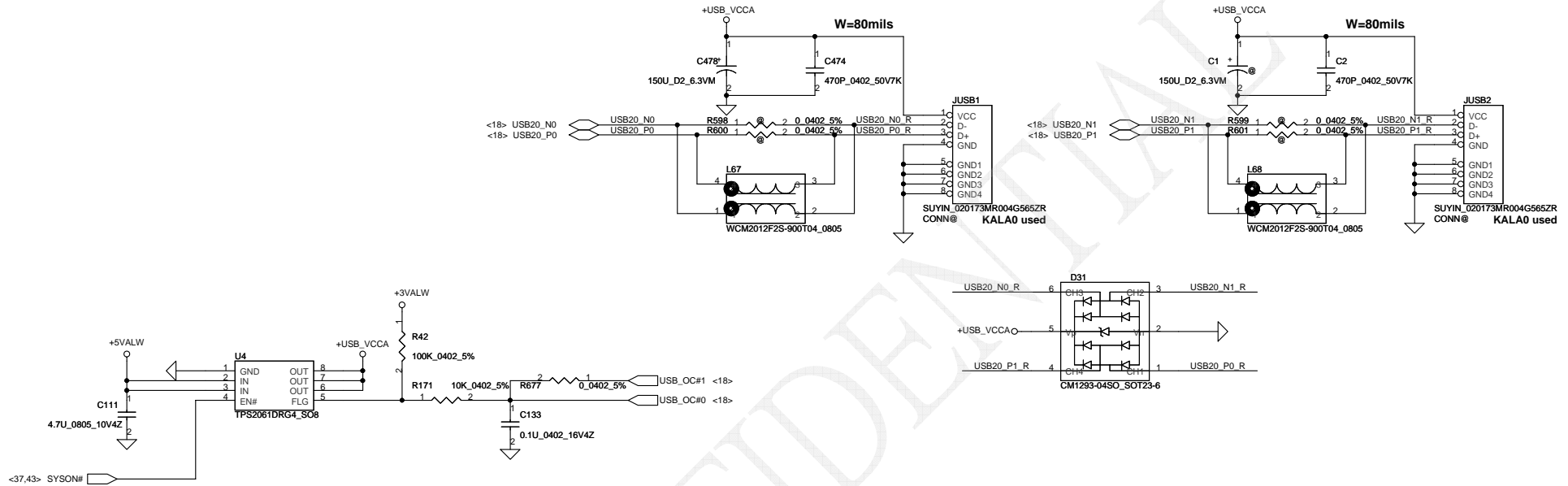
For MINICARD Port80 Debug

H:9.9mm

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USB CONN. 1 & 2

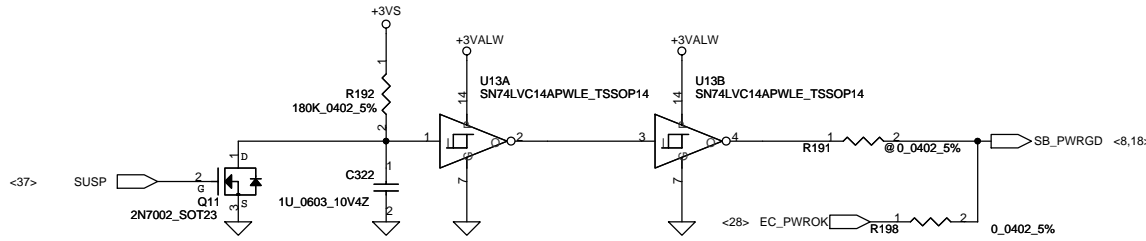


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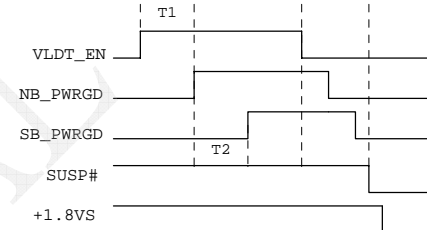
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Power ON Circuit

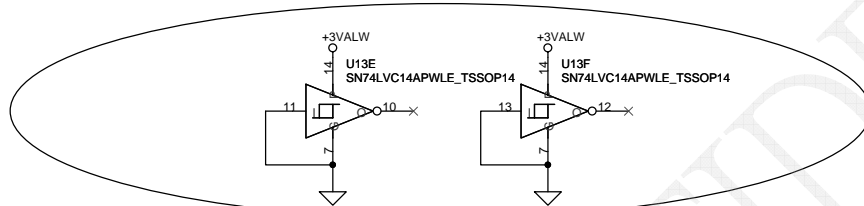
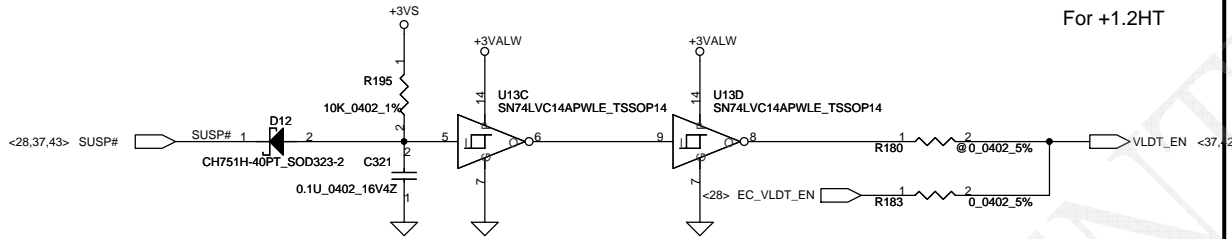
For South Bridge



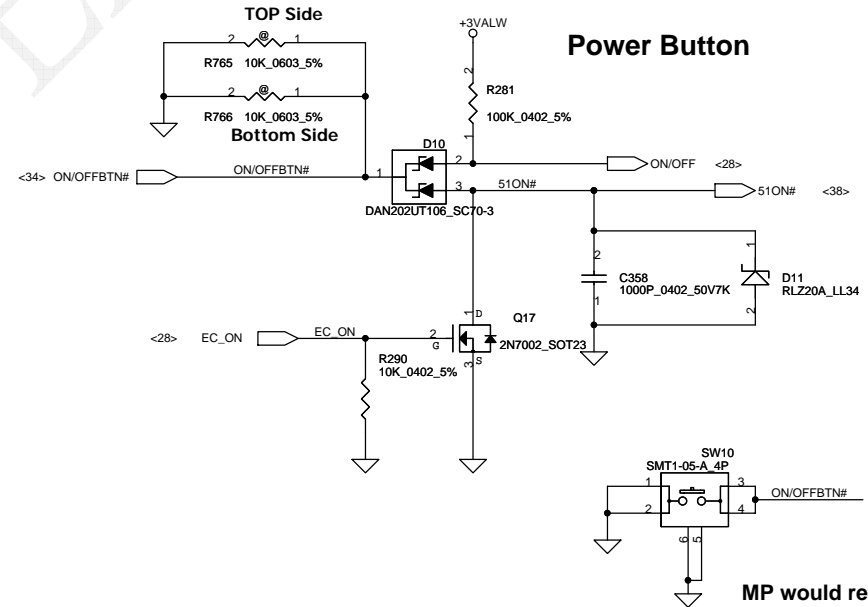
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



For +1.2HT

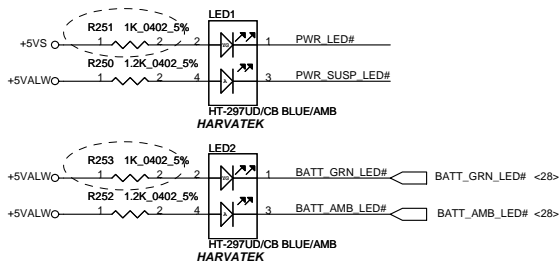
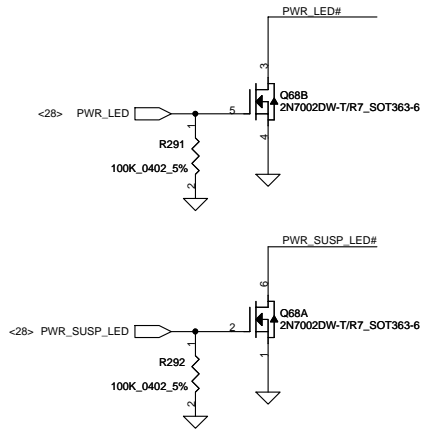


Power Button

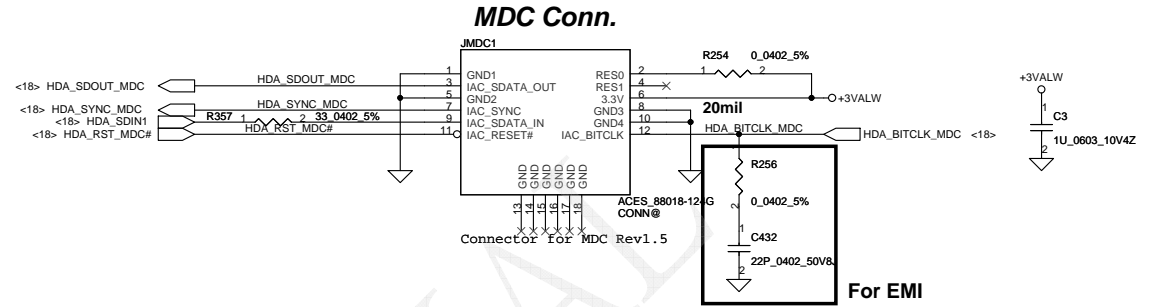


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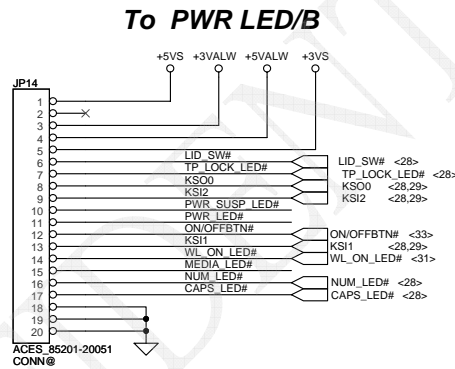
www.vinafx.vn



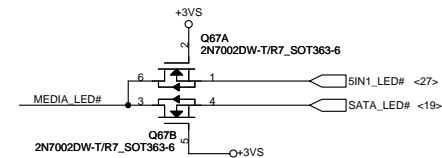
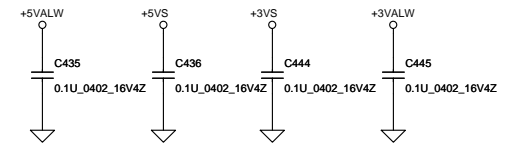
BLUE/AMB LED



For EMI

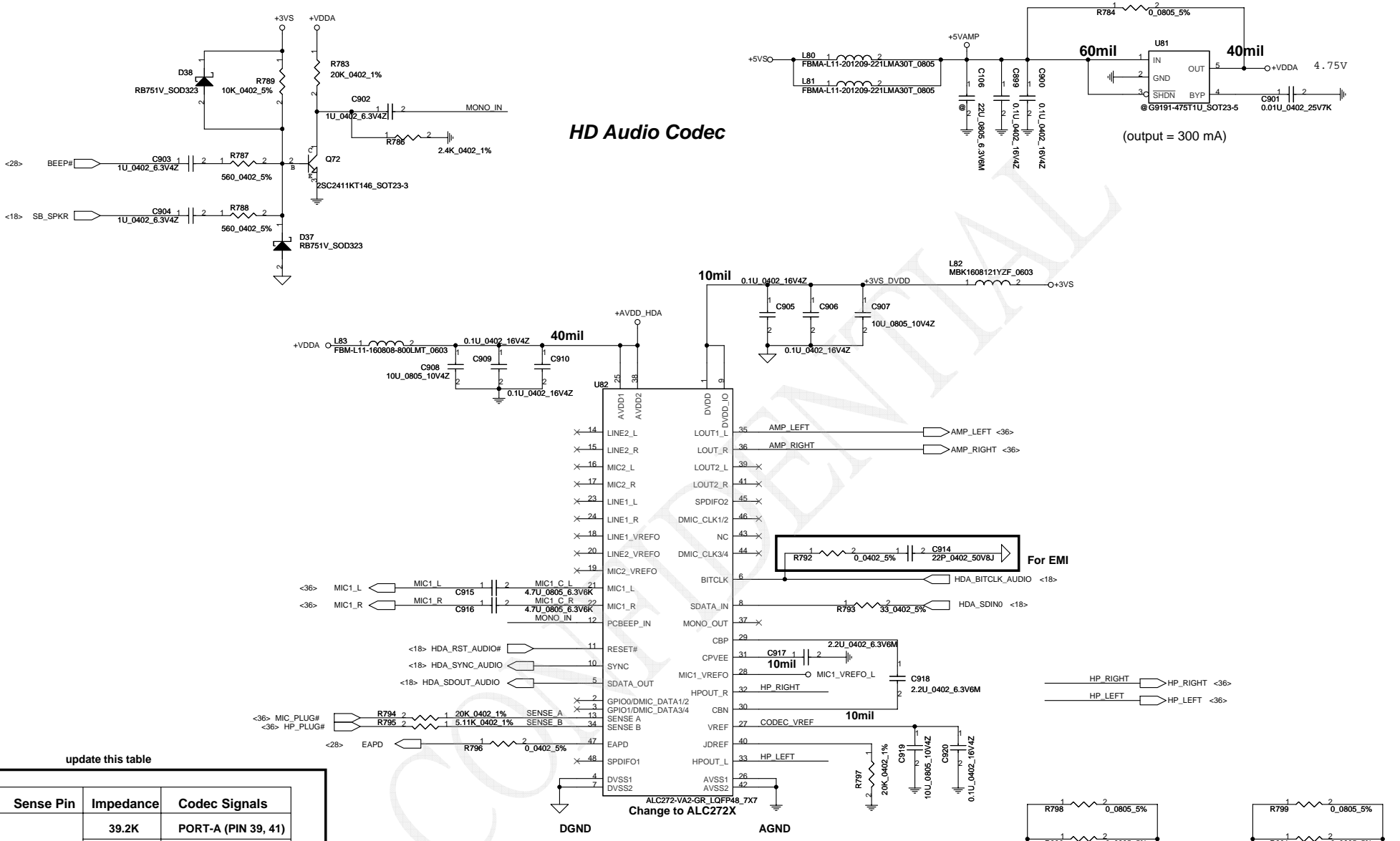


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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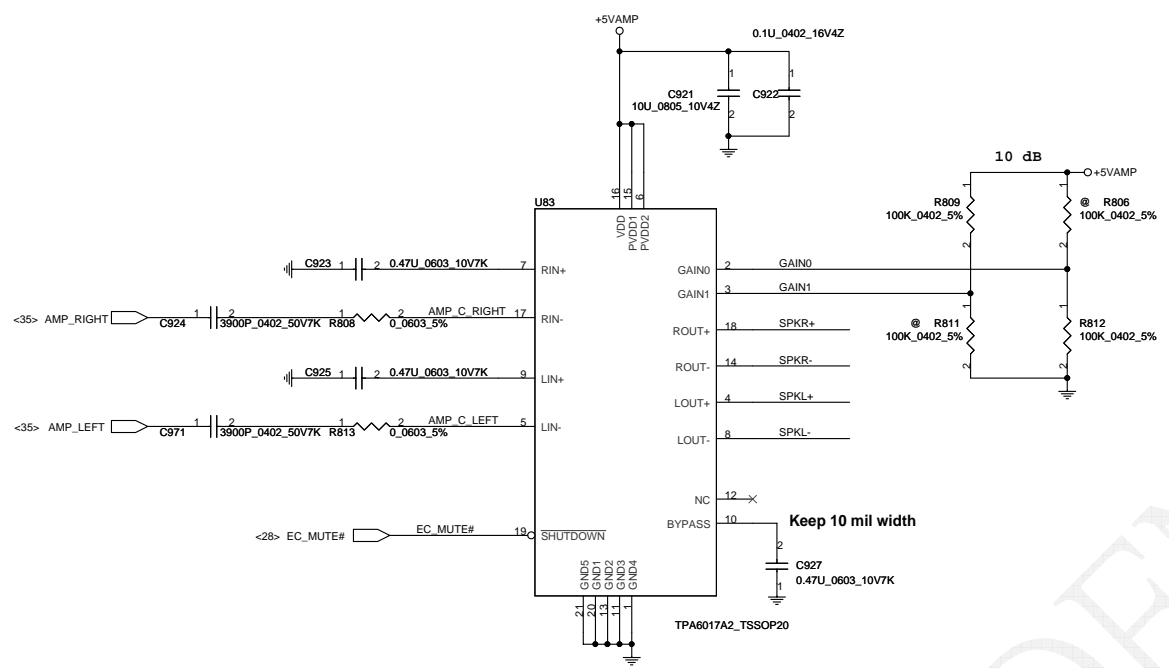
HD Audio Codec



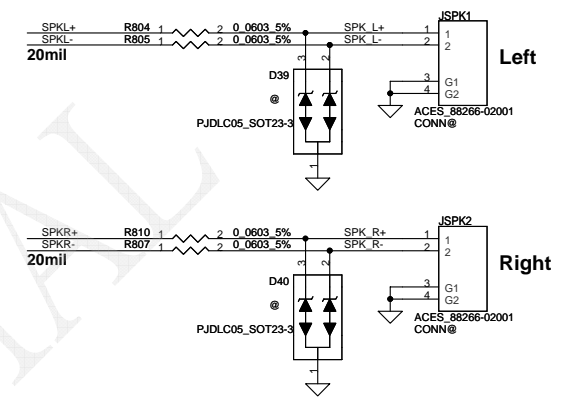
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

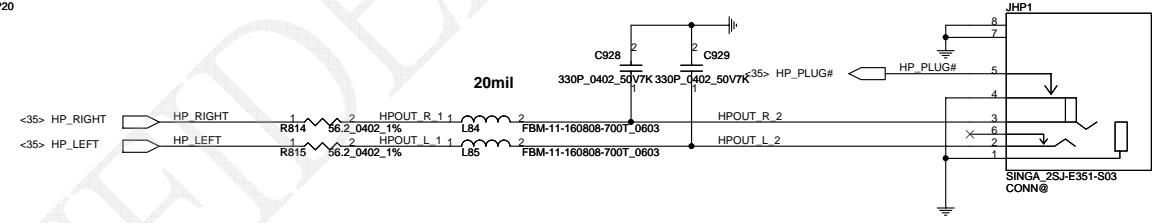
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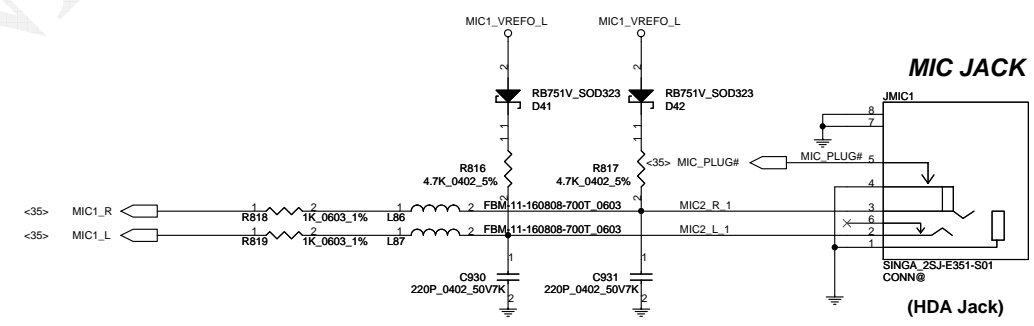
Int. Speaker Conn.



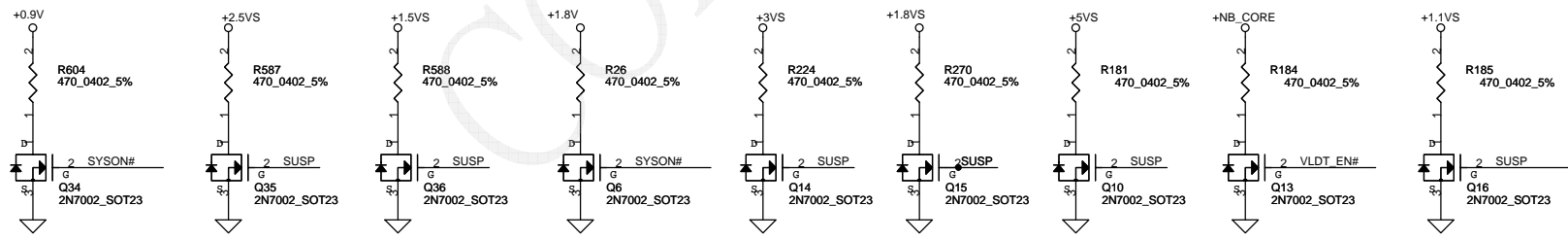
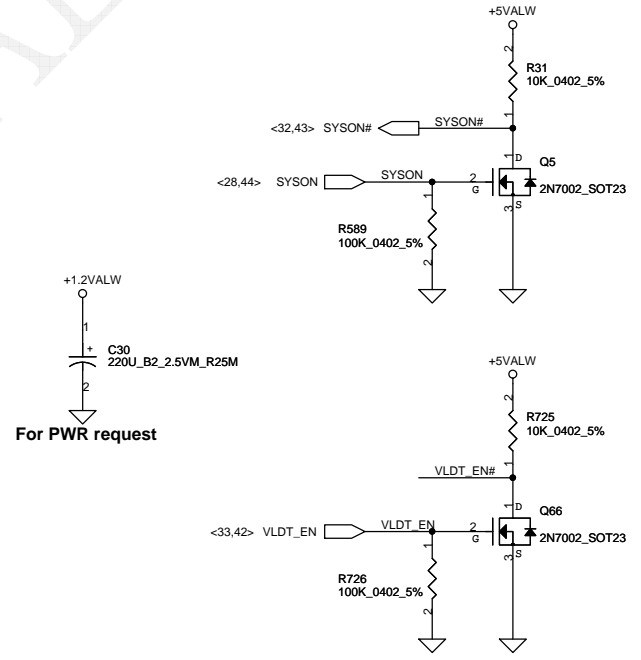
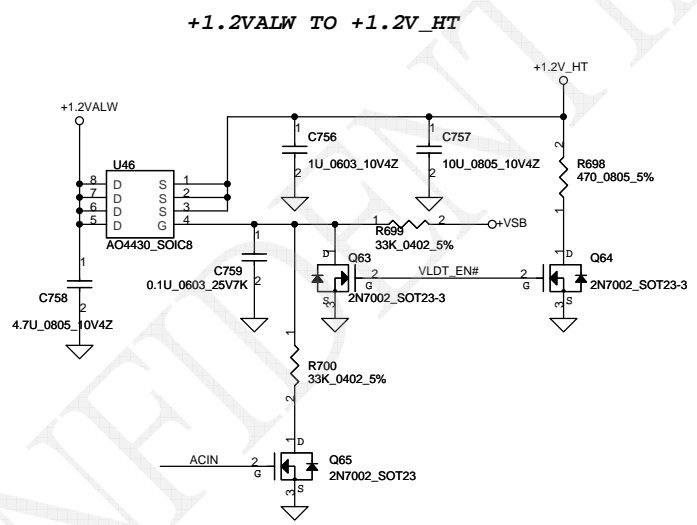
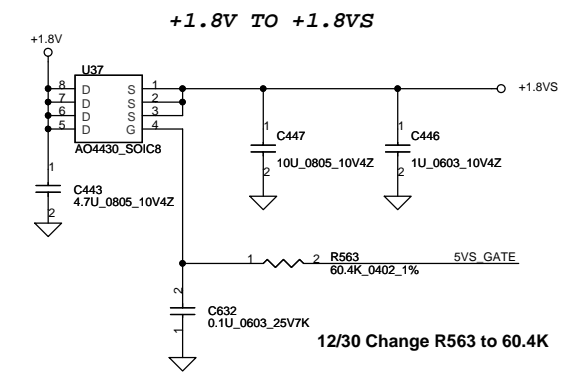
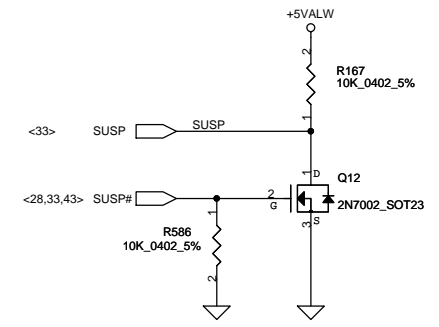
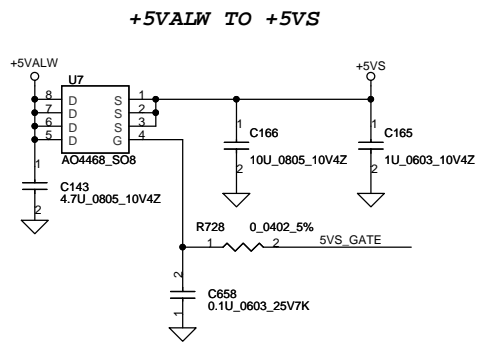
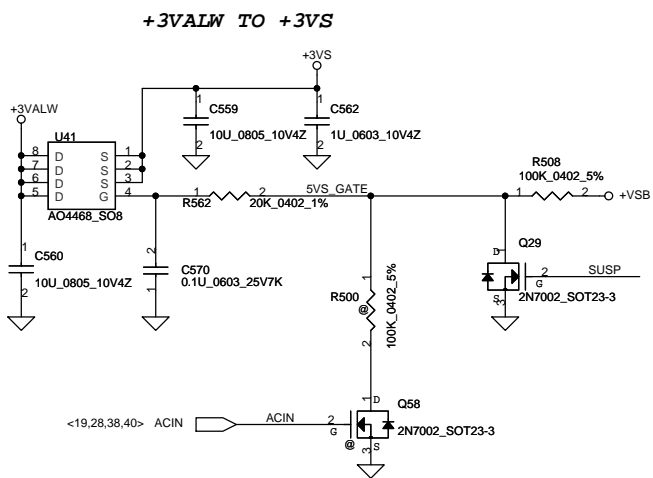
LINE Out/Headphone Out



MIC JACK



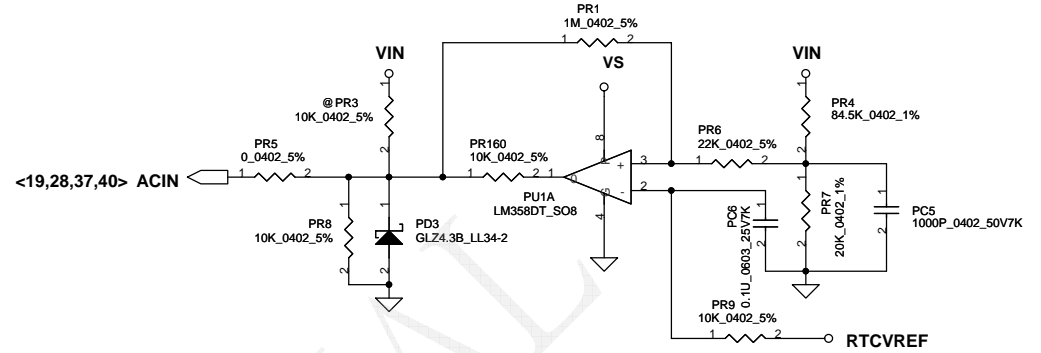
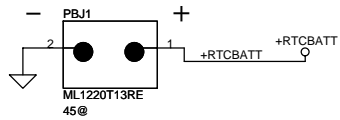
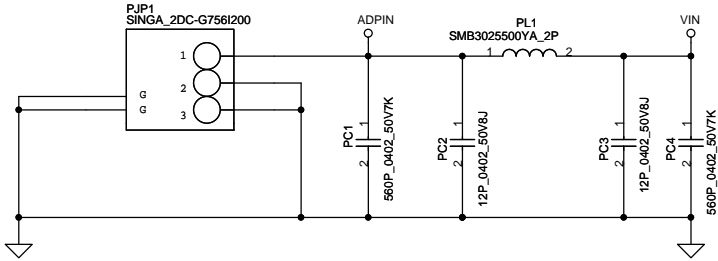
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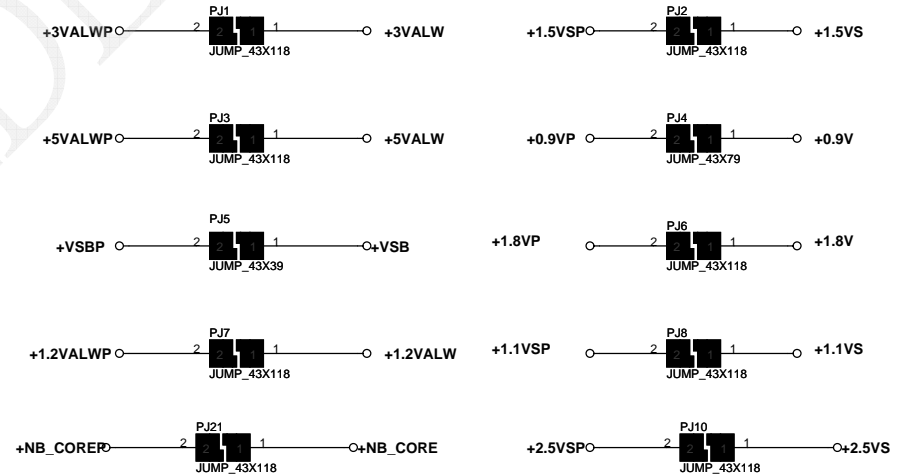
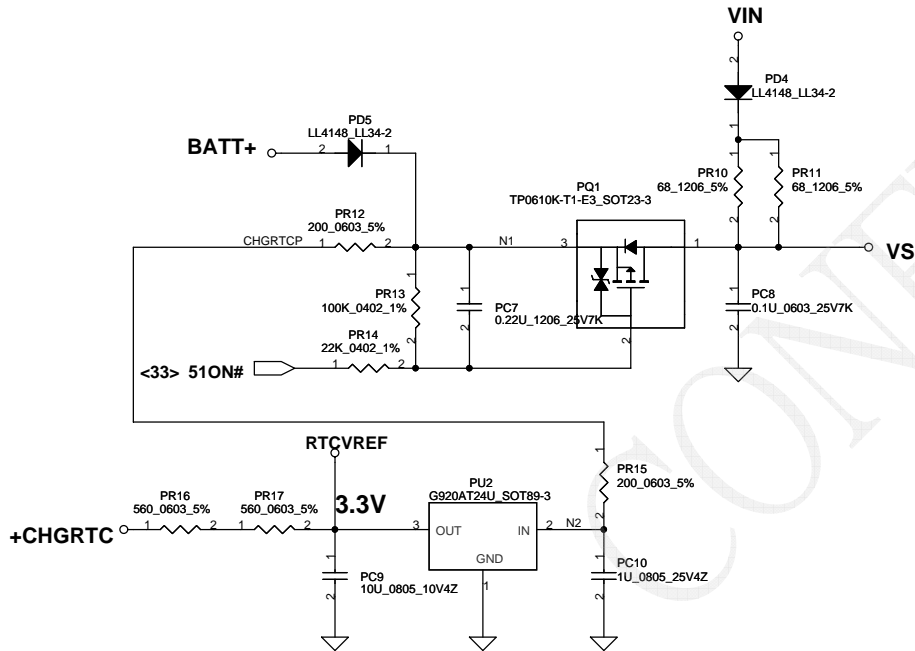
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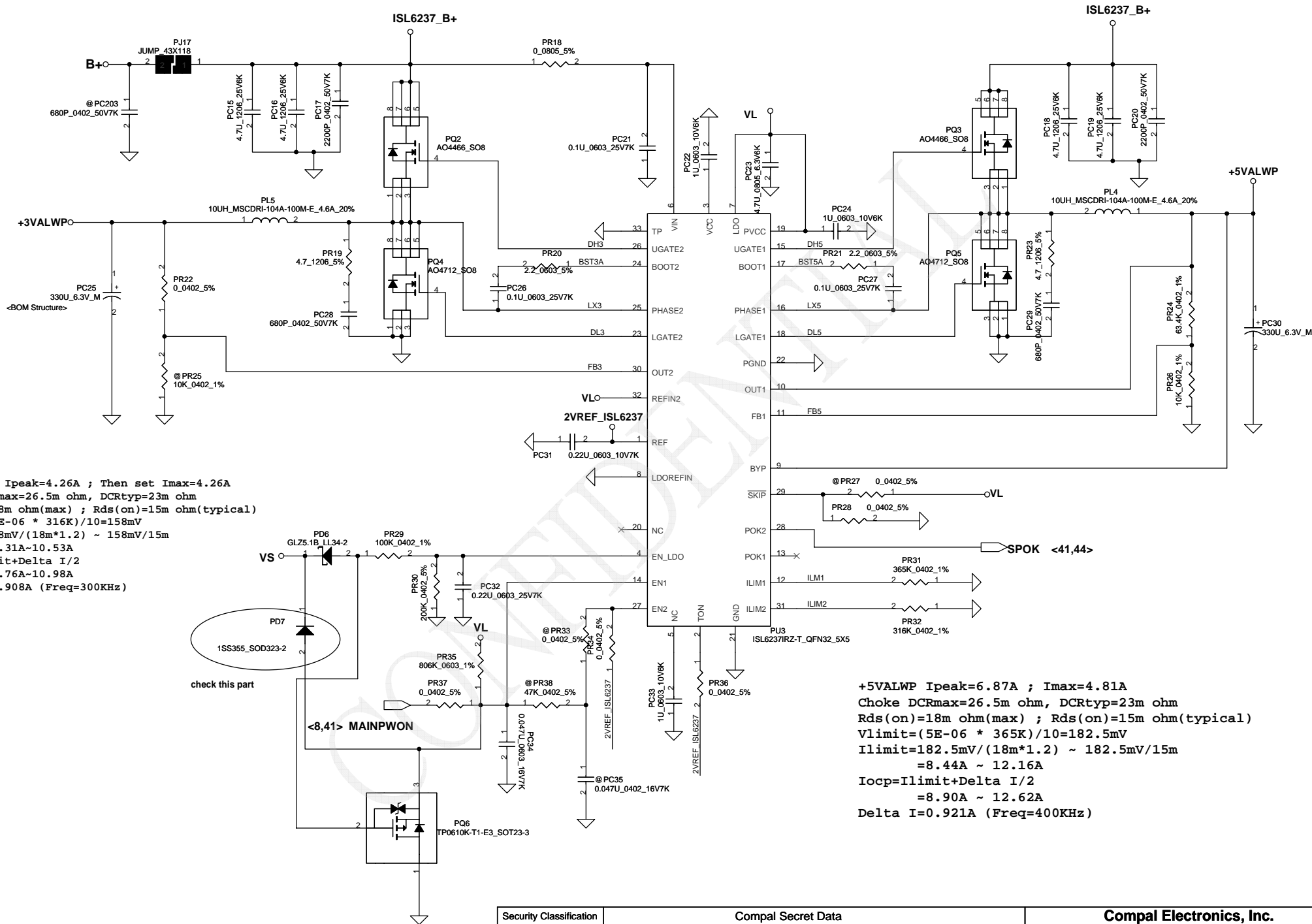


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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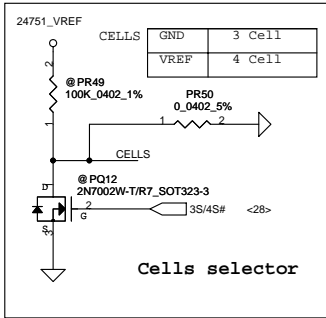
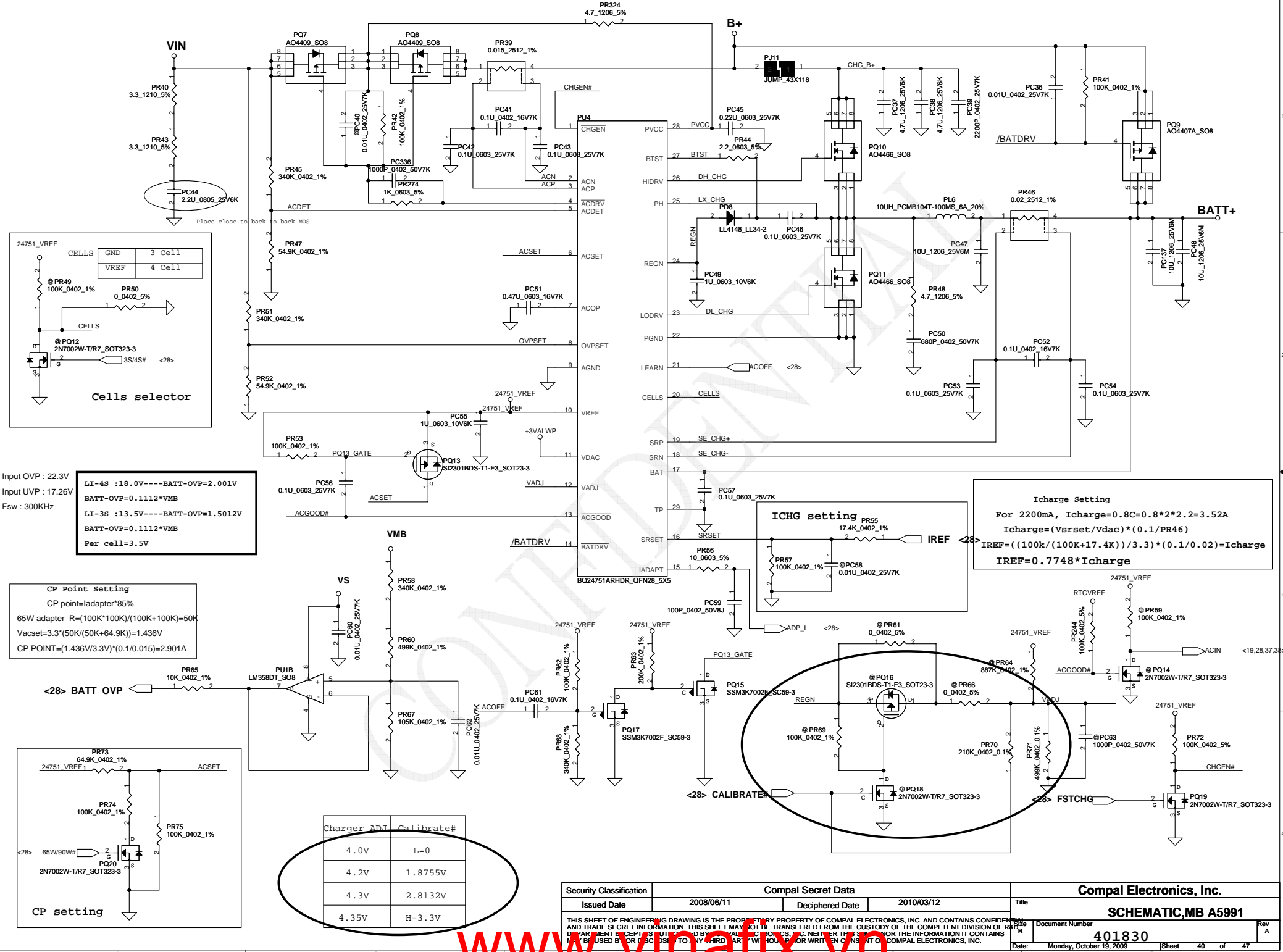


+3.3VALWP Ipeak=4.26A ; Then set I_{max}=4.26A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 316K)/10=158mV
 I_{limit}=158mV/(18m*1.2) ~ 158mV/15m
 =7.31A~10.53A
 I_{ocp}=I_{limit}+Delta I/2
 =7.76A~10.98A
 Delta I=0.908A (Freq=300KHz)

+5VALWP Ipeak=6.87A ; I_{max}=4.81A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 365K)/10=182.5mV
 I_{limit}=182.5mV/(18m*1.2) ~ 182.5mV/15m
 =8.44A ~ 12.16A
 I_{ocp}=I_{limit}+Delta I/2
 =8.90A ~ 12.62A
 Delta I=0.921A (Freq=400KHz)

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Input OVP : 22.3V

Input UVP : 17.26V

Fsw : 300KHz

LI-4S :18.0V----BATT-OVP=2.001V

BATT-OVP=0.1112*VMB

LI-3S :13.5V----BATT-OVP=1.5012V

BATT-OVP=0.1112*VMB

per cell=3.5V

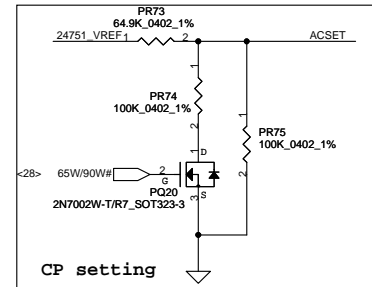
CP Point Setting

CP point=ladapter*85%

65W adapter R=(100K*100K)/(100K+100K)=50K

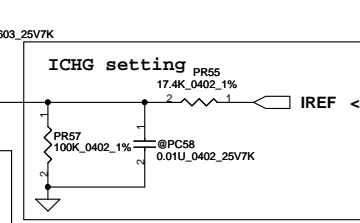
Vacset=3.3*(50K/(50K+64.9K))=1.436V

CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A



Charger ADI Calibrate

Calibrate#	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V



Icharge Setting

For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A

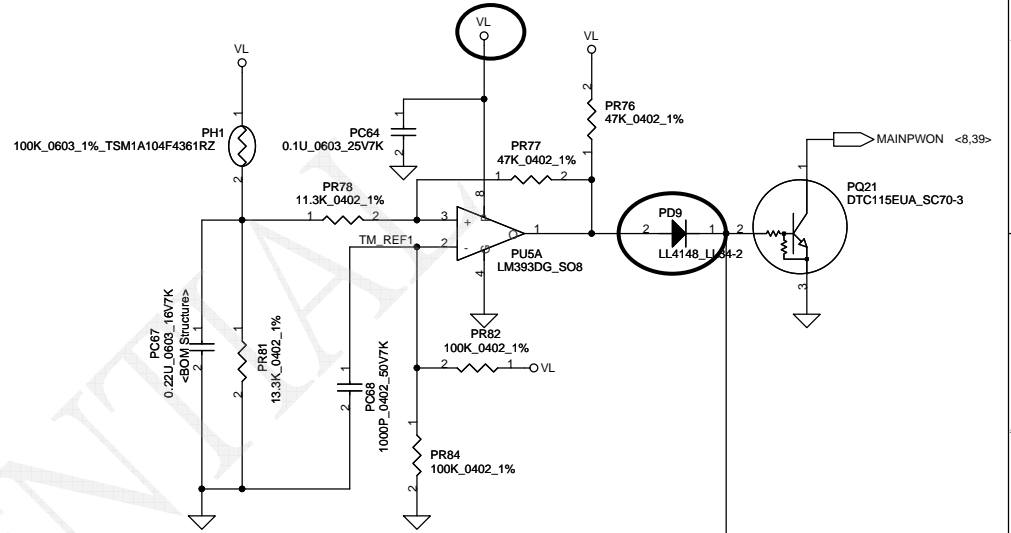
Icharge=(Vsrset/Vdac)*(0.1/PR46)

IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge

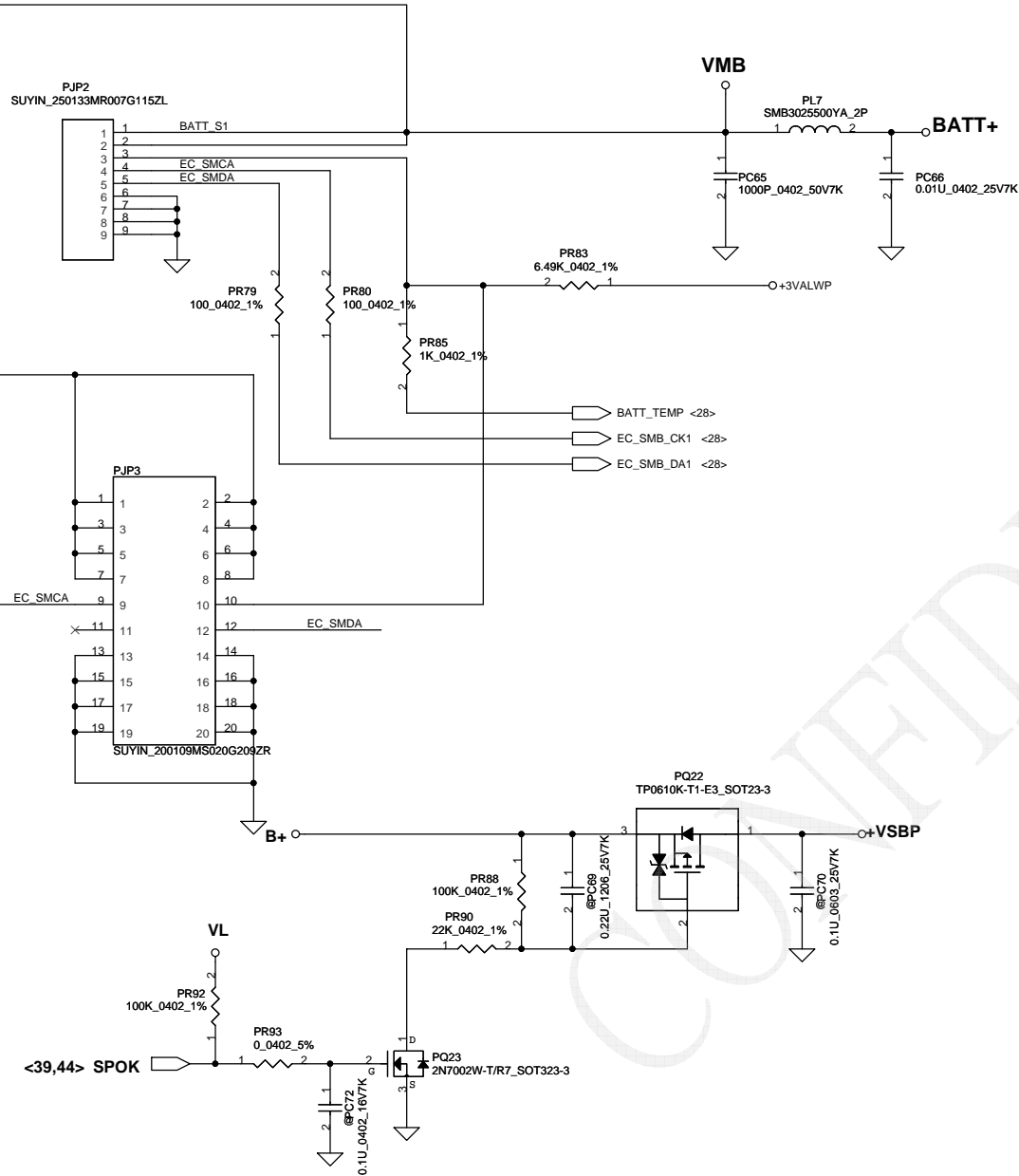
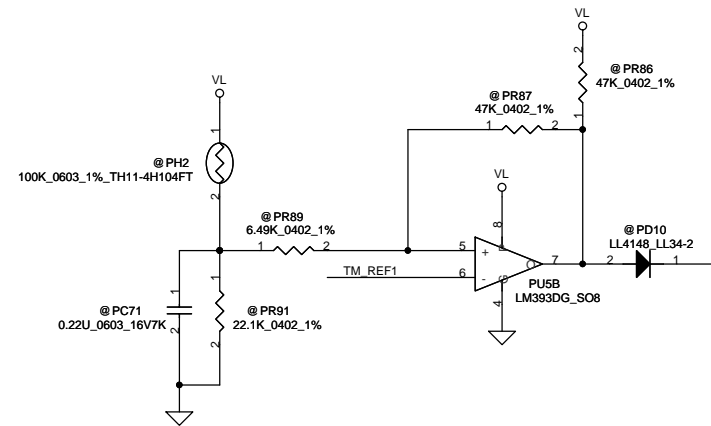
IREF=0.7748*Icharge

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PH1 under CPU botten side :
CPU thermal protection at 92 degree C

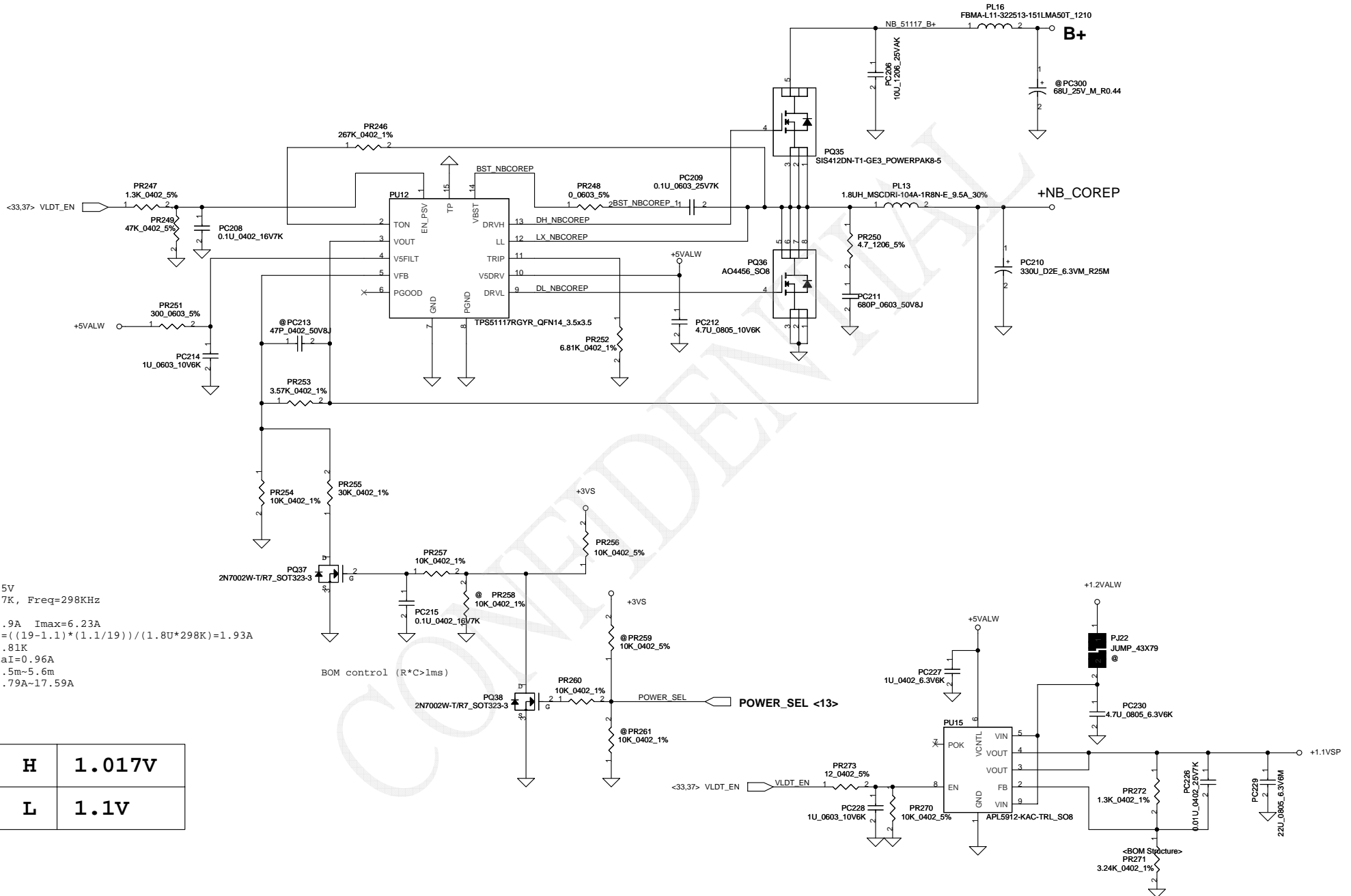


PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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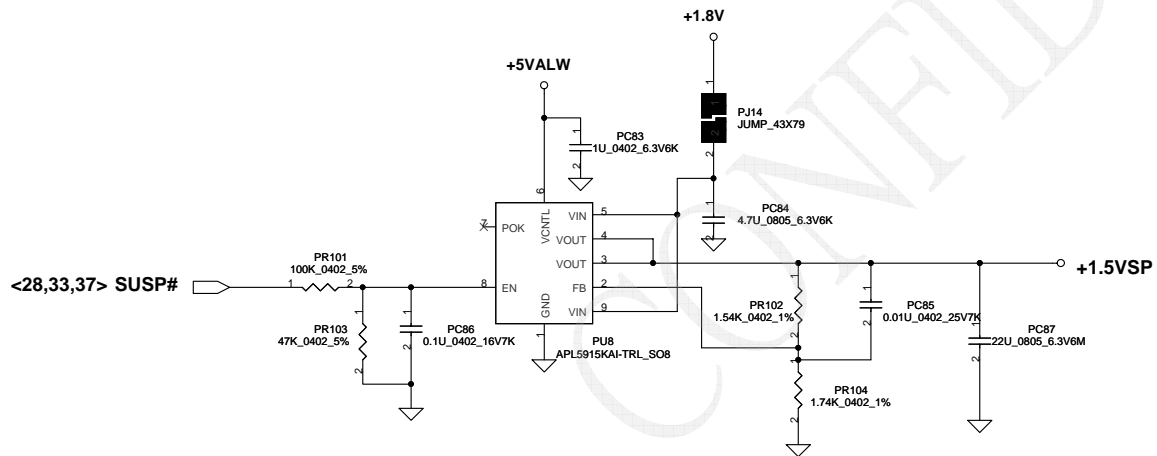
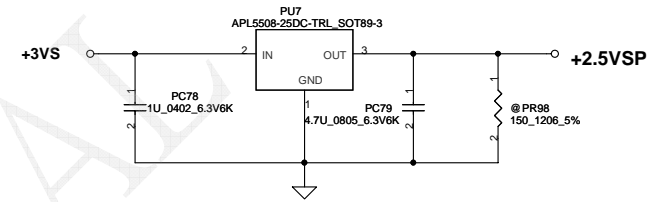
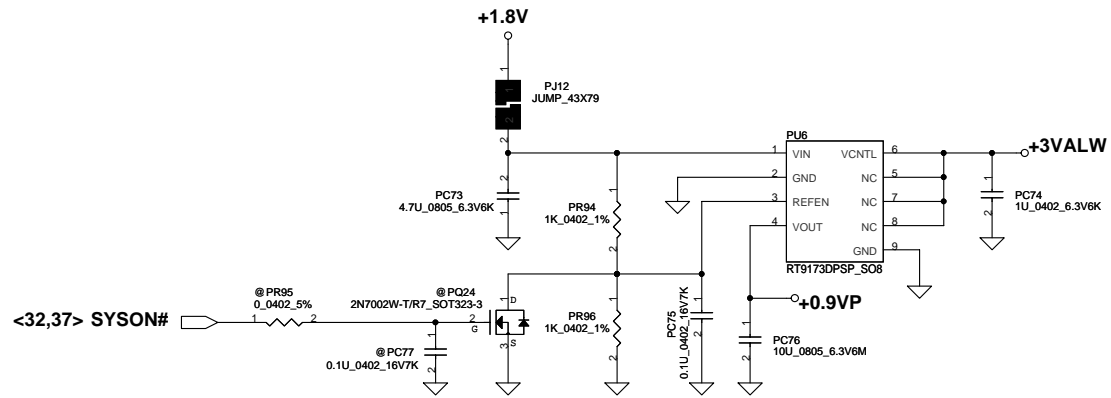
VFB=0.75V
 Rton=267K, Freq=298KHz
 Ipeak=8.9A Imax=6.23A
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$
 Rtrip=6.81K
 $1/2\Delta I = 0.96A$
 Rdson=4.5m~5.6m
 Iocp=10.79A~17.59A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

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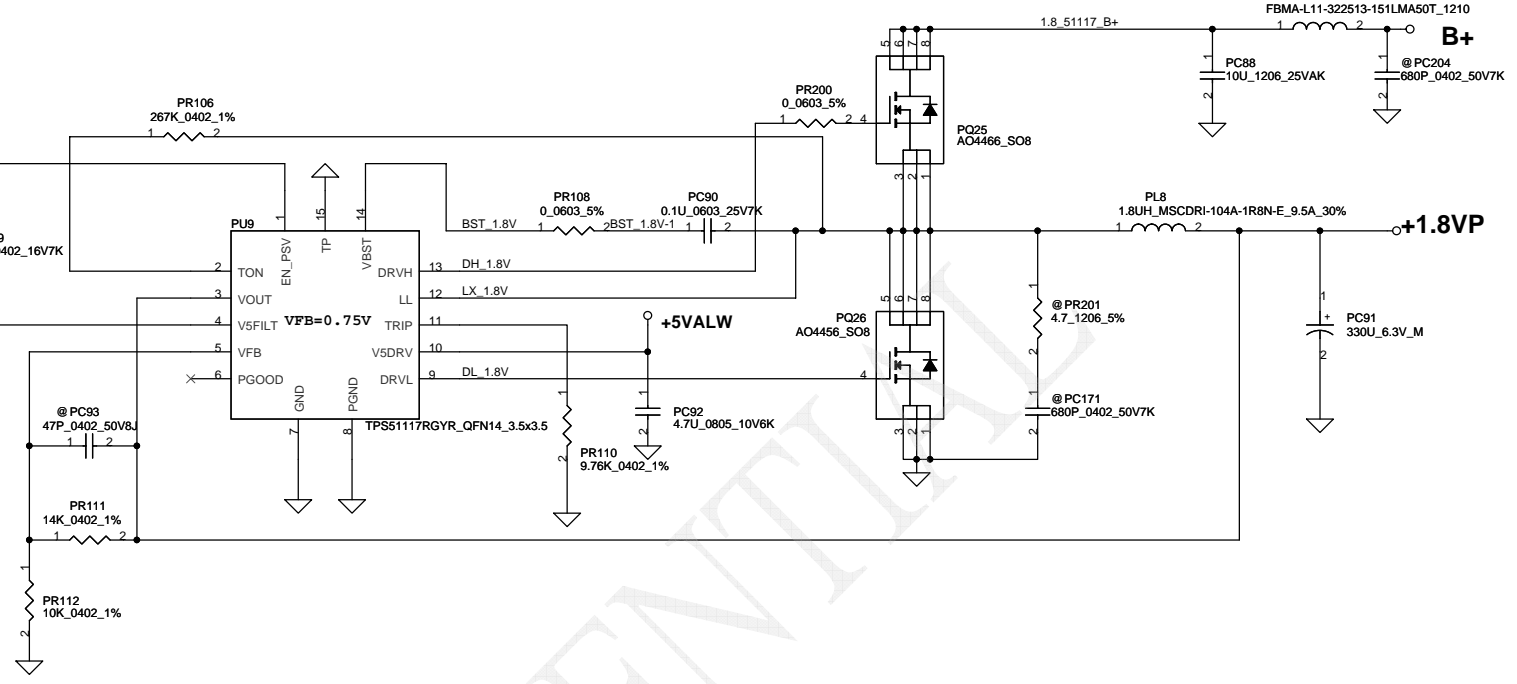
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<28,37> SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

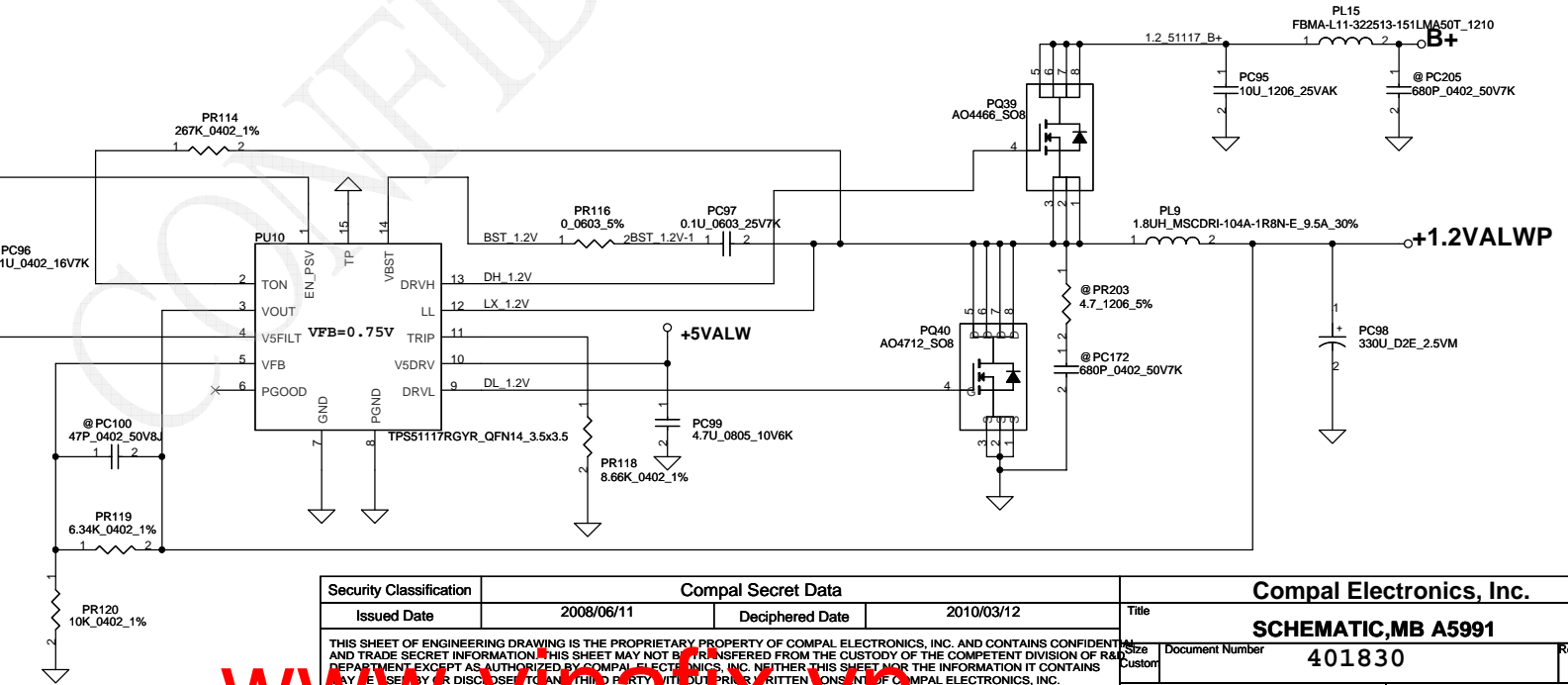
Cout ESR=15m ohm
 $I_{peak} = 11.96A, I_{max} = 8.372A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$



<39,41> SPOK

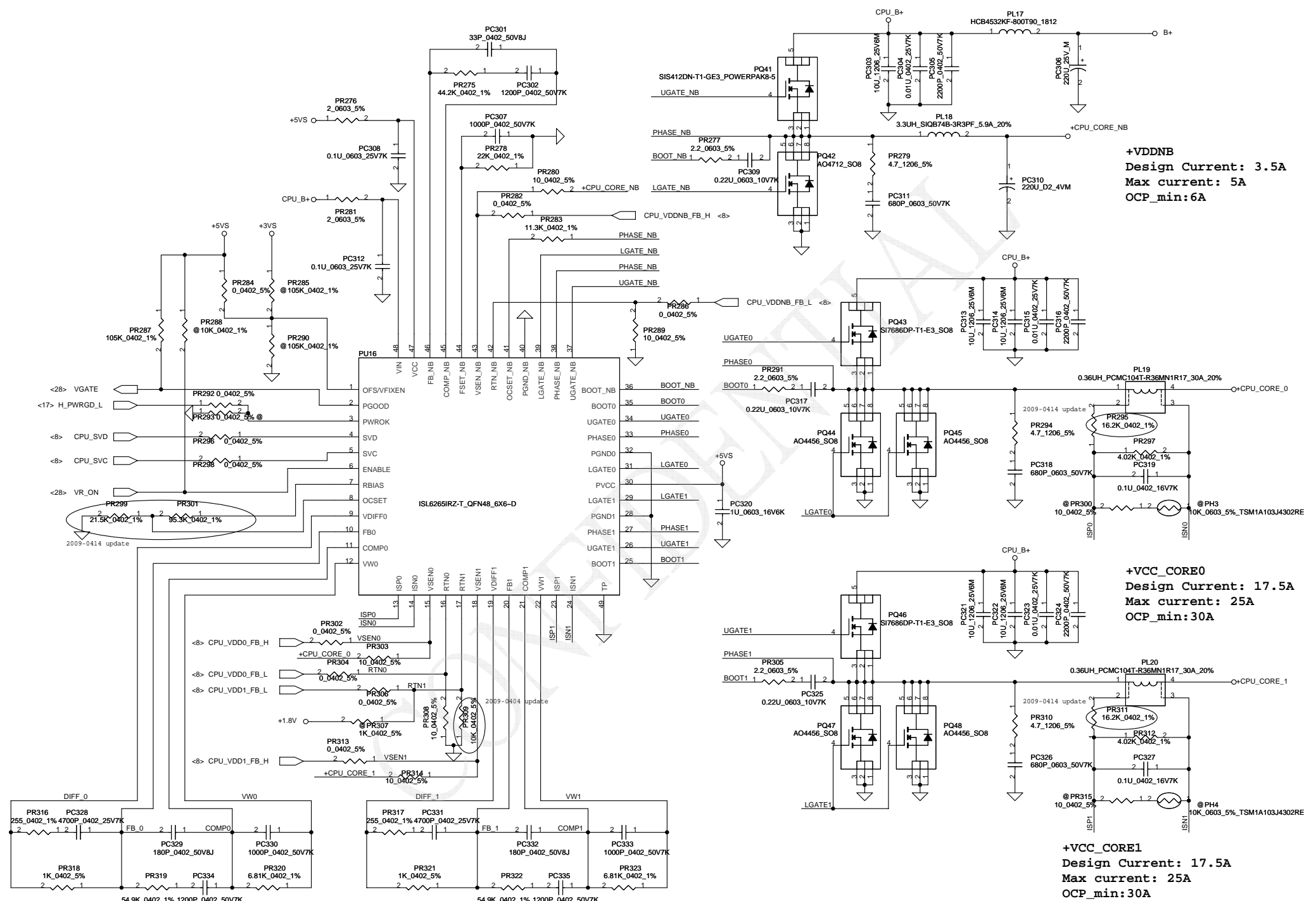
VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A ; I_{max} = 5.180A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m \text{ ohm}$
 $set R_{trip} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$



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