

Title	The power sequence of VT8235
Released Date	May 23, 2003

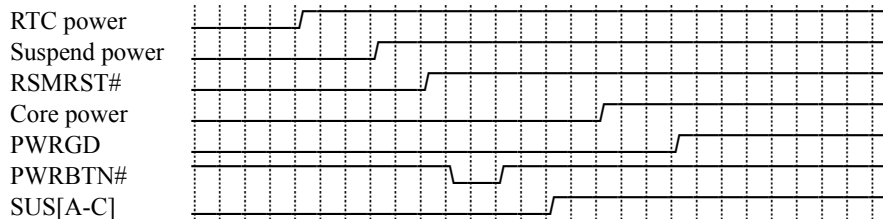
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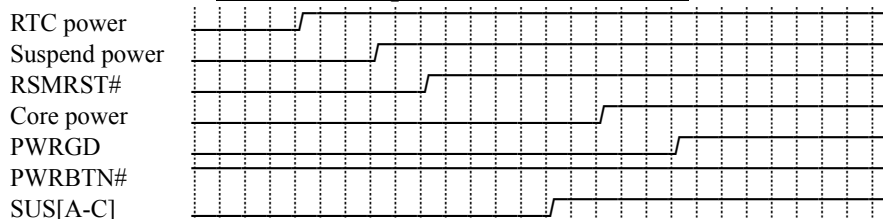
Revision History

Document Release	Date	Revision	Initials
AP228	07/09/2002	Initial release	MJ
AP228A	05/23/2003	Update item 4,5,11,12,13 and 14 of table 1.	MJ

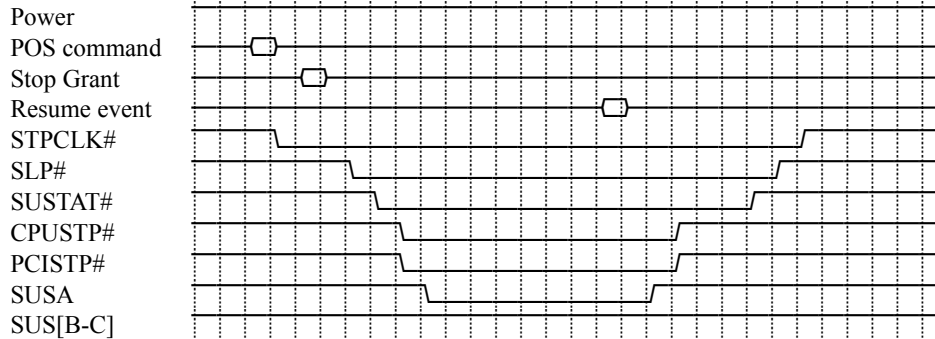
Power On Sequence with default OFF



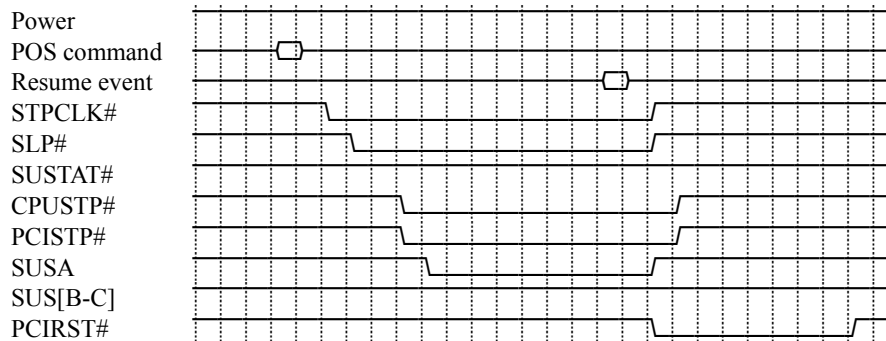
Power On Sequence with default ON



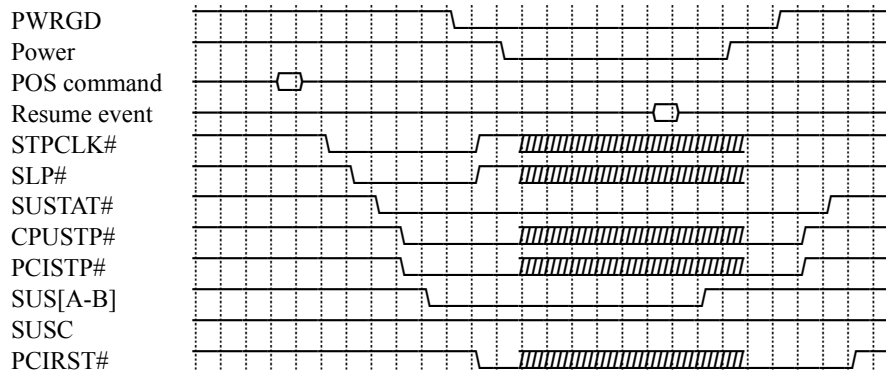
Power On Suspend sequence without RESET (S1)



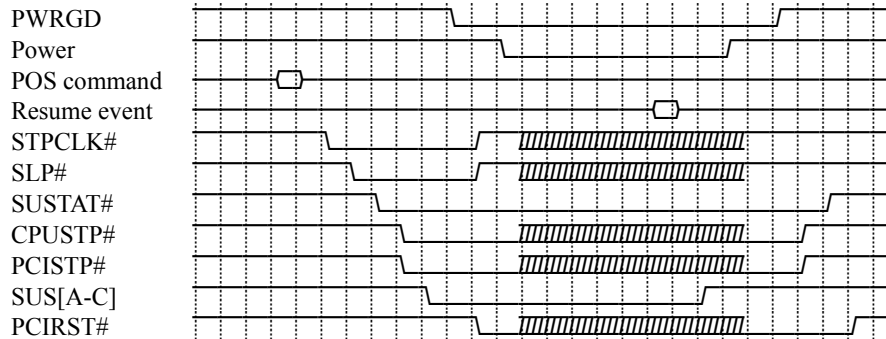
Power On Suspend sequence with CPU/PCI RESET



Suspend to RAM sequence



Suspend to DISK sequence



Item	Parameter	Min	Max	Unit
1	VCCsus good to RSMRST# inactive	1		ms
2	PWRBTN rising to SUS[A-C]# inactive	4	5	RTCCLK
3	RSMRST# inactive to SUS[A-C]# inactive (default ON)	12	14	ms
4	SUSPEND command to STPCLK active	0		RTCCLK
5	STPCLK active to SLP# active (after stop grant cycle)	2	4	RTCCLK
6	SLP# active to SUSTAT# active		1	RTCCLK
7	SUSTAT# active to CPUTSTP#/PCICTP# active		1	RTCCLK
8	CPUTSTP#/PCISTP# active to SUS[A-C]# active		1	RTCCLK
9	Resume event to SUS[A-C] inactive	1		RTCCLK
10	SUSA# inactive to CPUTSTP#/PCISTP# inactive	1		RTCCLK
11	PWRGD to CPUTSTP#/PCISTP# inactive. (Function 0 offset 95 bit 7 = 1)	1	2	ms
12	PWRGD to CPUTSTP#/PCISTP# inactive (Function 0 offset 95 bit 7 = 0)	16	32	ms
13	CPUTSTP#/PCISTP# inactive to SUSTAT# inactive (Function 0 offset 95 bit 7 = 1)	125	250	us
14	CPUTSTP#/PCISTP# inactive to SUSTAT# inactive (Function 0 offset 95 bit 7 = 0)	1	2	ms
15	SUSTAT# inactive to PCIRST# inactive	1		RTCCLK

Table 1.

Note: The timing font is required to display timing diagram. You can get it from VIA FAEs.