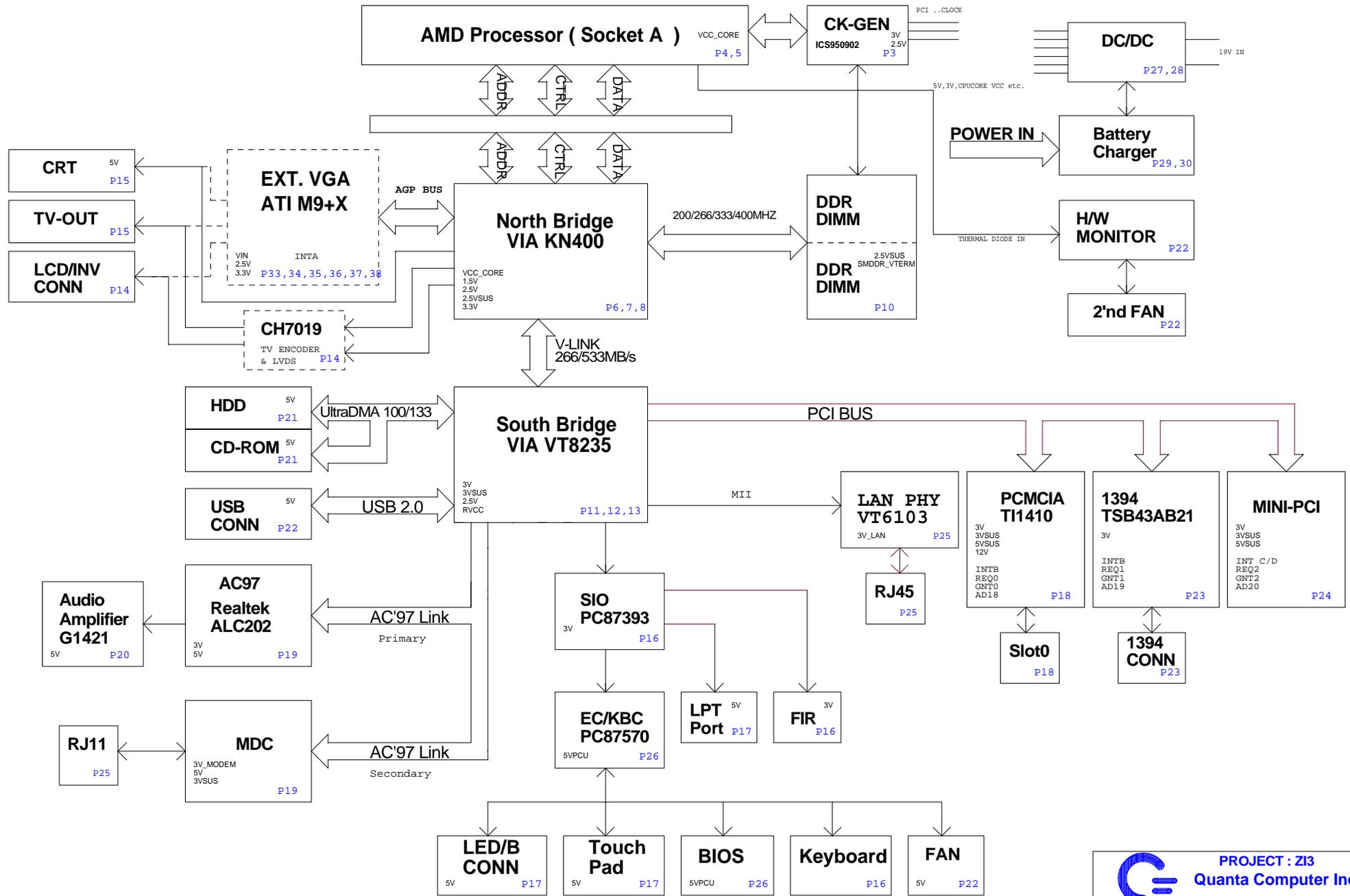
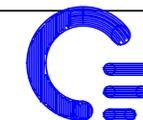


# ZI3 SYSTEM BLOCK DIAGRAM



Voltage Rails	Description	ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON
SMDDR_VTERM	1.25V for DDR Termination voltage	X				MAINON
+1.8V		X				MAINON
1.5VGA	VGA core power	X				MAINON
+1.5V		X				MAINON
2.5VSUS		X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
12V		X				MAINON
12VOUT		X	X	X	X	VL
RVCC		X	X	X		RVCC_ON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ/GNT#	Interrupts
PCI1410	AD18	-REQ0/-GNT0	-INTB
TSB43AB21	AD19	-REQ1/-GNT1	-INTB
MINI-PCI	AD20	-REQ2/-GNT2	-INTC/-INTD
ATi M9+XC			-INTA

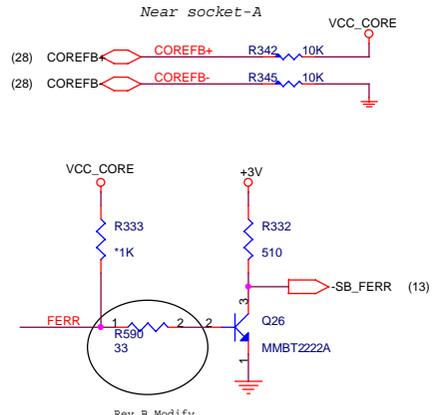
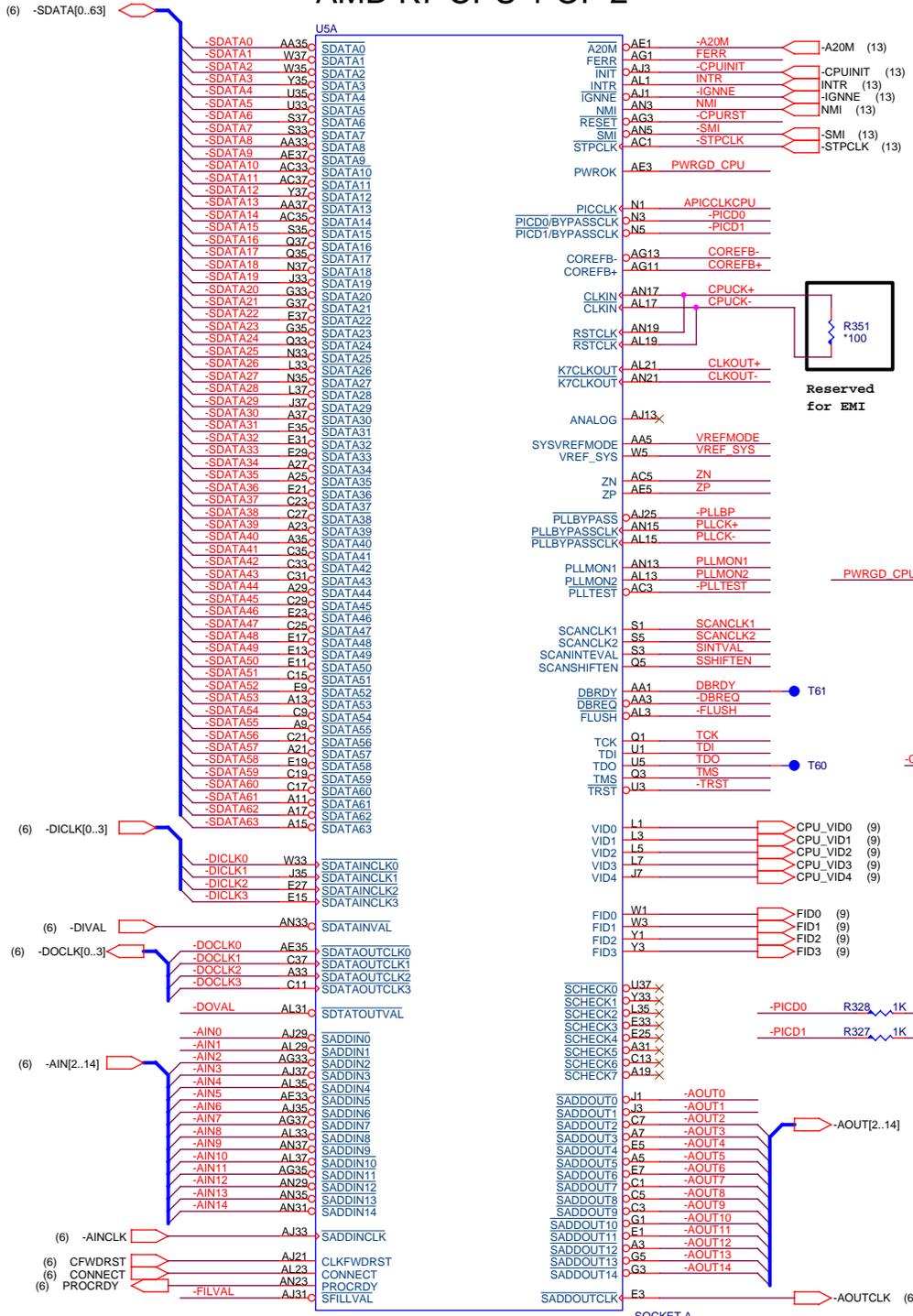


**PROJECT : ZI3**  
**Quanta Computer Inc.**

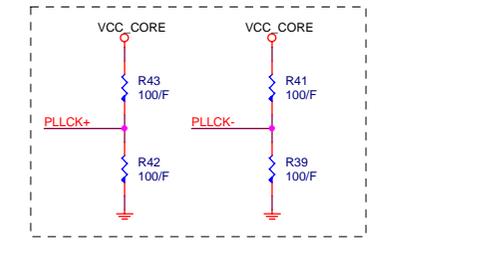
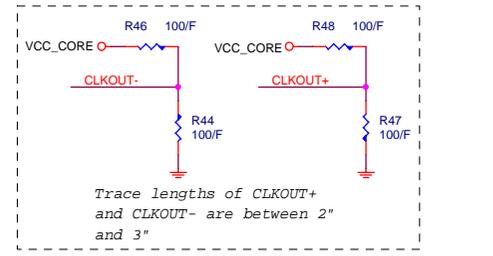
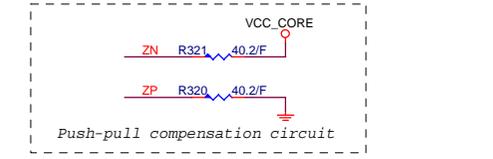
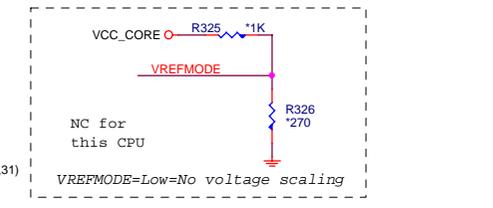
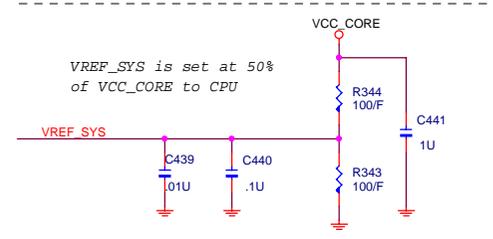
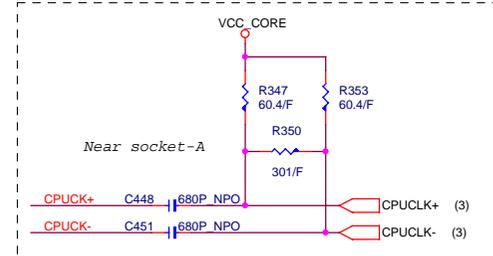
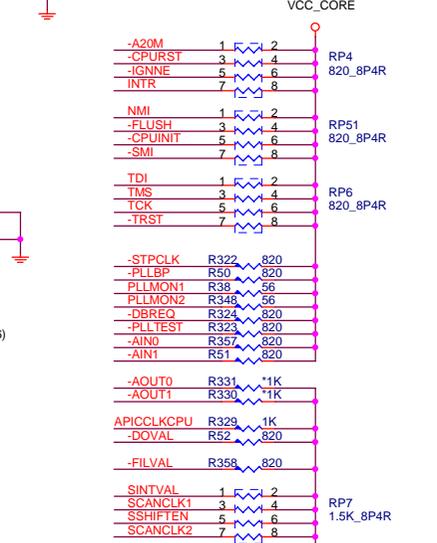
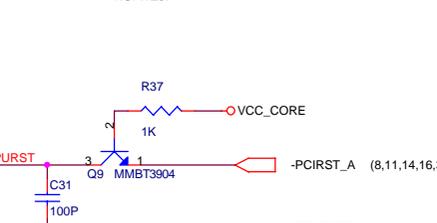
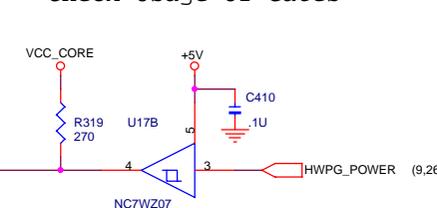
Size A4	Document Number	Rev 1A
<b>INFORMATION</b>		
Date:	Wednesday, September 24, 2003	Sheet 2 of 38



# AMD K7 CPU 1 OF 2



Check Usage of Gates



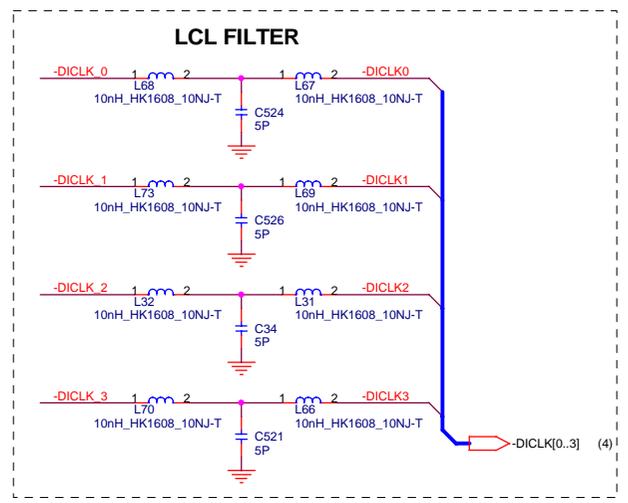
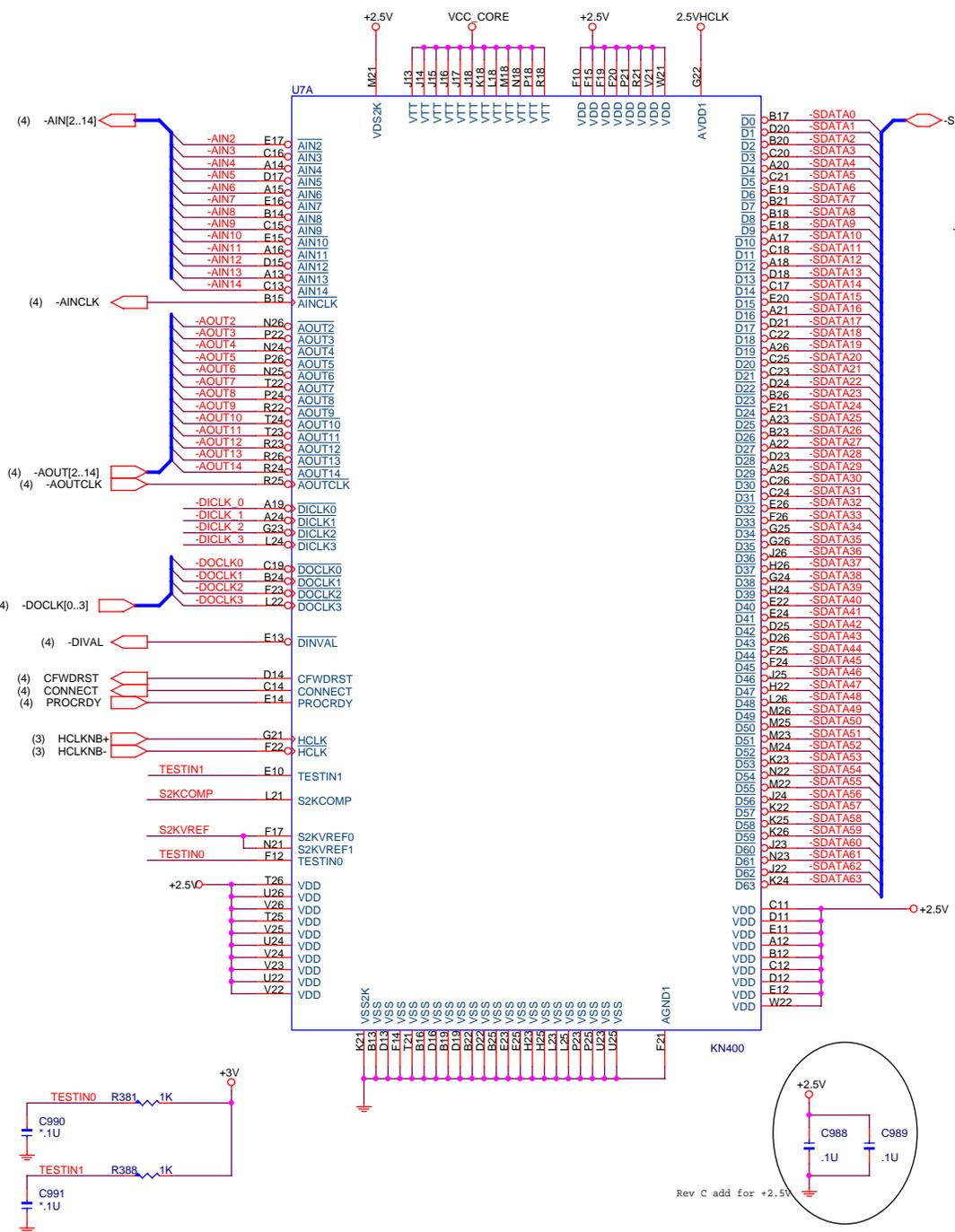


**PROJECT : ZI3**  
**Quanta Computer Inc.**

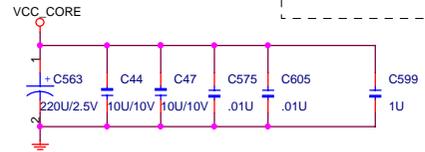
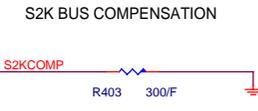
Size C	Document Number	Rev 2A
<b>CPU-1(S2K)</b>		
Date:	Wednesday, September 24, 2003	Sheet 4 of 38



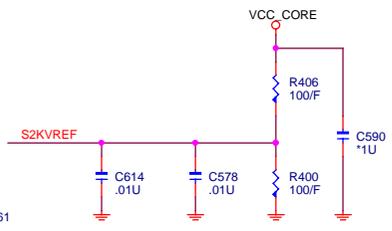
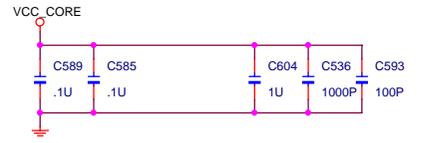
# NORTH BRIDGE 1 of 3 ( HOST BUS)



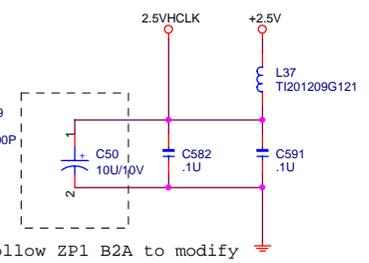
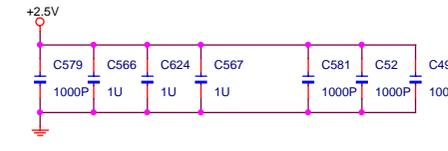
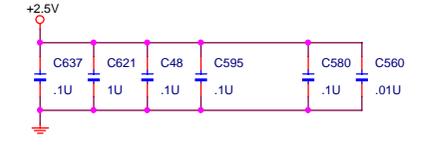
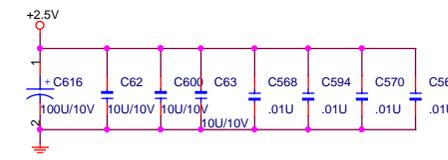
PLACED NEAR NORTH BRIDGE



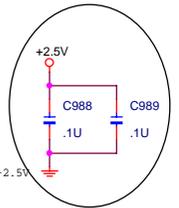
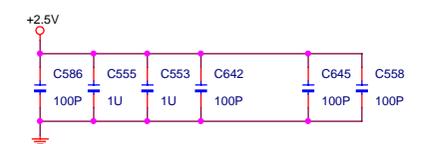
NORTH BRIDGE S2K REFERENCE VOTAGE (1/2 VCC\_CORE)  
PLACED UNDER BGA



AVDDHCLK/AGNDHCLK : POWER/GROUND FOR INTERNAL CPU CLOCK LOGIC



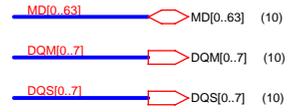
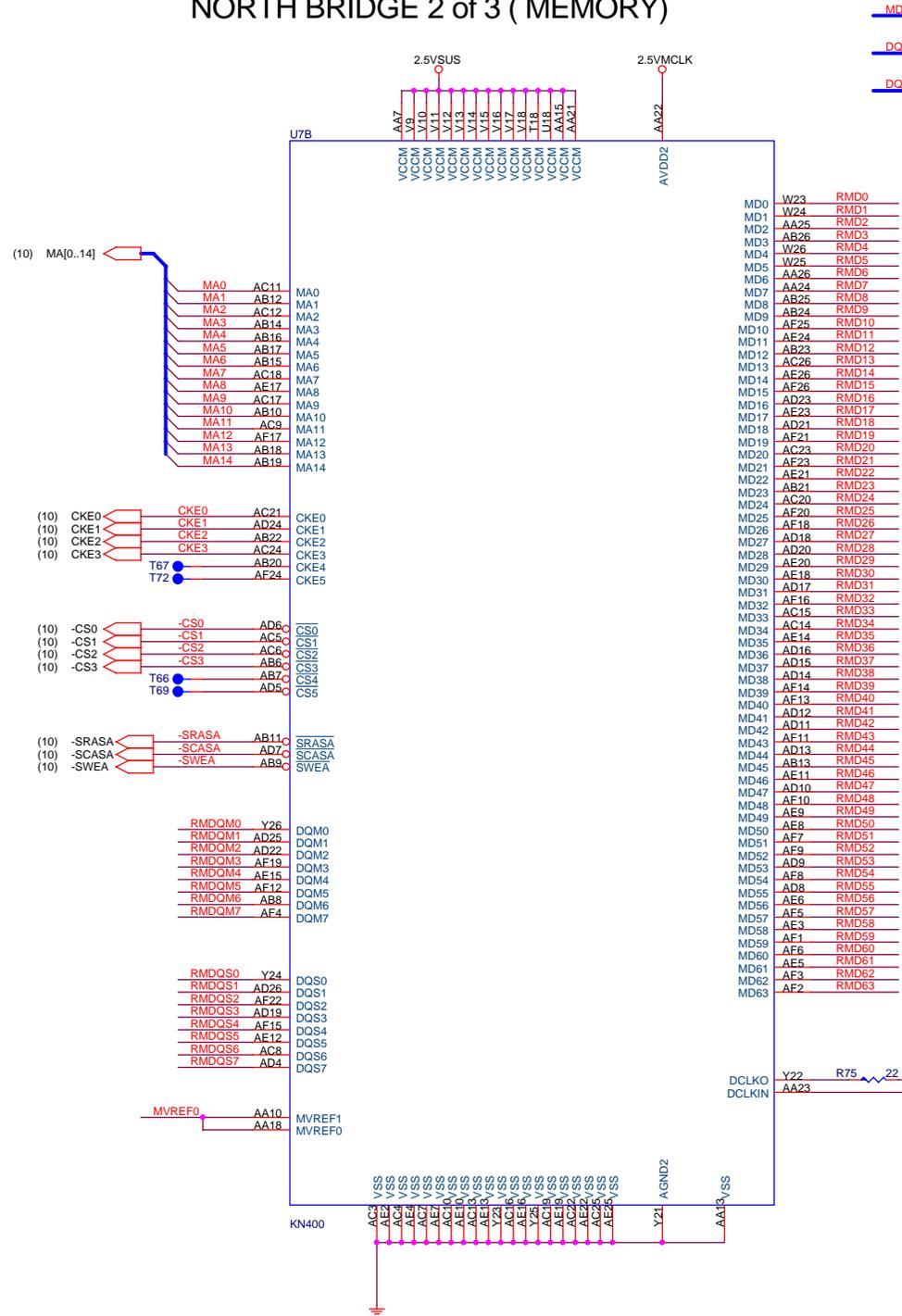
Follow ZP1 B2A to modify



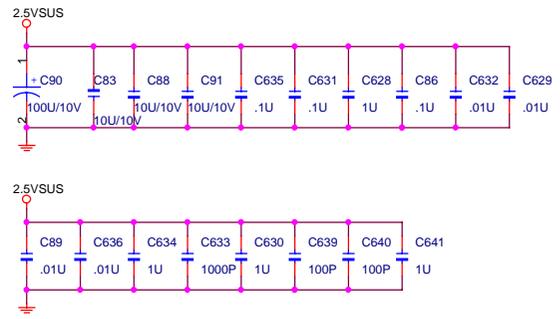
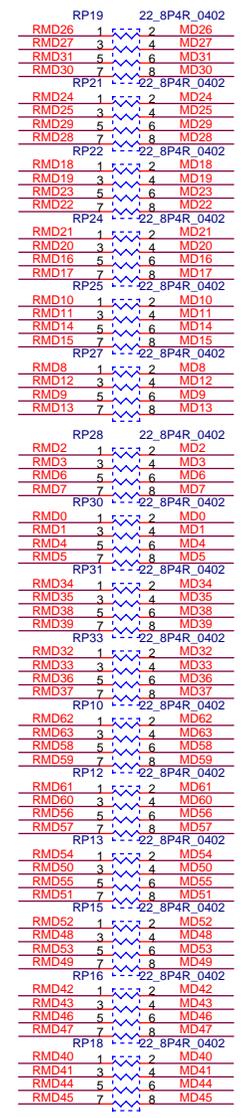
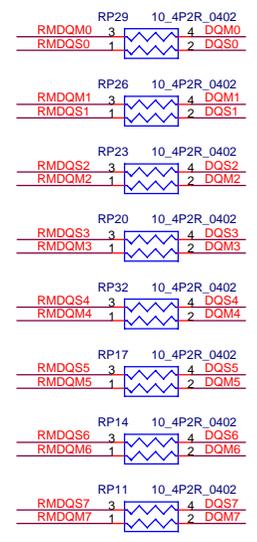
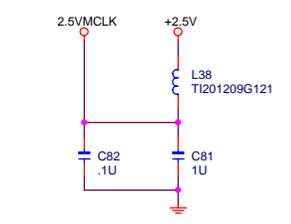
Rev C add for +2.5V

**PROJECT : ZI3**  
**Quanta Computer Inc.**

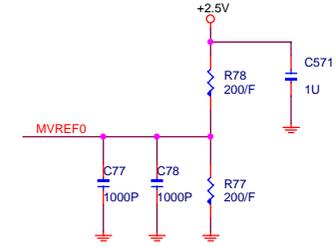
# NORTH BRIDGE 2 of 3 ( MEMORY)



## AVMCLK/AGNDMCLK : POWER/GROUND FOR DRAM CLOCK DESKEW CIRCUIT



## MVERF0/1 : SSTL\_2 RECEIVER VREF FOR DDR

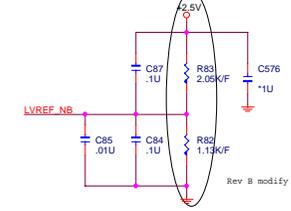


**PROJECT : ZI3**  
**Quanta Computer Inc.**

Size C	Document Number	Rev 2A
<b>NORTH BRIDGE(DDR)</b>		
Date: Wednesday, September 24, 2003	Sheet 7 of 38	

VLINK

1. VLINK REFERENCE VOLTAGE 0.9V

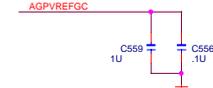


2. VLINK P-CHANNEL COMPENSATION

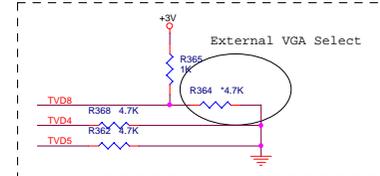


AGP

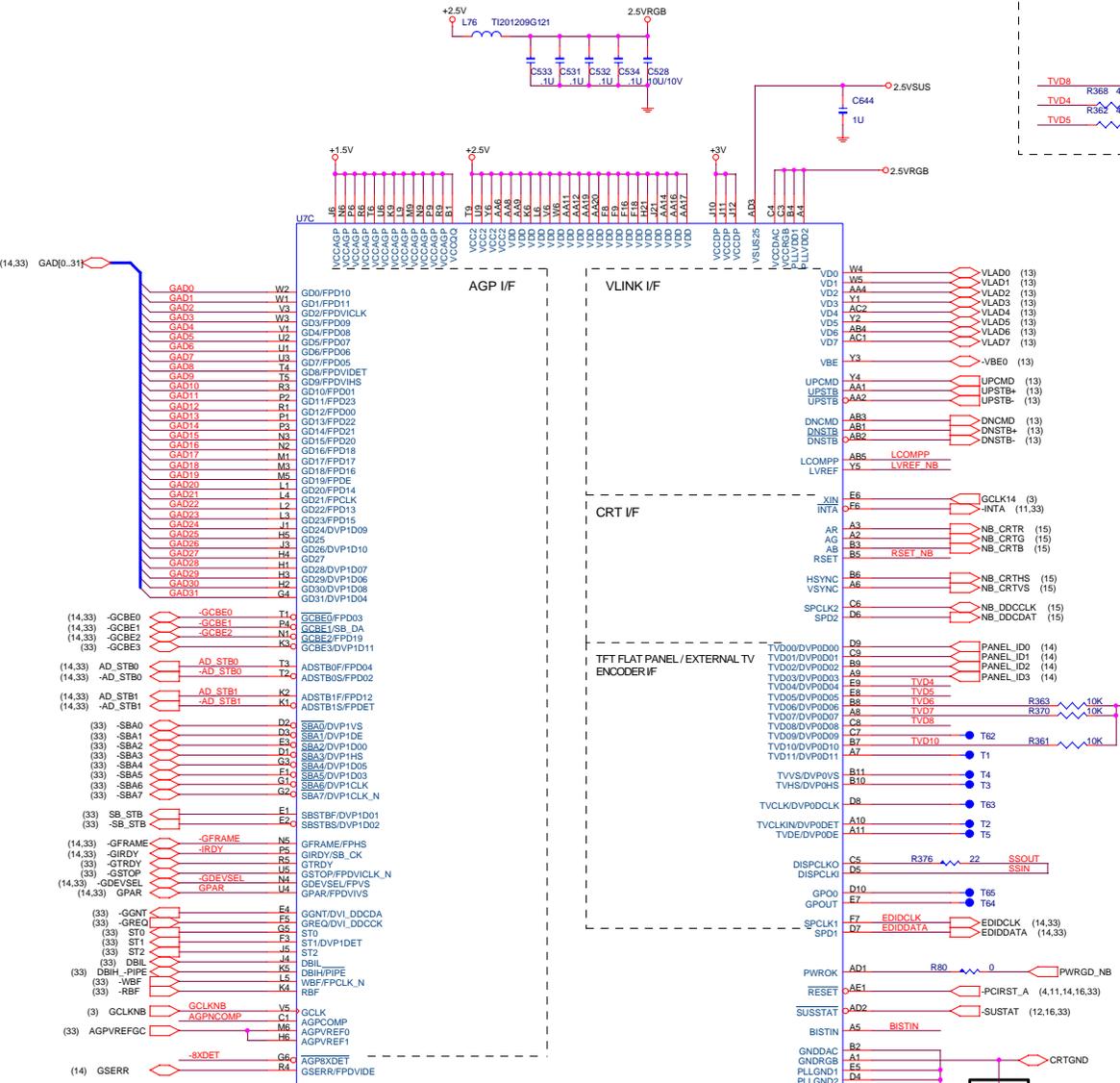
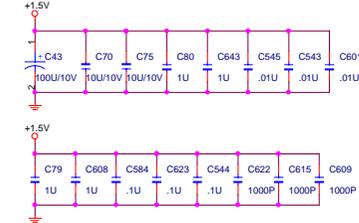
1. AGP/REF (PROVIDED BY AGP 8X CARD OR BY SYSTEM FOR OTHERS)



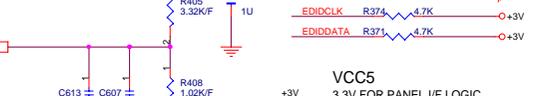
2. AGPNCOMP : AGP N-CHANNEL COMPENSATION



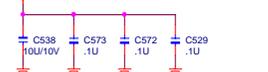
STRAP FOR EXT. VGA AND TV ENCODER SELECT



AGP VREF



VCC5 3.3V FOR PANEL I/F LOGIC

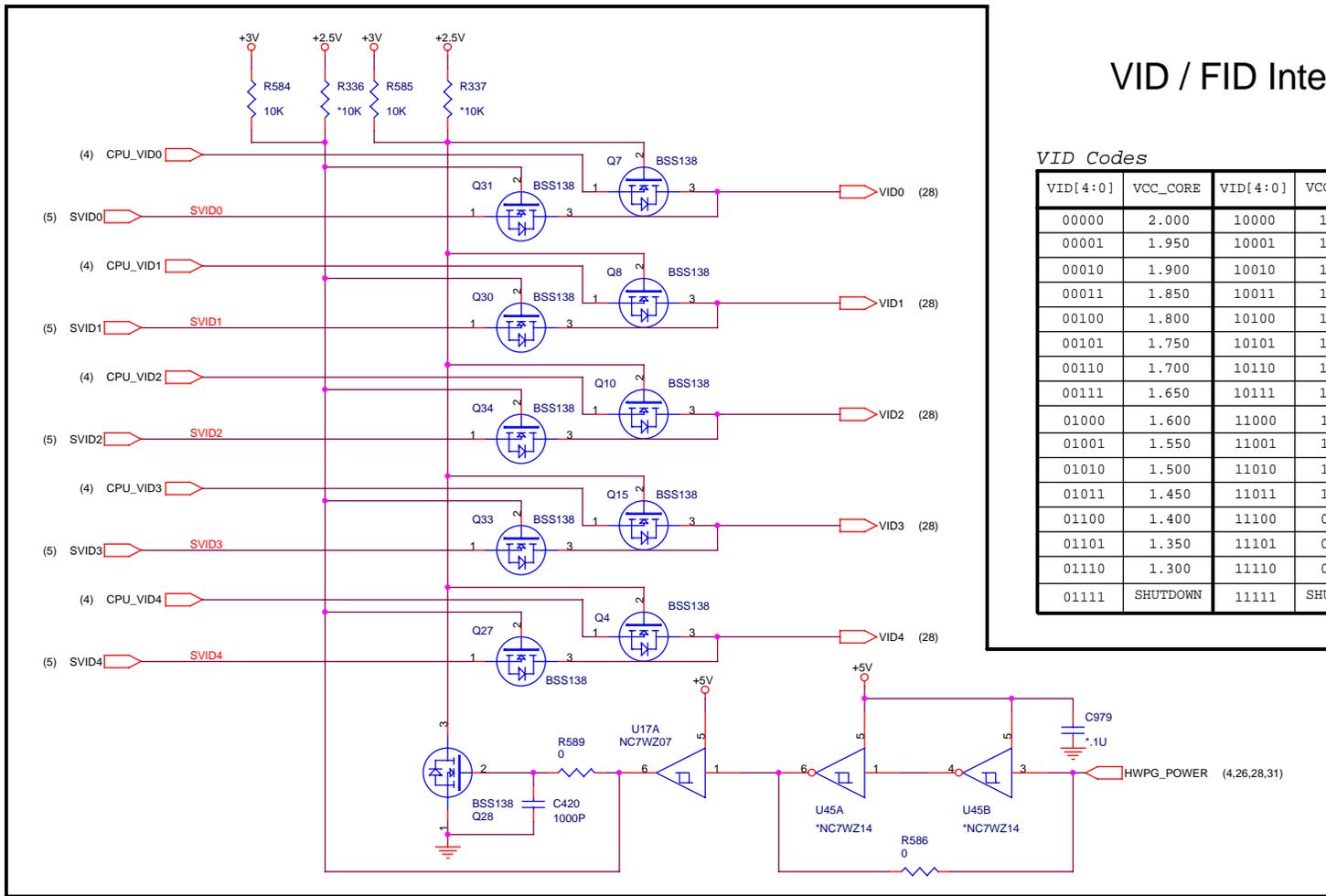
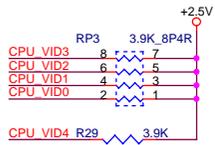
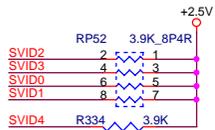


PLACE CLOSE TO N/B

**PROJECT : Z13**  
**Quanta Computer Inc.**

Size C Document Number **NORTH BRIDGE-3(VGA)** Rev 2A  
 Date: Wednesday, September 24, 2003 Sheet 8 of 38

AMD suggest 3.9K



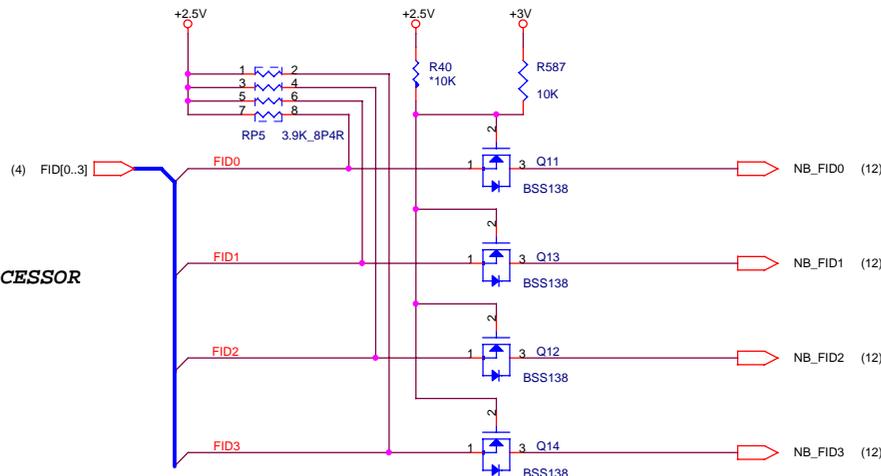
# VID / FID Interface

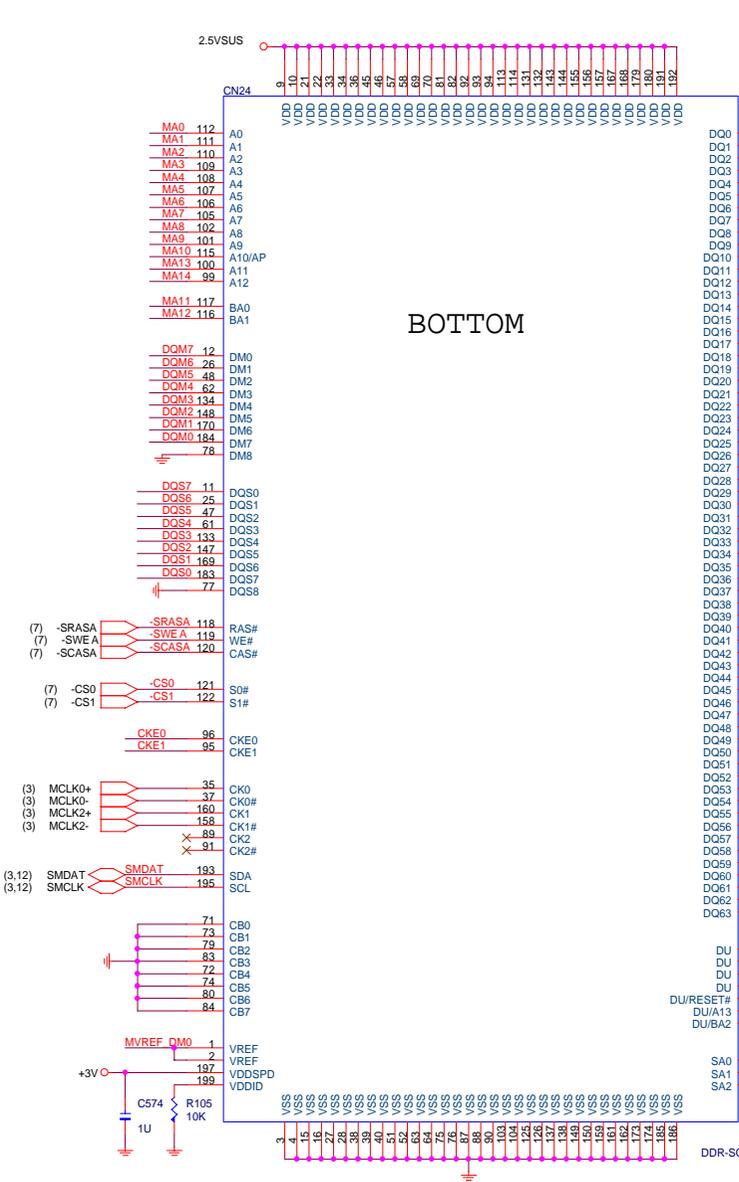
VID Codes

VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	SHUTDOWN	11111	SHUTDOWN

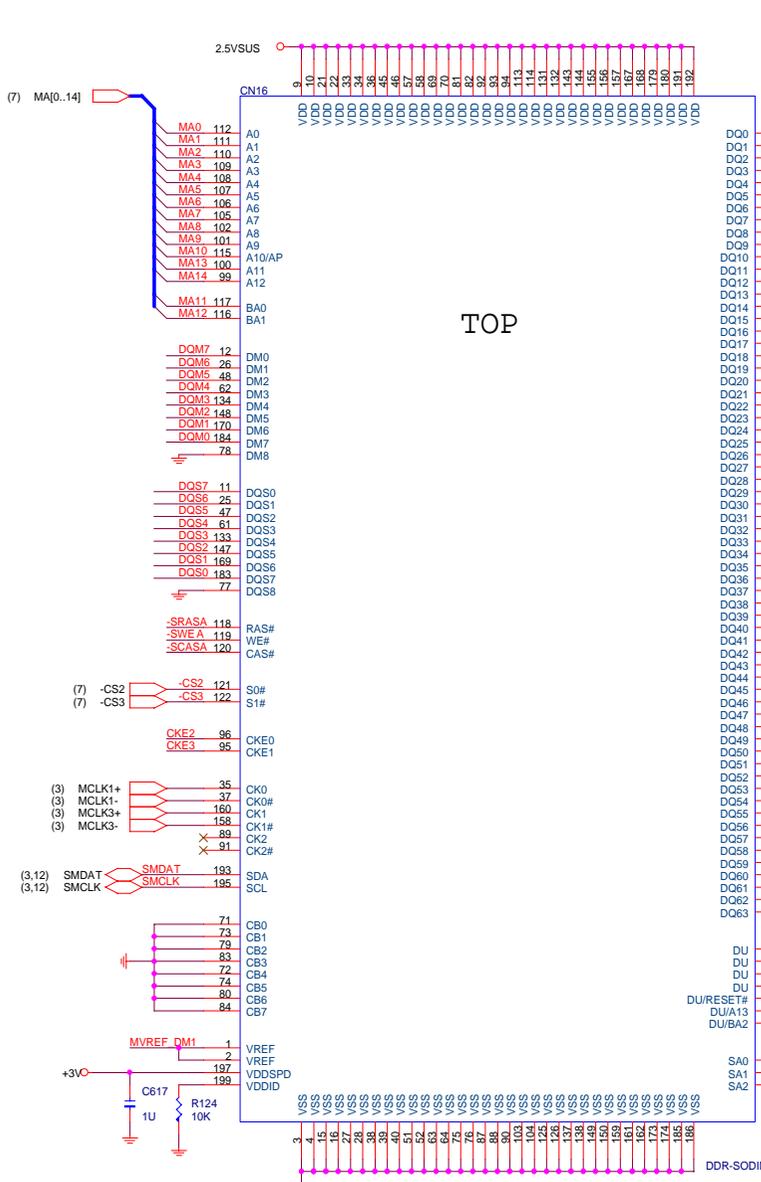
FID Codes

Four-Bit FID	Clock Multiplier	Four-Bit FID	Clock Multiplier
0000	11.0	1000	7.0
0001	11.5	1001	7.5
0010	12.0	1010	8.0
0011	12.5	1011	8.5
0100	5.0	1100	9.0
0101	5.5	1101	9.5
0110	6.0	1110	10.0
0111	6.5	1111	10.5

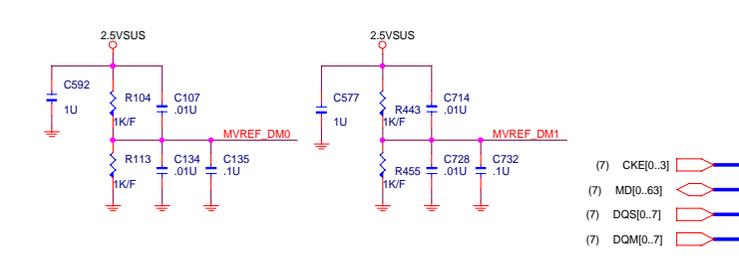
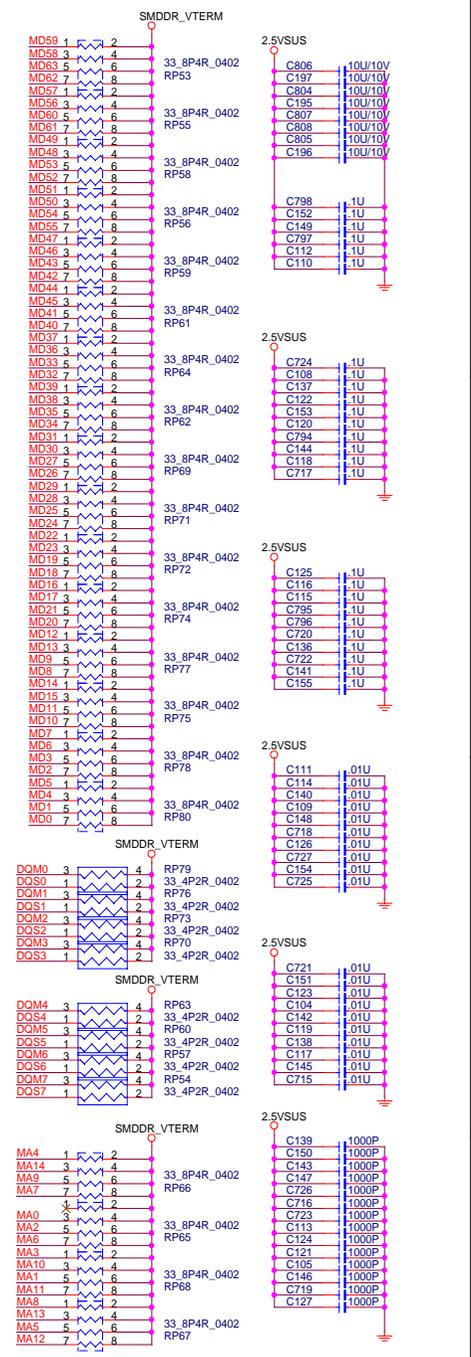


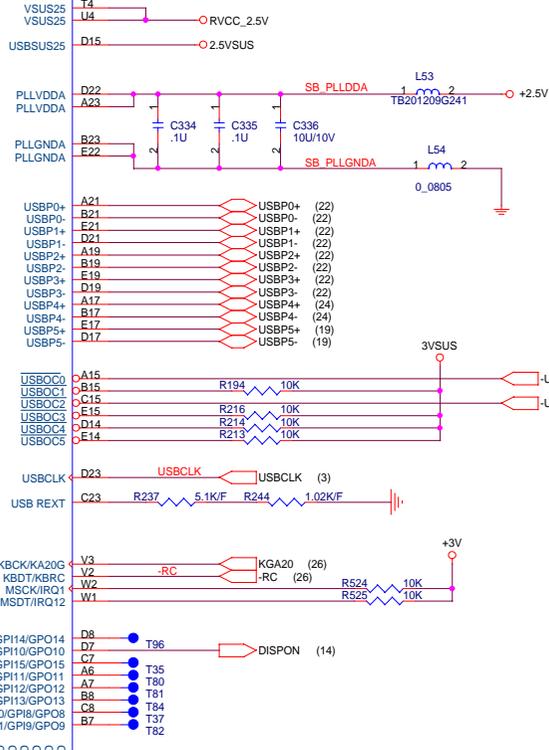
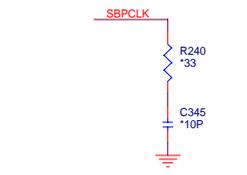
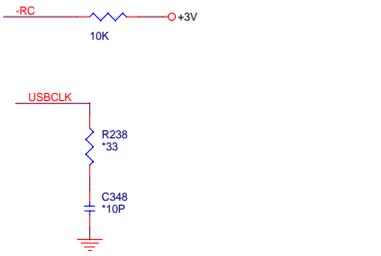
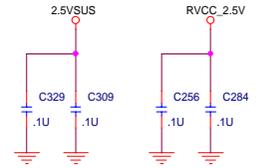
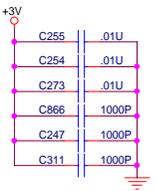
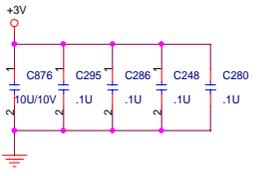
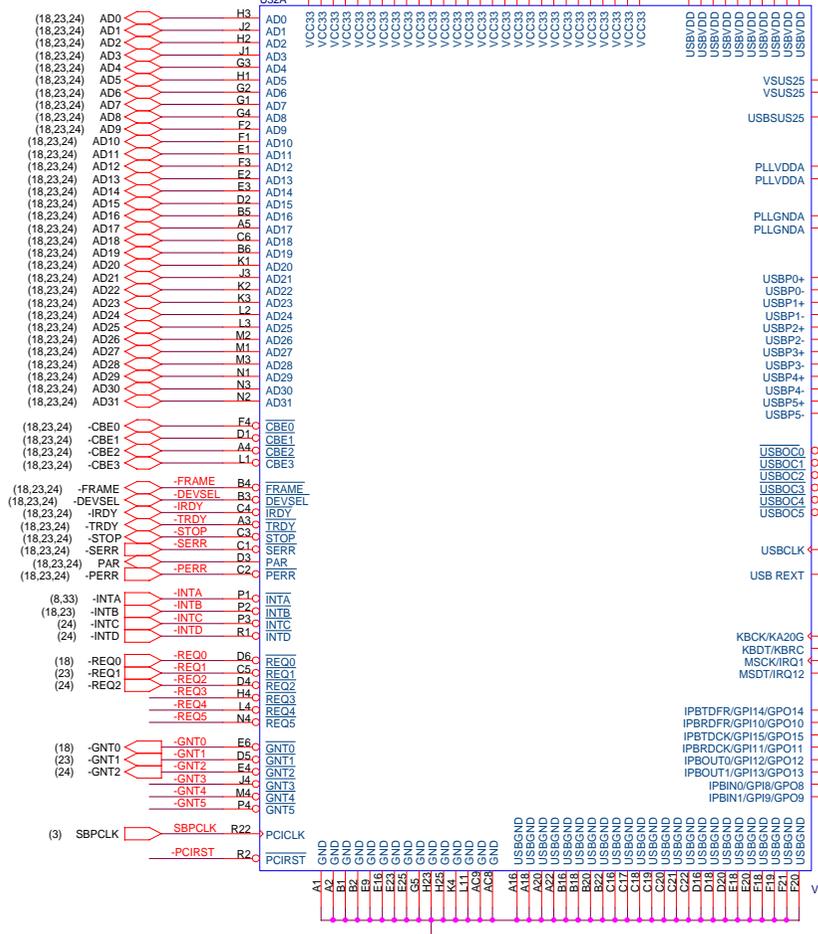
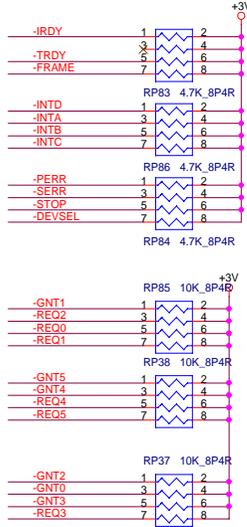
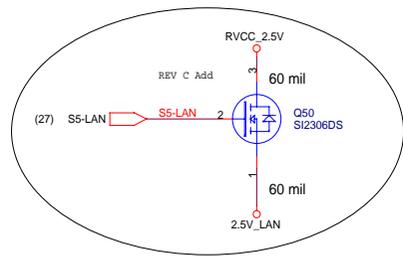


BOTTOM

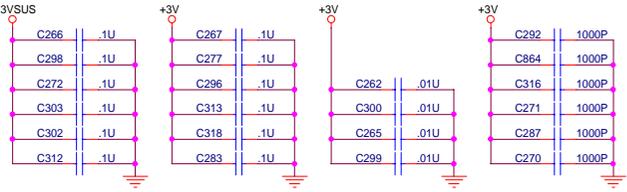
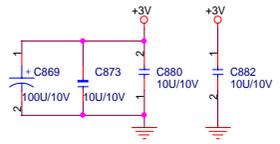
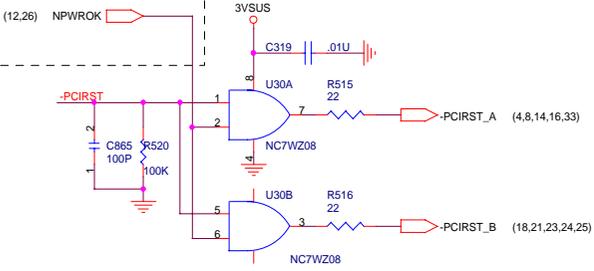


TOP

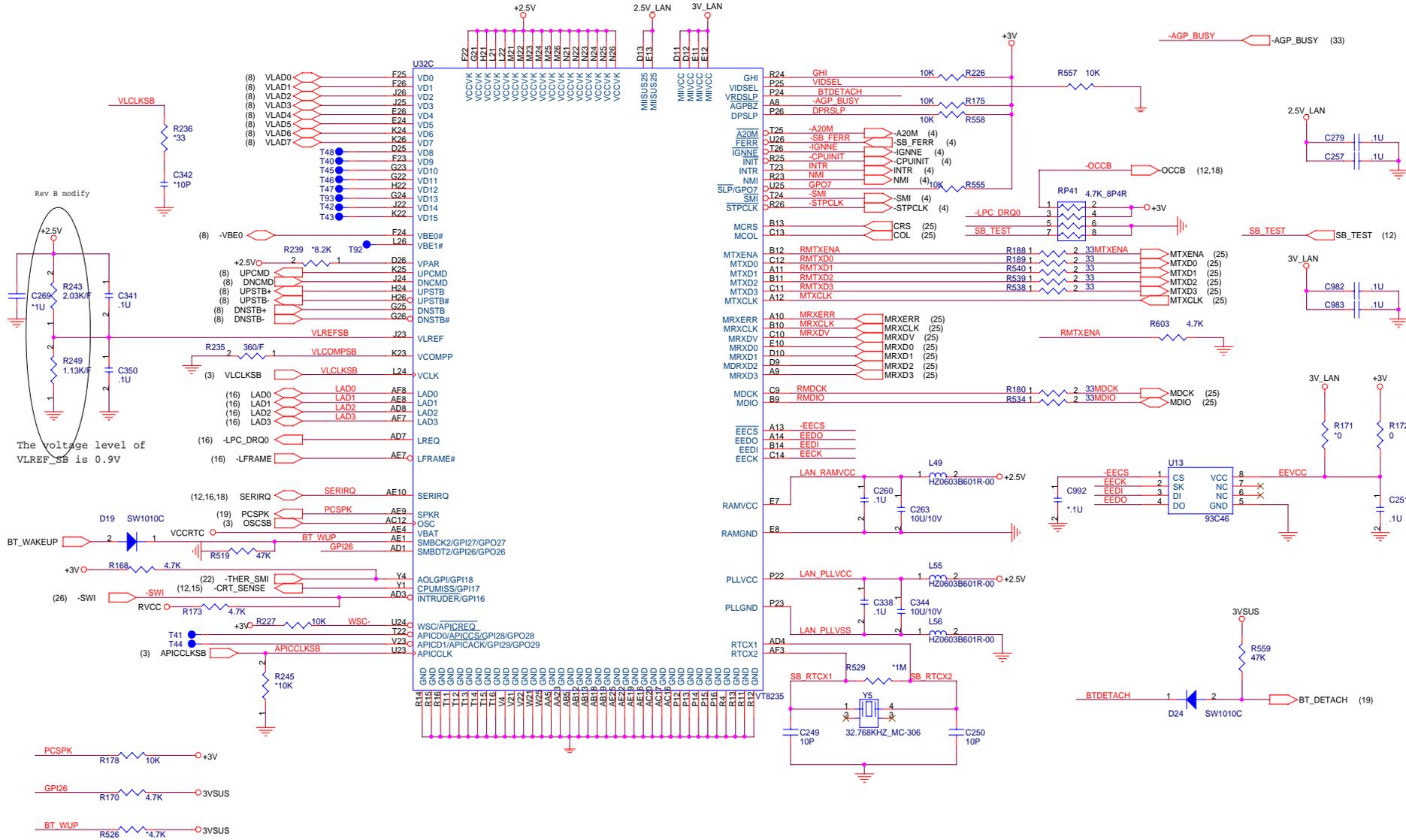




Follow ZP1 B2A to modify

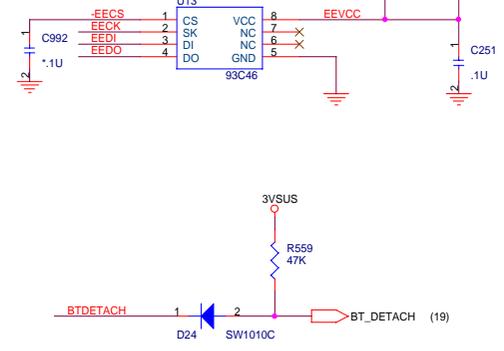
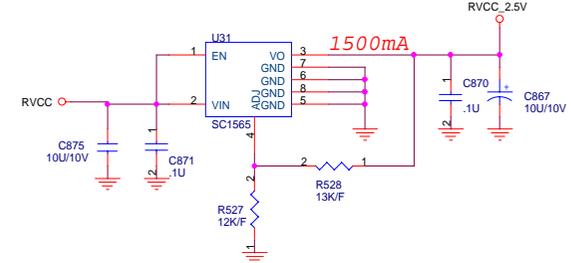
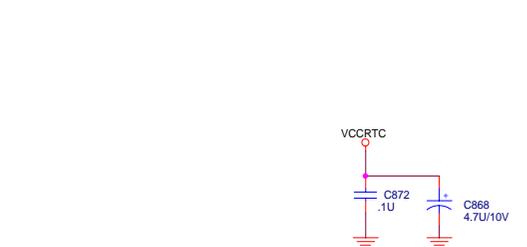
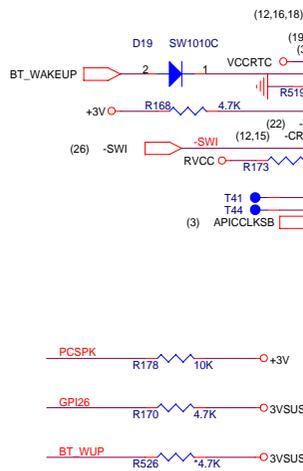




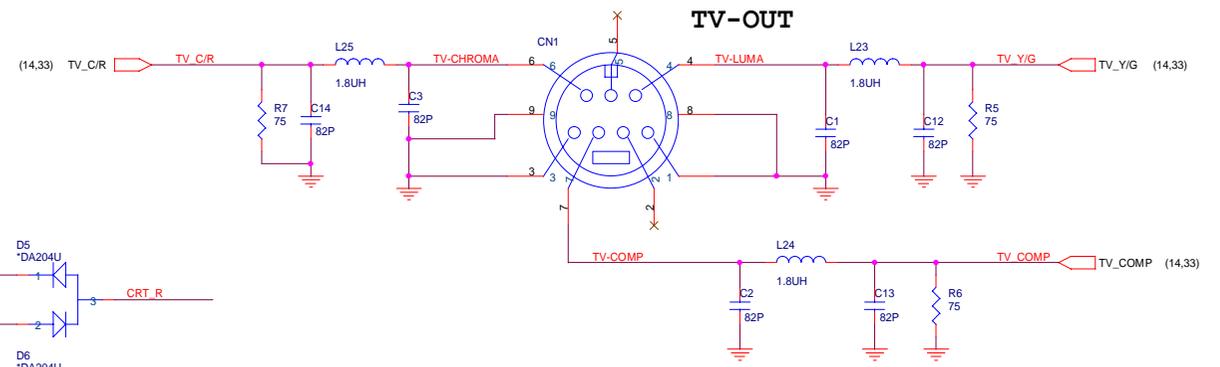
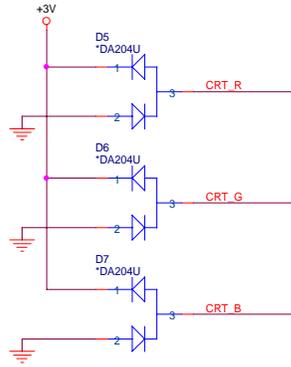
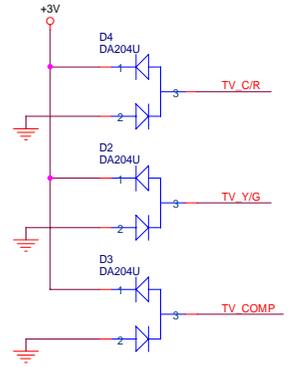


Rev B modify

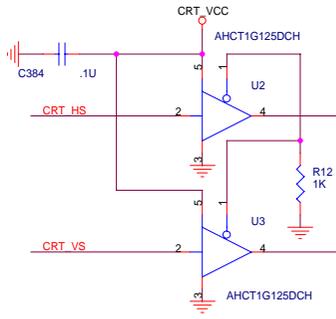
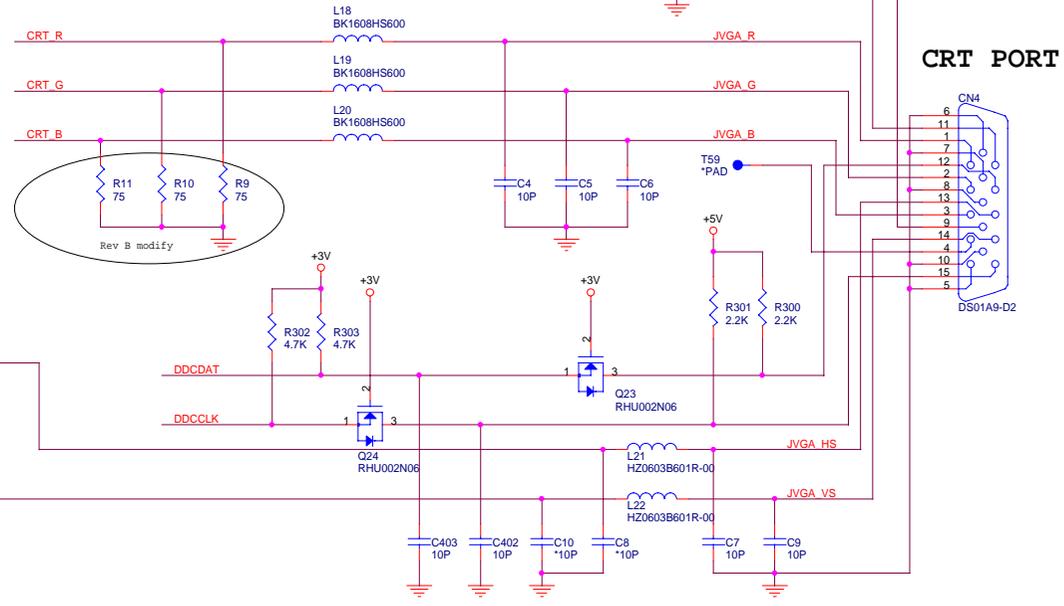
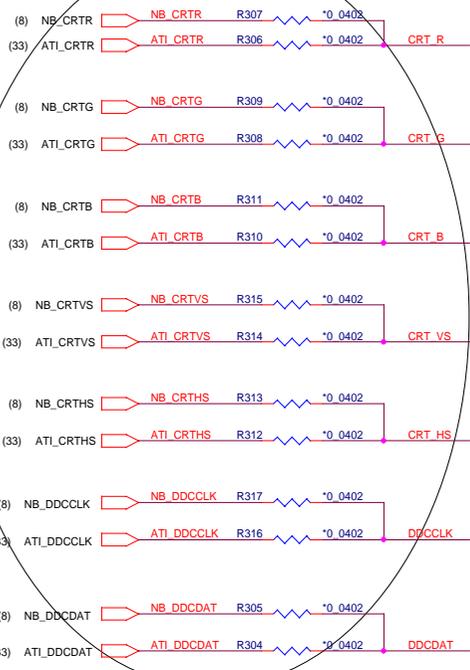
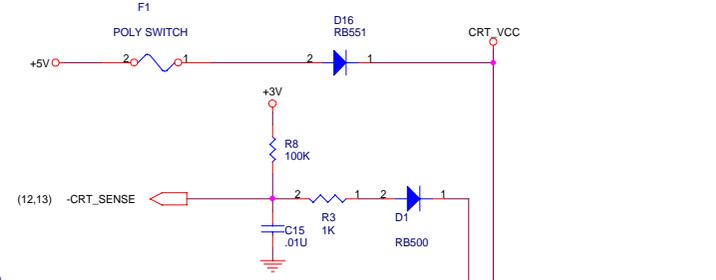
The voltage level of VLREF\_SB is 0.9V







**POSISTOR 0.2A (RC0603)**

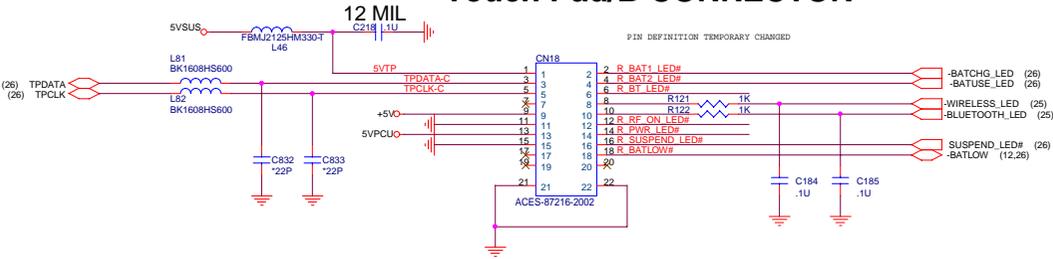


**PROJECT : Z13**  
**Quanta Computer Inc.**

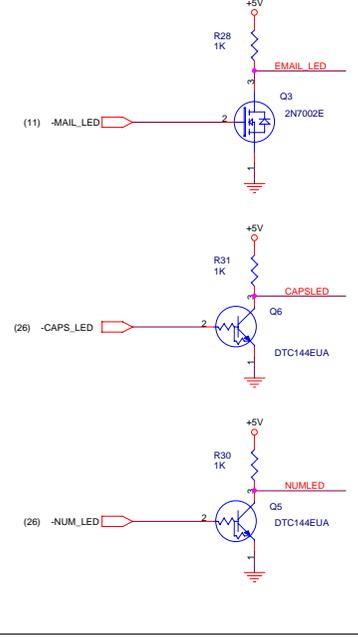
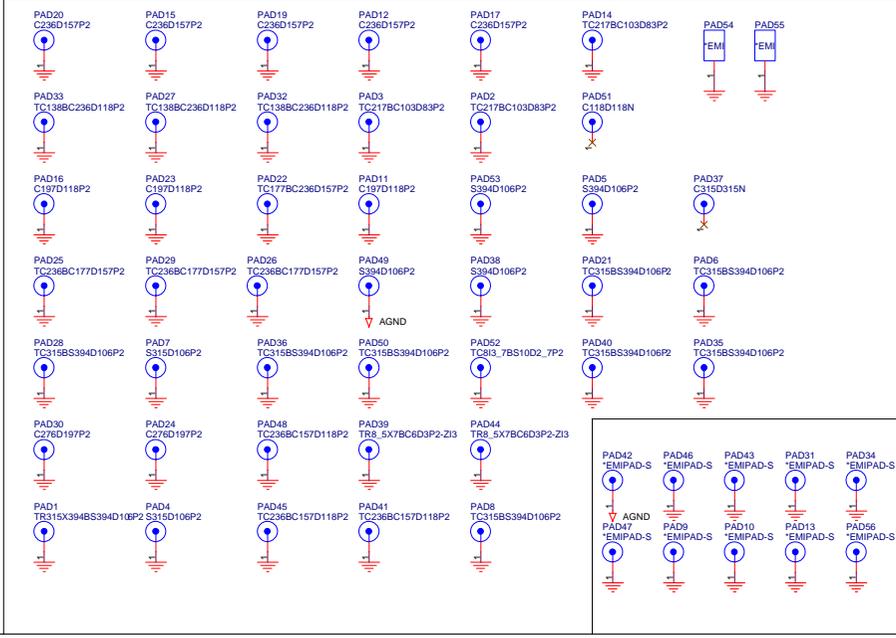
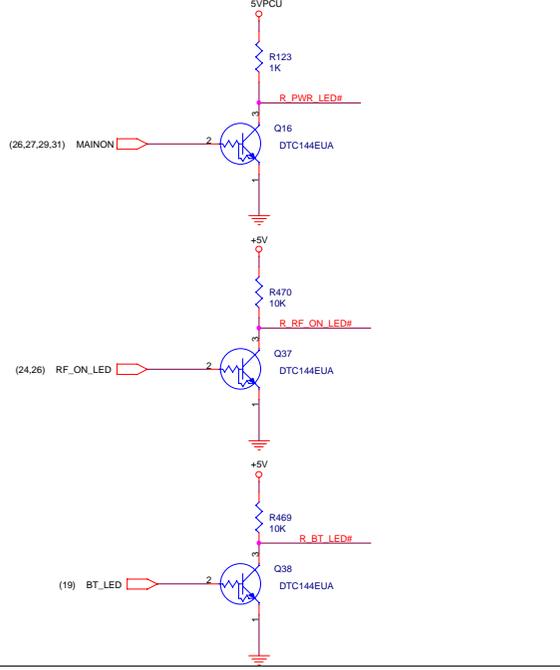
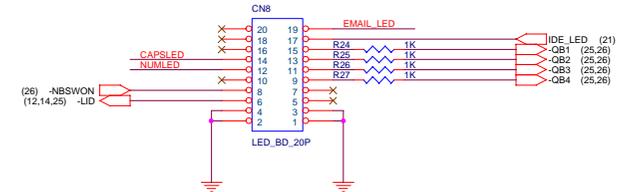
Size	Document Number	Rev
	<b>CRT PORT &amp; TV-OUT</b>	2A
Date:	Wednesday, September 24, 2003	Sheet 15 of 38



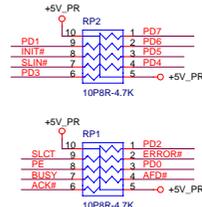
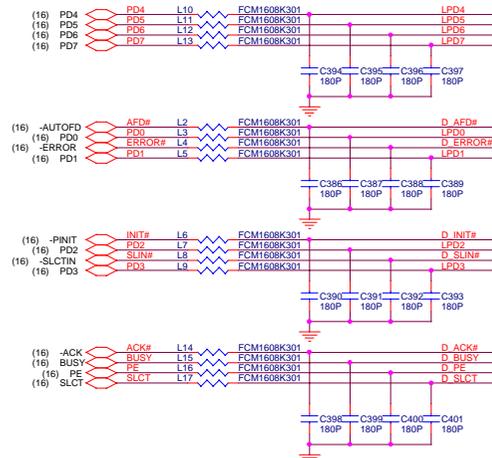
# Touch Pad/B CONNECTOR



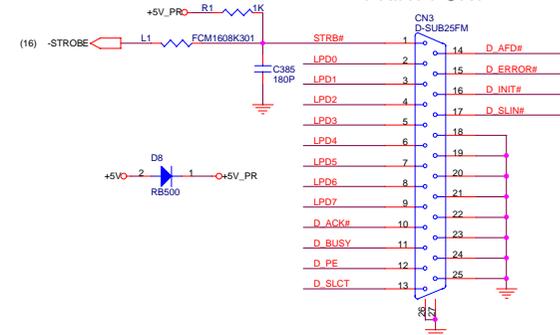
# LED/B CONNECTOR



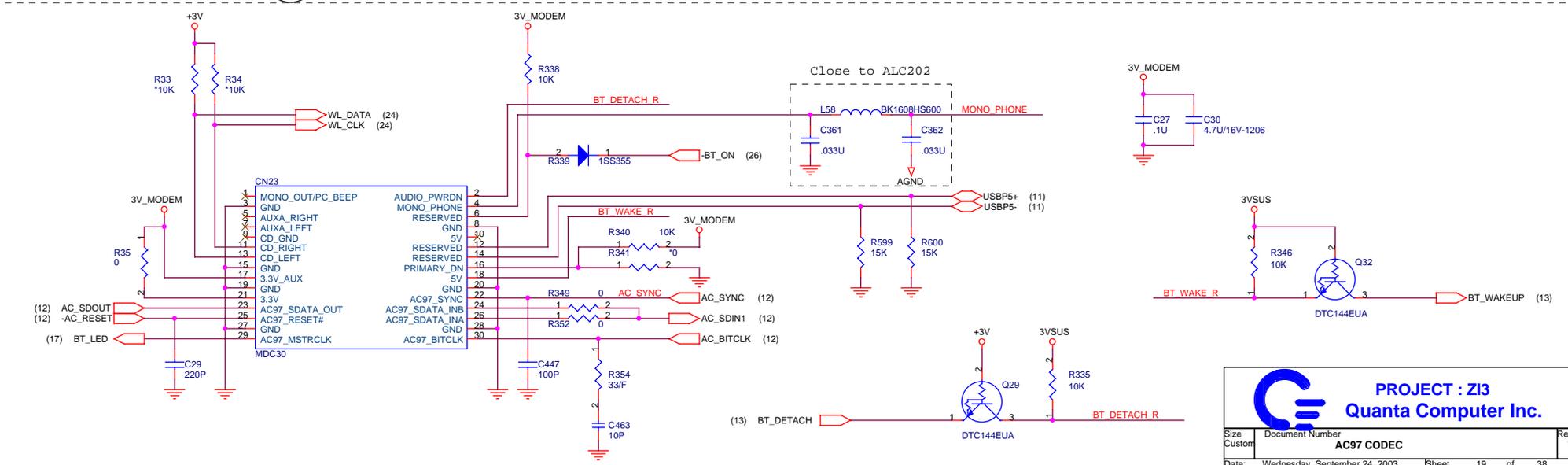
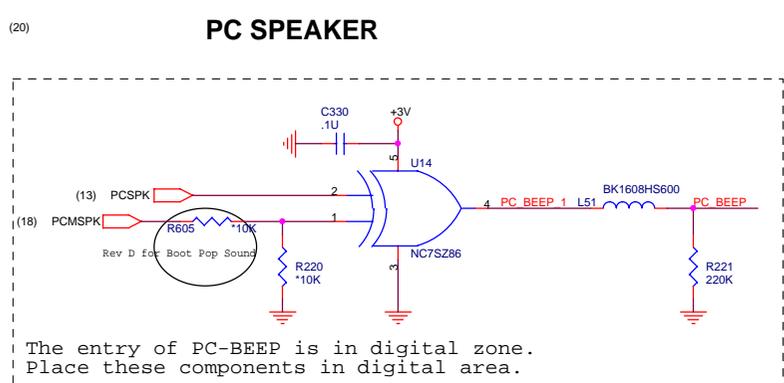
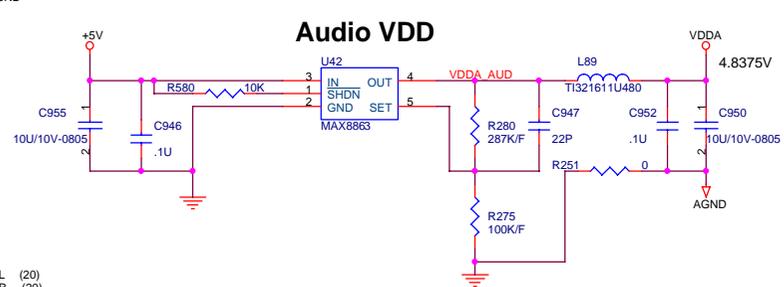
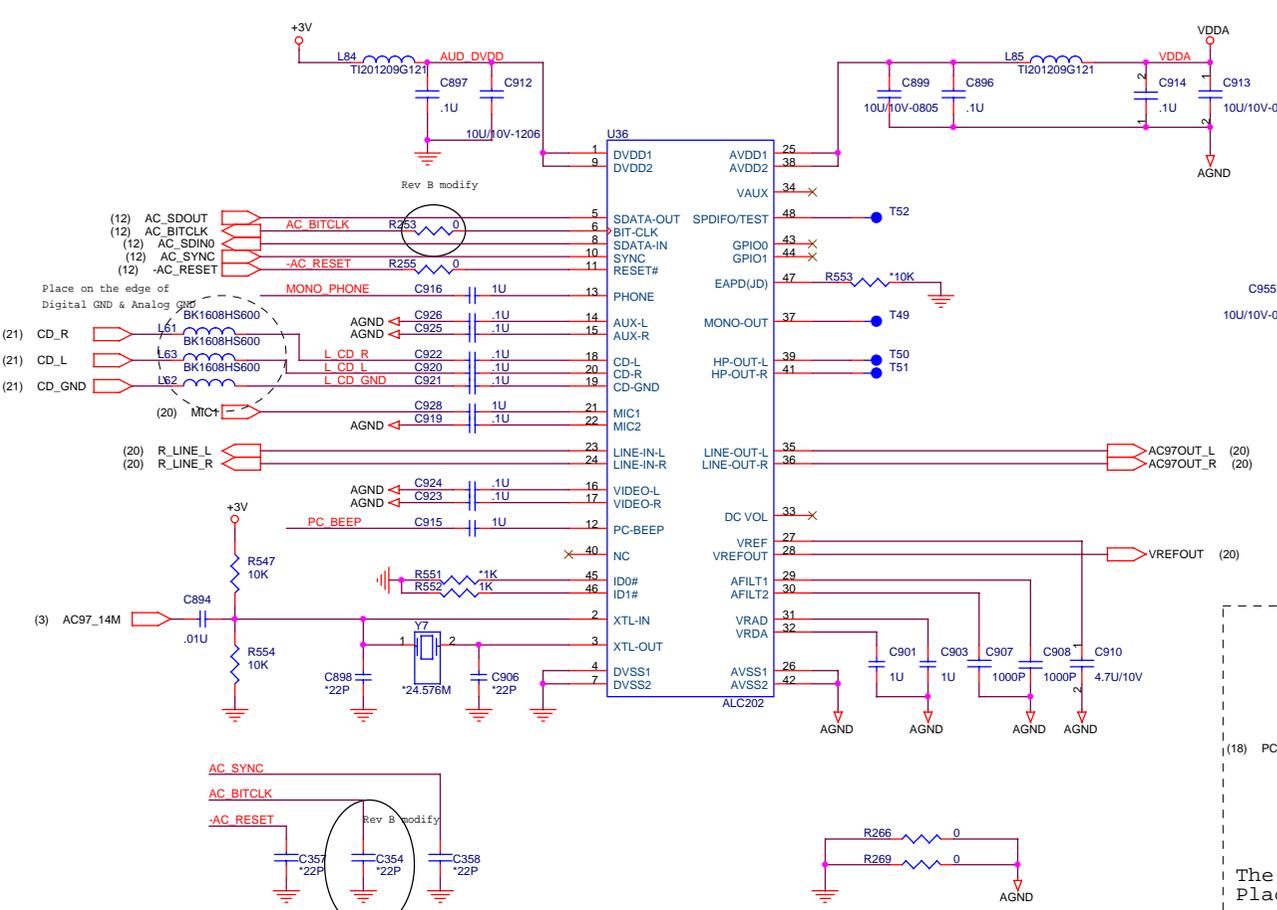
# LPT



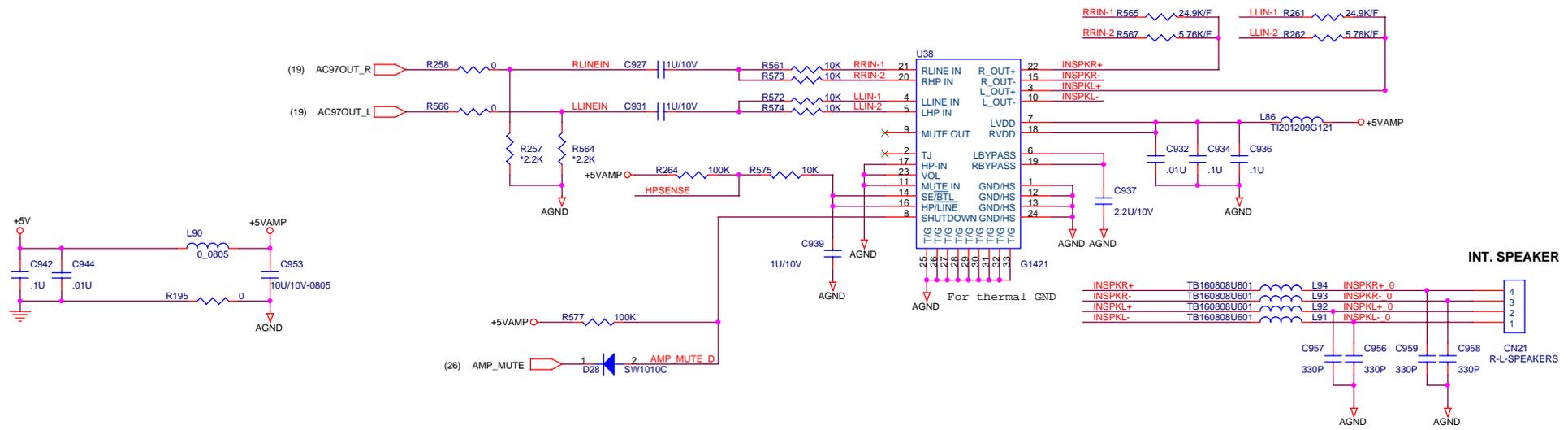
# PRINT PORT



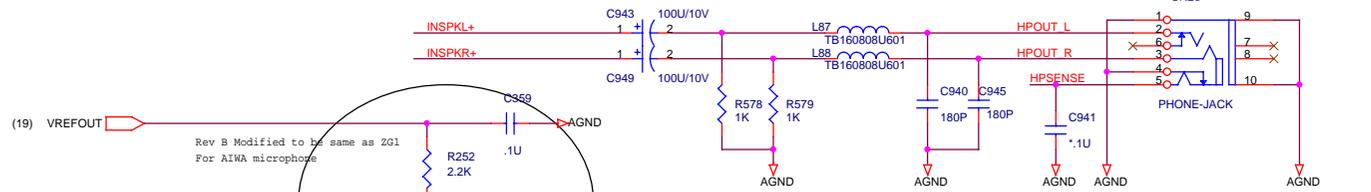




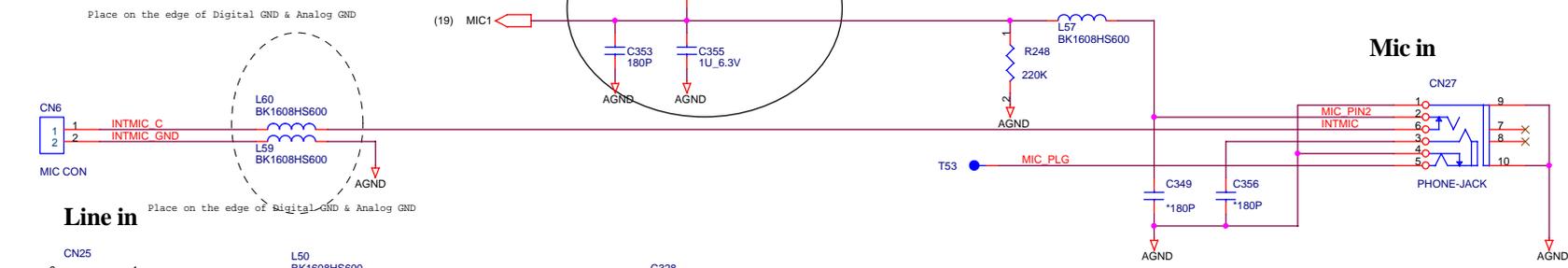
# Audio amplifier



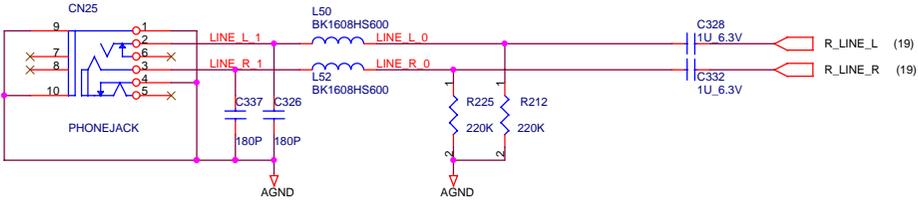
## Headphone out



## Mic in

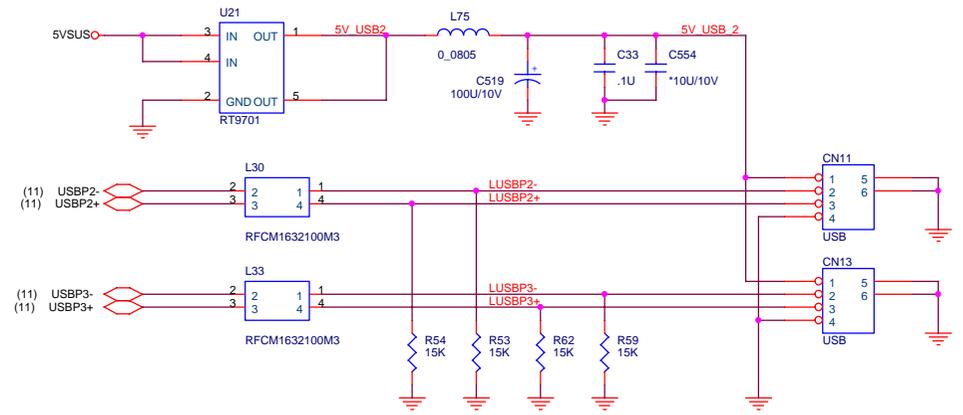
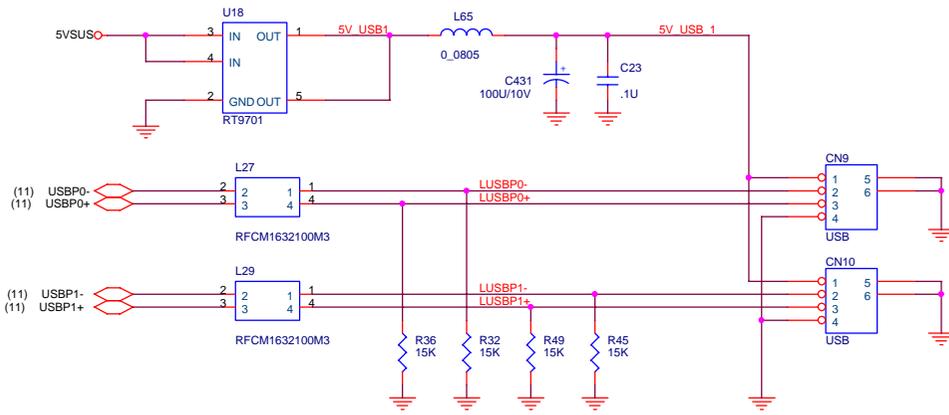


## Line in

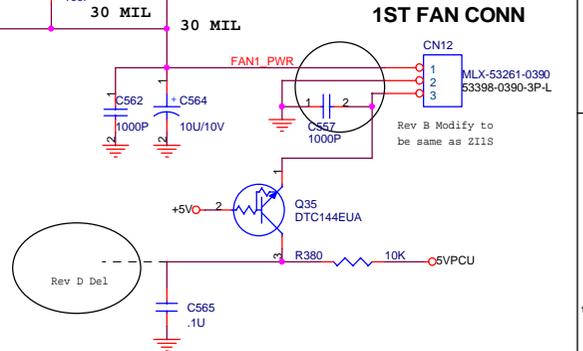
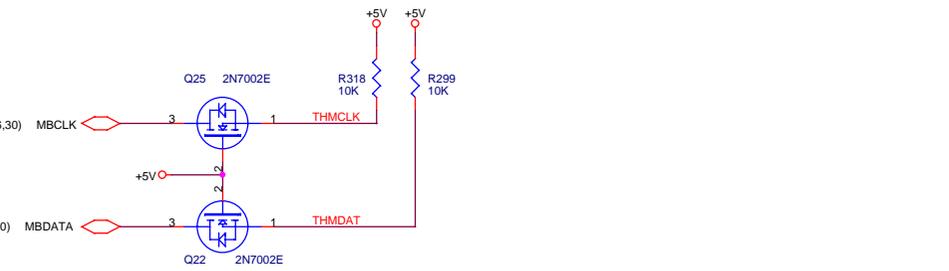
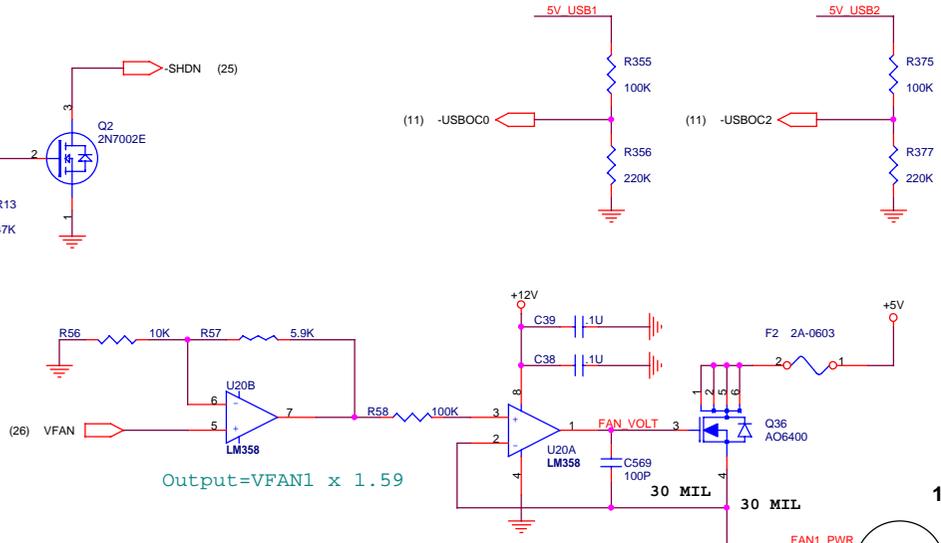
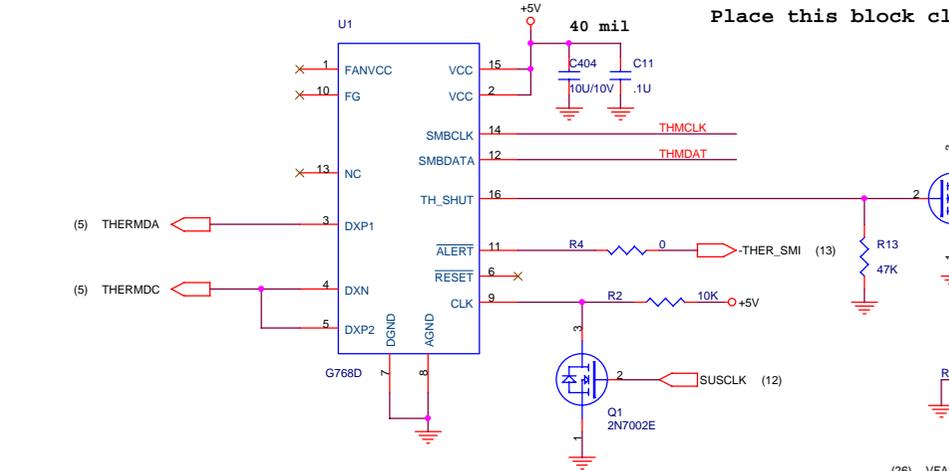


**PROJECT : Z13**  
**Quanta Computer Inc.**





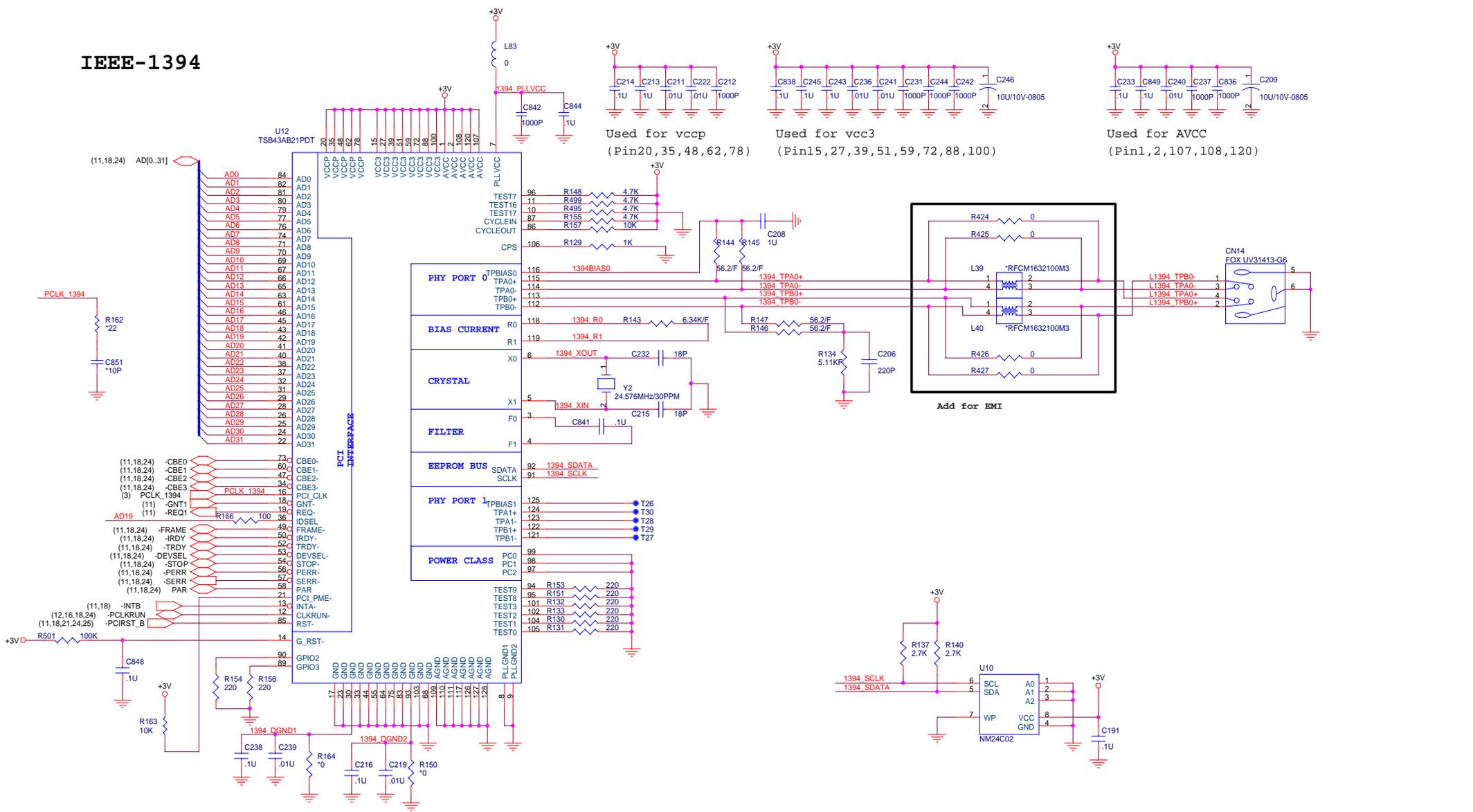
Place this block close to CPU



**PROJECT : ZI3**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
<b>USB &amp; FAN</b>		
Date: Wednesday, September 24, 2003	Sheet 22 of 38	

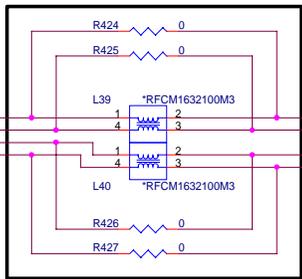
# IEEE-1394



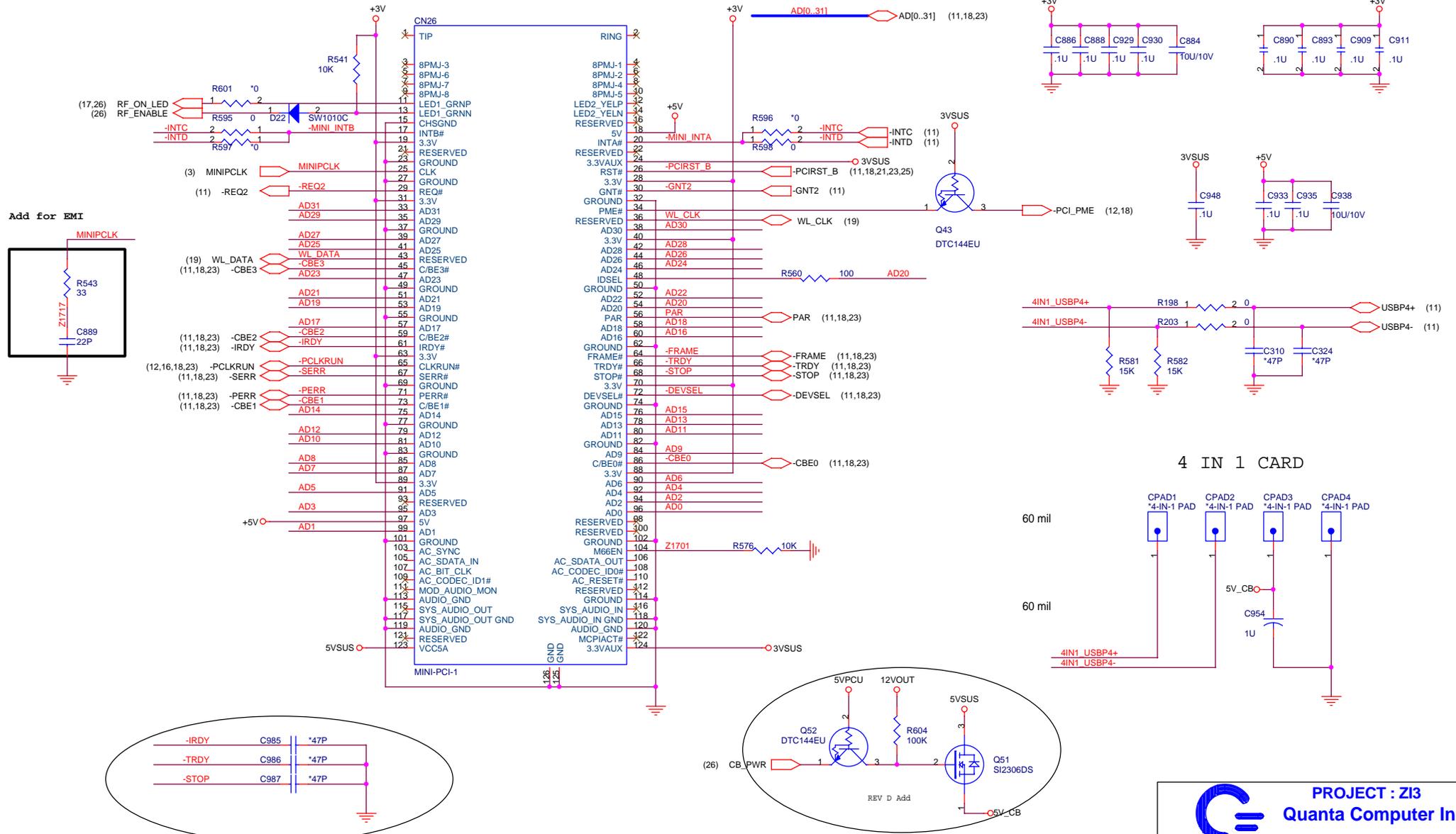
Used for vccp  
(Pin20, 35, 48, 62, 78)

Used for vcc3  
(Pin15, 27, 39, 51, 59, 72, 88, 100)

Used for AVCC  
(Pin1, 2, 107, 108, 120)

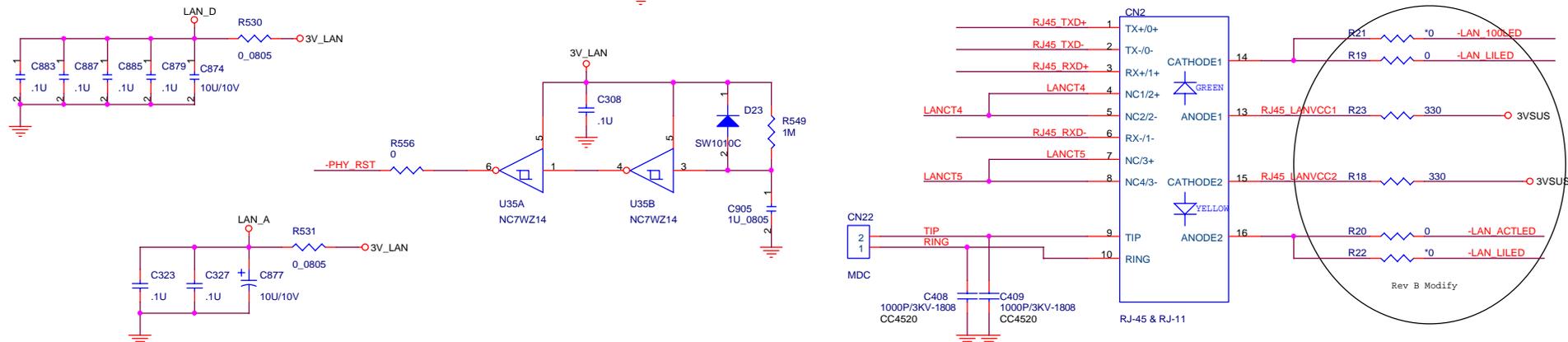
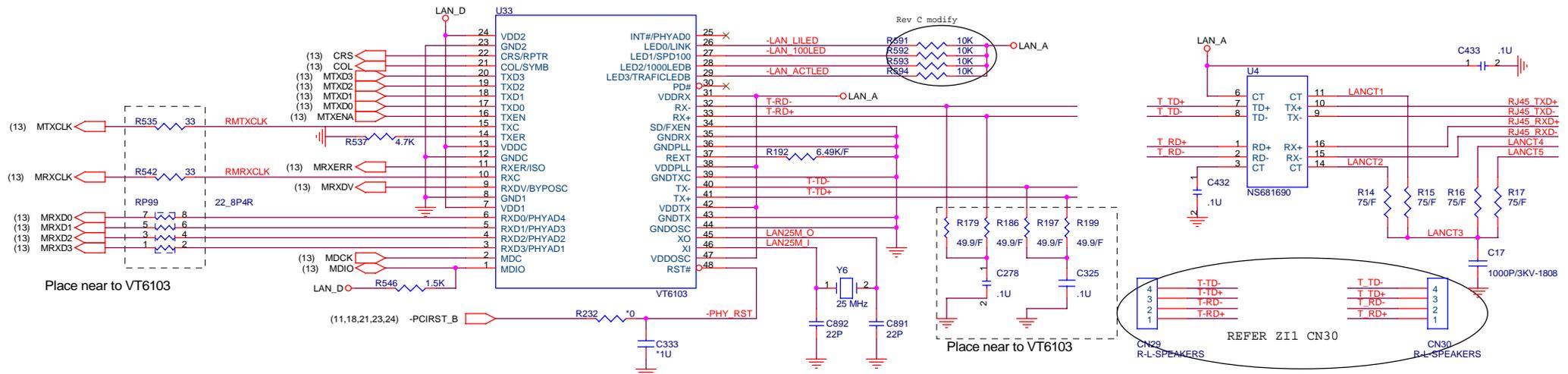


# TYPE III MINI PCI SOCKET

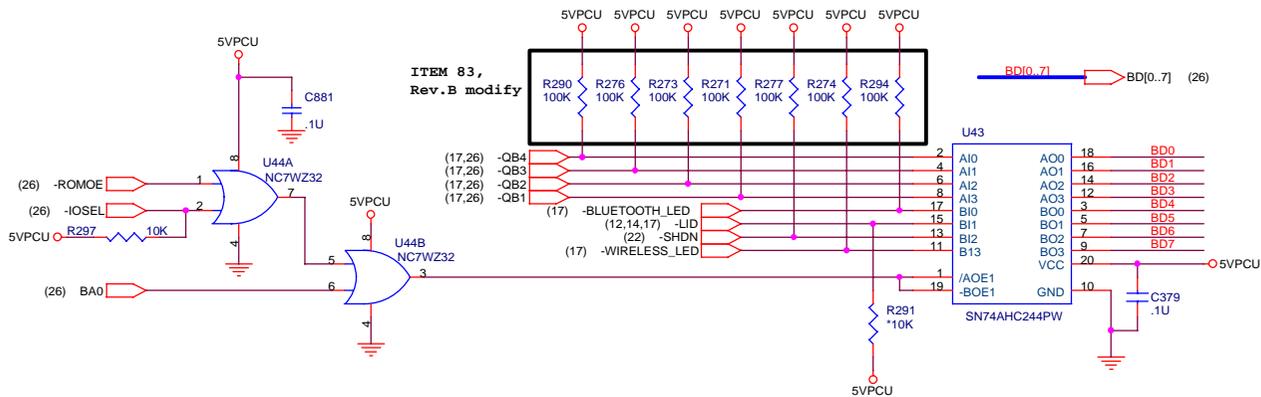


**PROJECT : Z13**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 2A
<b>MINI PCI, 4 IN 1 CARD</b>		
Date: Wednesday, September 24, 2003	Sheet 24 of 38	



### 570 EXP. IO

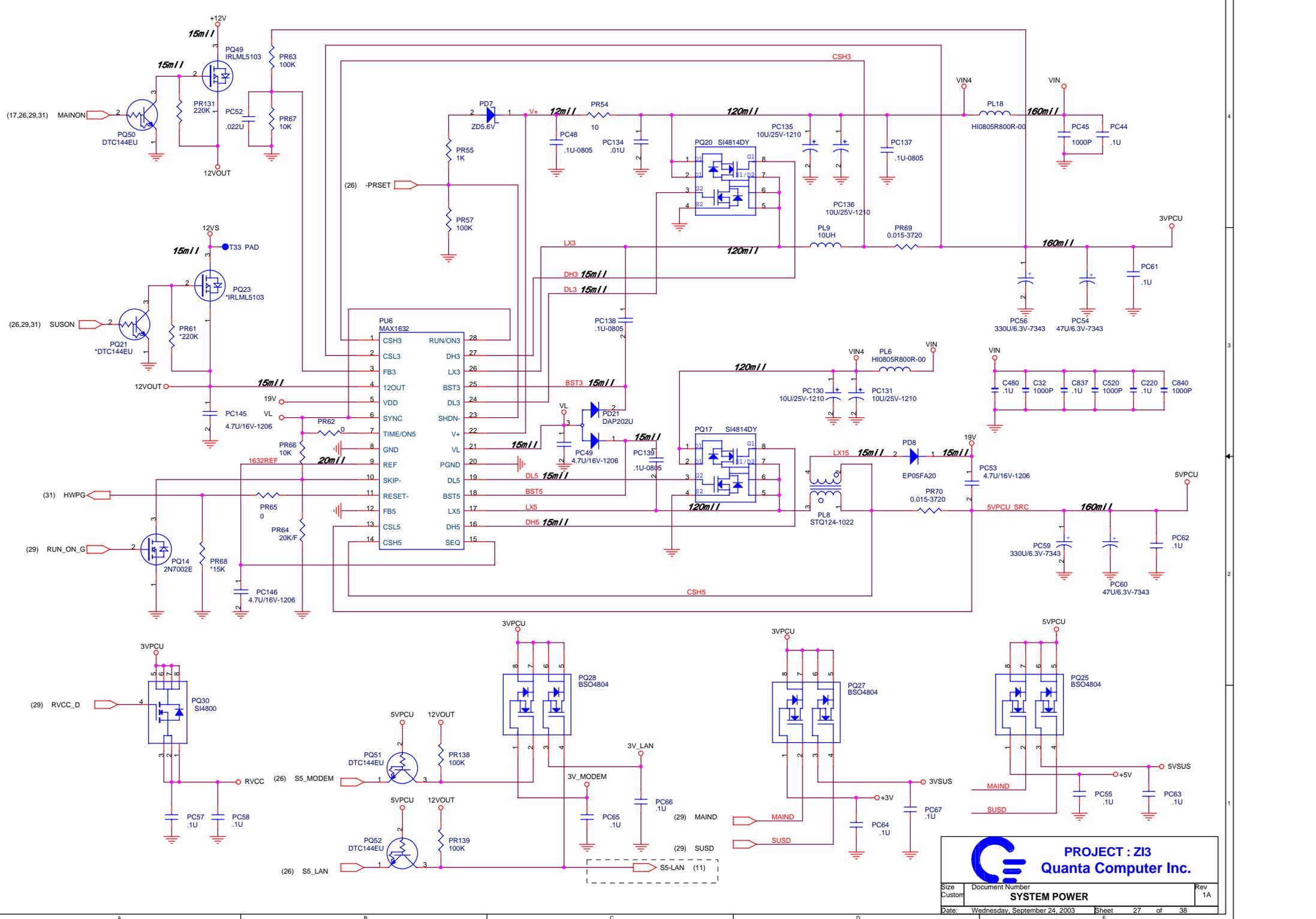




**PROJECT : Z13**  
Quanta Computer Inc.

Size A3	Document Number <b>LAN PHY VT6103 + RJ11&amp;RJ45, 570 EXP. IO</b>	Rev 2A
Date: Wednesday, September 24, 2003 Sheet 25 of 38		

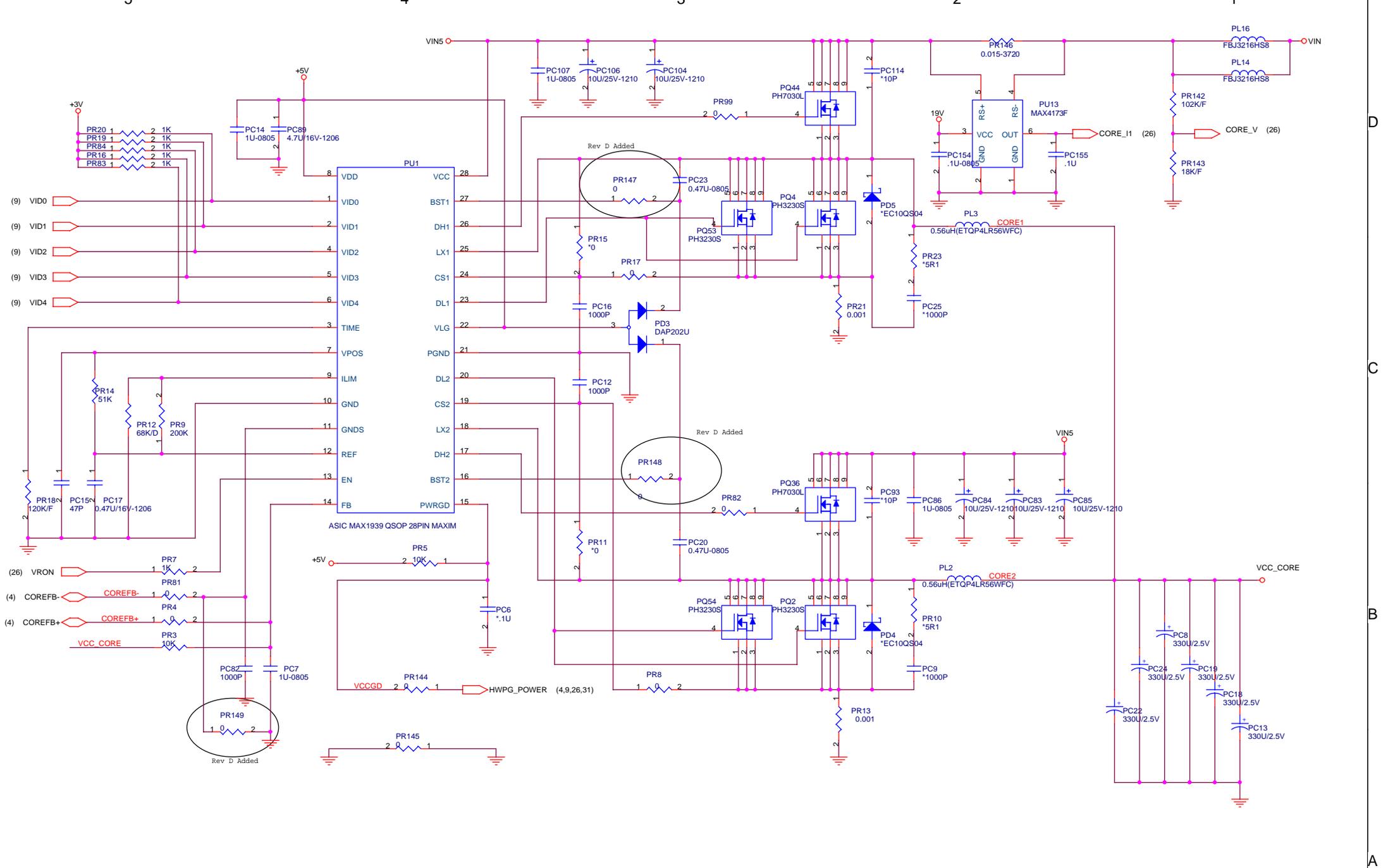


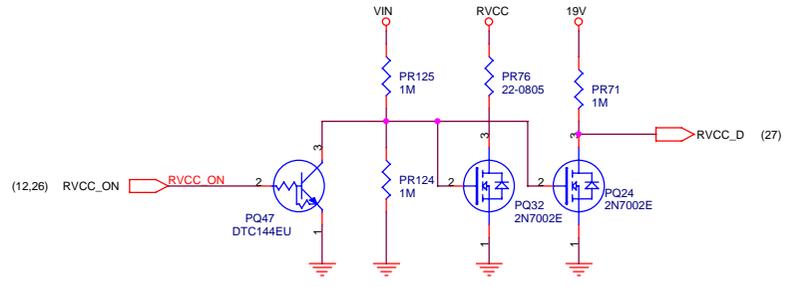
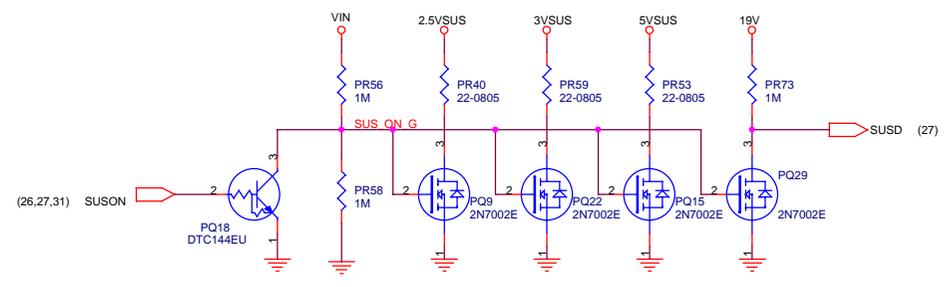
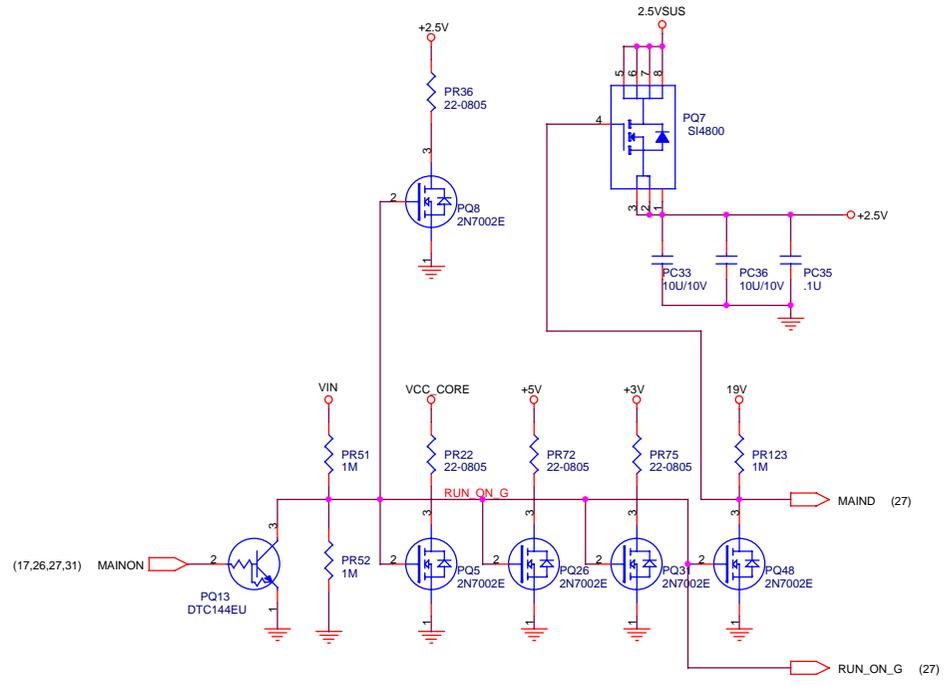
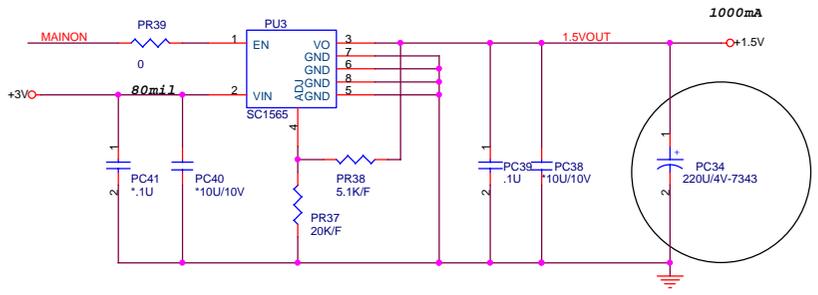
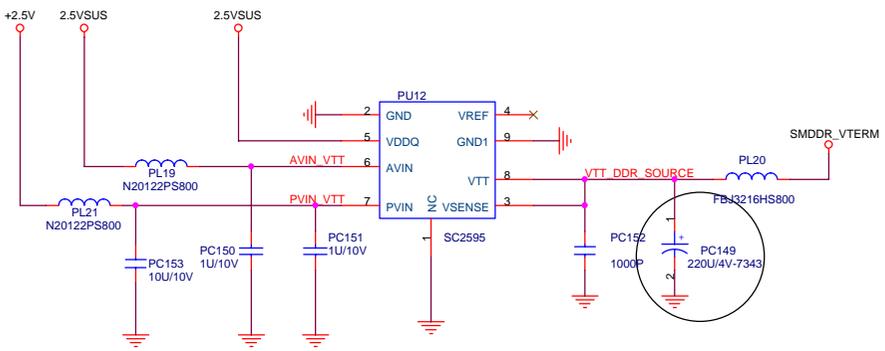
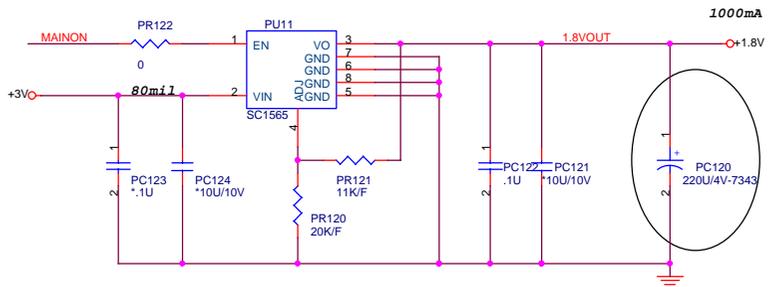




**PROJECT : Z13**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>SYSTEM POWER</b>	Rev 1A
Date:	Wednesday, September 24, 2003	Sheet 27 of 38

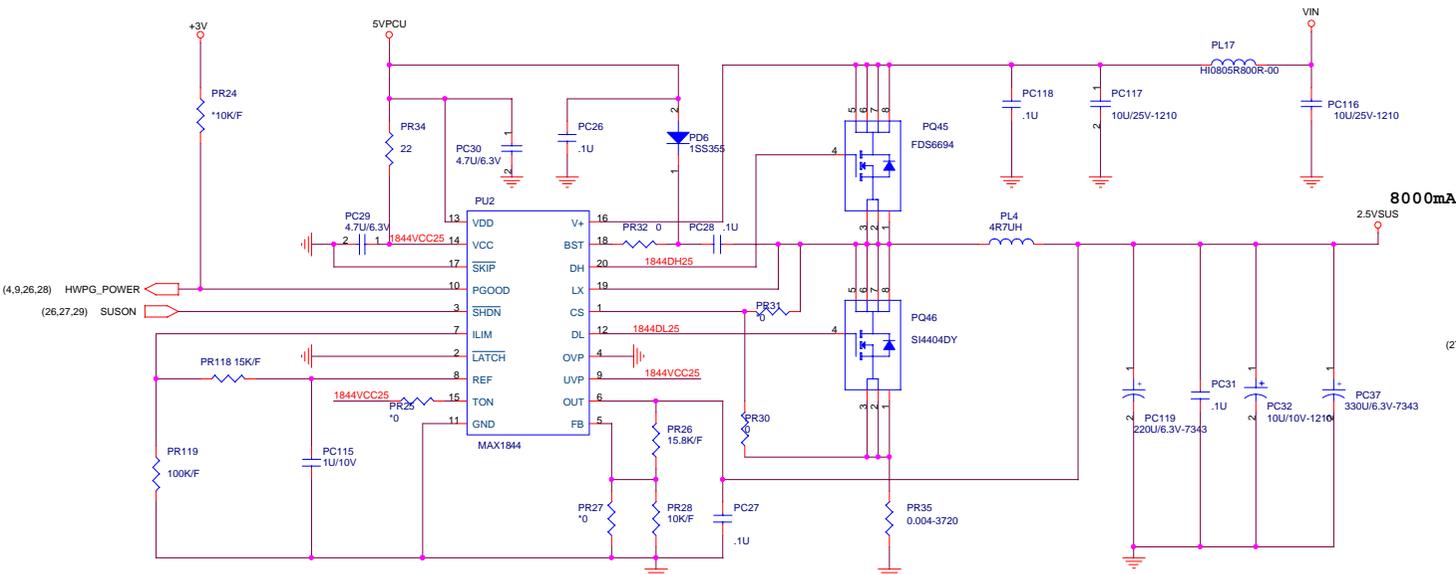




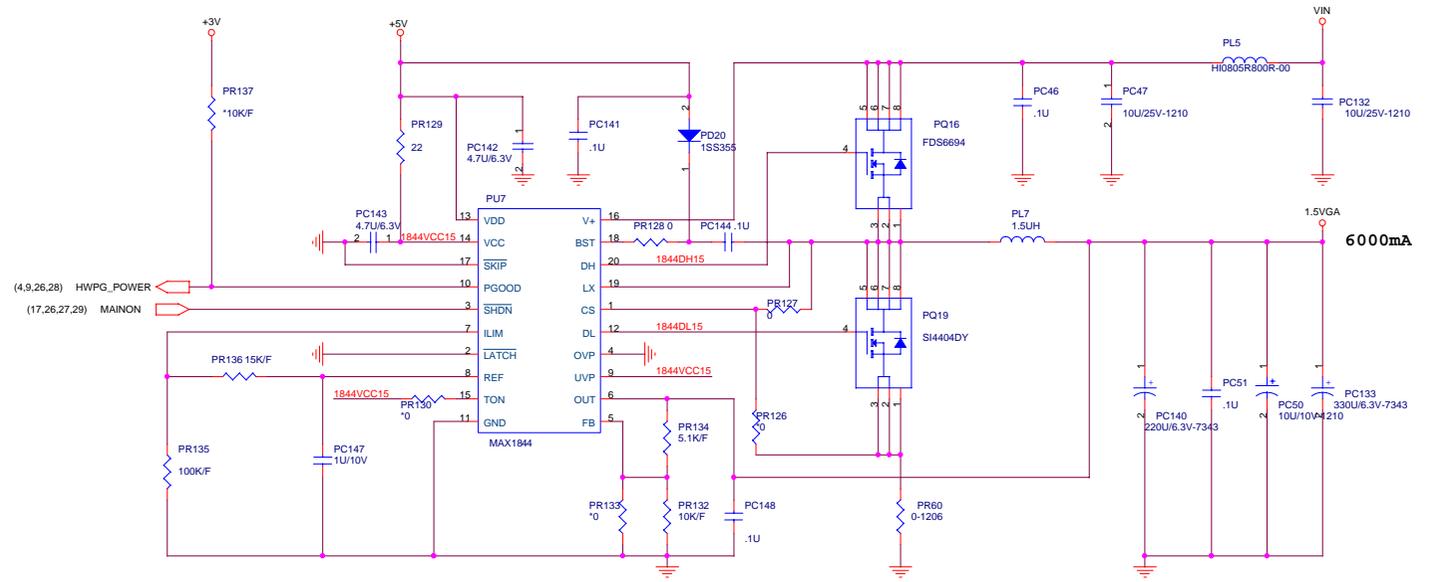
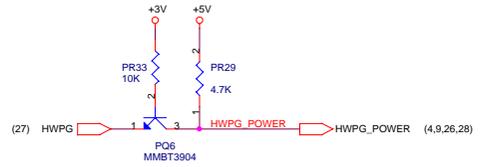
**PROJECT : Z13**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
<b>DISCHARGE CIRCUIT</b>		
Date:	Wednesday, September 24, 2003	Sheet 29 of 38



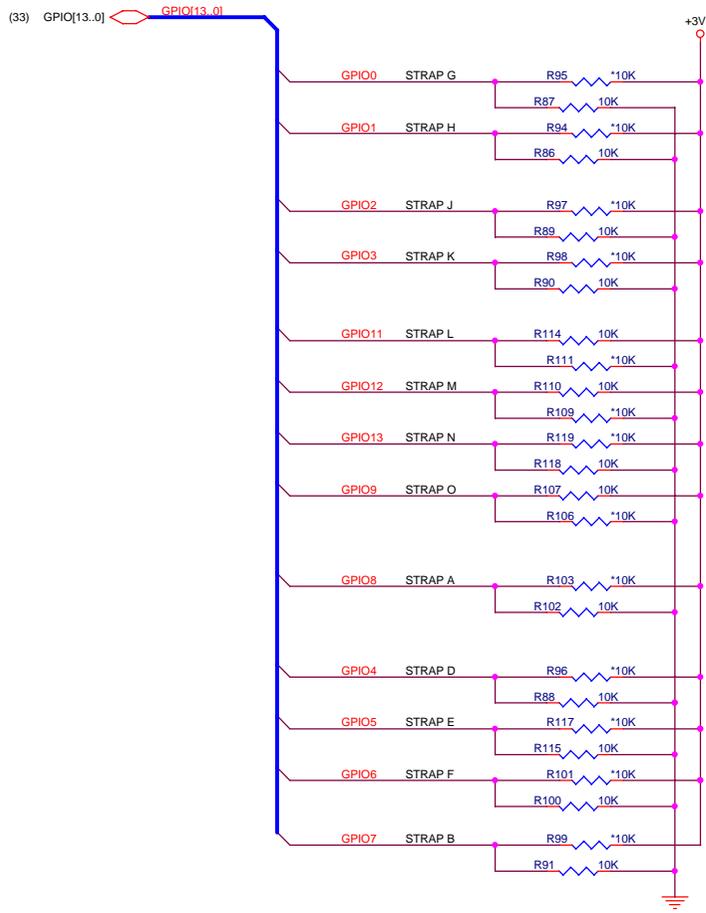


8000mA



6000mA

# OPTION STRAPS



STRAP H	STRAP G	AGP1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK)
LOW	LOW	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP K	STRAP J	AGP CLOCK PHASE ADJUSTMENT BETWEEN X1 AND X2 CLOCK
LOW	LOW	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP O	STRAP N	STRAP M	STRAP L	ROM IDENTIFIER
HIGH	LOW	HIGH	HIGH	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP A	ID DISABLE
LOW	NORMAL OPERATION (DEFAULT)
HIGH	SHUT DOWN

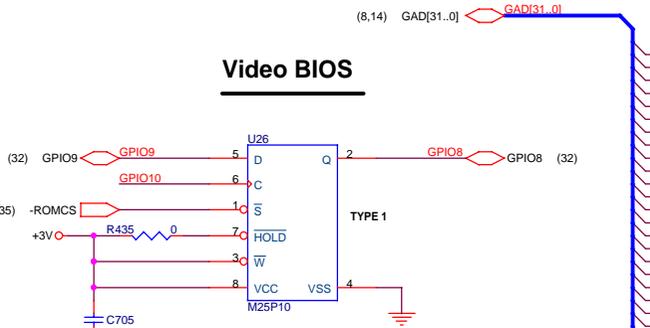
STRAP D	STRAP E	STRAP F	BUS_TYPE
LOW	LOW	LOW	(DEFAULT) SEE PIN BASED STRAPS IN PINOUT SPEC

STRAP B	VGA
LOW	ENABLE (DEFAULT)
HIGH	DISABLE

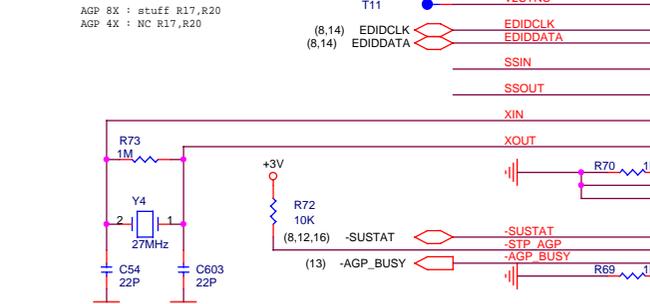
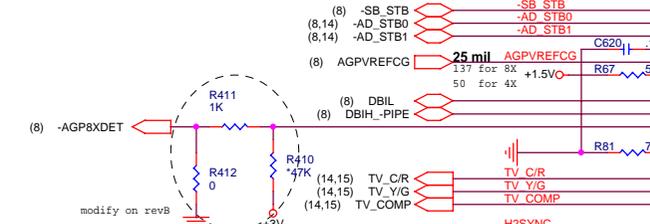
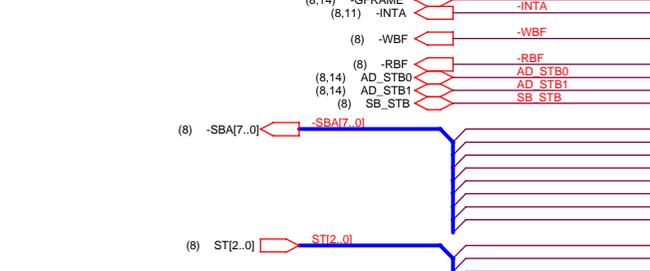
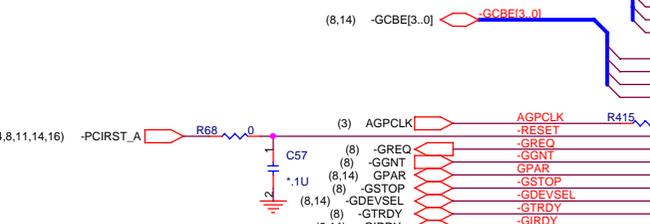
NOTE: THE M7 SUPPORTS THE USE OF STRAP RESISTORS (AS AN ALTERNATIVE TO CUSTOMIZED BIOS) TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS SUBSYSTEM. THE USE OF EXTERNAL STRAPS PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE UPGRADE. STRAPPED VALUES ARE LOADED INTO INTERNAL REGISTERS ON THE FIRST PCI COMMAND AFTER RESET# IS INACTIVE.

NOTE:  
THE I/O BUFFERS USE INTERNAL PULLDOWN RESISTOR. THIS DICTATES THE FOLLOWING STRAP CONFIGURATION:  
STRAP TO VCC VIA 10K RESISTOR.  
THIS PROVIDES THE LOGIC LEVELS SHOWN:  
'0' WHEN 10K RESISTOR NOT INSTALLED  
'1' WHEN 10K RESISTOR INSTALLED.

### Video BIOS



### SERIAL EEPROM BIOS



(8,14) GAD[31..0]  $\rightarrow$  GAD[31..0]

(8,14) -GCEBE[3..0]  $\rightarrow$  -GCEBE[3..0]

(3) AGPCLK  $\rightarrow$  AGPCLK

(8) STI[2..0]  $\rightarrow$  STI[2..0]

(8) -SB\_STB  $\rightarrow$  -SB\_STB

(8) -AGP8XDET  $\rightarrow$  -AGP8XDET

(8,14) EDIDCLK  $\rightarrow$  EDIDCLK

(8,14) EDIDDATA  $\rightarrow$  EDIDDATA

(13) -AGP\_BUSY  $\rightarrow$  -AGP\_BUSY

- GAD0 H29
- GAD1 H28
- GAD2 J28
- GAD3 J28
- GAD4 K28
- GAD5 K28
- GAD6 L28
- GAD7 L28
- GAD8 P28
- GAD9 P28
- GAD10 P28
- GAD11 R28
- GAD12 R28
- GAD13 R28
- GAD14 T28
- GAD15 U28
- GAD16 N28
- GAD17 R26
- GAD18 P26
- GAD19 P26
- GAD20 R25
- GAD21 T25
- GAD22 T26
- GAD23 U25
- GAD24 V27
- GAD25 W26
- GAD26 W25
- GAD27 Y26
- GAD28 Y25
- GAD29 A26
- GAD30 A25
- GAD31 AA27

- GCEBE0 N29
- GCEBE1 U28
- GCEBE2 P28
- GCEBE3 U26

- AGPCLK AG30
- RESET AG28
- GREQ AF28
- GGNT AD26
- GPARG M25
- GSTOP N26
- GDEVSEL V29
- GTRDY V28
- GIRDY W29
- GFRAME W28
- INTA AE26

- WBF AC26
- RBF AE29
- AD\_STB0 M28
- AD\_STB1 V25
- SB\_STB AB29

- SBA0 AD28
- SBA1 AD29
- SBA2 AC28
- SBA3 AC29
- SBA4 AA28
- SBA5 AA29
- SBA6 Y28
- SBA7 Y29

- ST0 AF28
- ST1 AD27
- ST2 AE28

- SB\_STB AB28
- AD\_STB0 M29
- AD\_STB1 V26

- AGPVREFCG M26
- AGPTTEST M27
- DBI\_LO AB26
- DBI\_HI AB25
- AGP8X\_DET# AC25

- R2SET AK21
- C\_R Y23
- TV\_C/R AJ23
- TV\_Y/G AJ22
- TV\_COMP AK22

- H2SYNC AJ24
- V2SYNC AK24
- EDIDCLK AG23
- EDIDDATA AG24

- SSIN AK25
- SSOUT AJ25
- XIN AH28
- XOUT AJ29

- TESTEN AH27
- EA NC
- BB NC
- AE25 NC

- SUS\_STAT# AG26
- STP\_AGP# AH30
- AGP\_BUSY# AG29
- NC AG29

M9+XC-708P

- GPIO0 AH5
- GPIO1 AH5
- GPIO2 AJ4
- GPIO3 AK4
- GPIO4 AH4
- GPIO5 AF4
- GPIO6 AJ3
- GPIO7 AK3
- GPIO8 AH3
- GPIO9 AJ2
- GPIO10 AH2
- GPIO11 AH1
- GPIO12 AG3
- GPIO13 AG1
- GPIO14 AG2
- GPIO15 AF3
- GPIO16 AF2

- AE10
- AH6
- AK6
- AH7
- AK7
- AJ7
- AH8
- AJ8
- AH9
- AK9
- AH10
- AE6
- AG6
- AF6
- AE7
- AE8
- AG8
- AF8
- AF9
- AG10
- AF10

- ZV\_LCDDATA0
- ZV\_LCDDATA1
- ZV\_LCDDATA2
- ZV\_LCDDATA3
- ZV\_LCDDATA4
- ZV\_LCDDATA5
- ZV\_LCDDATA6
- ZV\_LCDDATA7
- ZV\_LCDDATA8
- ZV\_LCDDATA9
- ZV\_LCDDATA10
- ZV\_LCDDATA11
- ZV\_LCDDATA12
- ZV\_LCDDATA13
- ZV\_LCDDATA14
- ZV\_LCDDATA15
- ZV\_LCDDATA16
- ZV\_LCDDATA17
- ZV\_LCDDATA18
- ZV\_LCDDATA19
- ZV\_LCDDATA20
- ZV\_LCDDATA21
- ZV\_LCDDATA22
- ZV\_LCDDATA23

- ZV\_LCDCNTL0
- ZV\_LCDCNTL1
- ZV\_LCDCNTL2
- ZV\_LCDCNTL3
- NC

- TXOUT\_L0N
- TXOUT\_L0P
- TXOUT\_L1N
- TXOUT\_L1P
- TXOUT\_L2N
- TXOUT\_L2P
- TXOUT\_L3N
- TXOUT\_L3P
- TXCLK\_LN
- TXCLK\_LP
- TXOUT\_U0N
- TXOUT\_U0P
- TXOUT\_U1N
- TXOUT\_U1P
- TXOUT\_U2N
- TXOUT\_U2P
- TXOUT\_U3N
- TXOUT\_U3P
- TXCLK\_UN
- TXCLK\_UP

- DIGON
- BLON
- TX0M
- TX0P
- TX1M
- TX1P
- TX2M
- TX2P
- TXCM
- TXCP

- DDC2CLK
- DDC2DATA
- HPD1
- DDC3CLK
- DDC3DATA
- R
- G
- B
- HSYNC
- VSYNC
- RSET
- DDC1DATA
- DDC1CLK
- EA
- NC
- AUXWIN

- DPLUS
- DMINUS
- NC

THERM

GPIO13..0]  $\rightarrow$  GPIO[13..0]

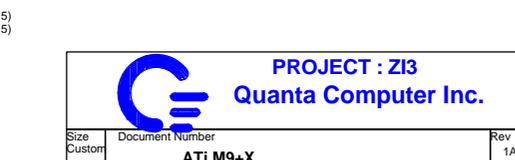
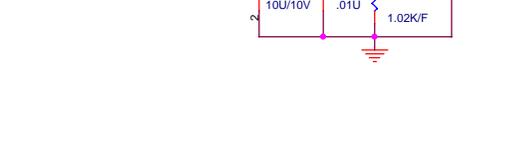
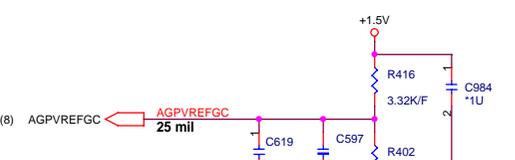
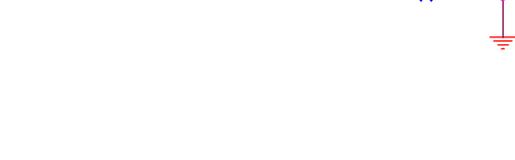
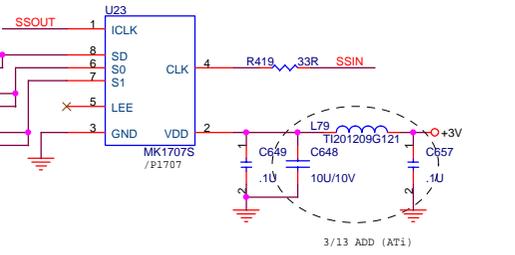
Rev B modify

Rev B modify

remove MAX6657 on revB

GPIO[13:10] AND ZV\_LCDDATA[23:16] MUST BE AVAILABLE FOR DEBUGGING CONNECTIONS , IF UNUSED , ENSURE TEST POINTS FOR ACCESSIBILITY

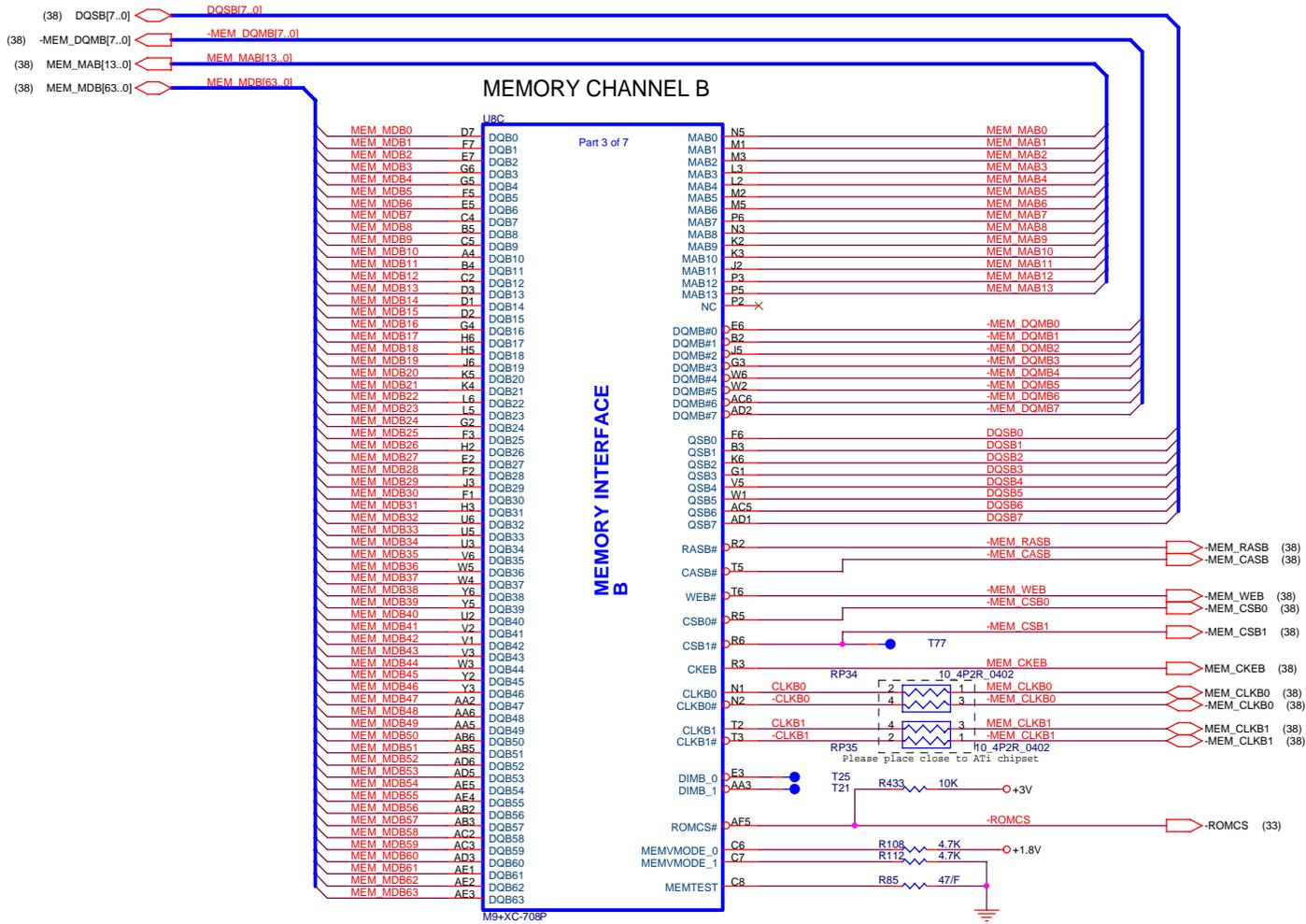
### SSC



PROJECT : Z13  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M9+X	1A
Date:	Wednesday, September 24, 2003	Sheet 33 of 38



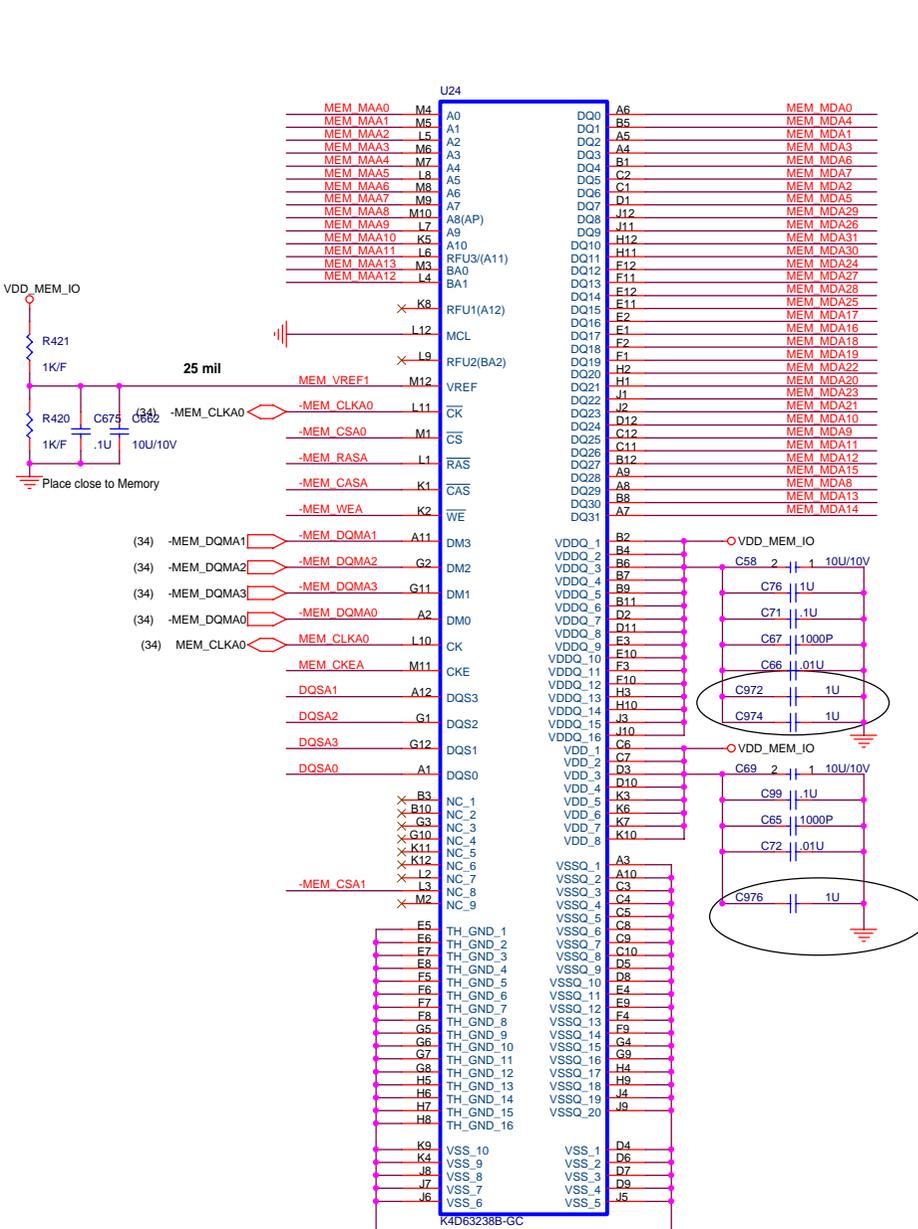


MEMMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

**PROJECT : Z13**  
**Quanta Computer Inc.**

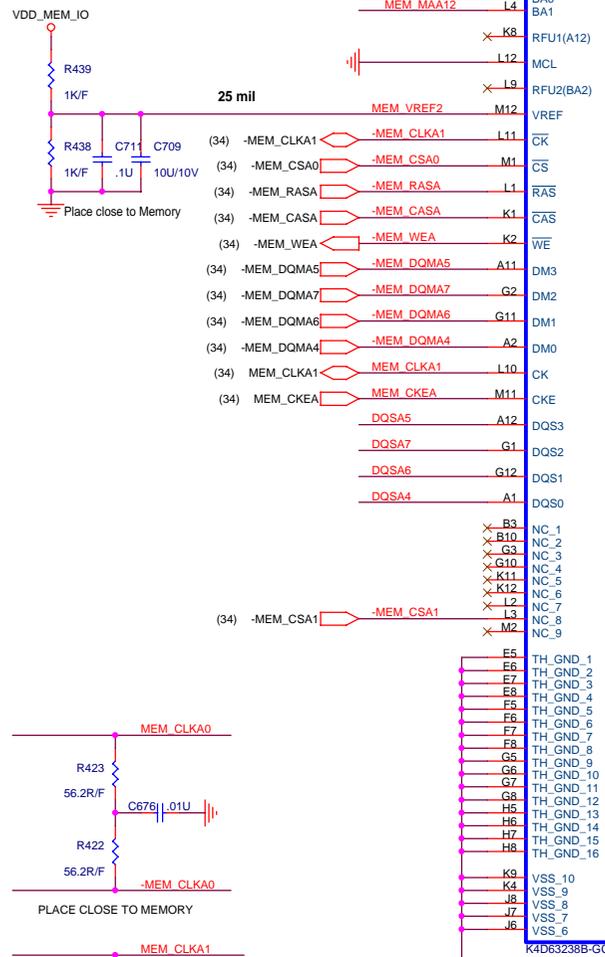
Size Custom	Document Number	Rev
	<b>M9+X Memory Bus B</b>	1A
Date:	Wednesday, September 24, 2003	Sheet 35 of 38



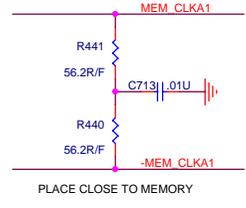
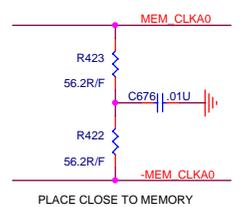


**4MX32 DDR BGA Memory**

- (34) MEM\_MAA[13..0] MEM\_MAA13..0
- (34) MEM\_MDA[63..0] MEM\_MDA63..0
- (34) DQSA[7..0] DQSA7..0



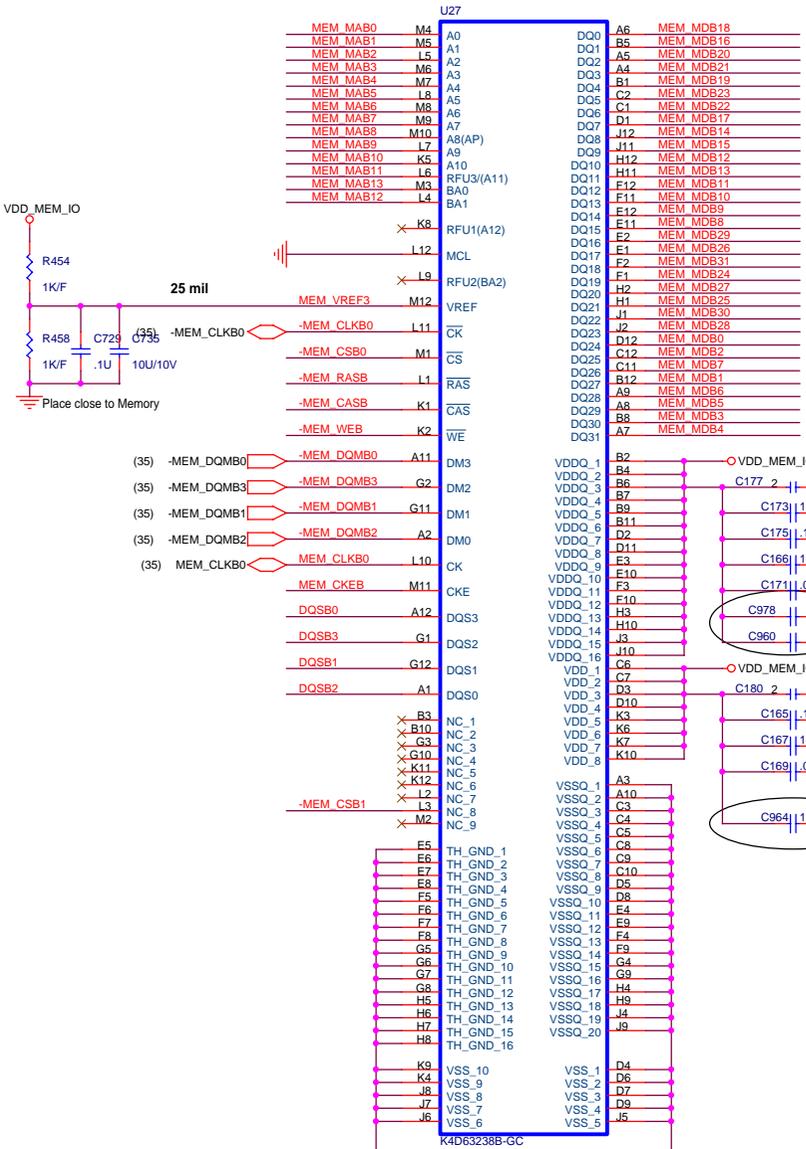
**4MX32 DDR BGA Memory**



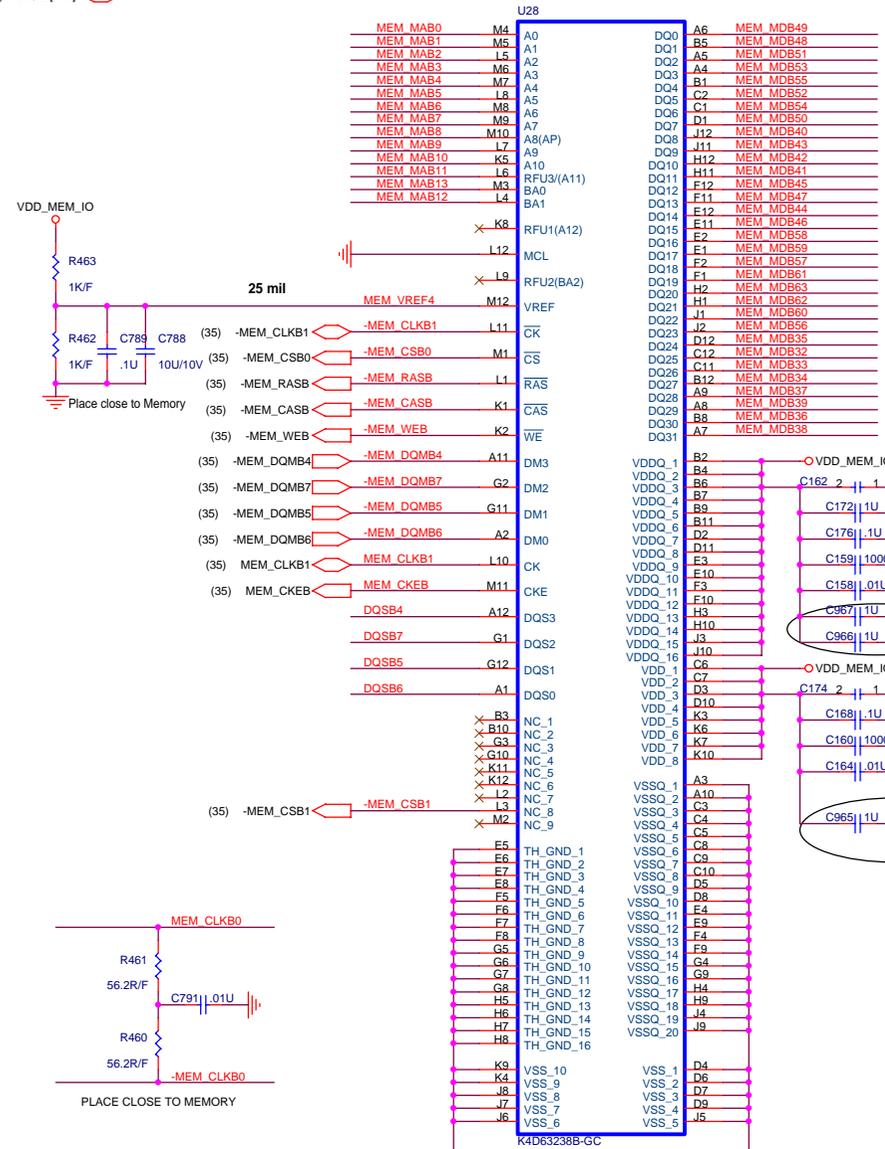
**PROJECT : ZI3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>Video DDR Memory A</b>	1A
Date:	Wednesday, September 24, 2003	Sheet 37 of 38

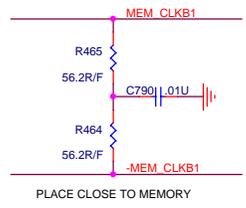
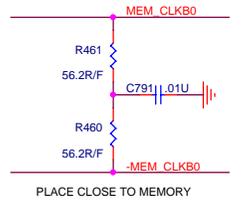
(35) MEM\_MAB[13..0] MEM\_MAB13..01  
 (35) MEM\_MDB[63..0] MEM\_MDB63..01  
 (35) DQS[7..0] DQS[7..0]



4MX32 DDR BGA Memory



4MX32 DDR BGA Memory



**PROJECT : Z13**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Video DDR Memory B</b>	Rev 1A
Date: Wednesday, September 24, 2003	Sheet 38 of 38	