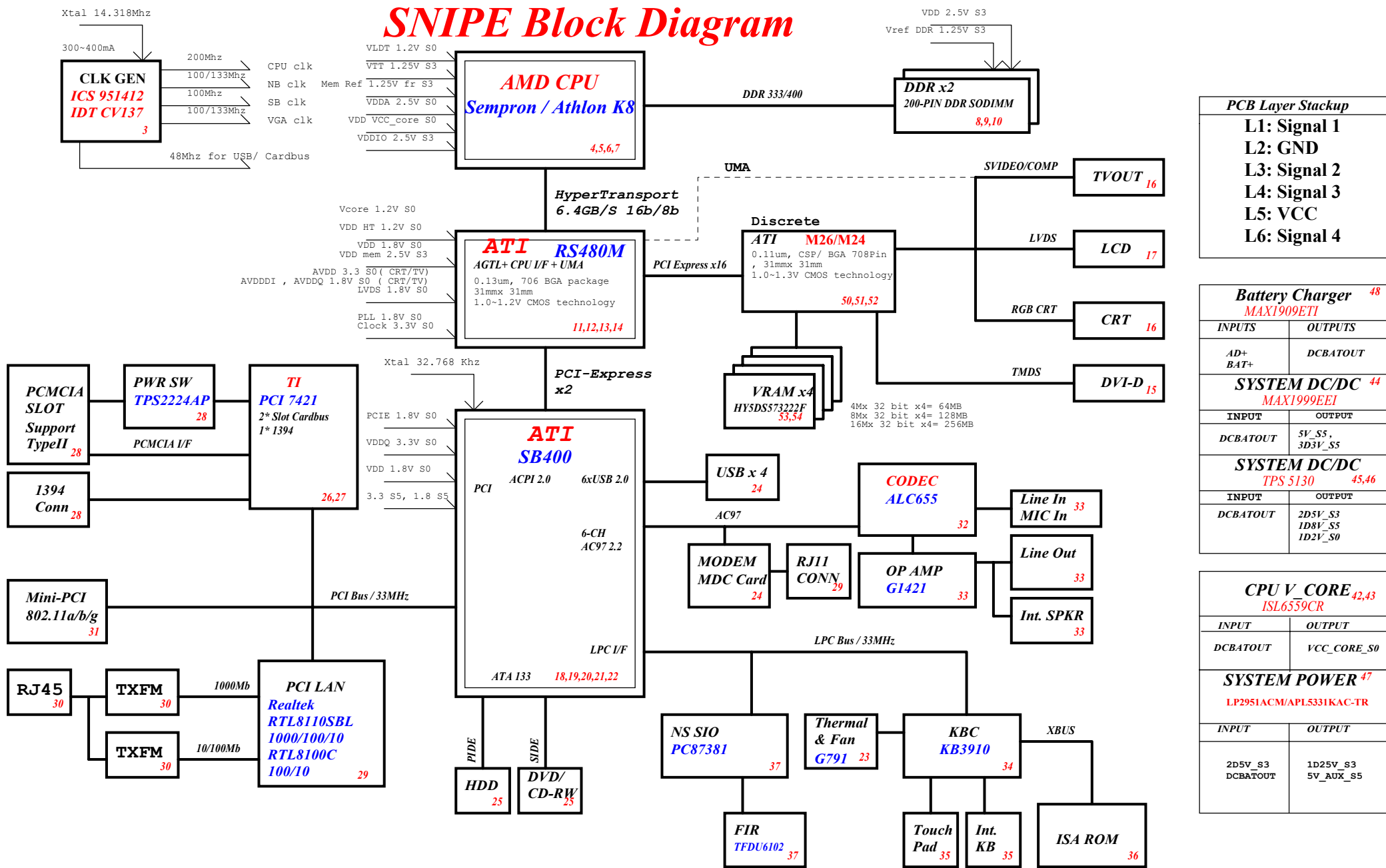


# SNIPE Block Diagram



**PCB Layer Stackup**

- L1: Signal 1
- L2: GND
- L3: Signal 2
- L4: Signal 3
- L5: VCC
- L6: Signal 4

**Battery Charger** 48  
MAX1909ETI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

**SYSTEM DC/DC** 44  
MAX1999EEI

INPUT	OUTPUT
DCBATOUT	5V_S5, 3D3V_S5

**SYSTEM DC/DC** 45,46  
TPS 5130

INPUT	OUTPUT
DCBATOUT	2D5V_S3 1D8V_S5 1D2V_S0

**CPU V CORE** 42,43  
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

**SYSTEM POWER** 47  
LP2951ACM/APL5331KAC-TR

INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **SNIPE** Rev: SA

Date: Monday, November 22, 2004 Sheet 1 of 56

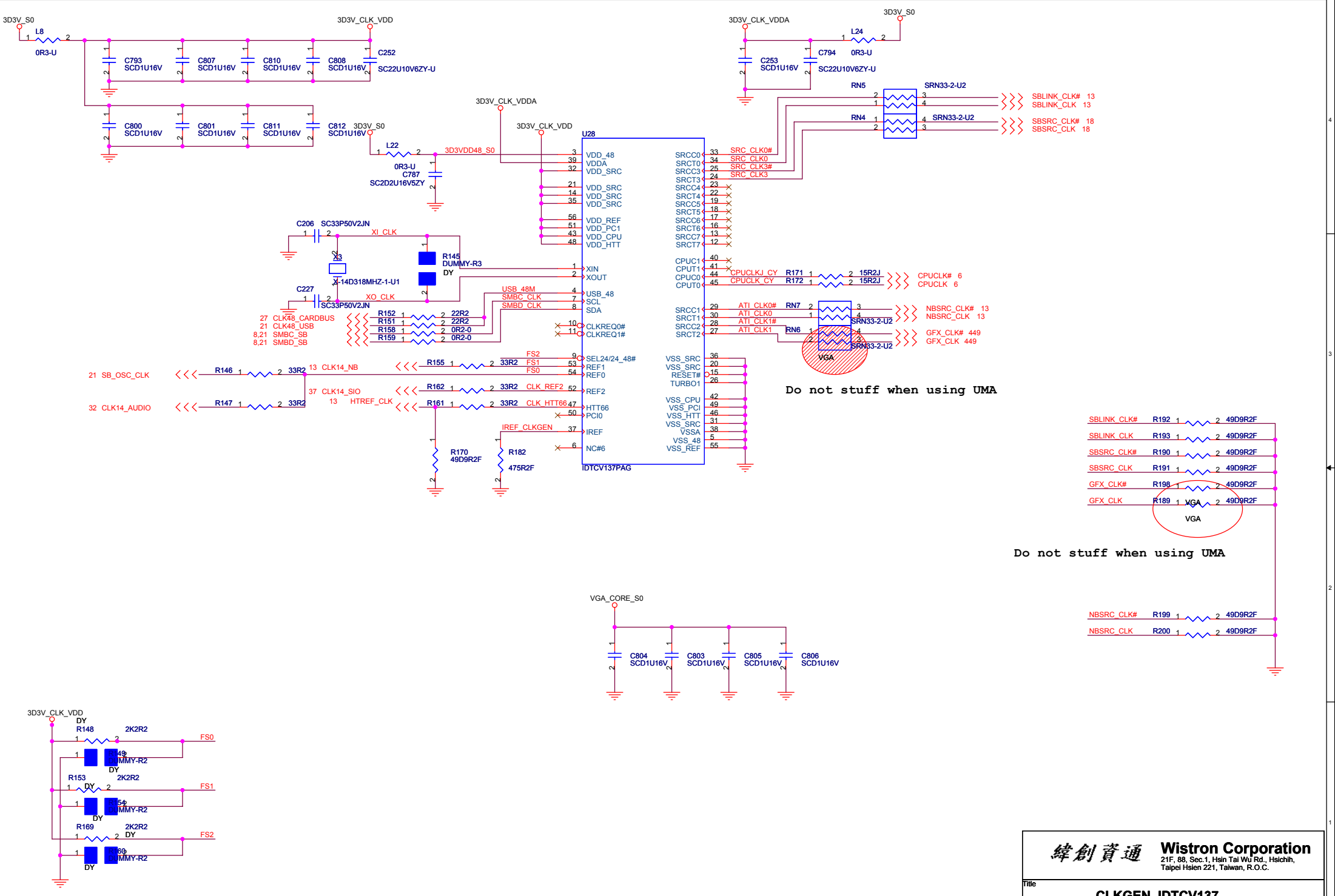
SA to SB need to check

1. connect G781 Thermal Alert pin to VGA\_GPIO14
2. ene KBC P165 LPCRST# , we suggest pull low avoid leakage
3. Clk to NB need to add Cap. when the trace change layer.
4. check page 9. what is the value of R481,R486, R498 and R499 is 100 ohm or 12 ohm.
5. check page 15, if on discrete mode does the 1D8V\_S0 power for lvds should dummy or still connect on power plan.
6. check page 19, can the 0 ohm resistance be dummied on P.19 right hand side?
7. check page 20, R203's voltage on pin 2.
8. page 21. check when the unused USB pin should be pull down or floating.
9. Can R471 change to common value?
10. check giga lan and 10/100 connect. Does them the same or can chose a cheaper one?
11. page 38. 12VGATE\_S0 can decreased resistance.
12. Does the 1D5V\_VGA\_S0 can come from TPS5130?

Schematic change:

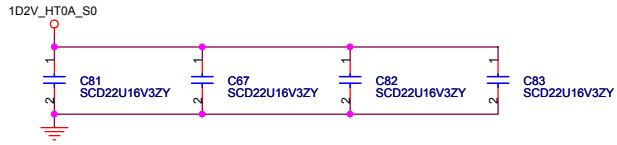
R659, change from 0R2 to 10Kr2

<b>緯創資通</b>		<b>Wistron Corporation</b>
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>
Title: CHANGE HISTORY		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004		
Sheet: 2		of: 56



hexainf@hotmail.com  
 GRATIS - FOR FREE

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CLKGEN_IDTCV137</b>	
Title Size A3 Date: Thursday, November 18, 2004	Document Number <b>SNIFE</b> Sheet 3 of 56
Rev SA	



HTT for CPU sideA  
 Transmit power  
 and NB sideA Receive  
 power

HTT for CPU sideB  
 Receive power  
 and NB sideA  
 Transmit power



62.10030.041

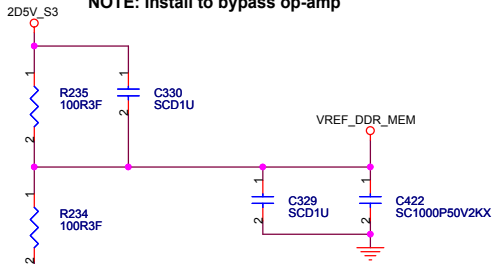
By ME request U11 P/N:  
 Main 62.10030.041  
 Second 62.10053.191  
 Third 62.10053.201

BGA754-SKT-U

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>CPU(1/4) HyperTransport I/F</b>		
Size	Document Number	Rev
A3	SNIPe	SA
Date: Thursday, November 18, 2004		
Sheet 4 of 56		

# VREF\_DDR\_MEM

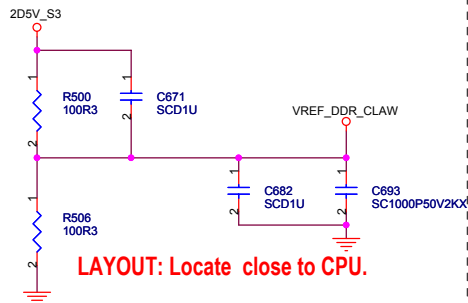
NOTE: Test with passive probes only.  
NOTE: Install to bypass op-amp



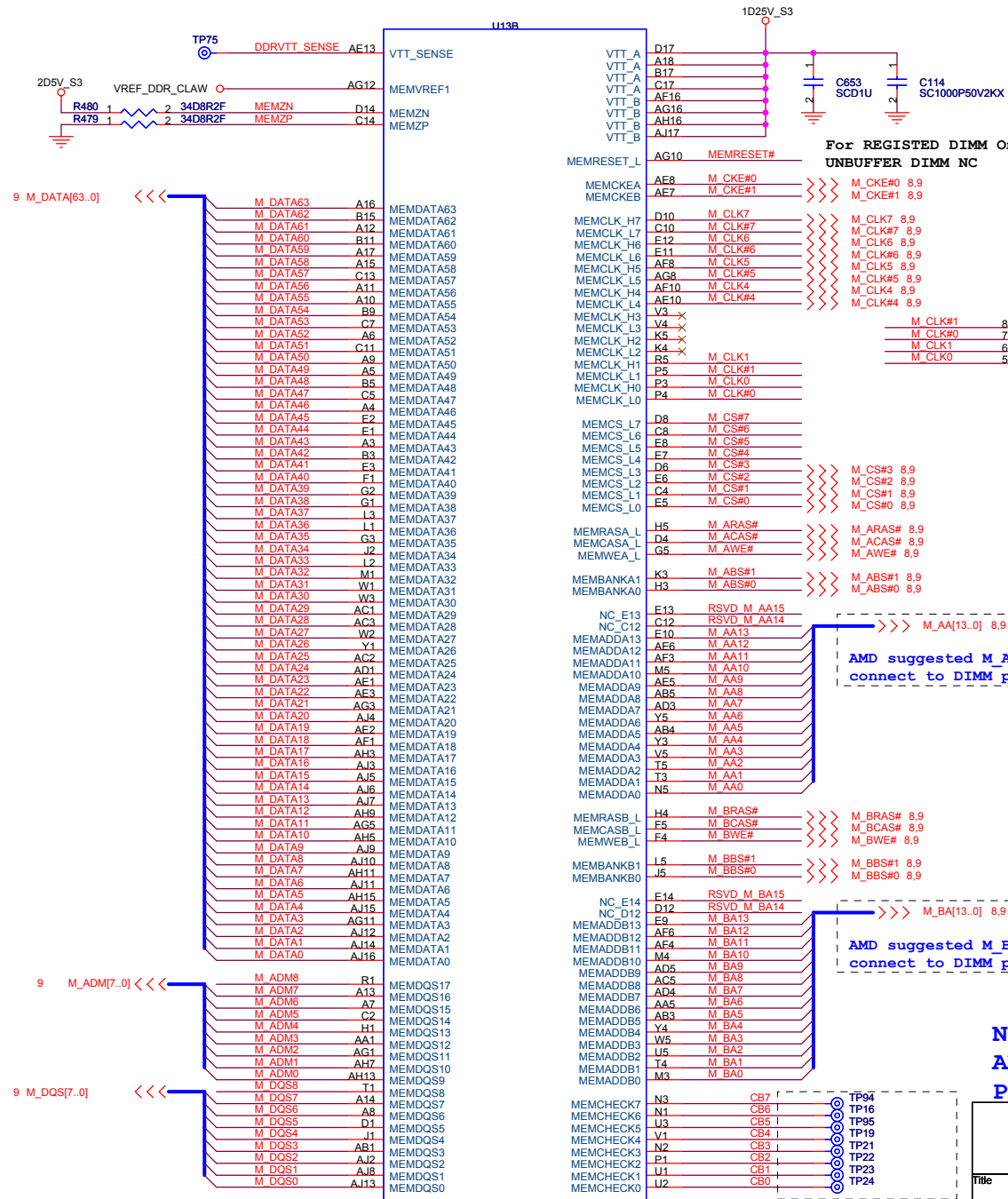
LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

# VREF\_DDR\_CLAW



LAYOUT: Locate close to CPU.



For REGISTERED DIMM Only  
UNBUFFER DIMM NC

AMD suggested M\_AA13  
connect to DIMM pin123

AMD suggested M\_BA13  
connect to DIMM pin123

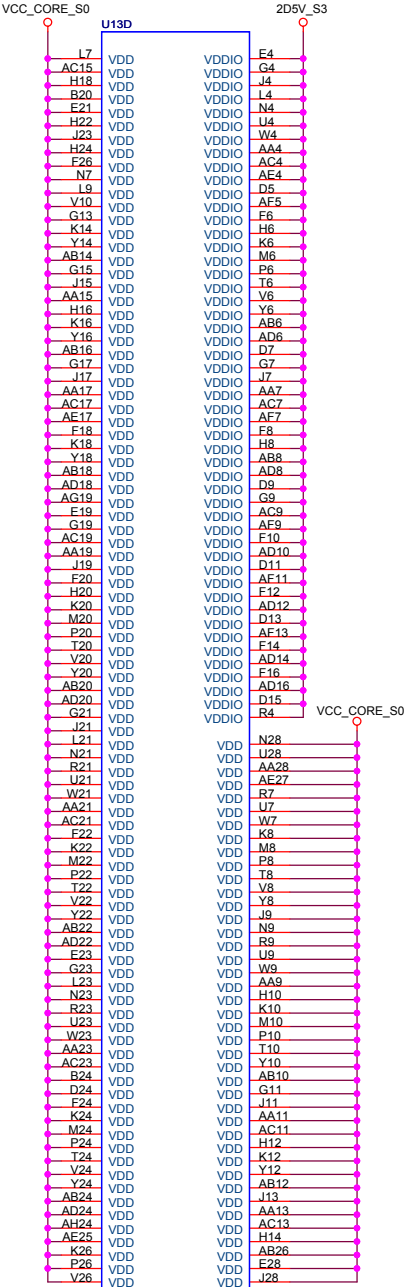
NOT SUPPORT ECC CHECK  
AMD suggested remove  
PULL-HI resistor.

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

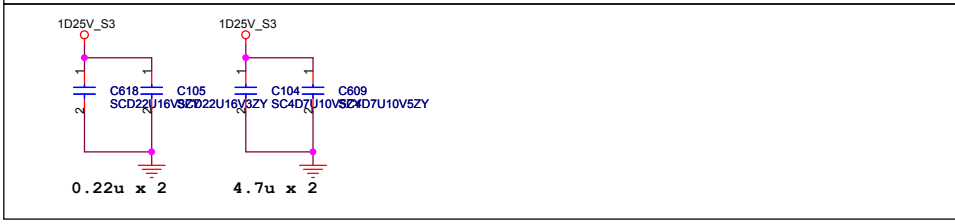
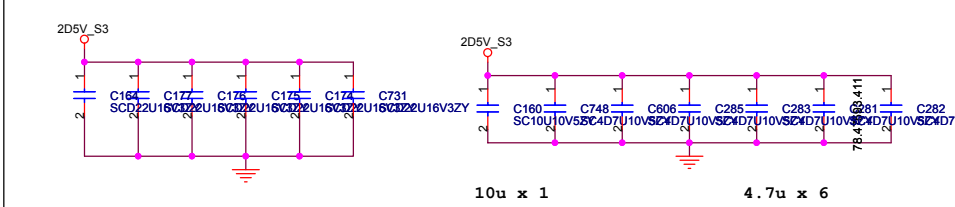
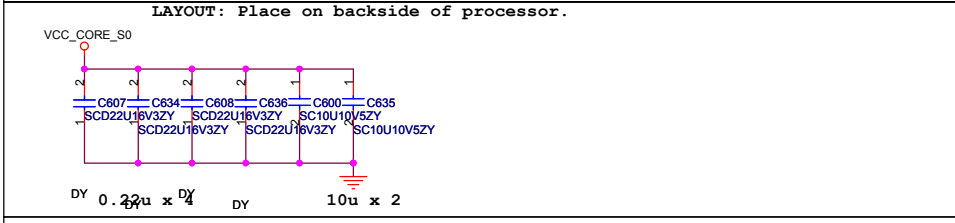
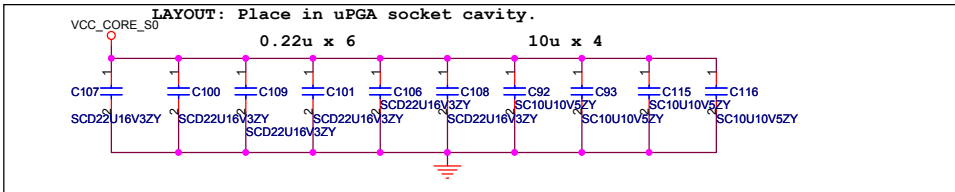
Title		
CPU(2/4)_DDR		
Size	Document Number	Rev
A3	SNIFE	SA
Date:	Thursday, November 18, 2004	Sheet 5 of 56



U13E	VSS	N20	VDD	E4
Y17	VSS	L20	VDDIO	G4
K17	VSS	L20	VDDIO	J4
H17	VSS	AF19	VDDIO	L4
F17	VSS	AD19	VDDIO	N4
E18	VSS	AB19	VDDIO	U4
AJ26	VSS	Y19	VDDIO	W4
AE29	VSS	K19	VDDIO	AA4
AC16	VSS	H22	VDDIO	AC4
AA18	VSS	F19	VDDIO	AE4
J18	VSS	D19	VDDIO	D5
G16	VSS	AC18	VDDIO	AF5
F16	VSS	AA18	VDDIO	H6
AH14	VSS	L9	VDDIO	K6
AD15	VSS	G18	VDDIO	M6
AB15	VSS	R16	VDDIO	P6
K15	VSS	G13	VDDIO	T6
E15	VSS	AB17	VDDIO	V6
D16	VSS	H15	VDDIO	Y8
AE14	VSS	F15	VDDIO	AB6
AC14	VSS	G28	VDDIO	AD6
AA14	VSS	J15	VDDIO	D7
G14	VSS	D28	VDDIO	G7
AF17	VSS	AB15	VDDIO	J7
AD13	VSS	C27	VDDIO	AA7
AB13	VSS	G15	VDDIO	AC7
V13	VSS	J15	VDDIO	H8
H13	VSS	D28	VDDIO	AB8
F13	VSS	B28	VDDIO	AD8
AH12	VSS	C27	VDDIO	D9
AC12	VSS	H18	VDDIO	G9
AA12	VSS	C25	VDDIO	AC9
G12	VSS	R25	VDDIO	AF9
C12	VSS	AJ24	VDDIO	F10
AD11	VSS	AG24	VDDIO	D11
AB11	VSS	AD18	VDDIO	AE11
Y11	VSS	AG19	VDDIO	F12
K11	VSS	E19	VDDIO	AD12
H11	VSS	G19	VDDIO	D13
AH10	VSS	U24	VDDIO	AE13
AC10	VSS	AA19	VDDIO	F14
W10	VSS	H19	VDDIO	AD14
U10	VSS	J24	VDDIO	F16
R10	VSS	H20	VDDIO	AD16
N10	VSS	K20	VDDIO	D15
L10	VSS	M20	VDDIO	R4
J10	VSS	P20	VDDIO	VDD
G10	VSS	T20	VDDIO	VDD
B10	VSS	Y23	VDDIO	VDD
AD9	VSS	Y20	VDDIO	VDD
Y9	VSS	AB20	VDDIO	VDD
V9	VSS	P23	VDDIO	VDD
T9	VSS	K23	VDDIO	VDD
P9	VSS	H23	VDDIO	VDD
M9	VSS	F23	VDDIO	VDD
K9	VSS	D23	VDDIO	VDD
H9	VSS	AJ22	VDDIO	VDD
F9	VSS	U21	VDDIO	VDD
AH8	VSS	AG22	VDDIO	VDD
AC8	VSS	AA21	VDDIO	VDD
W8	VSS	AC21	VDDIO	VDD
U8	VSS	AG28	VDDIO	VDD
R8	VSS	K22	VDDIO	VDD
N8	VSS	M22	VDDIO	VDD
L8	VSS	P22	VDDIO	VDD
J8	VSS	T22	VDDIO	VDD
G8	VSS	Y22	VDDIO	VDD
B8	VSS	Y22	VDDIO	VDD
AD7	VSS	E22	VDDIO	VDD
AB7	VSS	AD22	VDDIO	VDD
V7	VSS	E23	VDDIO	VDD
T7	VSS	G23	VDDIO	VDD
P7	VSS	L23	VDDIO	VDD
M7	VSS	V21	VDDIO	VDD
K7	VSS	N23	VDDIO	VDD
H7	VSS	R23	VDDIO	VDD
F7	VSS	U23	VDDIO	VDD
AH6	VSS	W23	VDDIO	VDD
AC6	VSS	K21	VDDIO	VDD
AA6	VSS	AA23	VDDIO	VDD
U6	VSS	H21	VDDIO	VDD
R6	VSS	F21	VDDIO	VDD
N6	VSS	D24	VDDIO	VDD
L6	VSS	AJ20	VDDIO	VDD
J6	VSS	AG20	VDDIO	VDD
G6	VSS	M24	VDDIO	VDD
B6	VSS	P24	VDDIO	VDD
AH4	VSS	T24	VDDIO	VDD
B4	VSS	V24	VDDIO	VDD
AH2	VSS	W24	VDDIO	VDD
AD2	VSS	AB24	VDDIO	VDD
AB2	VSS	AD24	VDDIO	VDD
Y2	VSS	G20	VDDIO	VDD
V2	VSS	J18	VDDIO	VDD
T2	VSS	AE16	VDDIO	VDD
P2	VSS	Y15	VDDIO	VDD
M2	VSS	B14	VDDIO	VDD
K2	VSS	J12	VDDIO	VDD
H2	VSS	AA10	VDDIO	VDD
F2	VSS	AB9	VDDIO	VDD
C29	VSS	AA8	VDDIO	VDD
AH28	VSS	Y7	VDDIO	VDD
AF28	VSS	W6	VDDIO	VDD
AC28	VSS	AE2	VDDIO	VDD
WC28	VSS	D2	VDDIO	VDD
R28	VSS	AG27	VDDIO	VDD
L28	VSS	AG25	VDDIO	VDD
		L24	VDDIO	VDD
		M23	VDDIO	VDD
		W22	VDDIO	VDD
		AB21	VDDIO	VDD
		AH20	VDDIO	VDD
		B2	VDDIO	VDD



BGA754-SKT-U



M_AA0	112	A0
M_AA1	111	A1
M_AA2	110	A2
M_AA3	109	A3
M_AA4	108	A4
M_AA6	107	A5
M_AA5	106	A6
M_AA7	105	A7
M_AA8	102	A7
M_AA9	101	A8
M_AA10	115	A9
M_AA11	100	A10 / AP
M_AA12	99	A11
M_ABS#0	117	A12
M_ABS#1	116	BA0
M_ABS#1	116	BA1
M_DATA R 0	5	DM0
M_DATA R 1	7	DM1
M_DATA R 2	13	DM2
M_DATA R 3	17	DM3
M_DATA R 4	6	DM4
M_DATA R 5	8	DM5
M_DATA R 6	14	DM6
M_DATA R 7	18	DM7
M_DATA R 8	19	DM8
M_DATA R 9	23	DM9
M_DATA R 10	29	DM10
M_DATA R 11	31	DM11
M_DATA R 12	20	DM12
M_DATA R 13	24	DM13
M_DATA R 14	30	DM14
M_DATA R 15	32	DM15
M_DATA R 16	41	DM16
M_DATA R 17	43	DM17
M_DATA R 18	49	DM18
M_DATA R 19	53	DM19
M_DATA R 20	42	DM20
M_DATA R 21	44	DM21
M_DATA R 22	50	DM22
M_DATA R 23	54	DM23
M_DATA R 24	55	DM24
M_DATA R 25	59	DM25
M_DATA R 26	65	DM26
M_DATA R 27	67	DM27
M_DATA R 28	56	DM28
M_DATA R 29	60	DM29
M_DATA R 30	66	DM30
M_DATA R 31	68	DM31
M_DATA R 32	127	DM32
M_DATA R 33	129	DM33
M_DATA R 34	135	DM34
M_DATA R 35	139	DM35
M_DATA R 36	128	DM36
M_DATA R 37	130	DM37
M_DATA R 38	136	DM38
M_DATA R 39	140	DM39
M_DATA R 40	141	DM40
M_DATA R 41	145	DM41
M_DATA R 42	151	DM42
M_DATA R 43	153	DM43
M_DATA R 44	142	DM44
M_DATA R 45	146	DM45
M_DATA R 46	152	DM46
M_DATA R 47	154	DM47
M_DATA R 48	165	DM48
M_DATA R 49	163	DM49
M_DATA R 50	171	DM50
M_DATA R 51	175	DM51
M_DATA R 52	164	DM52
M_DATA R 53	166	DM53
M_DATA R 54	172	DM54
M_DATA R 55	176	DM55
M_DATA R 56	177	DM56
M_DATA R 57	181	DM57
M_DATA R 58	187	DM58
M_DATA R 59	189	DM59
M_DATA R 60	178	DM60
M_DATA R 61	182	DM61
M_DATA R 62	188	DM62
M_DATA R 63	190	DM63

NORMAL TYPE

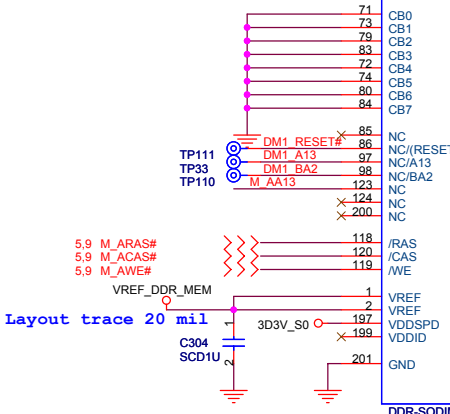
/CS0	121	A0
/CS1	122	A1
CKE0	96	A2
CKE1	95	A3
M_DQS R0	11	A4
M_DQS R1	25	A5
M_DQS R2	47	A6
M_DQS R3	61	A7
M_DQS R4	133	A8
M_DQS R5	147	A9
M_DQS R6	169	A10 / AP
M_DQS R7	183	A11
M_DQS R7	183	A12
M_BBS#0	117	BA0
M_BBS#1	116	BA1
M_DATA R 0	5	DM0
M_DATA R 1	7	DM1
M_DATA R 2	13	DM2
M_DATA R 3	17	DM3
M_DATA R 4	6	DM4
M_DATA R 5	8	DM5
M_DATA R 6	14	DM6
M_DATA R 7	18	DM7
M_DATA R 8	19	DM8
M_DATA R 9	23	DM9
M_DATA R 10	29	DM10
M_DATA R 11	31	DM11
M_DATA R 12	20	DM12
M_DATA R 13	24	DM13
M_DATA R 14	30	DM14
M_DATA R 15	32	DM15
M_DATA R 16	41	DM16
M_DATA R 17	43	DM17
M_DATA R 18	49	DM18
M_DATA R 19	53	DM19
M_DATA R 20	42	DM20
M_DATA R 21	44	DM21
M_DATA R 22	50	DM22
M_DATA R 23	54	DM23
M_DATA R 24	55	DM24
M_DATA R 25	59	DM25
M_DATA R 26	65	DM26
M_DATA R 27	67	DM27
M_DATA R 28	56	DM28
M_DATA R 29	60	DM29
M_DATA R 30	66	DM30
M_DATA R 31	68	DM31
M_DATA R 32	127	DM32
M_DATA R 33	129	DM33
M_DATA R 34	135	DM34
M_DATA R 35	139	DM35
M_DATA R 36	128	DM36
M_DATA R 37	130	DM37
M_DATA R 38	136	DM38
M_DATA R 39	140	DM39
M_DATA R 40	141	DM40
M_DATA R 41	145	DM41
M_DATA R 42	151	DM42
M_DATA R 43	153	DM43
M_DATA R 44	142	DM44
M_DATA R 45	146	DM45
M_DATA R 46	152	DM46
M_DATA R 47	154	DM47
M_DATA R 48	165	DM48
M_DATA R 49	163	DM49
M_DATA R 50	171	DM50
M_DATA R 51	175	DM51
M_DATA R 52	164	DM52
M_DATA R 53	166	DM53
M_DATA R 54	172	DM54
M_DATA R 55	176	DM55
M_DATA R 56	177	DM56
M_DATA R 57	181	DM57
M_DATA R 58	187	DM58
M_DATA R 59	189	DM59
M_DATA R 60	178	DM60
M_DATA R 61	182	DM61
M_DATA R 62	188	DM62
M_DATA R 63	190	DM63

M\_ADM#0  
M\_ADM#1  
M\_ADM#2  
M\_ADM#3  
M\_ADM#4  
M\_ADM#5  
M\_ADM#6  
M\_ADM#7

M\_CLK5 5.9  
M\_CLK#5 5.9  
M\_CLK7 5.9  
M\_CLK#7 5.9

SMBC\_SB 3.21  
SMDB\_SB 3.21

NOT SUPPORT ECC CHECK  
AMD suggested pull-low



DDR-SODIMM-N-U1

M_BA0	112	A0
M_BA1	111	A1
M_BA2	110	A2
M_BA3	109	A3
M_BA4	108	A4
M_BA6	107	A5
M_BA5	106	A6
M_BA7	105	A7
M_BA8	102	A7
M_BA9	101	A8
M_BA10	115	A9
M_BA11	100	A10 / AP
M_BA12	99	A11
M_BA12	99	A12
M_BBS#0	117	BA0
M_BBS#1	116	BA1
M_DATA R 0	5	DM0
M_DATA R 1	7	DM1
M_DATA R 2	13	DM2
M_DATA R 3	17	DM3
M_DATA R 4	6	DM4
M_DATA R 5	8	DM5
M_DATA R 6	14	DM6
M_DATA R 7	18	DM7
M_DATA R 8	19	DM8
M_DATA R 9	23	DM9
M_DATA R 10	29	DM10
M_DATA R 11	31	DM11
M_DATA R 12	20	DM12
M_DATA R 13	24	DM13
M_DATA R 14	30	DM14
M_DATA R 15	32	DM15
M_DATA R 16	41	DM16
M_DATA R 17	43	DM17
M_DATA R 18	49	DM18
M_DATA R 19	53	DM19
M_DATA R 20	42	DM20
M_DATA R 21	44	DM21
M_DATA R 22	50	DM22
M_DATA R 23	54	DM23
M_DATA R 24	55	DM24
M_DATA R 25	59	DM25
M_DATA R 26	65	DM26
M_DATA R 27	67	DM27
M_DATA R 28	56	DM28
M_DATA R 29	60	DM29
M_DATA R 30	66	DM30
M_DATA R 31	68	DM31
M_DATA R 32	127	DM32
M_DATA R 33	129	DM33
M_DATA R 34	135	DM34
M_DATA R 35	139	DM35
M_DATA R 36	128	DM36
M_DATA R 37	130	DM37
M_DATA R 38	136	DM38
M_DATA R 39	140	DM39
M_DATA R 40	141	DM40
M_DATA R 41	145	DM41
M_DATA R 42	151	DM42
M_DATA R 43	153	DM43
M_DATA R 44	142	DM44
M_DATA R 45	146	DM45
M_DATA R 46	152	DM46
M_DATA R 47	154	DM47
M_DATA R 48	165	DM48
M_DATA R 49	163	DM49
M_DATA R 50	171	DM50
M_DATA R 51	175	DM51
M_DATA R 52	164	DM52
M_DATA R 53	166	DM53
M_DATA R 54	172	DM54
M_DATA R 55	176	DM55
M_DATA R 56	177	DM56
M_DATA R 57	181	DM57
M_DATA R 58	187	DM58
M_DATA R 59	189	DM59
M_DATA R 60	178	DM60
M_DATA R 61	182	DM61
M_DATA R 62	188	DM62
M_DATA R 63	190	DM63

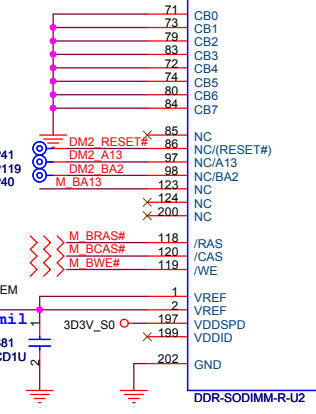
REVERSE TYPE

M\_ADM#0  
M\_ADM#1  
M\_ADM#2  
M\_ADM#3  
M\_ADM#4  
M\_ADM#5  
M\_ADM#6  
M\_ADM#7

M\_CLK4 5.9  
M\_CLK#4 5.9  
M\_CLK6 5.9  
M\_CLK#6 5.9

SMBC\_SB 3.21  
SMDB\_SB 3.21

NOT SUPPORT ECC CHECK  
AMD suggested pull-low



DDR-SODIMM-R-U2

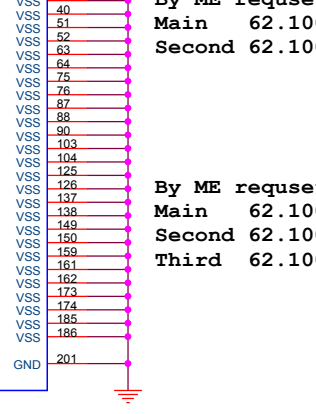
/CS0	121	A0
/CS1	122	A1
CKE0	96	A2
CKE1	95	A3
M_DQS R0	11	A4
M_DQS R1	25	A5
M_DQS R2	47	A6
M_DQS R3	61	A7
M_DQS R4	133	A8
M_DQS R5	147	A9
M_DQS R6	169	A10 / AP
M_DQS R7	183	A11
M_DQS R7	183	A12
M_BBS#0	117	BA0
M_BBS#1	116	BA1
M_DATA R 0	5	DM0
M_DATA R 1	7	DM1
M_DATA R 2	13	DM2
M_DATA R 3	17	DM3
M_DATA R 4	6	DM4
M_DATA R 5	8	DM5
M_DATA R 6	14	DM6
M_DATA R 7	18	DM7
M_DATA R 8	19	DM8
M_DATA R 9	23	DM9
M_DATA R 10	29	DM10
M_DATA R 11	31	DM11
M_DATA R 12	20	DM12
M_DATA R 13	24	DM13
M_DATA R 14	30	DM14
M_DATA R 15	32	DM15
M_DATA R 16	41	DM16
M_DATA R 17	43	DM17
M_DATA R 18	49	DM18
M_DATA R 19	53	DM19
M_DATA R 20	42	DM20
M_DATA R 21	44	DM21
M_DATA R 22	50	DM22
M_DATA R 23	54	DM23
M_DATA R 24	55	DM24
M_DATA R 25	59	DM25
M_DATA R 26	65	DM26
M_DATA R 27	67	DM27
M_DATA R 28	56	DM28
M_DATA R 29	60	DM29
M_DATA R 30	66	DM30
M_DATA R 31	68	DM31
M_DATA R 32	127	DM32
M_DATA R 33	129	DM33
M_DATA R 34	135	DM34
M_DATA R 35	139	DM35
M_DATA R 36	128	DM36
M_DATA R 37	130	DM37
M_DATA R 38	136	DM38
M_DATA R 39	140	DM39
M_DATA R 40	141	DM40
M_DATA R 41	145	DM41
M_DATA R 42	151	DM42
M_DATA R 43	153	DM43
M_DATA R 44	142	DM44
M_DATA R 45	146	DM45
M_DATA R 46	152	DM46
M_DATA R 47	154	DM47
M_DATA R 48	165	DM48
M_DATA R 49	163	DM49
M_DATA R 50	171	DM50
M_DATA R 51	175	DM51
M_DATA R 52	164	DM52
M_DATA R 53	166	DM53
M_DATA R 54	172	DM54
M_DATA R 55	176	DM55
M_DATA R 56	177	DM56
M_DATA R 57	181	DM57
M_DATA R 58	187	DM58
M_DATA R 59	189	DM59
M_DATA R 60	178	DM60
M_DATA R 61	182	DM61
M_DATA R 62	188	DM62
M_DATA R 63	190	DM63

M\_ADM#0  
M\_ADM#1  
M\_ADM#2  
M\_ADM#3  
M\_ADM#4  
M\_ADM#5  
M\_ADM#6  
M\_ADM#7

M\_CLK4 5.9  
M\_CLK#4 5.9  
M\_CLK6 5.9  
M\_CLK#6 5.9

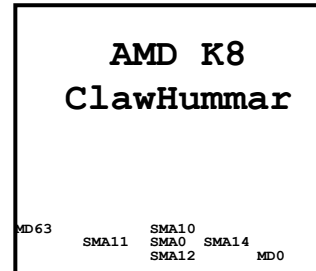
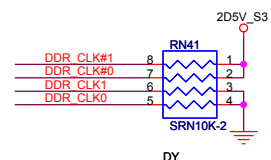
SMBC\_SB 3.21  
SMDB\_SB 3.21

NOT SUPPORT ECC CHECK  
AMD suggested pull-low

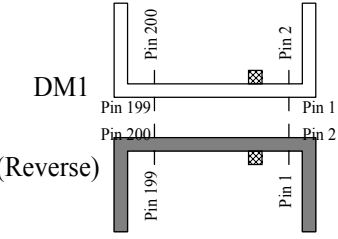


DDR-SODIMM-R-U2

- >>> M\_ADM\_R[7..0] 9
- >>> M\_DATA\_R[63..0] 9
- >>> M\_DQS\_R[7..0] 9
- >>> M\_AA[13..0] 5.9
- >>> M\_ABS#[1..0] 5.9
- >>> M\_BA[13..0] 5.9
- >>> M\_BBS#[1..0] 5.9



DDR SOCKET PLACEMENT  
TOP VIEW PERSPECTIVE DRAWING



By ME request DM1 P/N:  
Main 62.10017.191  
Second 62.10017.381

By ME request DM2 P/N:  
Main 62.10017.201  
Second 62.10017.371  
Third 62.10017.701

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR SO-DIMM SKT**

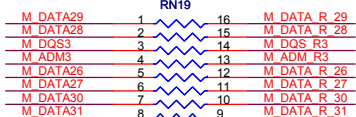
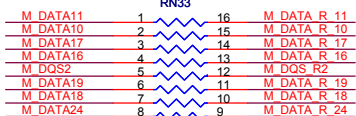
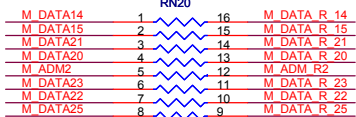
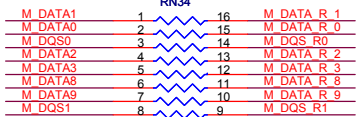
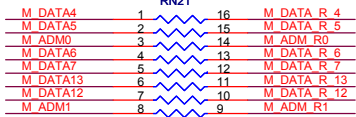
Size: A3 Document Number: **SNIFE** Rev: SA

Date: Thursday, November 18, 2004 Sheet: 8 of 56



# SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"  
STRICT EQUAL LENGTH LIMITATION WITH DQS,  
CB PINS

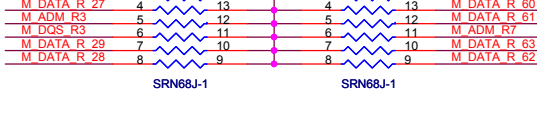
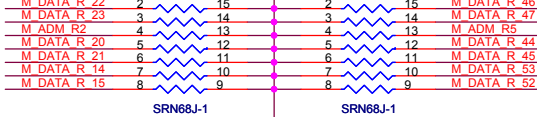
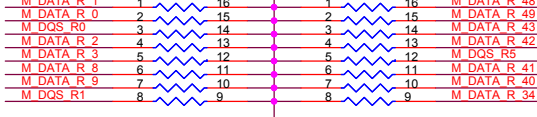
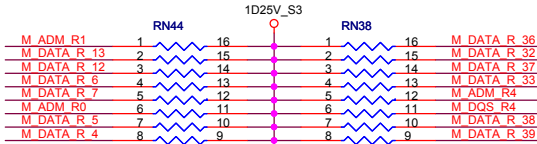


5.8 M\_CKE#0 <<< M\_CKE#0  
5.8 M\_CKE#1 <<< M\_CKE#1

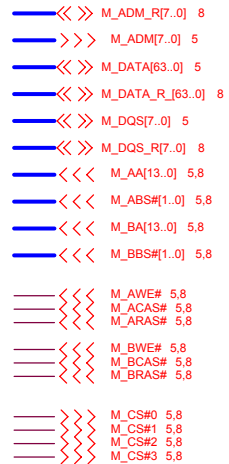
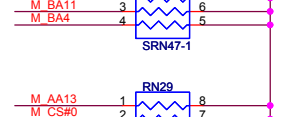
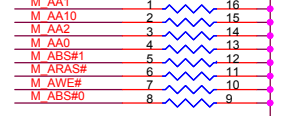
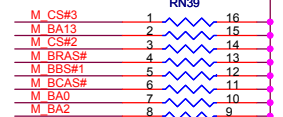
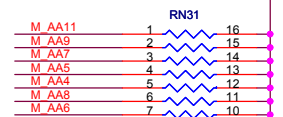
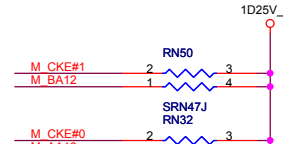
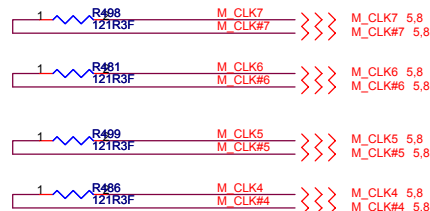
05/10  
Remove the damping resistor for AMD suggest.

# PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)  
NO EQUAL LENGTH LIMITATION



Place it near CPU



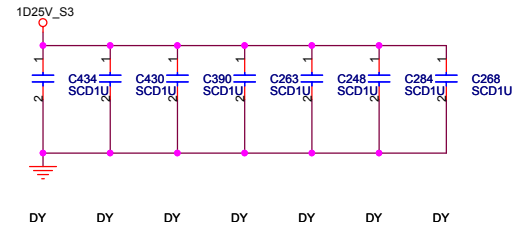
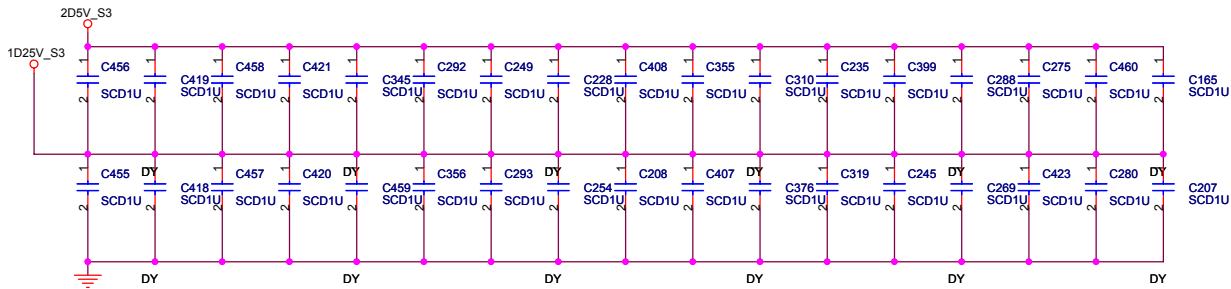
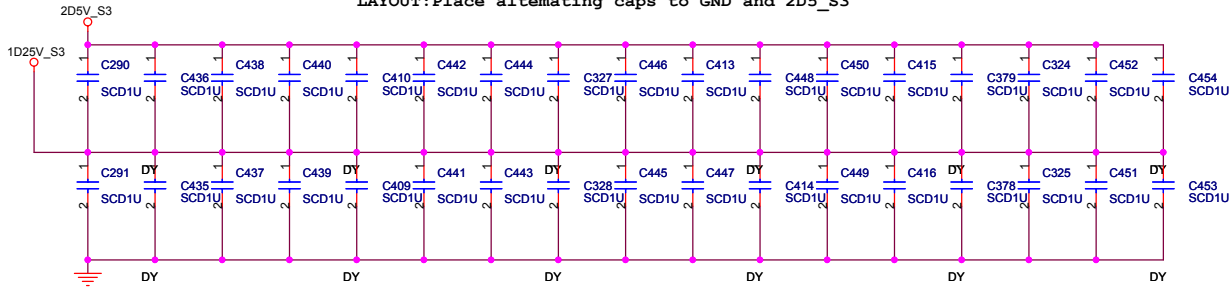
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

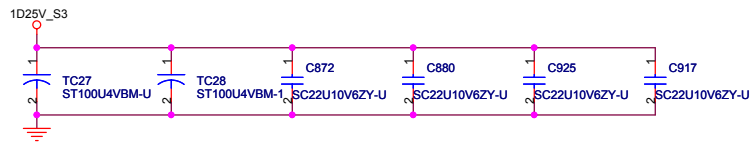
Size: A3 Document Number: **SNIP** Rev: SA

Date: Thursday, November 18, 2004 Sheet: 9 of 56

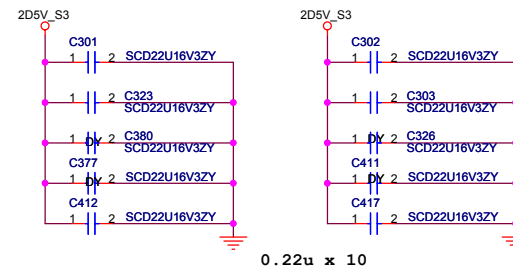
LAYOUT: Place alternating caps to GND and 2D5\_S3



LAYOUT: Place at end of the DIMMs



LAYOUT: Place close to Power Pin of DDR socket.



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Taipei Hsien 221, Taiwan, R.O.C.



449 PEG\_TXP[15..0] <<< ———  
 449 PEG\_TXN[15..0] <<< ———  
 449 PEG\_RXP[15..0] >>> ———  
 449 PEG\_RXN[15..0] >>> ———

**U20C PART 3 OF 6**

AE17	MEM_A0	MEM_D00	AE28
AK17	MEM_A1	MEM_D01	AG28
AH16	MEM_A2	MEM_D02	AE27
AF16	MEM_A3	MEM_D03	AE26
AJ22	MEM_A4	MEM_D04	AE25
AJ21	MEM_A5	MEM_D05	AE24
AH20	MEM_A6	MEM_D06	AG23
AK19	MEM_A7	MEM_D07	AE22
AH19	MEM_A8	MEM_D08	AE21
AJ17	MEM_A10	MEM_D010	AG30
AG16	MEM_A11	MEM_D011	AG29
AG17	MEM_A12	MEM_D012	AH28
AH17	MEM_A12	MEM_D012	AE22
AJ18	MEM_A13	MEM_D013	AH27
AJ18	MEM_A14	MEM_D014	AJ27
AG26	MEM_DM0	MEM_DM15	AE23
AJ29	MEM_DM1	MEM_DM17	AG22
AE21	MEM_DM2	MEM_DM18	AF23
AH24	MEM_DM3	MEM_DM19	AE20
AH12	MEM_DM4	MEM_DM20	AG19
AG13	MEM_DM5	MEM_DM21	AE20
AH8	MEM_DM6	MEM_DM22	AF22
AE8	MEM_DM7	MEM_DM23	AF19
AE25	MEM_D0S0P	MEM_D024	AH26
AH30	MEM_D0S1P	MEM_D025	AJ26
AG20	MEM_D0S1P	MEM_D026	AH25
AJ25	MEM_D0S2P	MEM_D027	AJ24
AH13	MEM_D0S3P	MEM_D028	AH23
AF14	MEM_D0S4P	MEM_D029	AH23
AJ7	MEM_D0S5P	MEM_D030	AJ23
AG8	MEM_D0S6P	MEM_D031	AH22
AG8	MEM_D0S7P	MEM_D032	AK14
AG25	MEM_D0S0N	MEM_D033	AK13
AH29	MEM_D0S1N	MEM_D034	AJ13
AE21	MEM_D0S1N	MEM_D035	AJ11
AK25	MEM_D0S2N	MEM_D036	AJ11
AJ12	MEM_D0S3N	MEM_D037	AH11
AE13	MEM_D0S4N	MEM_D038	AH10
AK7	MEM_D0S5N	MEM_D039	AE15
AE9	MEM_D0S6N	MEM_D040	AF15
AE9	MEM_D0S7N	MEM_D042	AG14
AE17	MEM_RAS#	MEM_D043	AE14
AH18	MEM_CAS#	MEM_D044	AE12
AH18	MEM_WE#	MEM_D045	AE12
AJ19	MEM_CS#	MEM_D045	AG11
AE18	MEM_CKE	MEM_D046	AE11
AK16	MEM_CKP	MEM_D047	AJ8
AJ16	MEM_CKN	MEM_D048	AH9
		MEM_D050	AJ8
		MEM_D051	AK8
		MEM_D052	AH7
		MEM_D053	AH6
		MEM_D054	AJ5
		MEM_D055	AJ5
		MEM_D056	AG10
		MEM_D057	AF11
		MEM_D058	AE9
		MEM_D059	AG7
		MEM_D080	AE8
		MEM_D081	AE7
		MEM_D062	AE7
		MEM_D063	AE7
		MEM_COMPN	

LANE REVERSE

MEM\_A I/F

**U20B PART 2 OF 6**

PEG_TXP15	D8	GFX_RX0P	GFX_TX0P	A7	PEG_RXP15_NB	1	2	C132	PEG_RXP15
PEG_TXN15	D7	GFX_RX0N	GFX_TX0N	B7	PEG_RXN15_NB	1	2	SCD1U16V	PEG_RXN15
PEG_TXP14	D5	GFX_RX1P	GFX_TX1P	B6	PEG_RXP14_NB	1	2	SCD1U16V	PEG_RXP14
PEG_TXN14	D4	GFX_RX1N	GFX_TX1N	B5	PEG_RXN14_NB	1	2	SCD1U16V	PEG_RXN14
PEG_TXP13	F4	GFX_RX2P	GFX_TX2P	A4	PEG_RXP13_NB	1	2	SCD1U16V	PEG_RXP13
PEG_TXN13	F4	GFX_RX2N	GFX_TX2N	F4	PEG_RXN13_NB	1	2	SCD1U16V	PEG_RXN13
PEG_TXP12	G5	GFX_RX3P	GFX_TX3P	B3	PEG_RXP12_NB	1	2	SCD1U16V	PEG_RXP12
PEG_TXN12	G4	GFX_RX3N	GFX_TX3N	B2	PEG_RXN12_NB	1	2	SCD1U16V	PEG_RXN12
PEG_TXP11	H4	GFX_RX4P	GFX_TX4P	C1	PEG_RXP11_NB	1	2	SCD1U16V	PEG_RXP11
PEG_TXN11	H4	GFX_RX4N	GFX_TX4N	D1	PEG_RXN11_NB	1	2	SCD1U16V	PEG_RXN11
PEG_TXP10	H5	GFX_RX5P	GFX_TX5P	D2	PEG_RXP10_NB	1	2	SCD1U16V	PEG_RXP10
PEG_TXN10	H6	GFX_RX5N	GFX_TX5N	E2	PEG_RXN10_NB	1	2	SCD1U16V	PEG_RXN10
PEG_TXP9	Q1	GFX_RX6P	GFX_TX6P	E2	PEG_RXP9_NB	1	2	SCD1U16V	PEG_RXP9
PEG_TXN9	Q2	GFX_RX6N	GFX_TX6N	F1	PEG_RXN9_NB	1	2	SCD1U16V	PEG_RXN9
PEG_TXP8	K5	GFX_RX8P	GFX_TX8P	H2	PEG_RXP8_NB	1	2	SCD1U16V	PEG_RXP8
PEG_TXN8	K4	GFX_RX7N	GFX_TX7N	J2	PEG_RXN8_NB	1	2	SCD1U16V	PEG_RXN8
PEG_TXP7	L4	GFX_RX8P	GFX_TX8P	J1	PEG_RXP7_NB	1	2	SCD1U16V	PEG_RXP7
PEG_TXN7	N5	GFX_RX8N	GFX_TX8N	K2	PEG_RXN7_NB	1	2	SCD1U16V	PEG_RXN7
PEG_TXP6	M4	GFX_RX9P	GFX_TX9P	K1	PEG_RXP6_NB	1	2	SCD1U16V	PEG_RXP6
PEG_TXN6	N4	GFX_RX9N	GFX_TX9N	L2	PEG_RXN6_NB	1	2	SCD1U16V	PEG_RXN6
PEG_TXP5	P4	GFX_RX10P	GFX_TX10P	L1	PEG_RXP5_NB	1	2	SCD1U16V	PEG_RXP5
PEG_TXN5	R4	GFX_RX10N	GFX_TX10N	M2	PEG_RXN5_NB	1	2	SCD1U16V	PEG_RXN5
PEG_TXP4	P5	GFX_RX11P	GFX_TX11P	N1	PEG_RXP4_NB	1	2	SCD1U16V	PEG_RXP4
PEG_TXN4	P2	GFX_RX11N	GFX_TX11N	N2	PEG_RXN4_NB	1	2	SCD1U16V	PEG_RXN4
PEG_TXP3	R2	GFX_RX12P	GFX_TX12P	R1	PEG_RXP3_NB	1	2	SCD1U16V	PEG_RXP3
PEG_TXN3	R2	GFX_RX12N	GFX_TX12N	T1	PEG_RXN3_NB	1	2	SCD1U16V	PEG_RXN3
PEG_TXP2	T5	GFX_RX13P	GFX_TX13P	U2	PEG_RXP2_NB	1	2	SCD1U16V	PEG_RXP2
PEG_TXN2	T4	GFX_RX13N	GFX_TX13N	V2	PEG_RXN2_NB	1	2	SCD1U16V	PEG_RXN2
PEG_TXP1	U4	GFX_RX14P	GFX_TX14P	U2	PEG_RXP1_NB	1	2	SCD1U16V	PEG_RXP1
PEG_TXN1	V4	GFX_RX14N	GFX_TX14N	V1	PEG_RXN1_NB	1	2	SCD1U16V	PEG_RXN1
PEG_TXP0	W1	GFX_RX15P	GFX_TX15P	Y2	PEG_RXP0_NB	1	2	SCD1U16V	PEG_RXP0
PEG_TXN0	W2	GFX_RX15N	GFX_TX15N	AA2	PEG_RXN0_NB	1	2	SCD1U16V	PEG_RXN0

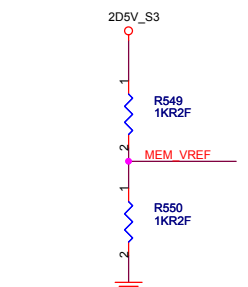
LANE REVERSE

PCIE I/F TO VIDEO

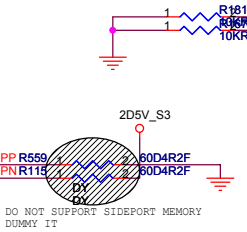
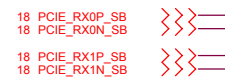
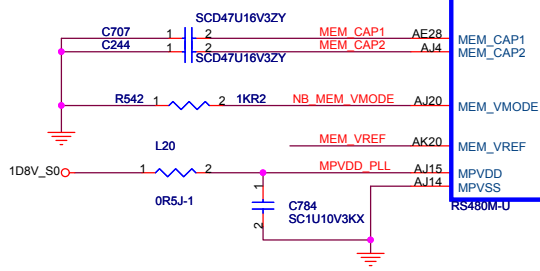
PCIE I/F TO SLOT

PCIE I/F TO SB

Do not stuff when using M26



Connect MEM\_VREF to VDD\_MEM/2 PA\_RS480F1.PDF



DO NOT SUPPORT SIDEPORT MEMORY DUMMY IT

DO NOT SUPPORT SIDEPORT MEMORY DUMMY IT

When disable local frame buffer,  
 VDD\_MEM connect to 2D5V\_S3, MEM\_VMODE  
 connect to GND, MEM\_VREF connect to  
 2D5V\_S3, MPVDD connected to 1D8V  
 DSG-215-RS480-04.PDF

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsin 221, Taiwan, R.O.C.

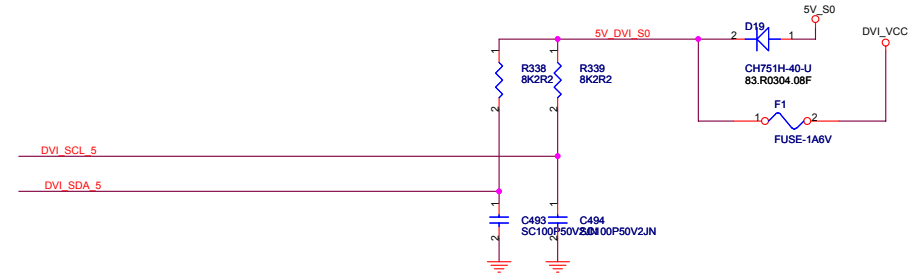
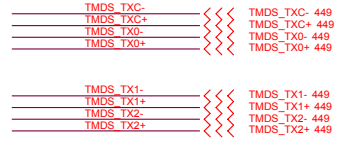
Title: **NB-RS480M\_MEM/PCIE\_LINK I/F**

Size: A3 Document Number: **SNIE** Rev: SA

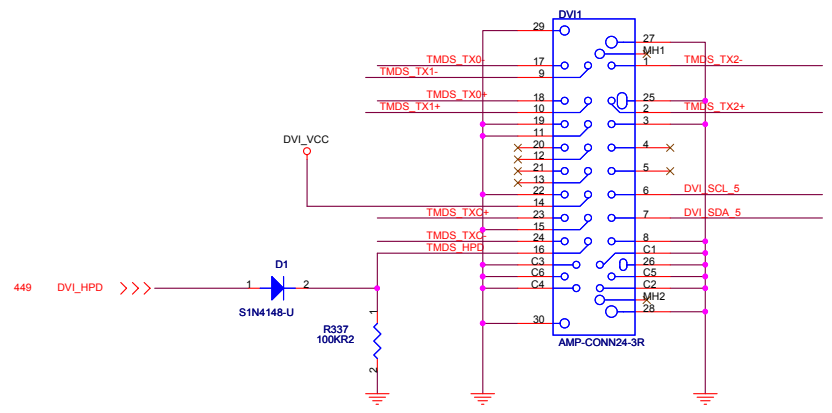
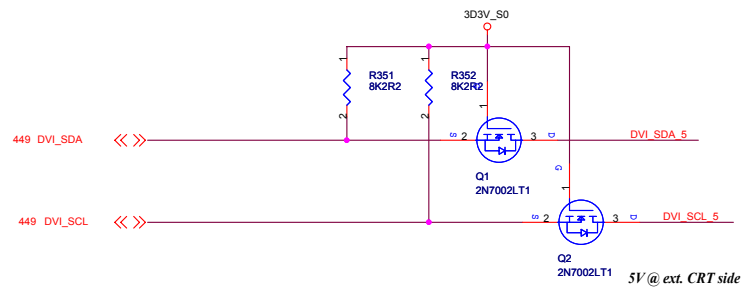
Date: Thursday, November 18, 2004 Sheet: 12 of 56





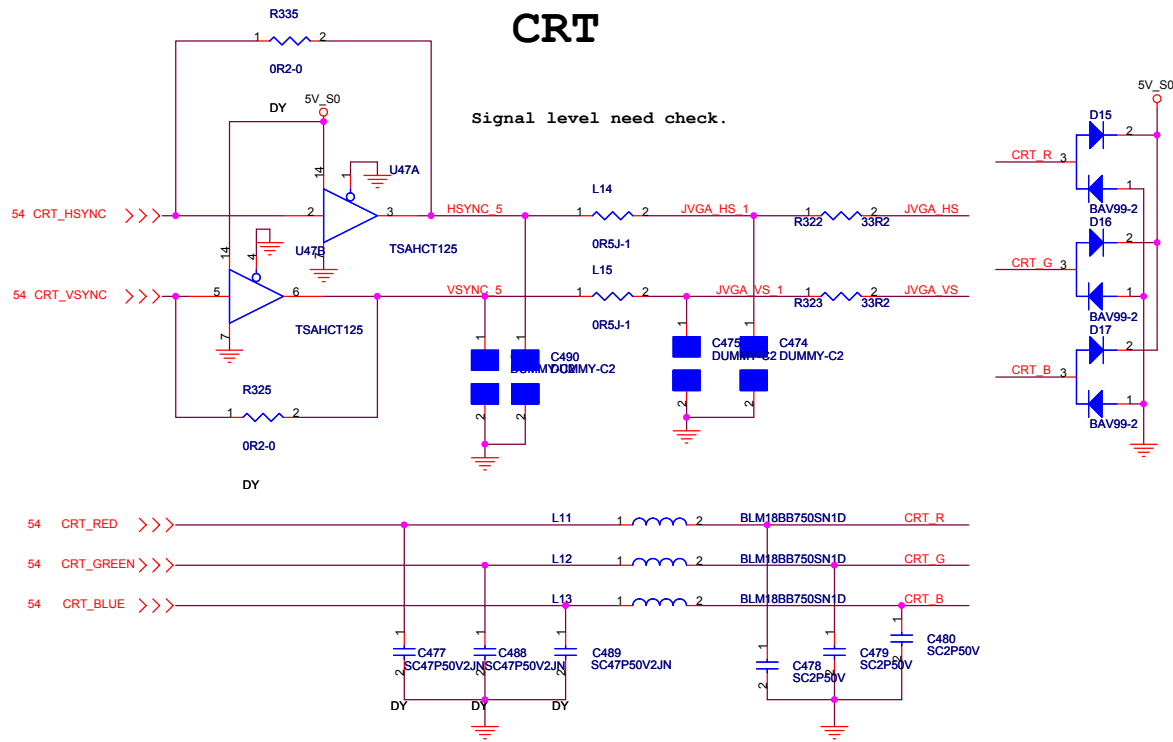


Do not stuff when using UMA



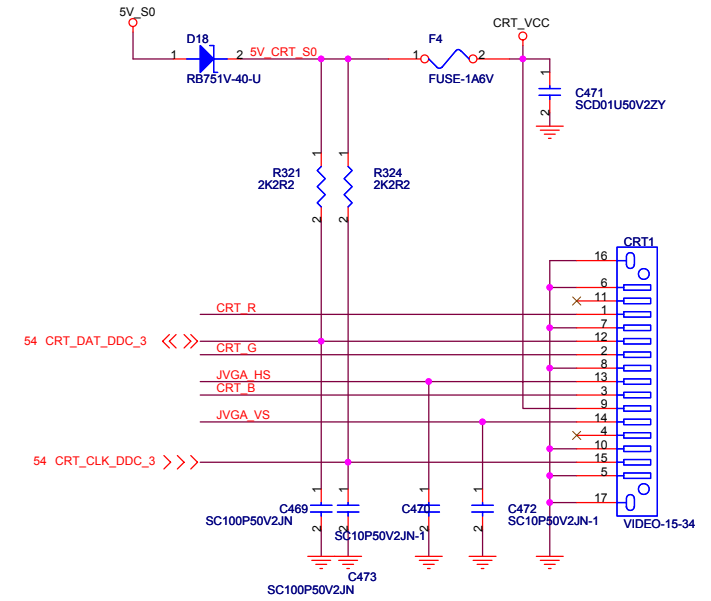
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
<b>DVI CONNECTOR</b>			
Size	Document Number	<b>SNIP</b>	
Custom		Rev <b>S4</b>	
Date: Thursday, November 18, 2004	Sheet 15	of 58	

# CRT



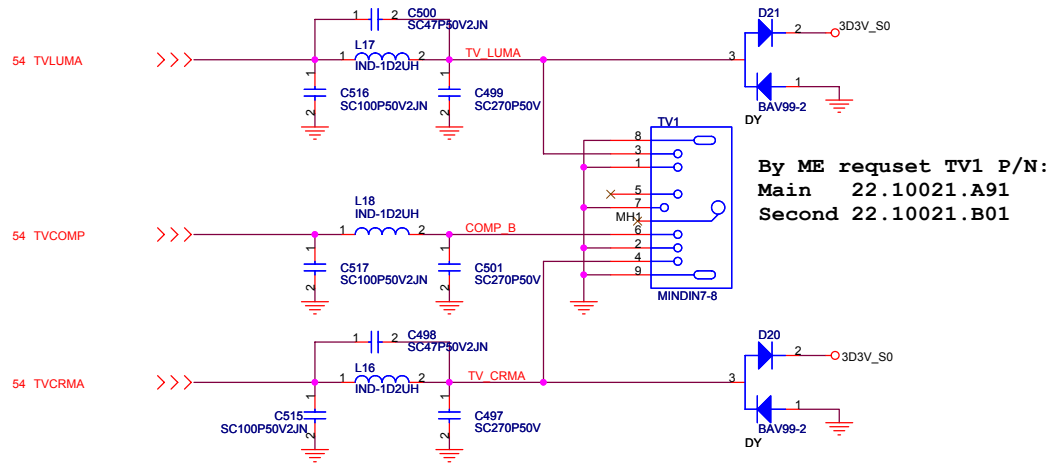
# CRT CONN

200mA Rating/Spec 500mA

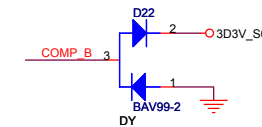


By ME request CRT1 P/N:  
Main 20.B0026.A15  
Second 20.B0034.015

# TV CONN



By ME request TV1 P/N:  
Main 22.10021.A91  
Second 22.10021.B01

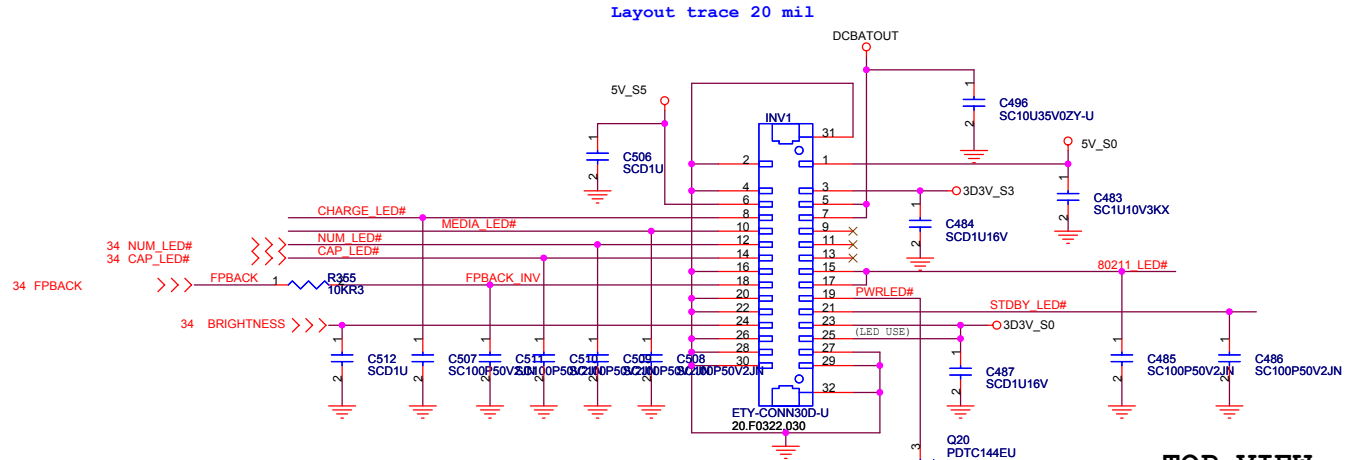
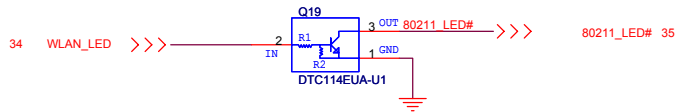
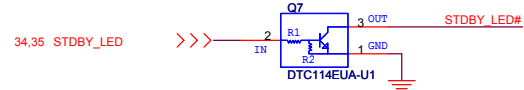
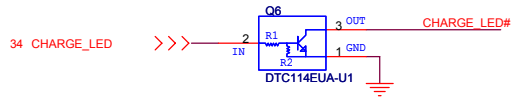


緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title <b>CRT / TV</b>		
Size A3	Document Number <b>SNIFE</b>	Rev SA
Date: Thursday, November 18, 2004	Sheet 16 of 56	



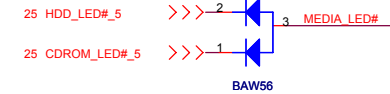
# INVERTER/LED



TOP VIEW

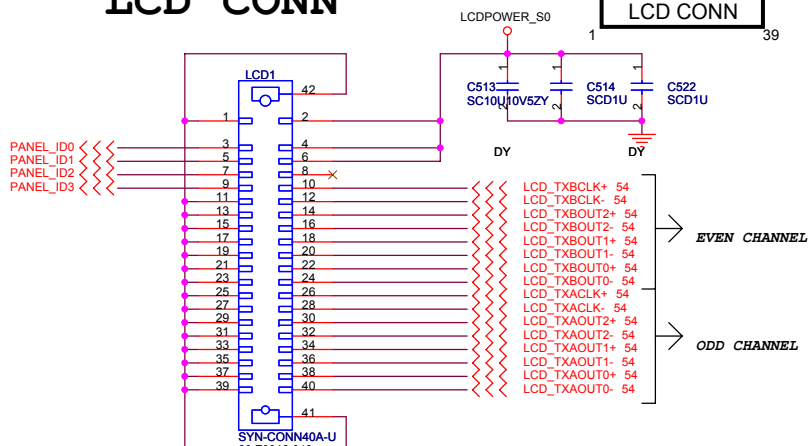


By ME request INV1 P/N:  
Main 20.F0322.030  
Second 20.D0144.215



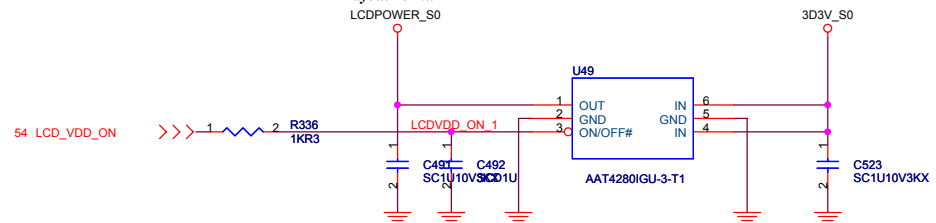
## LCD CONN

TOP VIEW



## LCD POWER

Layout 40 mil



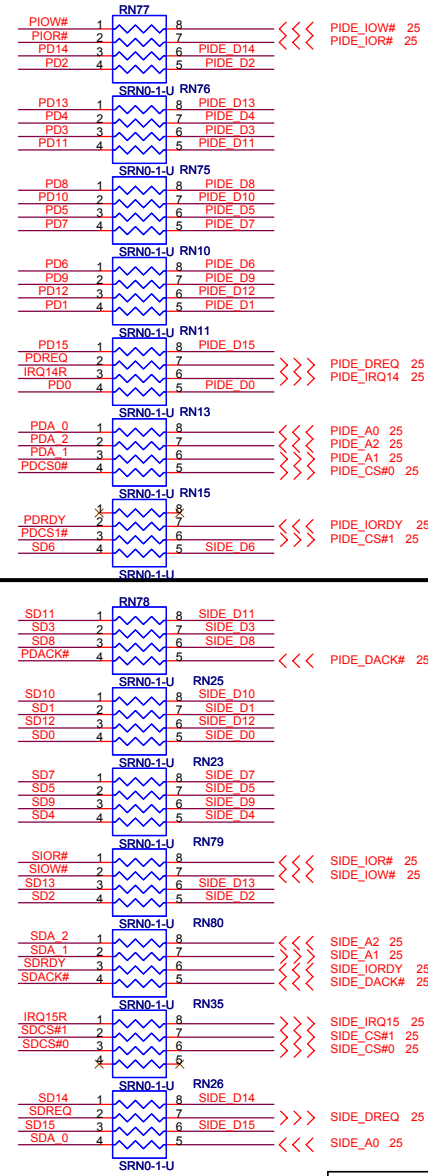
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
INV / LCD		
Size A3	Document Number	Rev SA
SNIPE		
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PIDE\_D[15..0] 25

SIDE\_D[15..0] 25



**SB400 SB**  
Part 2 of 4

SERIAL ATA

PRIMARY ATA 66/100

SECONDARY ATA 66/100

SERIAL ATA POWER

U84B

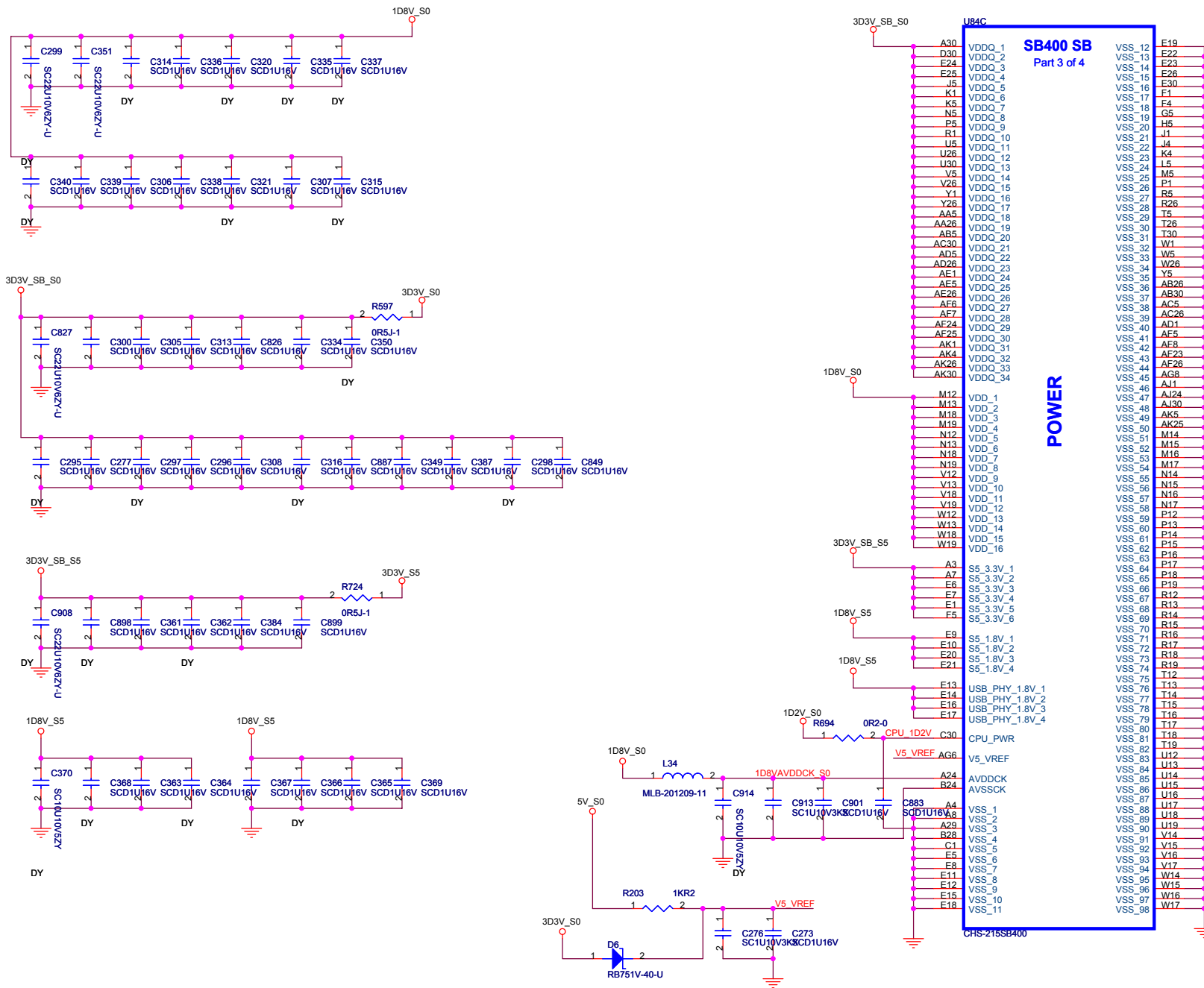
AK22	SATA_TX0+	AD30	PDRDY	V29	SDRDY	V28	SD0	AG13
AJ22	SATA_TX0-	AE28	IRQ14R	T27	IRO15R	W28	SD1	AH22
AK21	SATA_RX0-	AD27	PDA_0	T28	SDA_0	Y30	SD2	AK12
AJ21	SATA_RX0+	AC27	PDA_1	U29	SDA_1	Y30	SD3	AK11
AK19	SATA_TX1+	AD28	PDA_2	T29	SDA_2	AA30	SD4	AH11
AJ19	SATA_TX1-	AD29	PDACK#	U28	SDACK#	Y28	SD5	AJ17
AK18	SATA_RX1+	AE27	PDREQ	V30	SDREQ	AA28	SD6	AH14
AJ18	SATA_RX1-	AE30	PIOR#	W29	SIOR#	AB28	SD7	AH19
AK14	SATA_TX2+	AE29	PIOW#	W30	SIOIW#	AB27	SD8	AJ20
AJ14	SATA_TX2-	AC28	PDCS0#	R27	SDCS#0	AB29	SD9	AH21
AK13	SATA_RX2-	AC29	PDCS1#	R28	SDCS#1	AA27	SD10	AJ9
AJ13	SATA_RX2+	AE29	P00	Y27	SD10	AA29	SD11	AG16
AK11	SATA_TX3+	AH27	P01	U28	SD11	W27	SD12	AK15
AJ11	SATA_TX3-	AK28	P02	T28	SD12	Y29	SD13	AK20
AK10	SATA_RX3+	AH27	P03	U29	SD13	V27	SD14	
AJ10	SATA_RX3-	AG27	P04	T29	SD14	U27	SD15	
AJ15	SATA_CAL	AJ28	P05	U28	SD15			
AJ16	SATA_X1	AJ29	P06					
AK16	SATA_X2	AH29	P07					
AK8C	SATA_ACT#	AG28	P08					
AH15	PLLVDD_SATA	AE30	P09					
AH16	XTLVDD_SATA	AE28	P10					
AG10	AVDD_SATA_1	AE29	P11					
AG14	AVDD_SATA_2	AE27	P12					
AH12	AVDD_SATA_3	AG29	P13					
AG12	AVDD_SATA_4	AH30	P14					
AG18	AVDD_SATA_5	AH28	P15					
AG21	AVDD_SATA_6	AK29	P16					
AH18	AVDD_SATA_7	AK28	P17					
AG20	AVDD_SATA_8	AH27	P18					
AG9	AVSS_SATA_1	AJ28	P19					
AF10	AVSS_SATA_2	AJ29	P20					
AF11	AVSS_SATA_3	AH29	P21					
AF12	AVSS_SATA_4	AG28	P22					
AF13	AVSS_SATA_5	AE30	P23					
AF14	AVSS_SATA_6	AE29	P24					
AF15	AVSS_SATA_7	AE27	P25					
AF16	AVSS_SATA_8	AG29	P26					
AF17	AVSS_SATA_9	AH30	P27					
AF18	AVSS_SATA_10	AH28	P28					
AF19	AVSS_SATA_11	AK29	P29					
AF20	AVSS_SATA_12	AK28	P30					
AF21	AVSS_SATA_13	AH27	P31					
AF22	AVSS_SATA_14	AJ28	P32					
AH9	AVSS_SATA_15	AJ29	P33					
AG15	AVSS_SATA_16	AH29	P34					
AG17	AVSS_SATA_17	AG28	P35					
AG19	AVSS_SATA_18	AE30	P36					
AG22	AVSS_SATA_19	AE29	P37					
AG23	AVSS_SATA_20	AE27	P38					
AF9	AVSS_SATA_21	AG29	P39					
AH17	AVSS_SATA_22	AH30	P40					
AH23	AVSS_SATA_23	AH28	P41					
AH13	AVSS_SATA_24	AK29	P42					
AH20	AVSS_SATA_25	AK28	P43					
AK9	AVSS_SATA_26	AH27	P44					
AJ12	AVSS_SATA_27	AJ28	P45					
AK17	AVSS_SATA_28	AJ29	P46					
AK23	AVSS_SATA_29	AH29	P47					
AH10	AVSS_SATA_30	AG28	P48					
AJ23	AVSS_SATA_31	AE30	P49					
	AVSS_SATA_32	AE29	P50					

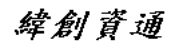
R207  
0R2-0

CHS-215SB400

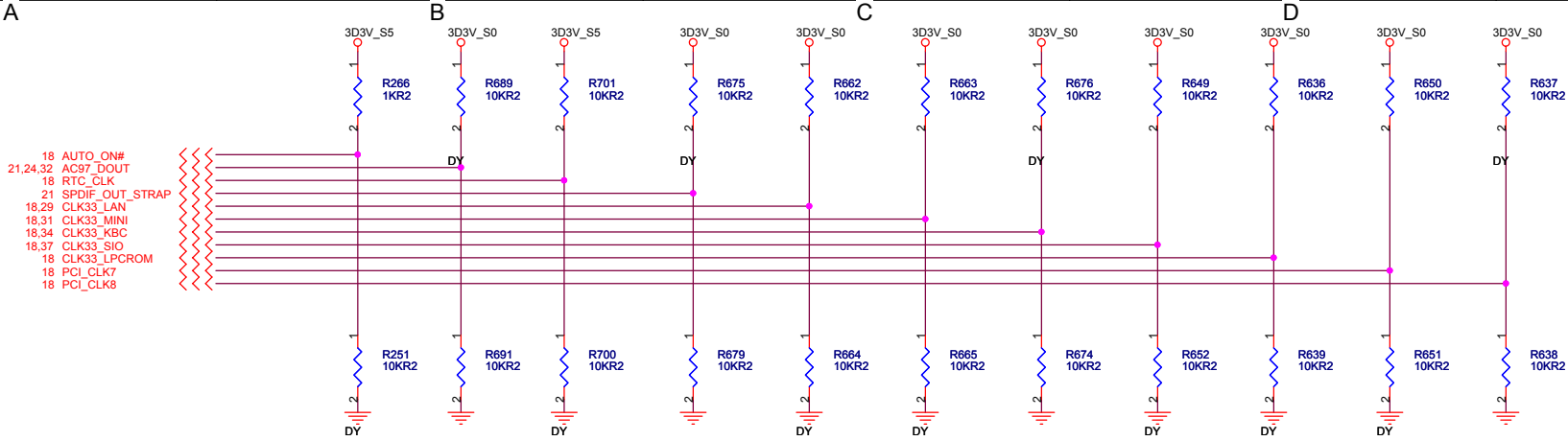
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SB400 ACPI/GPIO/SATA/IDE (2 of 5)		
Size	Document Number	Rev
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Date:	Thursday, November 18, 2004	Sheet 19 of 56



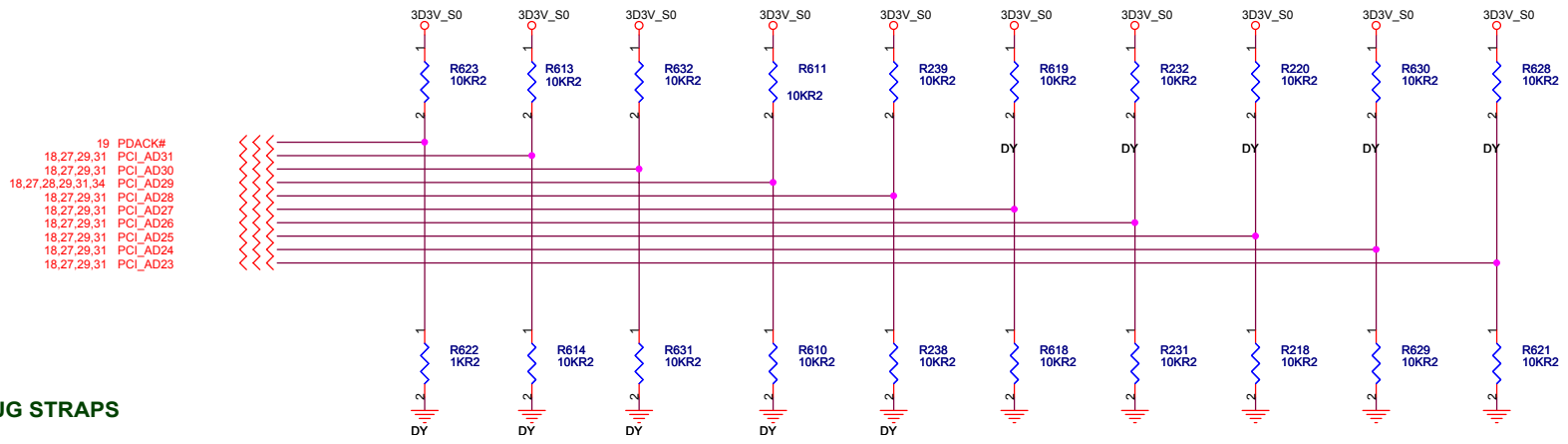
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>SB400 POWER/DECOUPLING</b>	
Title	
Size A3	Document Number
<b>SNIFE</b>	
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**REQUIRED SYSTEM STRAPS**

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
<b>STRAP HIGH</b>	MANUAL PWR ON <b>DEFAULT</b>	USE DEBUG STRAPS	INTERNAL RTC <b>DEFAULT</b>	SIO 24MHz	48MHZ-Clock Input Buffer <b>DEFAULT</b>	USB PHY PWRDOWN DISABLE <b>DEFAULT</b>	USB INT PLL48 <b>DEFAULT</b>	14MHZ OSC MODE <b>DEFAULT</b>	CPU I/F=K8 <b>DEFAULT</b>	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	
<b>STRAP LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS <b>DEFAULT</b>	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz <b>DEFAULT</b>	48MHZ-Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM	



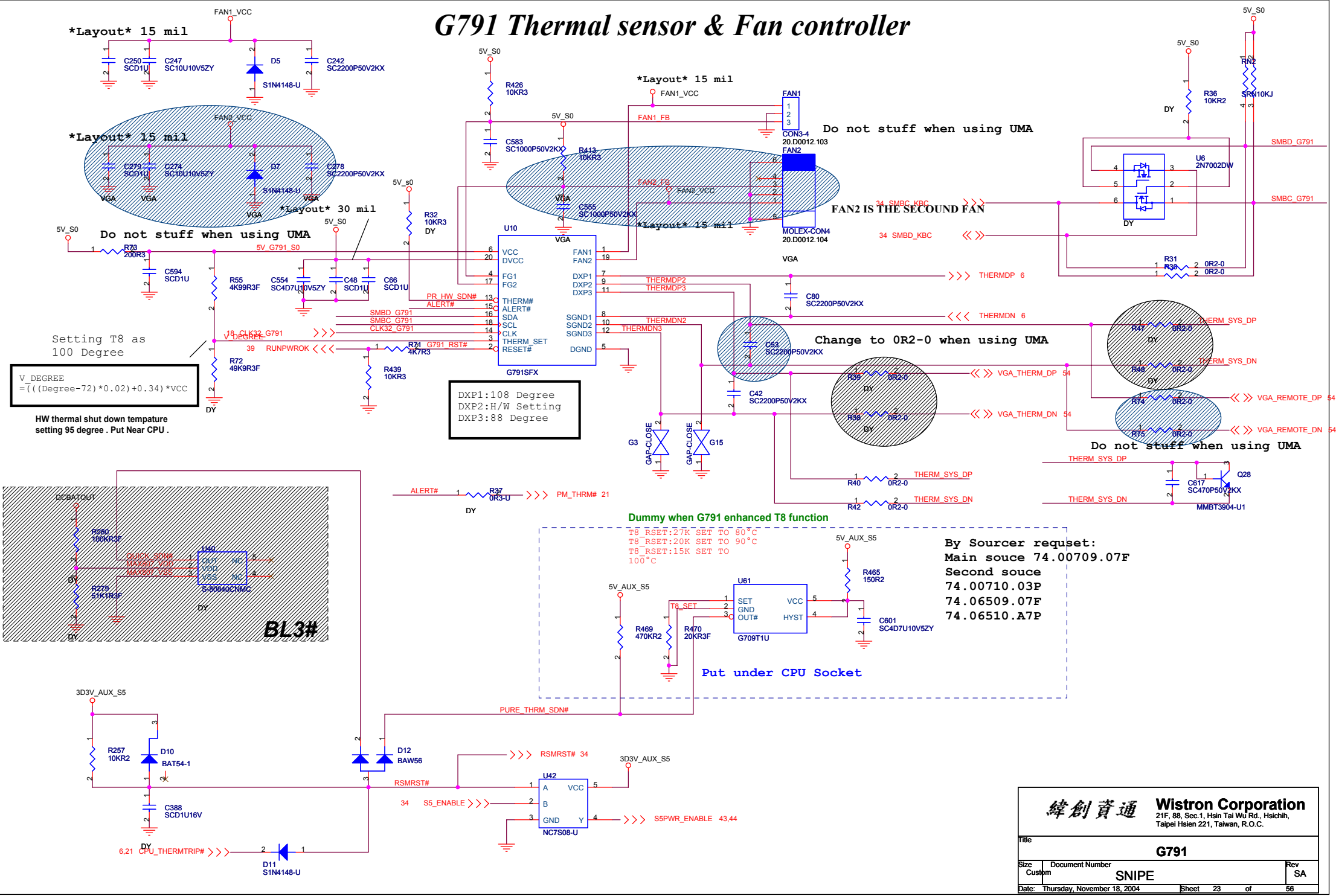
**DEBUG STRAPS**

	PDAck#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>STRAP HIGH</b>	USE LONG RESET <b>DEFAULT</b>	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
<b>STRAP LOW</b>	USE SHORT RESET					USE PCI PLL <b>DEFAULT</b>	USE ACPI BCLK <b>DEFAULT</b>	USE IDE PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	

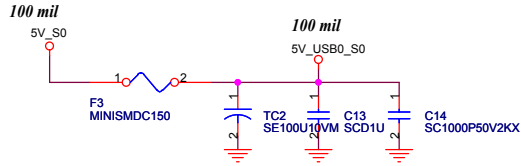
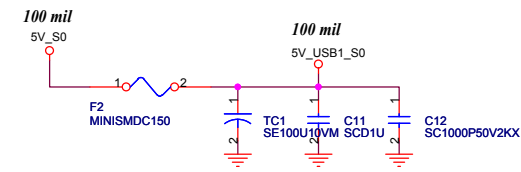
**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB400 STRAPPING PIN**  
 Size A3 Document Number **SNIE** Rev **SA**  
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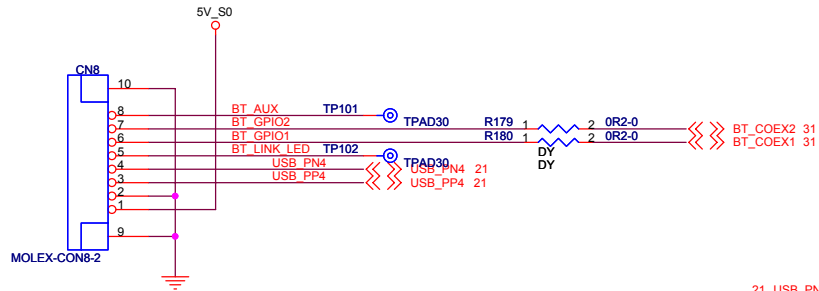
# G791 Thermal sensor & Fan controller



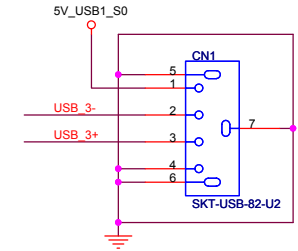
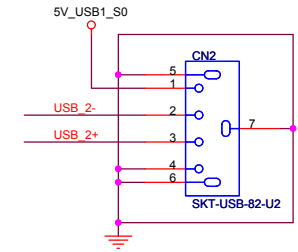
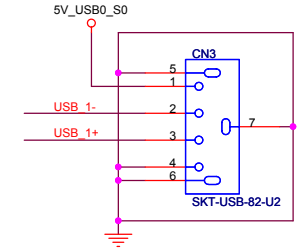
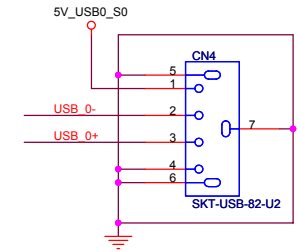
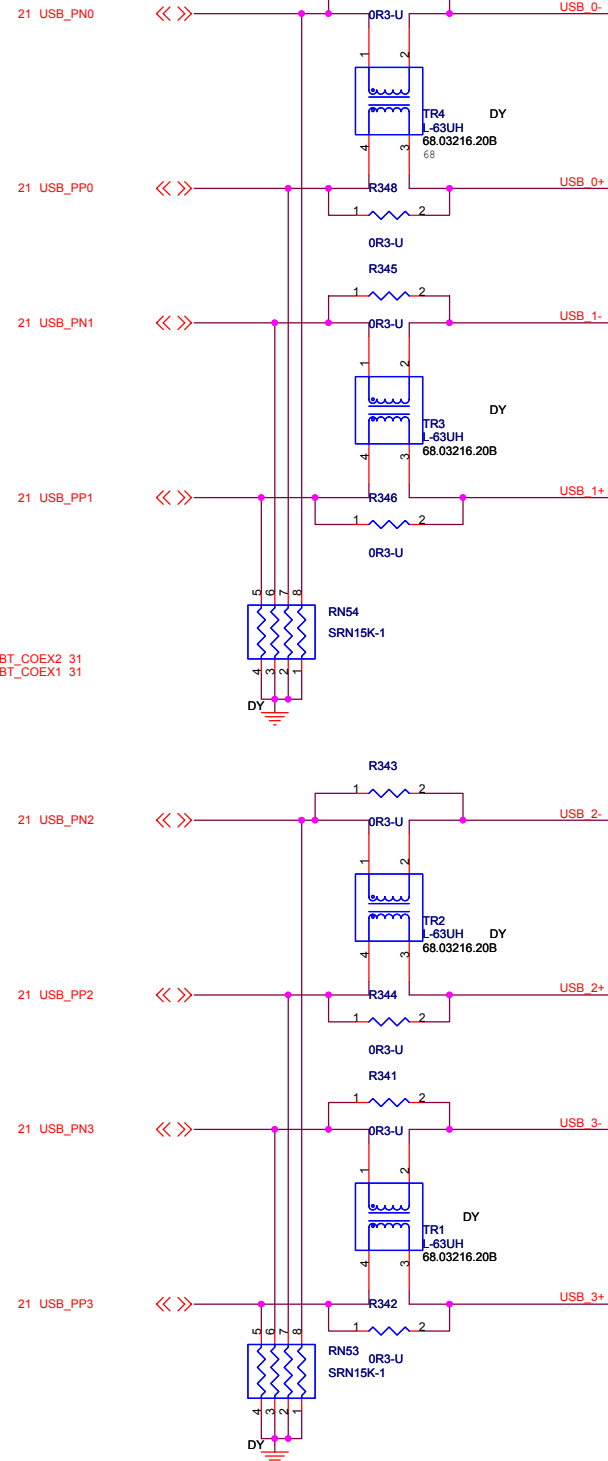
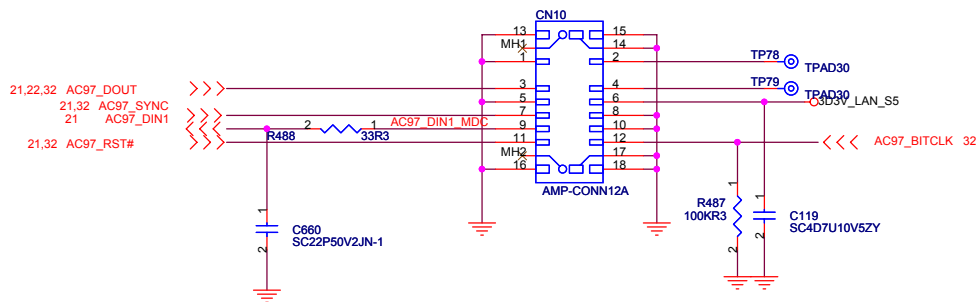
# USB PORT



## BLUETOOTH MODULE CONNECTOR



## MDC 1.5 CONNECTOR



By Sourcer request change P/N:  
From 22.10218.701  
To 22.10218.F51

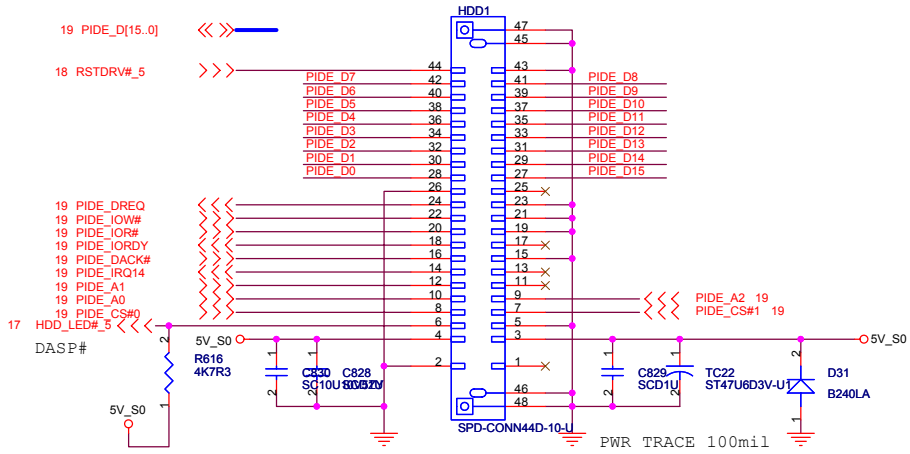
By ME request P/N:  
Main 22.10218.F51  
Second 22.10218.F41

**緯創資通** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

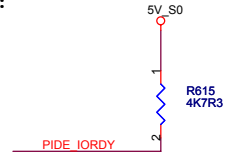
Title <b>USB and MDC</b>		
Size A3	Document Number <b>SNIFE</b>	Rev SA
Date: Thursday, November 18, 2004	Sheet 24	of 56



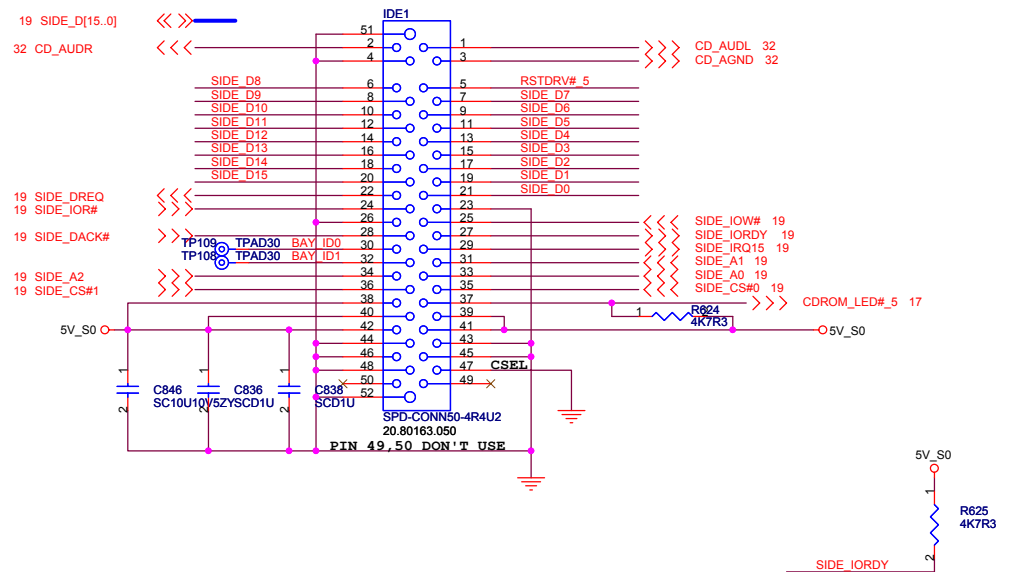
# HDD



By ME request change P/N:  
 from 20.F0385.044  
 to 20.F0385.A44



# CDROM

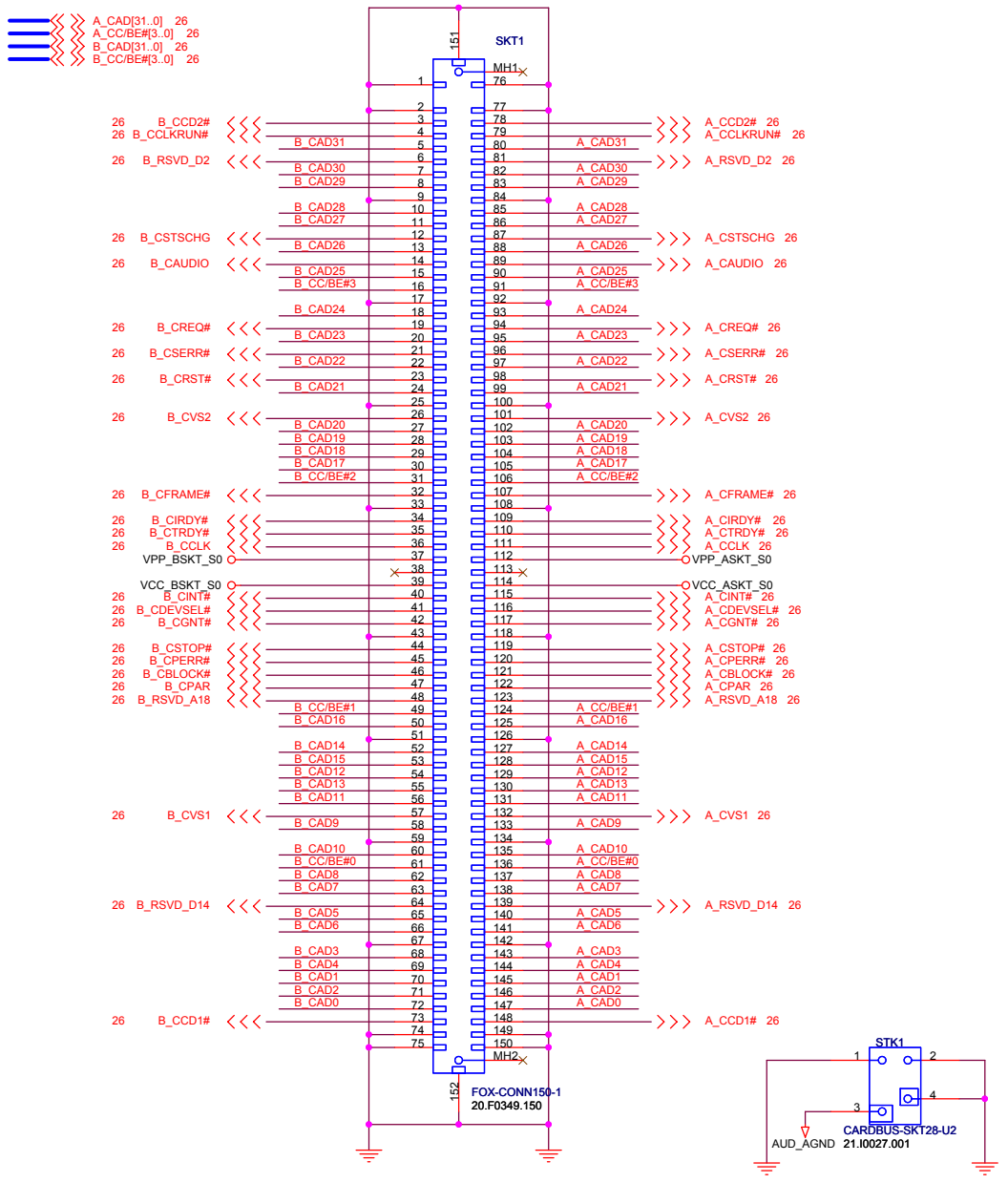
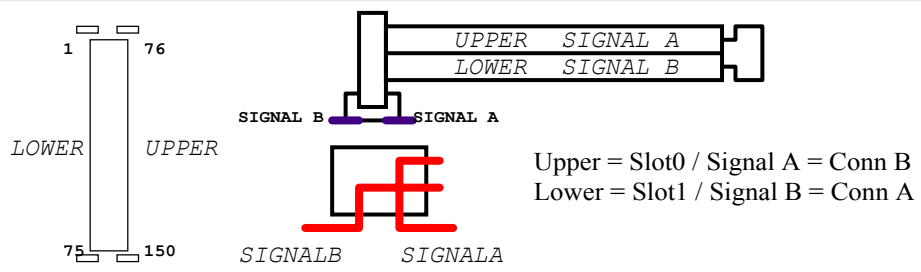


**緯創資通** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

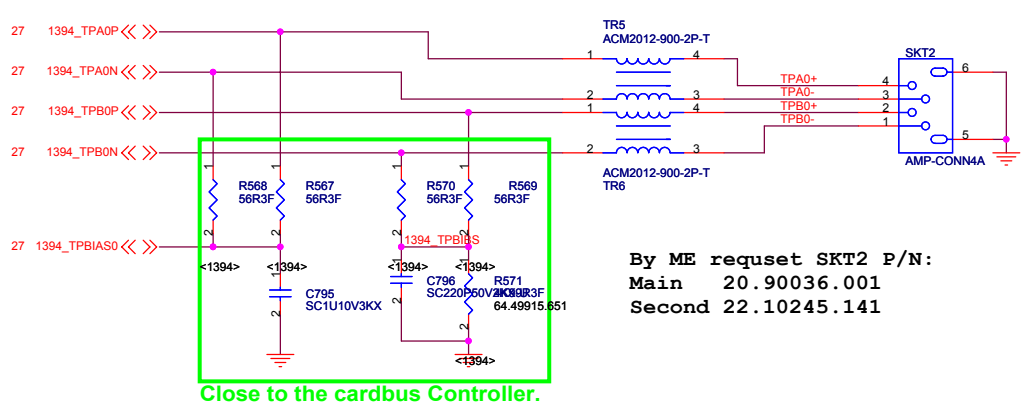
Title <b>HDD / CDROM</b>		
Size A3	Document Number <b>SNIPE</b>	Rev SA
Date: Thursday, November 18, 2004	Sheet 25 of 56	



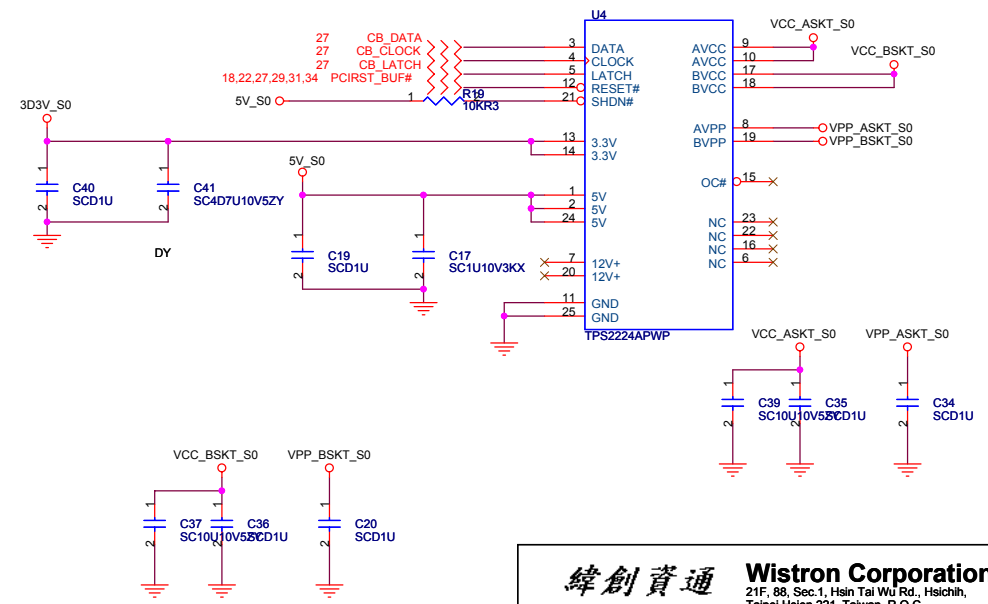




# 1394 Connector



# Power switch



緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

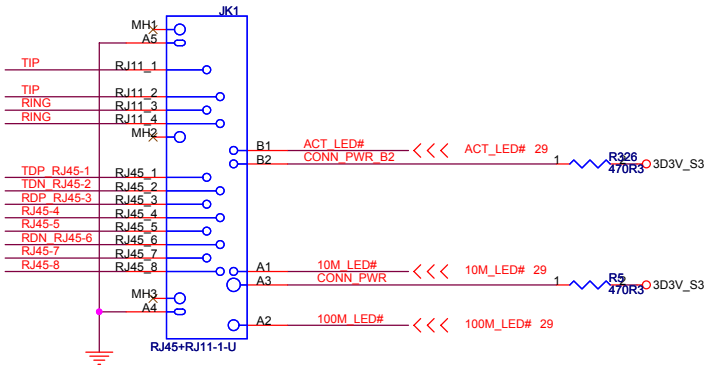
Title: **PCMCA SLOT\_1394 CONN**

Size A3 Document Number **SNIFE** Rev SA

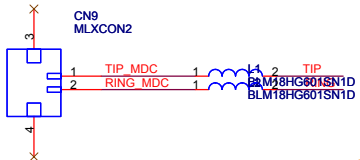
Date: Thursday, November 18, 2004 Sheet 28 of 56



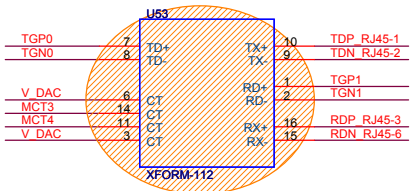
Link: Green - 10Mbps/802.11b  
 Orange - 100Mbps/802.11a  
 Yellow - 1Gbps



By ME request for  
 10/100 LAN change P/N:  
 From 22.10177.621  
 To 22.10177.731  
 By ME request for  
 GigaLAN JK1 P/N:  
 Main 22.10177.601  
 Second 22.10245.771  
 By ME request change P/N:  
 From 20.D0121.102  
 To 21.D0010.102



Do not stuff  
 when using GLAN



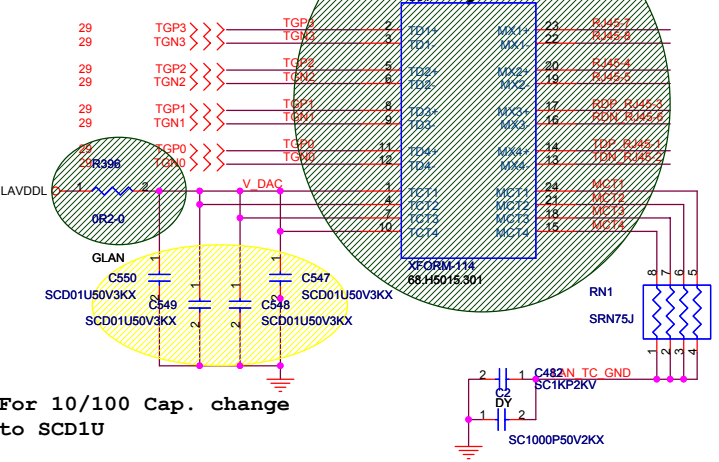
**10/100M Lan Transformer**

By Sourcer request change P/N:  
 From 68.H0013.301  
 To 68.0H80P.301

Do not stuff  
 when using 10/100

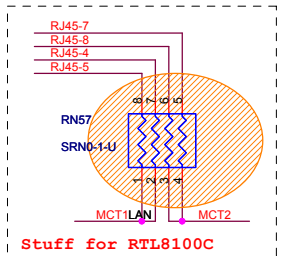
By Sourcer request change P/N:  
 From 68.H5015.301  
 To 68.02402.30A

**GIGA Lan Transformer**



For 10/100 Cap. change  
 to SCD1U

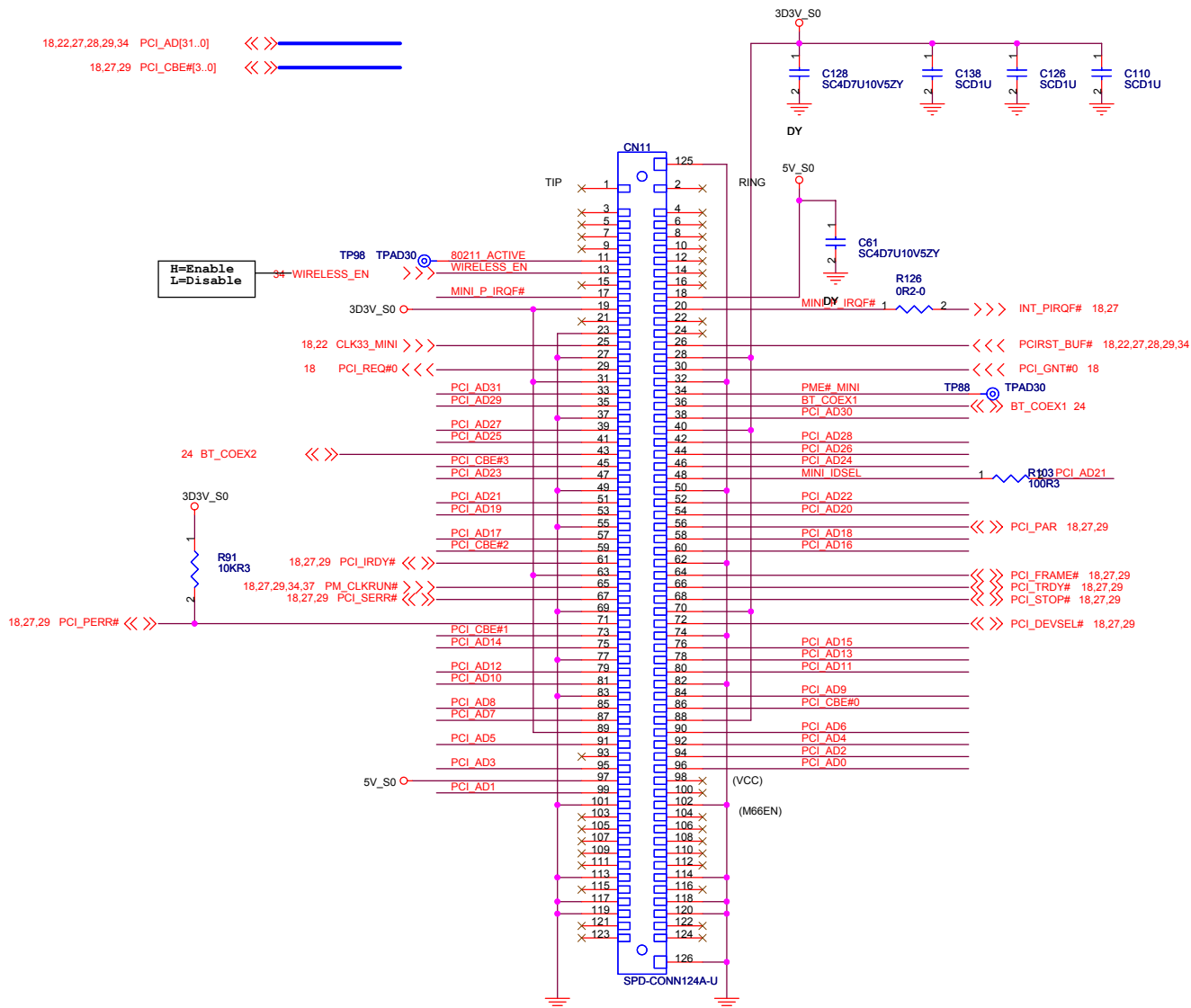
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



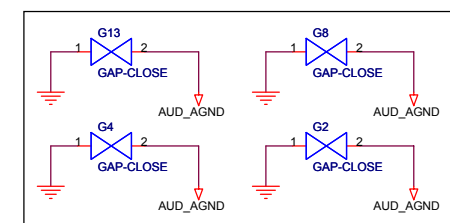
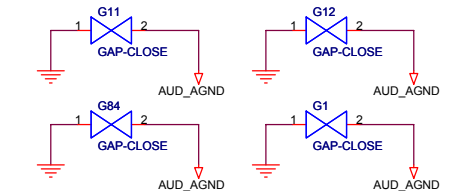
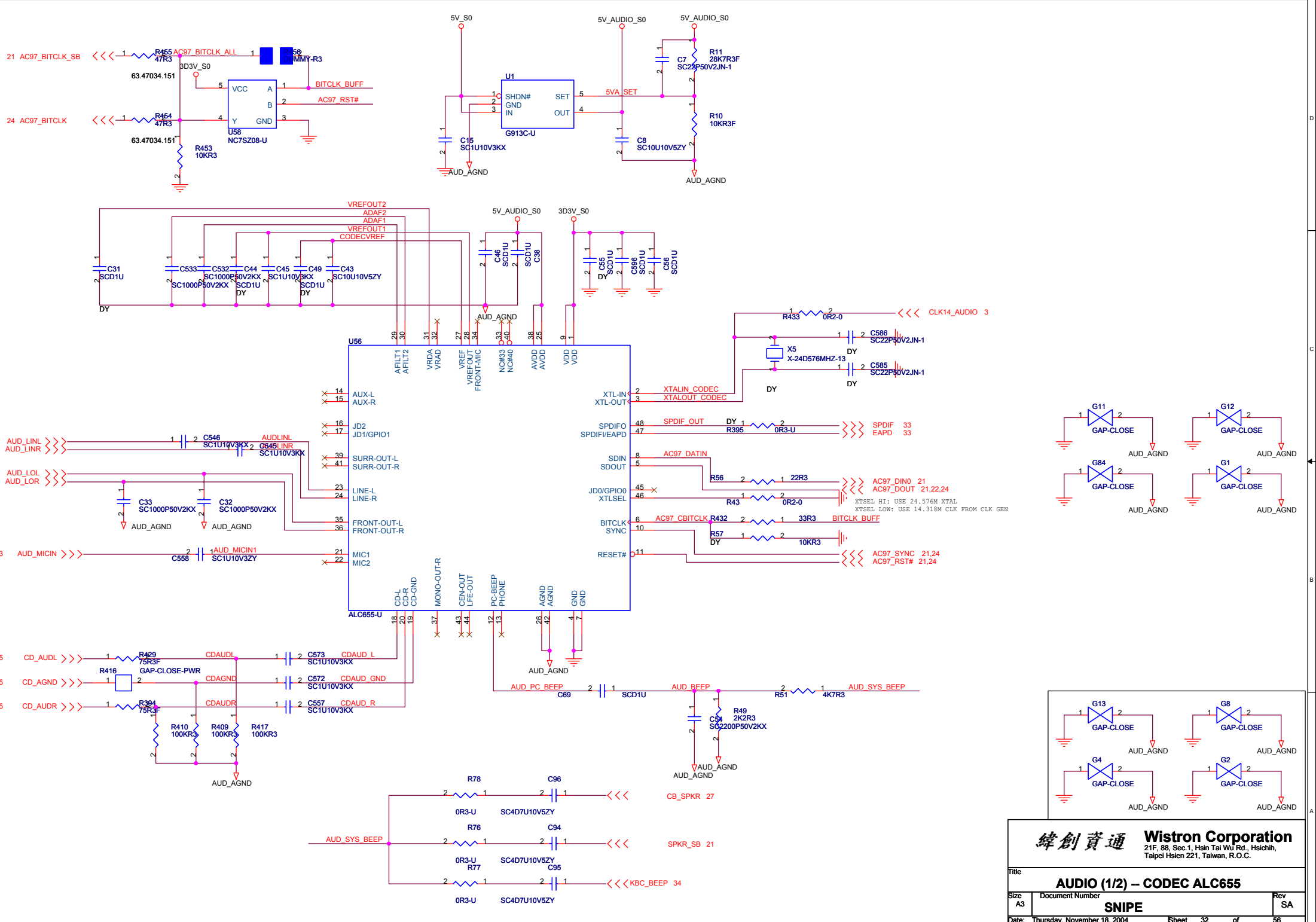
Stuff for RTL8100C  
 Do not stuff  
 when using GLAN

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>LAN_CONN 10/100/1000</b>	
Size A3	Document Number SA
<b>SNIFE</b>	
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# MINI-PCI



<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>MINI-PCI</b>	
Size	Document Number
A3	<b>SNIFE</b>
Date: Thursday, November 18, 2004	Sheet 31 of 56
Rev	SA



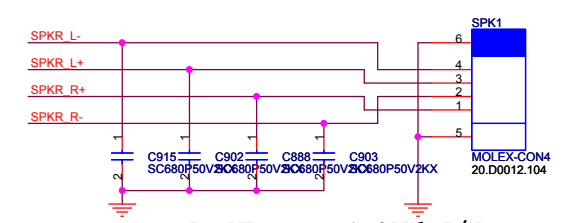
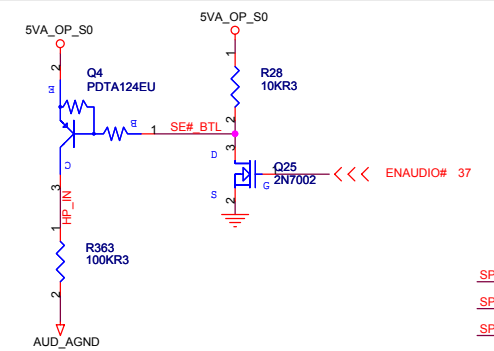
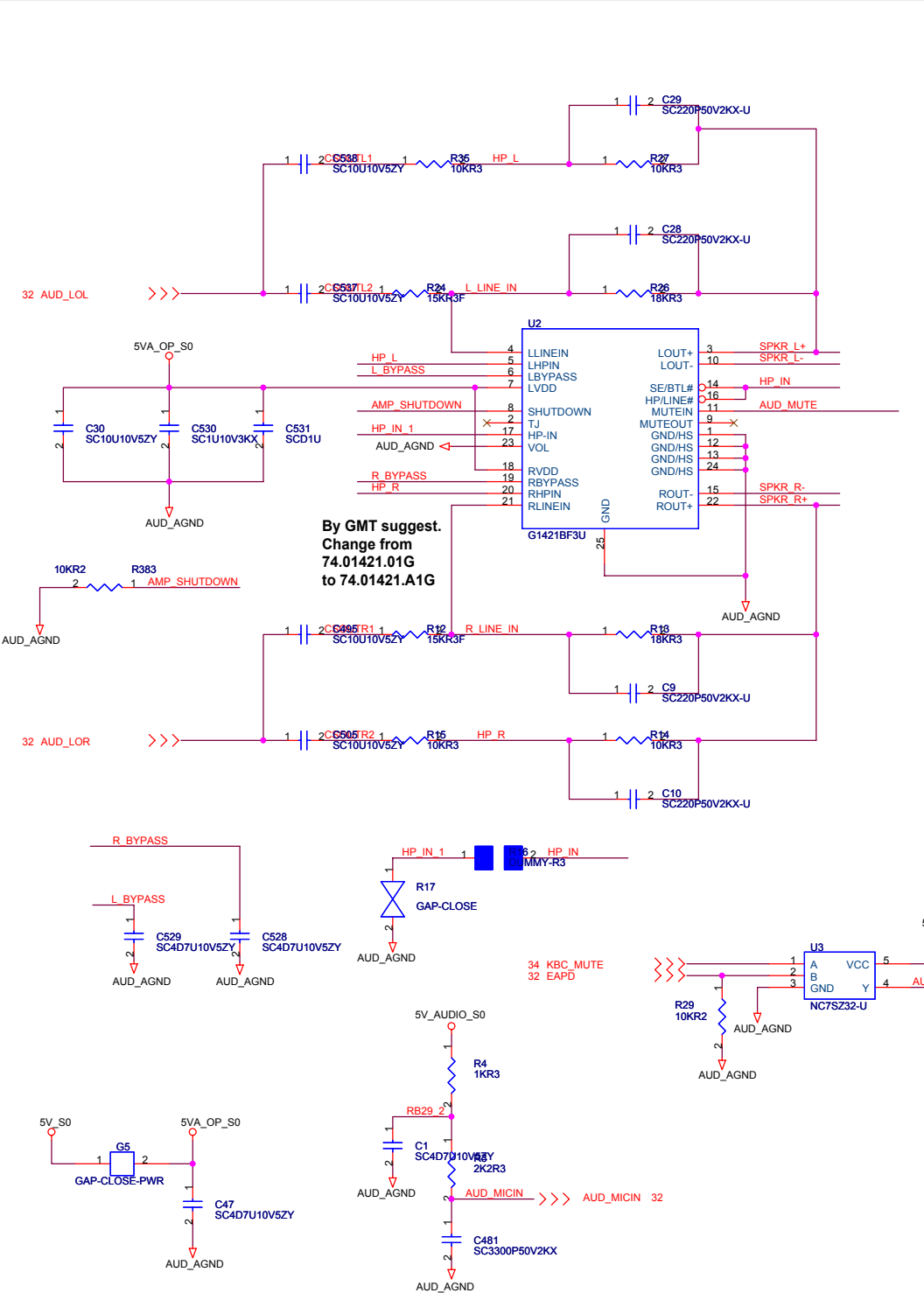
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **AUDIO (1/2) - CODEC ALC655**

Size: A3 Document Number: **SNIFE** Rev: SA

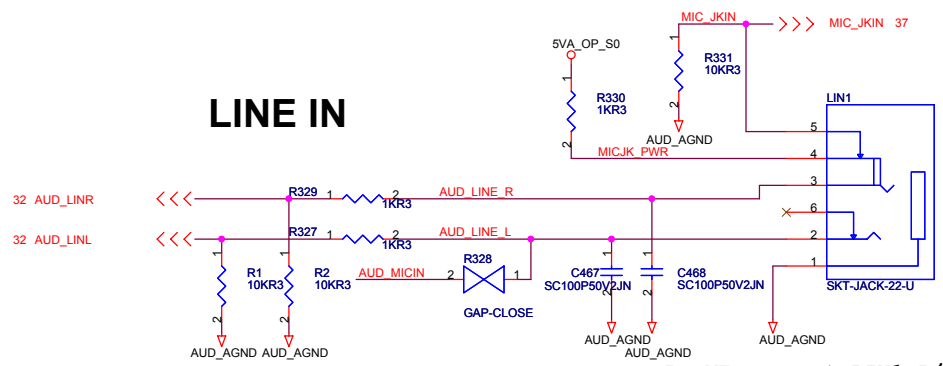
Date: Thursday, November 18, 2004 Sheet: 32 of 56





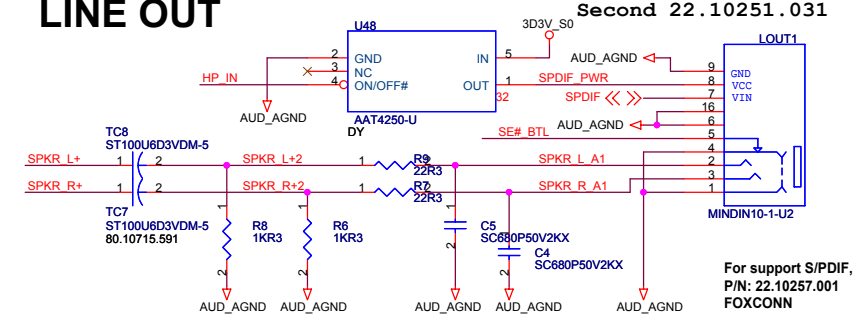
By ME request SPK1 P/N:  
Main 20.D0012.104  
Second 20.D0152.104

### LINE IN



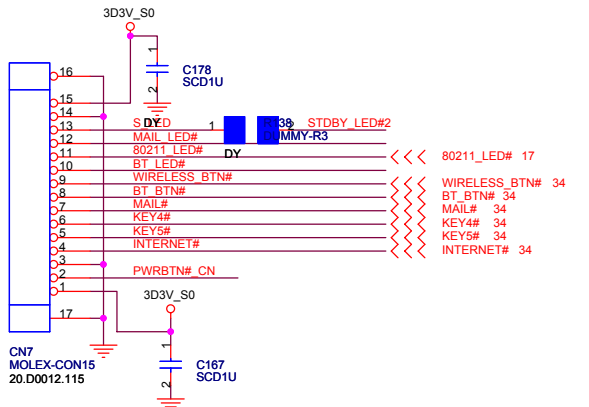
By ME request LIN1 P/N:  
Main 22.10271.031  
Second 22.10088.381  
By ME request LOUT1 P/N:  
Main 22.10147.031  
Second 22.10251.031

### LINE OUT

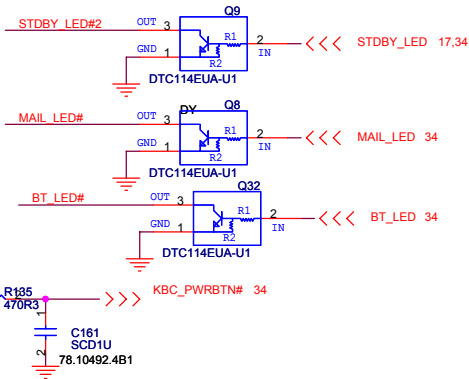


<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>AUDIO (2/2)</b>	
Size	Document Number
A3	<b>SNIFE</b>
Date: Thursday, November 18, 2004	Sheet 33 of 56
Rev	SA

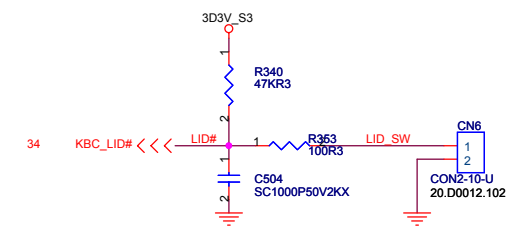
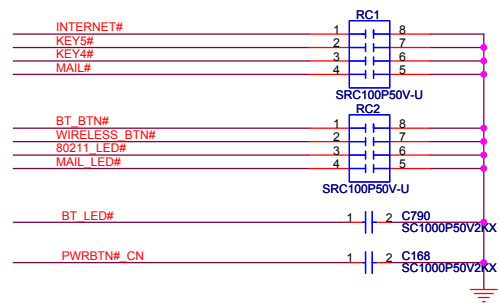




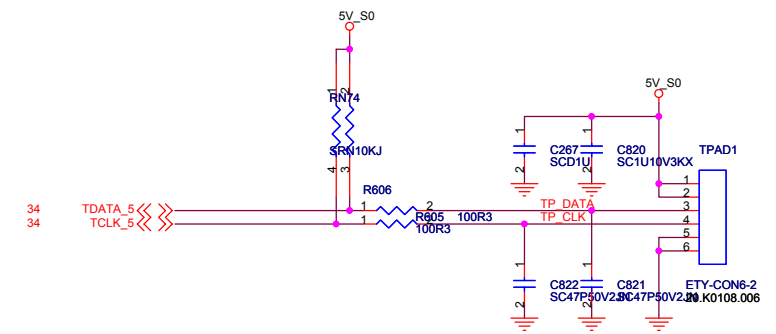
**POWER BUTTON**



**Launch Board CONN**



**Cover Up Switch**



**TOUCH PAD**

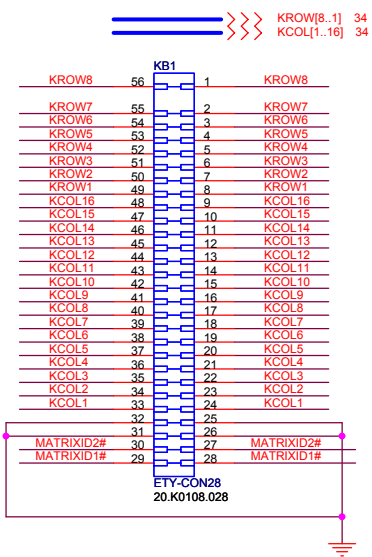
**Internal Keyboard CONN**



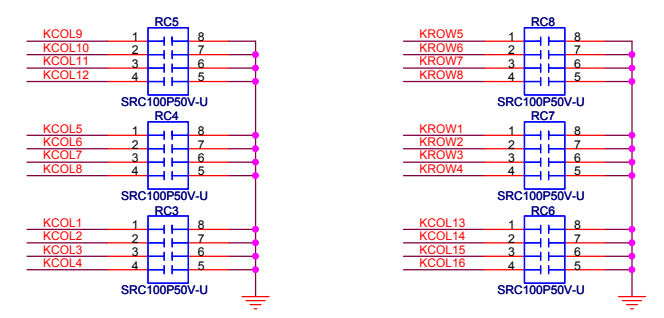
Keyboard matrix ( from vendor )				
	US	Jap	Eur	Other

Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

hexainf@hotmail.com  
GRATIS - FOR FREE



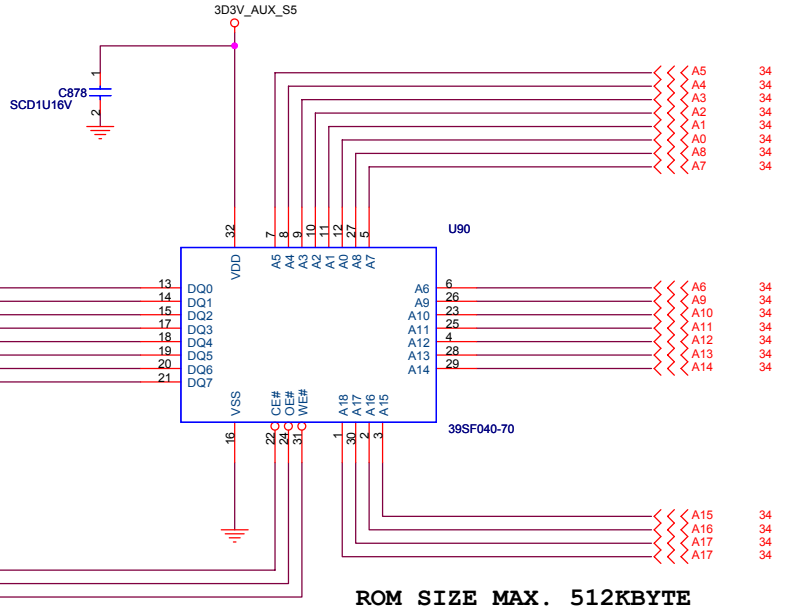
**EMI Bypass cap.**



**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH / TOUCHPAD / KB CONN**  
Size: A3 Document Number: **SNIFE** Rev: SA  
Date: Thursday, November 18, 2004 Sheet: 35 of 56

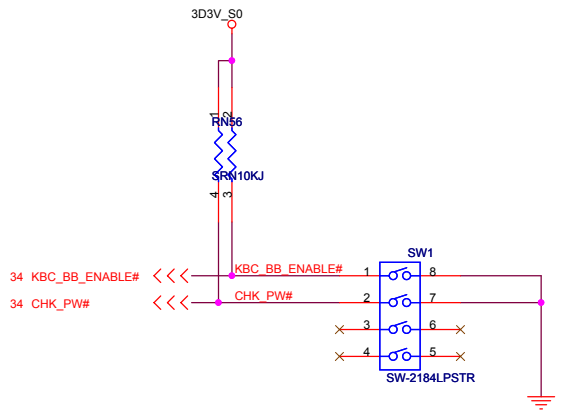
>>> KBC\_D[0..7] 34

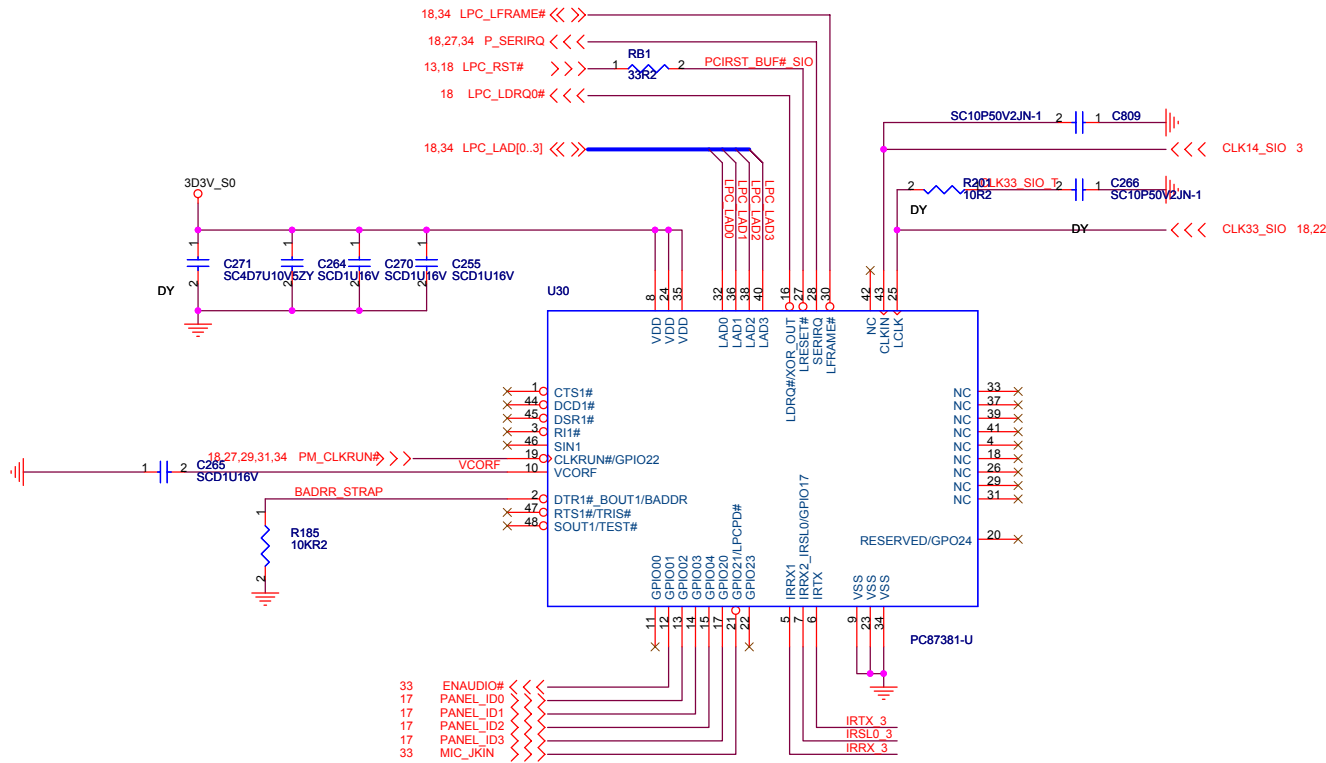


34 KBC\_D0  
34 KBC\_D1  
34 KBC\_D2  
34 KBC\_D3  
34 KBC\_D4  
34 KBC\_D5  
34 KBC\_D6  
34 KBC\_D7

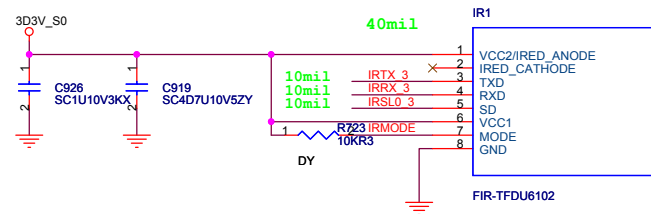
34 KBCBIOS\_CS#  
34 KBCBIOS\_RD#  
34 KBCBIOS\_WE#

PLCC32 Socket P/N:  
SSKT3262.10002.032  
SSKT32 62.10005.032





### Infineon FIR Module

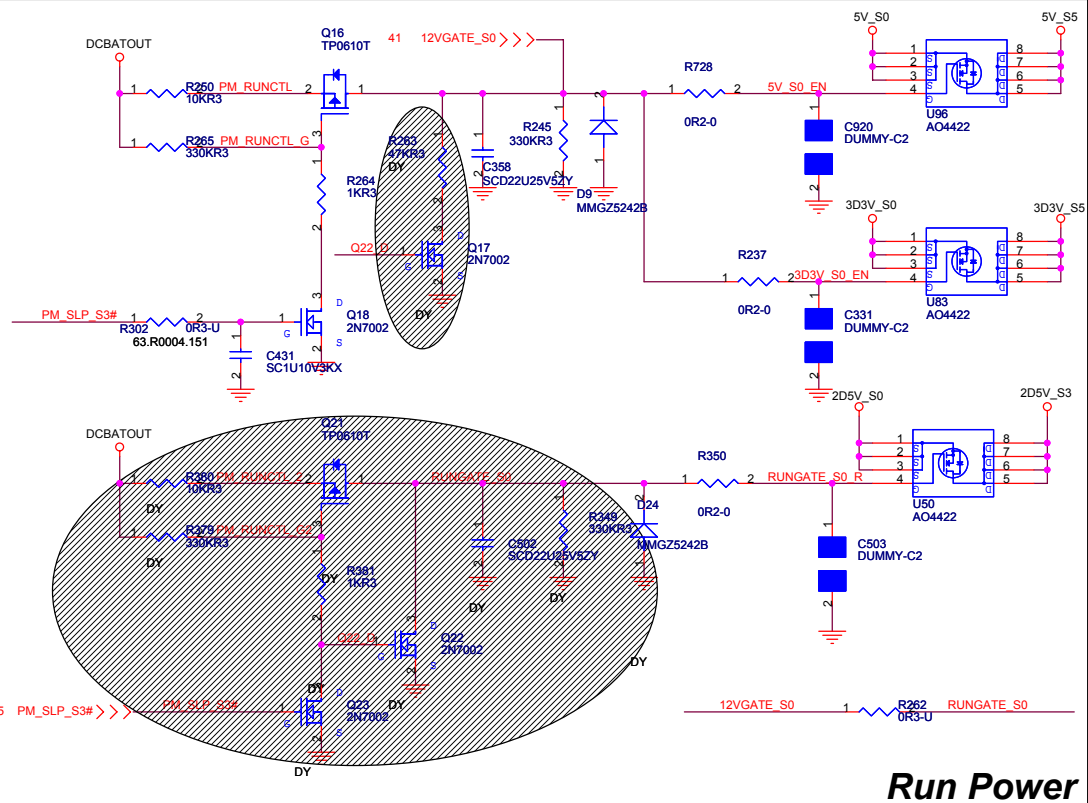


PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDOR
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14") SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO (15")
0	1	0	0	CMO (14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

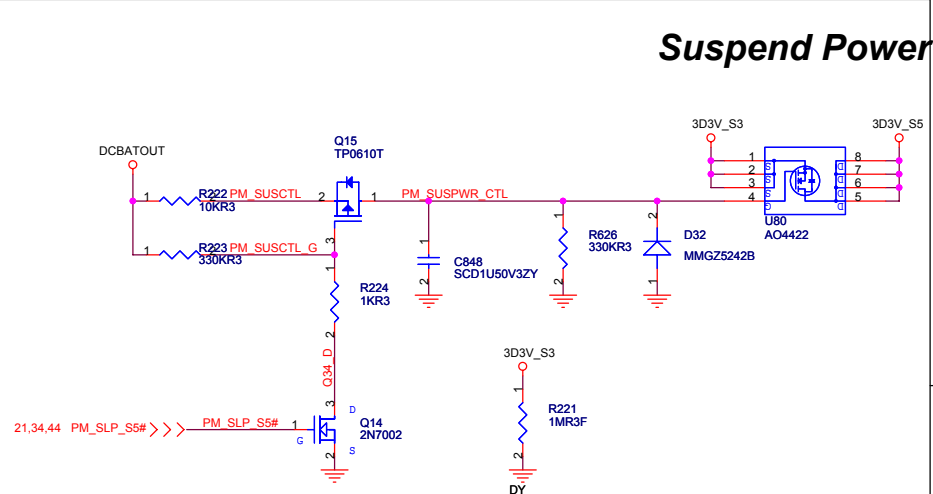
Note : AU (友達), CMO (奇美), \*\* : With Digitizer

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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>SUPER IO NC87381</b>			
Size A3	Document Number <b>SNIFE</b>	Rev SA	
Date: Thursday, November 18, 2004	Sheet 37	of	56

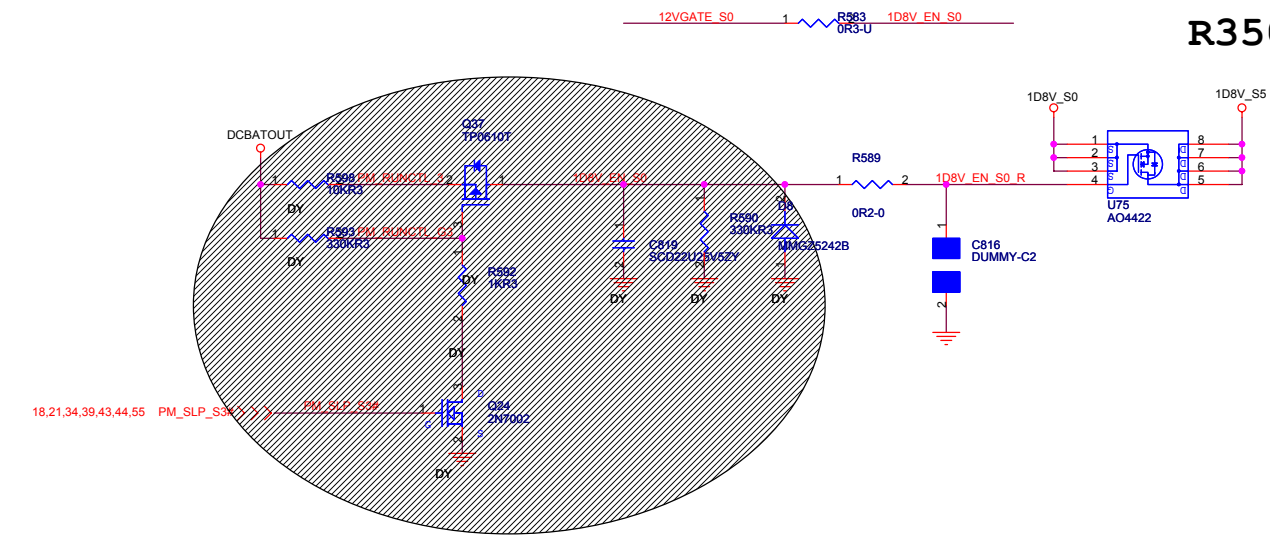


Run Power



Suspend Power

R350 & R589 WILL BE REMOVED ON VER SB

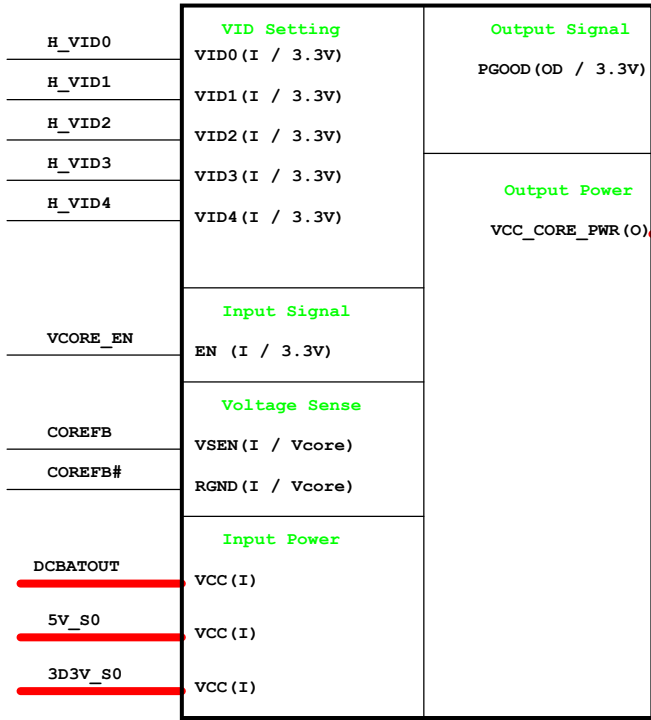


Power On Logic

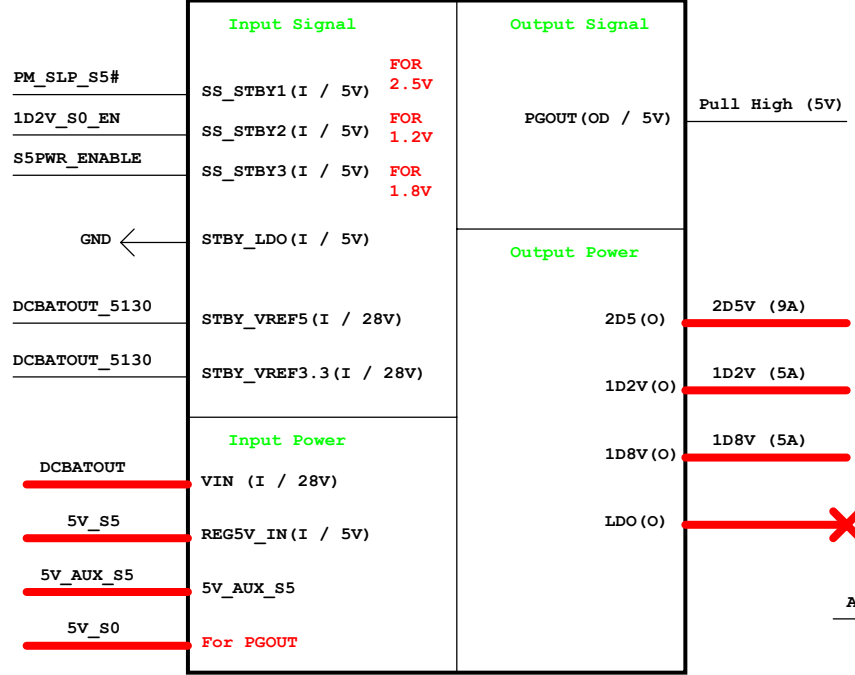
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title: PWR CTL LOGIC / PWR PLANE</p>	
Size: A3	Document Number: SNIPE
Date: Thursday, November 18, 2004	Sheet: 38 of 56



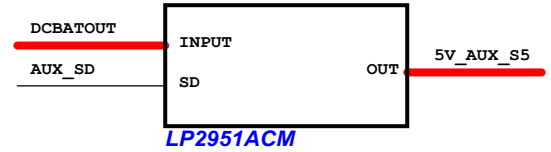
**CPU\_CORE**  
Intersil 6559CR + ISL6207CB\*3 (Dummy \*1)



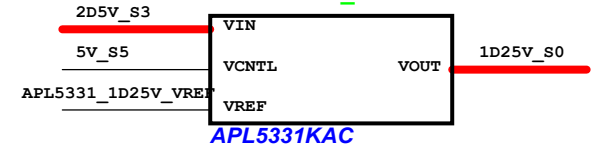
**TI TPS5130**  
2D5V/1D2V/1D8V



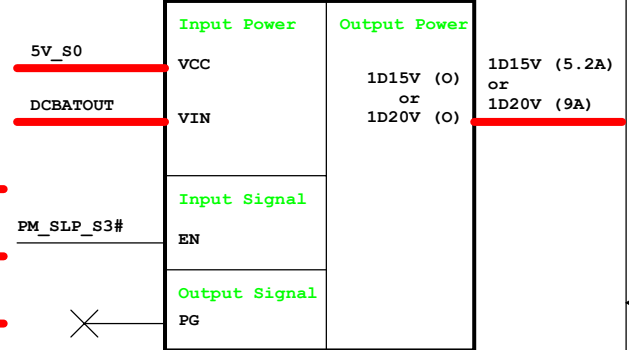
**5V\_AUX\_S5**



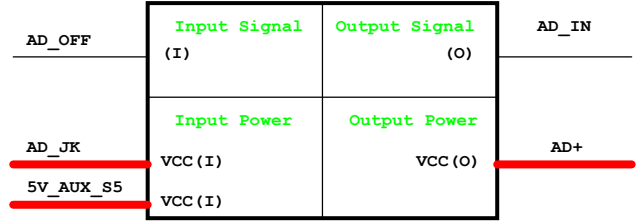
**1D25V\_S3**



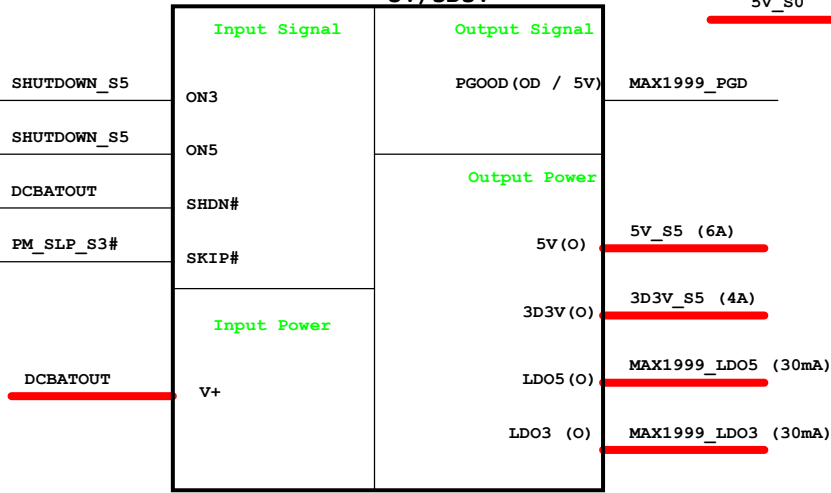
**FAN5234 VGA Core**  
1D15V or 1D20V



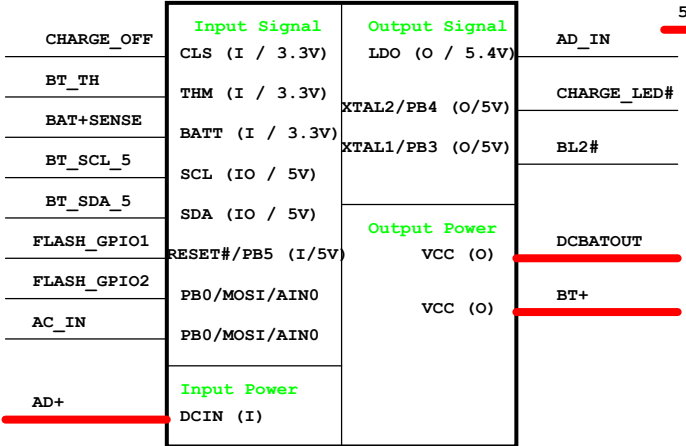
**Adapter**



**Max1999**  
5V/3D3V



**Charger\_Max1909**



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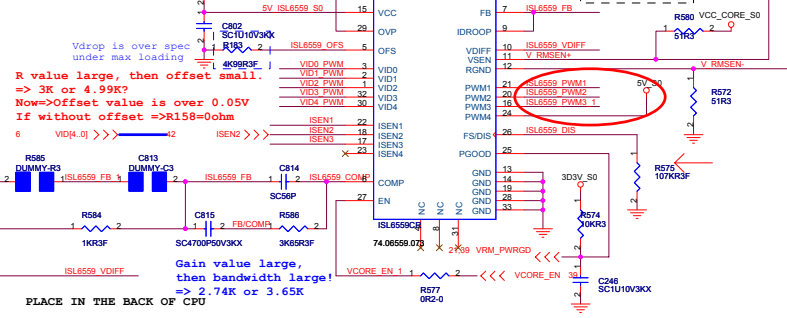
Title: **Power Block Diagram**

Size: A3 Document Number: **SNIFE** Rev: SA

Date: Thursday, November 18, 2004 Sheet: 40 of 56



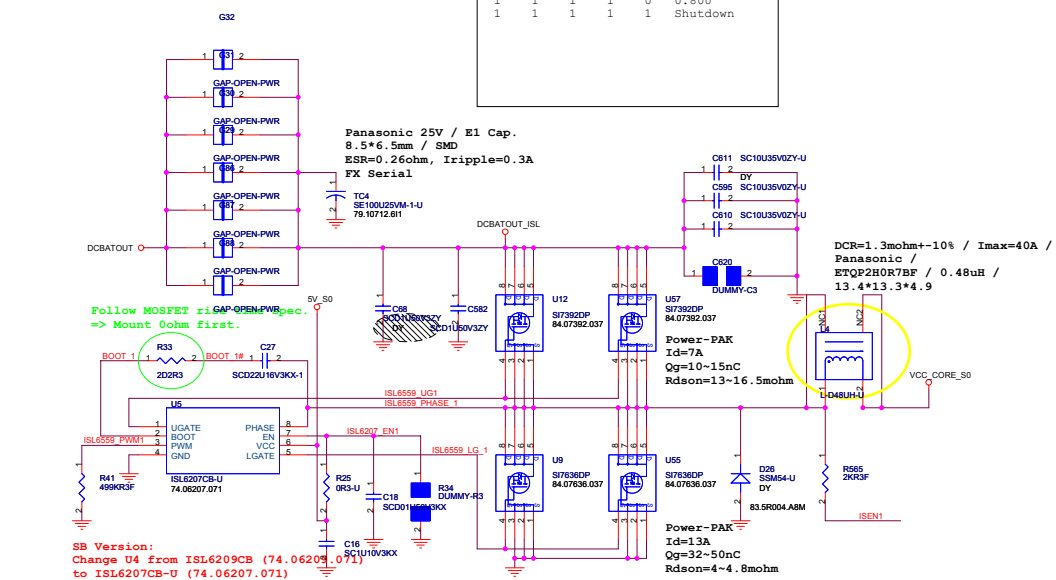
Vcore\_CPU=1.500V  
 Iomax=52.9A  
 Vcore\_CPU=1.400V  
 Iomax=42.7A



Vdrop is over spec under max loading  
 => 3K or 4.99K?  
 Now=>Offset value is over 0.05V  
 IF without offset =>R158=0ohm  
 R value large, then offset small.  
 Gain value large, then bandwidth large!  
 => 2.74K or 3.65K  
 PLACE IN THE BACK OF CPU

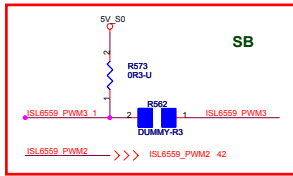
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	DAC	Volt
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	0	1	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown



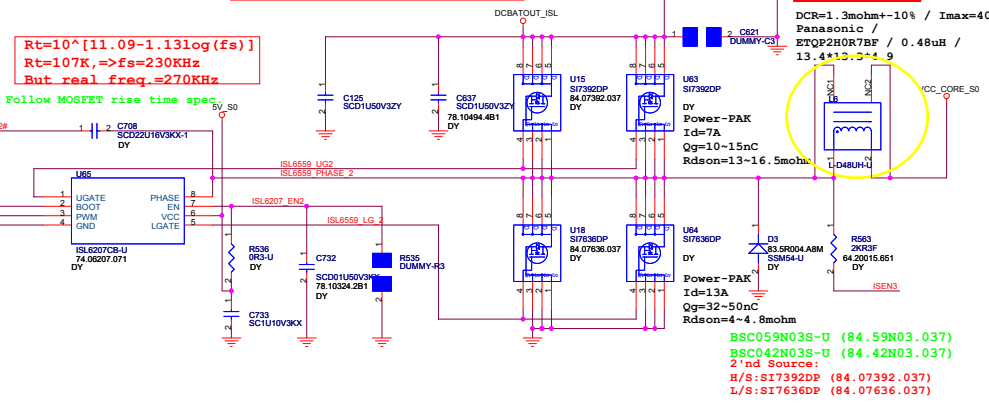
SB Version:  
 Change U4 from ISL6209CB (74.06209.071)  
 to ISL6207CB-U (74.06207.071)

$R_t = 10^{\wedge} [11.09 - 1.13 \log (f_s)]$   
 $R_t = 107K, \Rightarrow f_s = 230KHz$   
 But real freq. = 270KHz  
 Follow MOSFET rise time spec

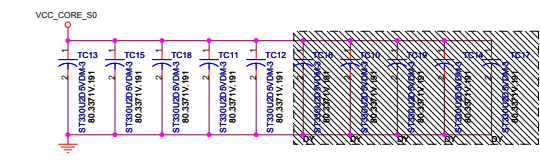
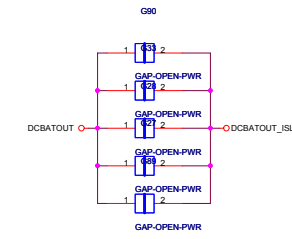


53A\*1.5=79.5A (OCP), =>79.5A/2Phase=39.75A/Phase  
 90uA\*Rsense=39.75A\*(6.5m/2)\*1.4  
 =>Rsense=2.0K

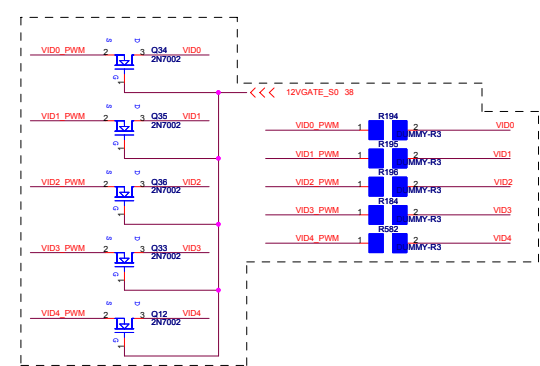
C216/C201/C140  
 Can not stuff!



BSC059N03S-U (84.59N03.037)  
 BSC042N03S-U (84.42N03.037)  
 2'nd Source:  
 R/S:SI7392DP (84.07392.037)  
 L/S:SI7636DP (84.07636.037)

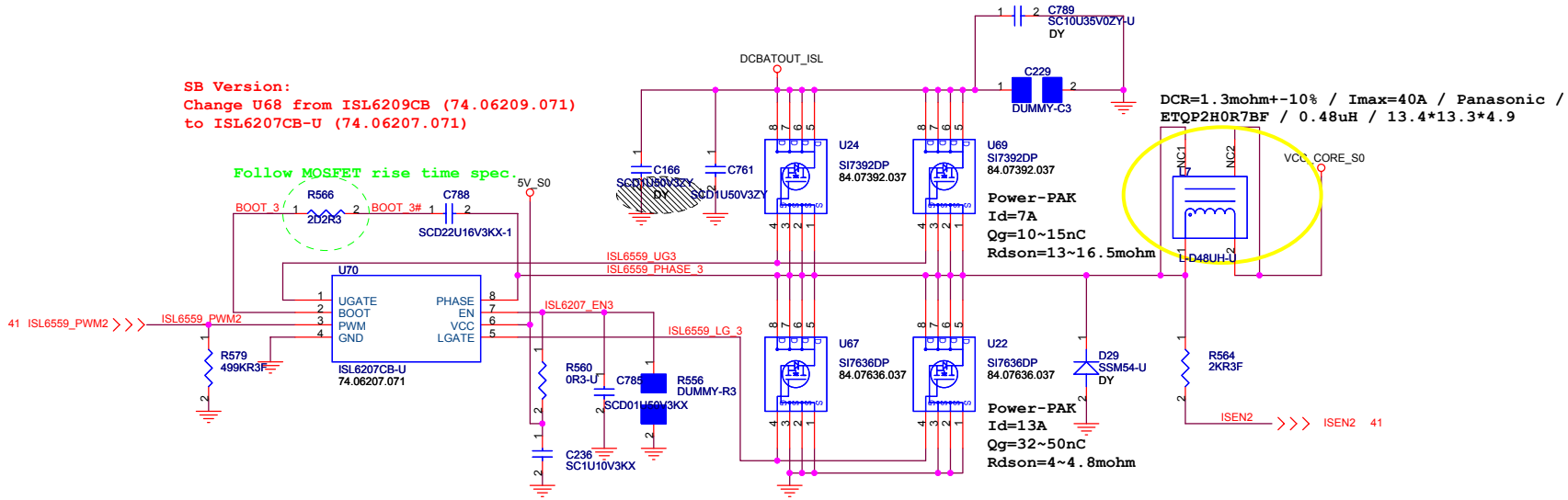


Main Source:  
 KEMET 2D5V/330uF / ESR=9mohm / Iripple=3.7A / ST330U2D5VDM-3  
 80.3371V.191 / 7.3\*4.3\*1.9 / NTS:9.5  
 2'nd Source:  
 Panasonic 2V/330uF / ESR=9mohm / Iripple=3.0A / SE330U2VDM-2  
 79.33719.20A / 7.3\*4.3\*1.9 / NTS:10.0



SB Version:  
 Change U68 from ISL6209CB (74.06209.071)  
 to ISL6207CB-U (74.06207.071)

Follow MOSFET rise time spec.



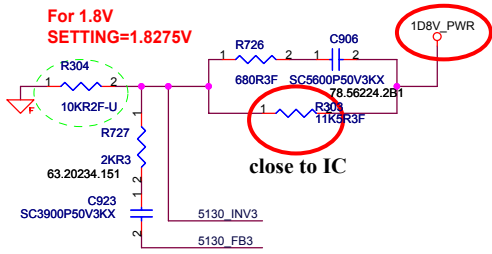


# TI TPS5130 for 2.5V, 1.2V, 1.8V

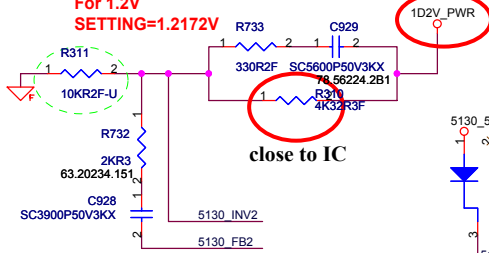
$$V_o = (R1 * 0.85) / R2 + 0.85$$

(2.5V=>CH1, 1.2V=>CH2, 1.8V=>CH3)

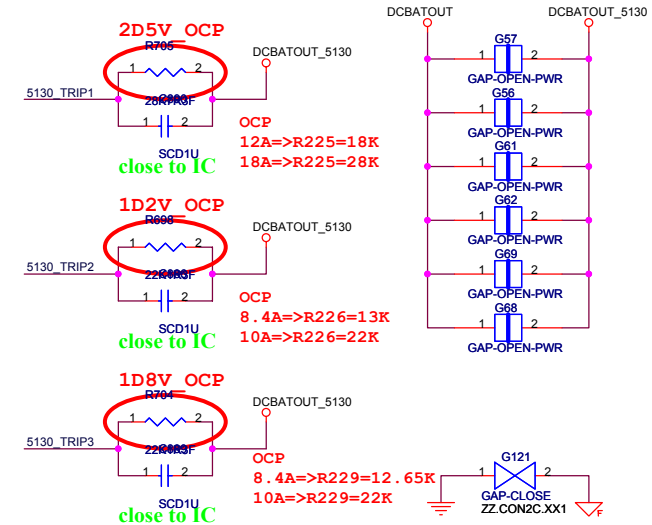
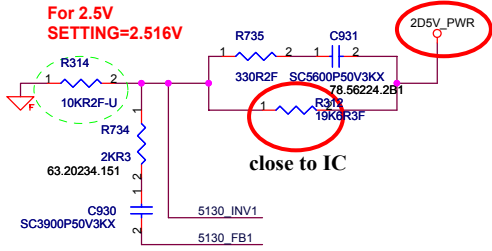
For 1.8V  
SETTING=1.8275V



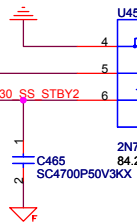
For 1.2V  
SETTING=1.2172V



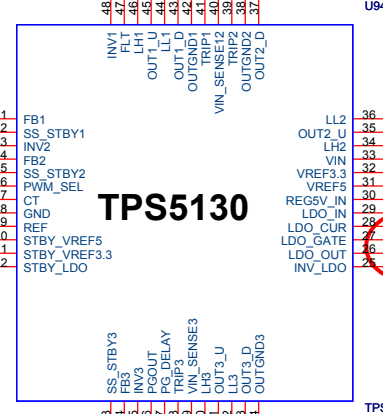
For 2.5V  
SETTING=2.516V



$$T(\text{soft}) = 1.736\text{ms}$$



## TPS5130



## LDO SETTING

	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V (Min) ~
	L : PWM fixed (300KHz)	~0.3V (Max)

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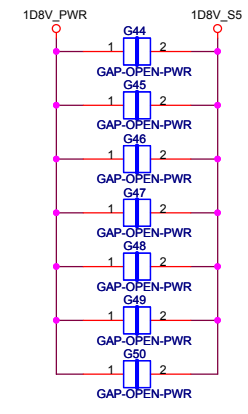
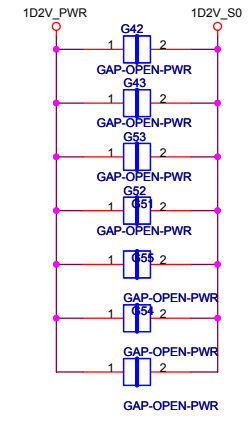
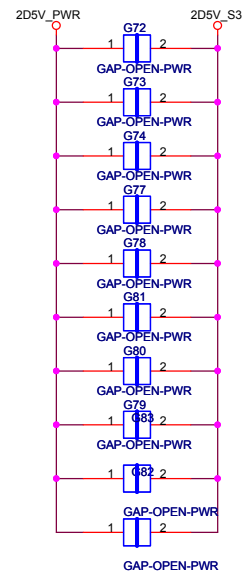
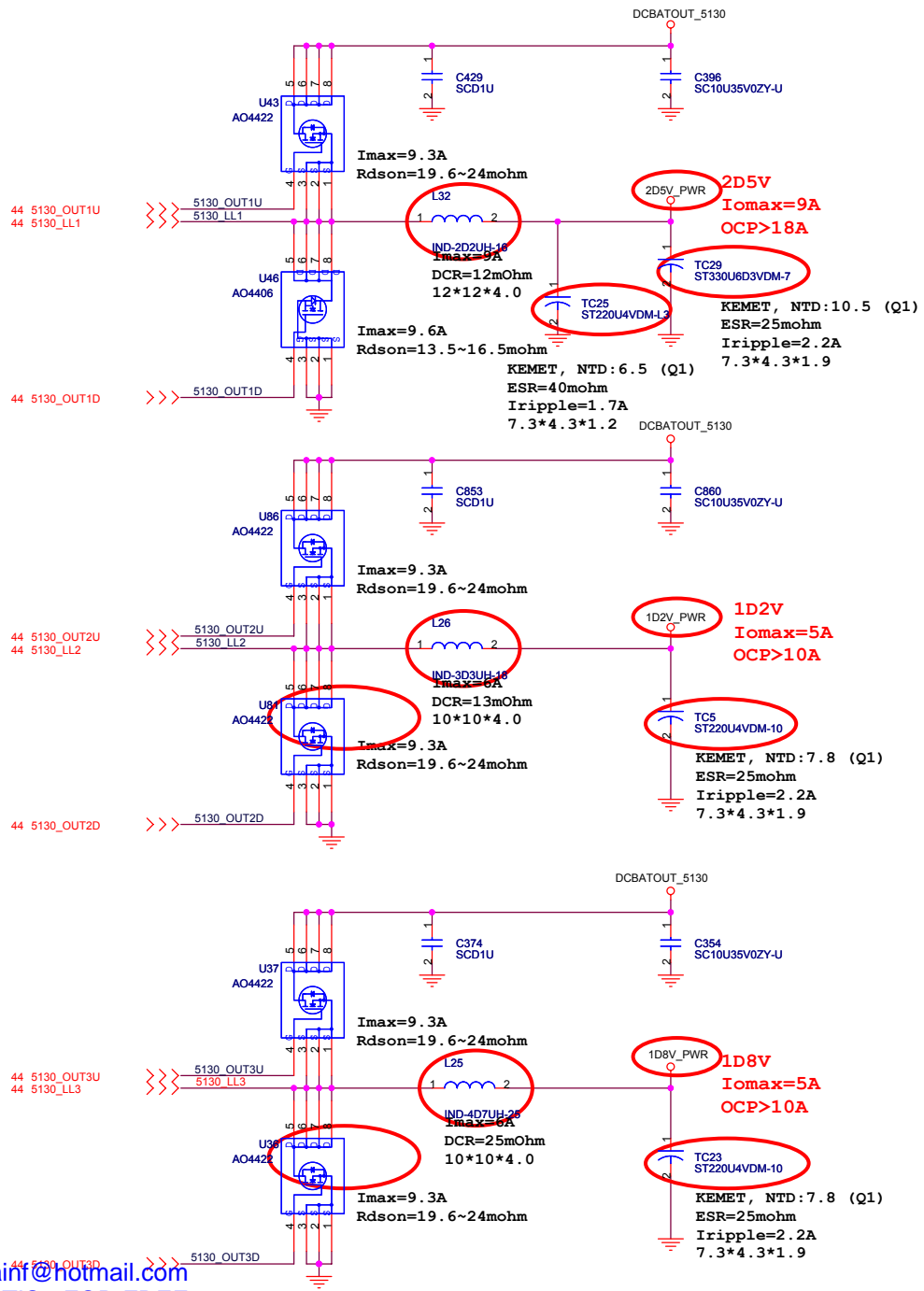
Title: **TI TPS5130 2D5V/1D2V/1D8V (1/2)**

Size: A3 Document Number: **SNIP** Rev: **SA**

Date: Thursday, November 18, 2004 Sheet 44 of 56

# TI TPS5130 for 2D5V, 1D2V, 1D8V

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

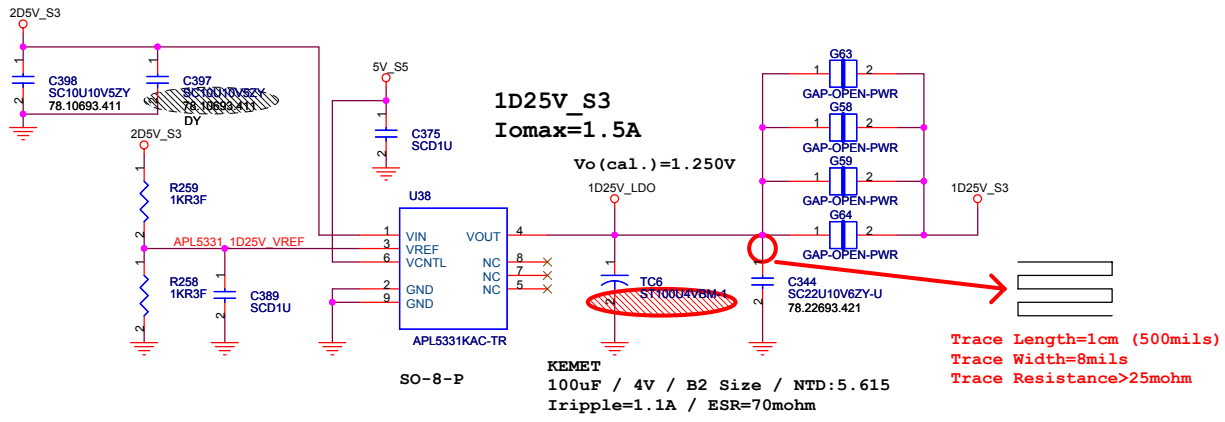
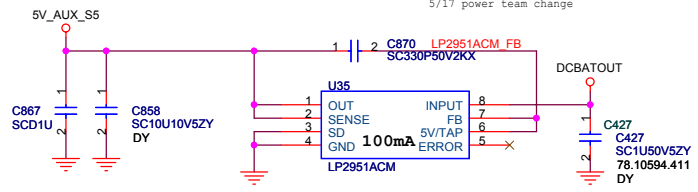


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<b>TI TPS5130 2D5V/1D2V/1D8V (2/2)</b>	
File	Rev SA
Size A3	Document Number
<b>SNIFE</b>	
Date: Thursday, November 18, 2004	Sheet 45 of 56

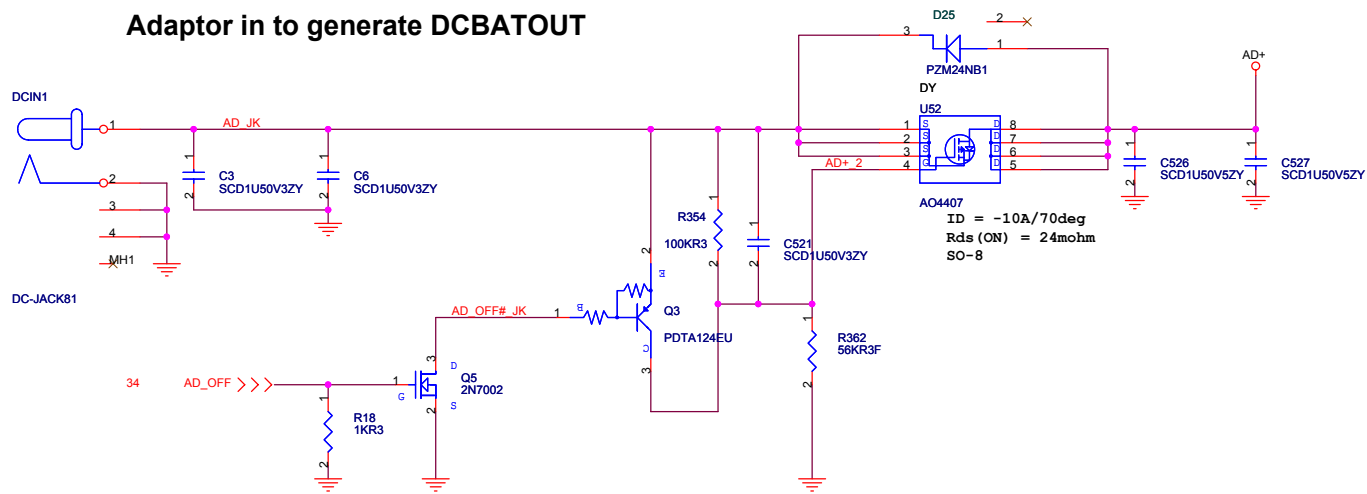
### 5V\_AUX\_S5

5/17 power team change

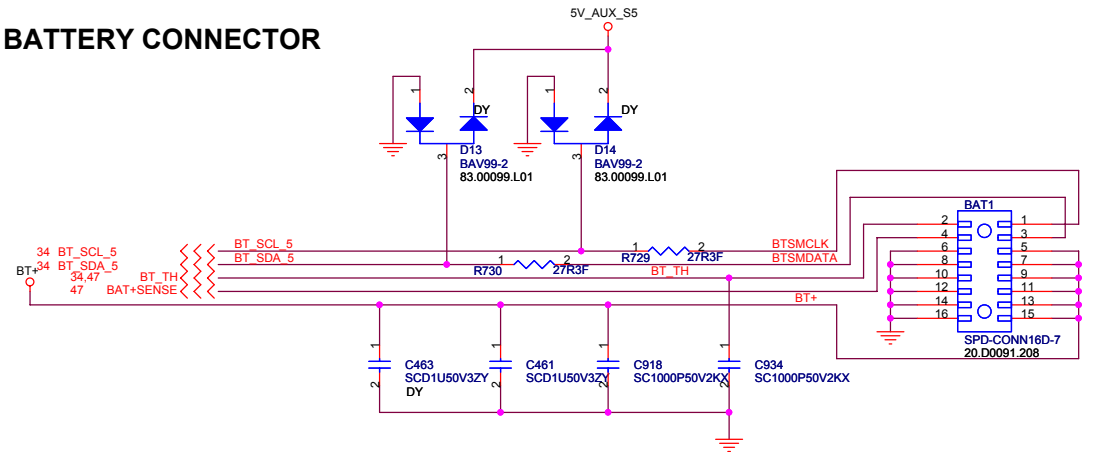




### Adaptor in to generate DCBATOUT



### BATTERY CONNECTOR

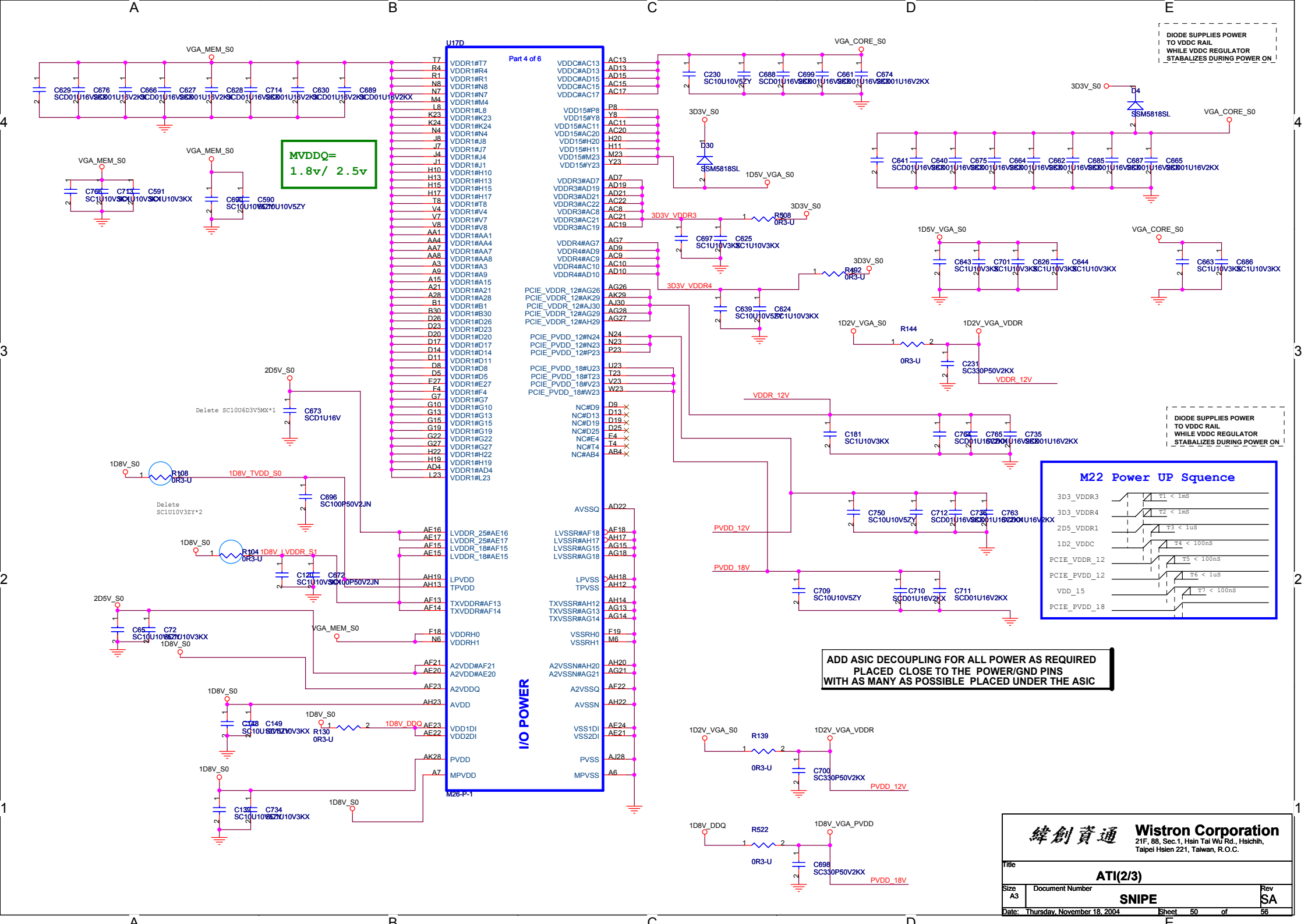


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Taipei Hsien 221, Taiwan, R.O.C.

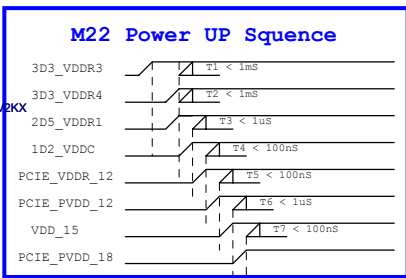
Title		DC/DC (1/2) -- 5V / 3.3V / 2.5V	
Size	Document Number	Rev	
A3	SNIFE	SA	
Date: Thursday, November 18, 2004	Sheet 48	of 56	







MVDDQ =  
1.8v / 2.5v



ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED  
PLACED CLOSE TO THE POWER/GND PINS  
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

DIODE SUPPLIES POWER  
TO VDDC RAIL  
WHILE VDDC REGULATOR  
STABILIZES DURING POWER ON

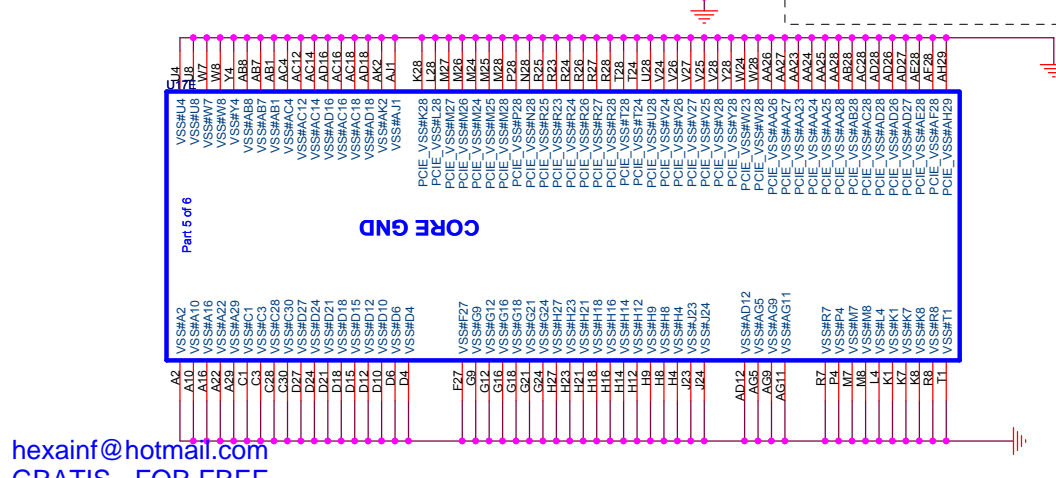
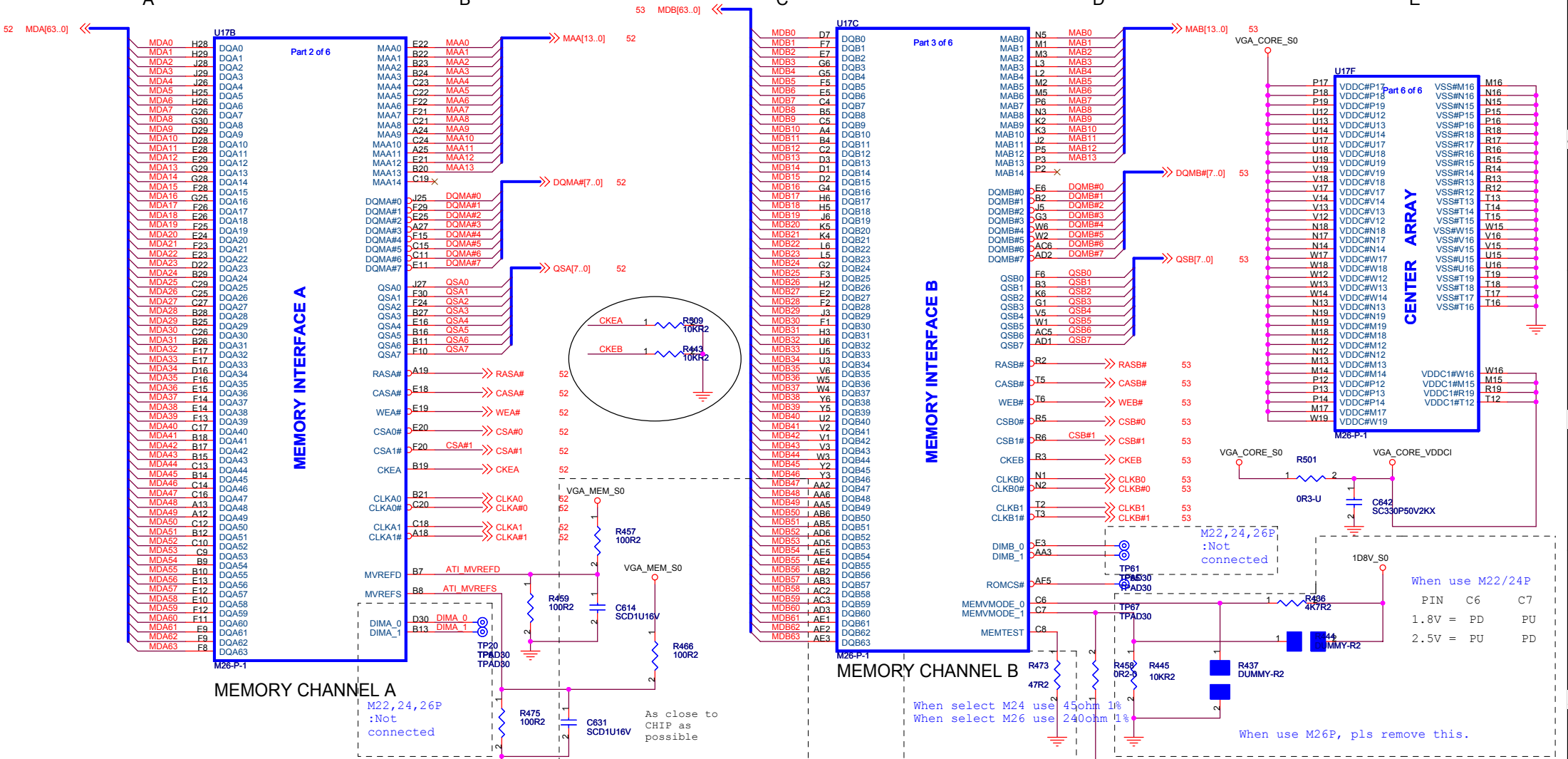
DIODE SUPPLIES POWER  
TO VDDQ RAIL  
WHILE VDDQ REGULATOR  
STABILIZES DURING POWER ON

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI(2/3)**

Size: A3 Document Number: **SNIFE** Rev: SA

Date: Thursday, November 18, 2004 Sheet 50 of 56



**MVDDQ=**  
1.8v/ 2.5v

	VDDR1	MEMMODE_0	MEMMODE_1
1.8V		GND	+VDDC_CT
2.5V		+VDDC_CT	GND
2.8V		+VDDC_CT	+VDDC_CT

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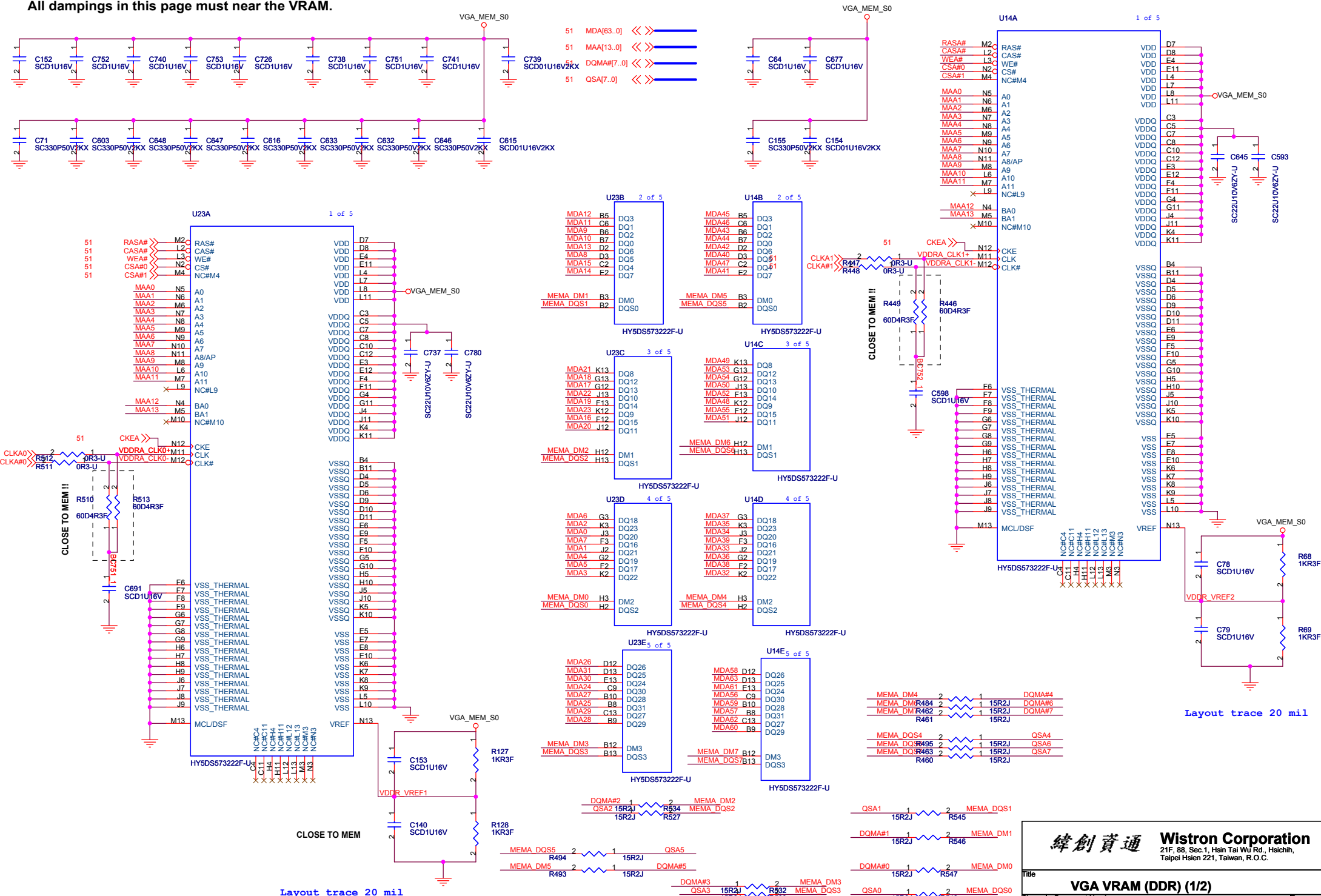
Title: **ATI(3 of 3)**

Size: A3 Document Number: **SNIFE** Rev: SA

Date: Thursday, November 18, 2004 Sheet 51 of 56

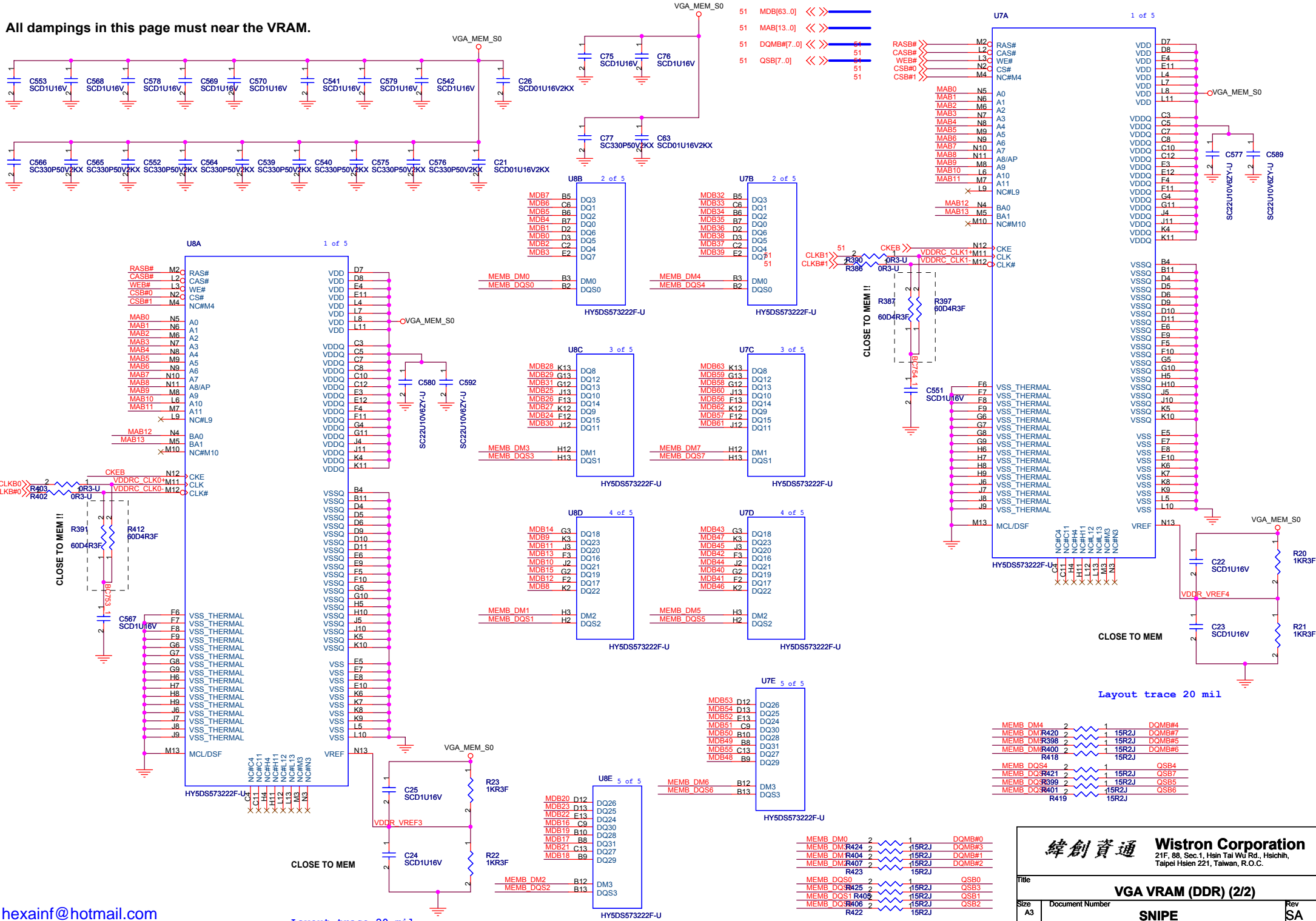
hexainf@hotmail.com  
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All dampings in this page must near the VRAM.



		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<b>Title</b> VGA VRAM (DDR) (1/2)		
<b>Size</b> A3	<b>Document Number</b>	<b>Rev</b> SA
<b>SNIE</b>		
<b>Date:</b> Thursday, November 18, 2004		
Sheet 52 of 56		

All dampings in this page must near the VRAM.



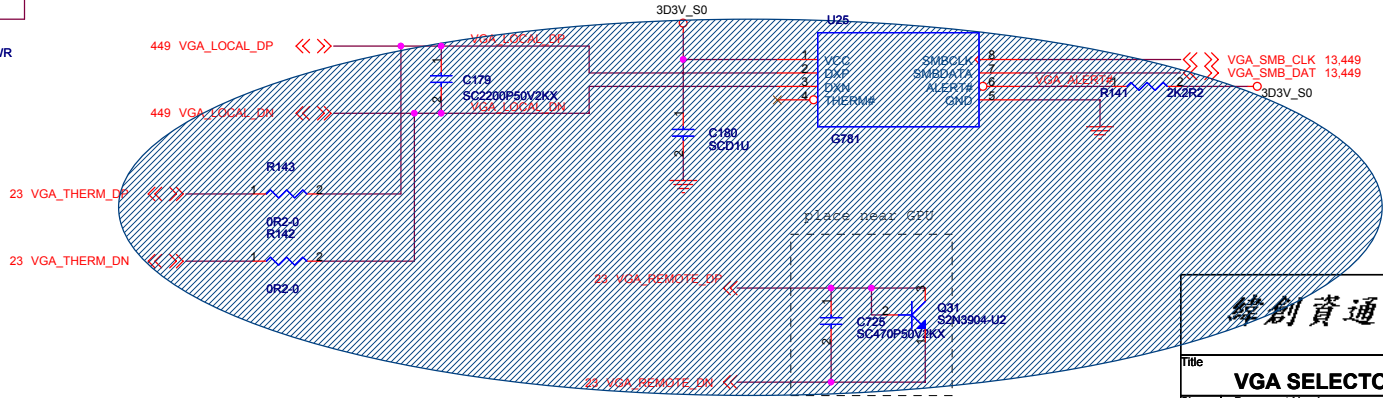
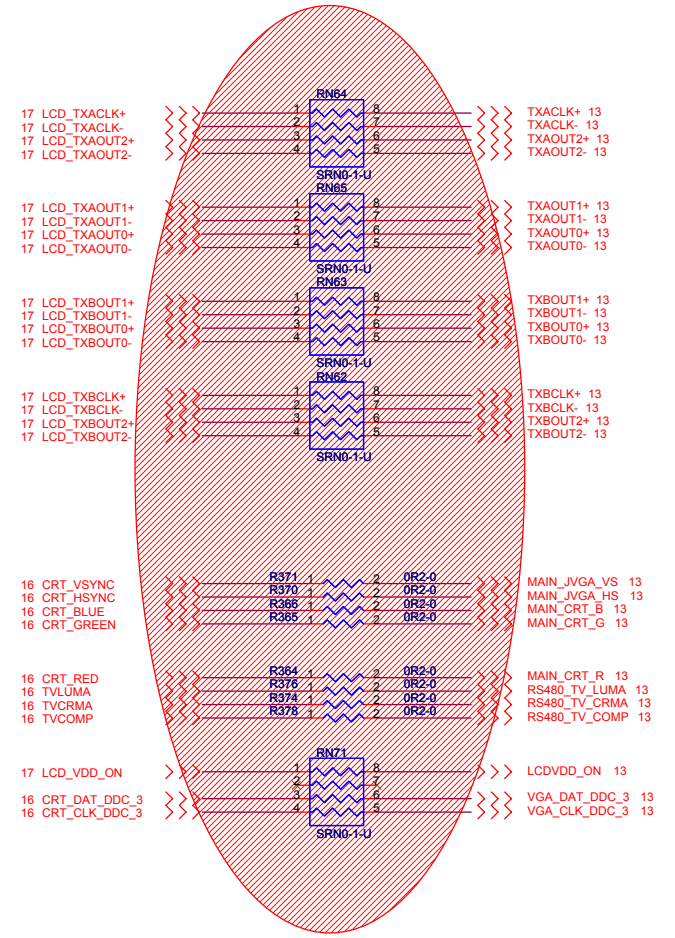
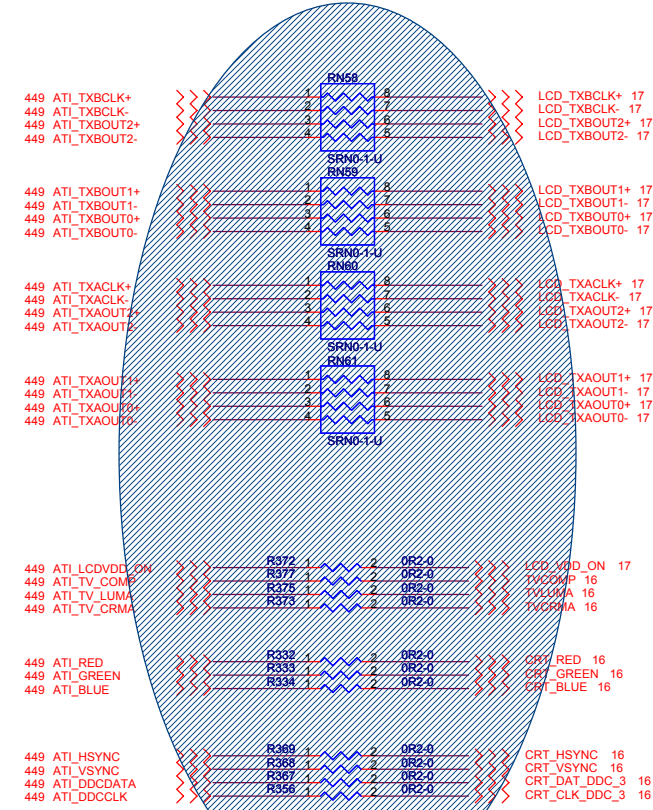
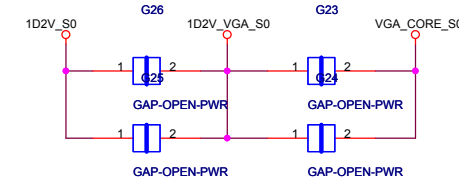
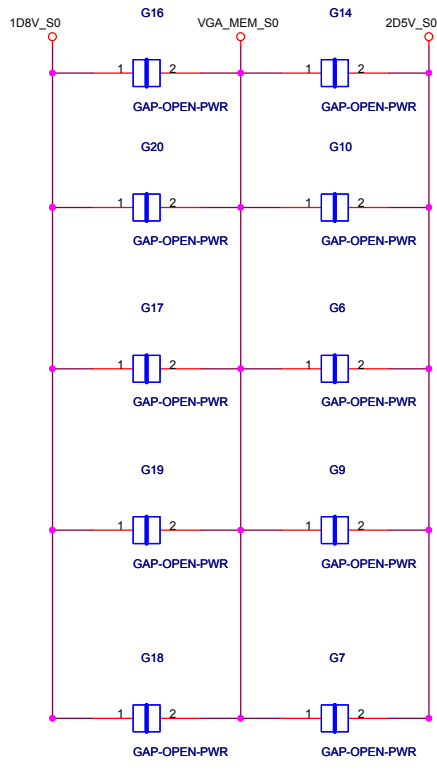
Layout trace 20 mil


MEMB DM4	2	1	DOMB#4
MEMB DM#R420	2	1	DOMB#7
MEMB DM#R398	2	1	DOMB#5
MEMB DM#R400	2	1	DOMB#6
			R418 15R2J
MEMB DQS4	2	1	QSB4
MEMB DQ#R421	2	1	QSB3
MEMB DQ#R399	2	1	QSB1
MEMB DQ#R401	2	1	QSB6
			R419 15R2J

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Title	
<b>VGA VRAM (DDR) (2/2)</b>	
Size	Document Number
A3	SNIE
Rev	SA
Date: Thursday, November 18, 2004	Sheet 53 of 56

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Layout trace 20 mil

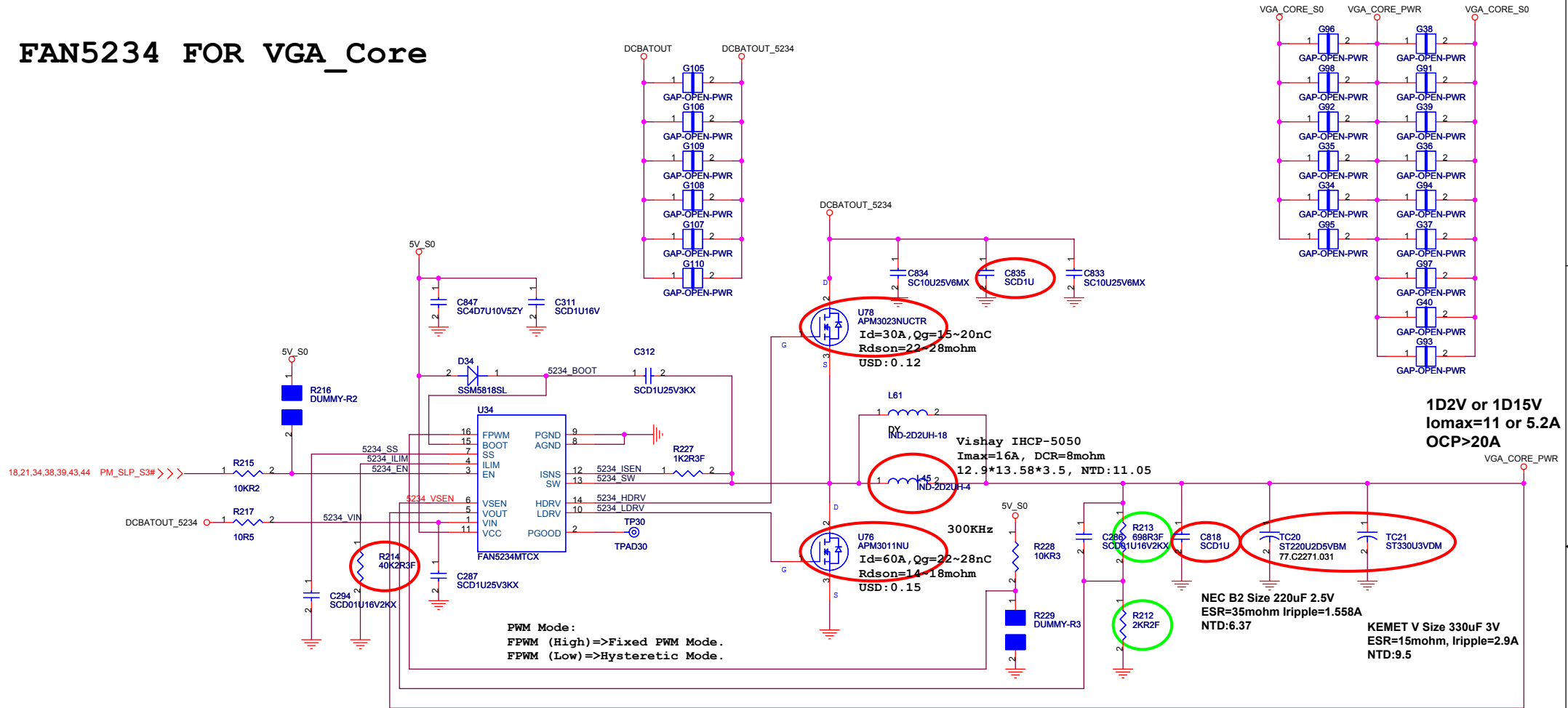



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 Taipei Hsien 221, Taiwan, R.O.C.

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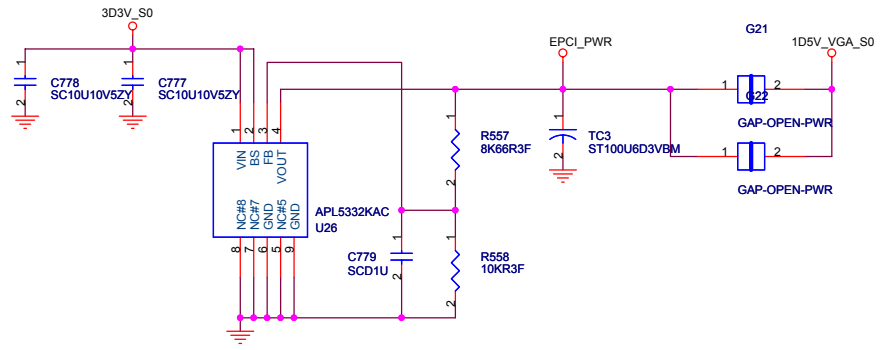
Title: **VGA SELECTOR**  
 Size: A3  
 Document Number: **SNIFE**  
 Date: Thursday, November 18, 2004  
 Sheet: 54 of 56

# FAN5234 FOR VGA\_Core

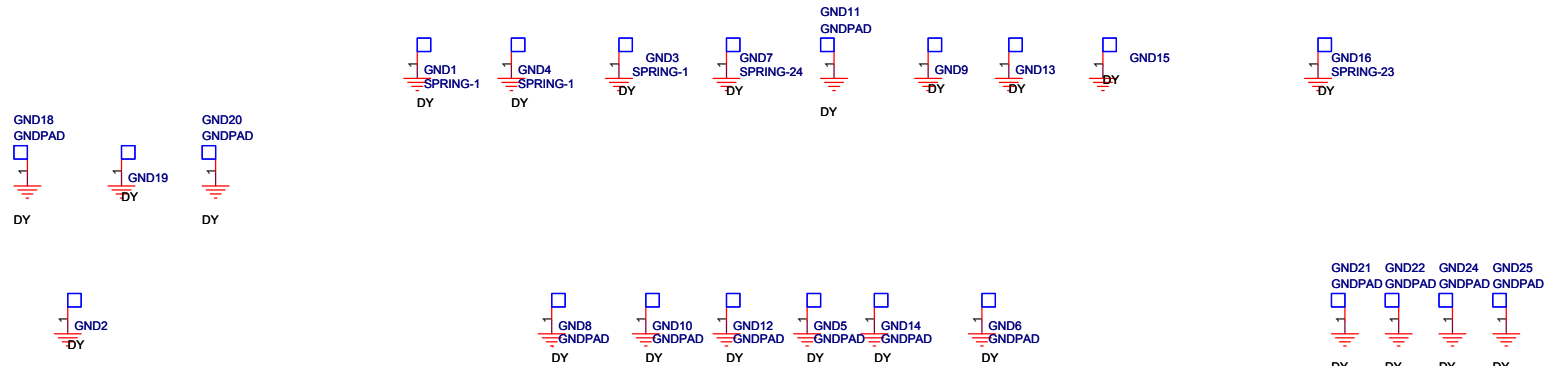
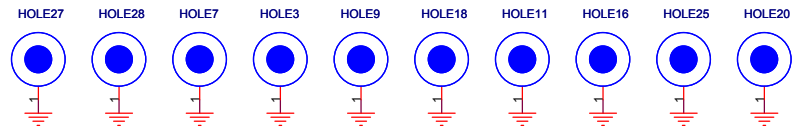
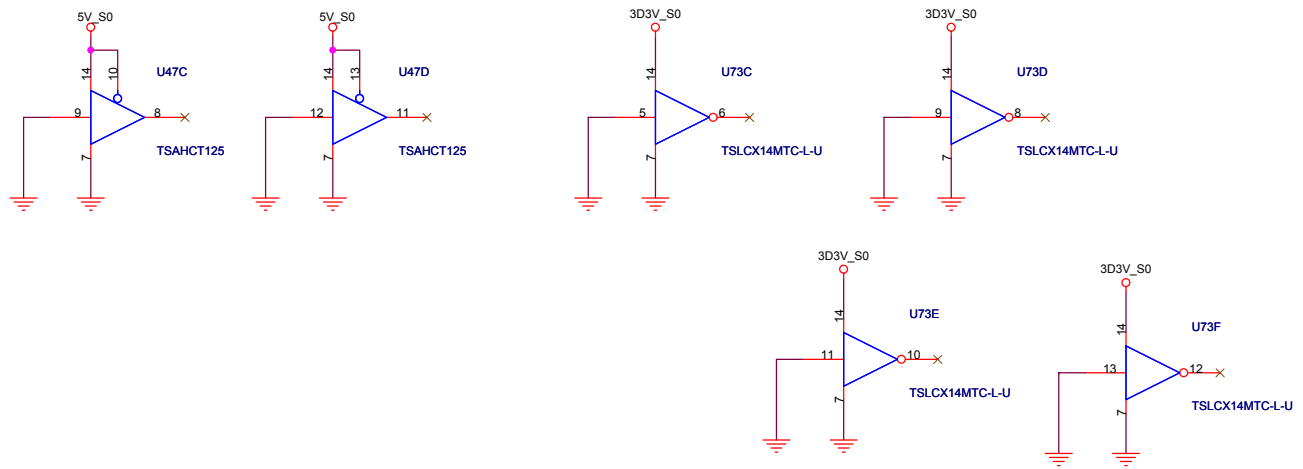
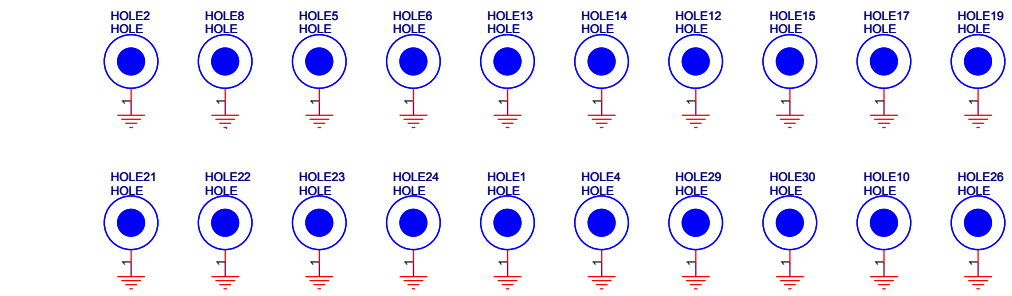
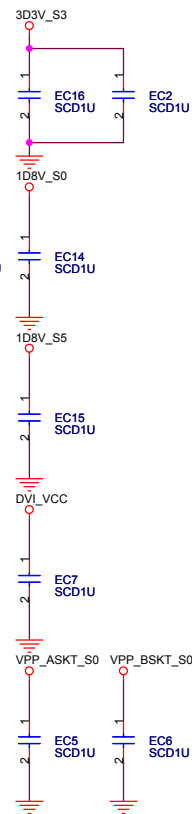
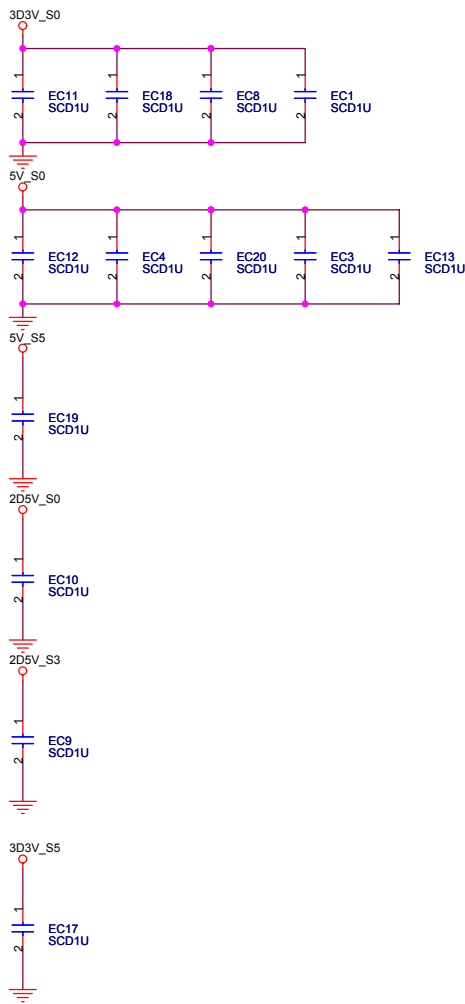


$$R_{ilim} = (11.2 / I_{ilim}) * ((100 + R_{sense}) / R_{dson})$$

$$V_o = 1.20V, R_{1775} = 0.698K\Omega (R_{3F}) \Rightarrow V_o (cal.) = 1.2141V \quad \text{for M26 \& M22}$$



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