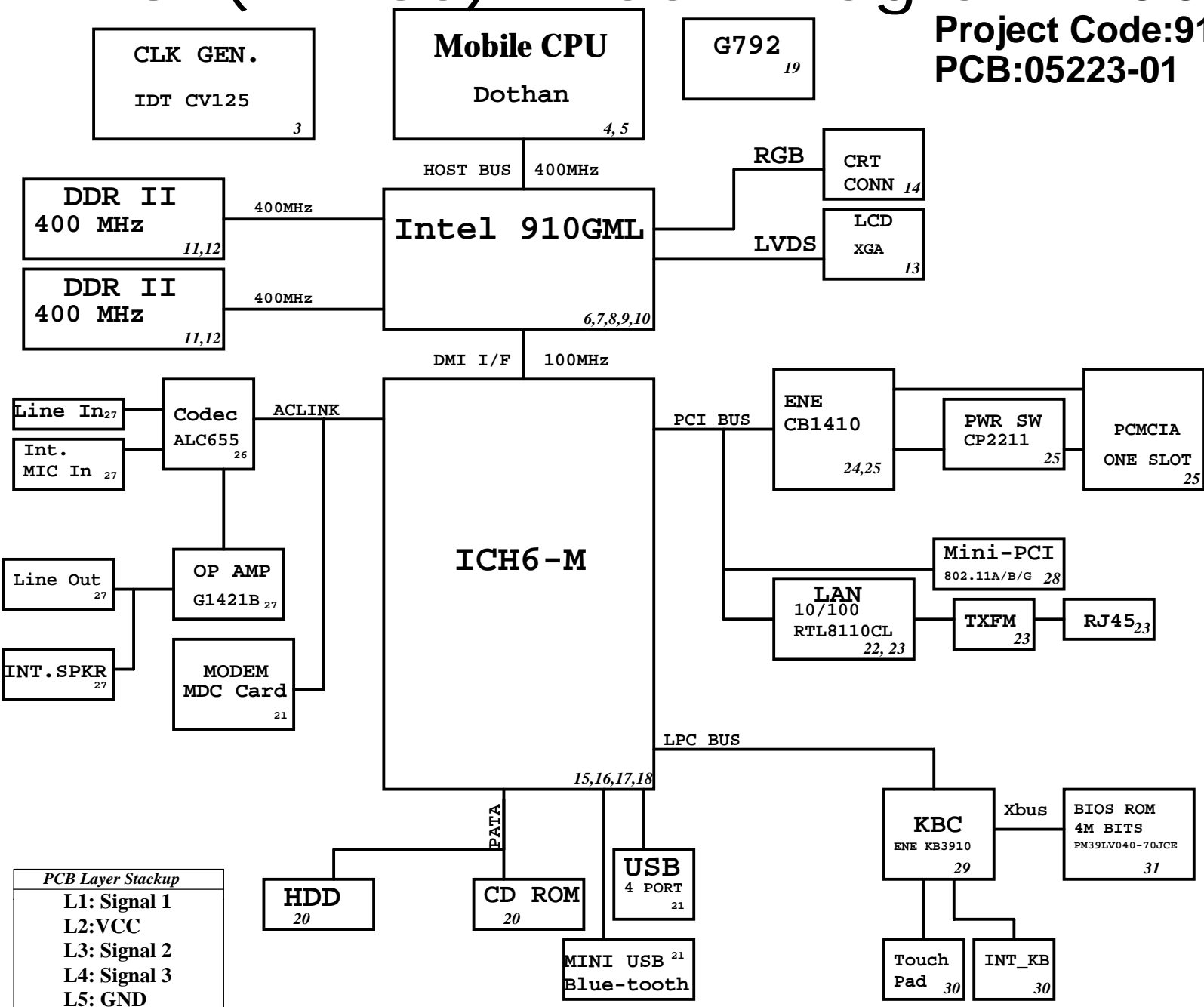


AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001
PCB:05223-01



PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Signal 2
- L4: Signal 3
- L5: GND
- L6: Signal 4

CPU DC/DC
ISL6218CV-T 34

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844-1.3V 27A

SYSTEM DC/DC
TPS51120 35

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC
APL5308-25AC 36

INPUTS	OUTPUTS
5V_S5	1D5V_S0
3D3V_S0	2D5V_S0

SYSTEM DC/DC
ISL6227 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DQ 37

INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER
ISL6255 38

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
Custom	AG1(Alviso)	01

Date: Tuesday, November 01, 2005 Sheet 1 of 40

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH FWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

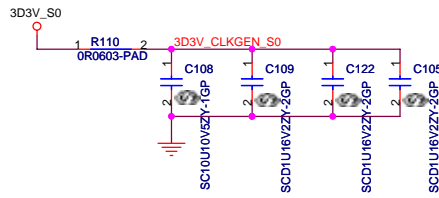
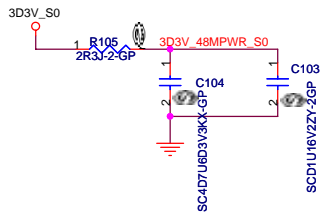
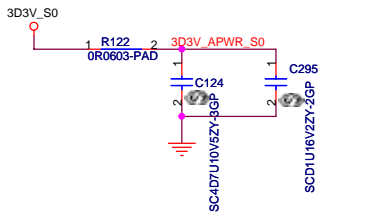
ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

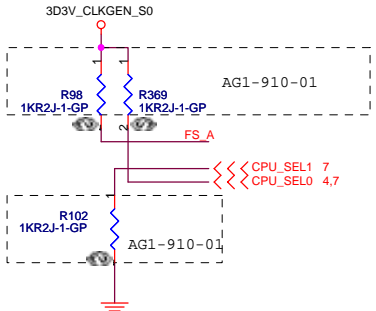
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

<Core Design>

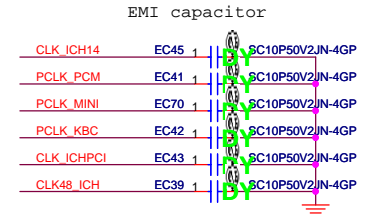
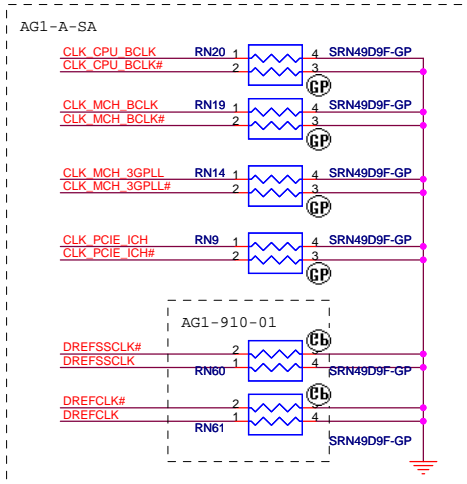
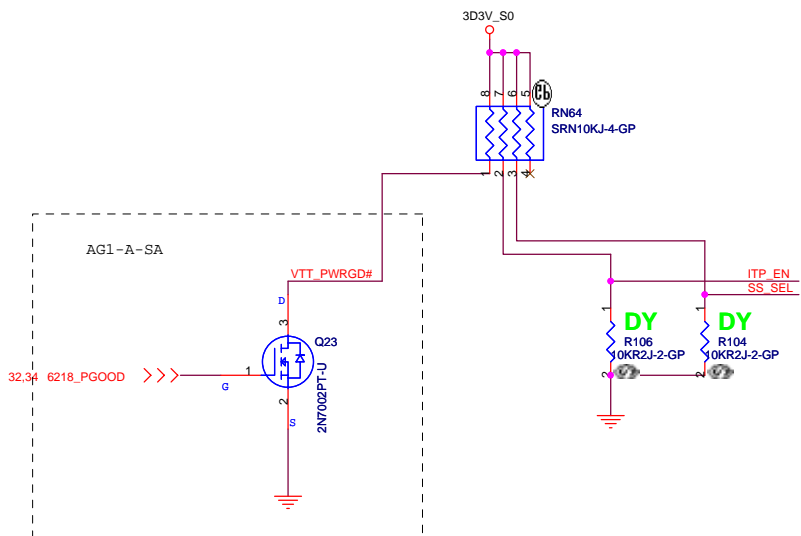
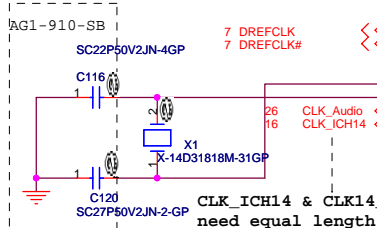
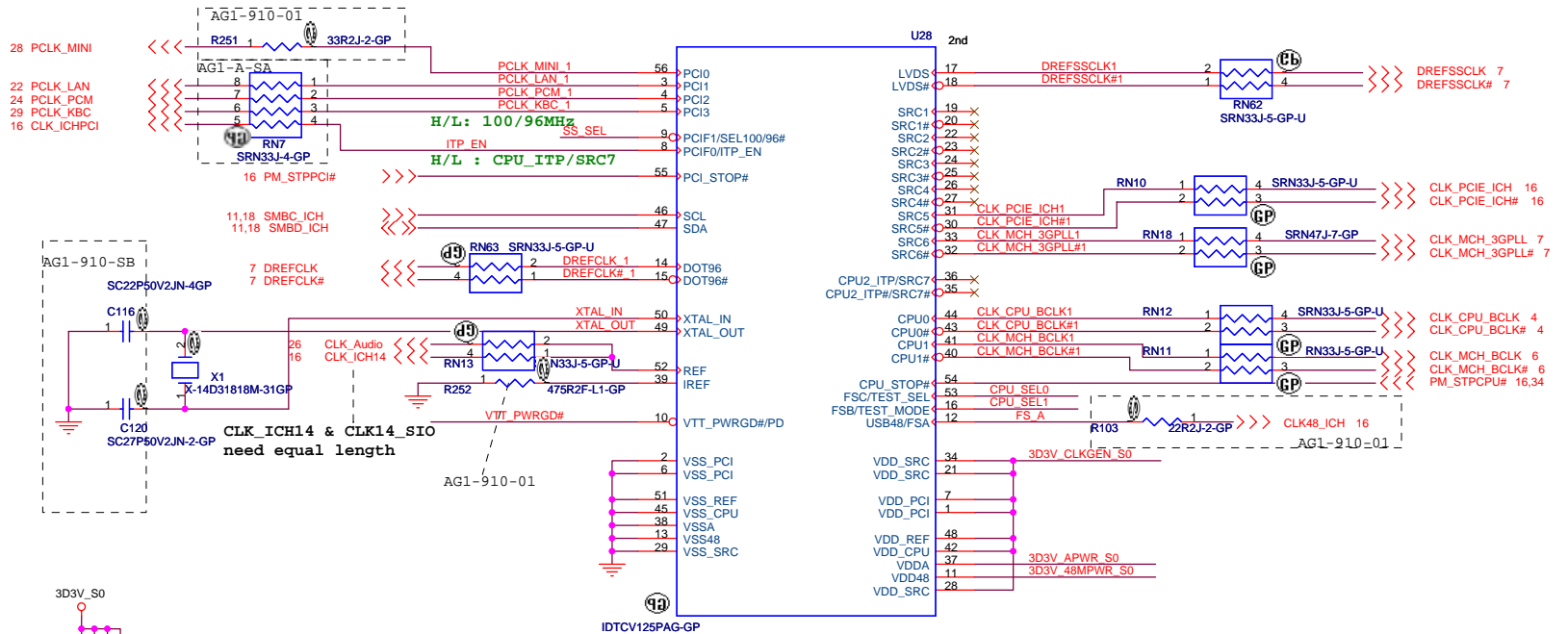
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Memo			
Size A3	Document Number AG1(Alviso)	Rev 01	
Date: Tuesday, November 01, 2005		Sheet 2	of 40



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	H1 - Z

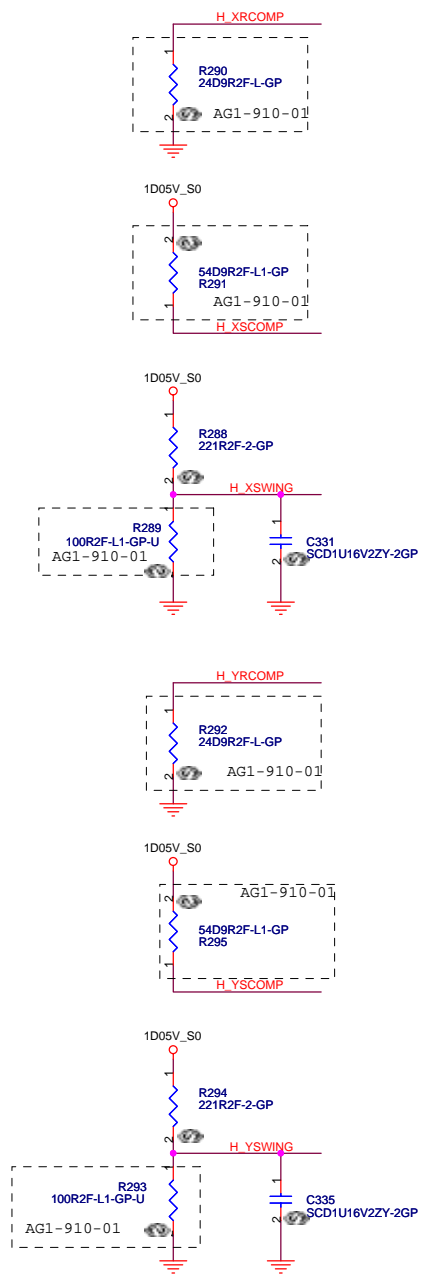


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



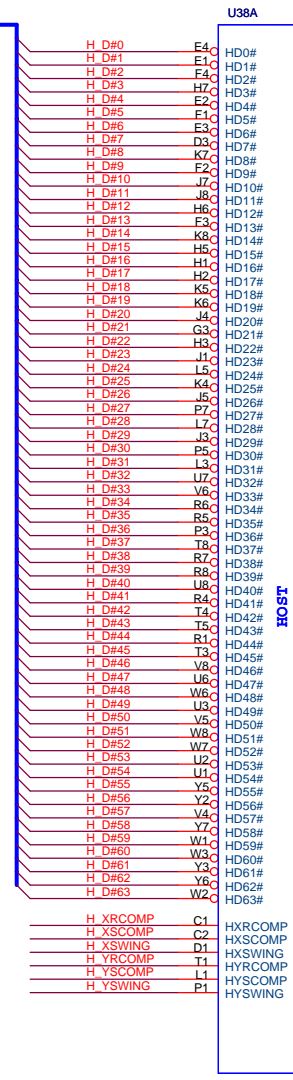
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Clock Generator - IDT125		
Title		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date:	Friday, October 28, 2005	Sheet 3 of 40



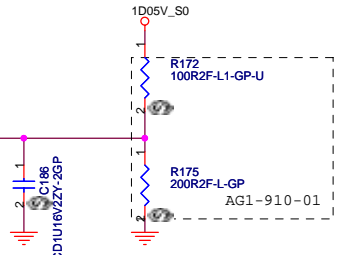
Place them near to the chip

4 H_D#[63.0]



71.0GMCH.08U

4 H_A#[31.3]



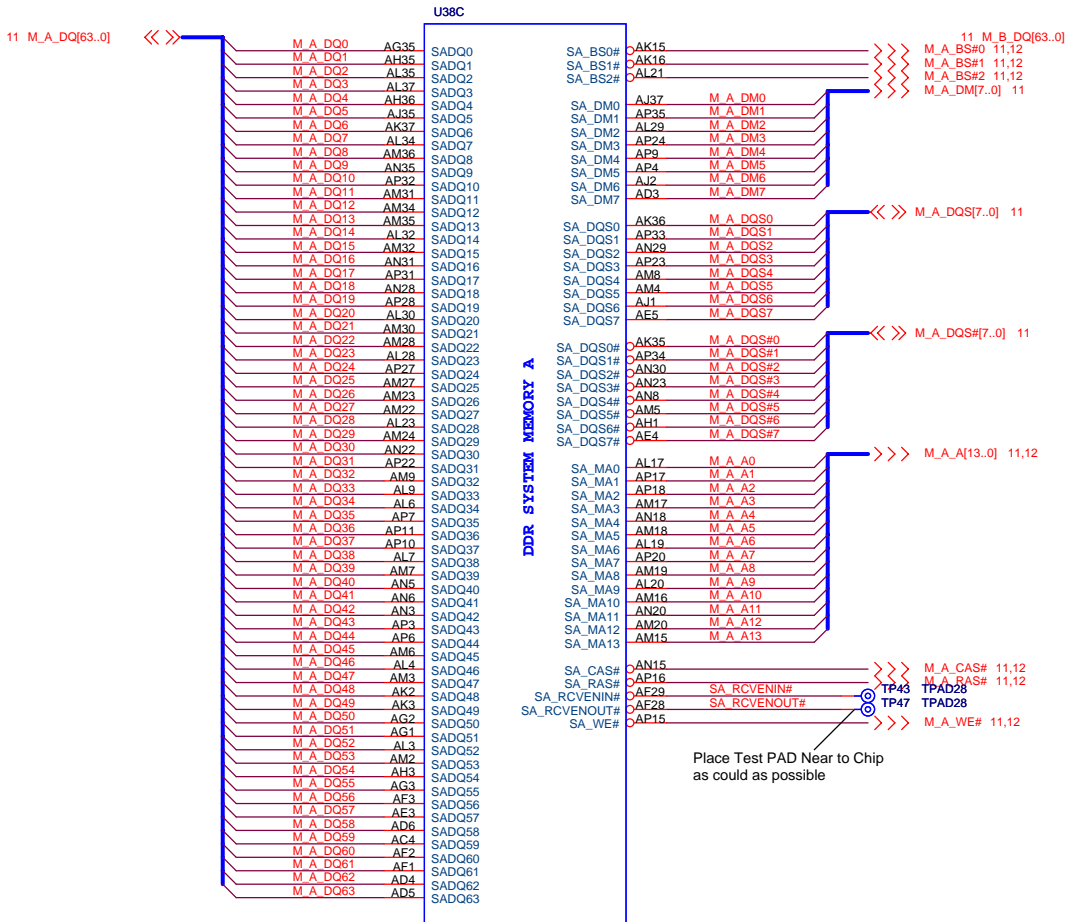
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

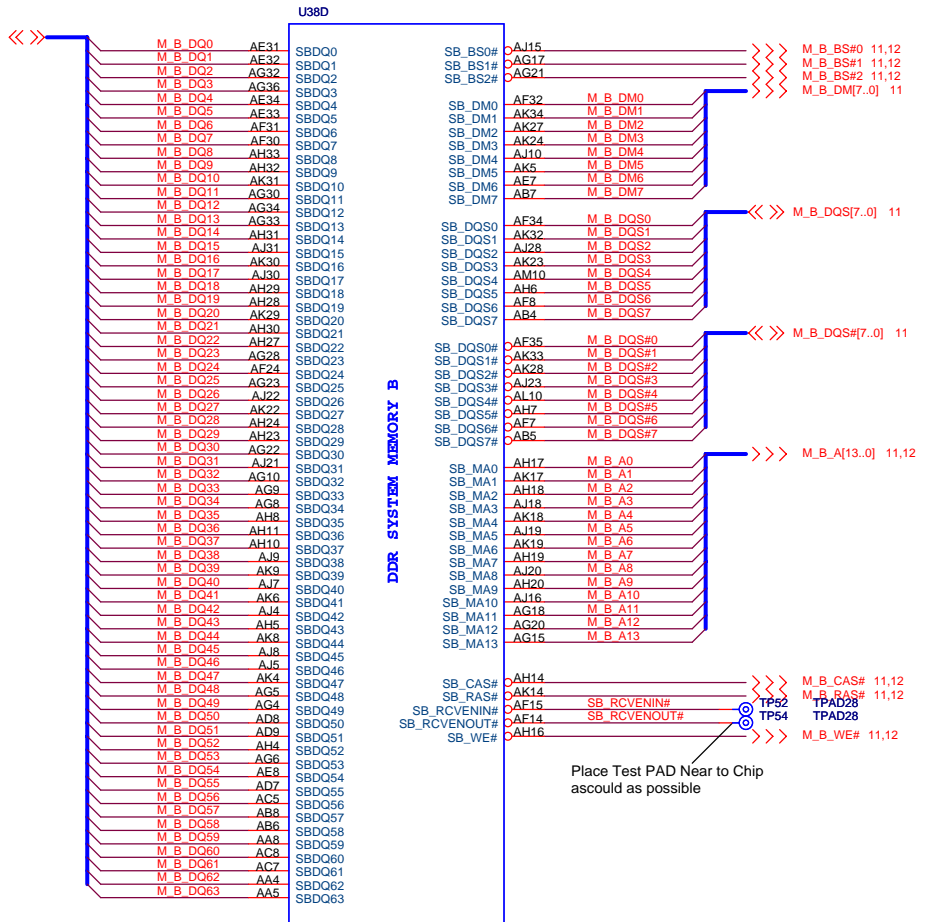
Title: **GMCH (1 of 5)**

Size A3 Document Number **AG1(Alviso)** Rev **01**

Date: Tuesday, October 25, 2005 Sheet 6 of 40



71.0GMCH.08U



71.0GMCH.08U

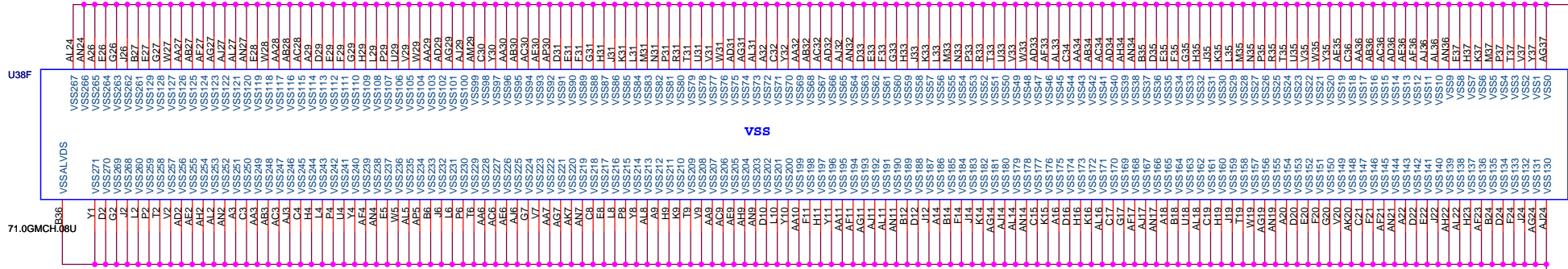
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

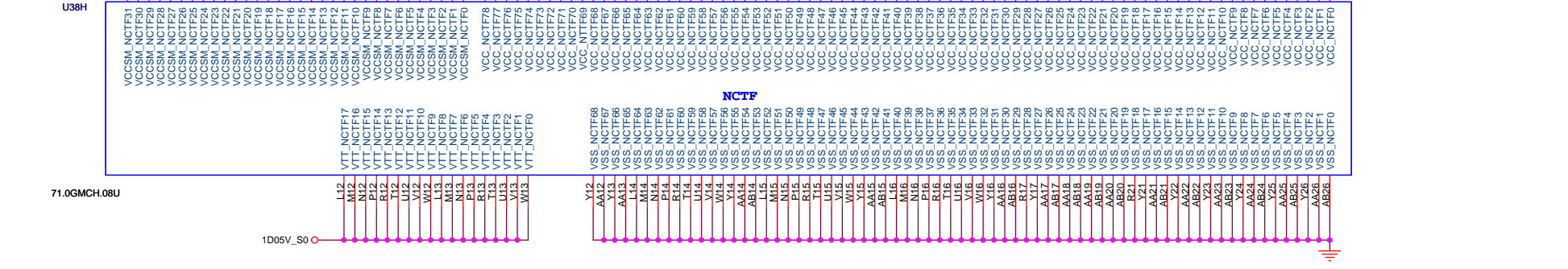
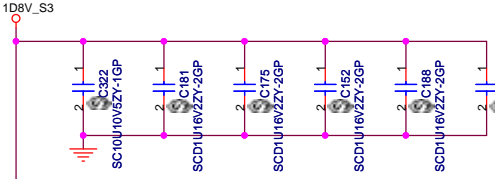
Title: **GMCH (3 of 5)**

Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

Date: Monday, October 17, 2005 Sheet: 8 of 40



Place these Hi-Freq decoupling caps near GMCH



Place these Hi-Freq decoupling caps near GMCH



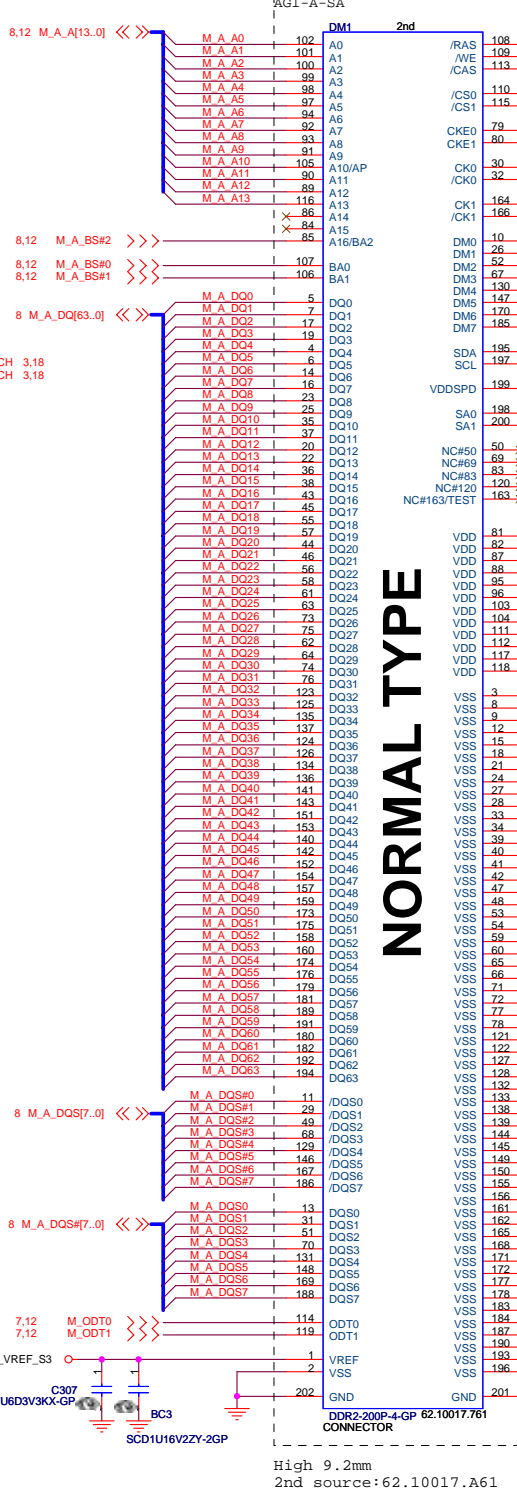
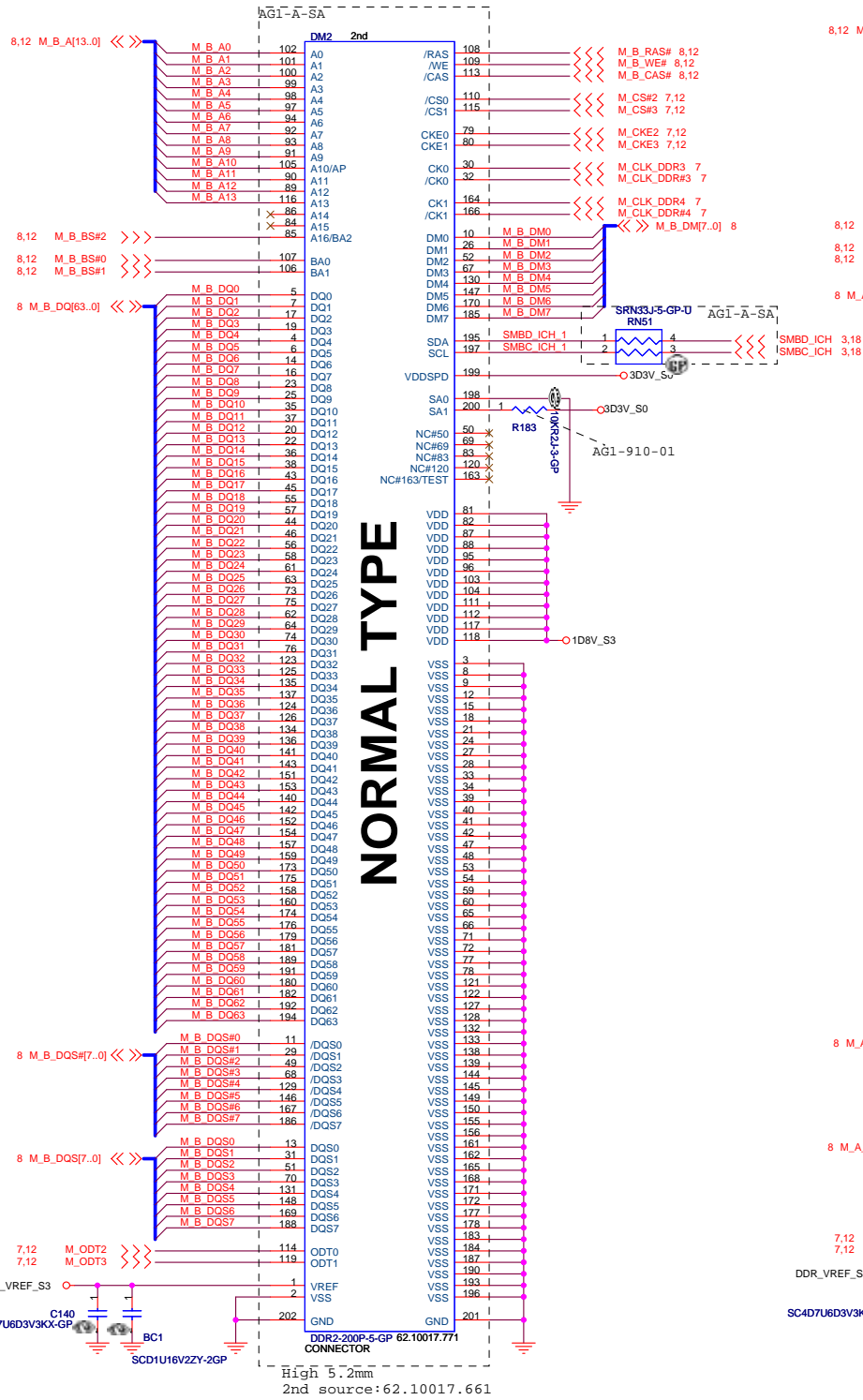
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (5 of 5)**

Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

Date: Monday, October 17, 2005 Sheet: 10 of 40



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

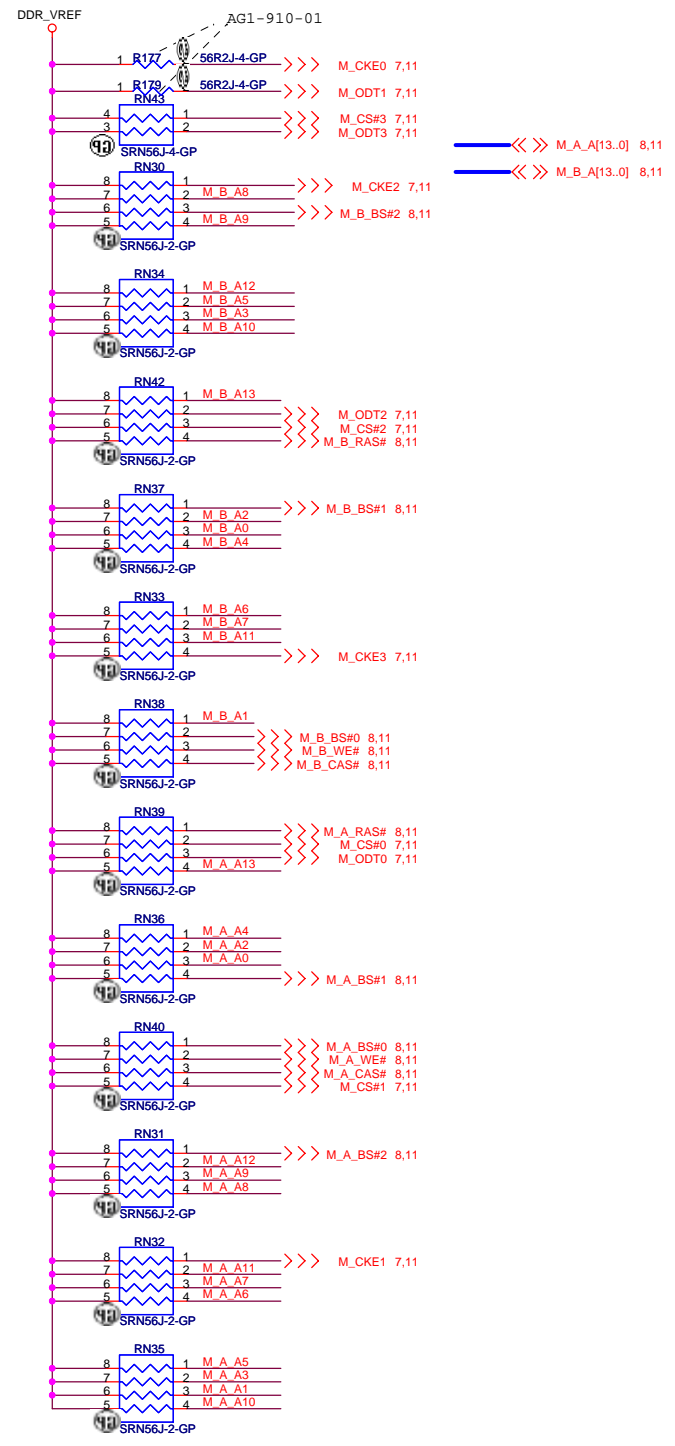
Title: **DDR Socket**

Size	Document Number	Rev
Custom	AG1(Alviso)	01

Date: Tuesday, October 25, 2005 Sheet 11 of 40

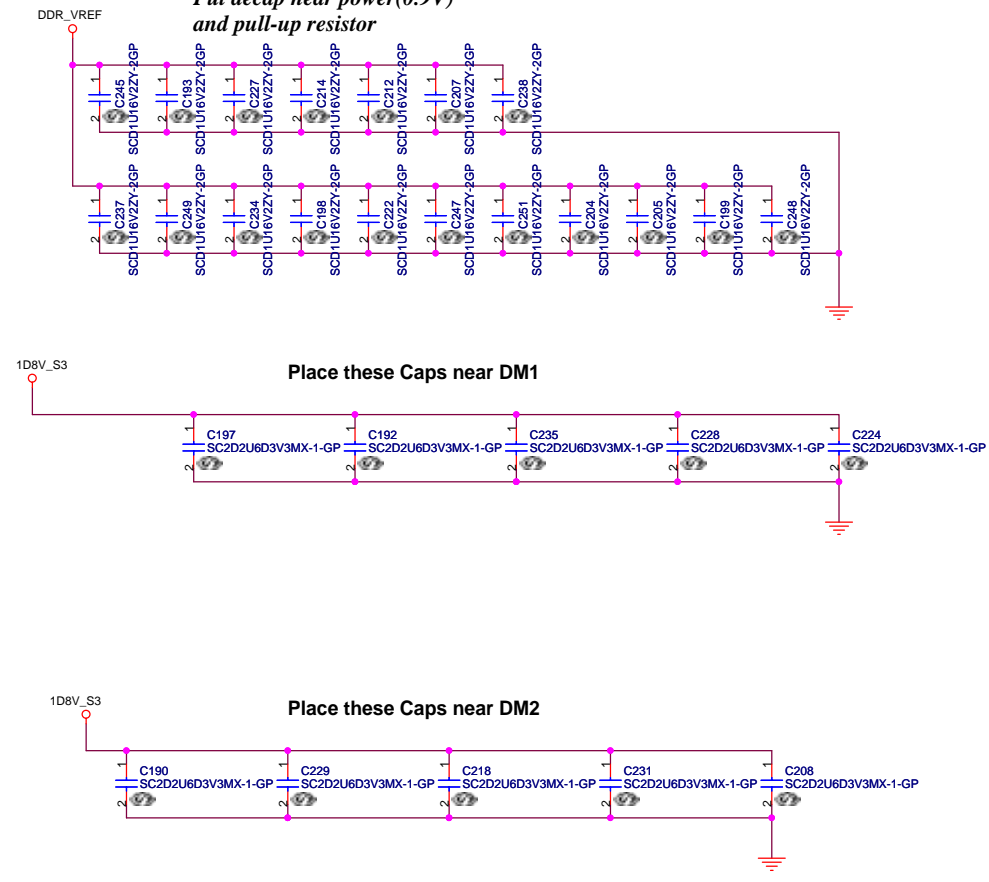
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



<Core Design>

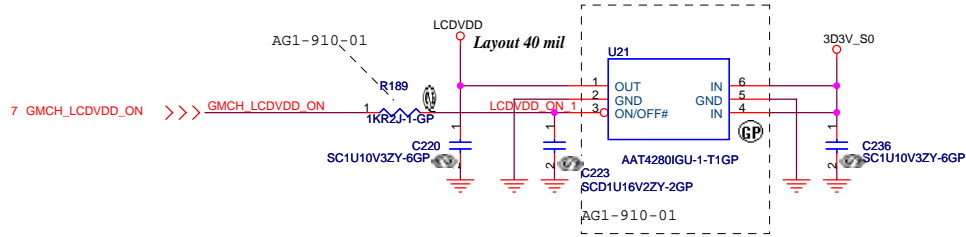
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Termination Resistor**

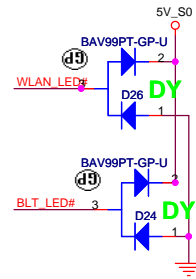
Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

Date: Tuesday, October 25, 2005 Sheet 12 of 40

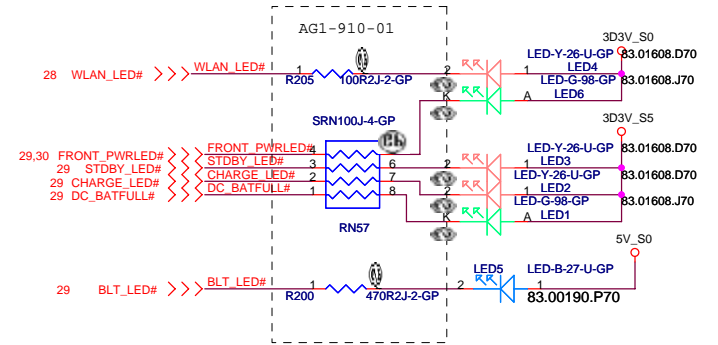
LED



LCD/INVERTER/CCD CONN



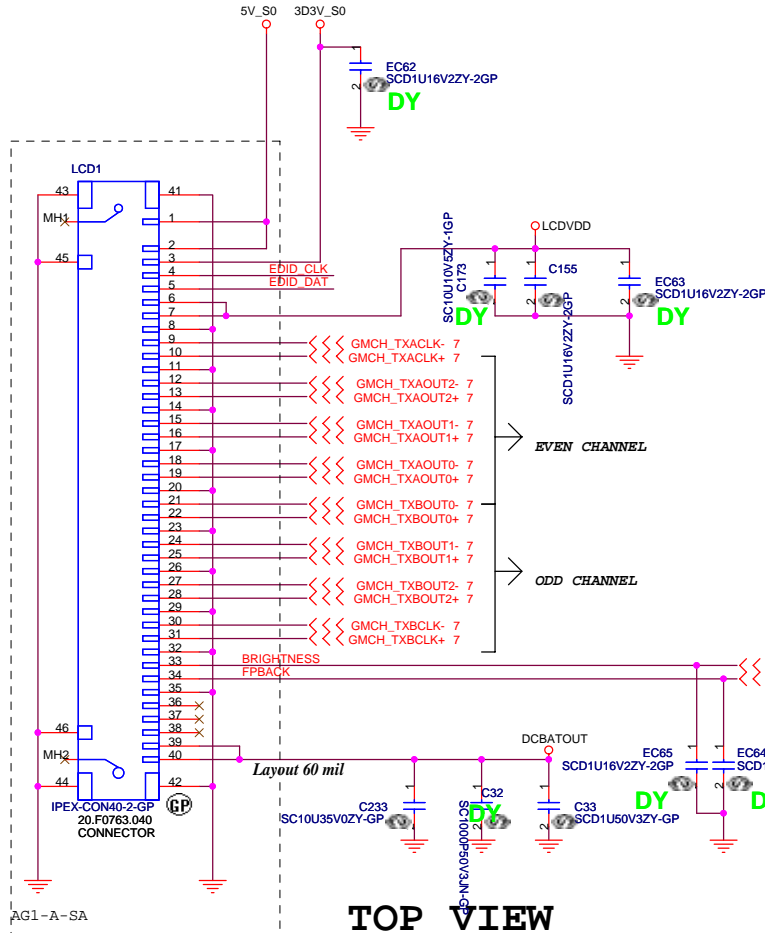
LED BD CONN



Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

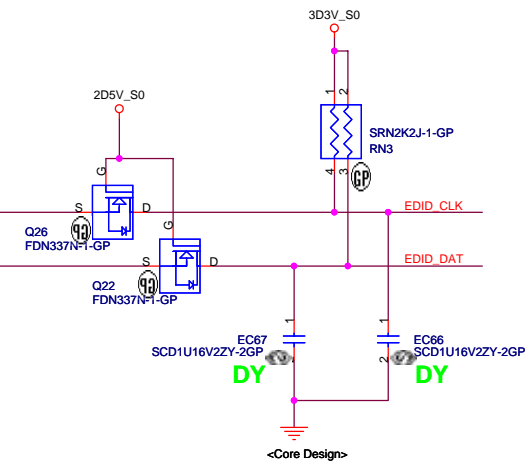
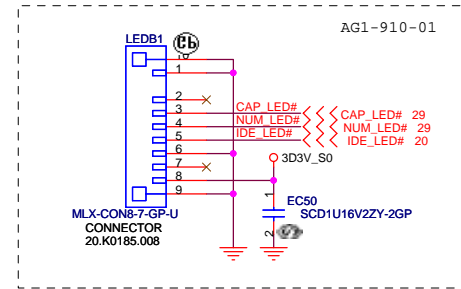
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND



TOP VIEW

LCD

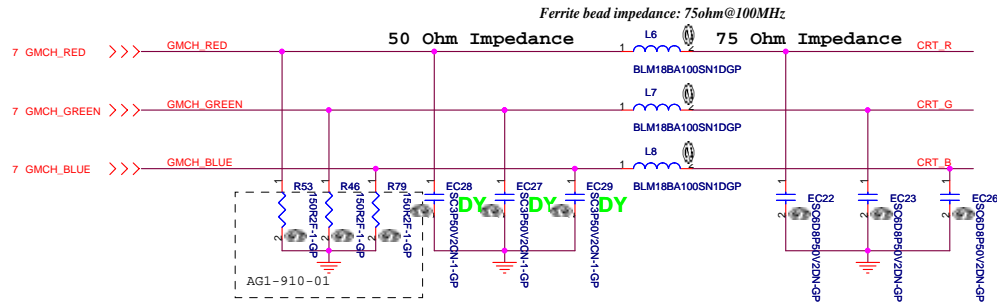


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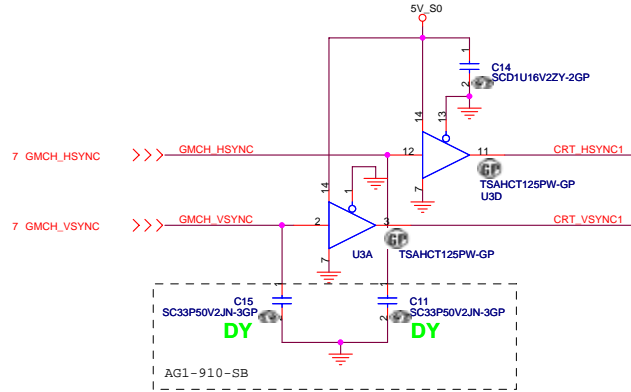
緯創資通 Wistron Corporation
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Title		
LCD CONN & LED		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date:	Friday, October 28, 2005	Sheet 13 of 40

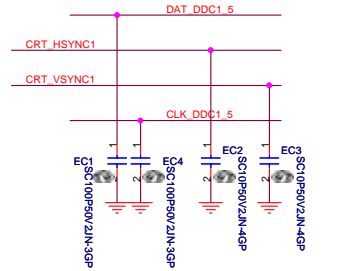
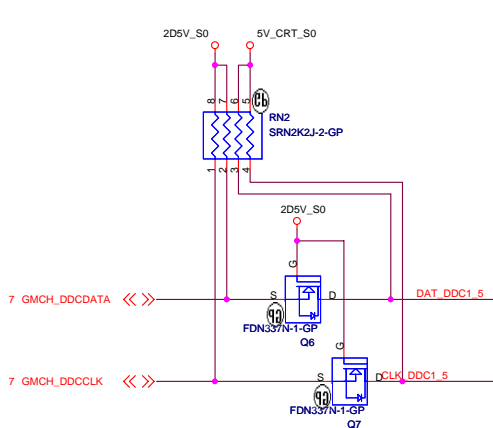
CRT CONNECTOR



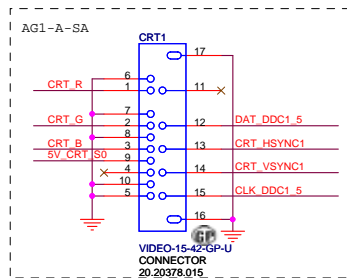
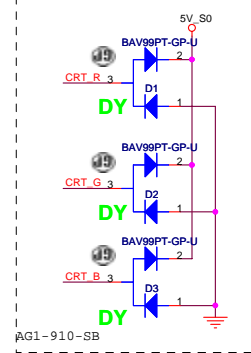
Hsync & Vsync level shift



DDC_CLK & DATA level shift

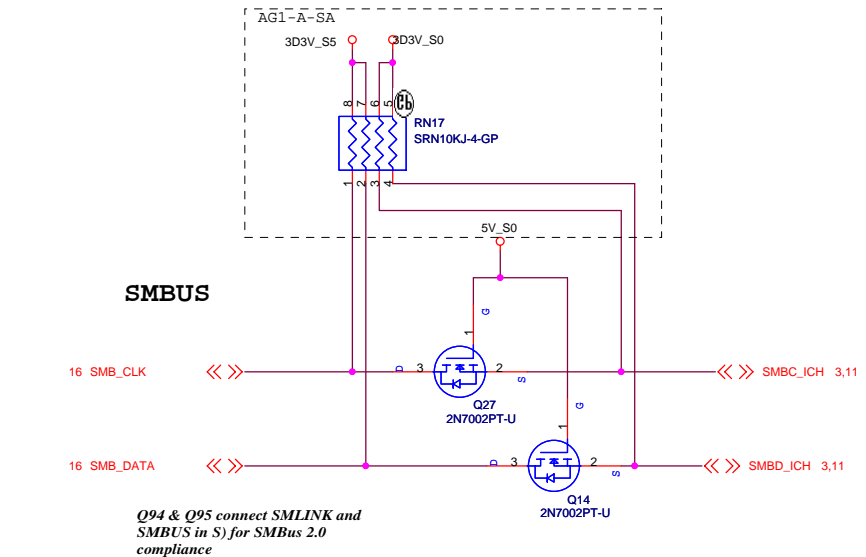
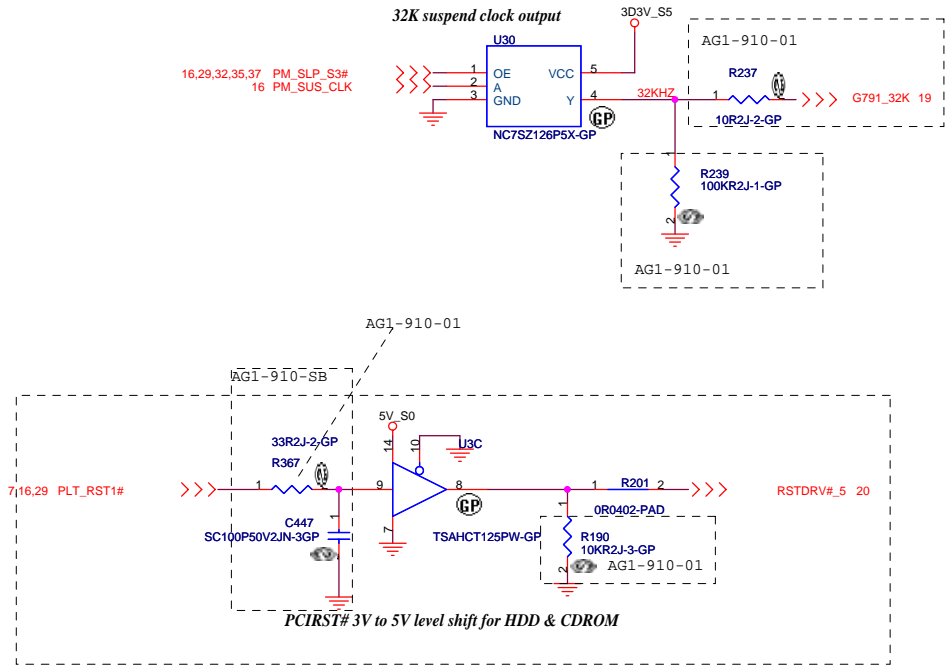


ESD Protection Diode



<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CRT Connector		
Size	Document Number	Rev
Custom	AG1(Alviso)	01
Date:	Friday, October 28, 2005	Sheet 14 of 40



U26D

E27	VSS	F4
Y6	VSS	F22
Y27	VSS	F19
Y26	VSS	F17
Y23	VSS	F25
W7	VSS	E19
W25	VSS	E18
W24	VSS	E15
W23	VSS	E14
W1	VSS	D7
V4	VSS	D22
V27	VSS	D18
V26	VSS	D18
V23	VSS	D14
U25	VSS	D13
U24	VSS	D10
U23	VSS	D1
U15	VSS	C4
U13	VSS	C22
T7	VSS	C20
T27	VSS	C18
T26	VSS	C14
T23	VSS	B25
T16	VSS	B24
T15	VSS	B23
T14	VSS	B21
T13	VSS	B19
T12	VSS	B15
T1	VSS	B13
R4	VSS	AG7
R25	VSS	AG3
R24	VSS	AG22
R23	VSS	AG20
R17	VSS	AG17
R16	VSS	AG14
R15	VSS	AG12
R14	VSS	AG1
R13	VSS	AF7
R12	VSS	AF3
R11	VSS	AF26
P22	VSS	AF12
P16	VSS	AF10
P15	VSS	AF1
P14	VSS	AE7
P13	VSS	AE6
P12	VSS	AE25
N7	VSS	AE21
N17	VSS	AE2
N16	VSS	AE12
N15	VSS	AE11
N14	VSS	AE10
N13	VSS	AD6
N12	VSS	AD24
N11	VSS	AD2
N1	VSS	AD18
M4	VSS	AD15
M27	VSS	AD10
M26	VSS	AD1
M23	VSS	AC6
M16	VSS	AC3
M15	VSS	AC26
M14	VSS	AC24
M13	VSS	AC23
M12	VSS	AC22
L25	VSS	AC12
L24	VSS	AC10
L23	VSS	AB9
L15	VSS	AB7
L13	VSS	AB2
K7	VSS	AB19
K27	VSS	AB10
K26	VSS	AB1
K23	VSS	AA4
K1	VSS	AA16
J4	VSS	AA13
J25	VSS	AA11
J24	VSS	A9
J23	VSS	A7
H27	VSS	A4
H26	VSS	A26
H23	VSS	A23
G9	VSS	A21
G7	VSS	A19
G21	VSS	A15
G12	VSS	A12
G1	VSS	A1

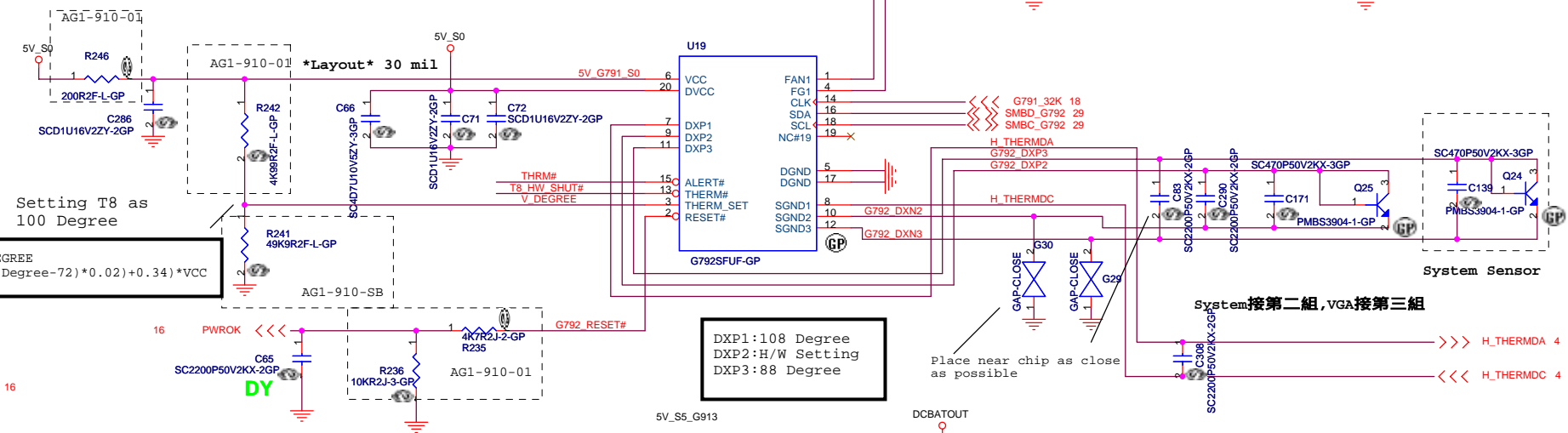
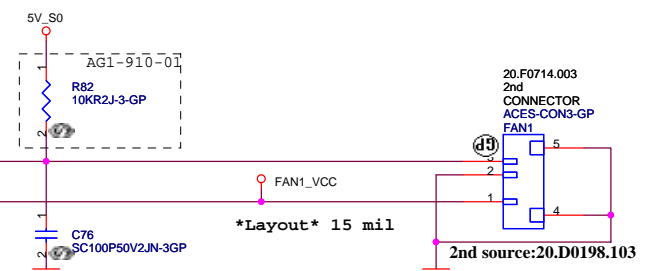
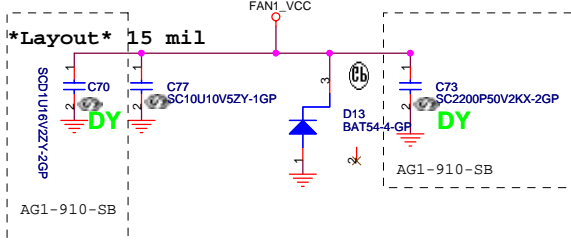
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (4 of 4)**

Size A3 Document Number **AG1(Alviso)** Rev **01**

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Setting T8 as 100 Degree

$$V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

System接第二組,VGA接第三組

<Core Design>

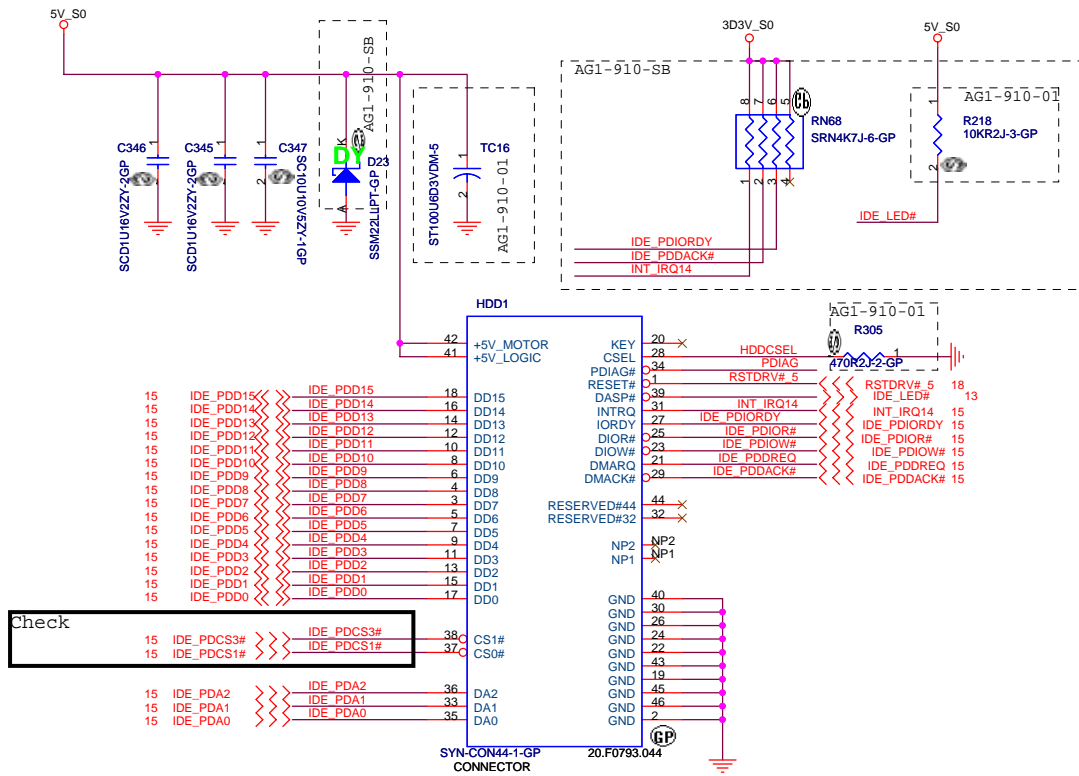
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controller**

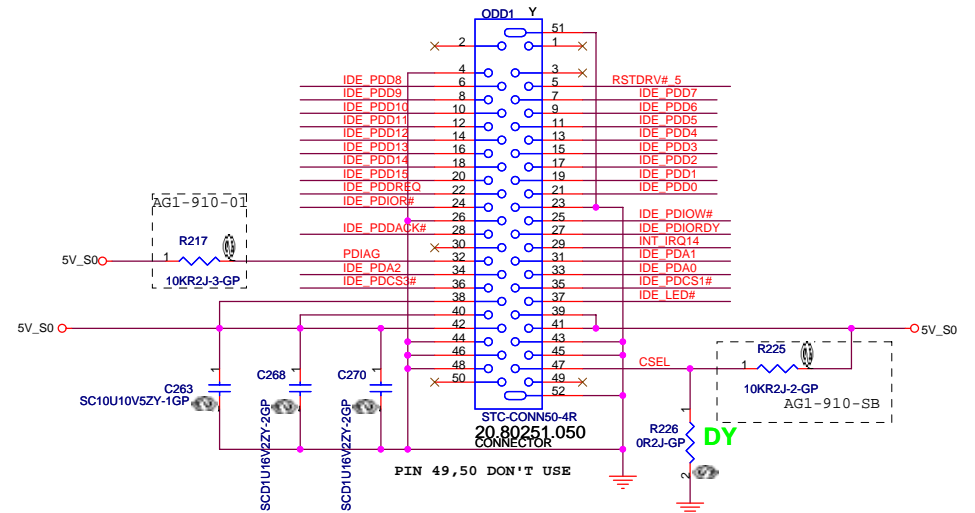
Size Custom	Document Number	Rev
	AG1(Alviso)	01

Date: Wednesday, November 02, 2005 Sheet 19 of 40

HDD Connector

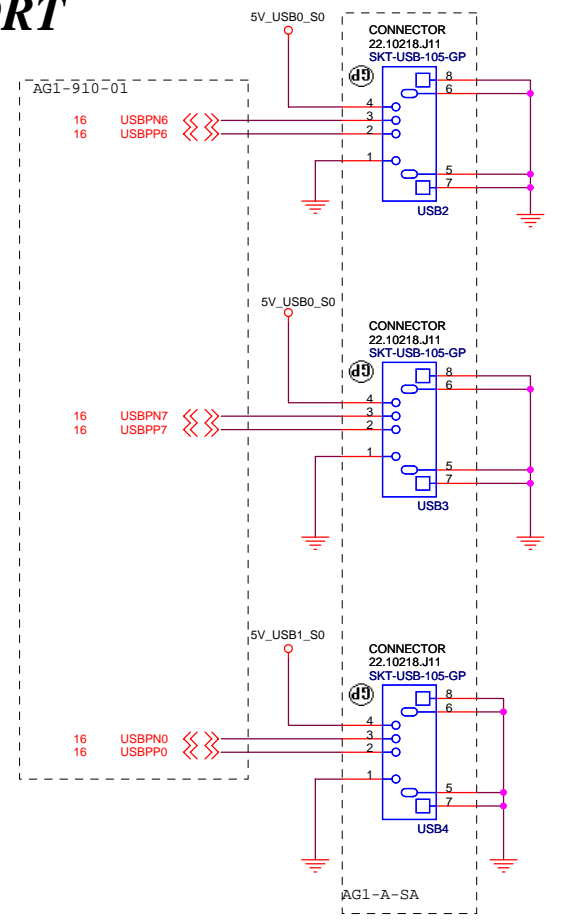
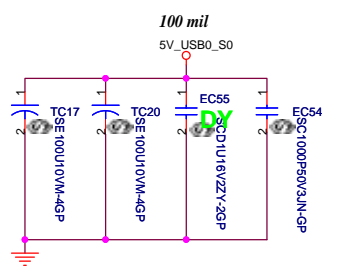
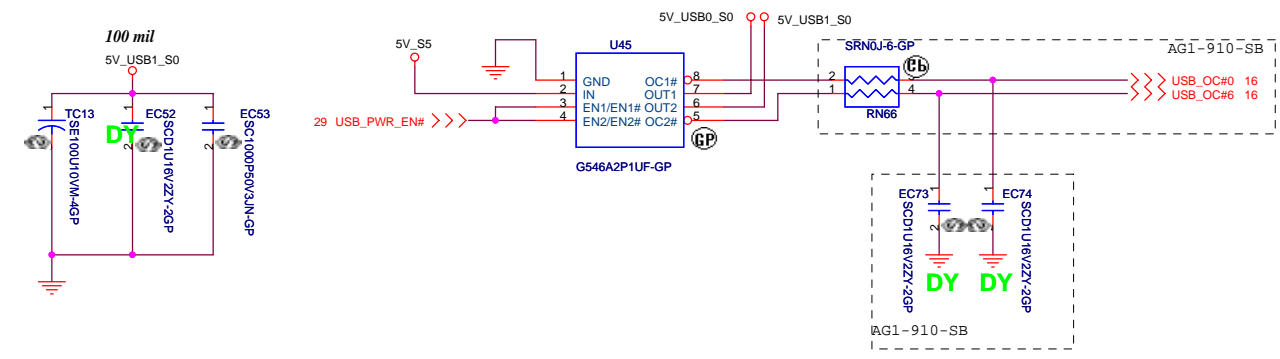


CD-ROM Connector

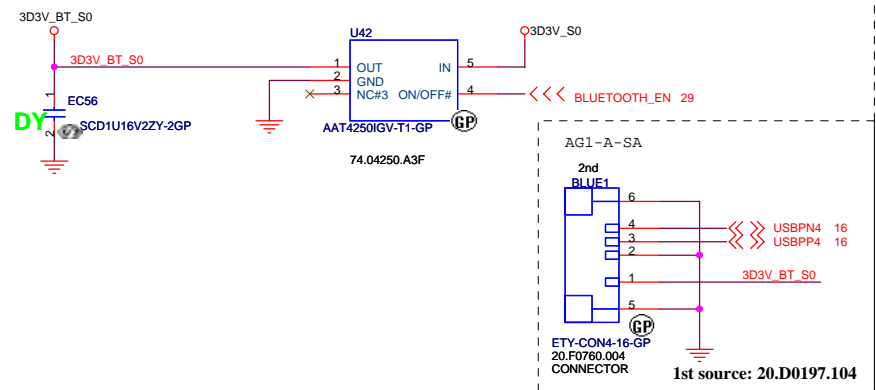


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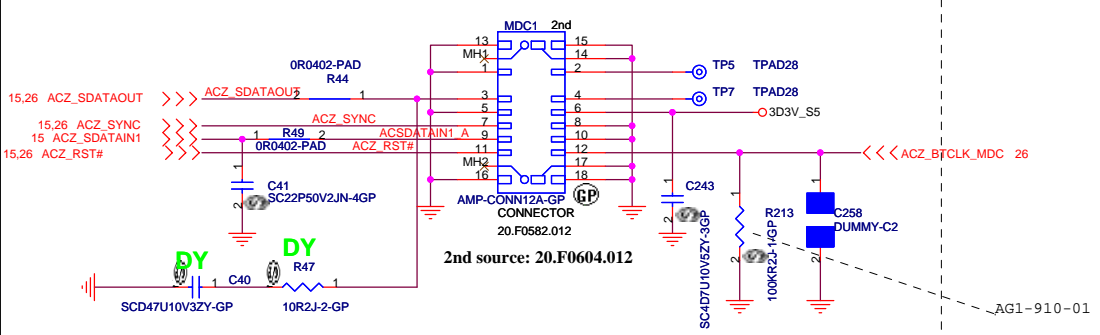
USB PORT



BLUETOOTH MODULE



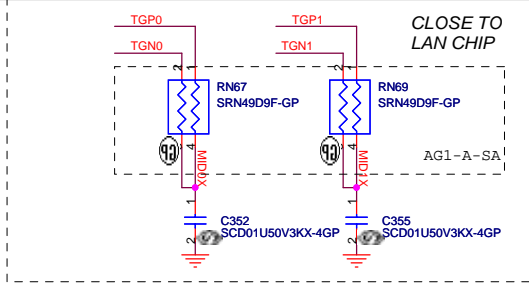
MDC 1.5 CONNECTOR



<Core Design>

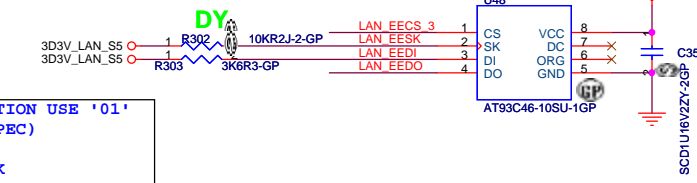
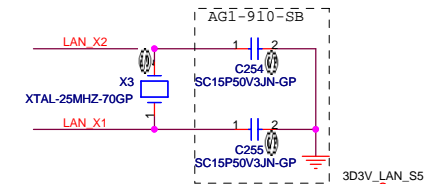
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB / MDC / BLUETOOTH		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date: Friday, October 28, 2005	Sheet 21 of 40	

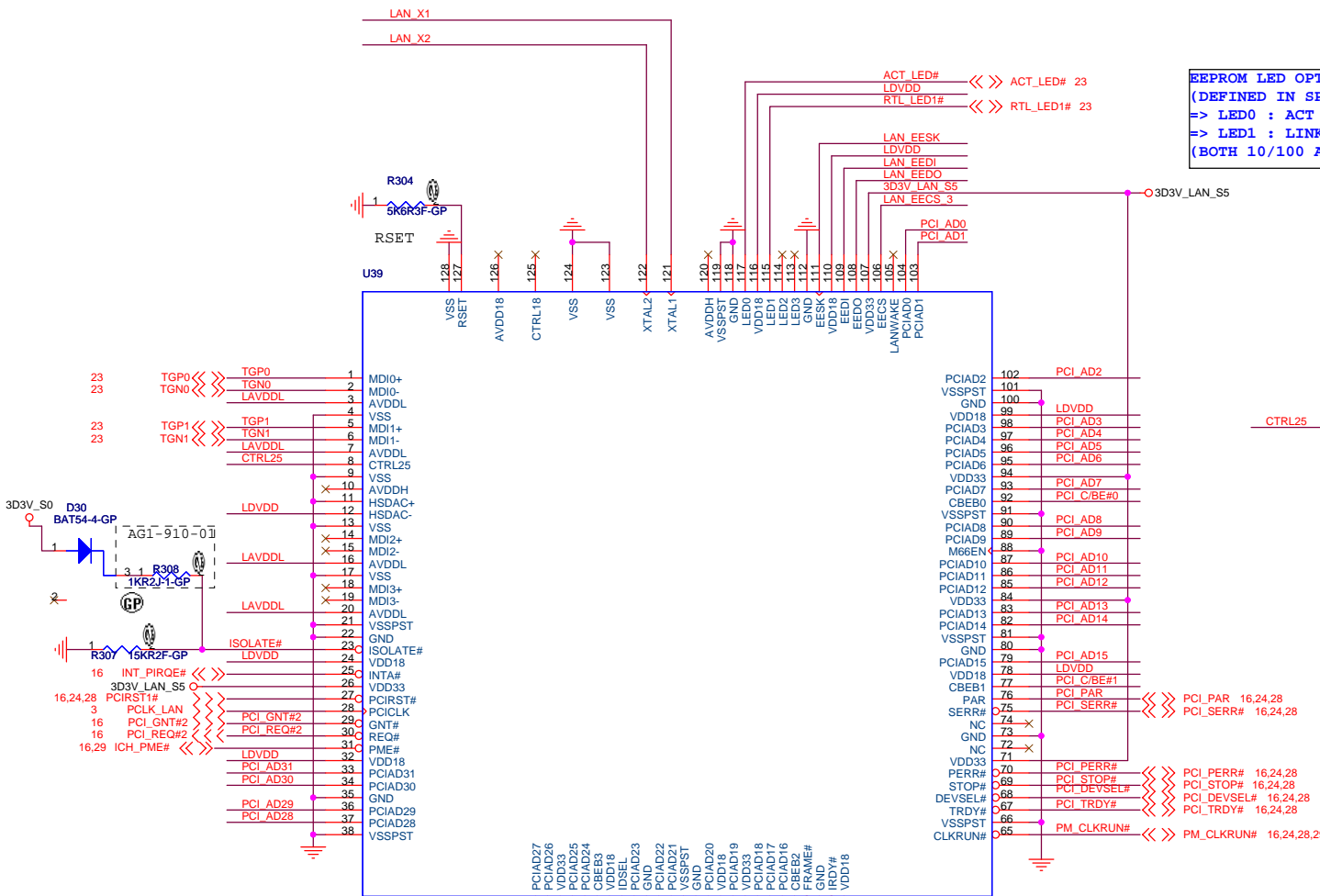


16,24,28 PCI_C/BE#(3..0) <<<

16,24,28 PCI_AD(31..0) <<<



EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)



GIGALAN: RTL810SBL
10/100 LAN: RTL810C

<Core Design>

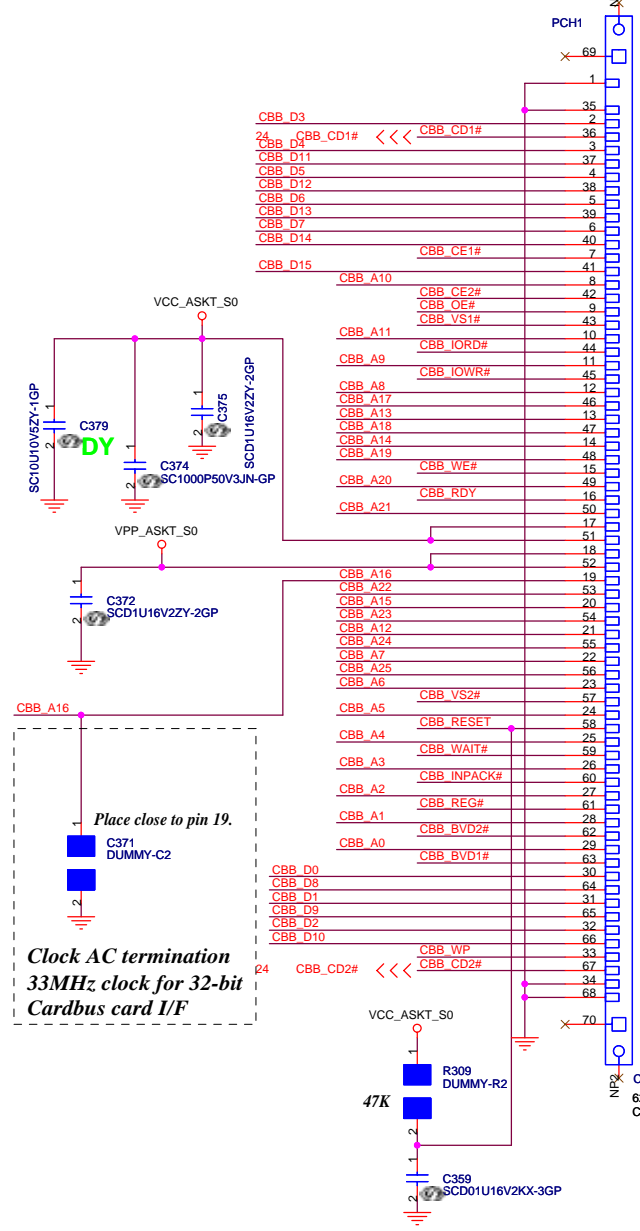
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8100CL**

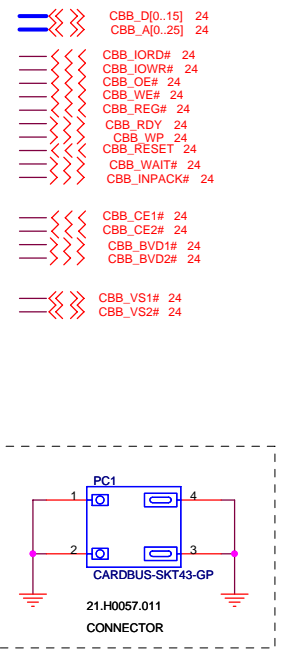
Size: A3, Document Number: **AG1(Alviso)**, Rev: **01**

Date: Tuesday, October 25, 2005, Sheet: 22 of 40

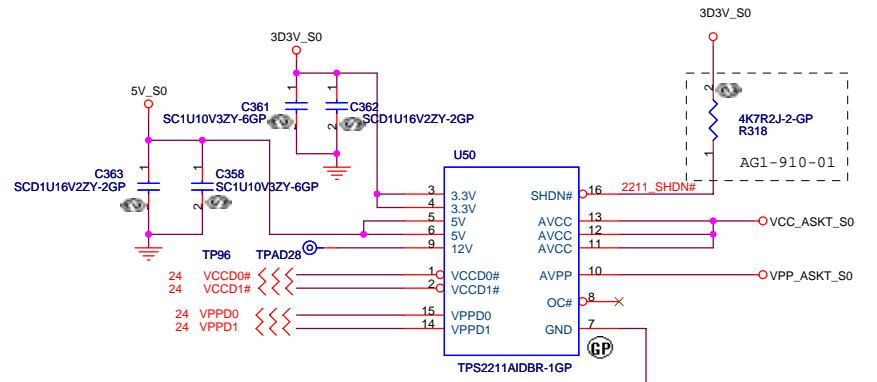
PCMCIA Socket



Cardbus I/F



Power switch

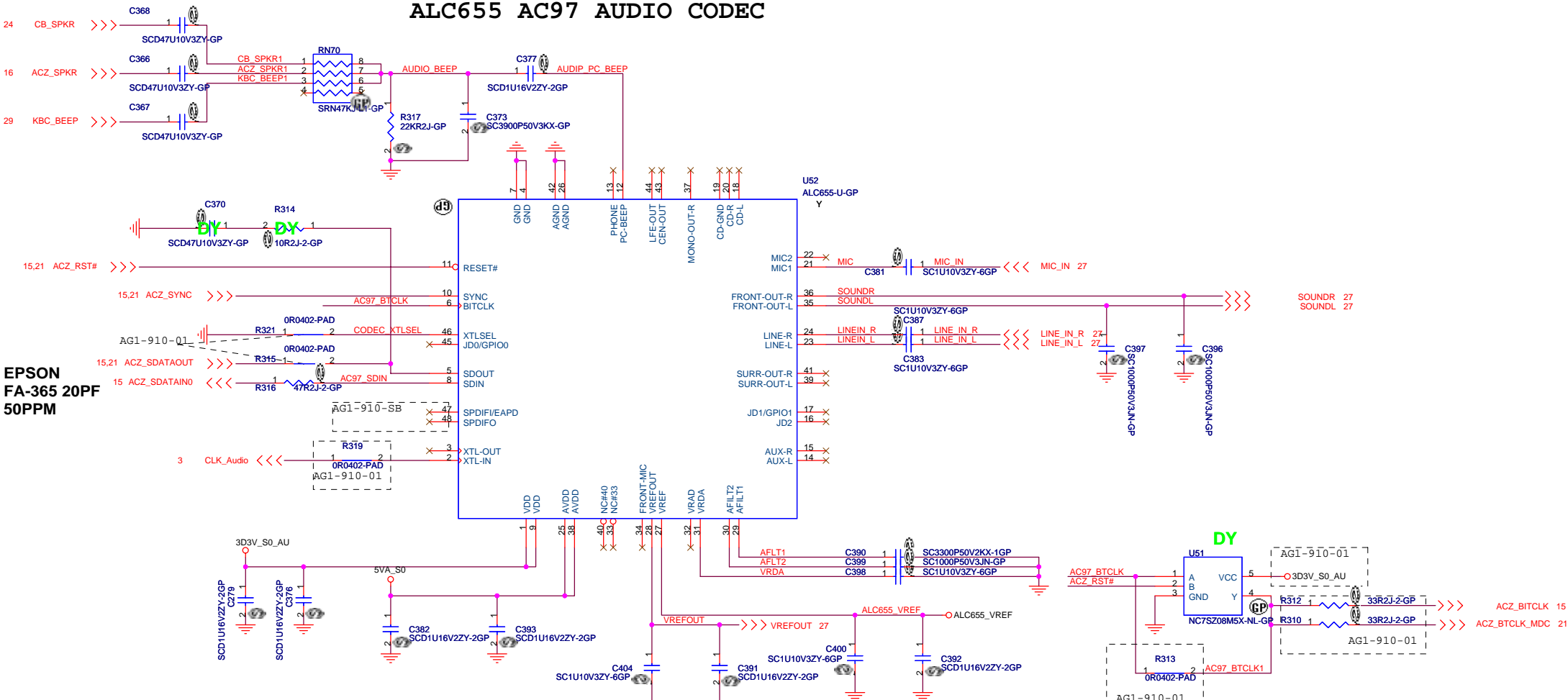


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		PCMCIA	
Size	A3	Document Number	AG1(Alviso)
Date:	Tuesday, October 25, 2005	Sheet	25 of 40
Rev	01		

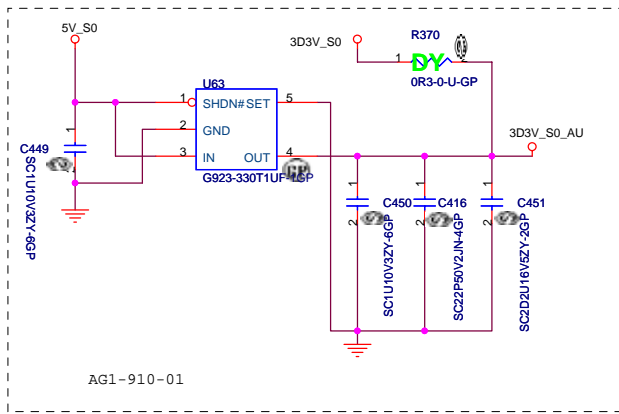
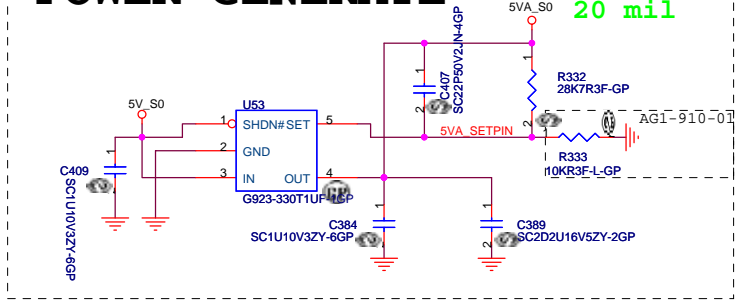
ALC655 AC97 AUDIO CODEC



EPSON
FA-365 20PF
50PPM

POWER GENERATE

Layout
20 mil



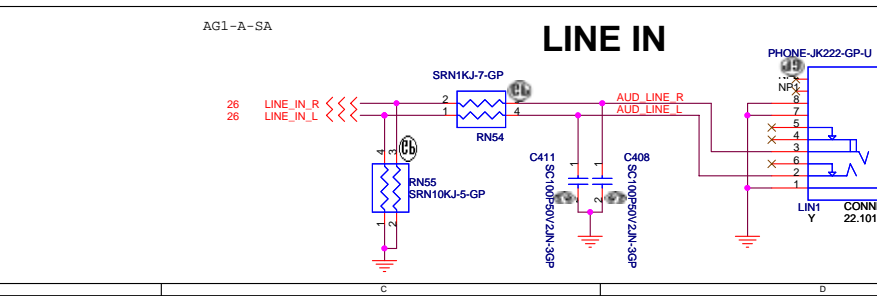
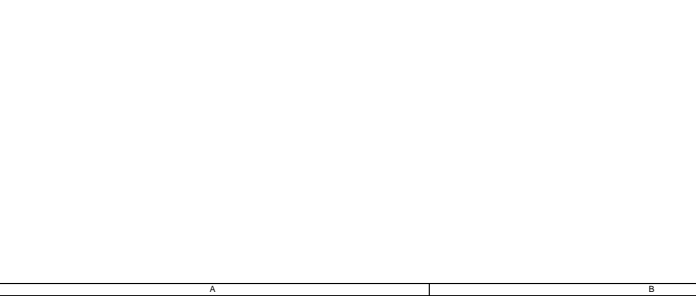
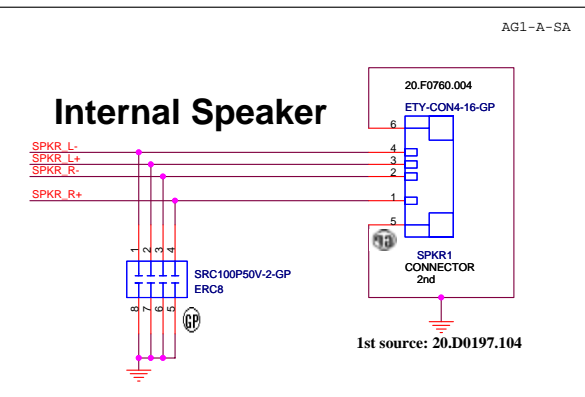
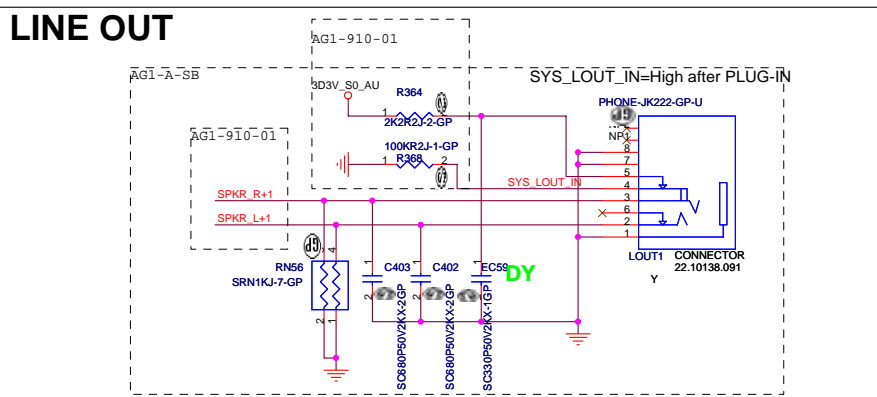
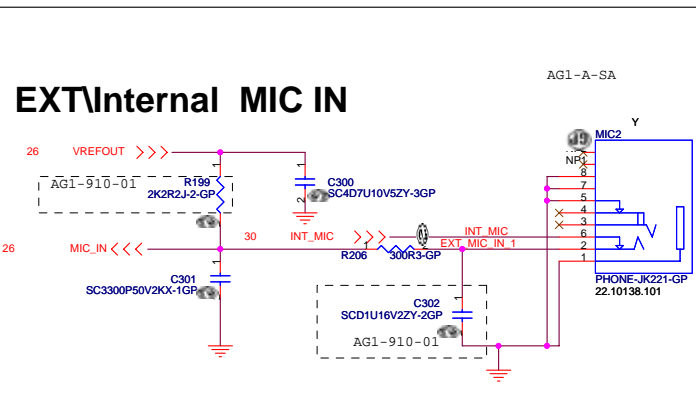
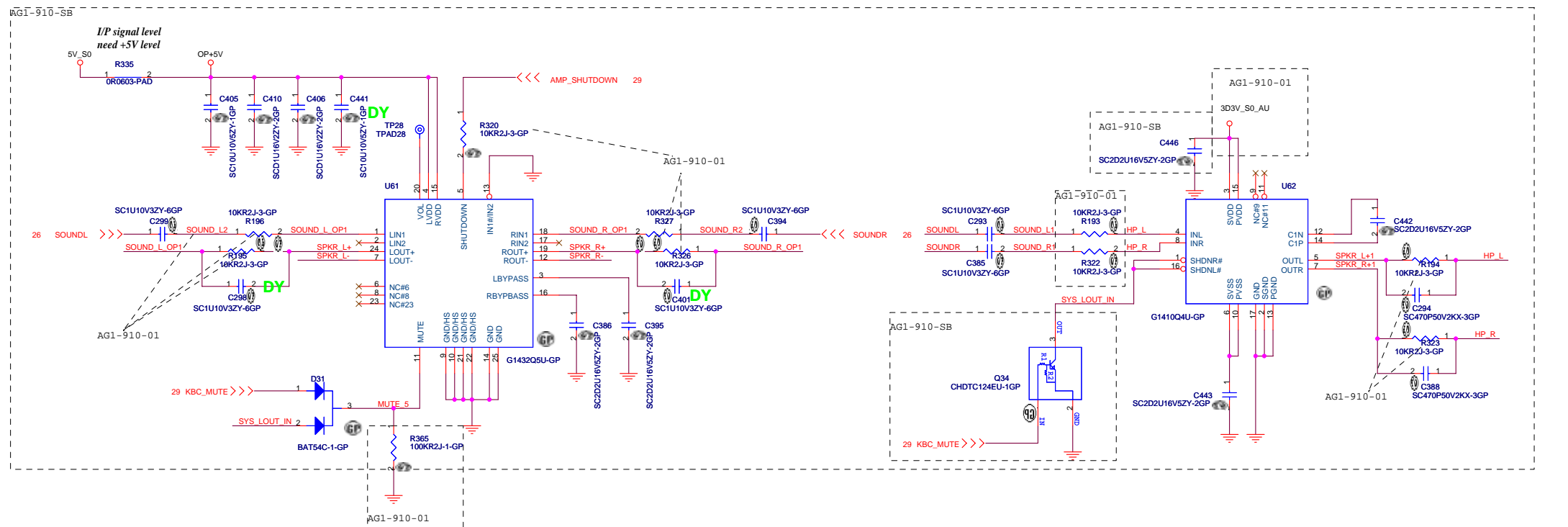
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AC'97 CODEC - ALC655**

Size: A3	Document Number: AG1(Alviso)	Rev: 01
Date: Tuesday, November 01, 2005		Sheet 26 of 40

AUDIO OP AMPLIFIER

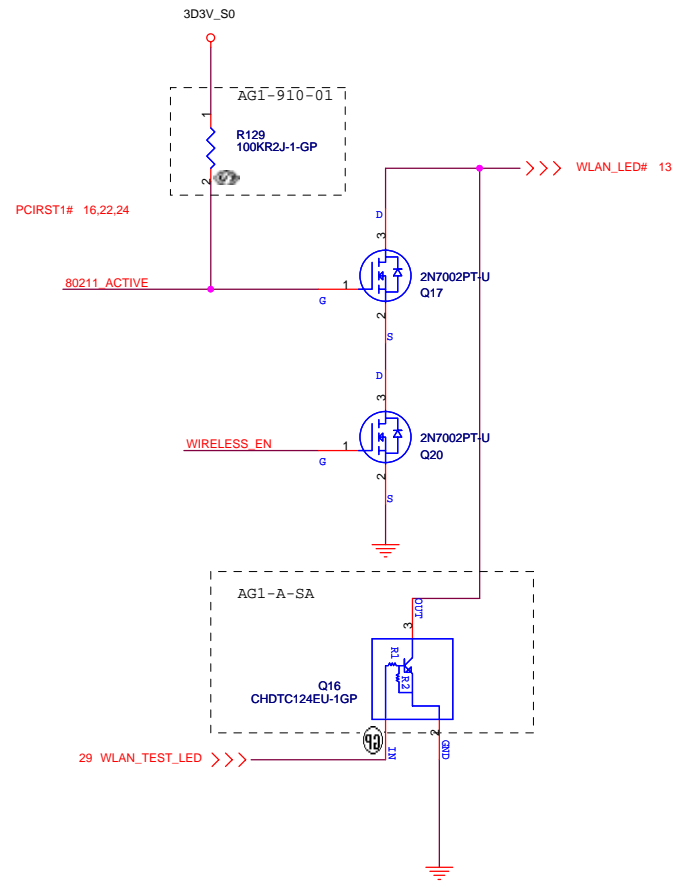
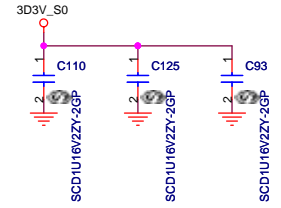
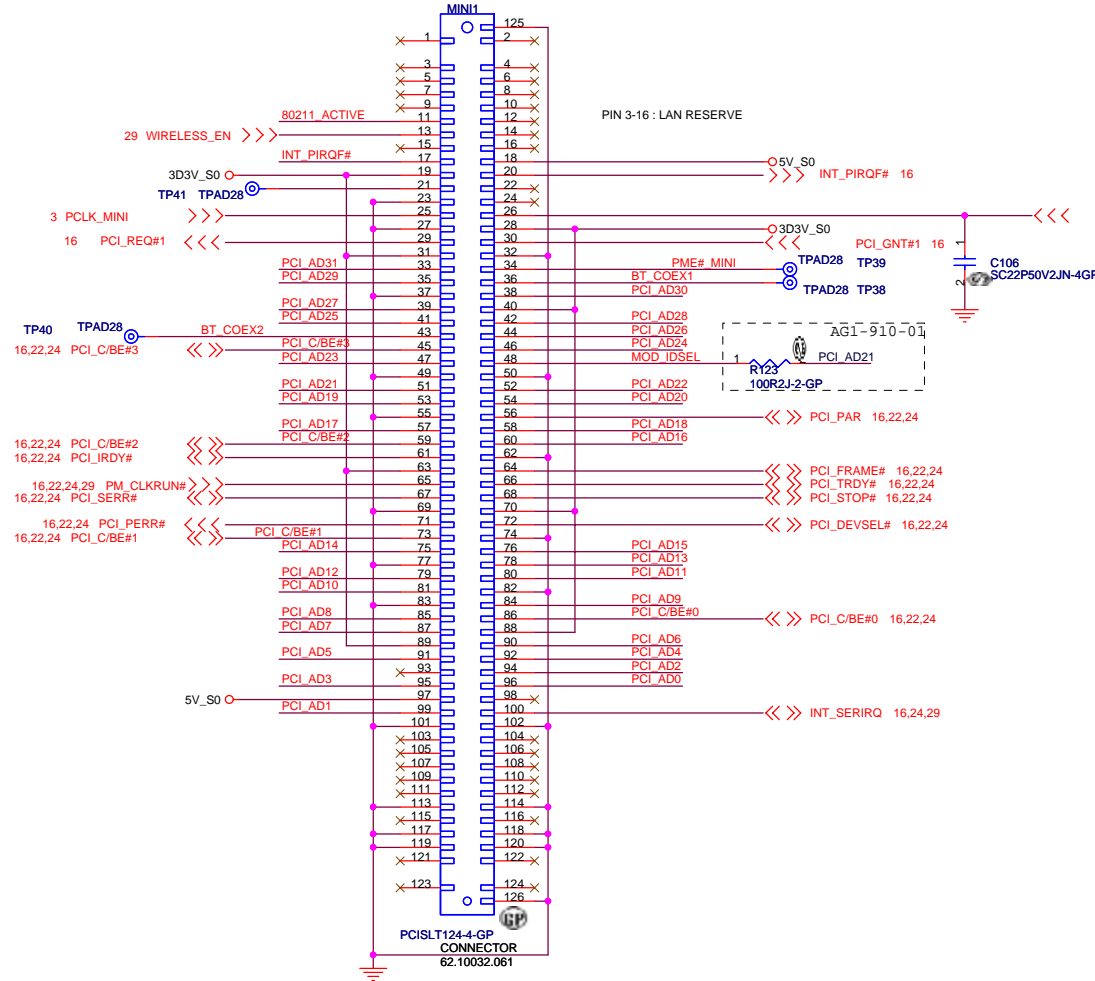


<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		Audio AMP and Jack	
Size	Document Number	Rev	
AG1(Alviso)		01	
Date: Monday, October 31, 2005	Sheet 27	of 40	

16.22.24 PCI_AD[31..0] <<<



<Core Design>

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Title: **MINI-PCI**

Size A3 Document Number: **AG1(Alviso)** Rev: **01**

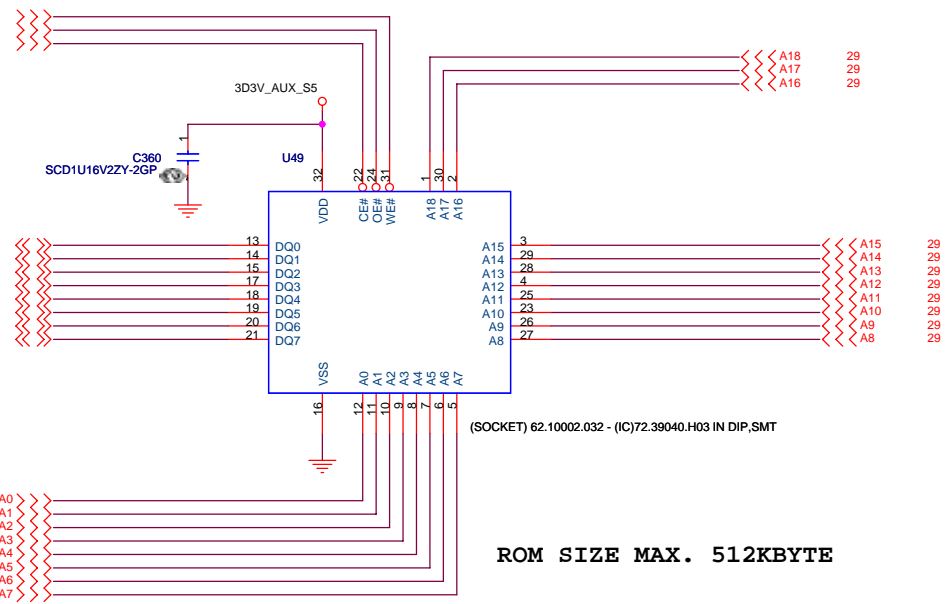
Date: Tuesday, October 25, 2005 Sheet 28 of 40

>>> KBC_D[0..7] 29

29 KBCBIOS_WE#
29 KBCBIOS_RD#
29 KBCBIOS_CS#

29 KBC_D0
29 KBC_D1
29 KBC_D2
29 KBC_D3
29 KBC_D4
29 KBC_D5
29 KBC_D6
29 KBC_D7

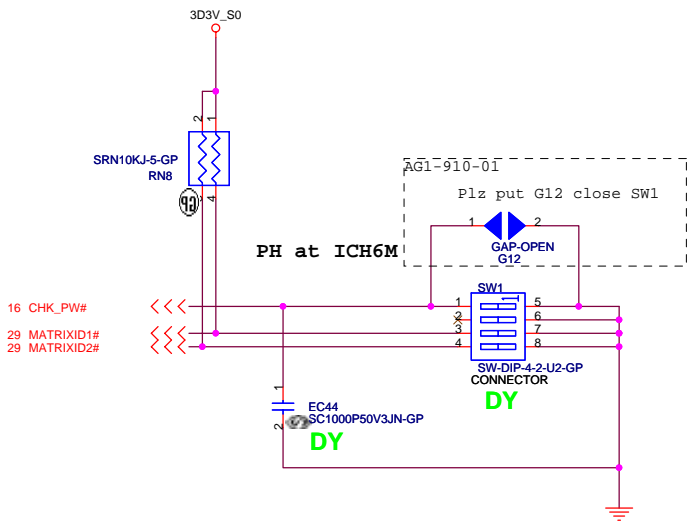
29 A0
29 A1
29 A2
29 A3
29 A4
29 A5
29 A6
29 A7



(SOCKET) 62.10002.032 - (IC)72.39040.H03 IN DIP,SMT

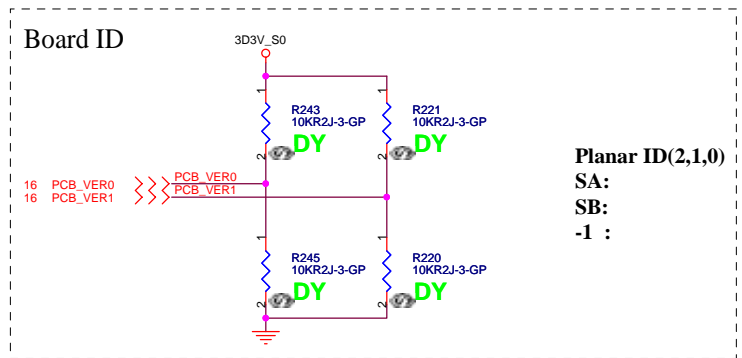
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

	US	Jap	Eur	Other	
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0



Board ID

Planar ID(2,1,0)
SA:
SB:
-1 :

<Core Design>

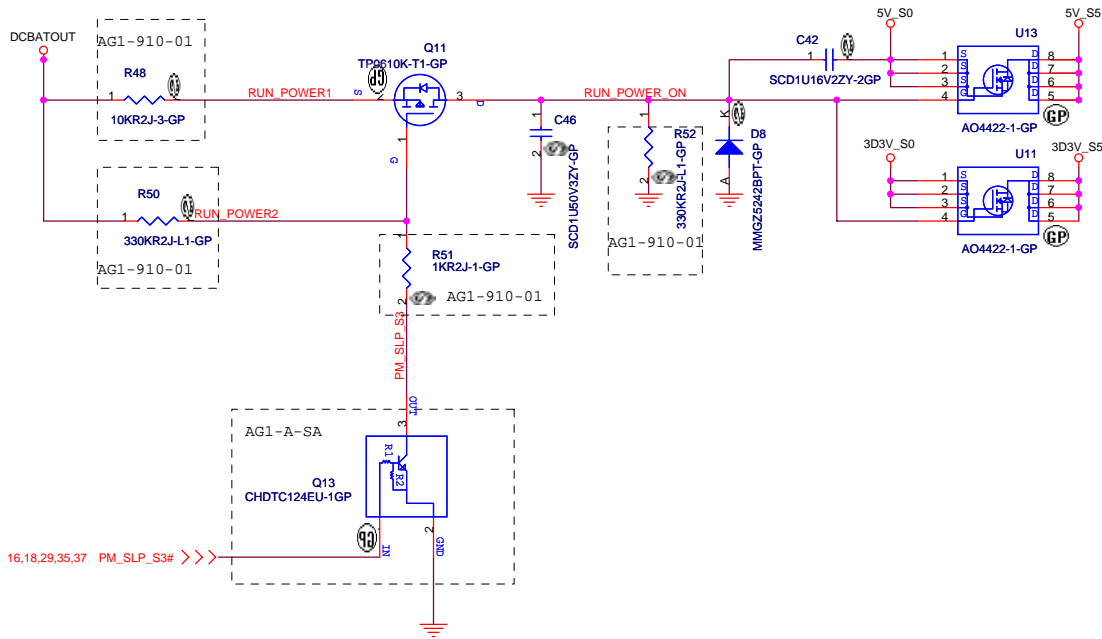
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

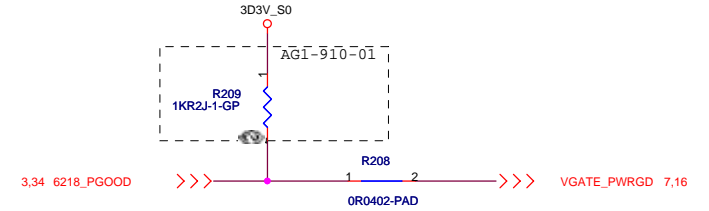
Size A3	Document Number	Rev
	AG1-910	01

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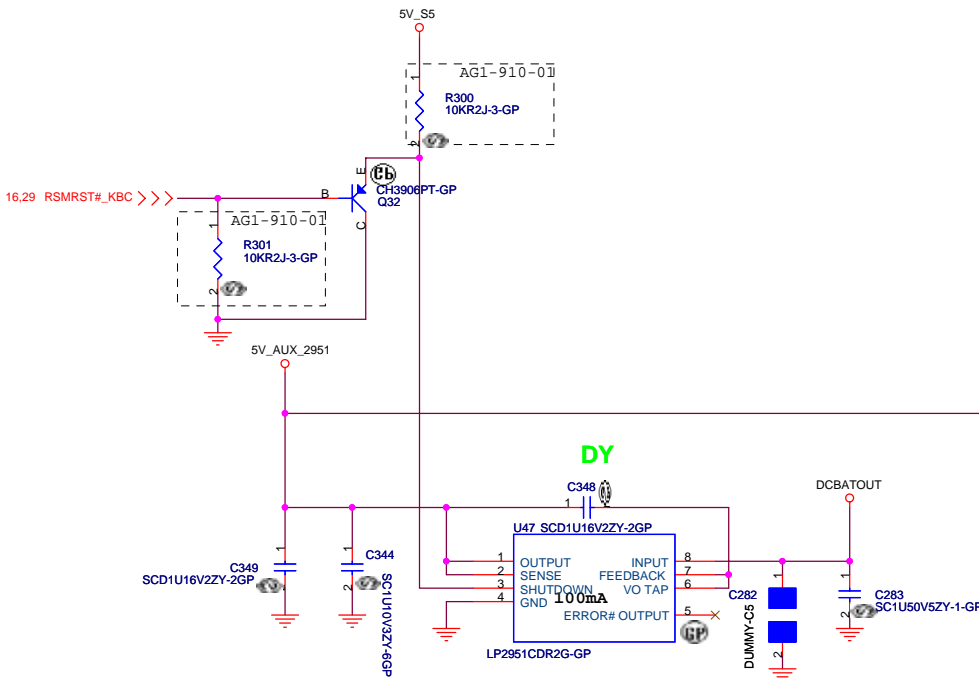
Run Power



PWRGD for NB and SB

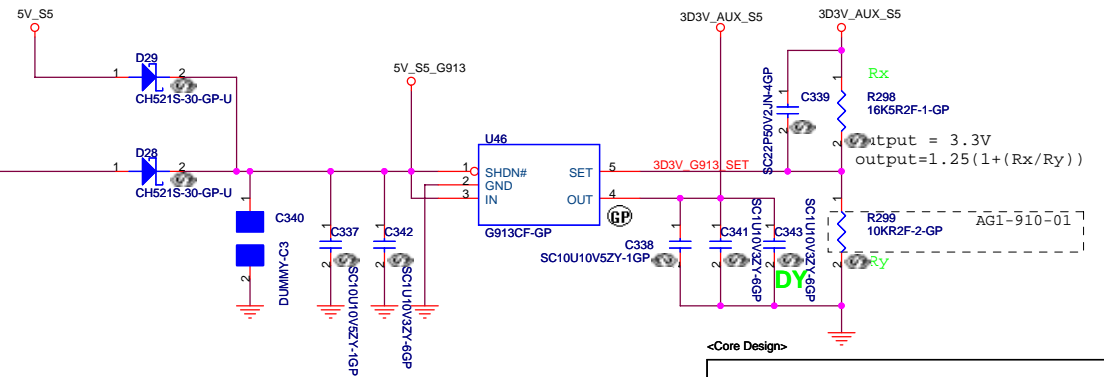


PWRGD to Turn on CPU_Core_Power



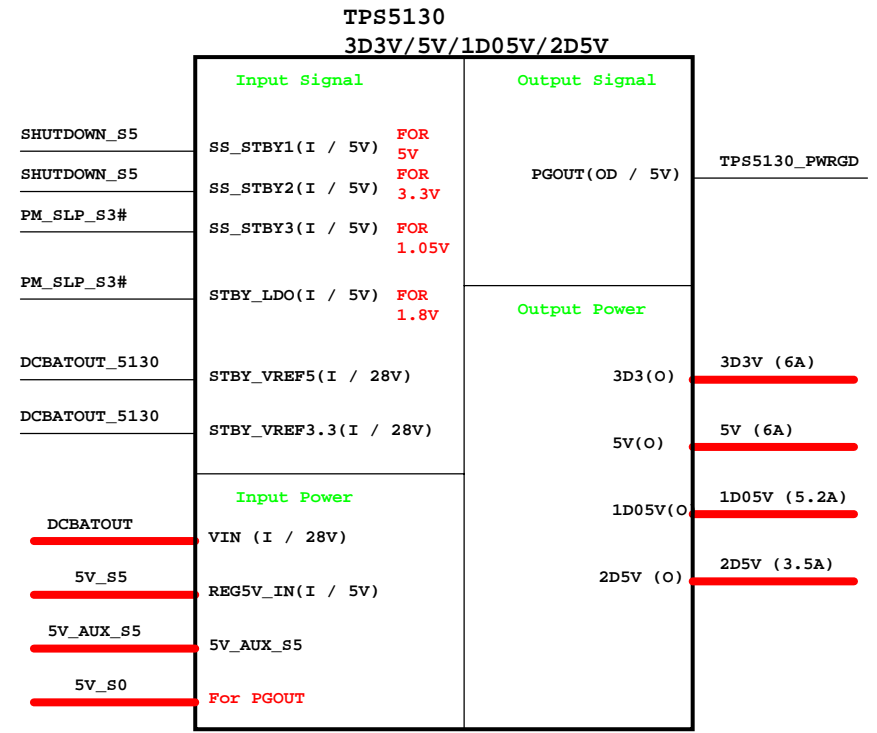
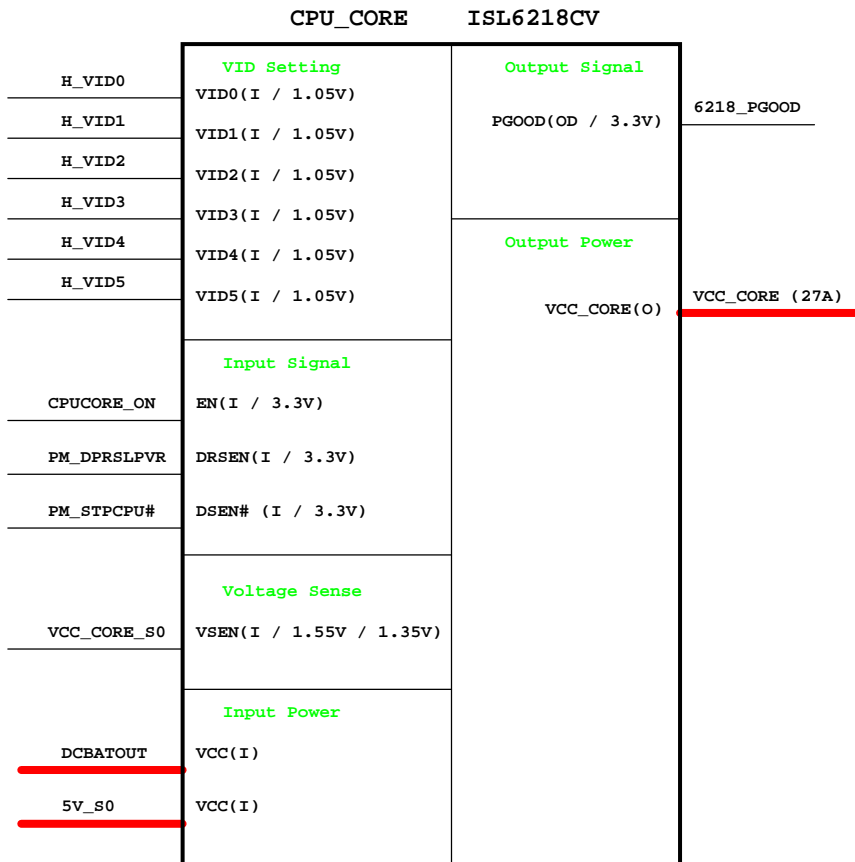
Aux Power

3D3V_AUX_S5

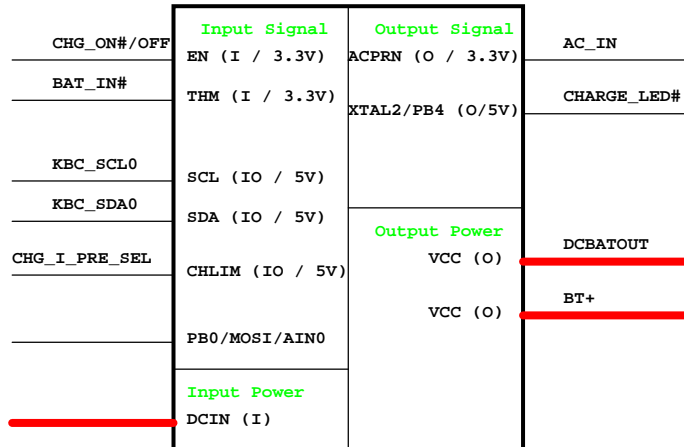


<Core Design>

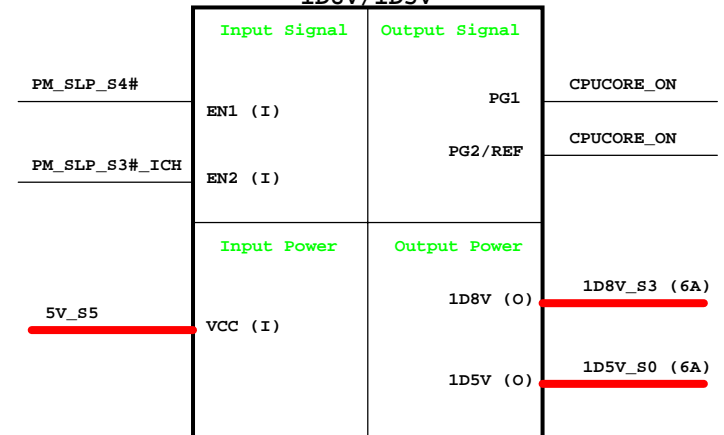
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RUN POWER and 3D3V AUX S5			
Size A3	Document Number AG1-910	Rev 01	
Date: Tuesday, October 25, 2005		Sheet 32	of 40



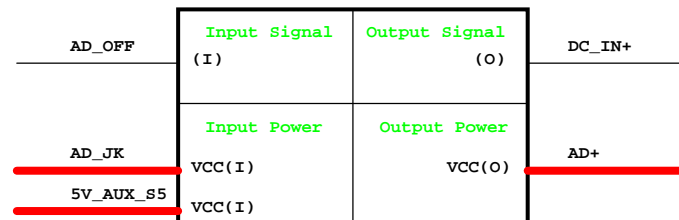
Charger_ISL6255



ISL6227 1D8V/1D5V



Adapter



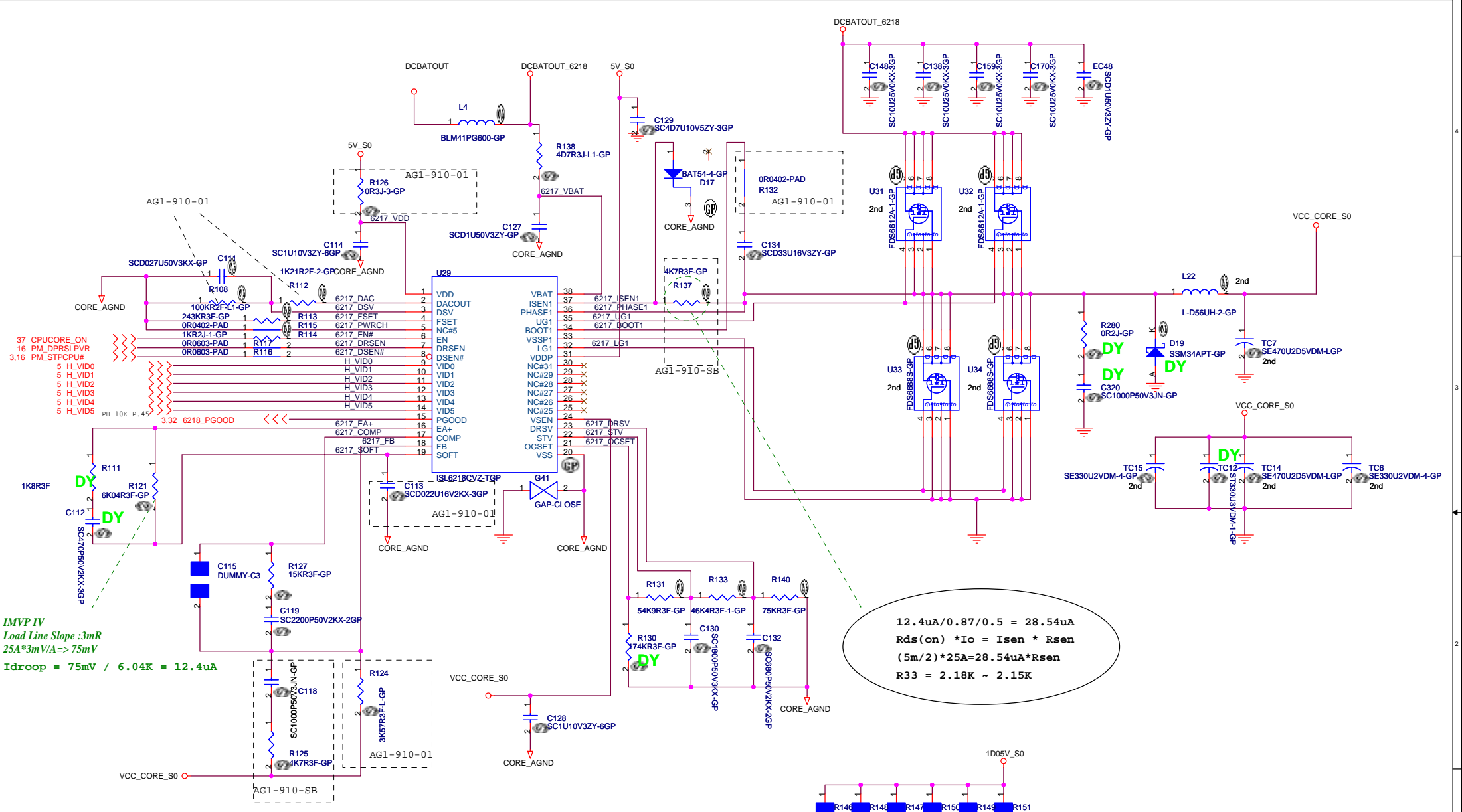
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Diagram**

Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

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37 CPUCORE_ON
16 PM_DPRS1PVR
3,16 PM_STPCPU#
5 H_VID0
5 H_VID1
5 H_VID2
5 H_VID3
5 H_VID4
5 H_VIDS

IMVP IV
Load Line Slope :3mR
25A*3mV/A=>75mV
Idroop = 75mV / 6.04K = 12.4uA

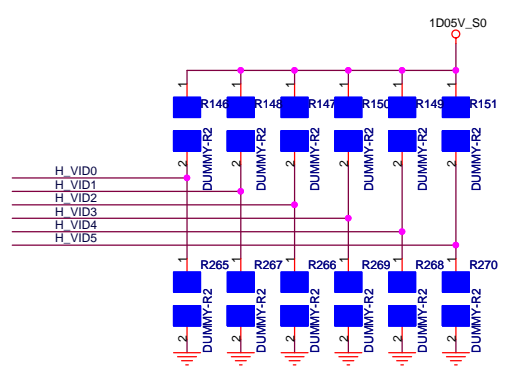
$$12.4\mu\text{A} / 0.87 / 0.5 = 28.54\mu\text{A}$$

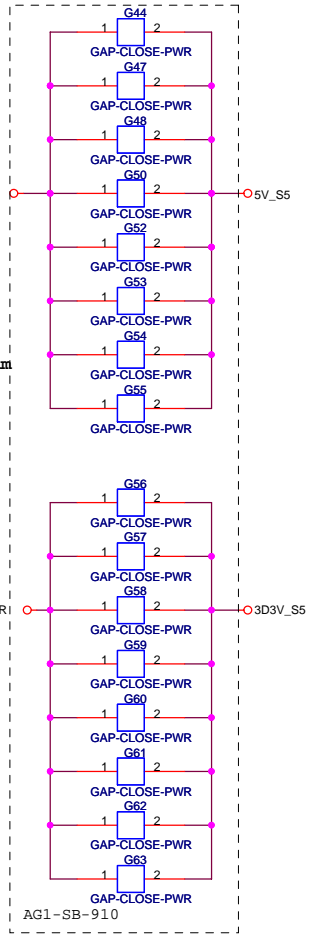
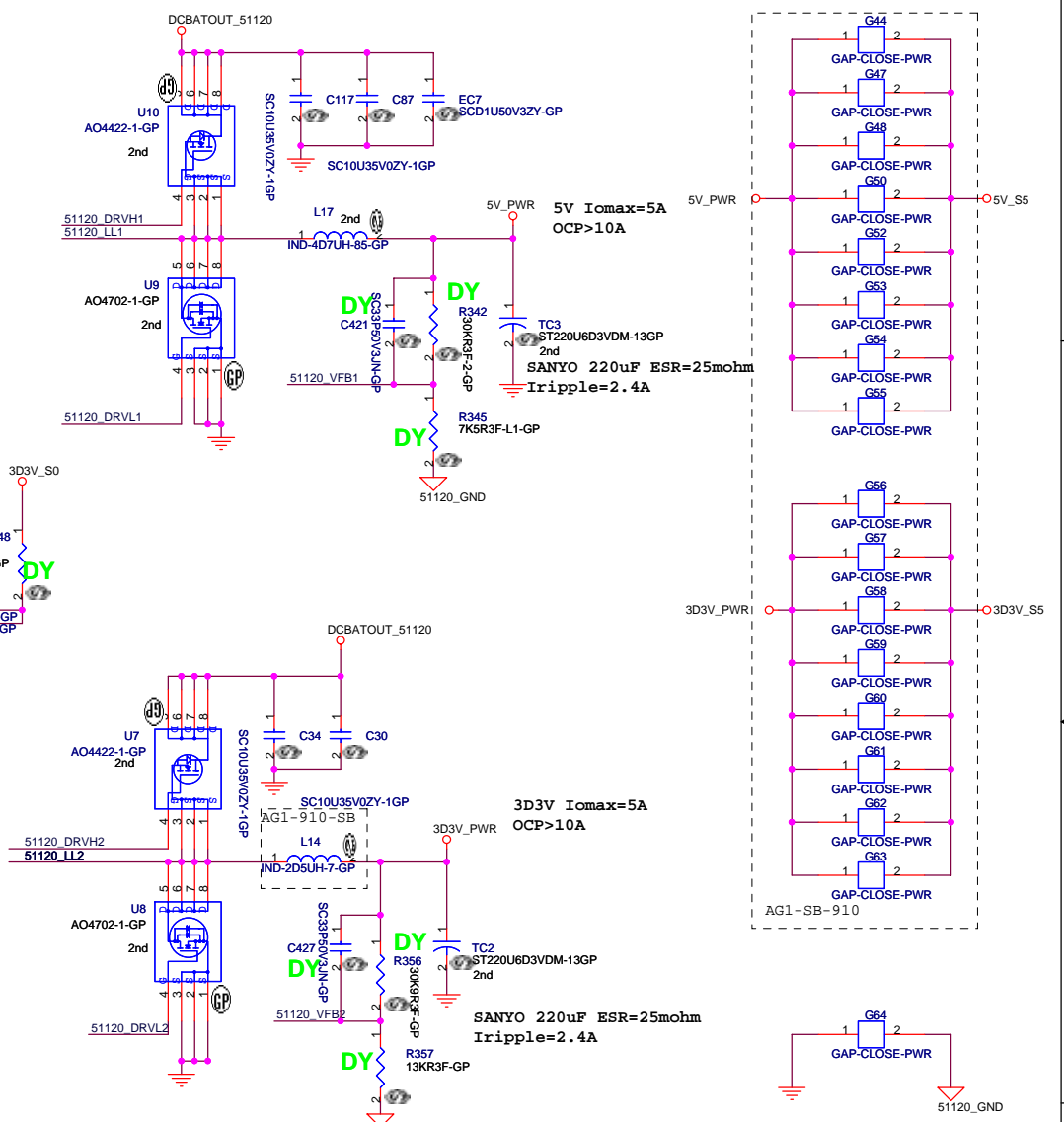
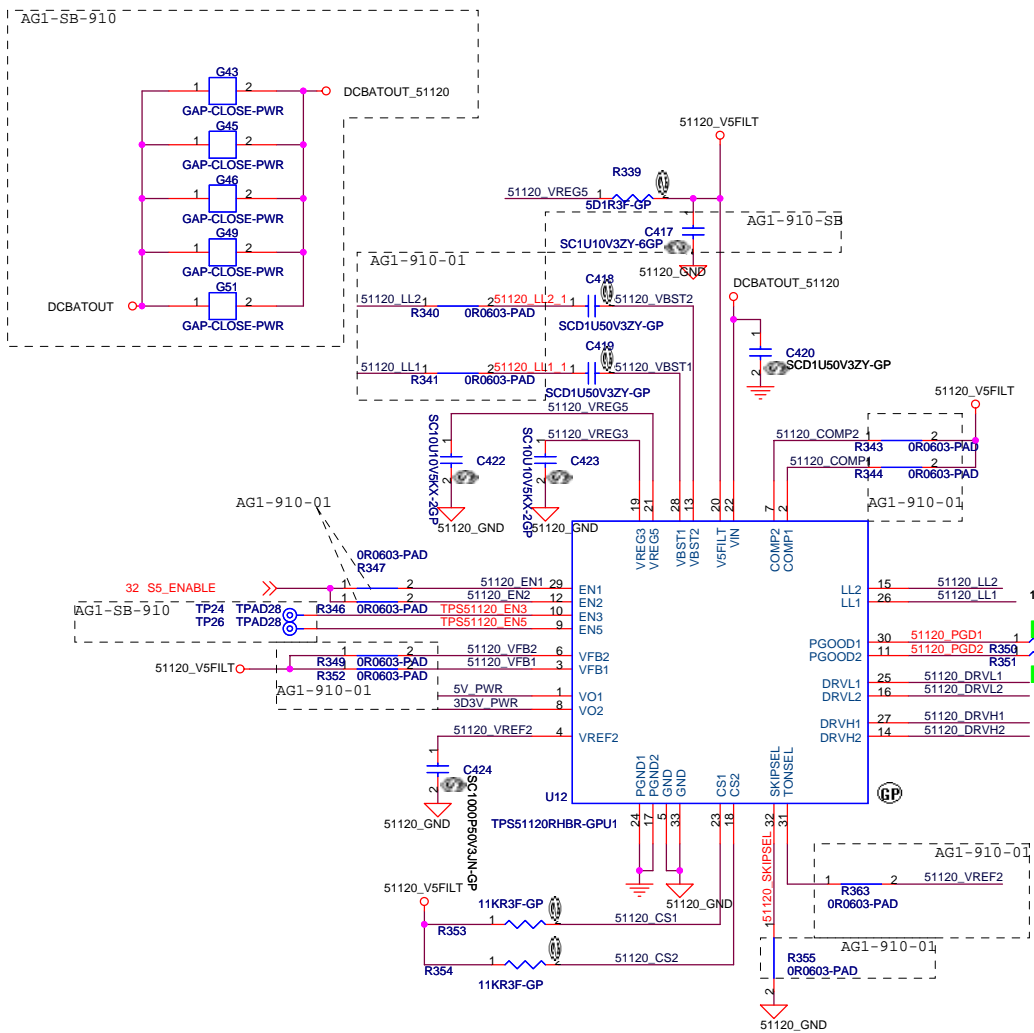
$$R_{ds(on)} * I_o = I_{sen} * R_{sen}$$

$$(5\text{m} / 2) * 25\text{A} = 28.54\mu\text{A} * R_{sen}$$

$$R_{33} = 2.18\text{K} \sim 2.15\text{K}$$

- U12,U14:AO4422 84.04422.037
U13,U15:AO4430 84.04430.B37
R100:3K83R2F
- U12,U14:IRF7413 84.07413.037
U13,U15:IRF7832-U 84.07832.037
R100:2K43R2F





$$V_{out} = 1V * (R1 + R2) / R2$$

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

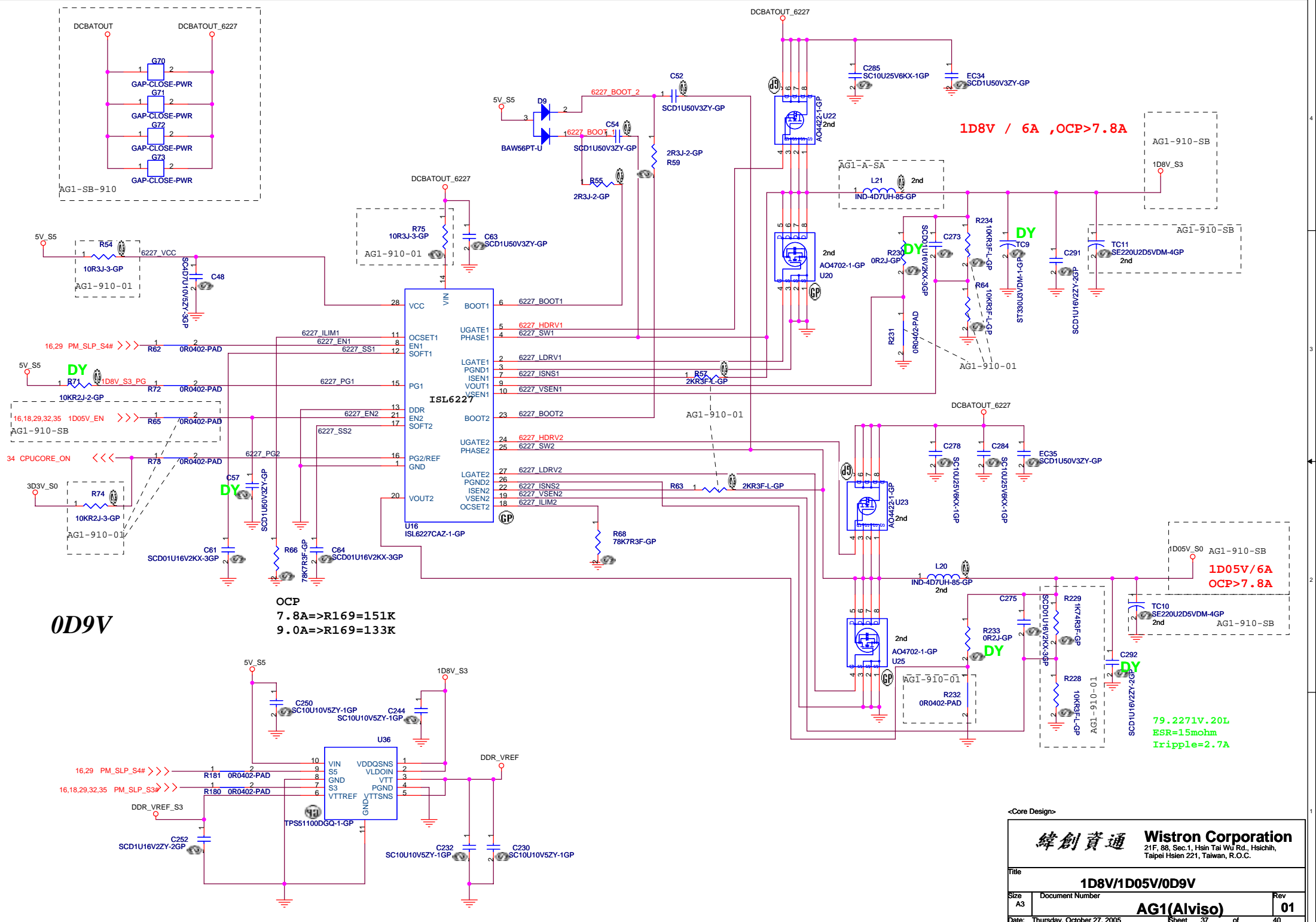
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: TPS51120 3D3V 5V

Size: A3 Document Number: AG1(Alviso) Rev: 01

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0D9V

OCP
 7.8A=>R169=151K
 9.0A=>R169=133K

1D8V / 6A ,OCP>7.8A

1D05V / 6A
 OCP>7.8A

79.2271V.20L
 ESR=15mohm
 Tripple=2.7A

<Core Design>

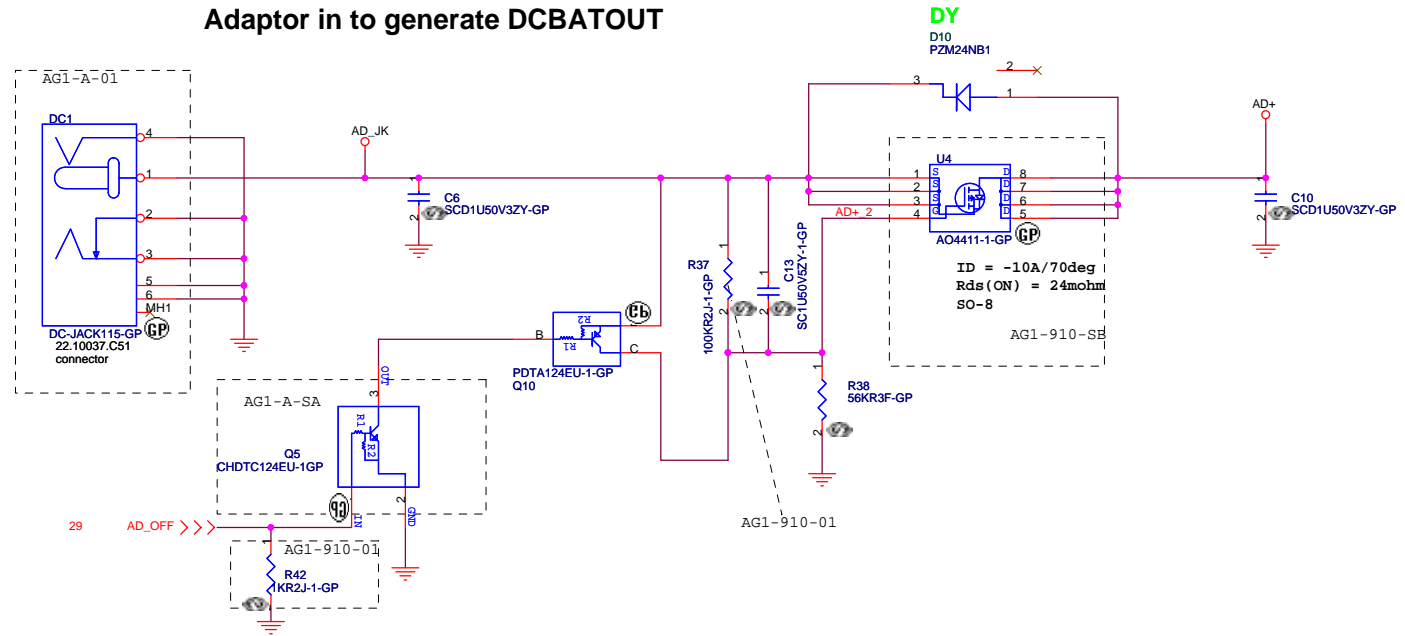
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **1D8V/1D05V/0D9V**

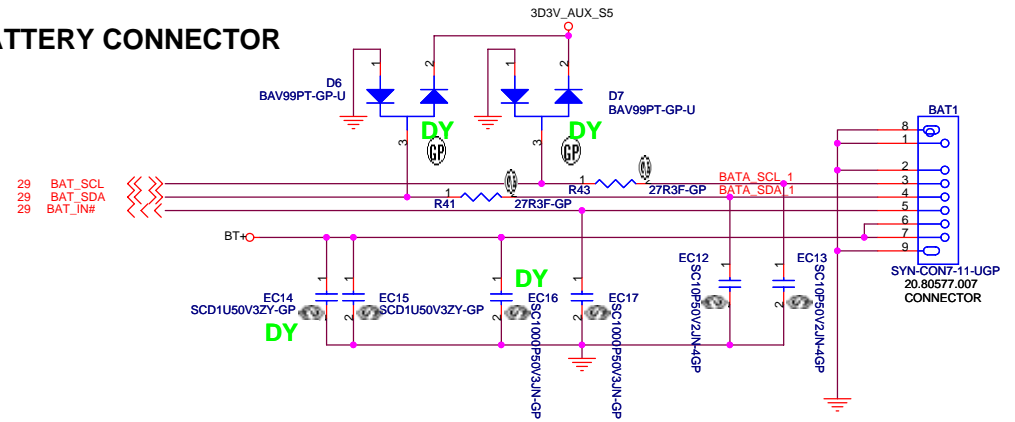
Size: A3	Document Number:	Rev: 01
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Date: Thursday, October 27, 2005 Sheet 37 of 40

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
A3		01
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