

# Compal Confidential

## PAV70 Schematics Document

### Intel Pineview Processor with Tigerpoint + DDRII

2010-07-01

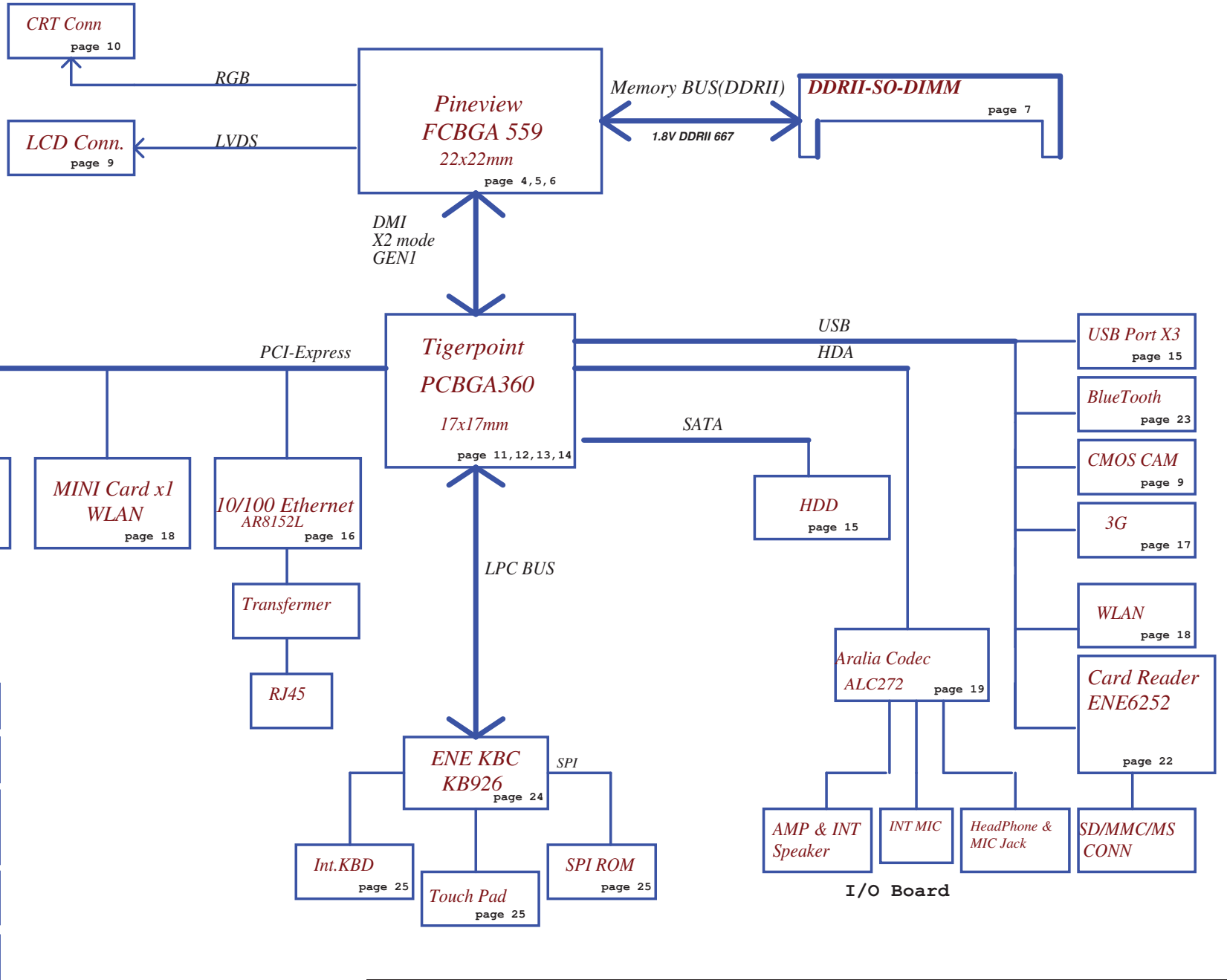
REV: 1.0

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# Compal Confidential

Model Name :  
File Name : LA-6221P

Clock Generator  
CK505  
page 8



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				Block Diagrams	
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>
0 (EVT)	0	0 V	0 V	0 V
1 (DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2 (PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3 (MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

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## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

## No PCI Device

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

## Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

## USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
	UHCI2	Port1	MB USB Conn2.
		Port2	MB USB Conn3.
UHCI3	Port3	CMOS	
	Port4	Card Reader	
	Port5	WWAN	
EHCI2	UHCI4	Port6	BT
	UHCI5	Port7	WLAN
		Port8	
	UHCI6	Port9	
		Port10	
			Port11

## PCIE table

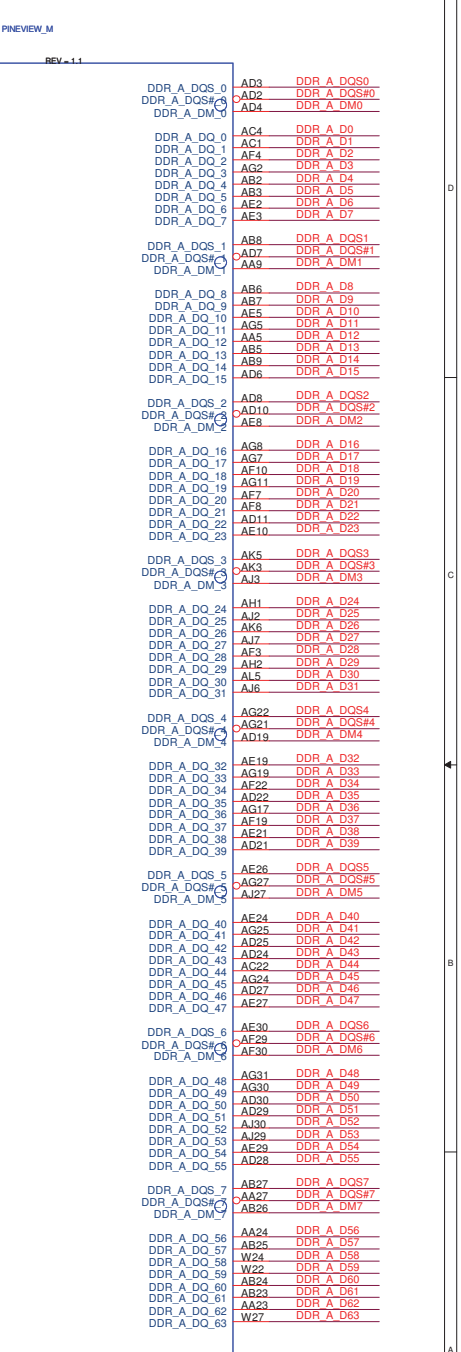
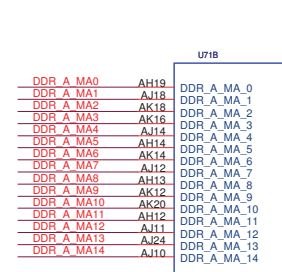
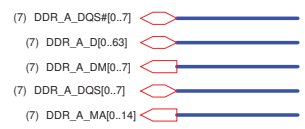
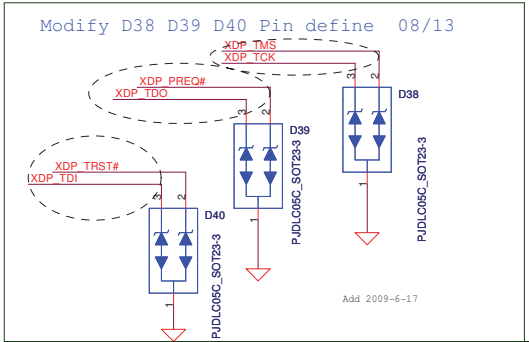
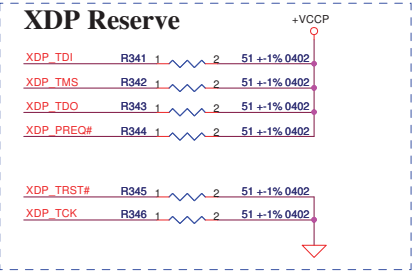
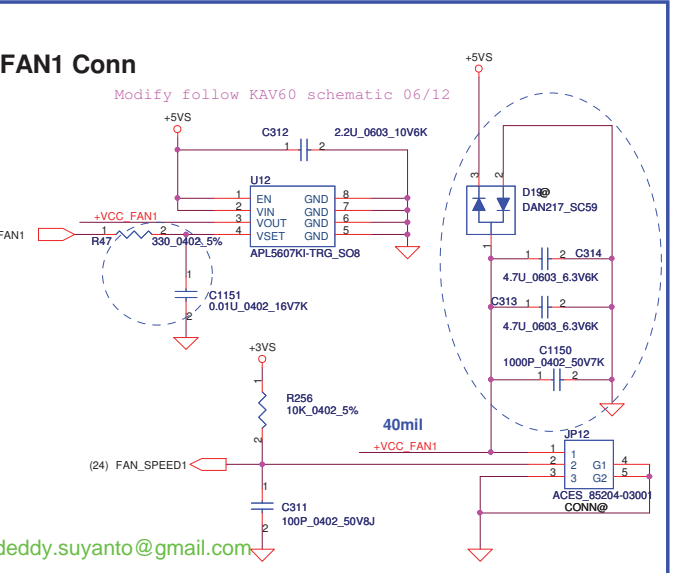
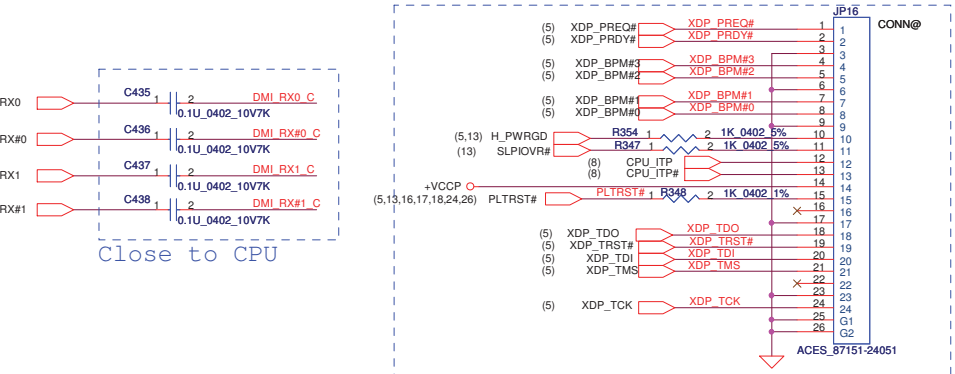
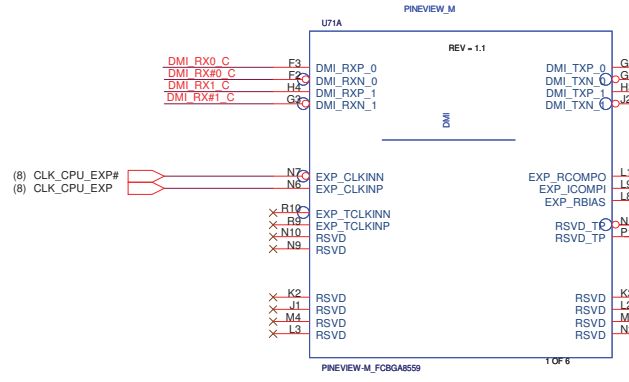
PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	3G
PCIE port4	
PCIE port5	
PCIE port6	

## SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

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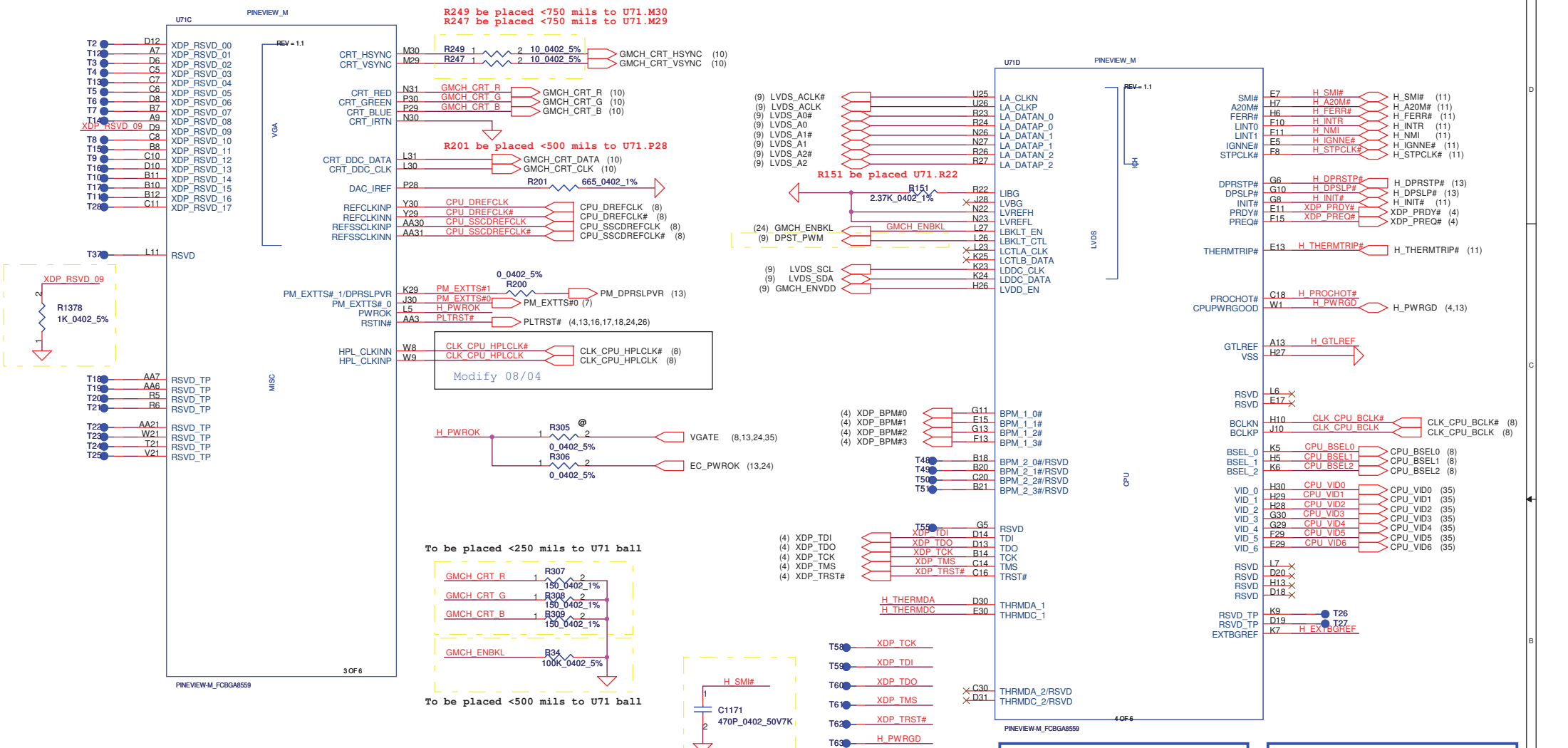


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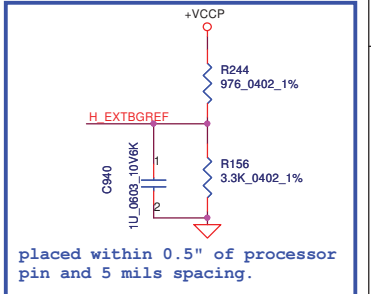
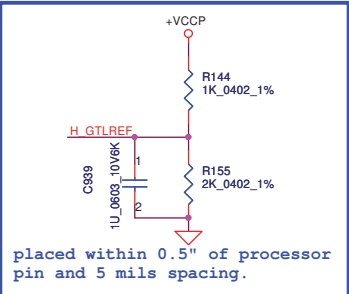
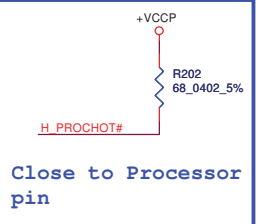
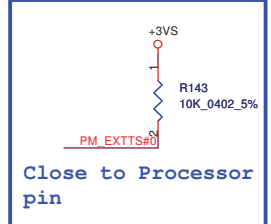
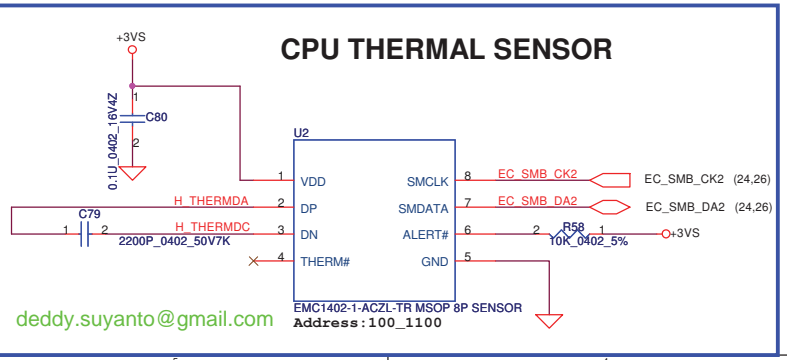
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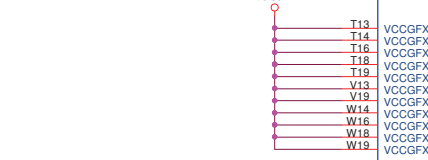
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



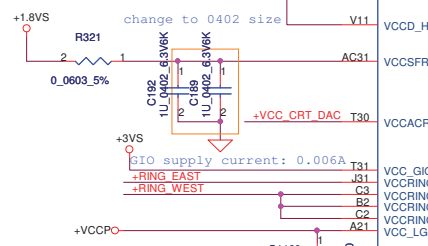
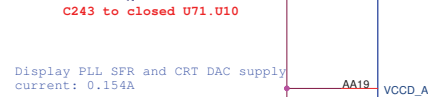
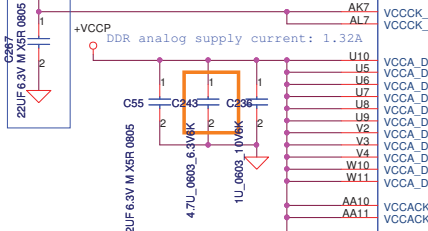
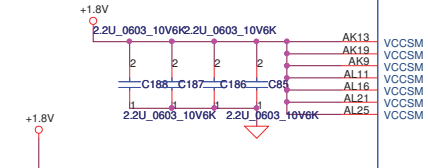
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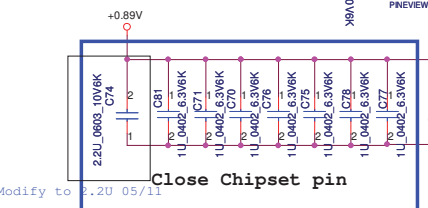
GFX supply current: 1.38A  
Sustained GFX supply current: 1.05A



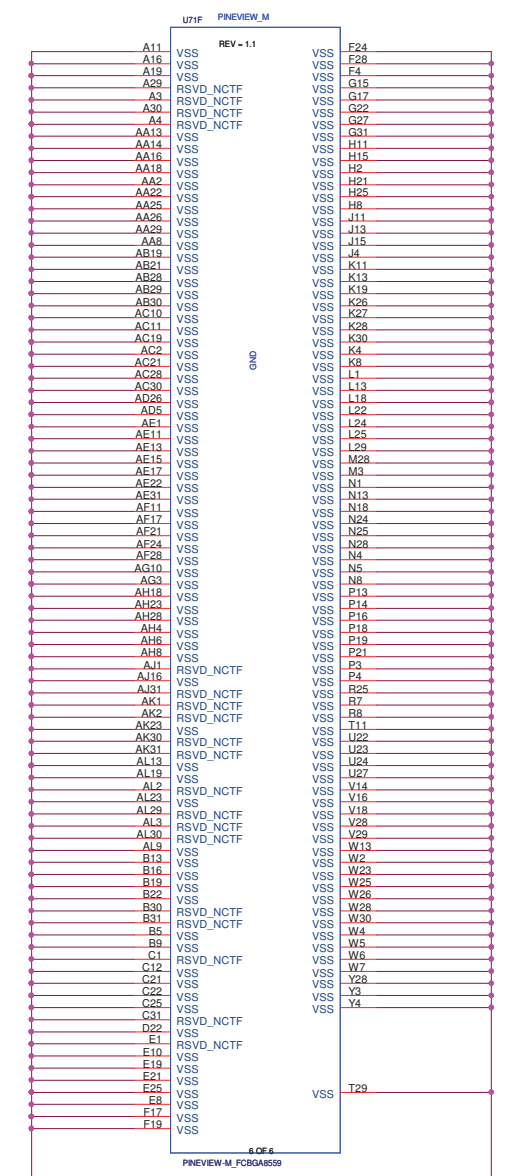
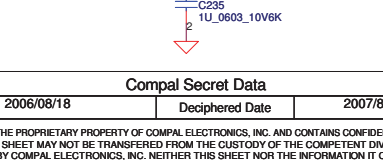
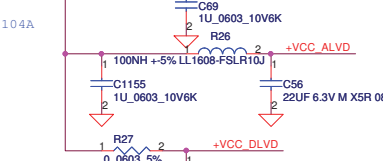
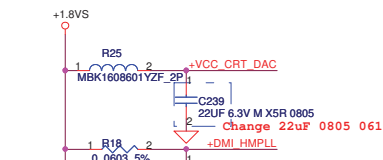
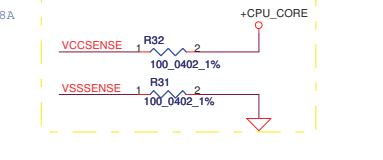
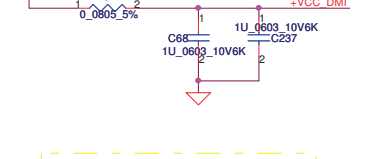
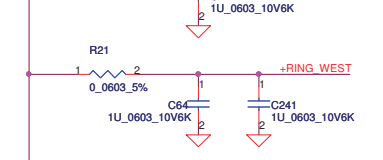
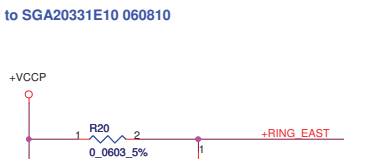
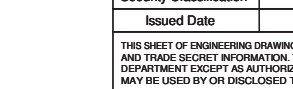
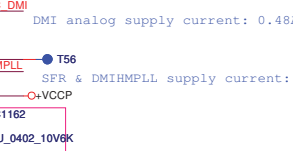
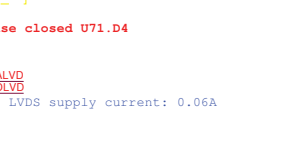
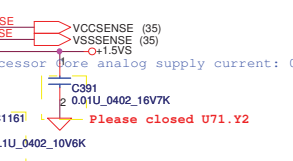
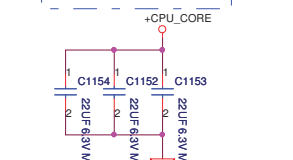
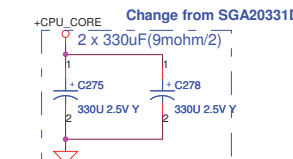
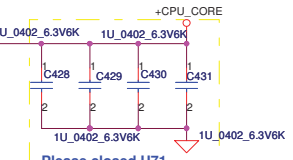
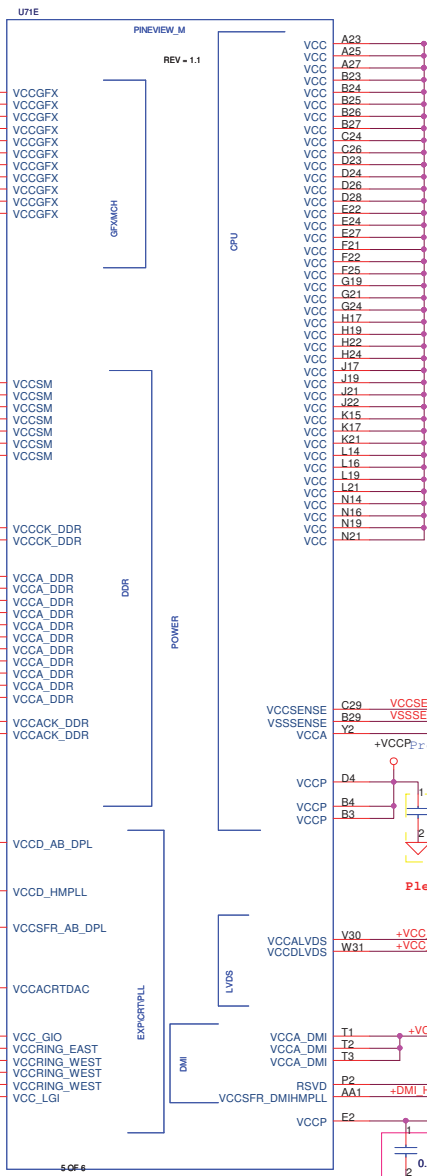
DDR supply current 2.27A



DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A



Modify to 2.2U 05/11  
Close Chipset pin  
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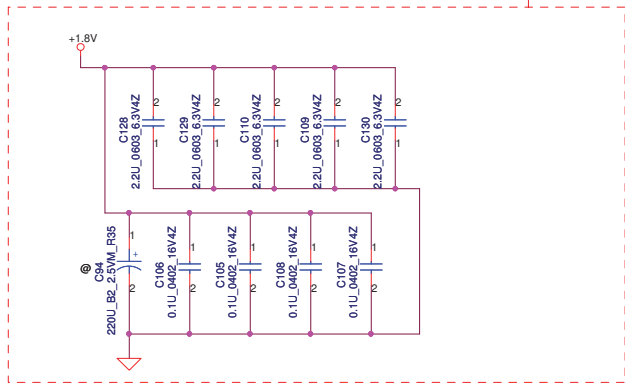
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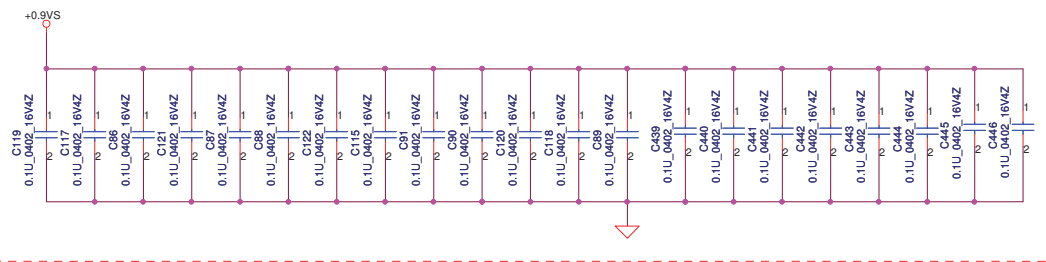
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- (4) DDR\_A\_DOS[0..7]
- (4) DDR\_A\_D[0..63]
- (4) DDR\_A\_DM[0..7]
- (4) DDR\_A\_DOS[0..7]
- (4) DDR\_A\_MA[0..14]

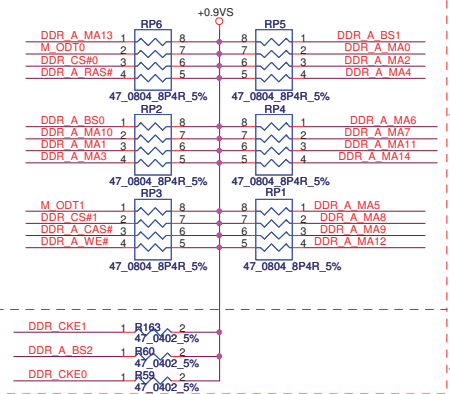
**Layout Note:**  
Place near JDIM1



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

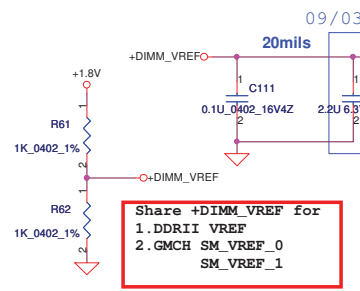


**Layout Note:**  
Place these resistor closely DIMMA, all trace length < 750 mil



**Layout Note:**  
Place these resistor closely DIMMA, all trace length Max=1.3"

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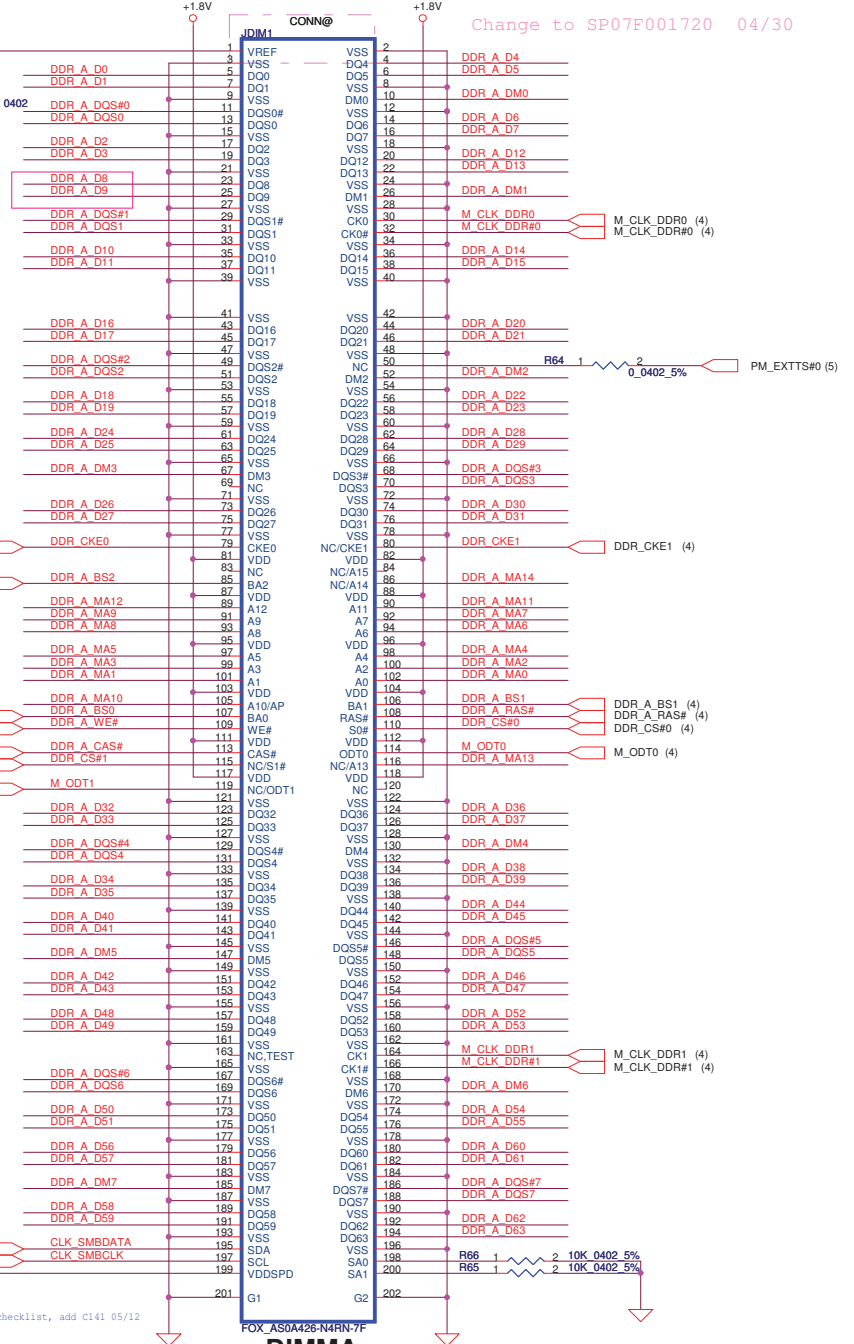


**Share +DIMM\_VREF for**  
1. DDRII VREF  
2. GMCH SM\_VREF\_0  
SM\_VREF\_1

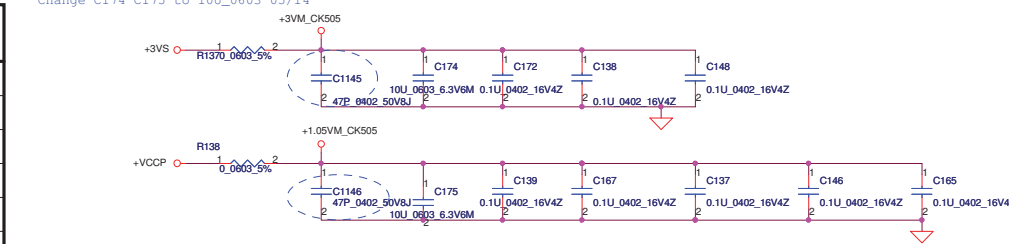
- (4) DDR\_CKE0
- (4) DDR\_A\_BS2
- (4) DDR\_A\_BS0
- (4) DDR\_A\_CAS#
- (4) DDR\_CS#1
- (4) M\_ODT1

- (8,17,18,26) CLK\_SMBDATA
- (8,17,18,26) CLK\_SMBCLK

Follow Intel Layout checklist, add C141 05/12

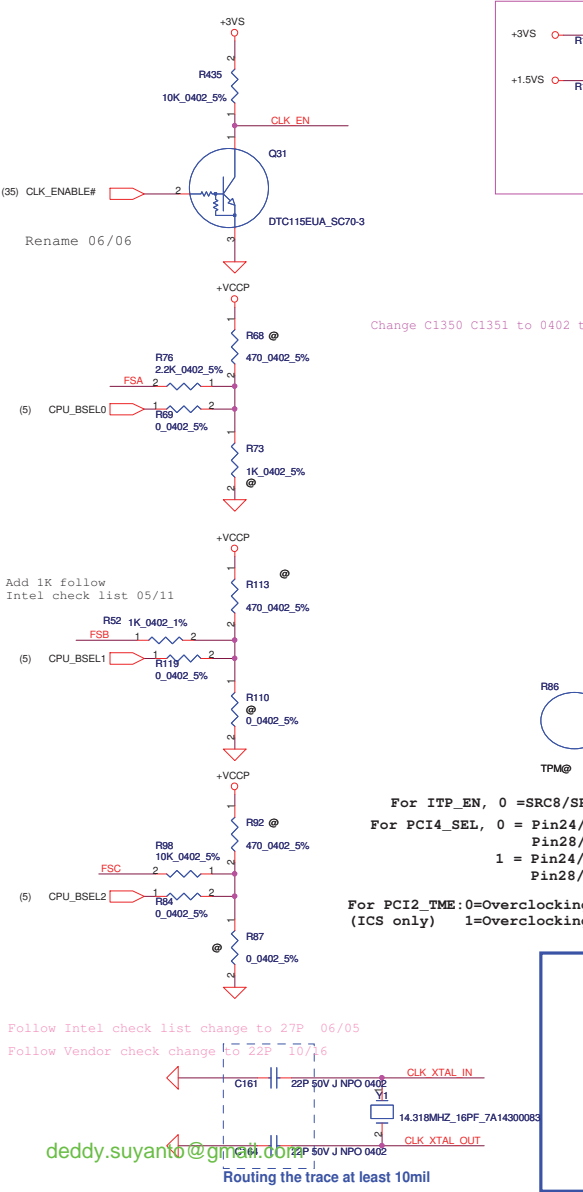
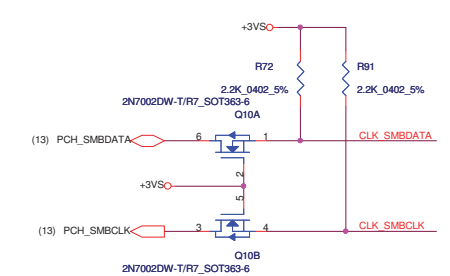


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

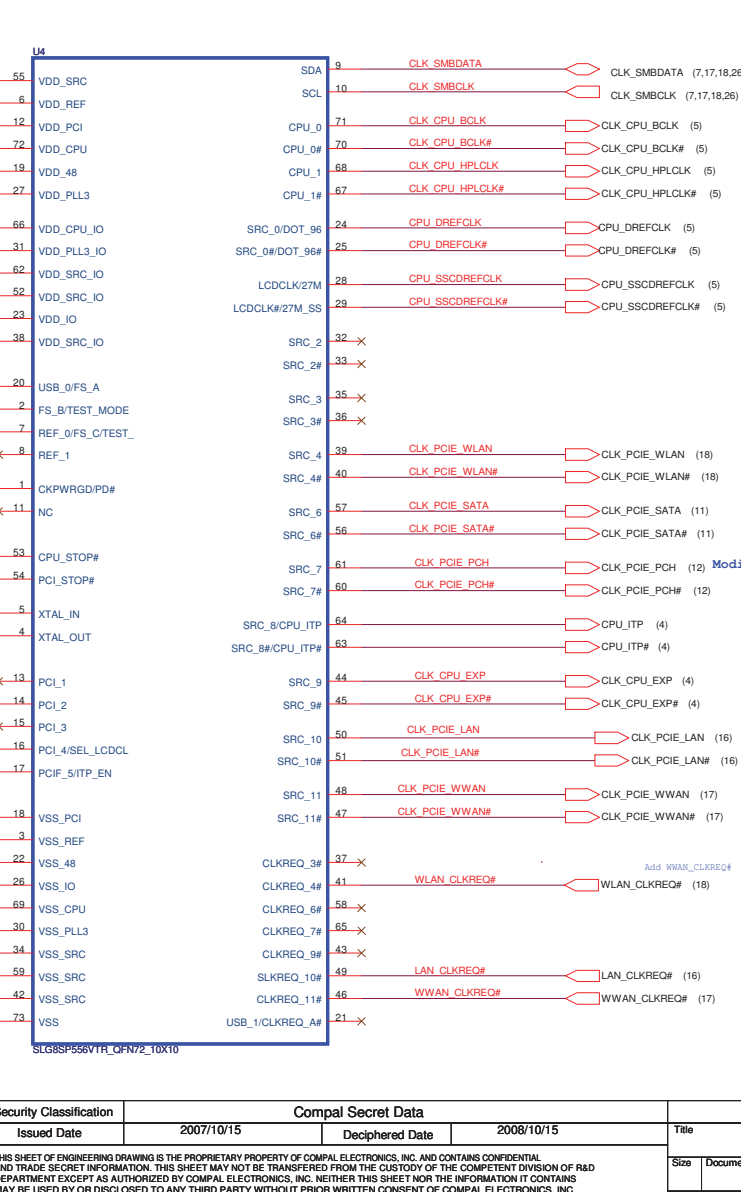
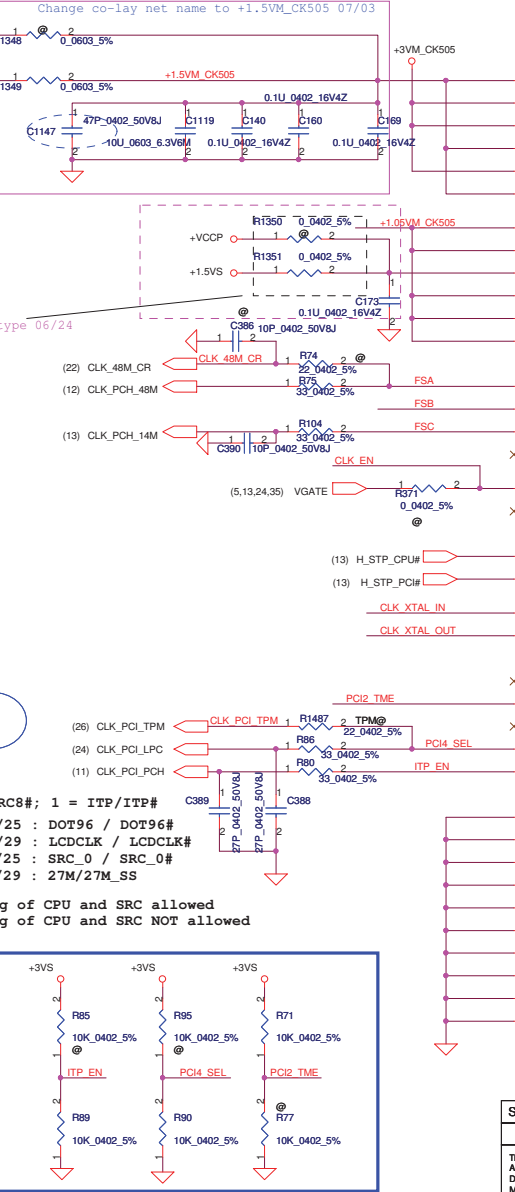


Add C1145 C1146 C1147 for EMI 06/12

### Low Power (Silego : SA00003H730) IDT SA00003H610



Routing the trace at least 10mil



#### SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

#### REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	PCIE_WWAN
REQ_A#	

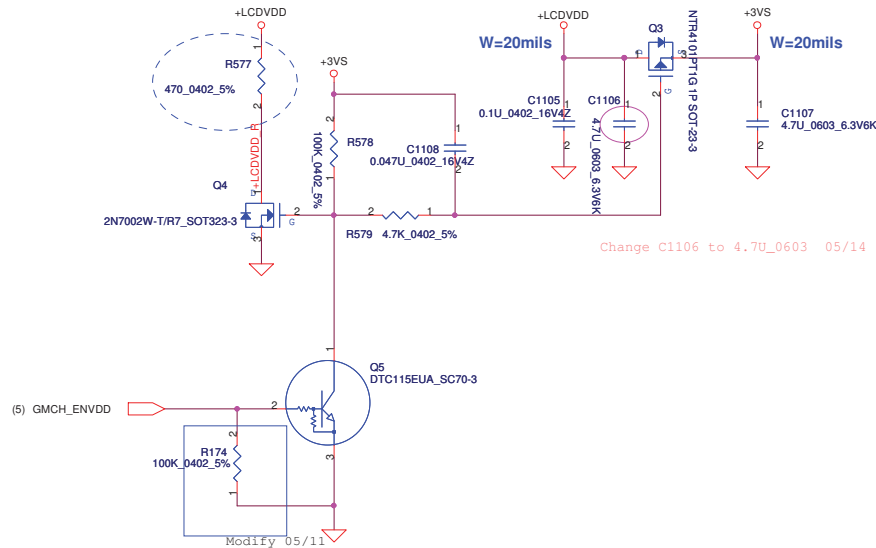
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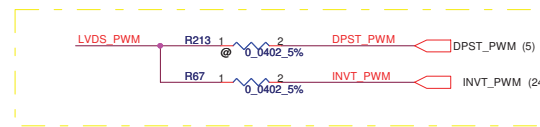
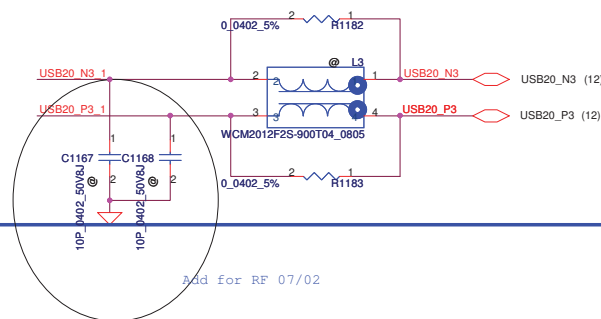
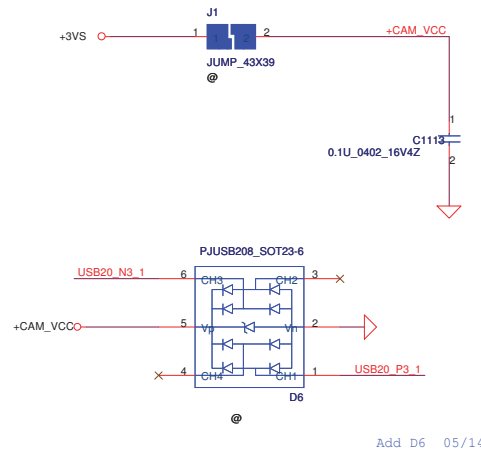
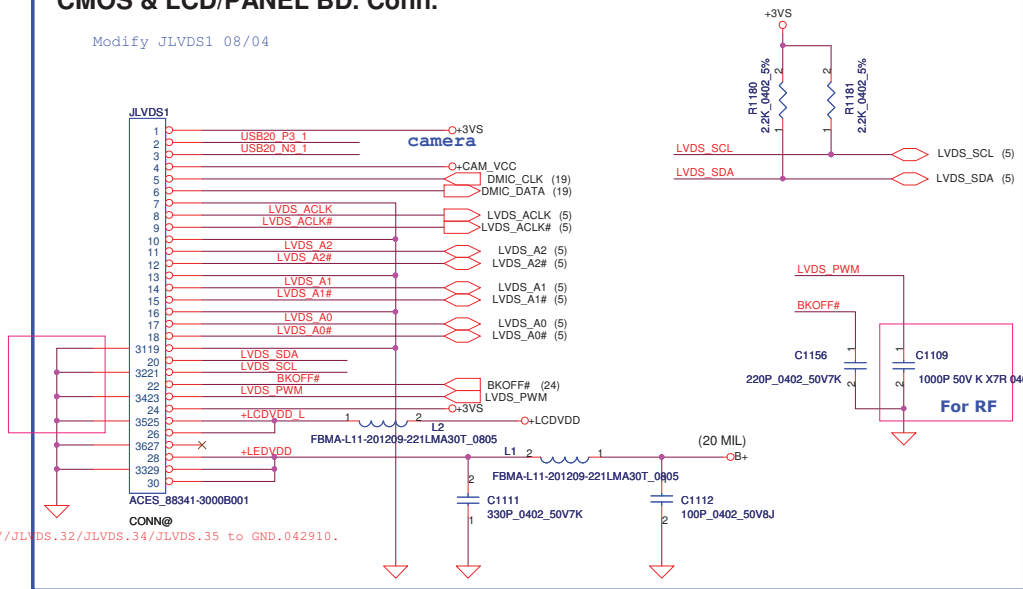
### LCD POWER CIRCUIT

Change R577 to 0402 SIZE 06/16

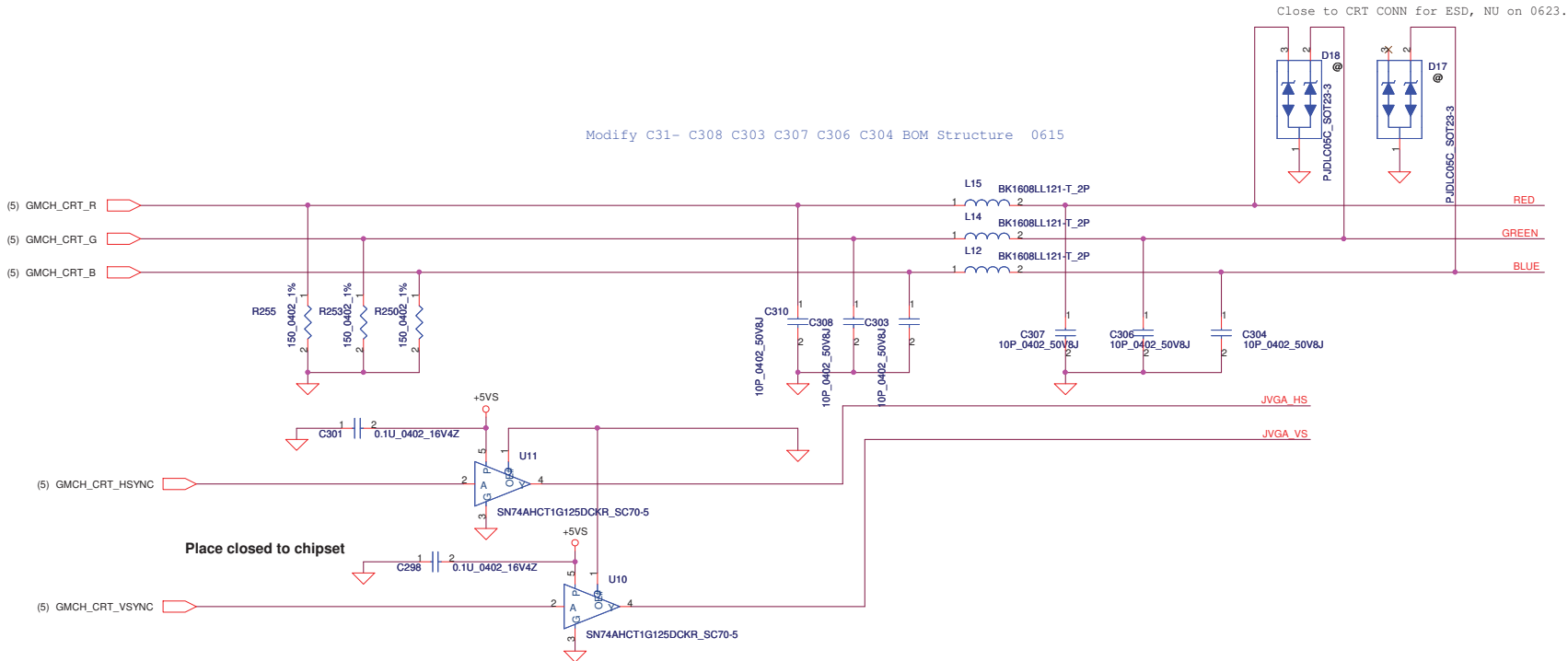


### CMOS & LCD/PANEL BD. Conn.

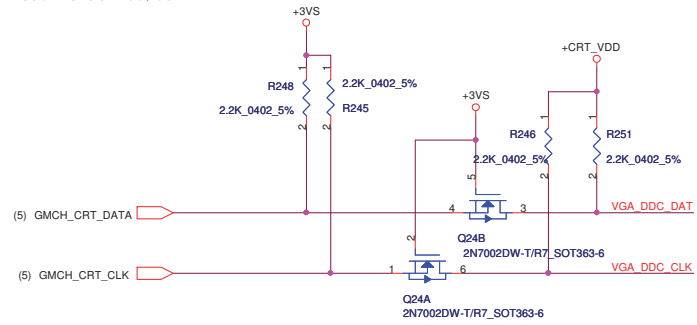
Modify JLVDS1 08/04



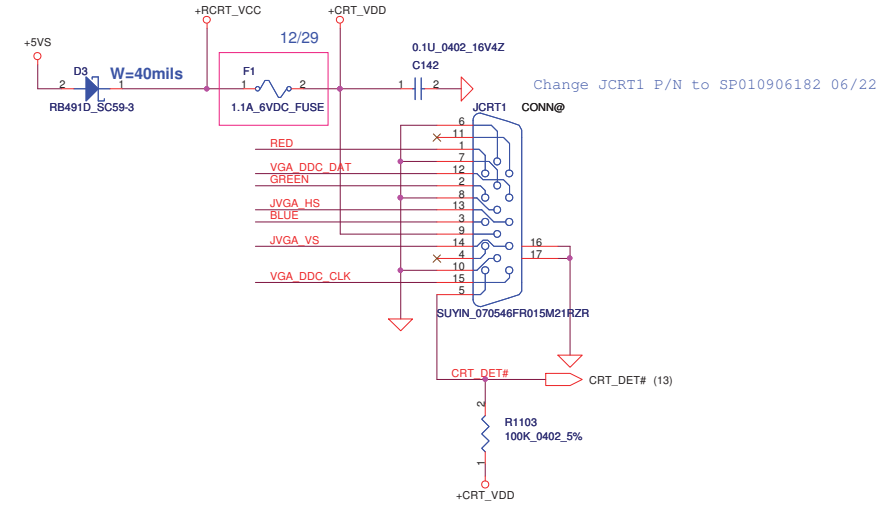
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				LVDS /INVERTER	
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				LA-6221P	
				Date:	Thursday, July 01, 2010
				Sheet	9 of 39
				Rev	1.0



Add R1283 R1284  
 Change R247 R249 to 10 ohm  
 Add @ on U10 U11 C301 C298 06/08

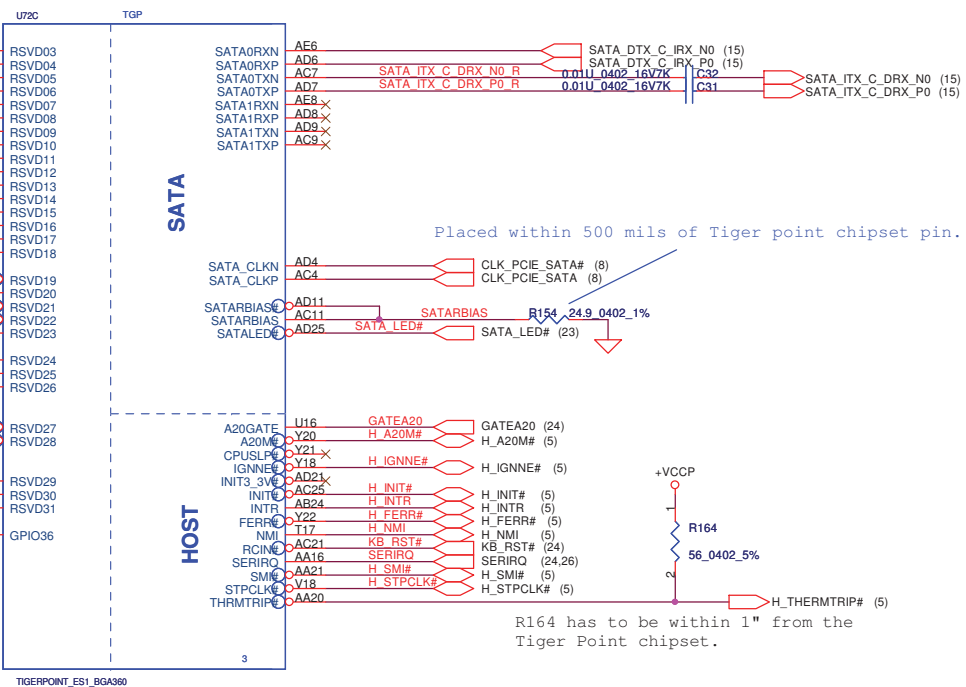
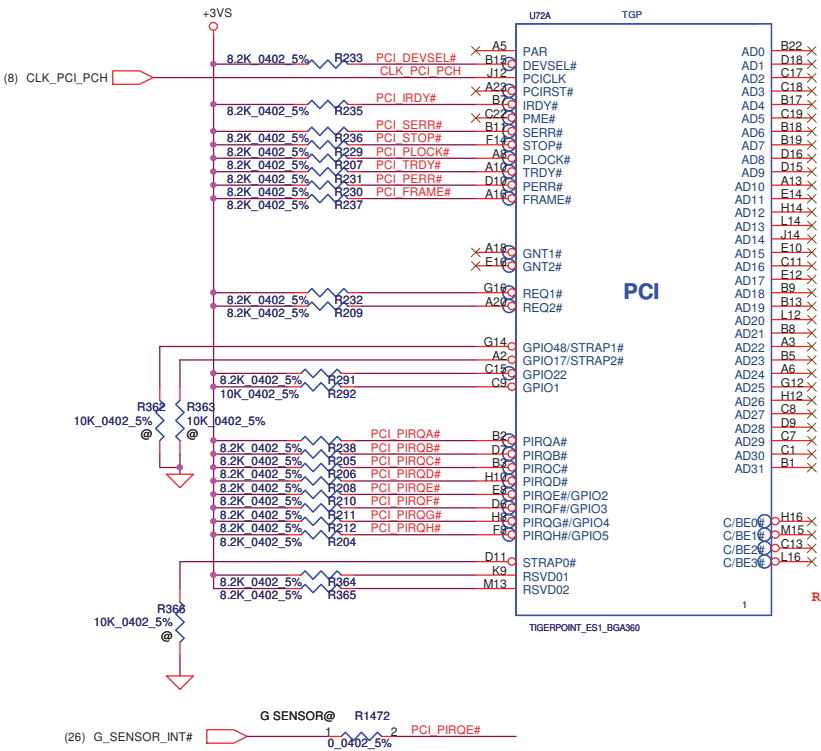
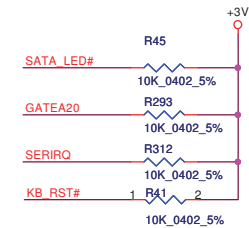
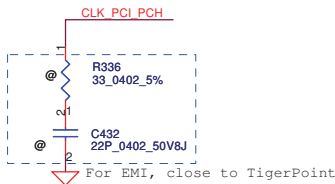


### CRT PORT



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				Date:	Thursday, July 01, 2010
				Sheet	10 of 39



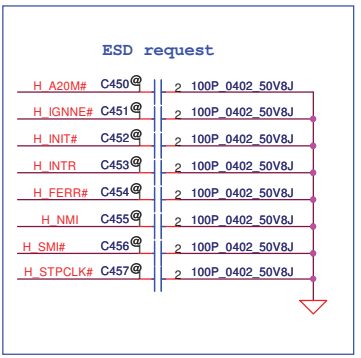
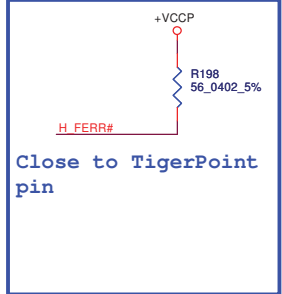
R294 be placed <200 mils to U72.AD23

Placed within 500 mils of Tiger point chipset pin.

R164 has to be within 1" from the Tiger Point chipset.



STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



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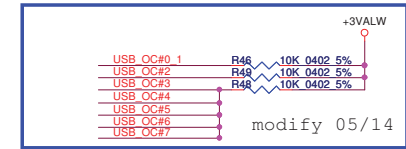
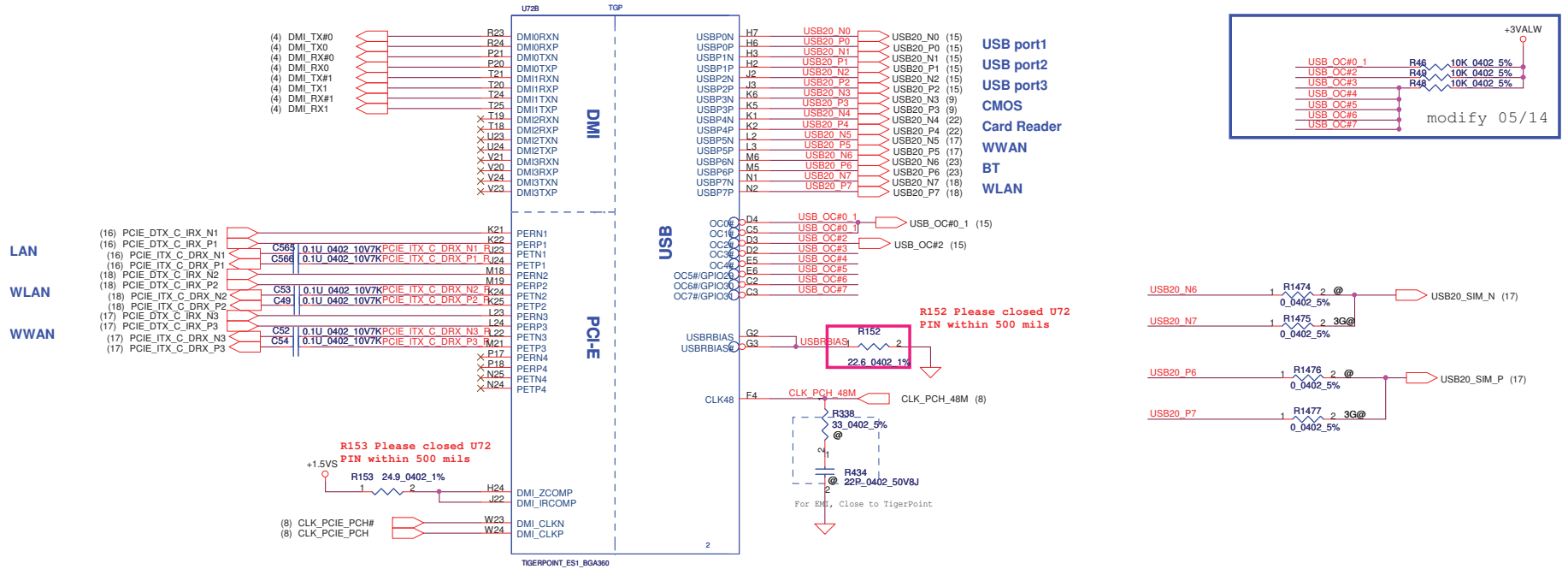
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				Tigerpoint(1/4)	
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				LA-6221P	
Date:	Thursday, July 01, 2010	Sheet	11	of	39
				Rev	1.0

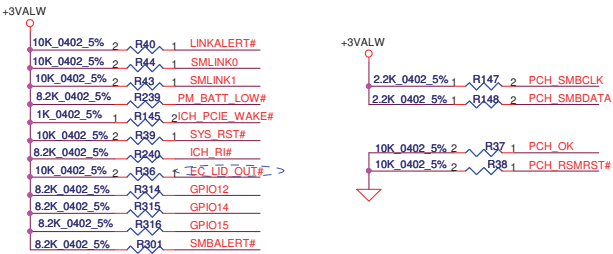
PCIE Port List

1	LAN
2	WLAN
3	WWAN
4	

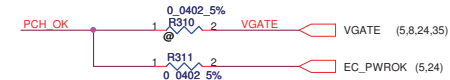
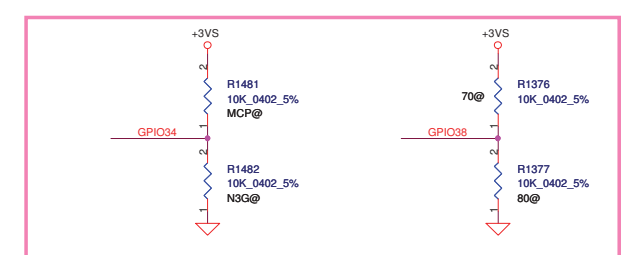
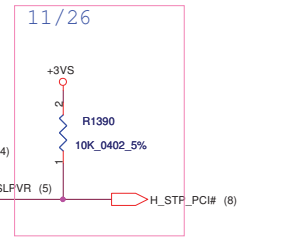
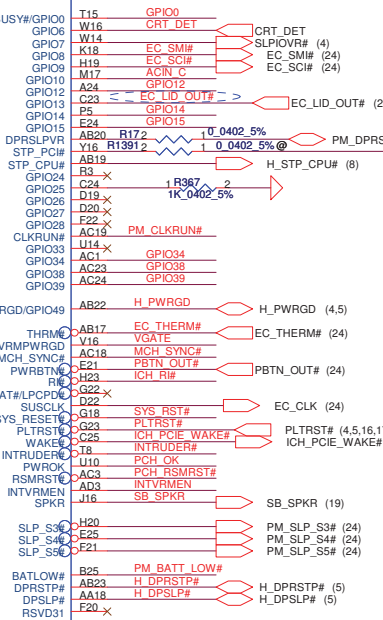
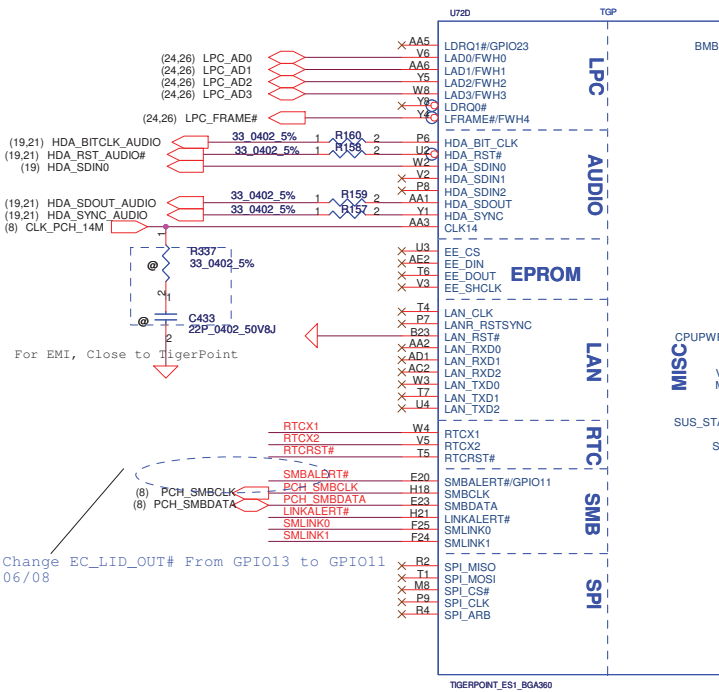
USB Port List

0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX

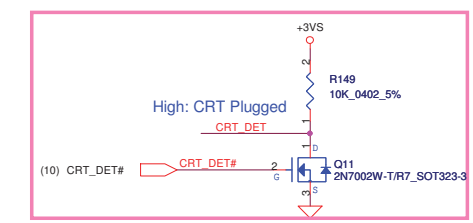




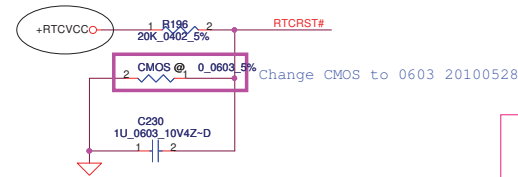
follow-EC check list change to pull down 060810



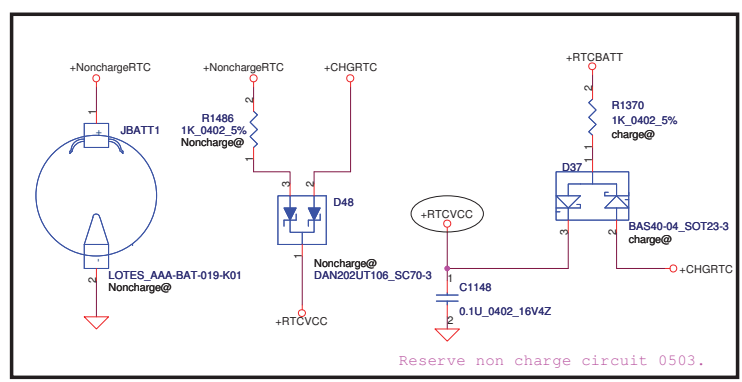
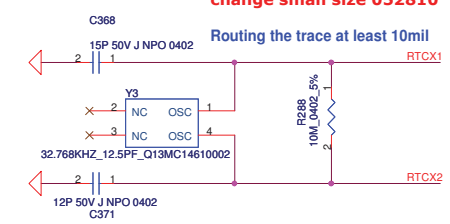
Change CRT\_DET# From Page 10 to Page 13



Change EC\_LID\_OUT# From GPIO13 to GPIO11 06/08



change small size 052810



Reserve non charge circuit 0503.

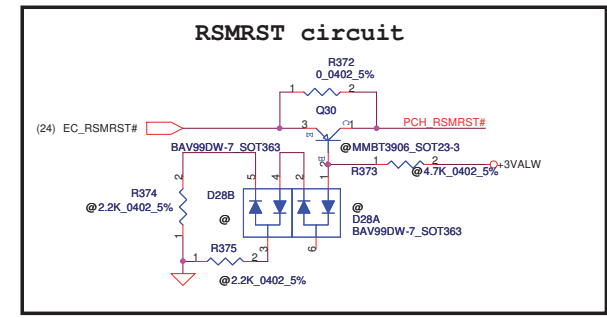
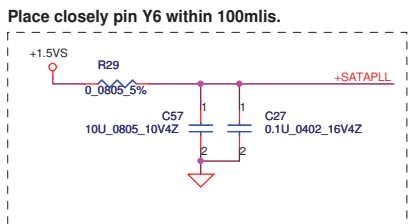
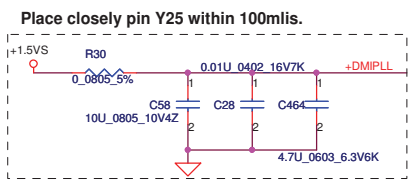
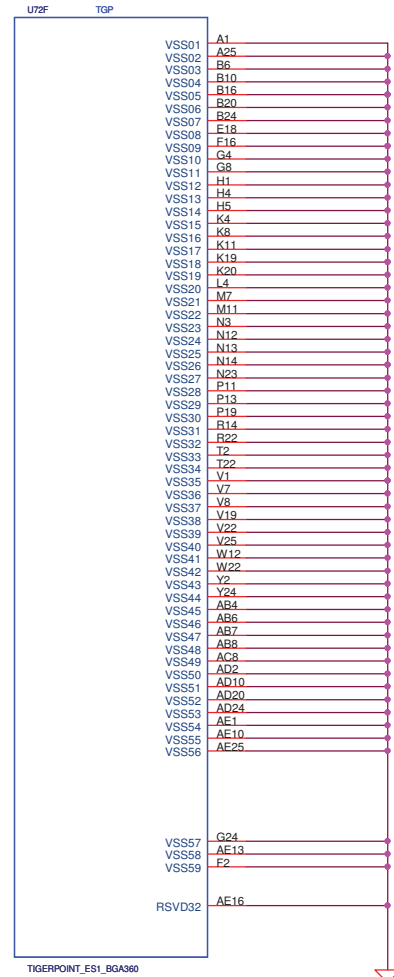
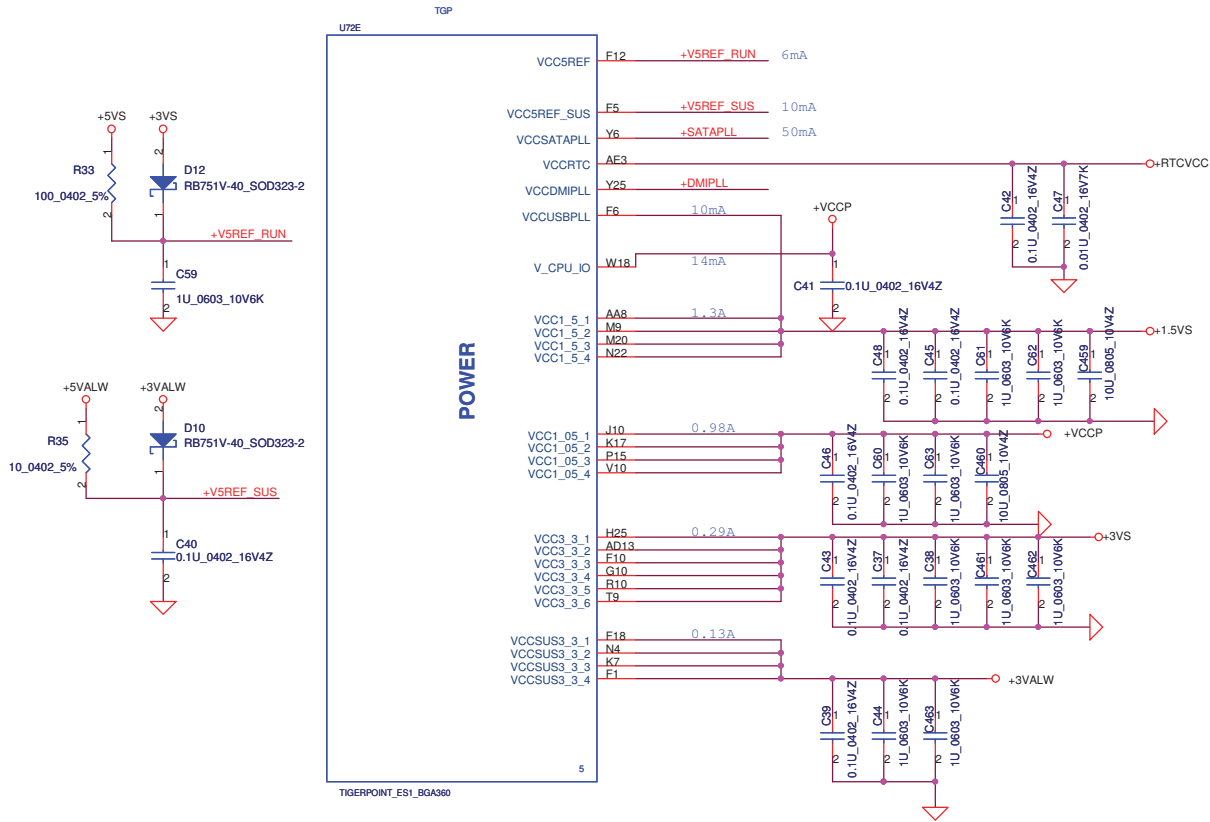


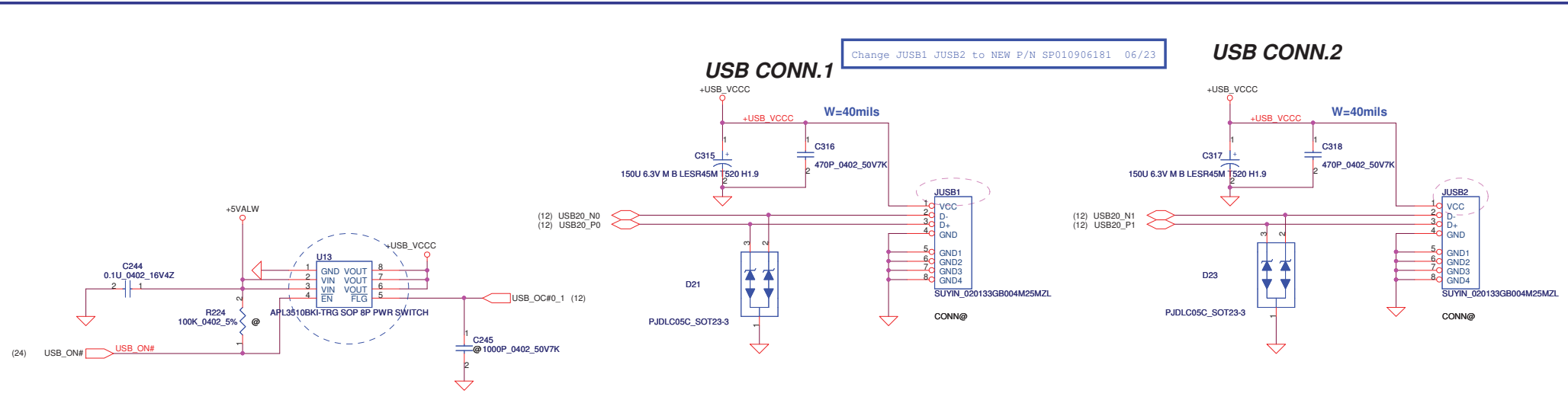
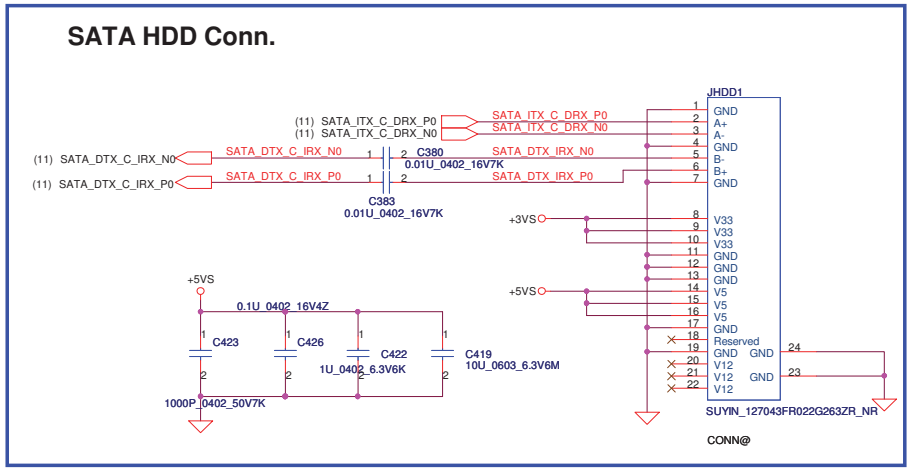
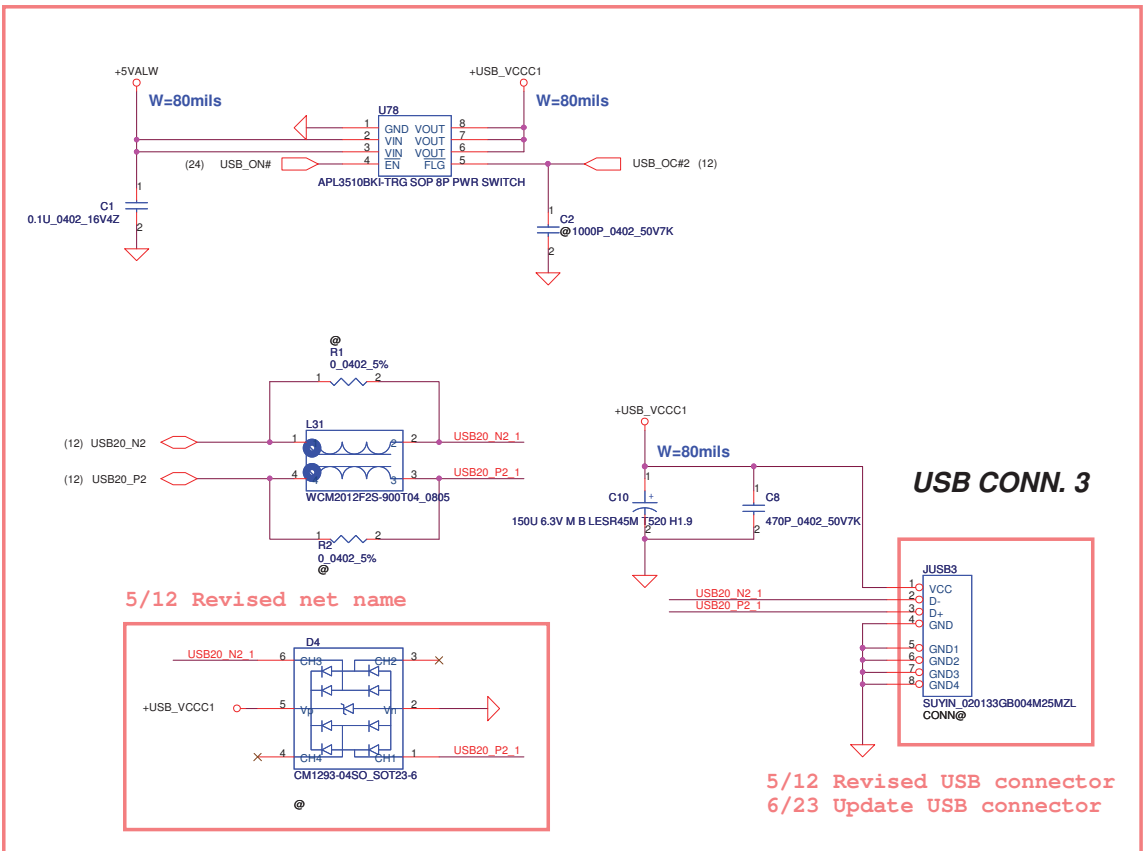
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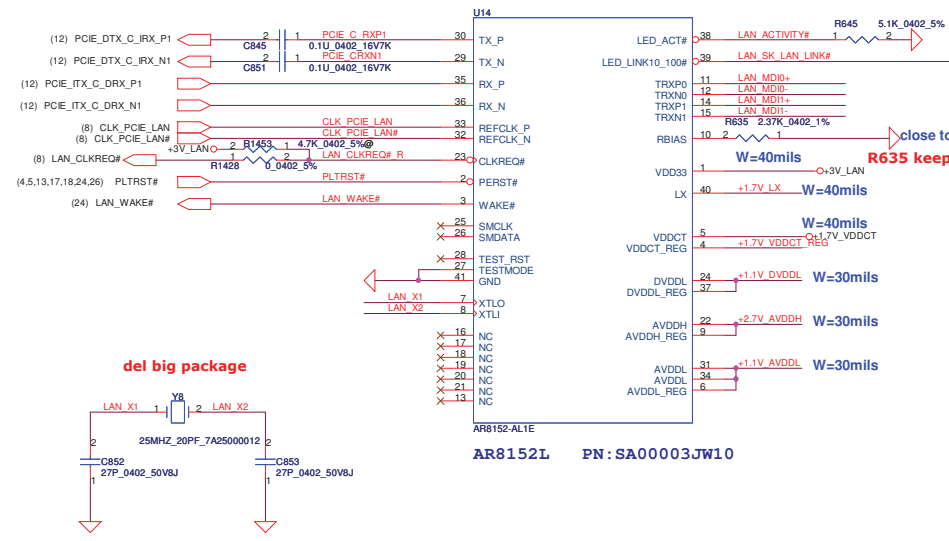
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Issued Date	2009/04/15	Deciphered Date	2010/04/15	Title Tigerpoint(4/4)	
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Date:	Thursday, July 01, 2010	Sheet	14	of	39
Rev	0.1				



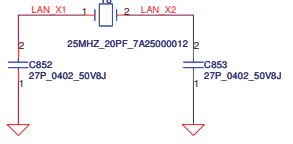
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				LA-6221P		
				Date:	Thursday, July 01, 2010	Sheet 15 of 39

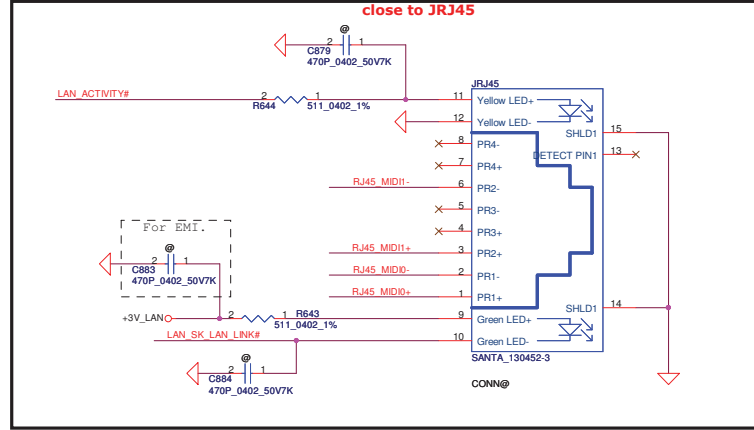
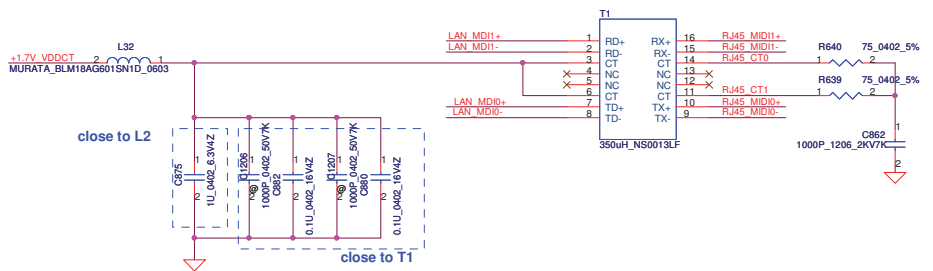
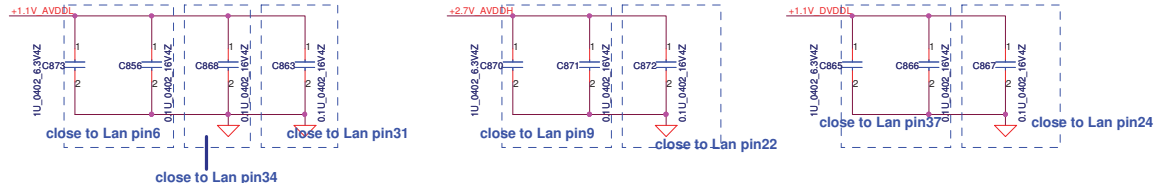
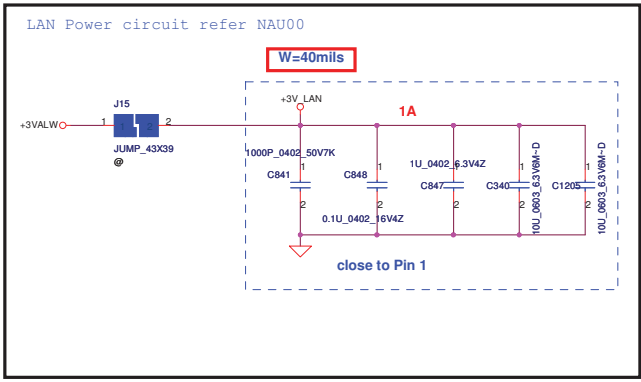
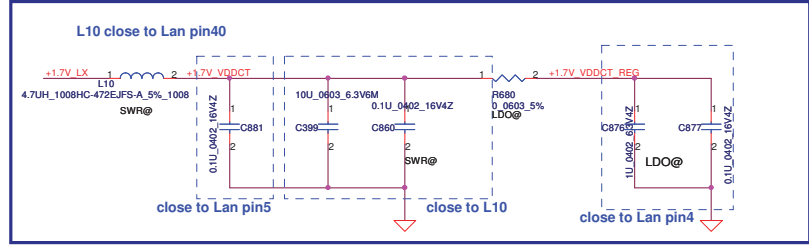
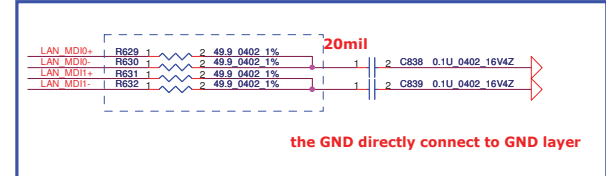
Change LAN chip to AR8152-L for NAV70/80 DDR3 2010/01/22



del big package



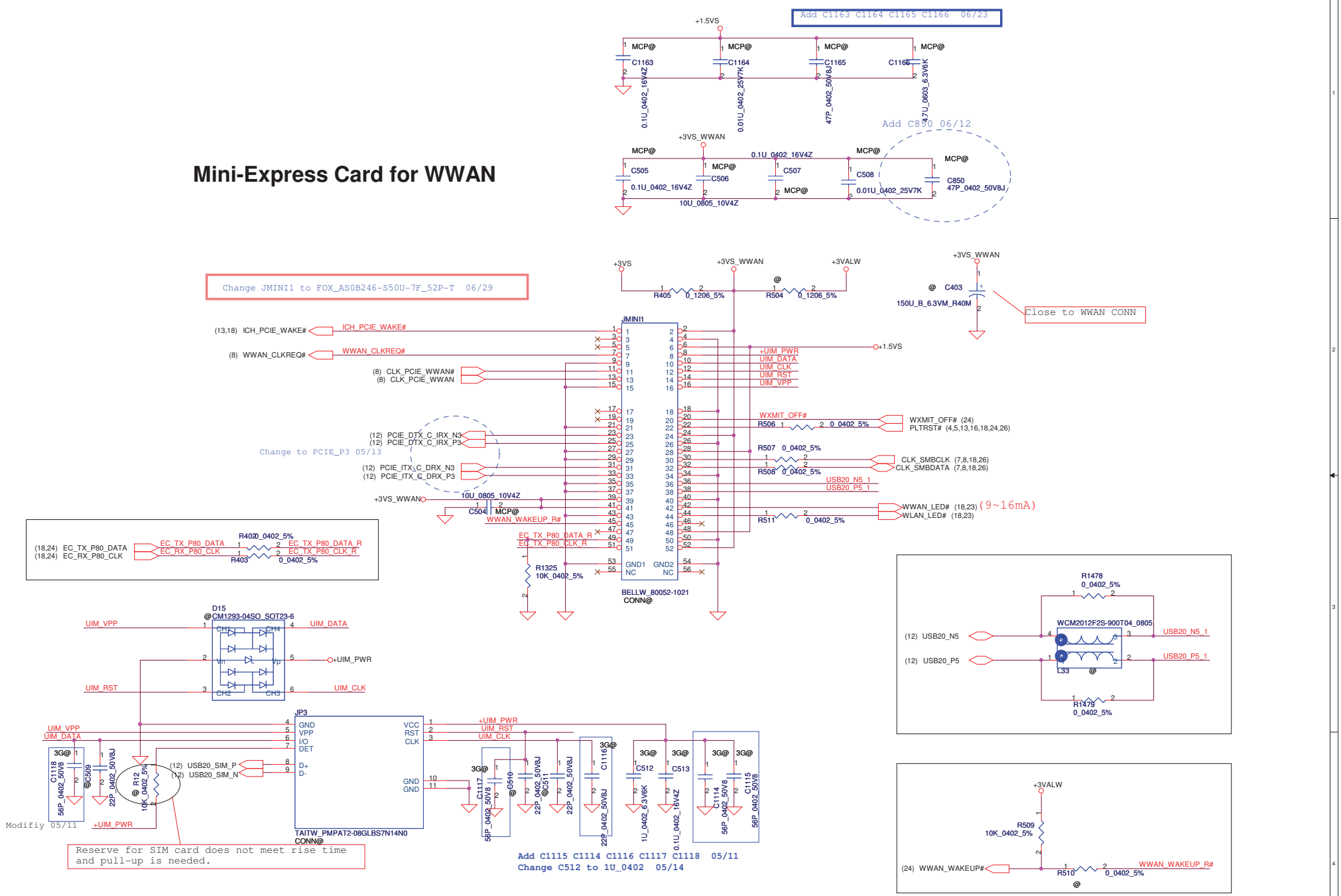
Switch mode:由+1.7V\_LX供給+VDDCT pin39 need to pull high resistor of 5.1k  
LDO mode:由+1.7V\_VDDCT\_REG供給+VDDCT pin39 need to pull low resistor of 5.1k



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Size	Custom	Document Number	LA-6221P	Rev
Date:	Thursday, July 01, 2010	Sheet	16	of 39



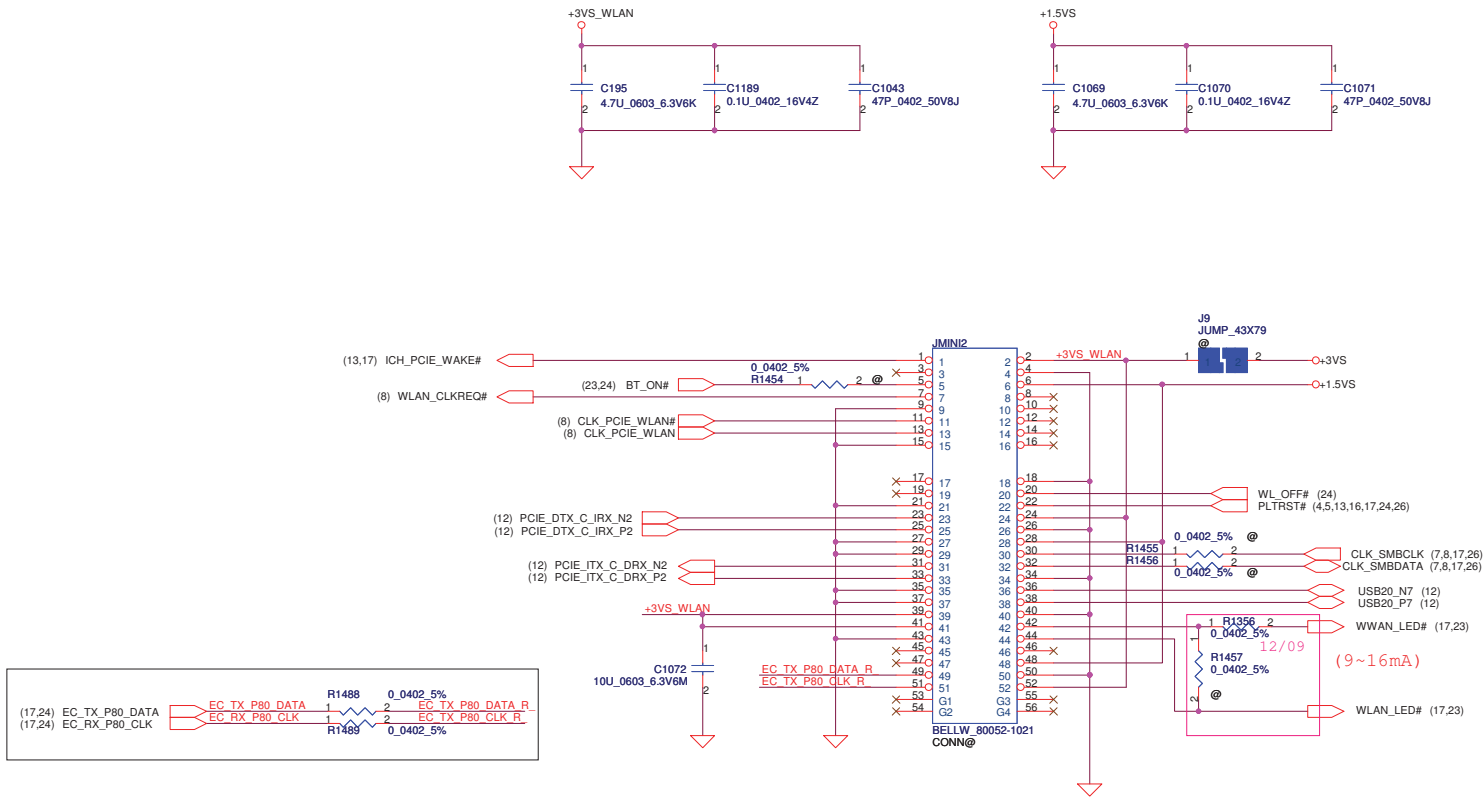
# Mini-Express Card for WWAN



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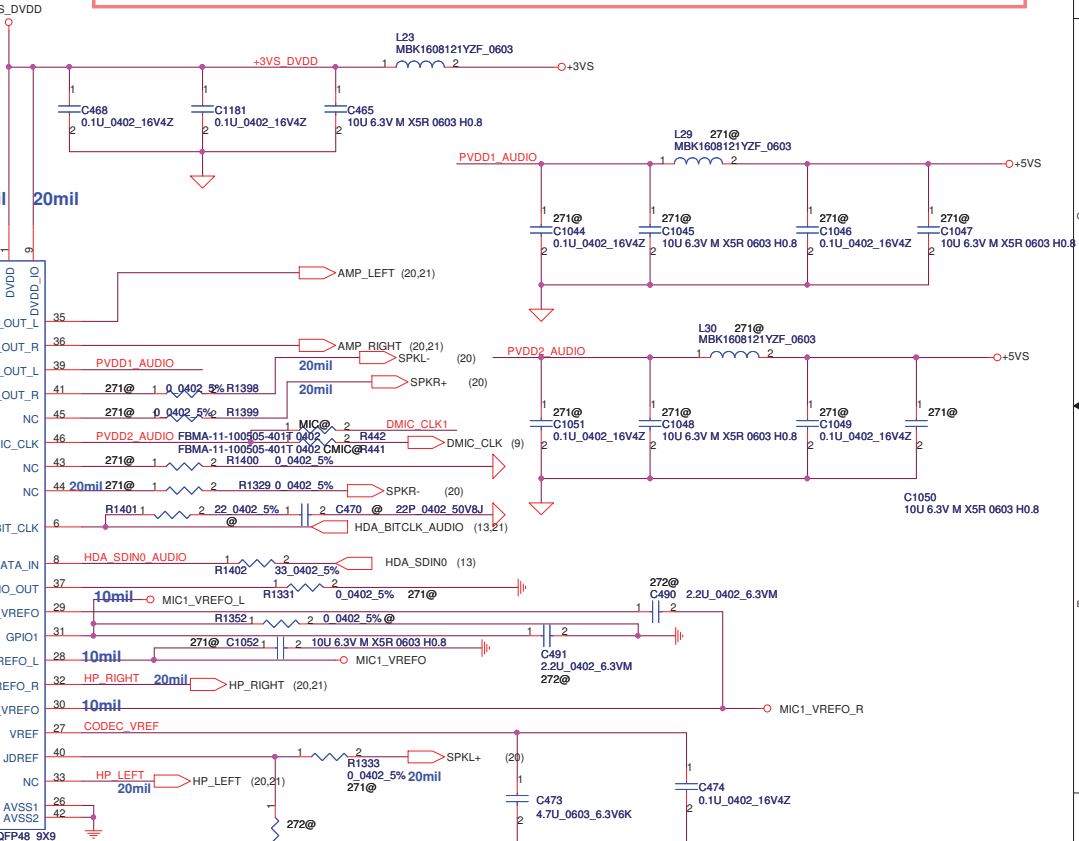
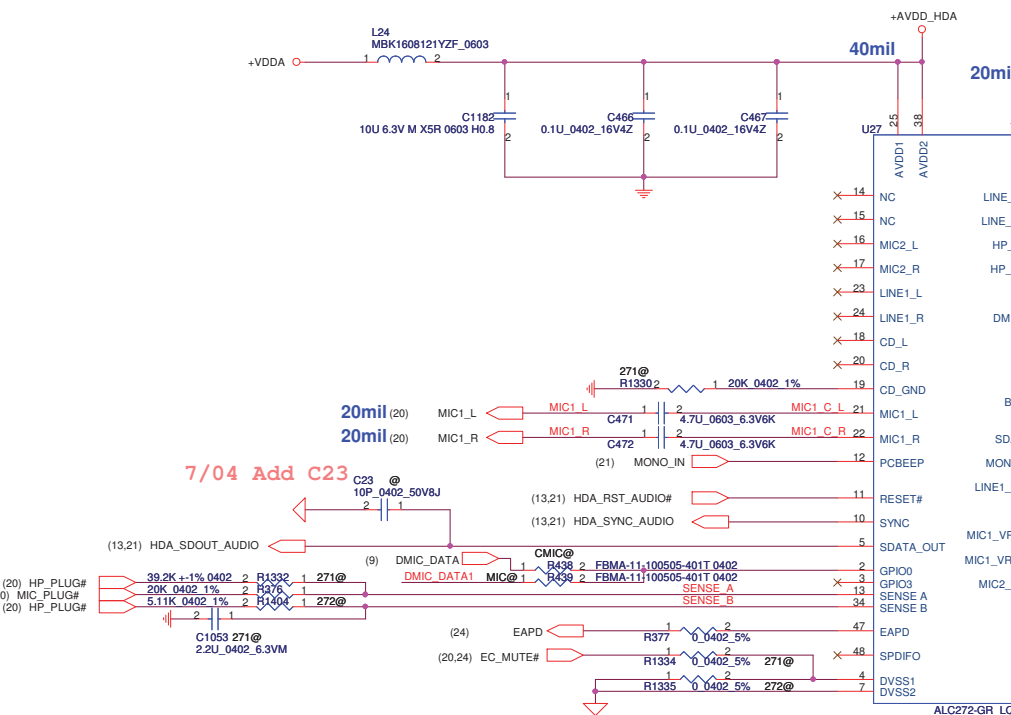
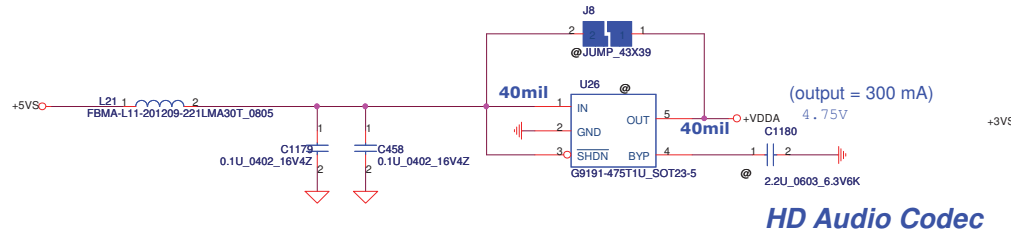
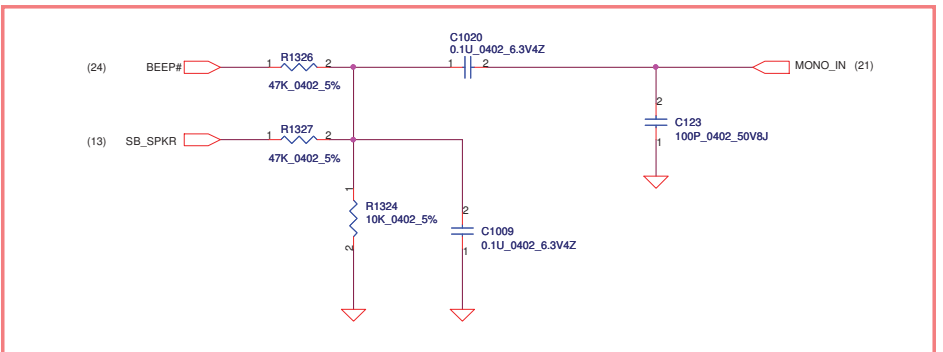
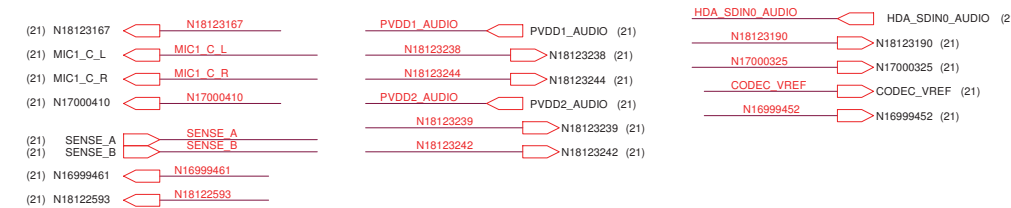
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	Mini-Card
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				Date	Thursday, July 01, 2010
				Sheet	17 of 39
				File	0.2
				LA-6221P	

# Mini-Express Card for WLAN

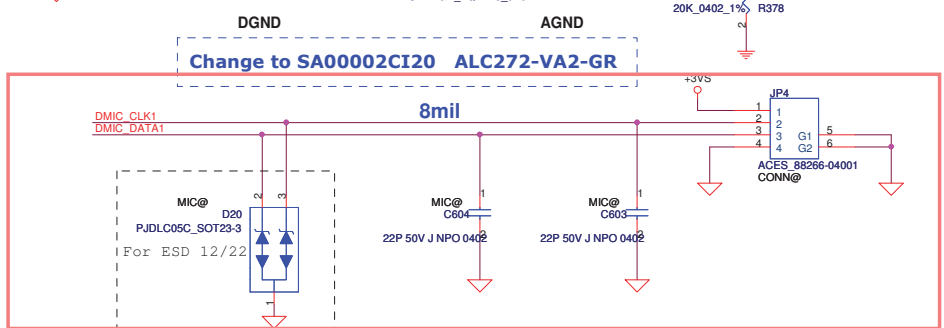


5/12 Update WLAN connector(the same as KAV60)  
 6/1 Revised 37、39、41、42、43 to NC  
 6/12 Update connector to DC040006S00  
 6/26 Update JMINI1 footprint  
 7/01 update pin 23,25,31,33

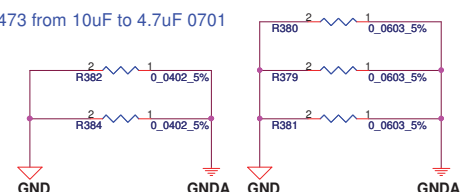
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Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	
				WLAN	
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				Date:	Thursday, July 01, 2010
				Sheet	18 of 39
				Rev	0.2



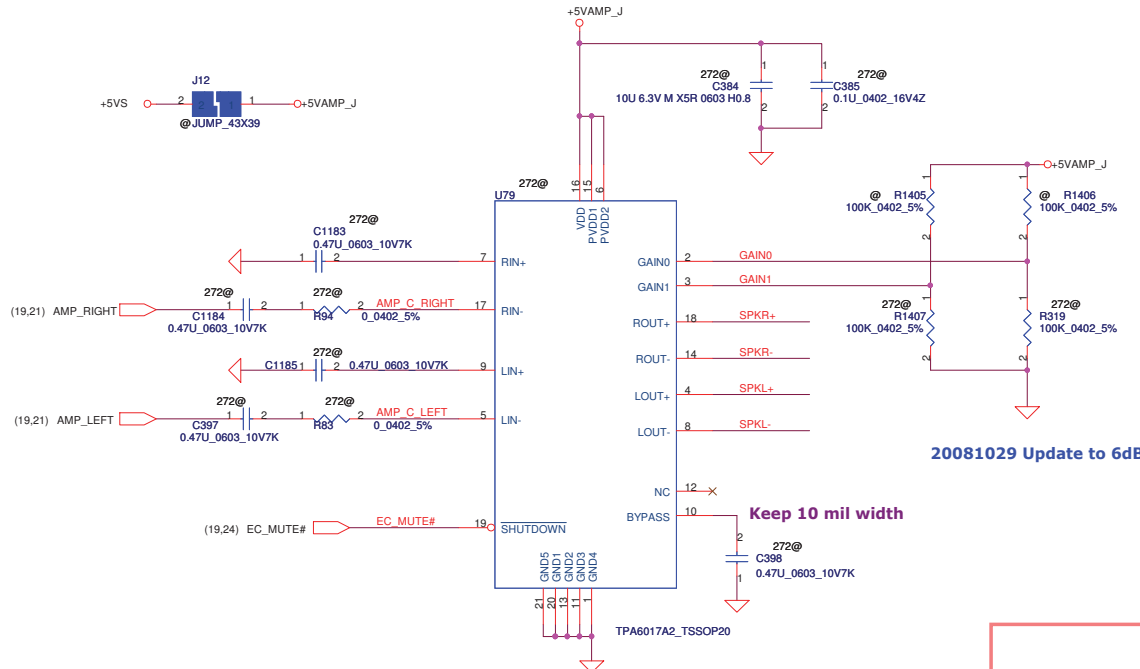
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



change C473 from 10uF to 4.7uF 0701

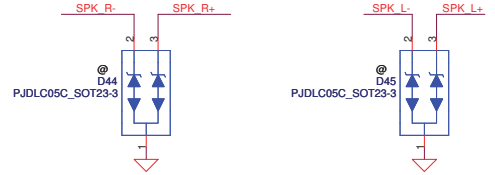
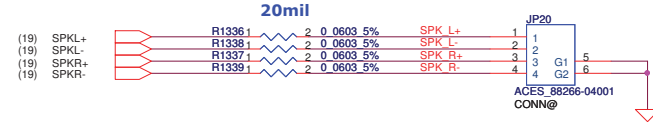


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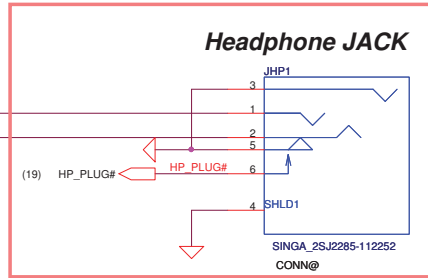
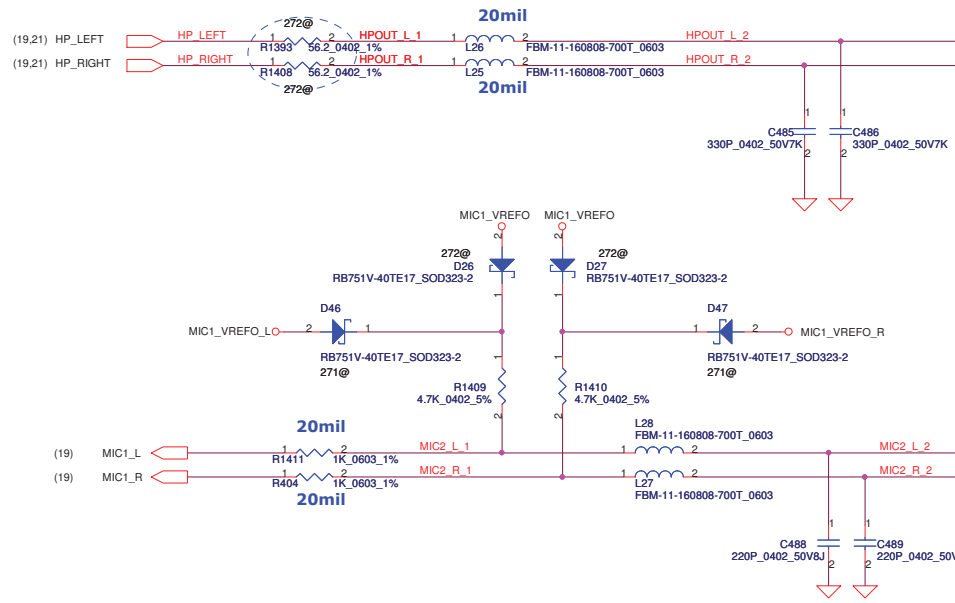


20081029 Update to 6dB

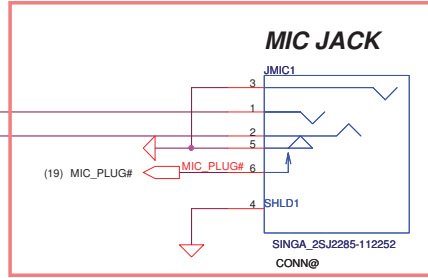
### Int. Speaker Conn.



NU D44 & D45 0623



6/19 Update Headphone connector

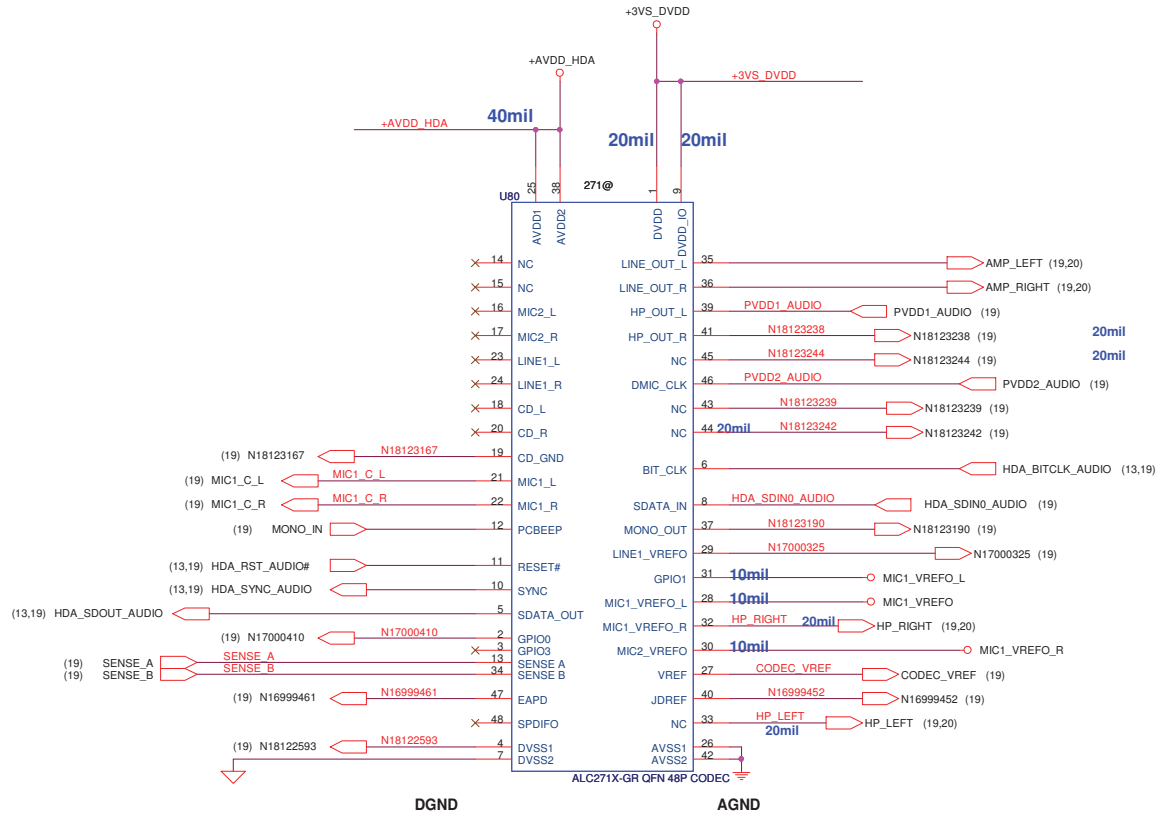


6/19 Update MIC connector

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Issued Date	2006/08/05	Deciphered Date	2007/8/18	Amplifier & Audio Jack	
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				LA-6221P	Rev 0.2
Date: Thursday, July 01, 2010				Sheet 20	of 39

# HD Audio Codec

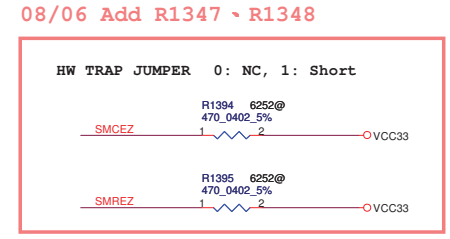
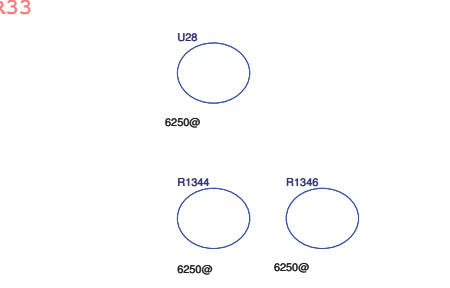
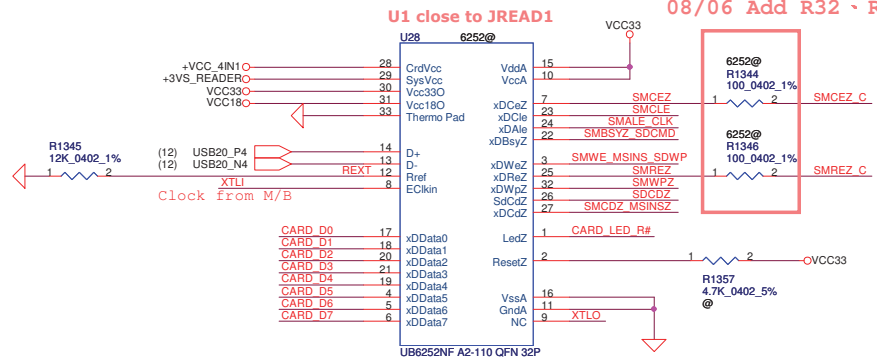
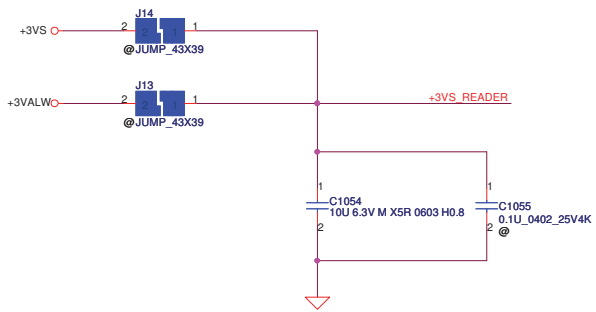


DGND AGND

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

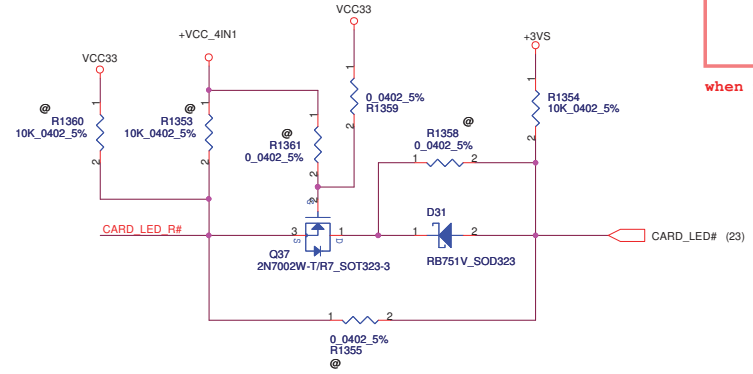
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				Document Number		0.2
				LA-6221P		
				Date:	Thursday, July 01, 2010	Sheet 21 of 39

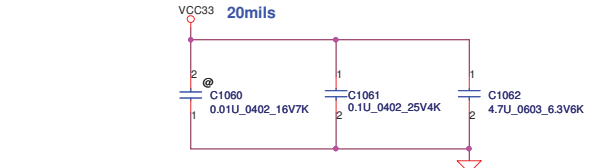
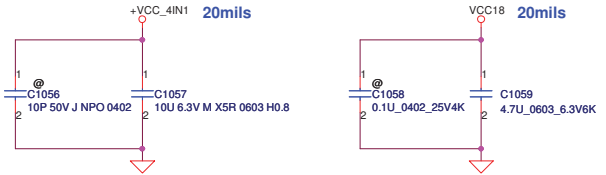


when you use UB6250 , R1347 - R1348 is NC

If use external crystal (Y4), U1 will change UB6252

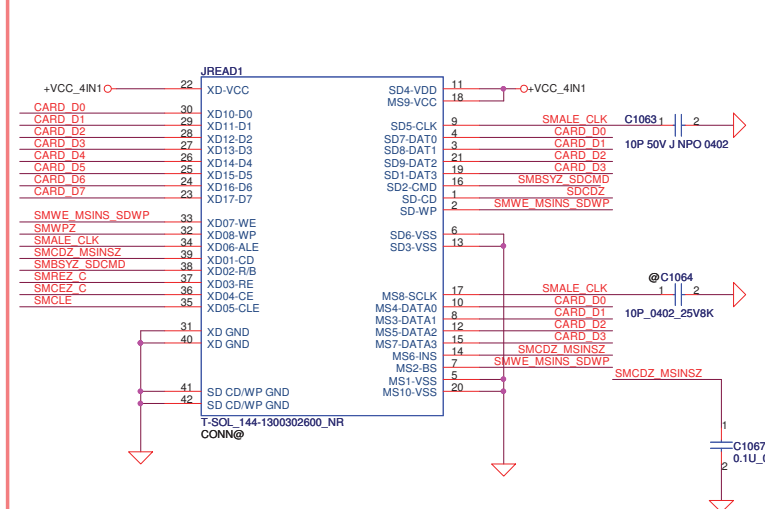


C1056 - C1057 close to U1

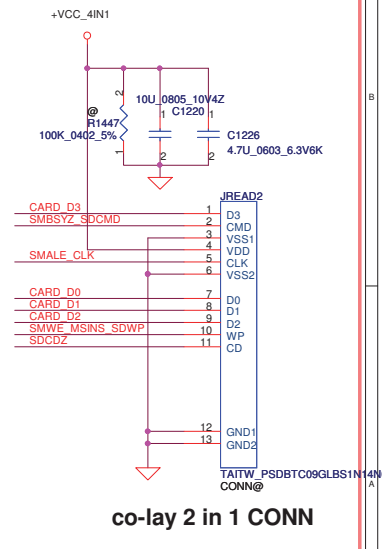


07/02 Revised C1053 to 0.01u ByPass Capacitors

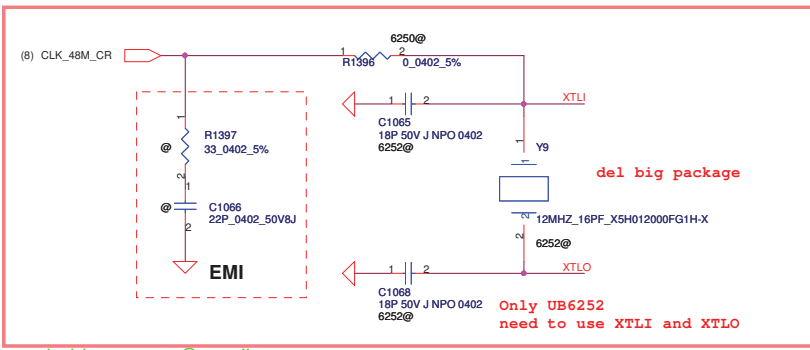
07/02 Update JREADER1



Card Reader Connector



4/30 Add CLK\_SD\_48M



Only UB6252 need to use XTLI and XTLO

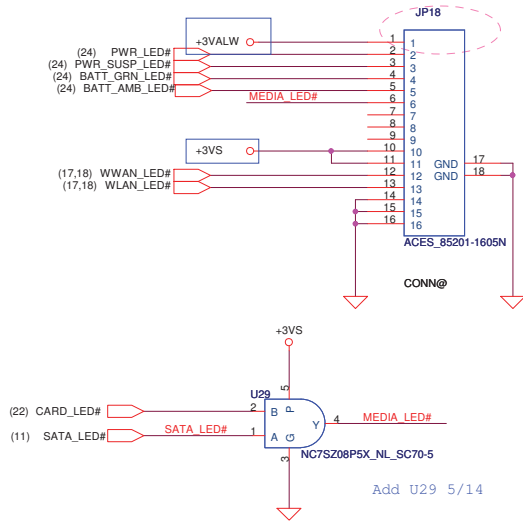
Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/22	Deciphered Data	2009/11/20	Compal Electronics, Inc.	
				Card reader	
				LA-6221P	
				Rev 0.1	
				Date: Thursday, July 01, 2010	
				Sheet 22 of 39	

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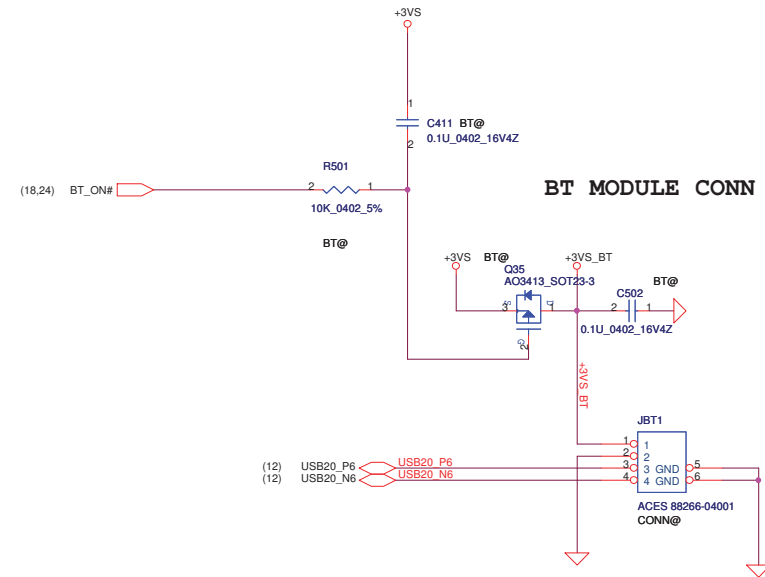
### LED PCB CONN

#### ADD LED PCB CONN 06/12

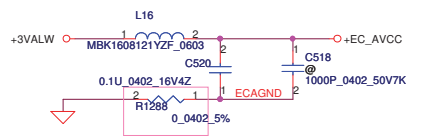
Change JP18 to NEW P/N 06/23  
09/03 Change +5VALW , +5VS to +3VALW +3VS



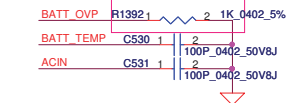
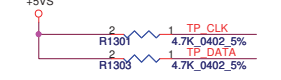
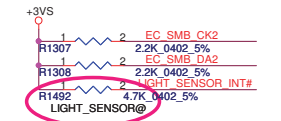
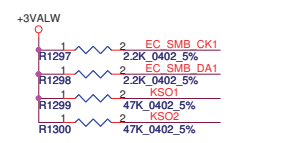
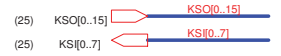
### BT MODULE CONN



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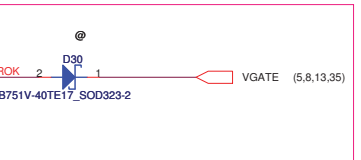
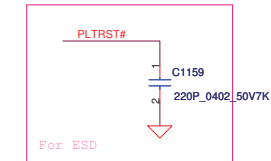
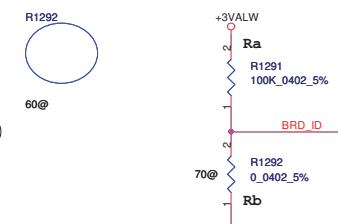
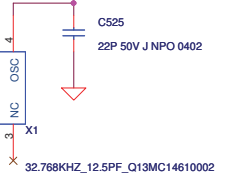
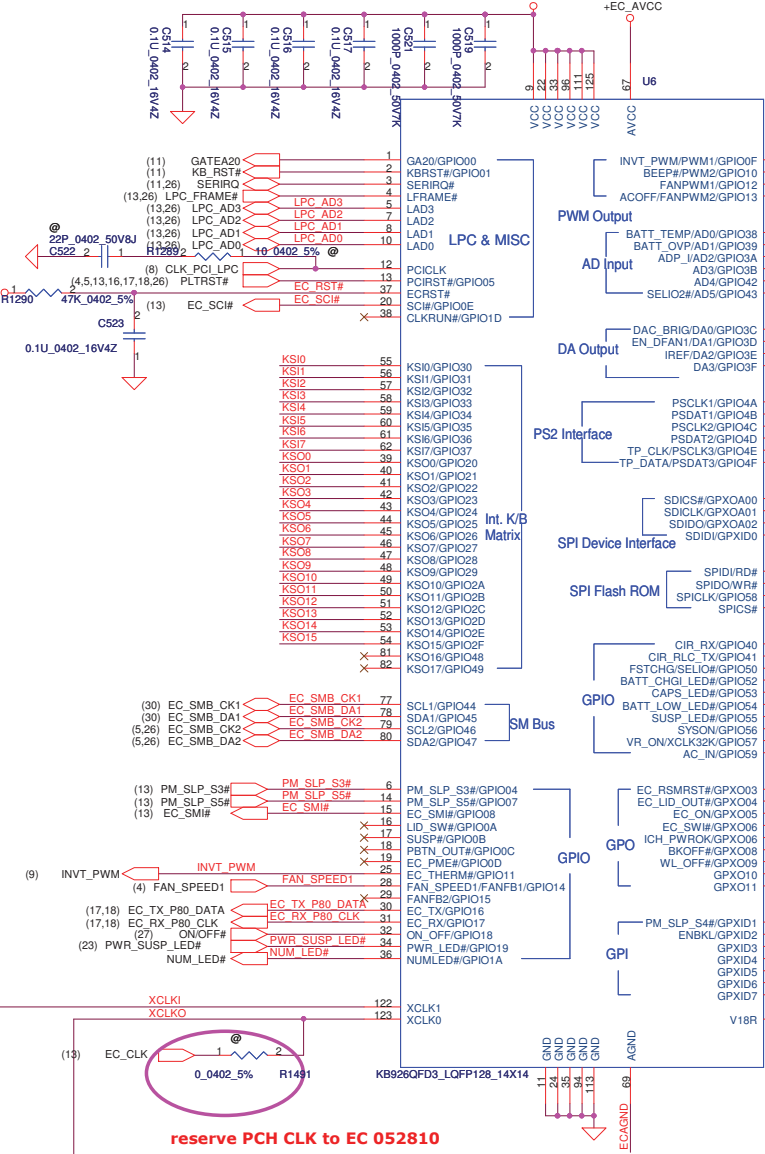
Change to R\_0402 05/14



	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF#	v	v		Low

Swap to WLAN

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#



change small size 052810

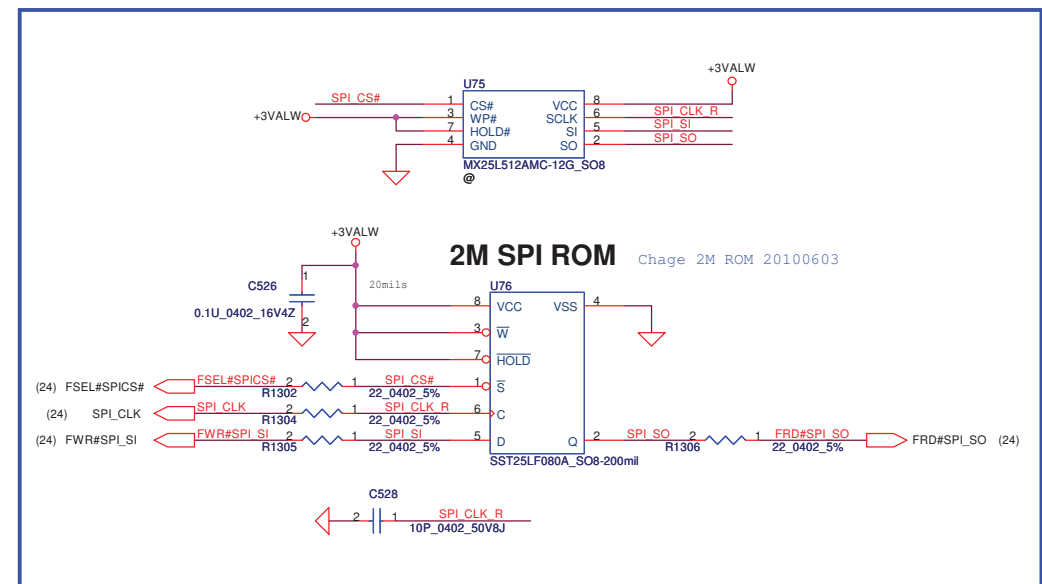
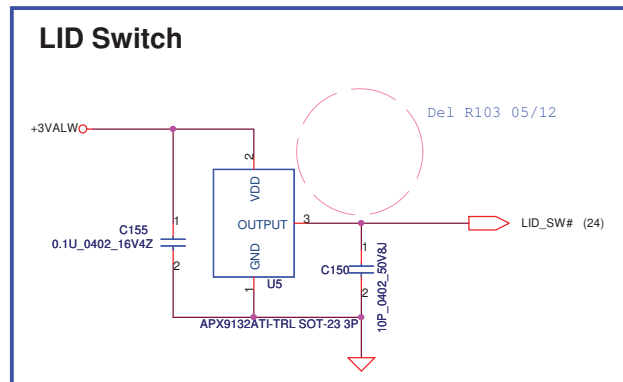
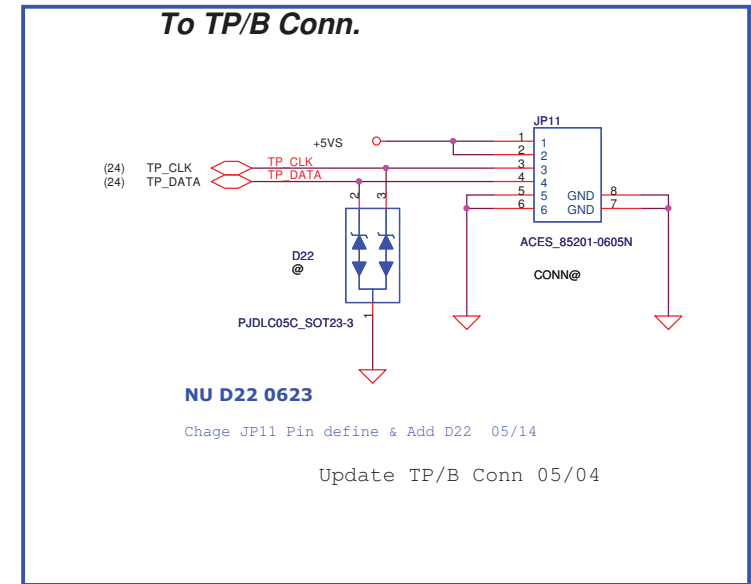
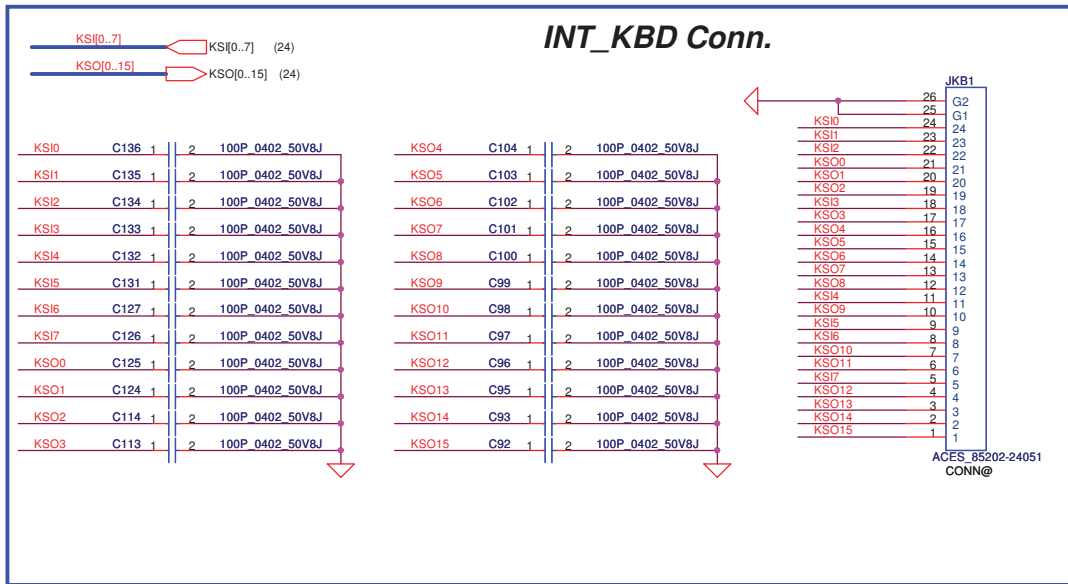
reserve PCH CLK to EC 052810

0.0402\_5% R1309 Add 0 ohm R1309 06/08

Change BT\_ON# from Pin98 to Pin108 06/24

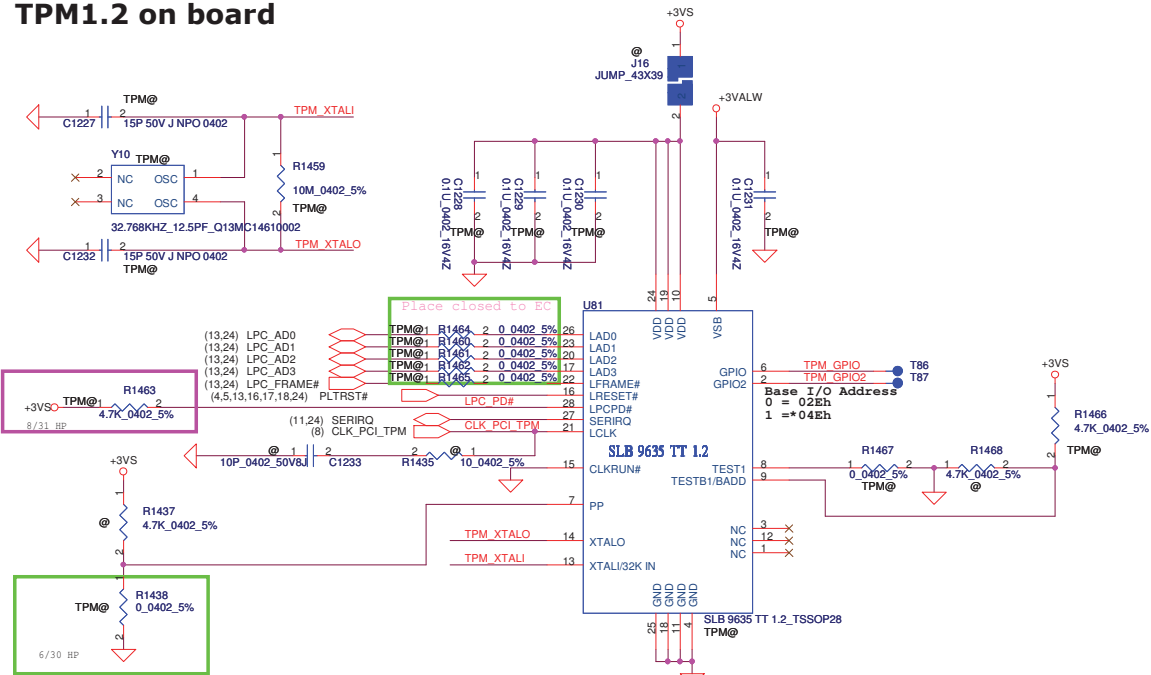
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Issued Date	2006/08/04	Deciphered Date	2007/8/18	Title	KB926
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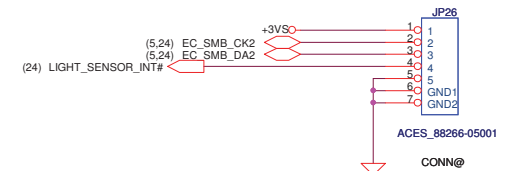


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				Date:	Friday, July 02, 2010
				Sheet	25 of 39
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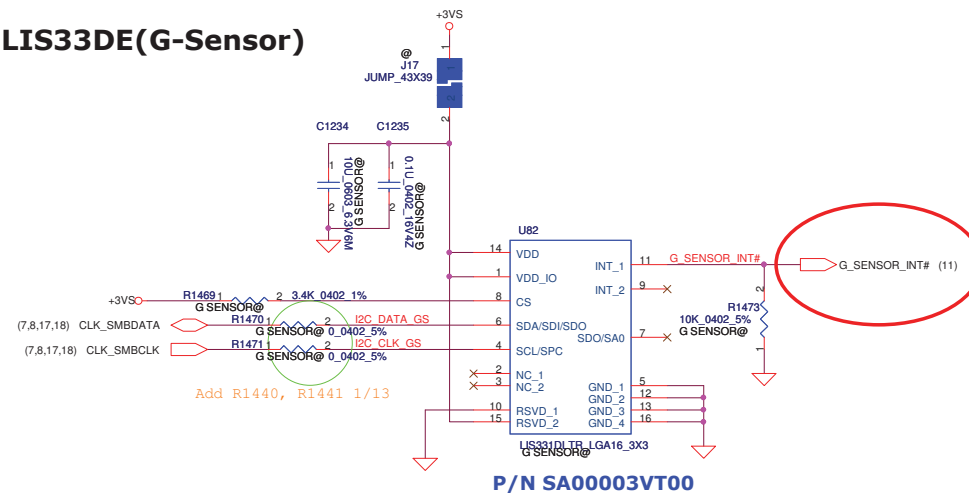
# TPM1.2 on board



# ALS (Ambient Light Sensor)

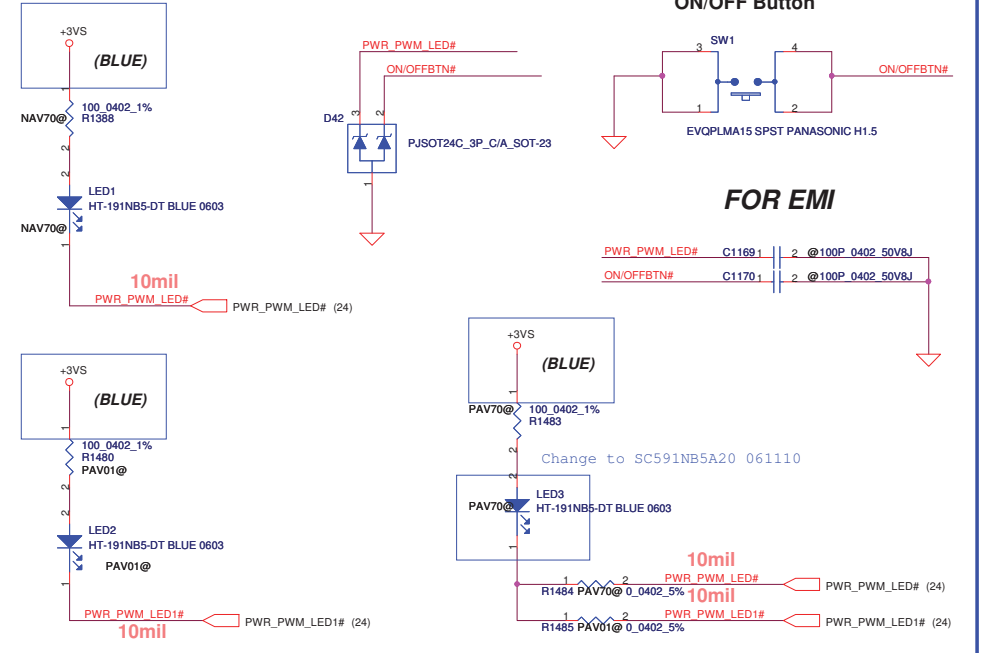


# ST LIS33DE (G-Sensor)

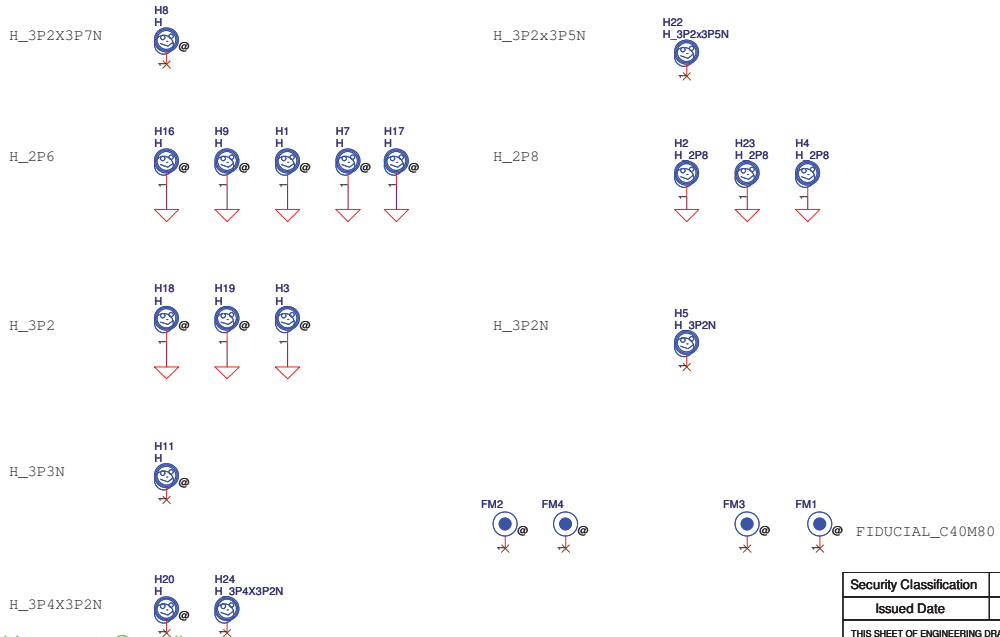
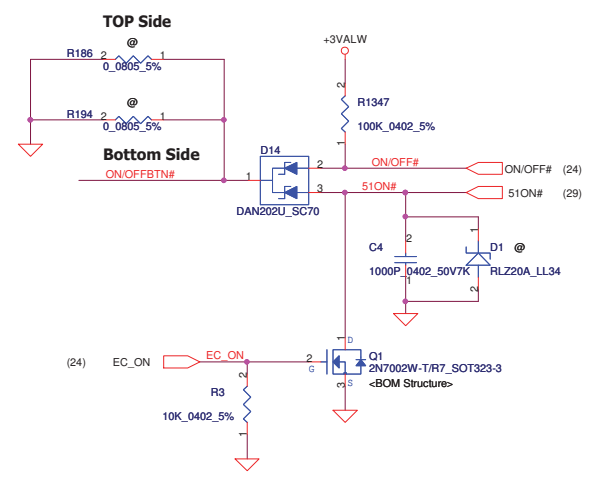


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				TPM/G-Sensor/Light sensor		
Size	Document Number			Rev		
	LA-6221P			0.1		
Date:	Thursday, July 01, 2010	Sheet	26	of 39		

Add For NAV50 07/06  
09/03 Change +5VS to +3VS



### Power Button Logic

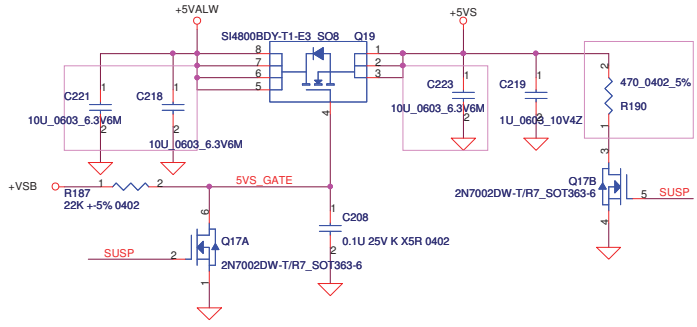


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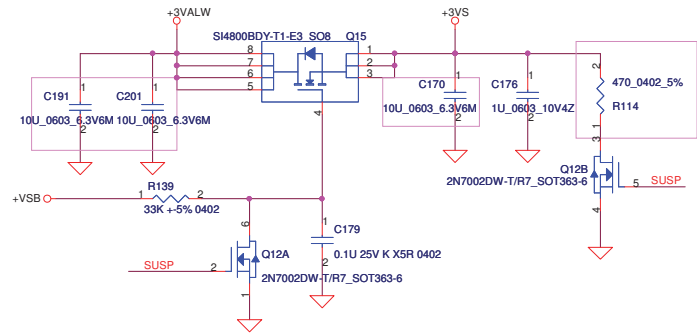
Security Classification		Compal Secret Data		Title	
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30  
 Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

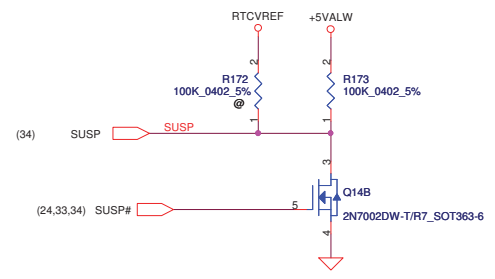
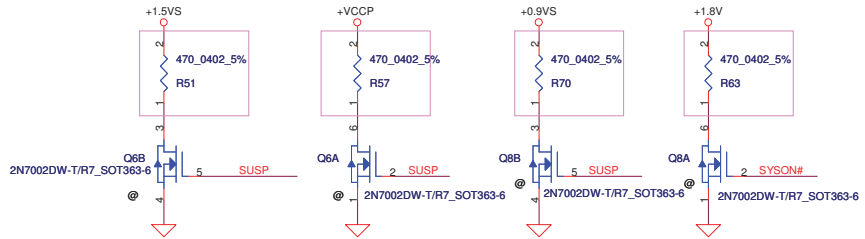
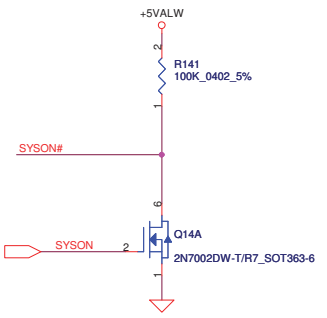
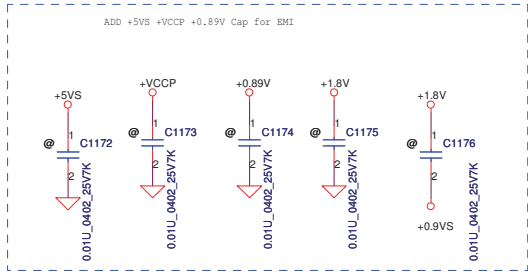
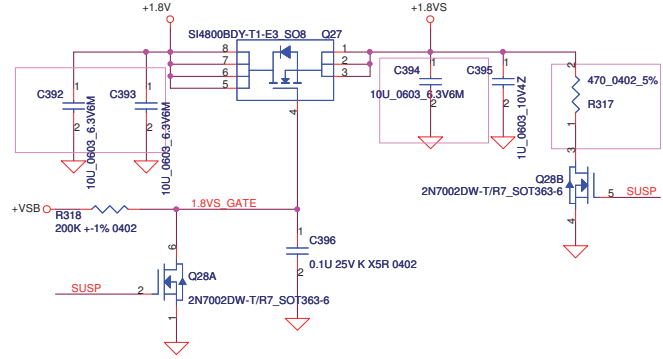
**+5VALW TO +5VS**



**+3VALW TO +3VS**

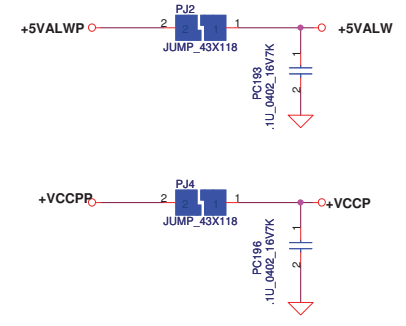
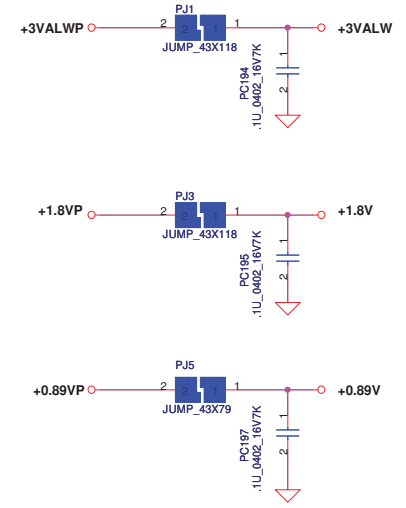
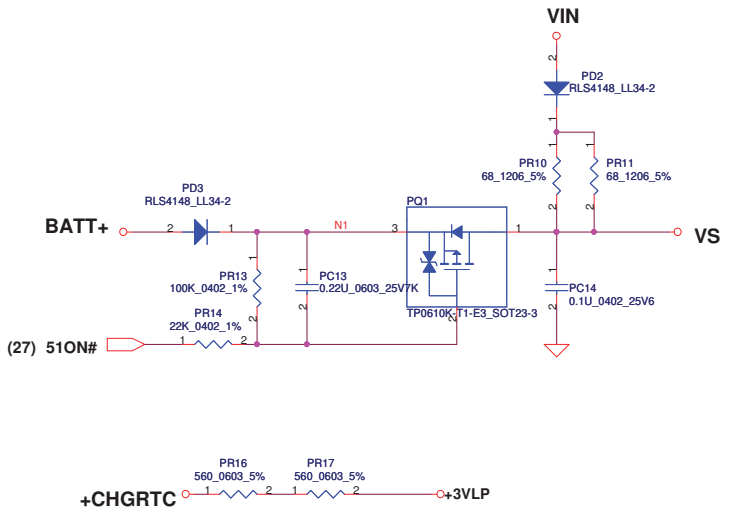
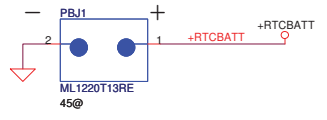
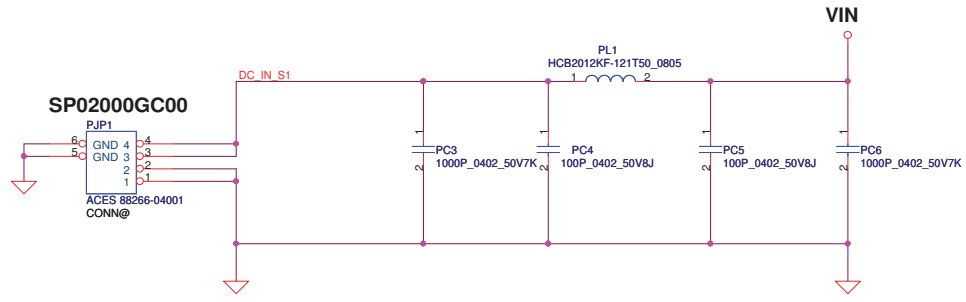


**+1.8V to +1.8VS**



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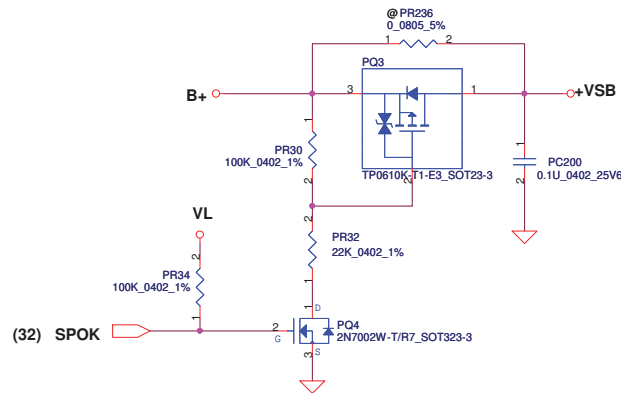
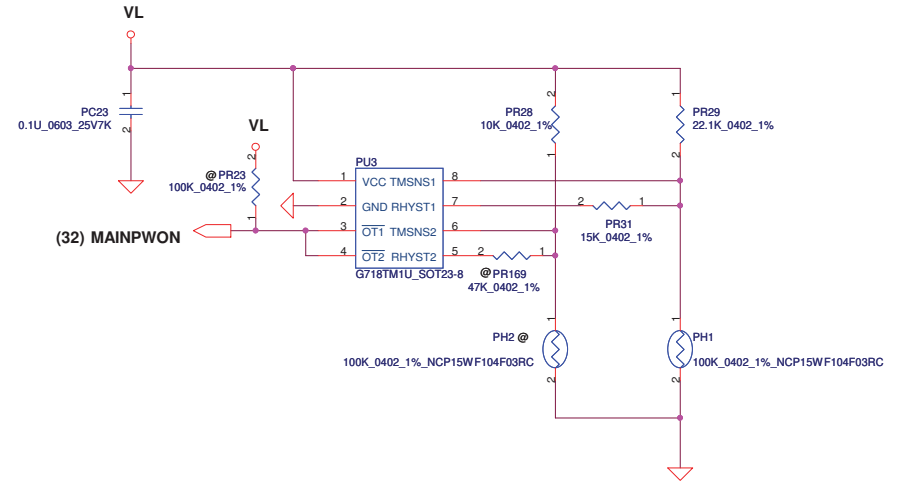
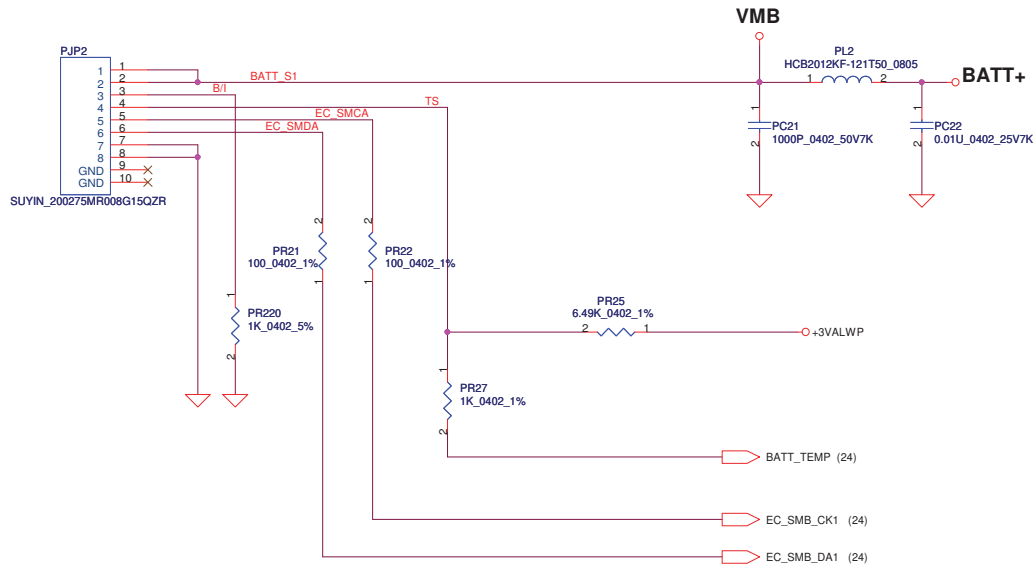
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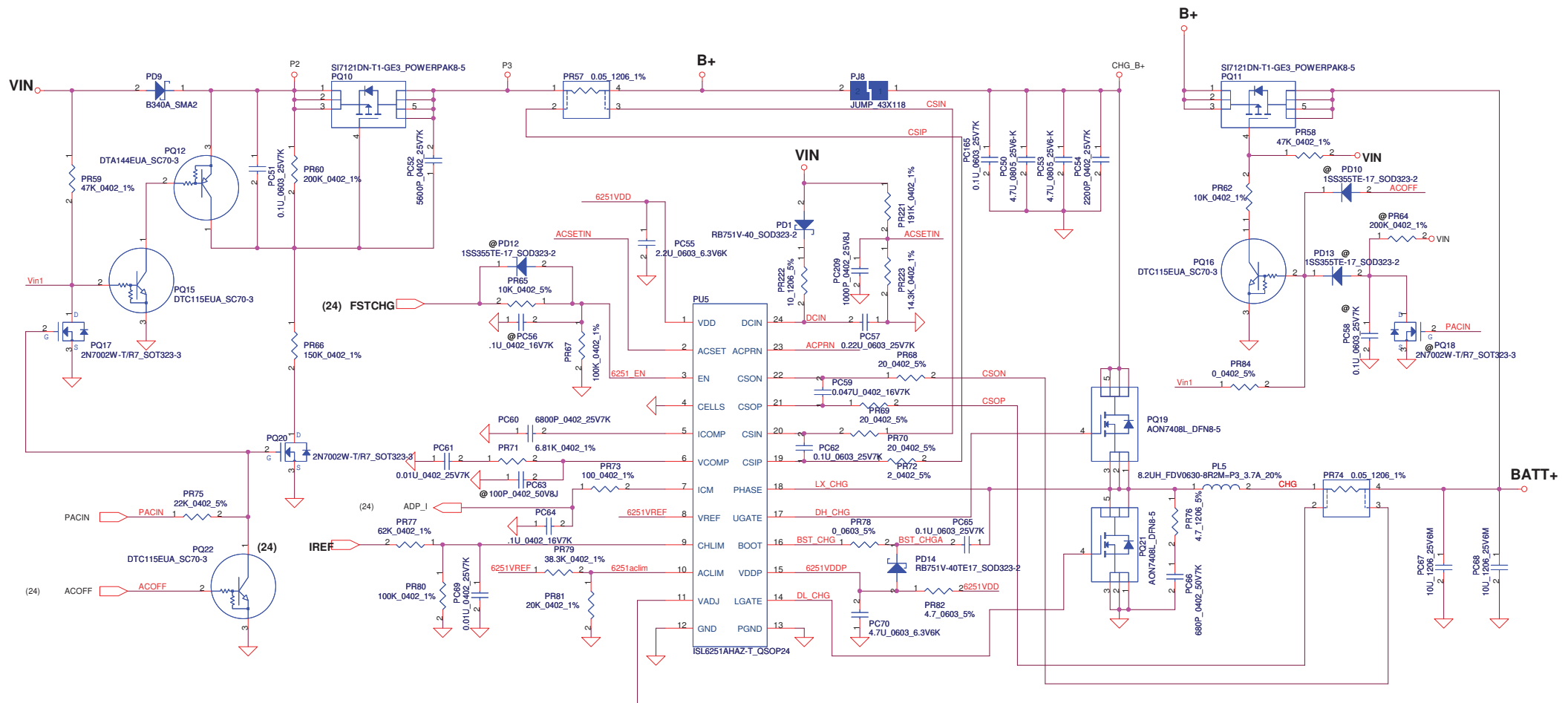
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PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 72 degree C



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Size	Document Number	Rev		Date	
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Date		Sheet		30 of 39	



$I_{ada} = 0 \sim 1.58A (30W)$      $CP = 85\% * I_{ada}$  ;  $CP = 1.343A$

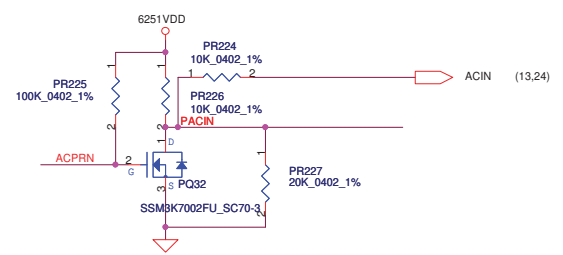
CP mode  
 $V_{aClim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$   
 $I_{input} = (1 / 0.05) * ((0.05 * V_{aClim}) / 2.39 + 0.05)$   
 where  $V_{aClim} = 0.8199V$ ,  $I_{input} = 1.343A$

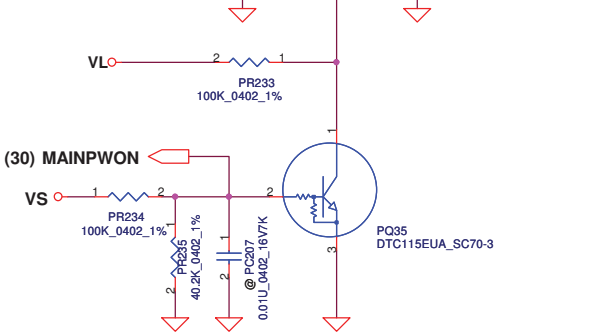
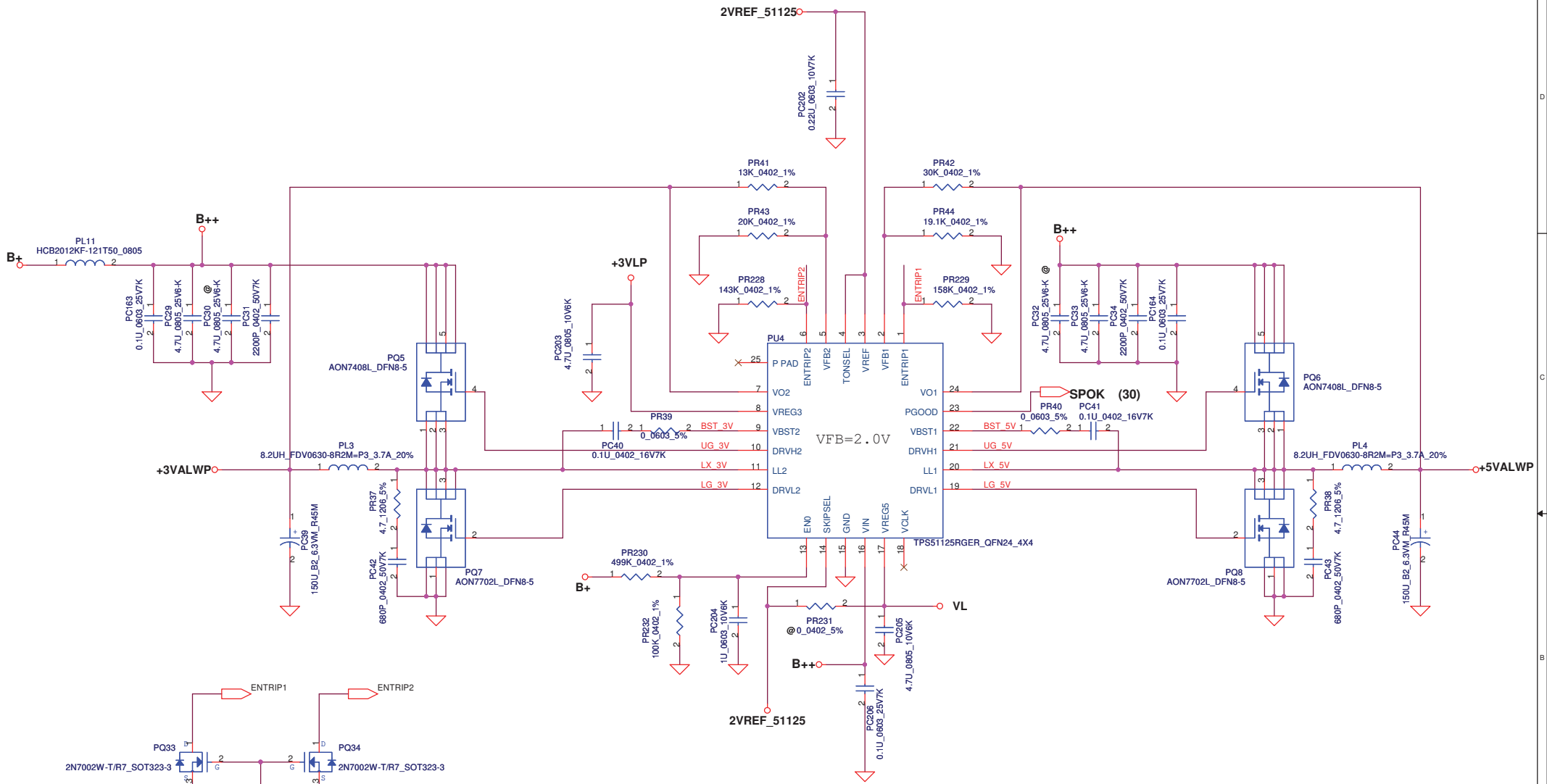
$CC = 0.3 \sim 1.76A$   
 $I_{REF} = 1.62 * I_{charge}$   
 $I_{REF} = 0.486V \sim 2.85V$   
 $3.24V \implies 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

$VADJ \rightarrow VREF \rightarrow 4.41V$   
 $VADJ \rightarrow G_{round} \rightarrow 3.99V$   
 deddy.suyanto@gmail.com  
 $V_{ce11} = (0.175 * VADJ) + 3.99$

(24) CALIBRATE#    PR83 15.4K\_0402\_1%  
 PR85 31.6K\_0402\_1%





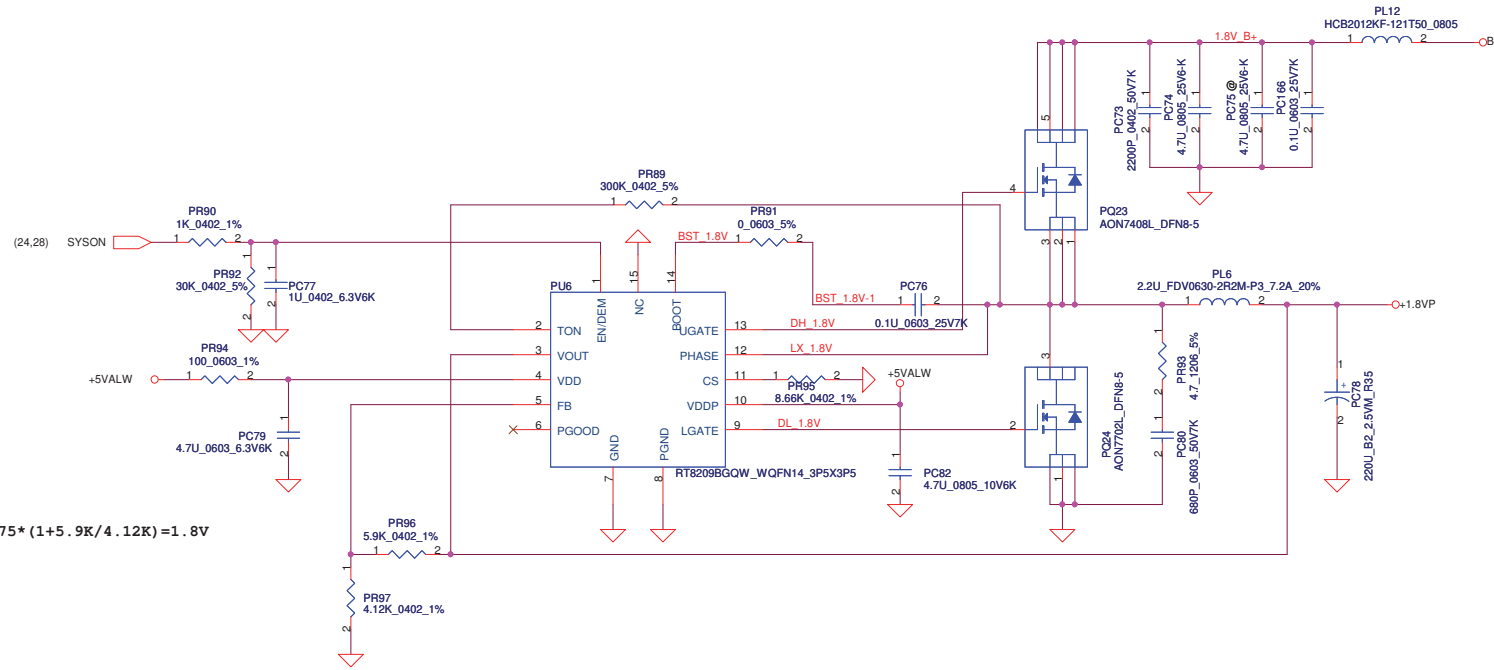
**+3.3VALWP** Ipeak=5.731A I<sub>max</sub>=4.012A  
 R<sub>ds(on)</sub>=17.9m ohm(max) ; R<sub>ds(on)</sub>=14.5m ohm(typical)  
 V<sub>trip</sub>=(10E-06 \* 143K)/9-24mV=134.9mV  
 I<sub>limit</sub>=134.9mV/17.9m ~134.9mV/14.5m x 1.2  
 =7.536A ~ 7.752A  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =8.081A ~ 8.297A  
 Delta I=1.090A (Freq=305KHz)

**+5VALWP** Ipeak=7.0A I<sub>max</sub>=4.9A  
 R<sub>ds(on)</sub>=17.9m ohm(max) ; R<sub>ds(on)</sub>=14.5m ohm(typical)  
 V<sub>trip</sub>=(10E-06 \* 158K)/9-24mV=151mV  
 I<sub>limit</sub>=151mV/17.9m ~151mV/14.5m x 1.2  
 =8.467A ~ 8.710A  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =9.384A ~ 9.627A  
 Delta I=1.834A (Freq=245KHz)

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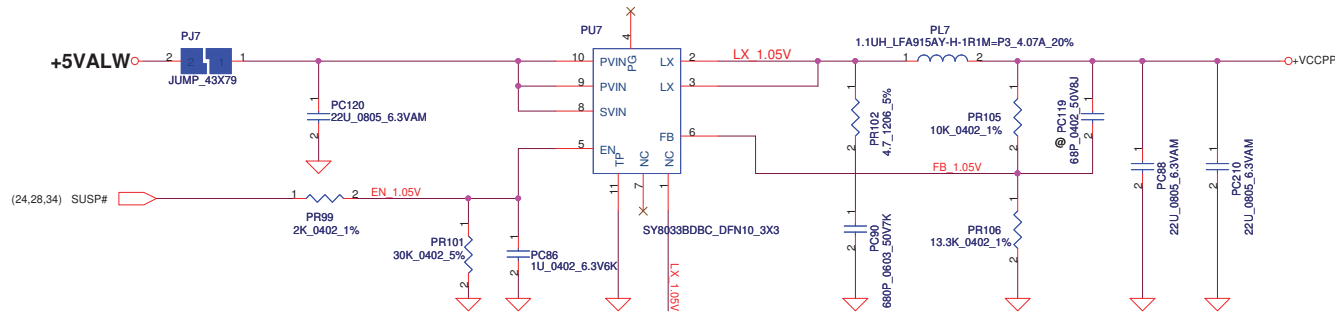
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				+5V/+3V		
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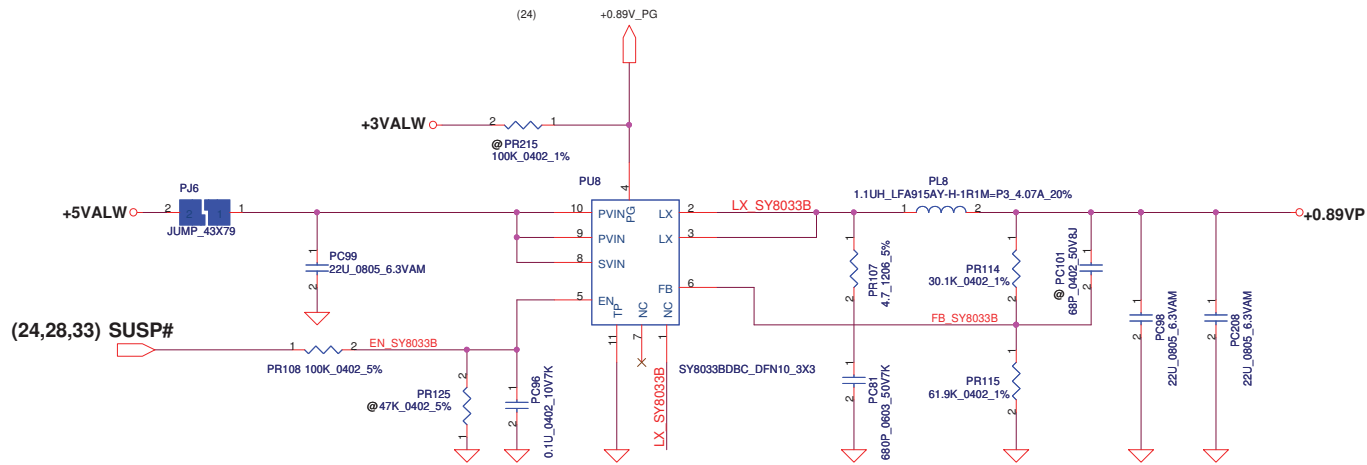


$\langle V_o=1.8V \rangle$      $V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR96/PR97)=0.75 \cdot (1+5.9K/4.12K)=1.8V$   
 $F_{sw}=328KHz$

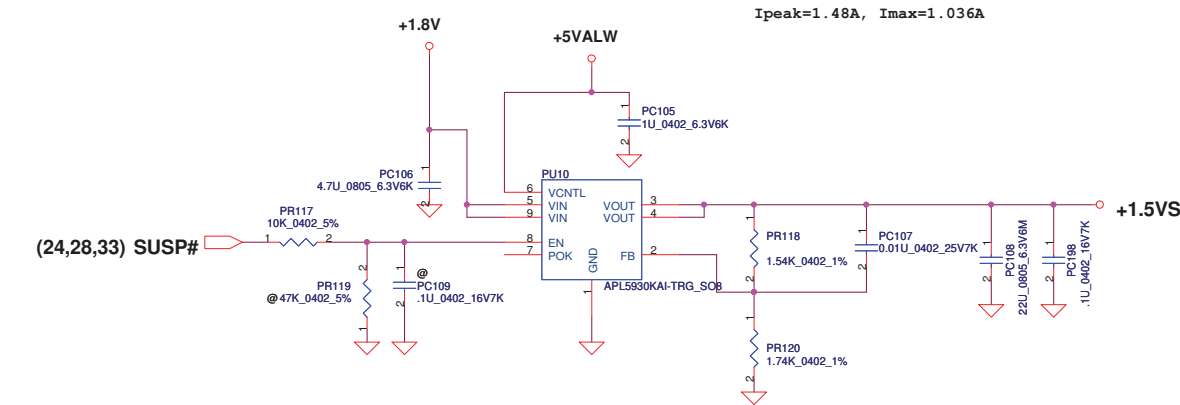
$\langle V_o=1.05V \rangle$      $V_{FB}=0.6V$   
 $V_o=V_{FB} \cdot (1+PR105/PR106)=0.6 \cdot (1+124K/61.9K)=1.05V$   
 $I_{peak}=3.124A$ ,  $I_{max}=2.187A$



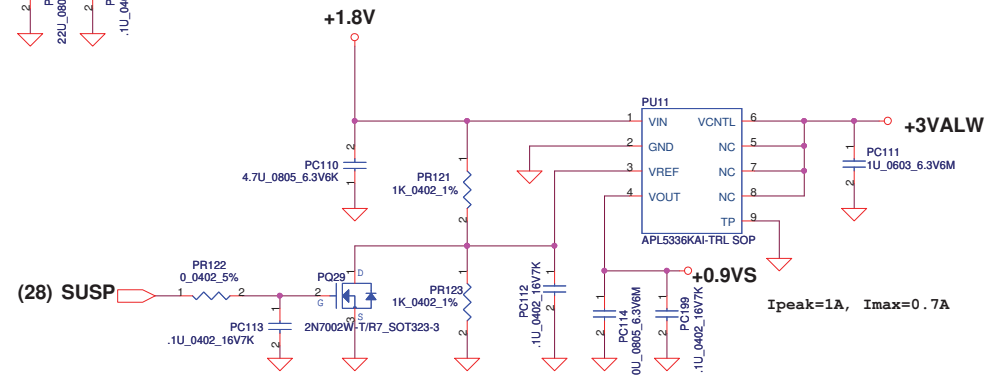
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$\langle V_o = 0.89V \rangle \quad V_{FB} = 0.6V$   
 $V_o = V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9) = 0.89V$   
 $I_{peak} = 2.64A, I_{max} = 1.848A$



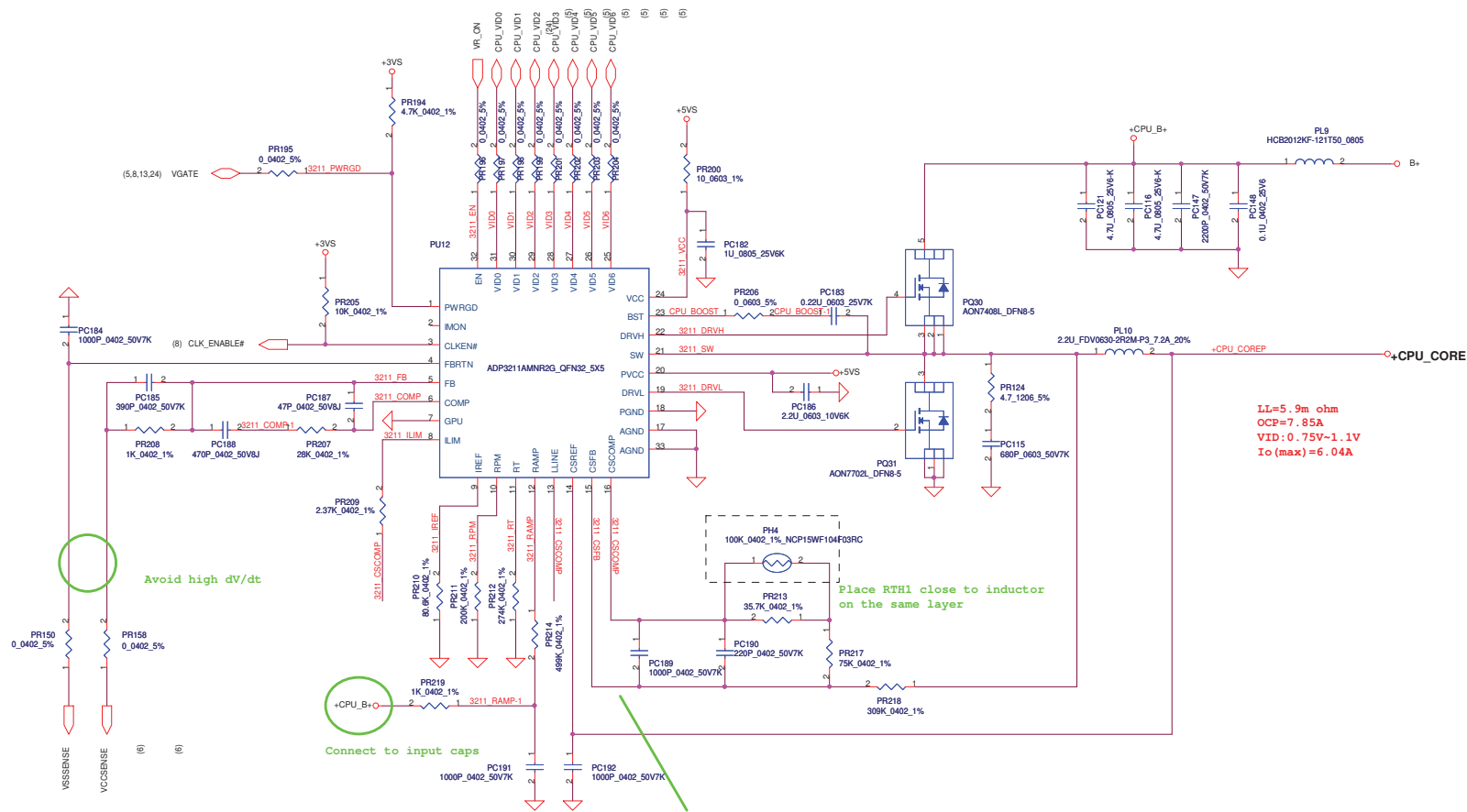
$I_{peak} = 1.48A, I_{max} = 1.036A$



$I_{peak} = 1A, I_{max} = 0.7A$

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LL=5.9m ohm  
 OCP=7.85A  
 VID: 0.75V~1.1V  
 I<sub>o</sub>(max)=6.04A

Avoid high dV/dt

Connect to input caps

Shortest the net trace

Place RTH1 close to inductor on the same layer

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add PR84	For design change	0.1	30	add PR84 (SD028000080 , S RES 1/16W 0 +-5% 0402)	2010.4.10	EVT
2	Change power solution	For design change	0.1	32	Change PU7 from SA000031D00(S IC RT8209BGQW WQFN 14P PWM) to SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK)	2010.4.12	EVT
3	Change SY8033B Pin1 net	For design change	0.1	32,33	Change SY8033B Pin1 connect Pin2 & Pin3	2010.4.13	EVT
4	Change PC101 & PC119	For design change	0.1	32,33	Change PC101 & PC119 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2010.4.13	EVT
5	Change PR105	For design change	0.1	32	Change PR105 from SD034100200(S RES 1/16W 10K +-1% 0402 ) to SD034100280 (S RES 1/16W 10K +-1% 0402 )	2010.5.13	DVT
6	Change PC30 & PC32 to non-pop	For cost down plan	0.1	32		2010.6.1	PVT
7	Change PL3,PL4,PL5,PL6,PL7,PL8,PL10	For TMP choke shortage issue	0.1	32	Change PL3,PL4,PL5 from SH00000JI00 to SH00000BS00 Change PL6,PL10 from SH00000FD10 to SH000000700 Change PL7,PL8 from SH00000J300 to SH000007N00	2010.6.1	PVT
8	Change PD10.PD13.PC58.PR64. PQ18 to non-pop Change PR84 to pop	For cost down plan	0.1	31		2010.6.11	PVT
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