

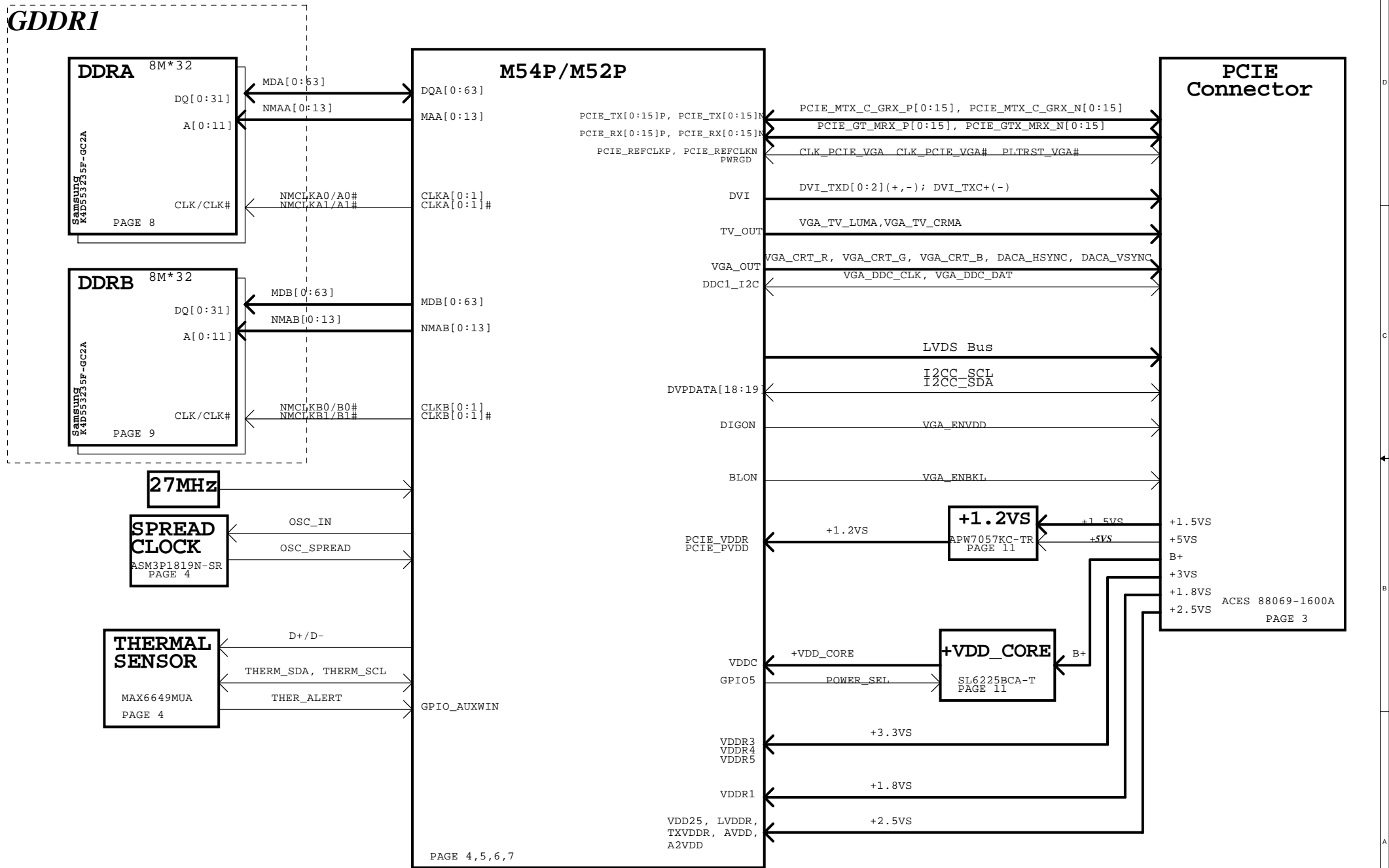


Mini (EFL50) ATI VGA/B M52-P

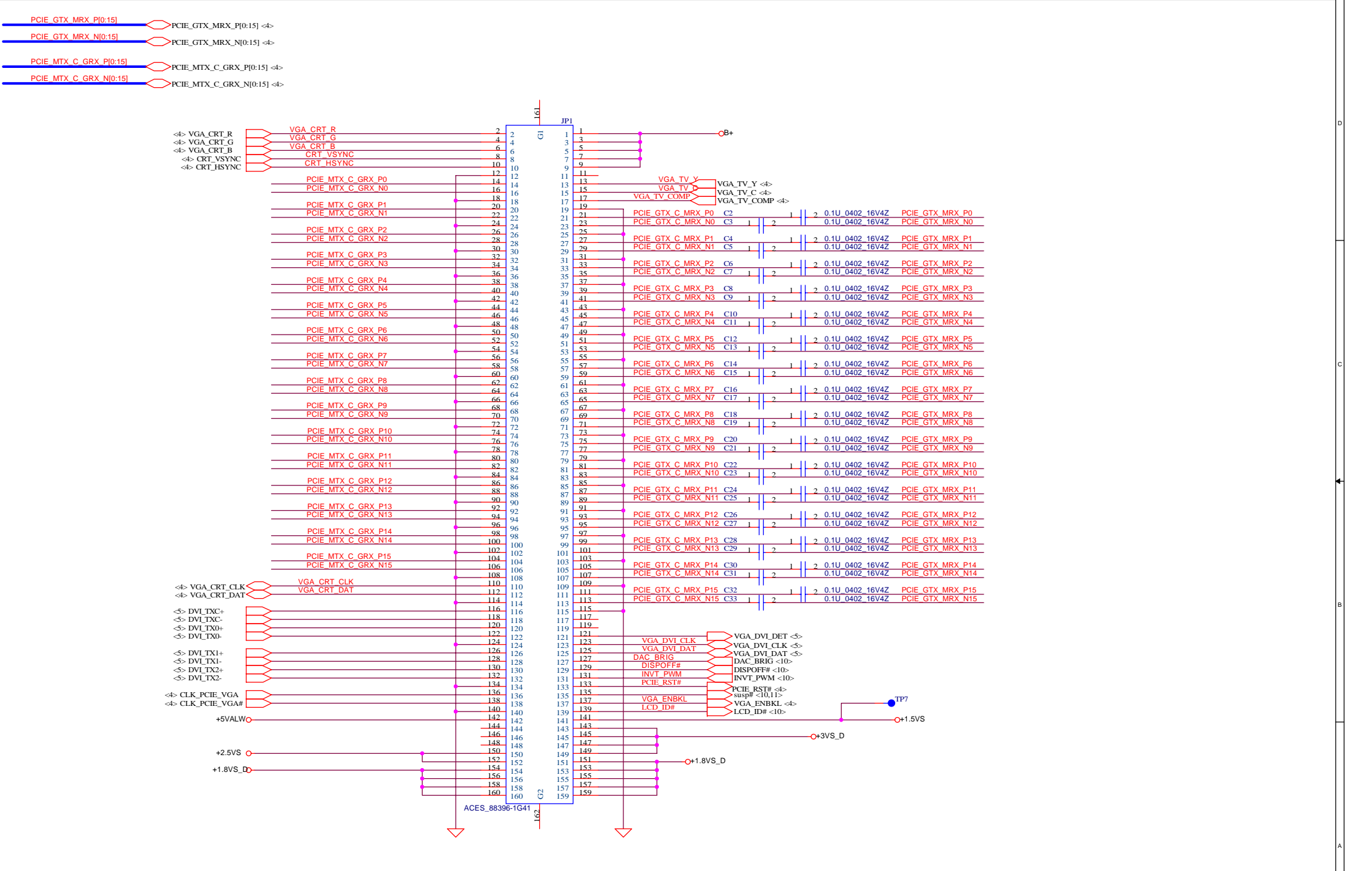
Revision 1.0

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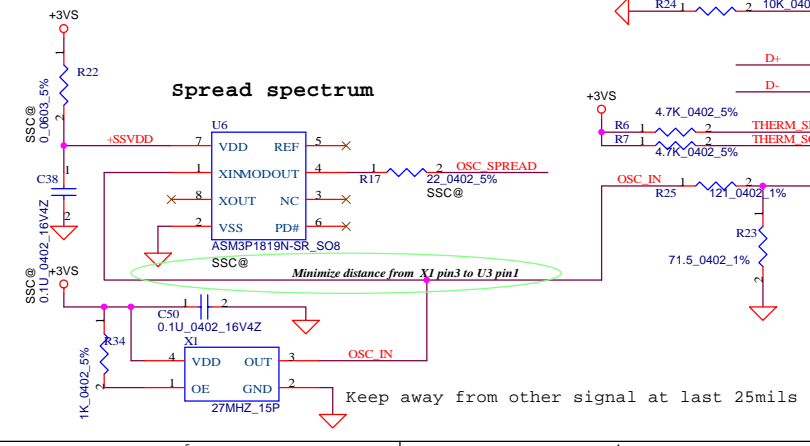
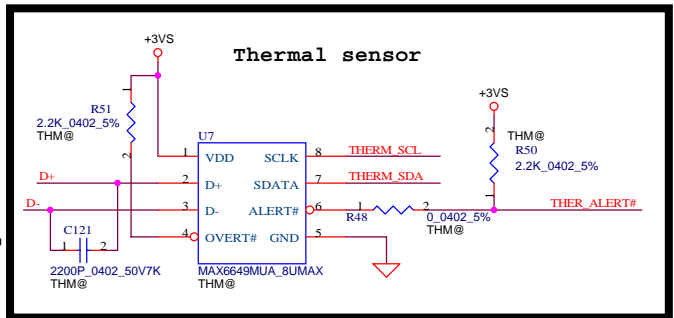
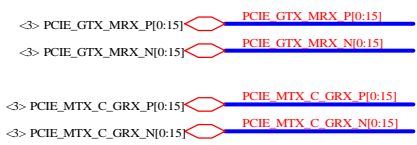
M54P/M52P BLOCK DIAGRAM



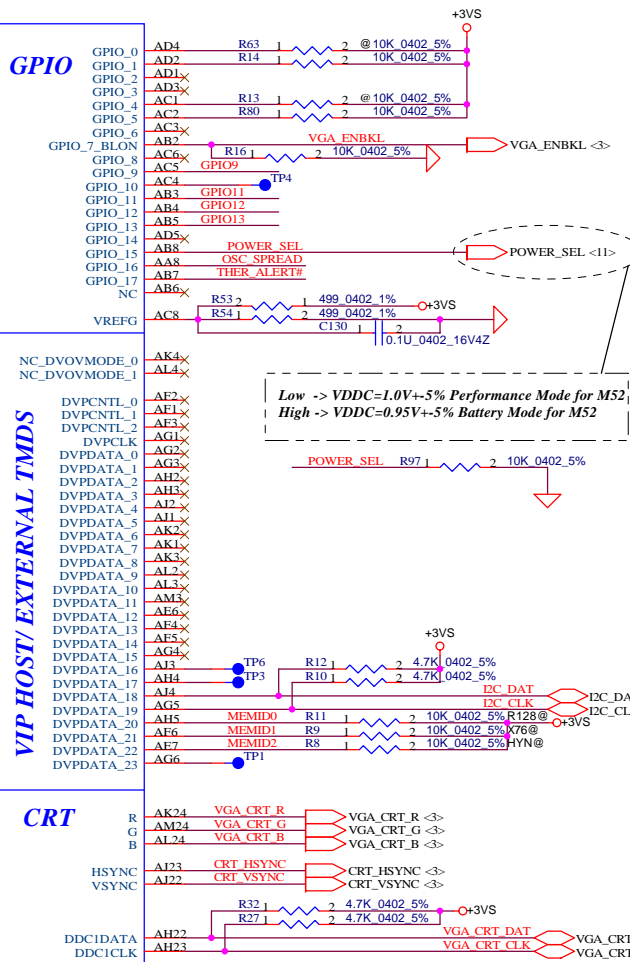
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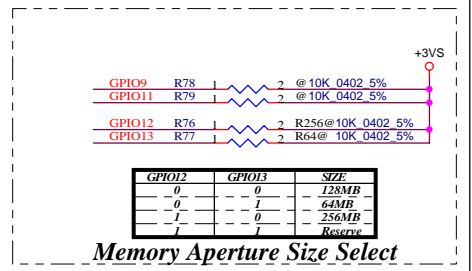
PCIE GTX_MRX P0	PCIE GTX_MRX N0	PCIE GTX_MRX P1	PCIE GTX_MRX N1	PCIE GTX_MRX P2	PCIE GTX_MRX N2	PCIE GTX_MRX P3	PCIE GTX_MRX N3	PCIE GTX_MRX P4	PCIE GTX_MRX N4	PCIE GTX_MRX P5	PCIE GTX_MRX N5	PCIE GTX_MRX P6	PCIE GTX_MRX N6	PCIE GTX_MRX P7	PCIE GTX_MRX N7	PCIE GTX_MRX P8	PCIE GTX_MRX N8	PCIE GTX_MRX P9	PCIE GTX_MRX N9	PCIE GTX_MRX P10	PCIE GTX_MRX N10	PCIE GTX_MRX P11	PCIE GTX_MRX N11	PCIE GTX_MRX P12	PCIE GTX_MRX N12	PCIE GTX_MRX P13	PCIE GTX_MRX N13	PCIE GTX_MRX P14	PCIE GTX_MRX N14	PCIE GTX_MRX P15	PCIE GTX_MRX N15	PCIE MTX_C_GRX P0	PCIE MTX_C_GRX N0	PCIE MTX_C_GRX P1	PCIE MTX_C_GRX N1	PCIE MTX_C_GRX P2	PCIE MTX_C_GRX N2	PCIE MTX_C_GRX P3	PCIE MTX_C_GRX N3	PCIE MTX_C_GRX P4	PCIE MTX_C_GRX N4	PCIE MTX_C_GRX P5	PCIE MTX_C_GRX N5	PCIE MTX_C_GRX P6	PCIE MTX_C_GRX N6	PCIE MTX_C_GRX P7	PCIE MTX_C_GRX N7	PCIE MTX_C_GRX P8	PCIE MTX_C_GRX N8	PCIE MTX_C_GRX P9	PCIE MTX_C_GRX N9	PCIE MTX_C_GRX P10	PCIE MTX_C_GRX N10	PCIE MTX_C_GRX P11	PCIE MTX_C_GRX N11	PCIE MTX_C_GRX P12	PCIE MTX_C_GRX N12	PCIE MTX_C_GRX P13	PCIE MTX_C_GRX N13	PCIE MTX_C_GRX P14	PCIE MTX_C_GRX N14	PCIE MTX_C_GRX P15	PCIE MTX_C_GRX N15		
AK27	AJ25	AH25	AH28	AG27	AE27	AE25	AE25	AE25	AE28	AD28	AD27	AD27	AC27	AC25	AB25	AB28	AA28	AA27	Y27	Y25	W25	W28	V28	V27	U27	U25	T25	T28	R28	R27	P27	AH31	AH30	AH30	AG30	AG32	AE32	AE31	AE31	AE31	AE30	AD30	AD32	AC32	AC31	AB31	AB30	AB30	AA30	AA32	Y32	Y31	W31	W30	W30	W32	U32	U31	T31	T30	R32	R32	P32	P31	N31
AK27	AJ25	AH25	AH28	AG27	AE27	AE25	AE25	AE25	AE28	AD28	AD27	AD27	AC27	AC25	AB25	AB28	AA28	AA27	Y27	Y25	W25	W28	V28	V27	U27	U25	T25	T28	R28	R27	P27	AH31	AH30	AH30	AG30	AG32	AE32	AE31	AE31	AE31	AE30	AD30	AD32	AC32	AC31	AB31	AB30	AB30	AA30	AA32	Y32	Y31	W31	W30	W30	W32	U32	U31	T31	T30	R32	R32	P32	P31	N31



Straps: (Internal pull down)

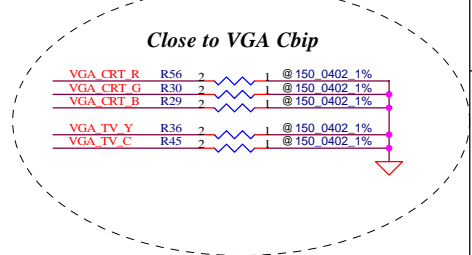
Transmitter power saving enable	GPIO[0]	0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable	GPIO[1]	0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access	GPIO[4]	0: OFF 1: ON
Current bias for the PCI Express PHY PLL	GPIO[5]	GPIO5 = 1 (must be pulled to 3.3V at reset using)
ROM ID Config	GPIO[9, 13:11]	GPIO[9]=1 External ROM Attached GPIO[9]=0 No External ROM For No External ROM: GPIO[13,12] is for MEM_AP_SIZE[1,0] GPIO[11] don't care
VIP_DEVICE	VSYNC	0: Slave VIP host device present 1: No slave VIP host device present

* The readback of this strap is the inverted with respect to the value on the pin



For DDRII

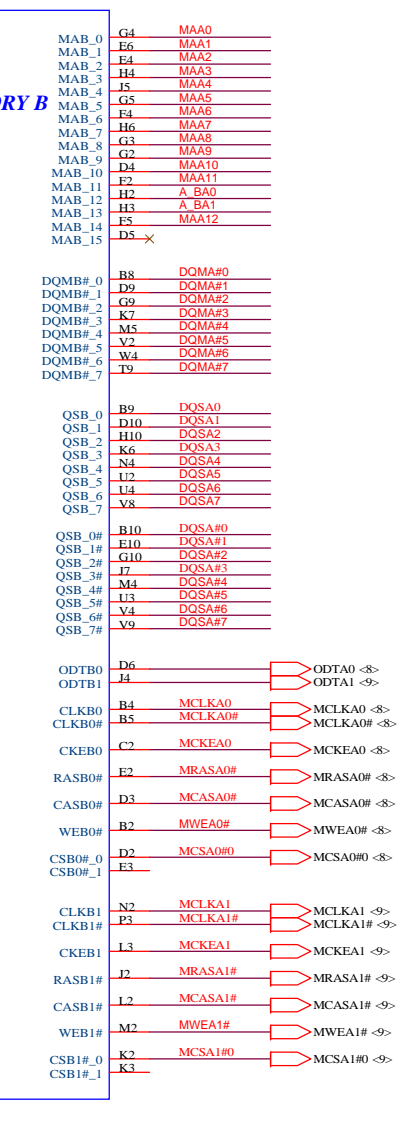
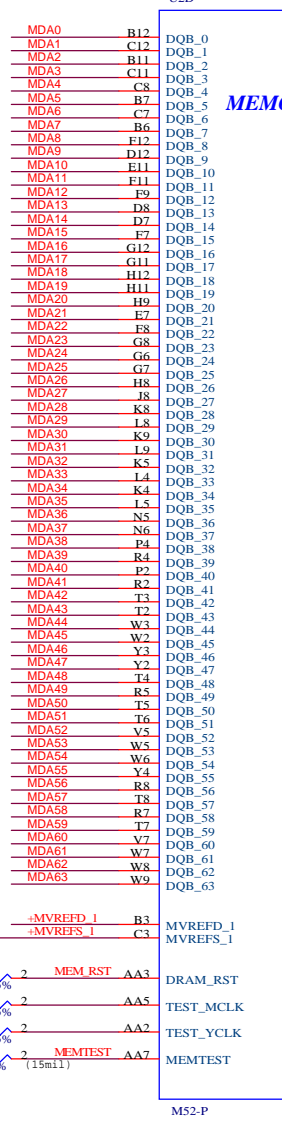
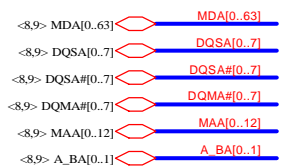
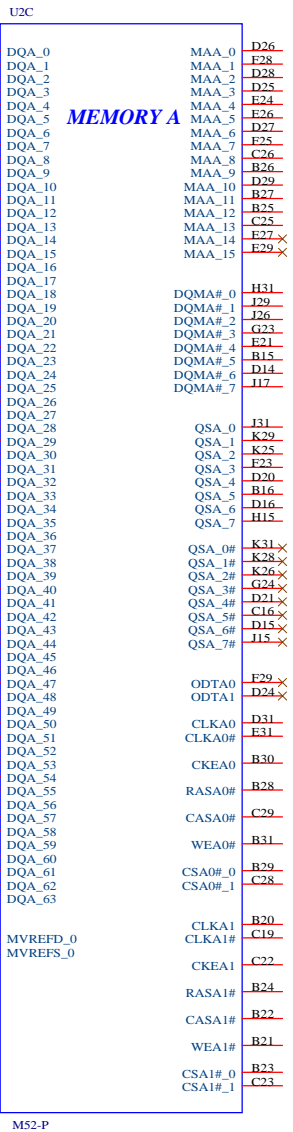
Vedio Memory Config. (VGA Internal PD)				
MEMID[2:0]	Size	Size (Speed)	Vender	Chips
0 0 0	64MB	16M16 (300MHz)	Samsung	2
0 0 1	128MB	16M16 (300MHz)	Samsung	4
1 0 0	64MB	16M16 (300MHz)	Hynix	2
1 0 1	128MB	16M16 (300MHz)	Hynix	4



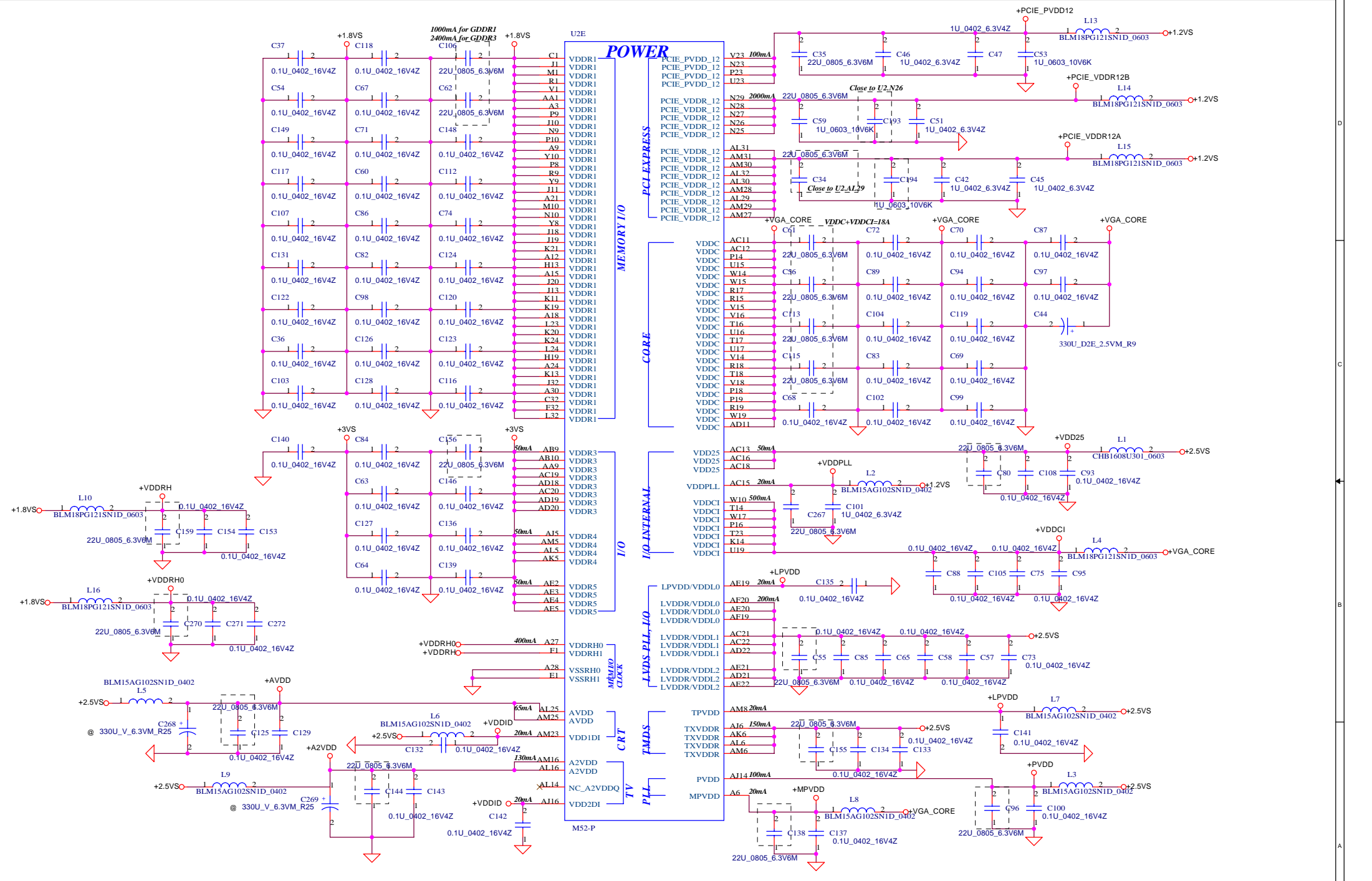
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M52-P Main			
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GDDR2



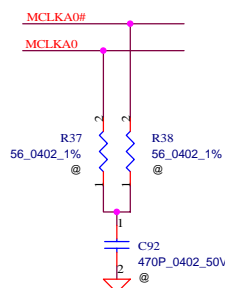
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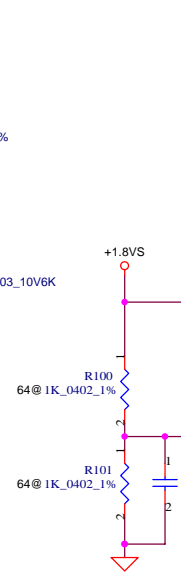
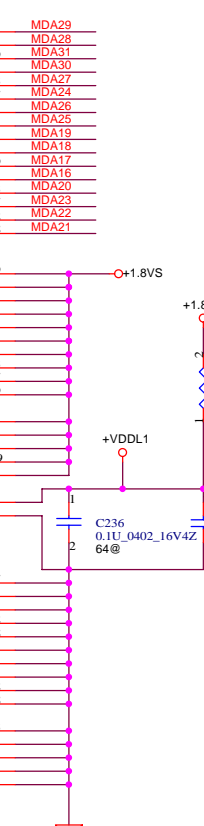
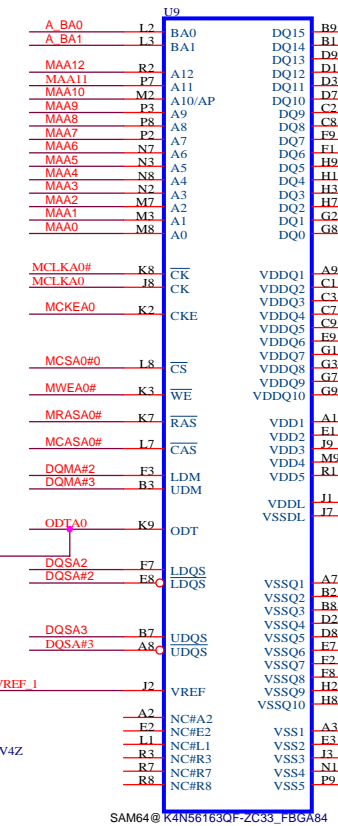
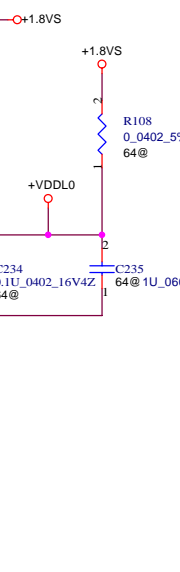
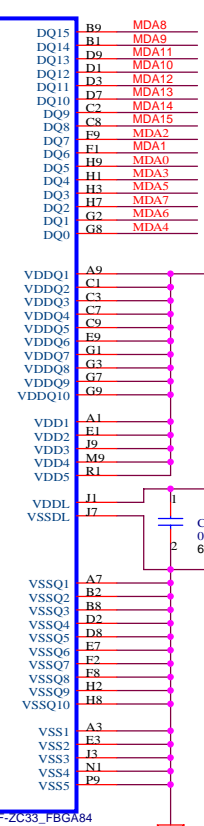
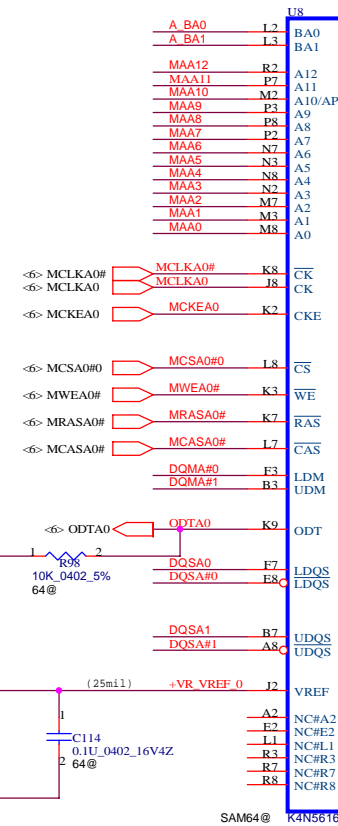
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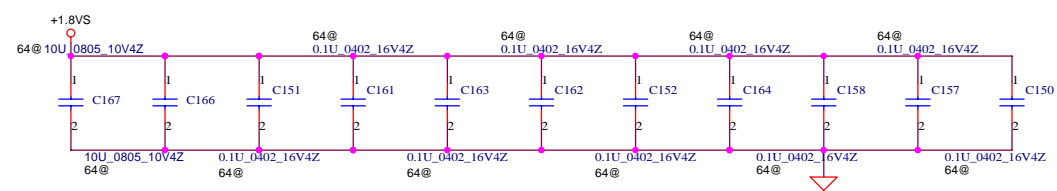
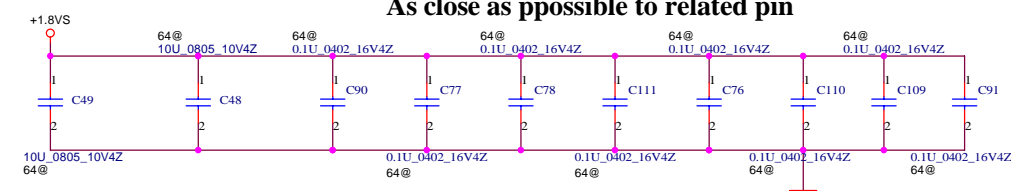


- <6.9> MDA[0..63] MDA[0..63]
- <6.9> DQSA[0..7] DQSA[0..7]
- <6.9> DQSA#[0..7] DQSA#[0..7]
- <6.9> DQMA[0..7] DQMA#[0..7]
- <6.9> MAA[0..12] MAA[0..12]
- <6.9> A_BA[0..11] A_BA[0..11]

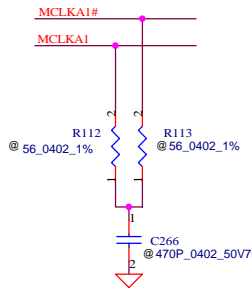
Default VRAM chip is SAM: SA00000YC00.



As close as possible to related pin

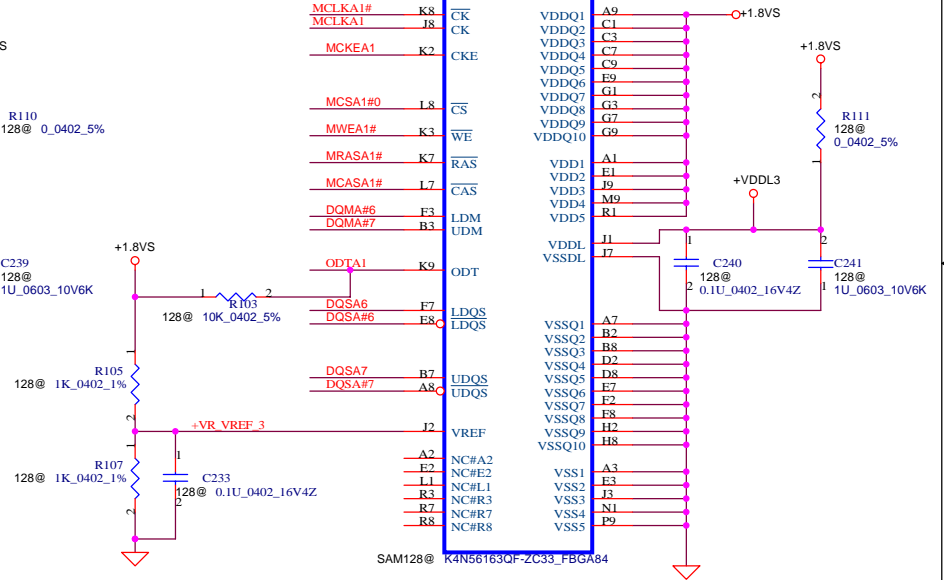
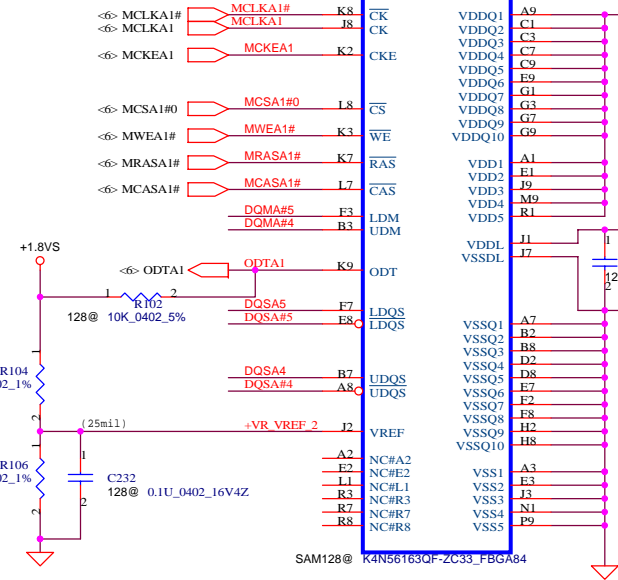
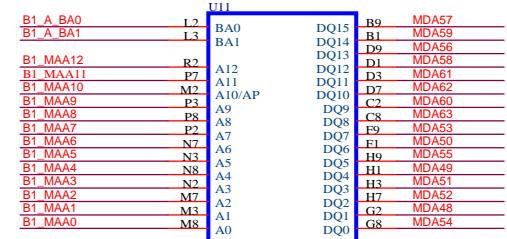
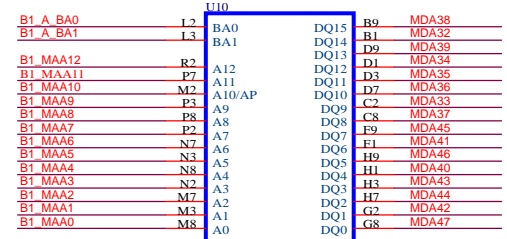
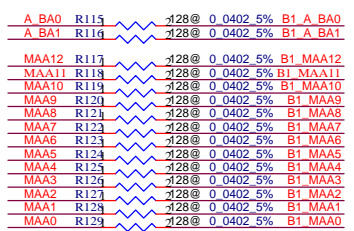


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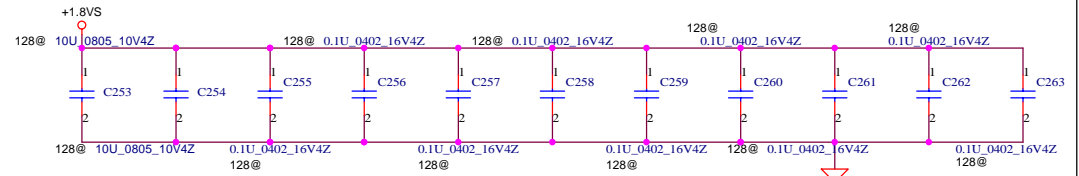
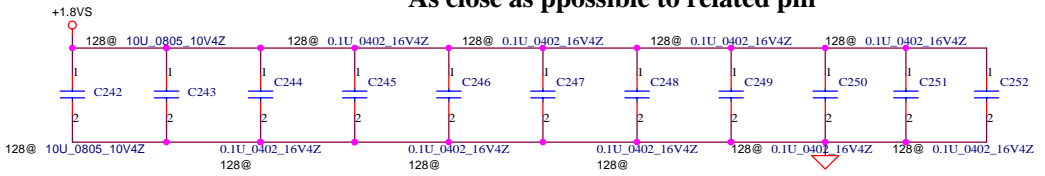


- <6,8> MDA[0..63] — MDA[0..63]
- <6,8> DQSA[0..7] — DQSA[0..7]
- <6,8> DQSA#[0..7] — DQSA#[0..7]
- <6,8> DQMA#[0..7] — DQMA#[0..7]
- <6,8> MAA[0..12] — MAA[0..12]
- <6,8> A_BA[0..1] — A_BA[0..1]

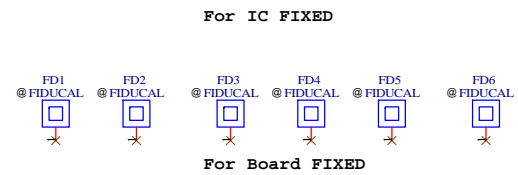
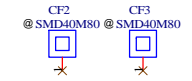
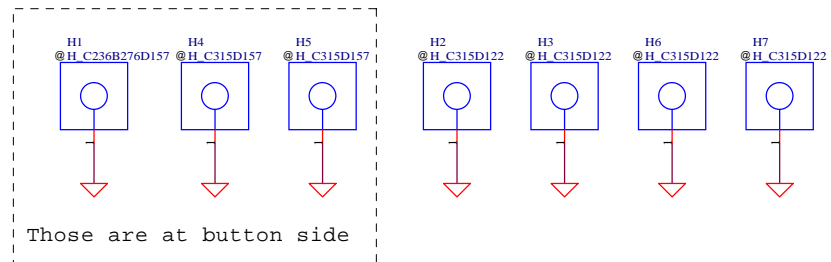
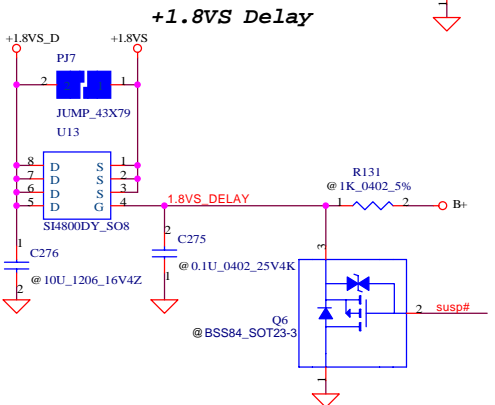
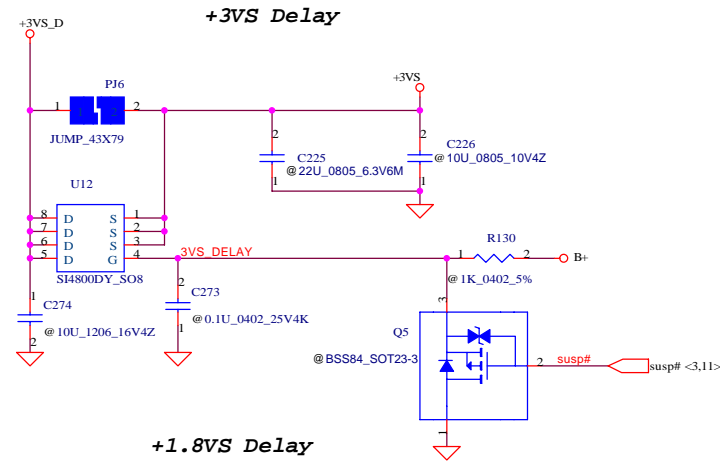
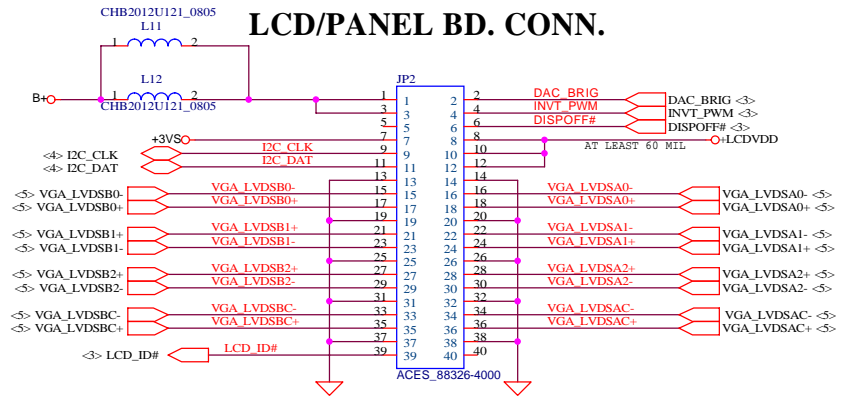
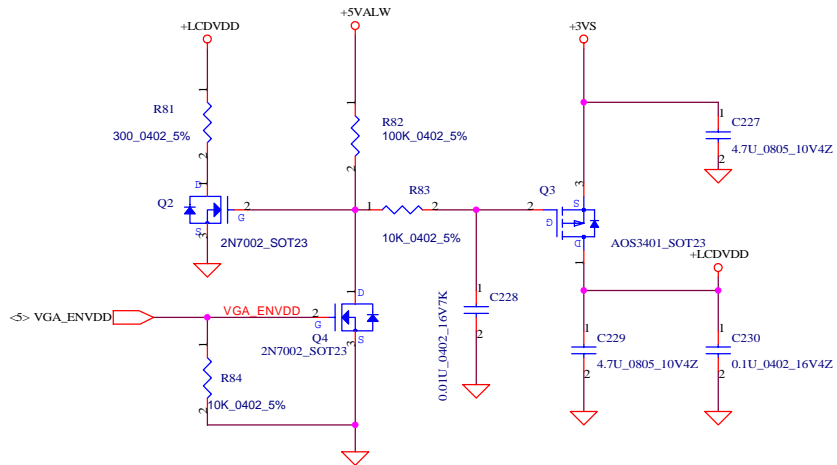
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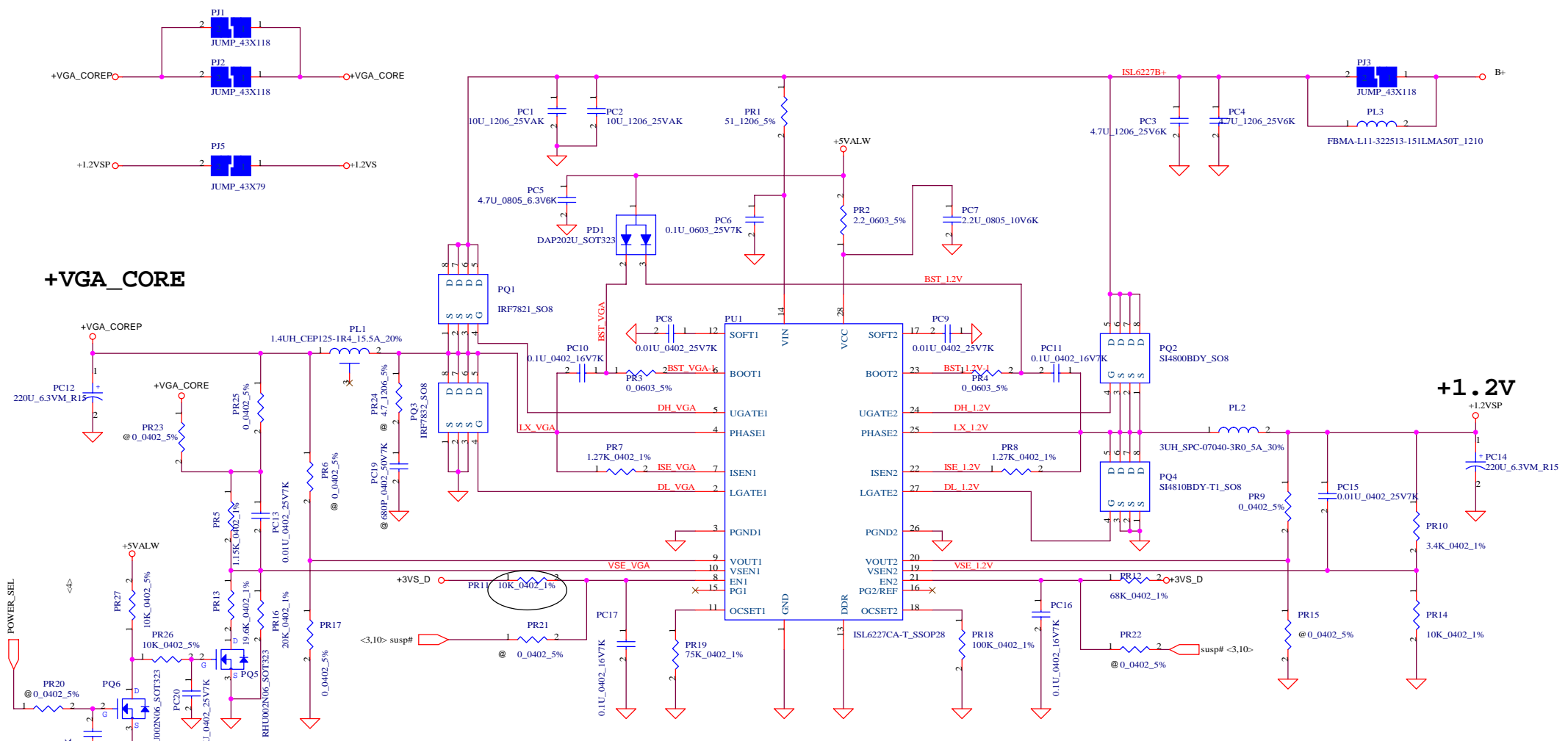
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	W/O POWER PLAY	With POWER PLAY
POWER_SEL	Low	High
+VGA_CORE	1.0V	0.95V
	PR5=1.15K, PR16=20K, PR13=19.6K	PR5=1.15K, PR16=20K
	PJ3, PJ1, PJ2, PJ4 short	PJ3, PJ1, PJ2, PJ4 short

Version change list (P.I.R. List)

===== 2005/12 R0.2 =====

- 01. Reserve +3VS and +1.8VS delay circuit and reserve Jump. == To meet ATI PWR sequence.
Reserve PJ6, PJ7, U12, U13, C273, C274, C275, C276,
Q5, Q6, R130 and R131.
- 02. Change C42, C45, C46, C47 and C51, from 0.1U to 1U. == For 3D hang issue.
- 03. Change C101, from 0.1U to 1U. == For 3D hang issue.
- 04. Add C44 as 330U == For 3D hang issue.
- 05. Delete R63, 10K_0402_5% == PCIE TX power saving.

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ZZZ
DA800005F10
--PCB ZKD LS-2766P
REV1 VGA/B

DA800005F10

U8
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN64@ SA00000JW00

U9
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN64@ SA00000JW00

U10
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN128@ SA00000JW00

U11
SA00000JW00
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HY5PS561621AFP-33
FBGA

HYN128@ SA00000JW00

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