

# Dunlin LA-2601 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-2 / ICH6-M

(NV43/44M)

2005 / 03 / 14

Rev:1.0

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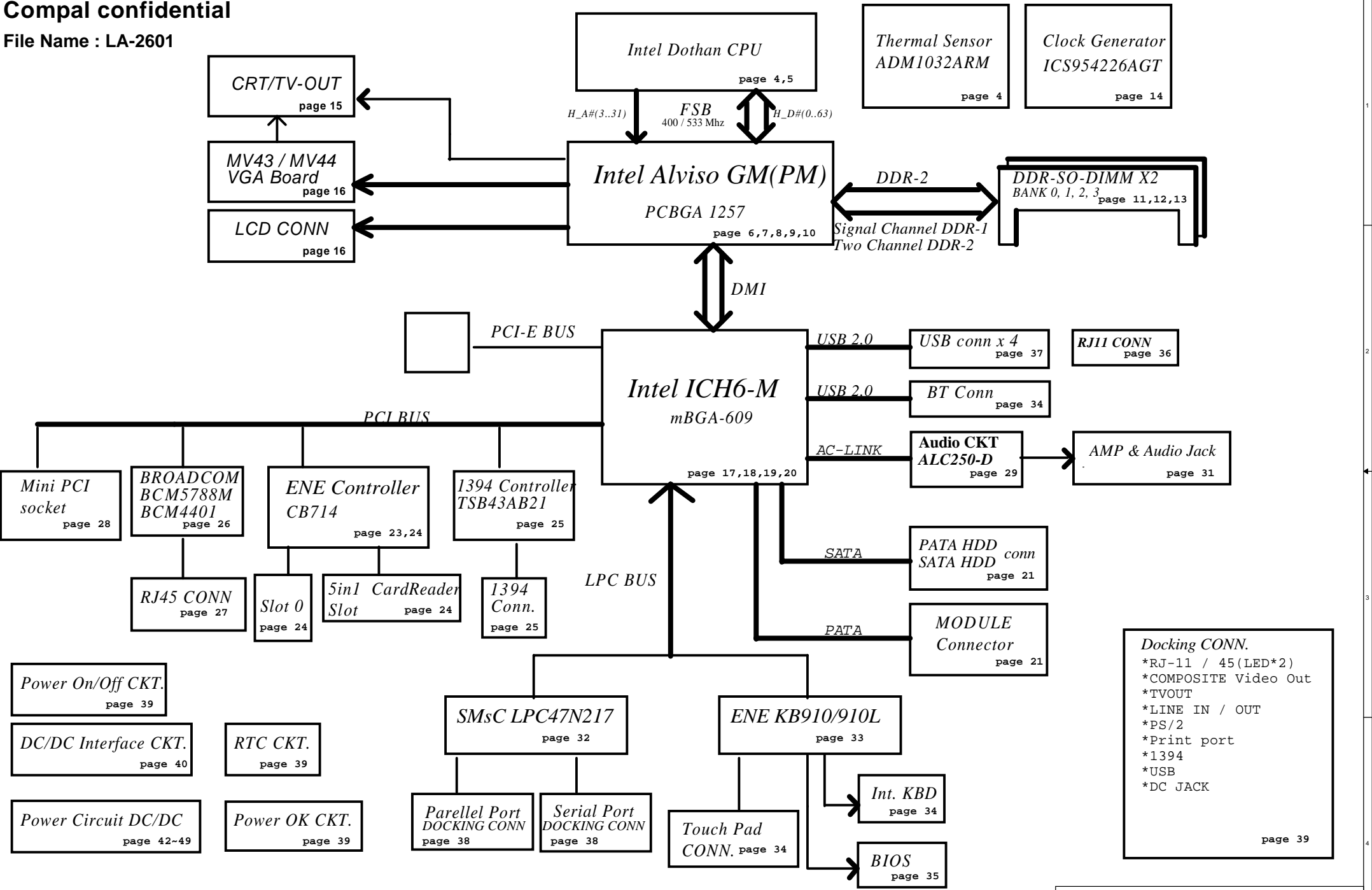
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**Compal confidential**

File Name : LA-2601



**Docking CONN.**  
 \*RJ-11 / 45(LED\*2)  
 \*COMPOSITE Video Out  
 \*TVOUT  
 \*LINE IN / OUT  
 \*PS/2  
 \*Print port  
 \*1394  
 \*USB  
 \*DC JACK

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCACC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH
LAN	AD17	3	PIRQF

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb		

## EC SM Bus2 address

## ICH6M SM Bus address

Device	Address
Clock Generator ( ICS 952623)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

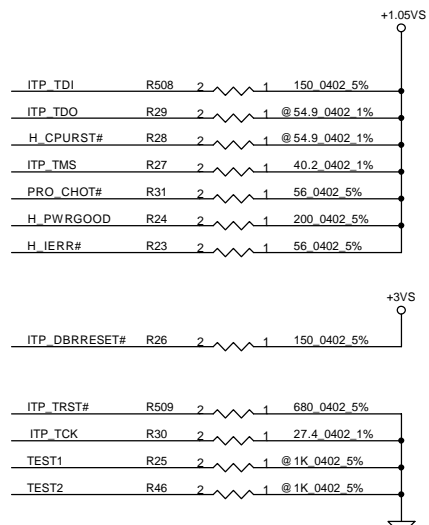
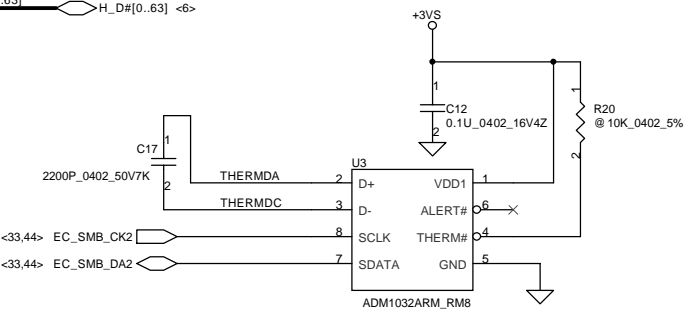
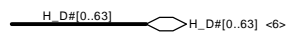
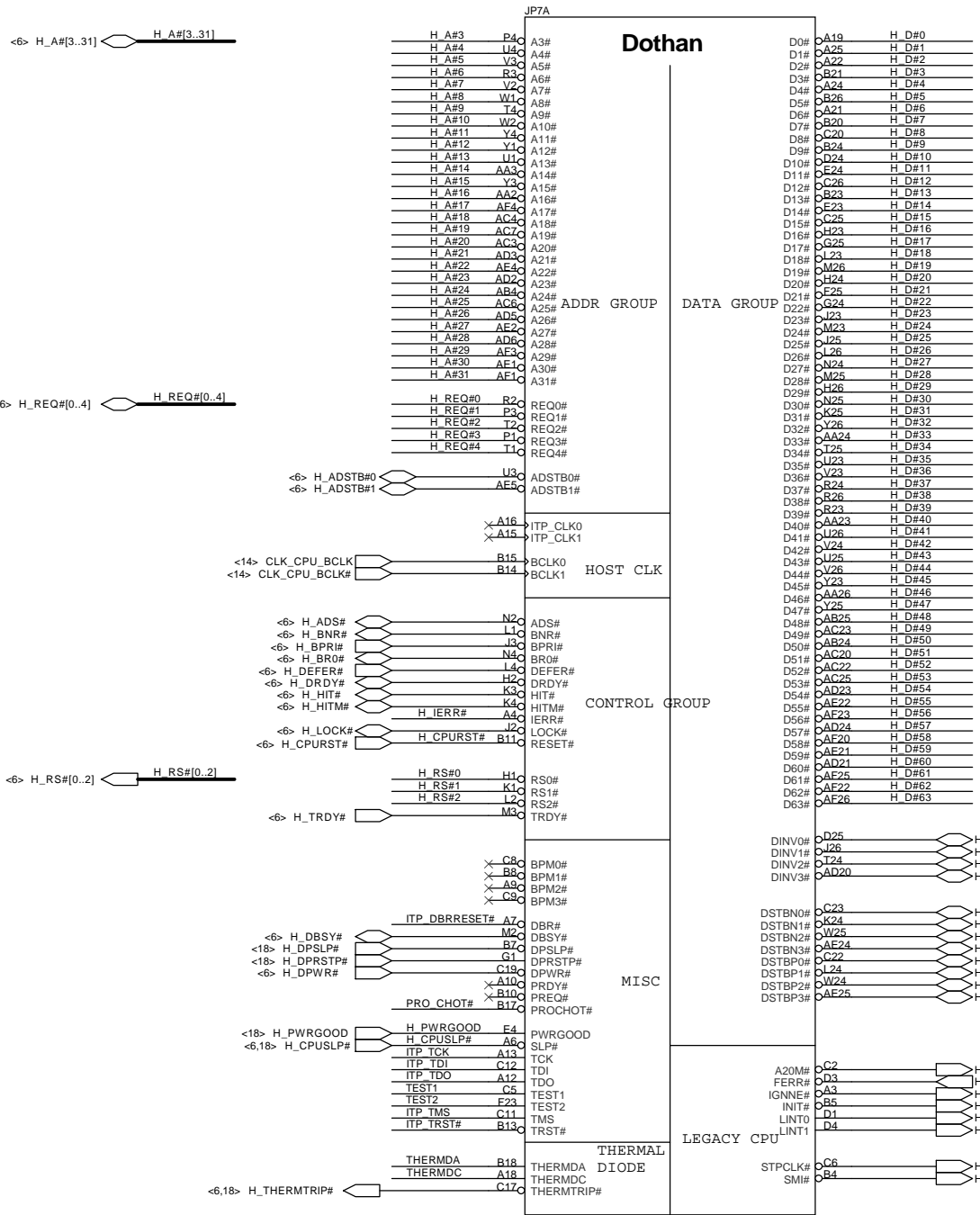
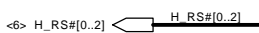
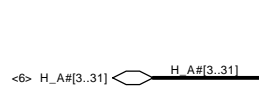
## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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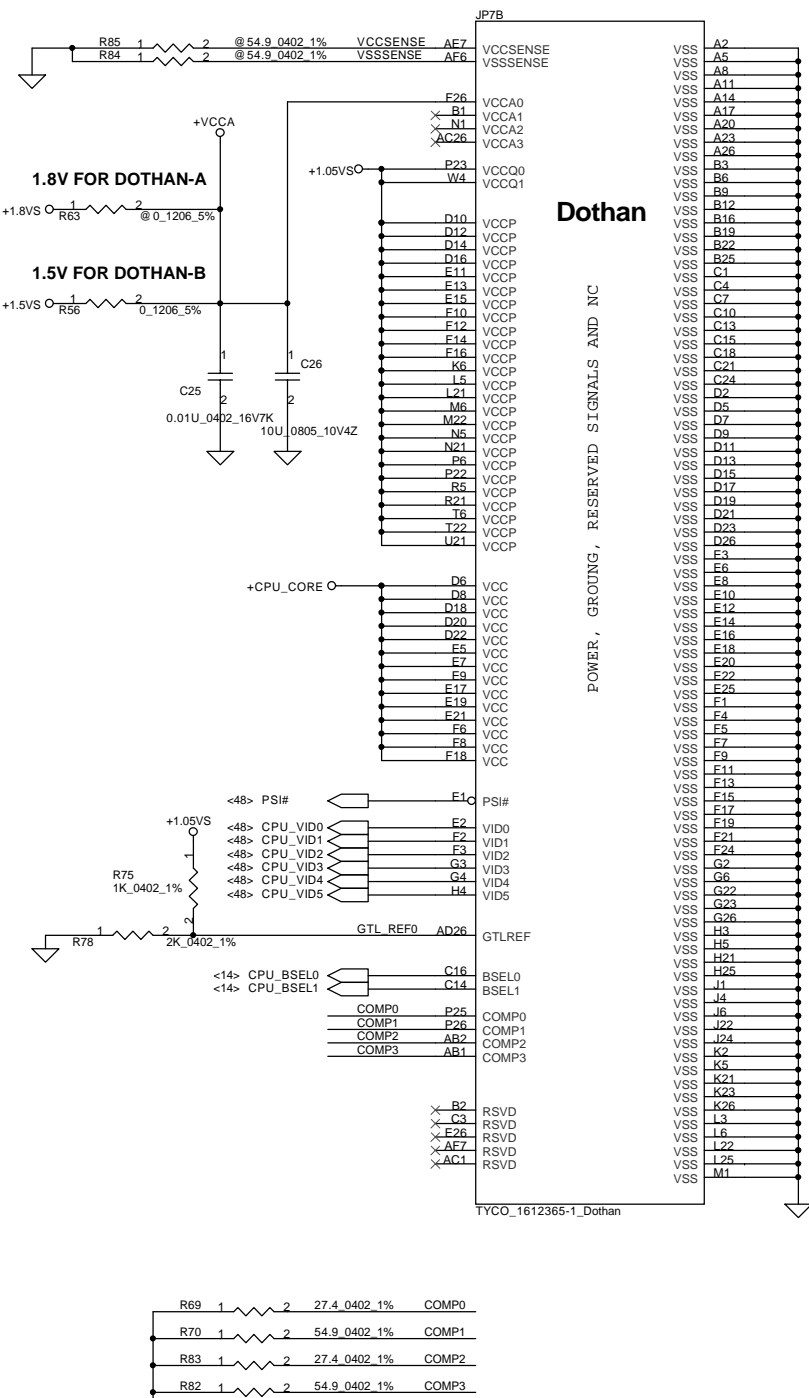
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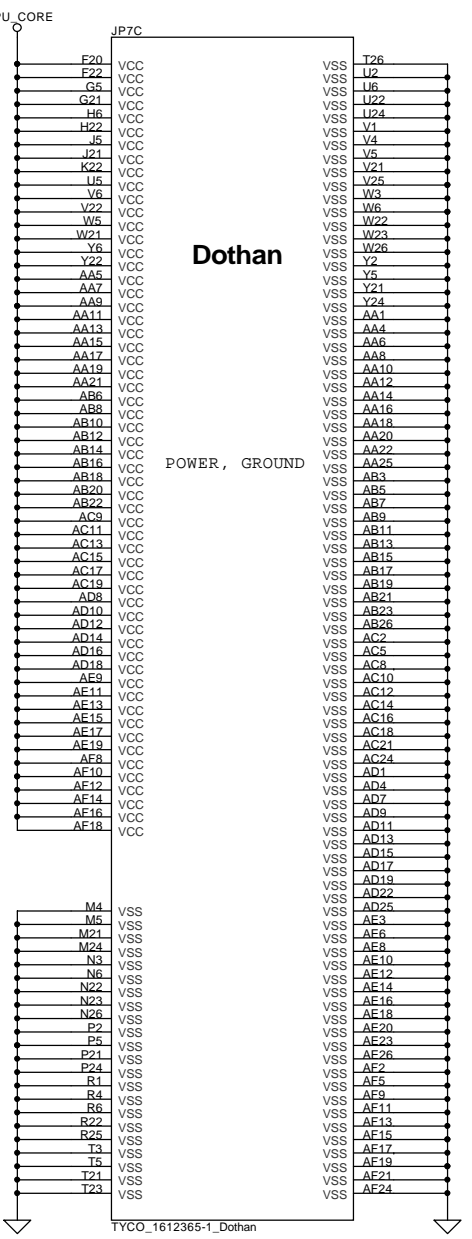
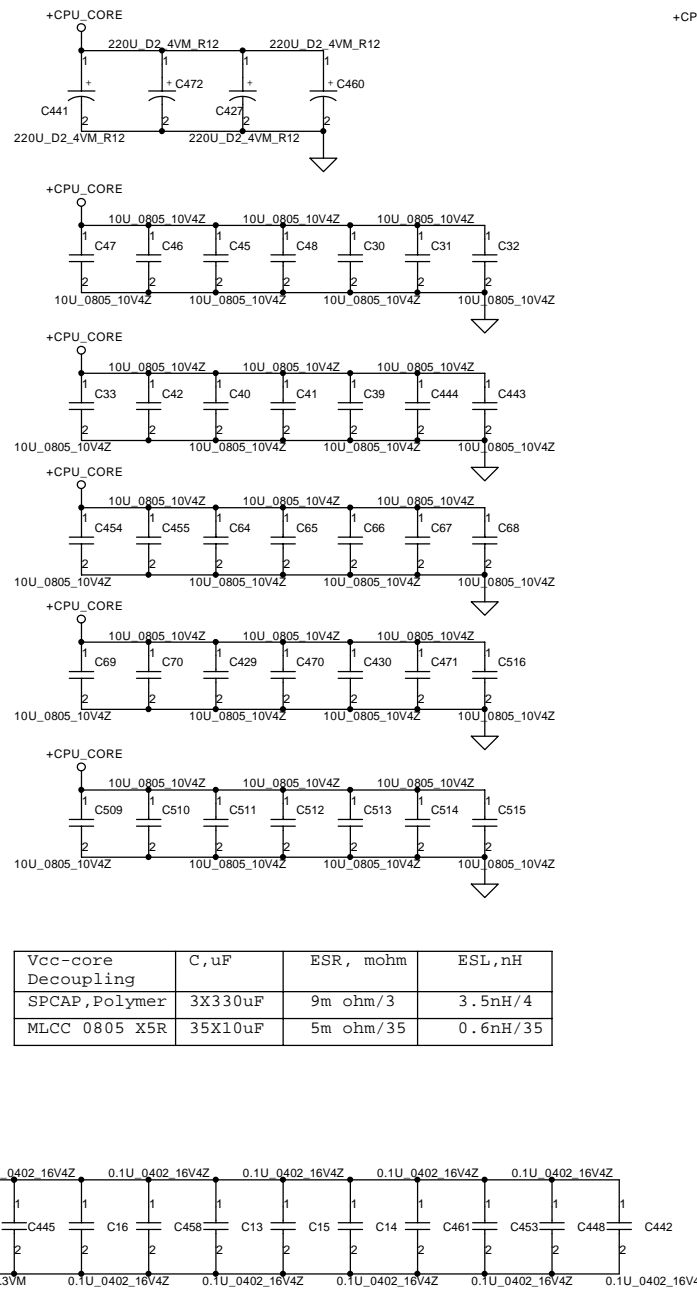
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TYCO\_1612365-1\_Dothan



**TRACE CLOSELY CPU < 0.5"**

COMP0, COMP2 layout : Width 18mils and Space 25mils  
 COMP1, COMP3 layout : Space 25mils



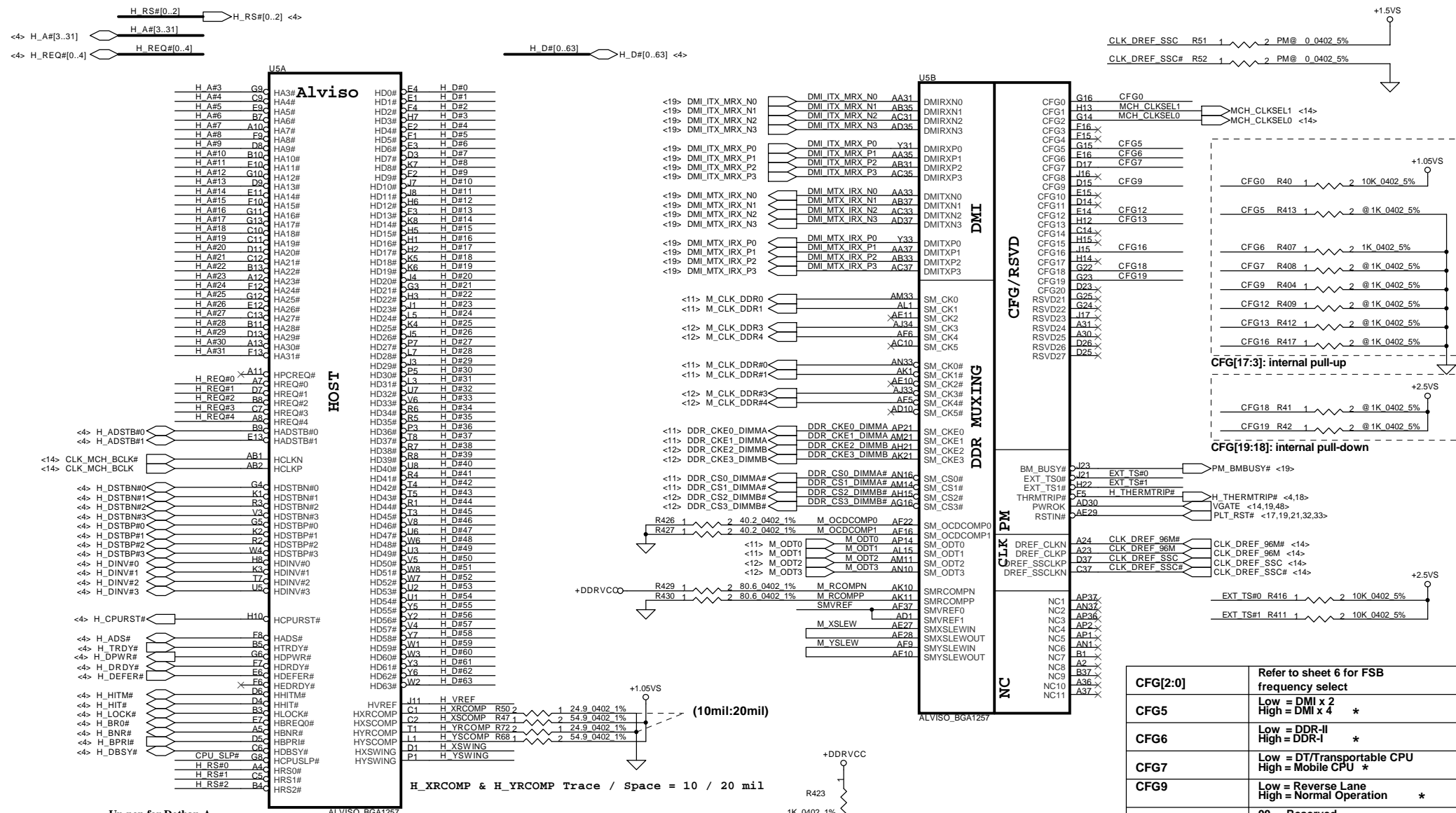
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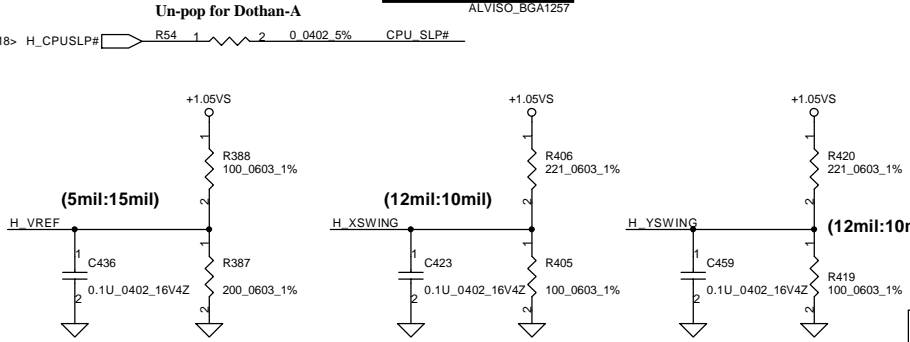
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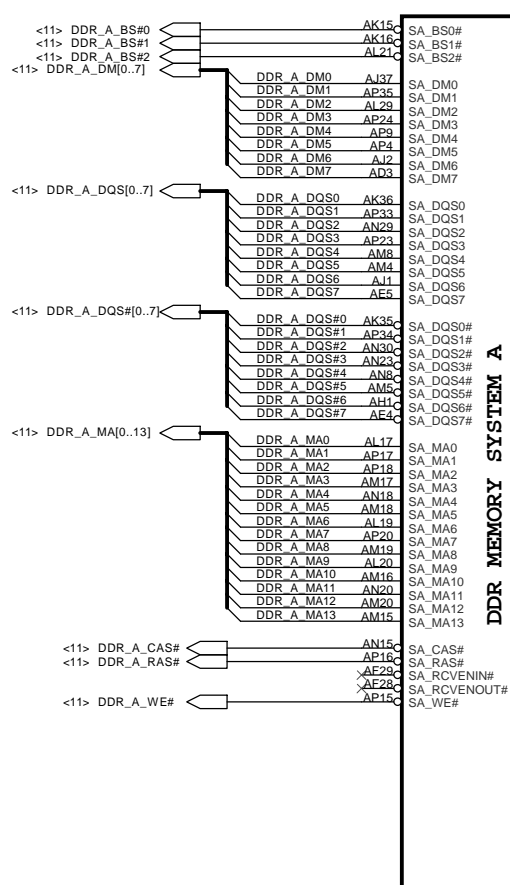
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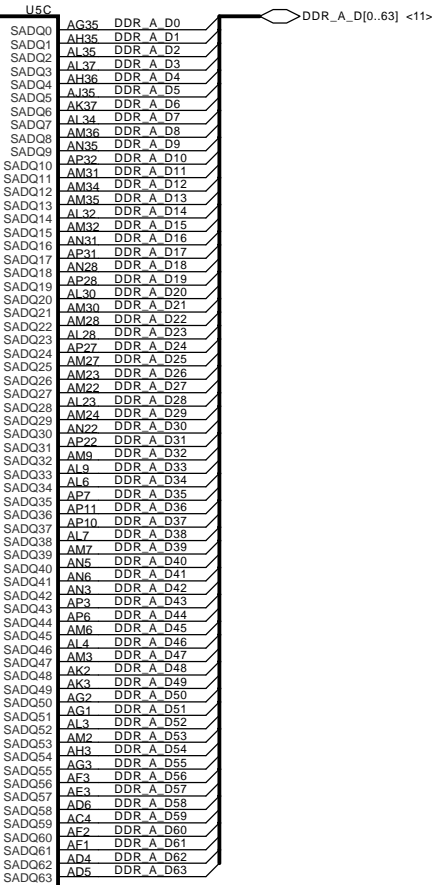
CFG[2:0]	Refer to sheet 6 for FSF frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V





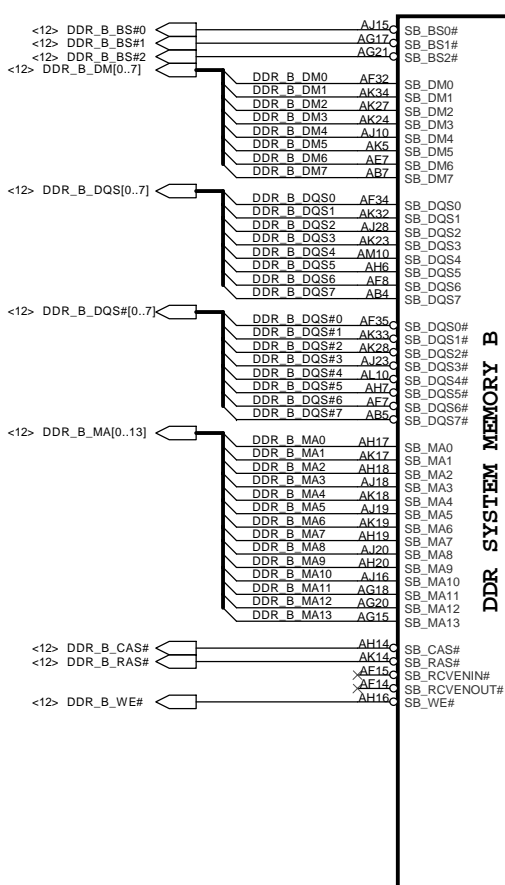
ALVISO\_BGAT257

DDR MEMORY SYSTEM A



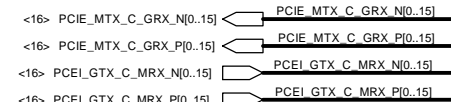
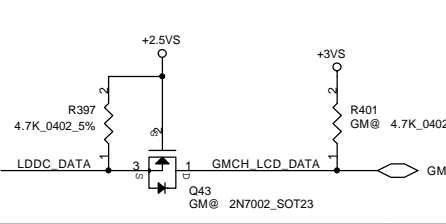
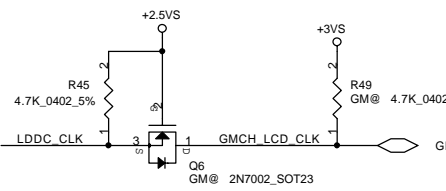
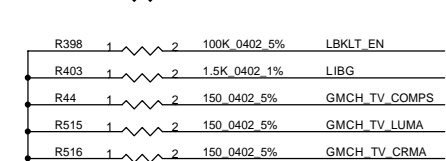
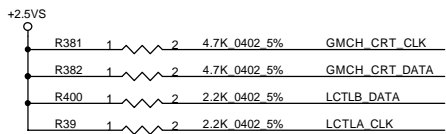
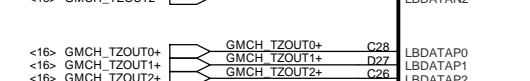
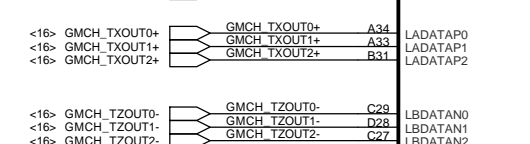
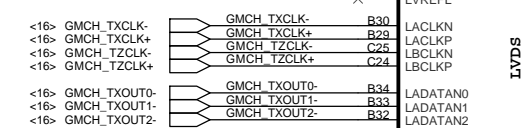
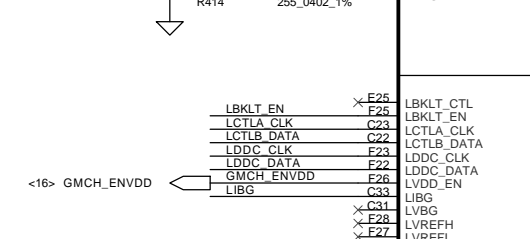
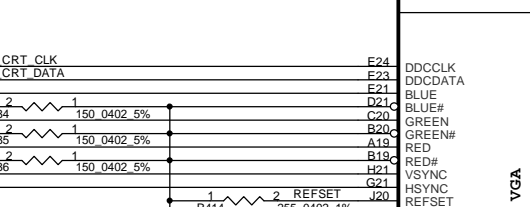
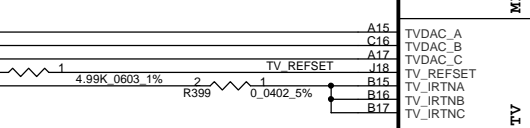
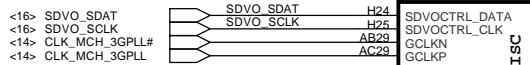
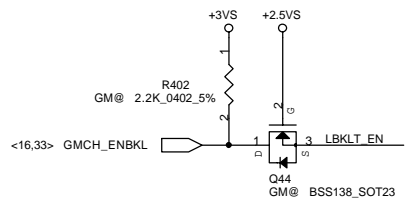
ALVISO\_BGAT257

DDR SYSTEM MEMORY B



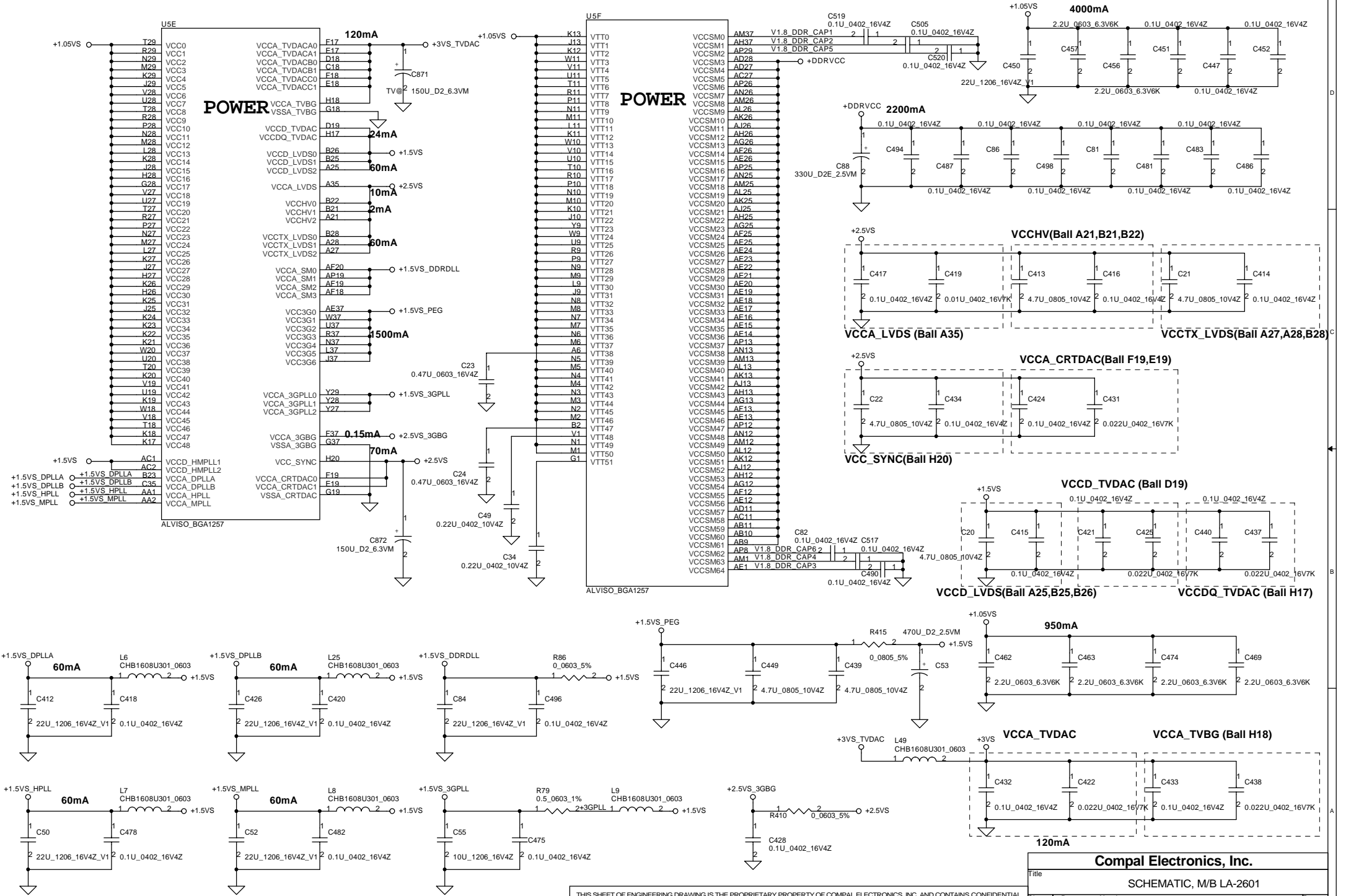
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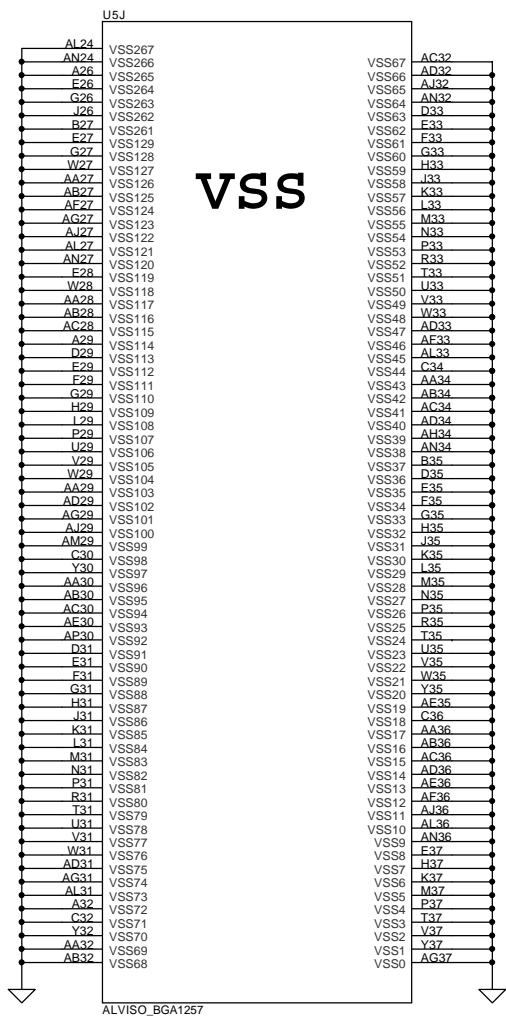
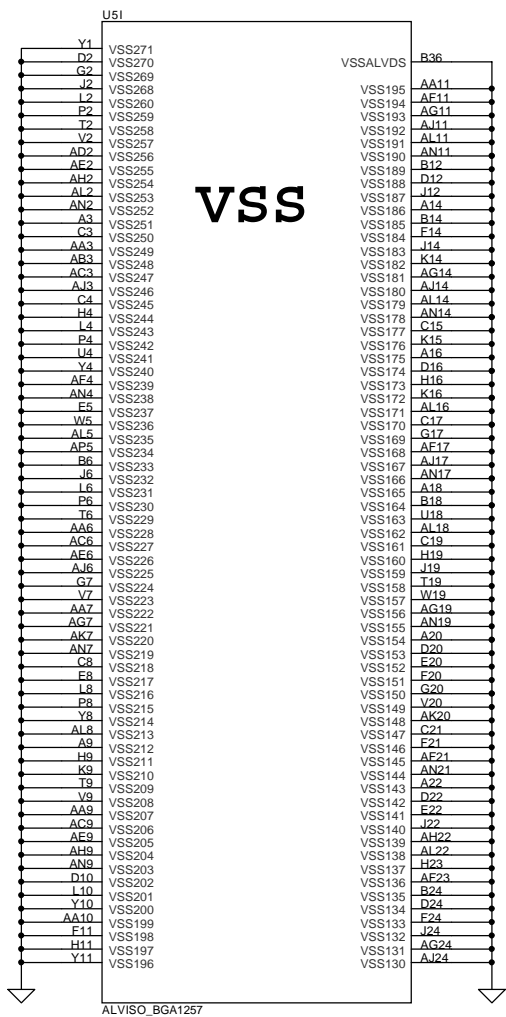
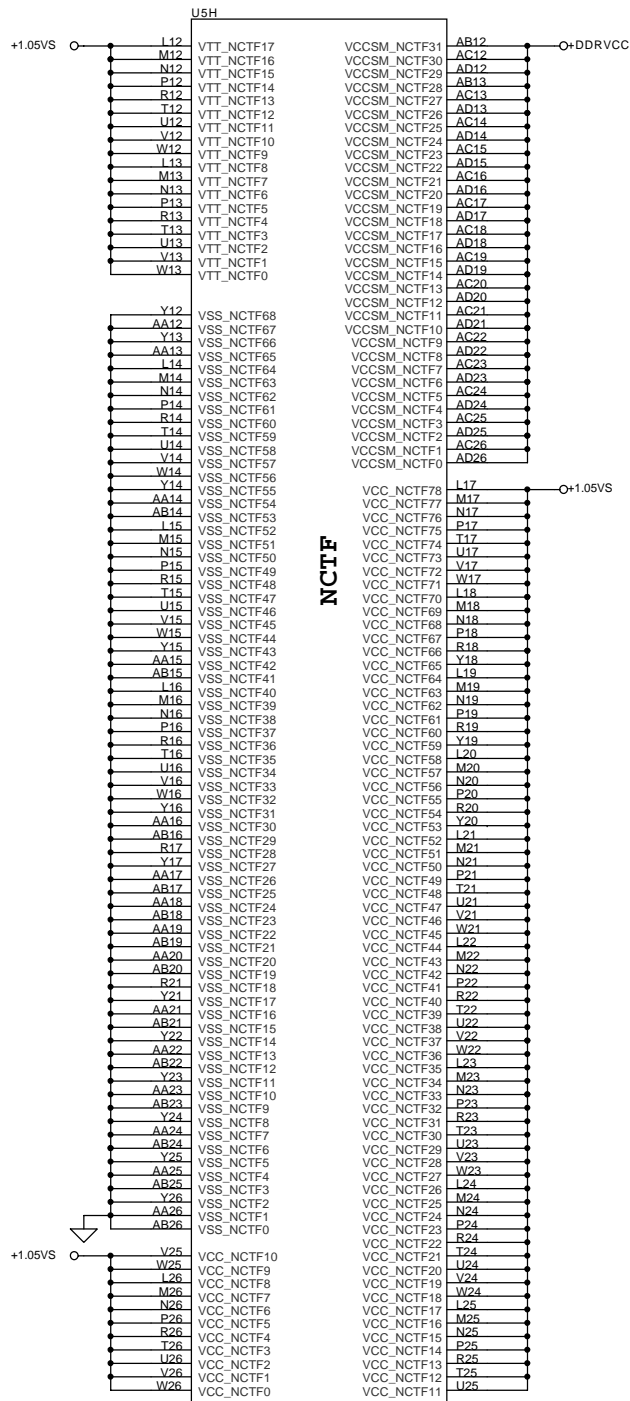
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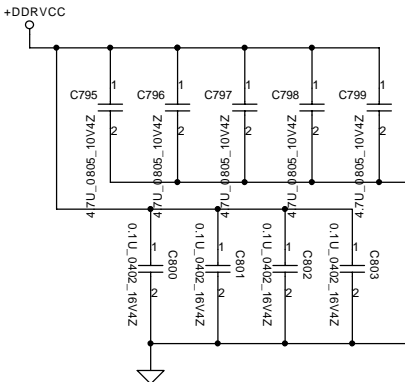
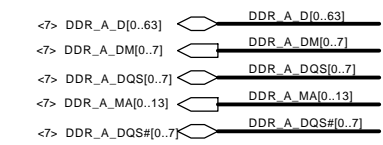
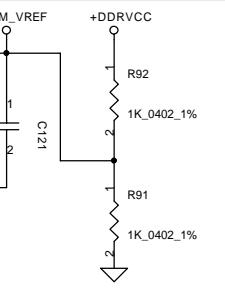
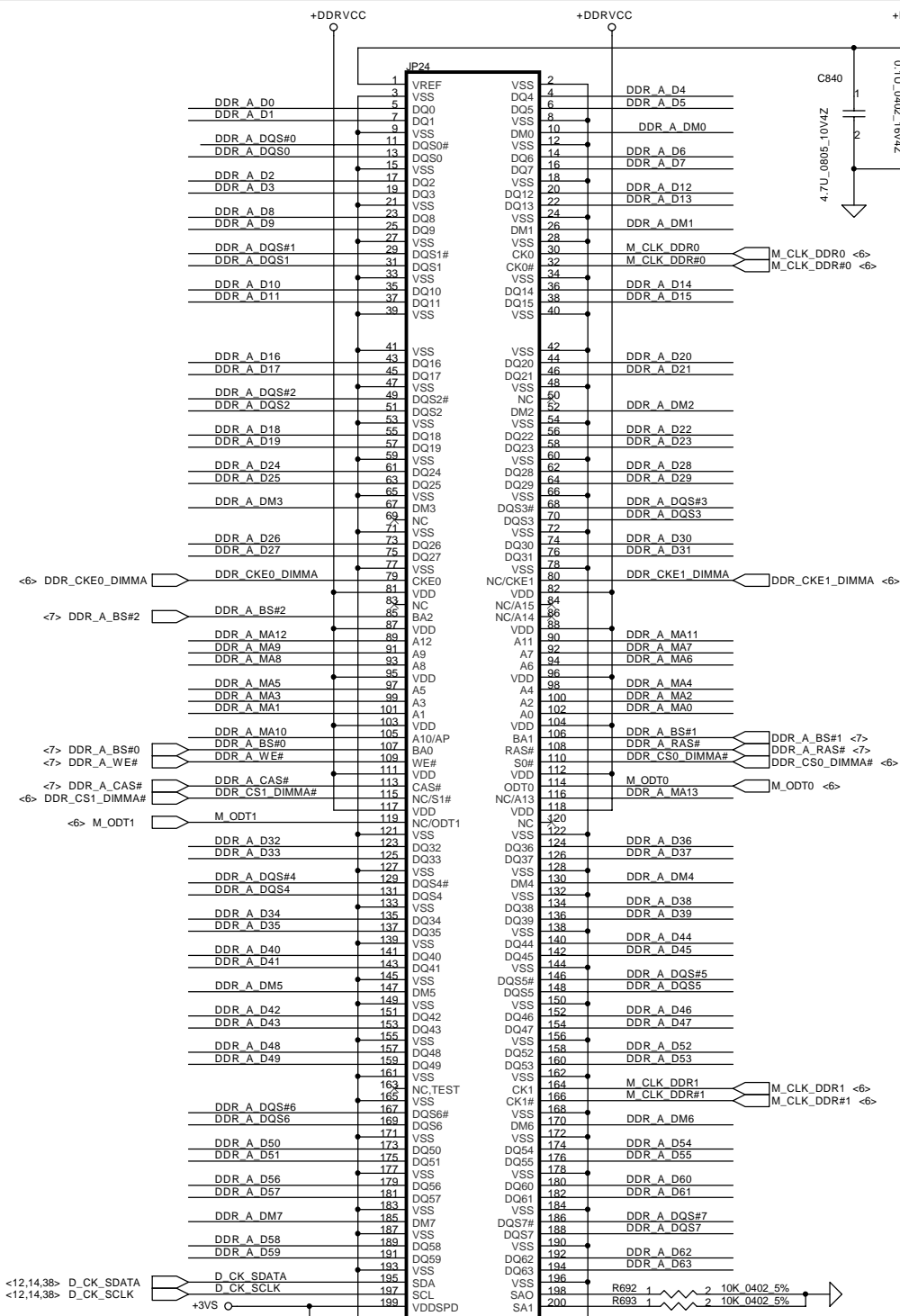


Signal	Pin	Component	Value	Notes
EXP_COMP1	D36	PEG COMP	24.9_0402_1%	+1.5VS
EXP_ICOMPO	D34			
EXP_RXN0/SDVO_TVCLKIN#	E30	PCI_E GTX C MRX N0		
EXP_RXN1/SDVO_INT#	E34	PCI_E GTX C MRX N1		
EXP_RXN2/SDVO_FLDSTALL#	G30	PCI_E GTX C MRX N2		
EXP_RXN3	H34	PCI_E GTX C MRX N3		
EXP_RXN4	J30	PCI_E GTX C MRX N4		
EXP_RXN5	K34	PCI_E GTX C MRX N5		
EXP_RXN6	L30	PCI_E GTX C MRX N6		
EXP_RXN7	M34	PCI_E GTX C MRX N7		
EXP_RXN8	N30	PCI_E GTX C MRX N8		
EXP_RXN9	P34	PCI_E GTX C MRX N9		
EXP_RXN10	R30	PCI_E GTX C MRX N10		
EXP_RXN11	T34	PCI_E GTX C MRX N11		
EXP_RXN12	U30	PCI_E GTX C MRX N12		
EXP_RXN13	V34	PCI_E GTX C MRX N13		
EXP_RXN14	W30	PCI_E GTX C MRX N14		
EXP_RXN15	Y34	PCI_E GTX C MRX N15		
EXP_RXP0/SDVO_TVCLKIN	D30	PCI_E GTX C MRX P0		
EXP_RXP1/SDVO_INT#	E34	PCI_E GTX C MRX P1		
EXP_RXP2/SDVO_FLDSTALL#	F30	PCI_E GTX C MRX P2		
EXP_RXP3	G34	PCI_E GTX C MRX P3		
EXP_RXP4	H30	PCI_E GTX C MRX P4		
EXP_RXP5	J34	PCI_E GTX C MRX P5		
EXP_RXP6	K30	PCI_E GTX C MRX P6		
EXP_RXP7	L34	PCI_E GTX C MRX P7		
EXP_RXP8	M30	PCI_E GTX C MRX P8		
EXP_RXP9	N34	PCI_E GTX C MRX P9		
EXP_RXP10	P30	PCI_E GTX C MRX P10		
EXP_RXP11	R34	PCI_E GTX C MRX P11		
EXP_RXP12	T30	PCI_E GTX C MRX P12		
EXP_RXP13	U34	PCI_E GTX C MRX P13		
EXP_RXP14	V30	PCI_E GTX C MRX P14		
EXP_RXP15	W34	PCI_E GTX C MRX P15		
EXP_TXN0/SDVOB_RED#	E32	PCI_E MTX GRX N0	C57 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N0
EXP_TXN1/SDVOB_GREEN#	F36	PCI_E MTX GRX N1	C59 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N1
EXP_TXN2/SDVOB_BLUE#	G32	PCI_E MTX GRX N2	C62 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N2
EXP_TXN3/SDVOB_CLKN	H36	PCI_E MTX GRX N3	C71 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N3
EXP_TXN4/SDVOC_RED#	J32	PCI_E MTX GRX N4	C74 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N4
EXP_TXN5/SDVOC_GREEN#	K36	PCI_E MTX GRX N5	C76 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N5
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EXP_TXN7/SDVOC_CLKN	M36	PCI_E MTX GRX N7	C80 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N7
EXP_TXN8	P36	PCI_E MTX GRX N8	C91 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N8
EXP_TXN9	R32	PCI_E MTX GRX N9	C97 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N9
EXP_TXN10	T36	PCI_E MTX GRX N10	C100 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N10
EXP_TXN11	U32	PCI_E MTX GRX N11	C104 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N11
EXP_TXN12	V36	PCI_E MTX GRX N12	C109 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N12
EXP_TXN13	W32	PCI_E MTX GRX N13	C114 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N13
EXP_TXN14	Y36	PCI_E MTX GRX N14	C116 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX N14
EXP_TXN15				
EXP_TXP0/SDVOB_RED	D32	PCI_E MTX GRX P0	C56 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P0
EXP_TXP1/SDVOB_GREEN	E36	PCI_E MTX GRX P1	C58 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P1
EXP_TXP2/SDVOB_BLUE	F32	PCI_E MTX GRX P2	C61 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P2
EXP_TXP3/SDVOB_CLKP	G36	PCI_E MTX GRX P3	C63 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P3
EXP_TXP4/SDVOC_RED	H32	PCI_E MTX GRX P4	C73 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P4
EXP_TXP5/SDVOC_GREEN	J36	PCI_E MTX GRX P5	C75 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P5
EXP_TXP6/SDVOC_BLUE	K32	PCI_E MTX GRX P6	C77 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P6
EXP_TXP7/SDVOC_CLKP	L36	PCI_E MTX GRX P7	C79 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P7
EXP_TXP8	M32	PCI_E MTX GRX P8	C83 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P8
EXP_TXP9	N36	PCI_E MTX GRX P9	C89 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P9
EXP_TXP10	P32	PCI_E MTX GRX P10	C92 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P10
EXP_TXP11	R36	PCI_E MTX GRX P11	C98 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P11
EXP_TXP12	T32	PCI_E MTX GRX P12	C101 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P12
EXP_TXP13	U36	PCI_E MTX GRX P13	C105 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P13
EXP_TXP14	V32	PCI_E MTX GRX P14	C110 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P14
EXP_TXP15	W36	PCI_E MTX GRX P15	C115 1	2 DVI@ 0.1U 0402 16V4Z PCIE MTX C GRX P15

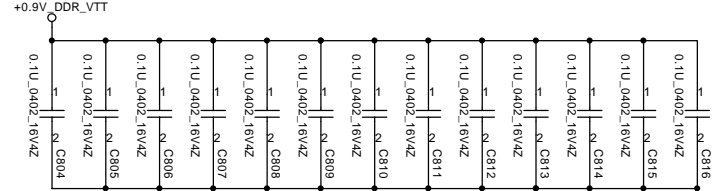




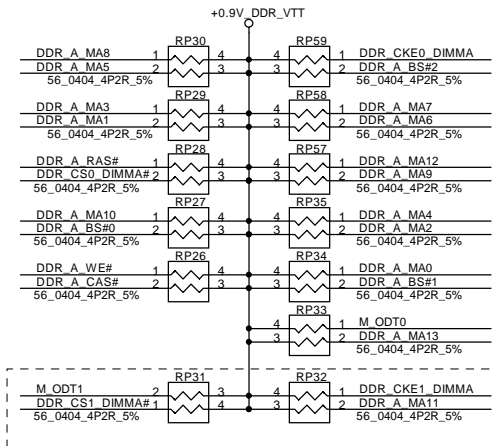




Layout Note:  
Place near DIMM



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



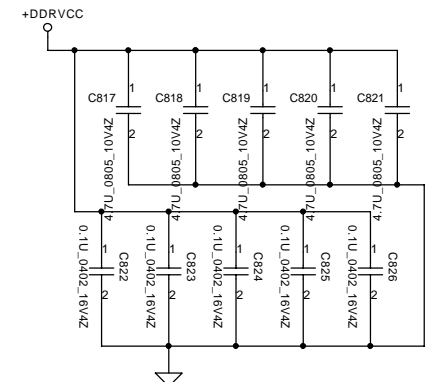
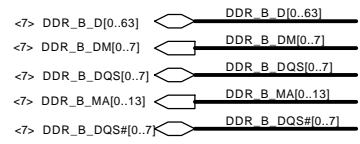
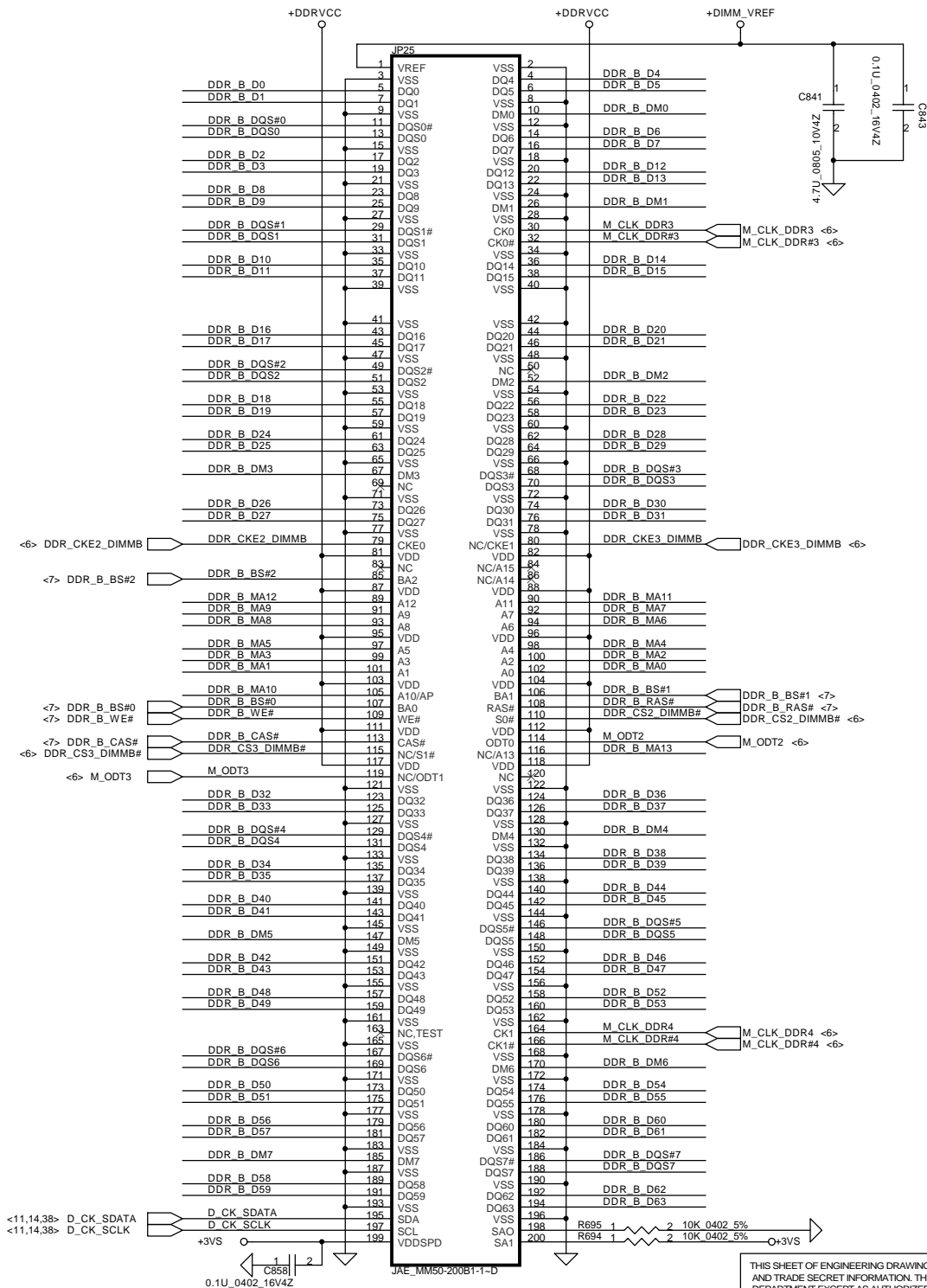
Layout Note:  
Place these resistor closely DIMM0, all trace length < 750 mil

Layout Note:  
Place these resistor closely DIMM0, all trace length Max=1.3"

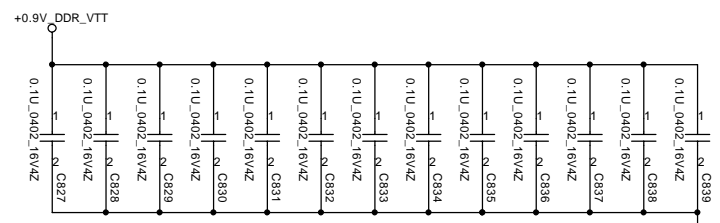


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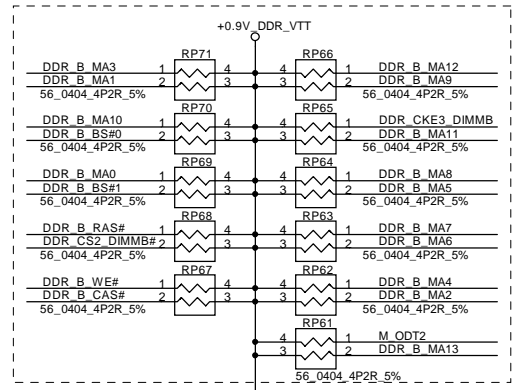
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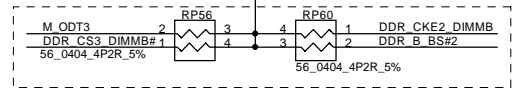
Layout Note:  
Place near DIMM



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



Layout Note:  
Place these resistor closely DIMM0, all trace length < 750 mil

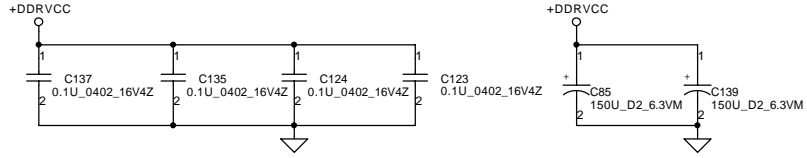
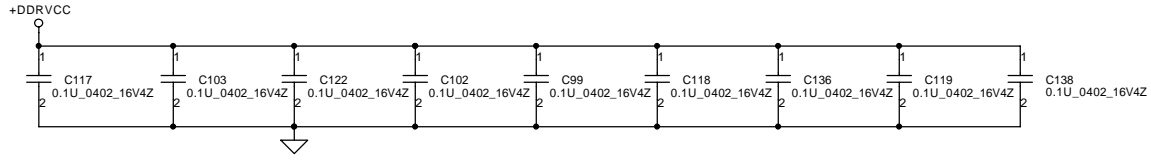


Layout Note:  
Place these resistor closely DIMM0, all trace length Max=1.3"

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**Layout note :**  
Distribute as close as possible  
to DDR-SODIMM.



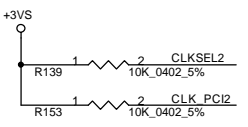
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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

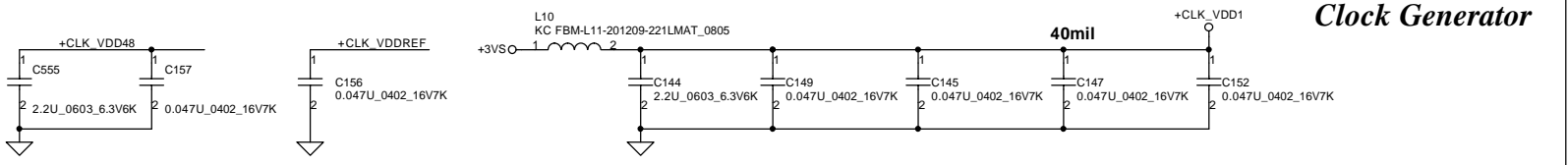
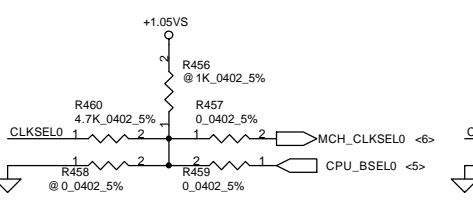
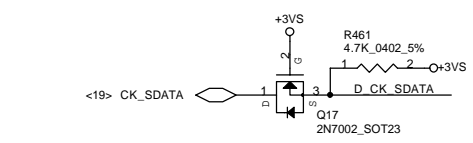
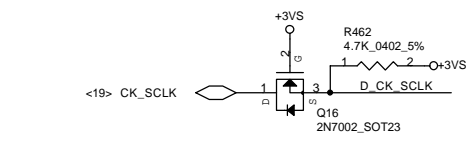
Table : ICS 954206B

CLK\_PCI2 = 1, Pin 32,33 are PEREQ# pin

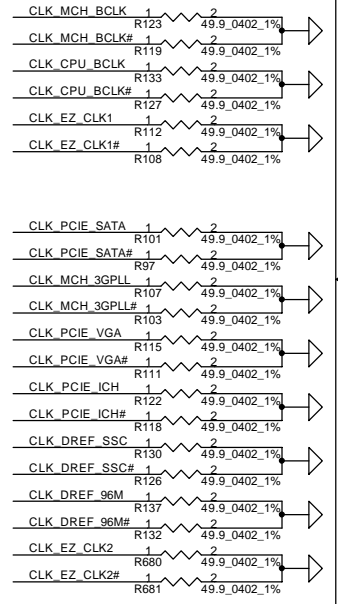
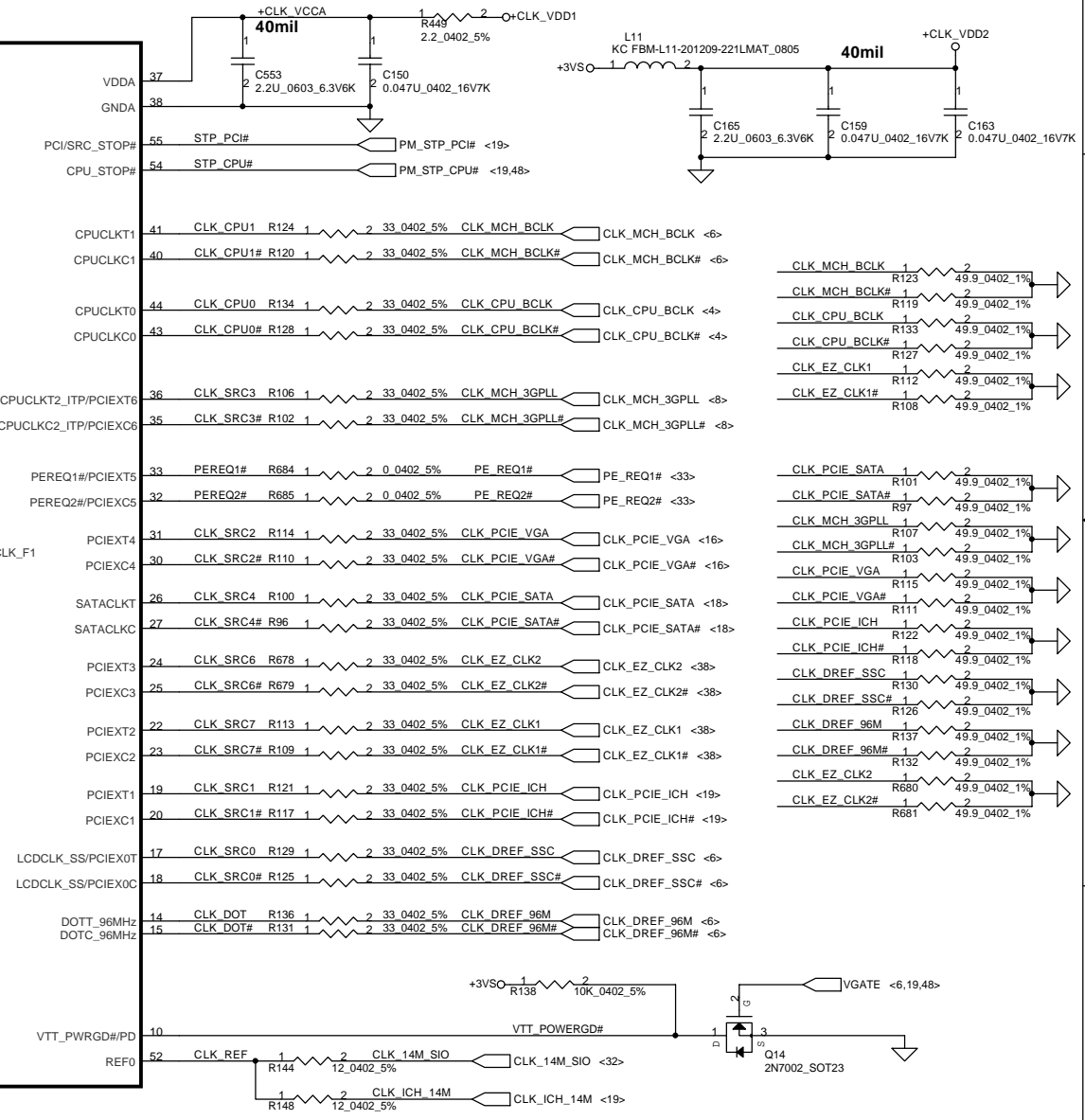
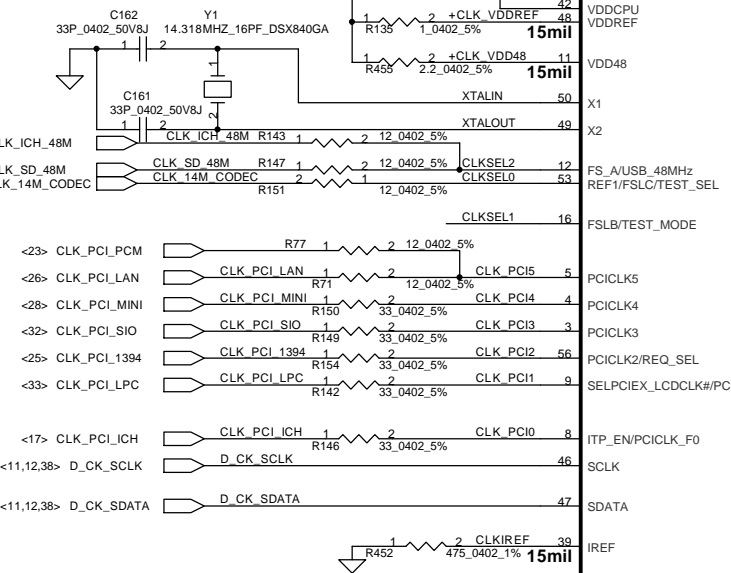


CLK\_PCIO = 0, Pin 35,36 are PCIe CLK pair

CLK\_PC11 = 0, Pin 17,18 are 96MHz



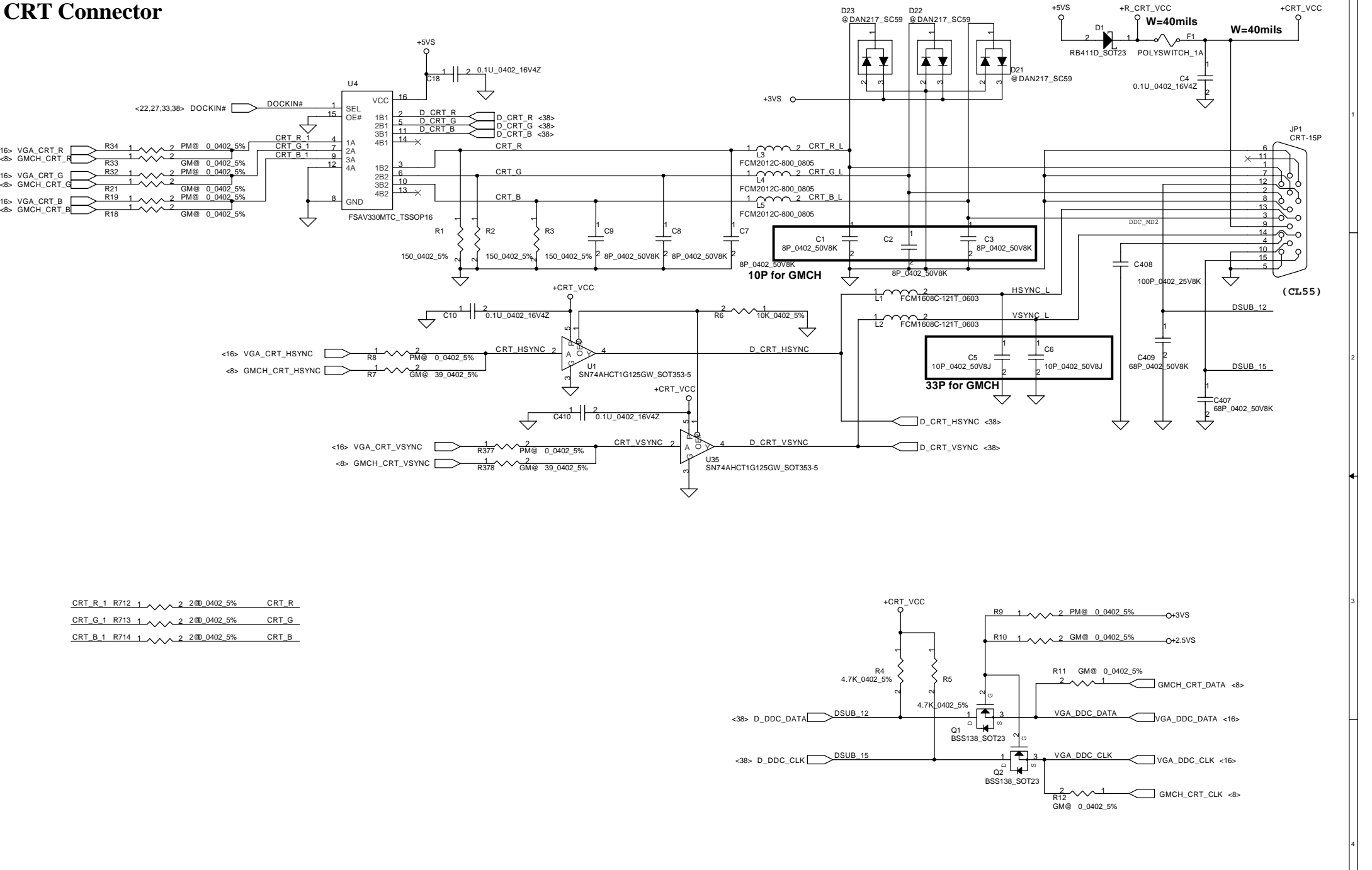
# Clock Generator



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# CRT Connector

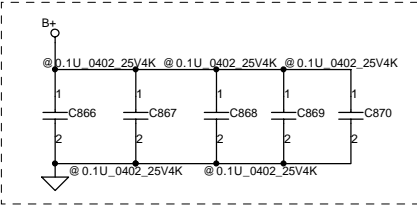
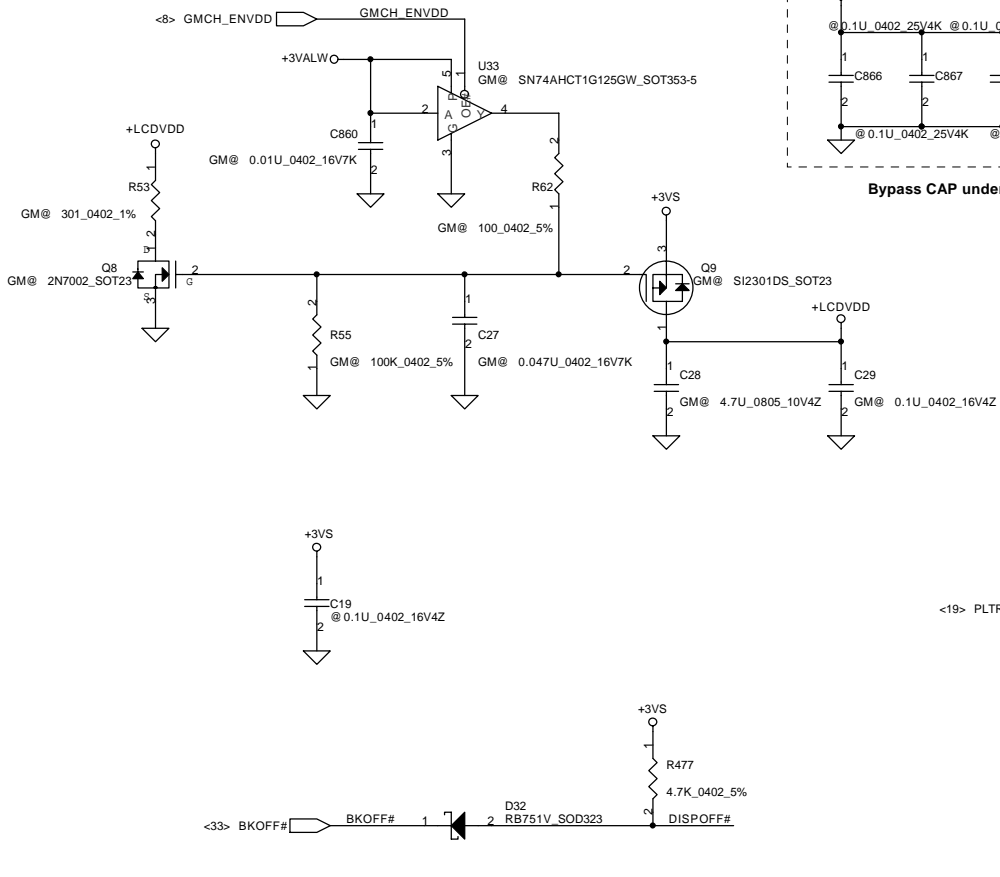


- CRT\_R\_1 R712 1 2 2@ 0.0402\_5% CRT\_R
- CRT\_G\_1 R713 1 2 2@ 0.0402\_5% CRT\_G
- CRT\_B\_1 R714 1 2 2@ 0.0402\_5% CRT\_B

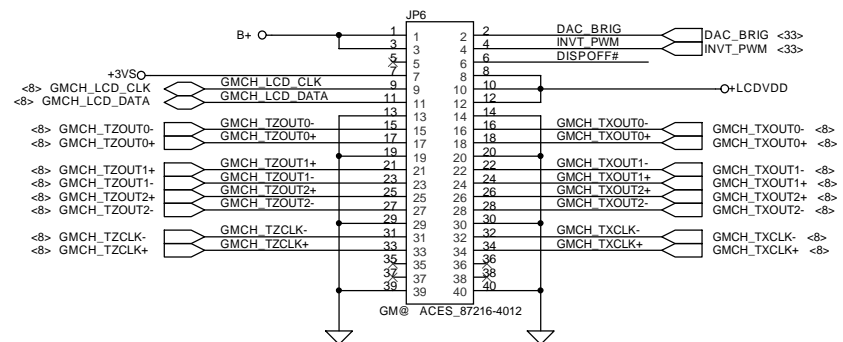
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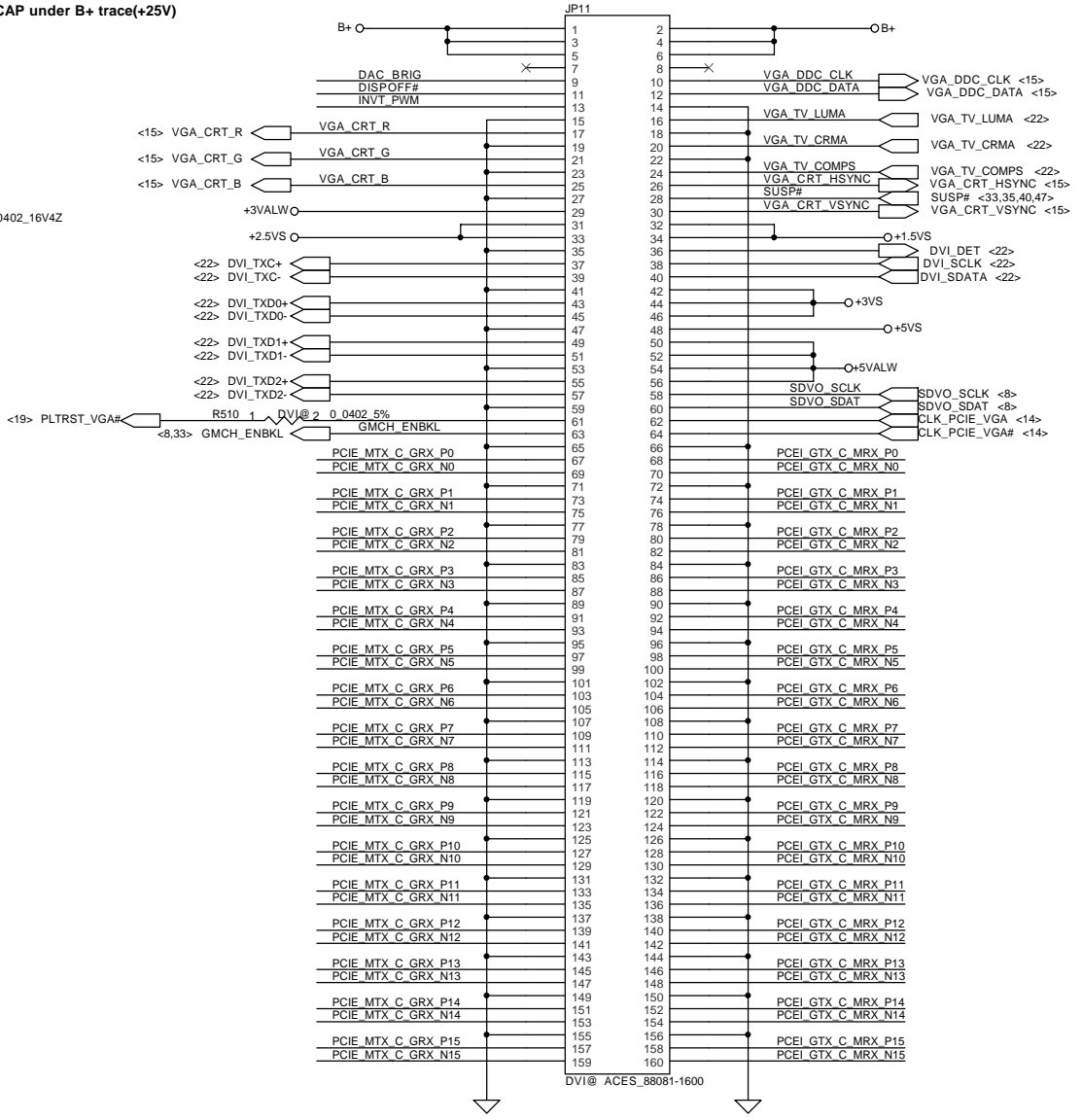
# LCD POWER CIRCUIT



# LCD/PANEL BD. Conn.



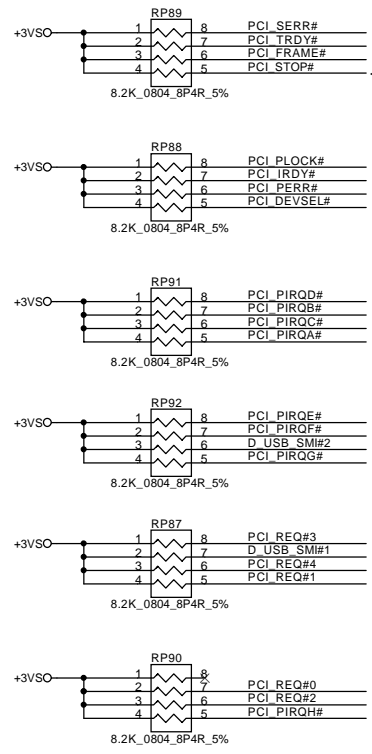
# VGA BOARD Conn.



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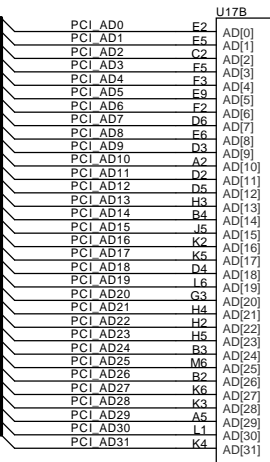


<23,25,26,28> PCI\_AD[0..31]

<23,25,26,28> PCI\_FRAME#

<23> PCI\_PIRQA#

<23> PCI\_PIRQB#



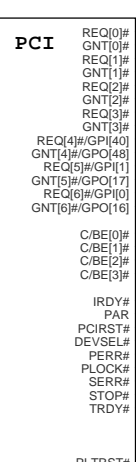
PCI\_FRAME# J3

PCI\_PIRQA# N2

PCI\_PIRQB# L2

PCI\_PIROC# M1

PCI\_PIRQD# L3



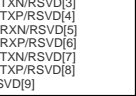
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PCI\_PIRQA# N2

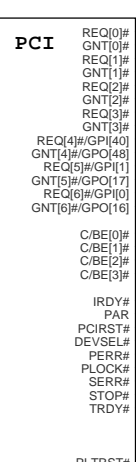
PCI\_PIRQB# L2

PCI\_PIROC# M1

PCI\_PIRQD# L3



ICH6\_BGA609



FRAME#

Interrupt I/F

PIRQ[A]# PIRQ[E]#/GPI[2]

PIRQ[B]# PIRQ[F]#/GPI[3]

PIRQ[C]# PIRQ[G]#/GPI[4]

PIRQ[D]# PIRQ[H]#/GPI[5]

RESERVED

PIRQ[E]# PIRQ[I]#/GPI[6]

PIRQ[F]# PIRQ[J]#/GPI[7]

PIRQ[G]# PIRQ[K]#/GPI[8]

PIRQ[H]# PIRQ[L]#/GPI[9]

PIRQ[I]# PIRQ[M]#/GPI[10]

PIRQ[J]# PIRQ[N]#/GPI[11]

PIRQ[K]# PIRQ[O]#/GPI[12]

PIRQ[L]# PIRQ[P]#/GPI[13]

PIRQ[M]# PIRQ[Q]#/GPI[14]

PIRQ[N]# PIRQ[R]#/GPI[15]

PIRQ[O]# PIRQ[S]#/GPI[16]

PIRQ[P]# PIRQ[T]#/GPI[17]

PIRQ[Q]# PIRQ[U]#/GPI[18]

PIRQ[R]# PIRQ[V]#/GPI[19]

PIRQ[S]# PIRQ[W]#/GPI[20]

PIRQ[T]# PIRQ[X]#/GPI[21]

PIRQ[U]# PIRQ[Y]#/GPI[22]

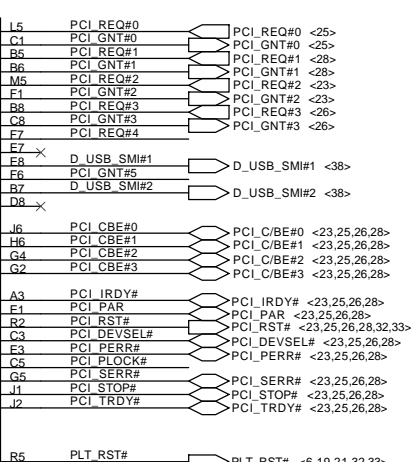
PIRQ[V]# PIRQ[Z]#/GPI[23]

PIRQ[W]# PIRQ[AA]#/GPI[24]

PIRQ[X]# PIRQ[AB]#/GPI[25]

PIRQ[Y]# PIRQ[AC]#/GPI[26]

PIRQ[Z]# PIRQ[AD]#/GPI[27]



PLTRST# PLT\_RST# <6,19,21,32,33>

PCICLK CLK\_ICH\_PCI CLK\_PCI\_ICH <14>

PME#

PIRQ[A]# PIRQ[E]#/GPI[2]

PIRQ[B]# PIRQ[F]#/GPI[3]

PIRQ[C]# PIRQ[G]#/GPI[4]

PIRQ[D]# PIRQ[H]#/GPI[5]

RESERVED

PIRQ[E]# PIRQ[I]#/GPI[6]

PIRQ[F]# PIRQ[J]#/GPI[7]

PIRQ[G]# PIRQ[K]#/GPI[8]

PIRQ[H]# PIRQ[L]#/GPI[9]

PIRQ[I]# PIRQ[M]#/GPI[10]

PIRQ[J]# PIRQ[N]#/GPI[11]

PIRQ[K]# PIRQ[O]#/GPI[12]

PIRQ[L]# PIRQ[P]#/GPI[13]

PIRQ[M]# PIRQ[Q]#/GPI[14]

PIRQ[N]# PIRQ[R]#/GPI[15]

PIRQ[O]# PIRQ[S]#/GPI[16]

PIRQ[P]# PIRQ[T]#/GPI[17]

PIRQ[Q]# PIRQ[U]#/GPI[18]

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PIRQ[S]# PIRQ[W]#/GPI[20]

PIRQ[T]# PIRQ[X]#/GPI[21]

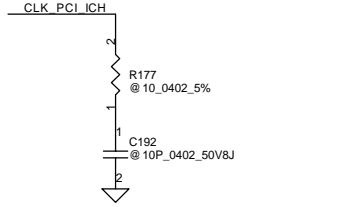
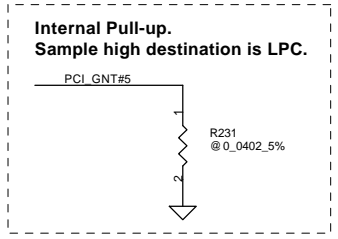
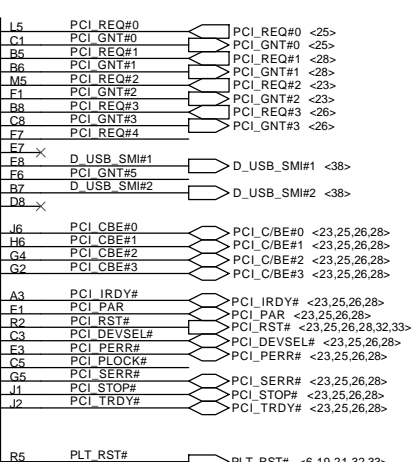
PIRQ[U]# PIRQ[Y]#/GPI[22]

PIRQ[V]# PIRQ[Z]#/GPI[23]

PIRQ[W]# PIRQ[AA]#/GPI[24]

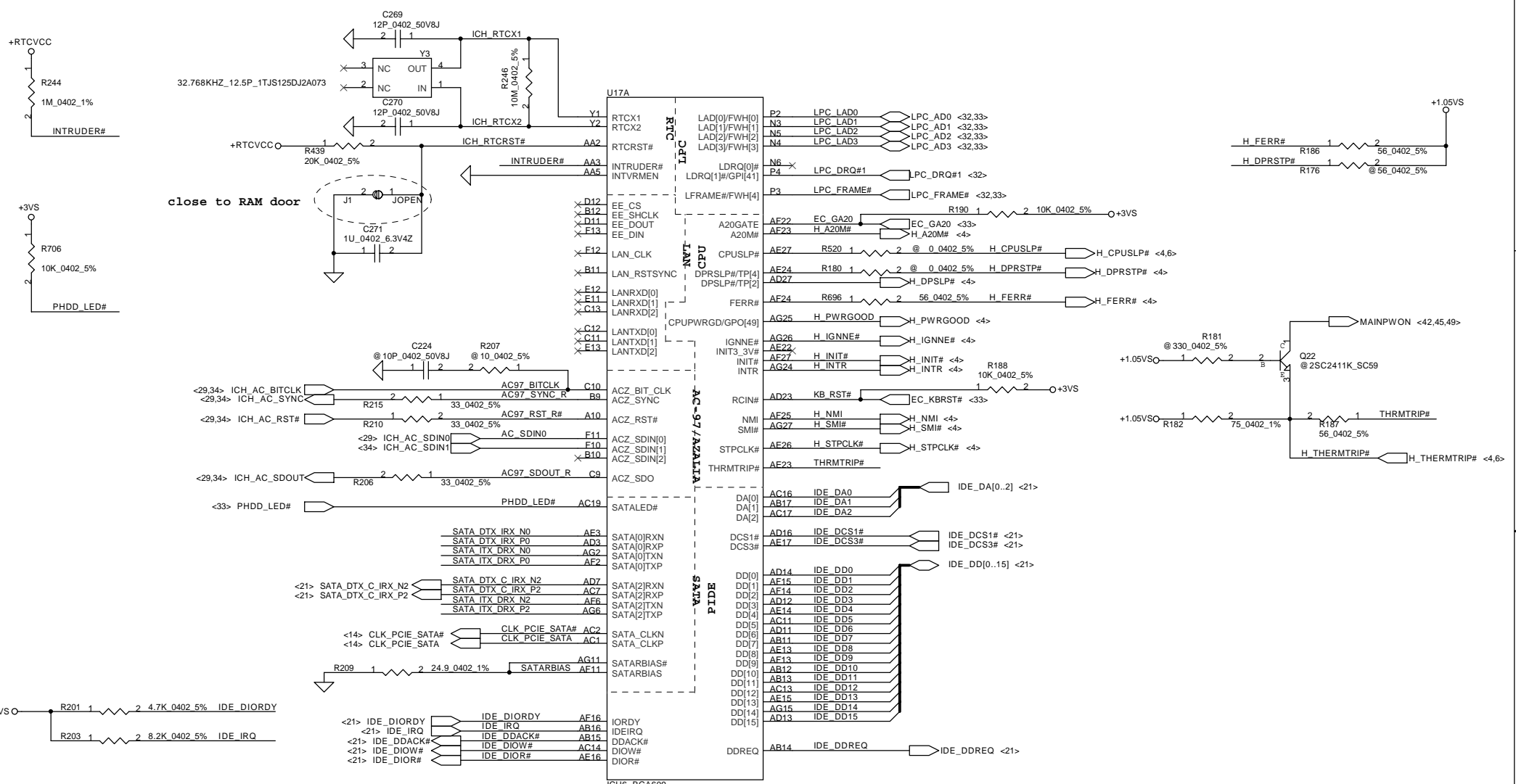
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PIRQ[Y]# PIRQ[AC]#/GPI[26]

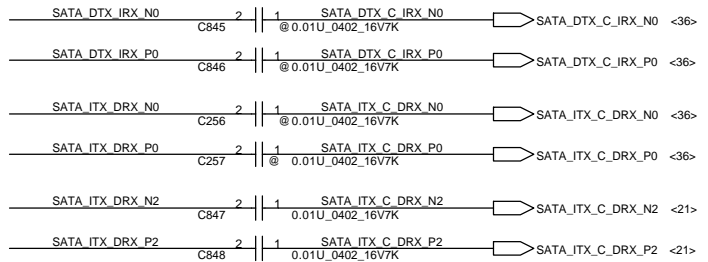


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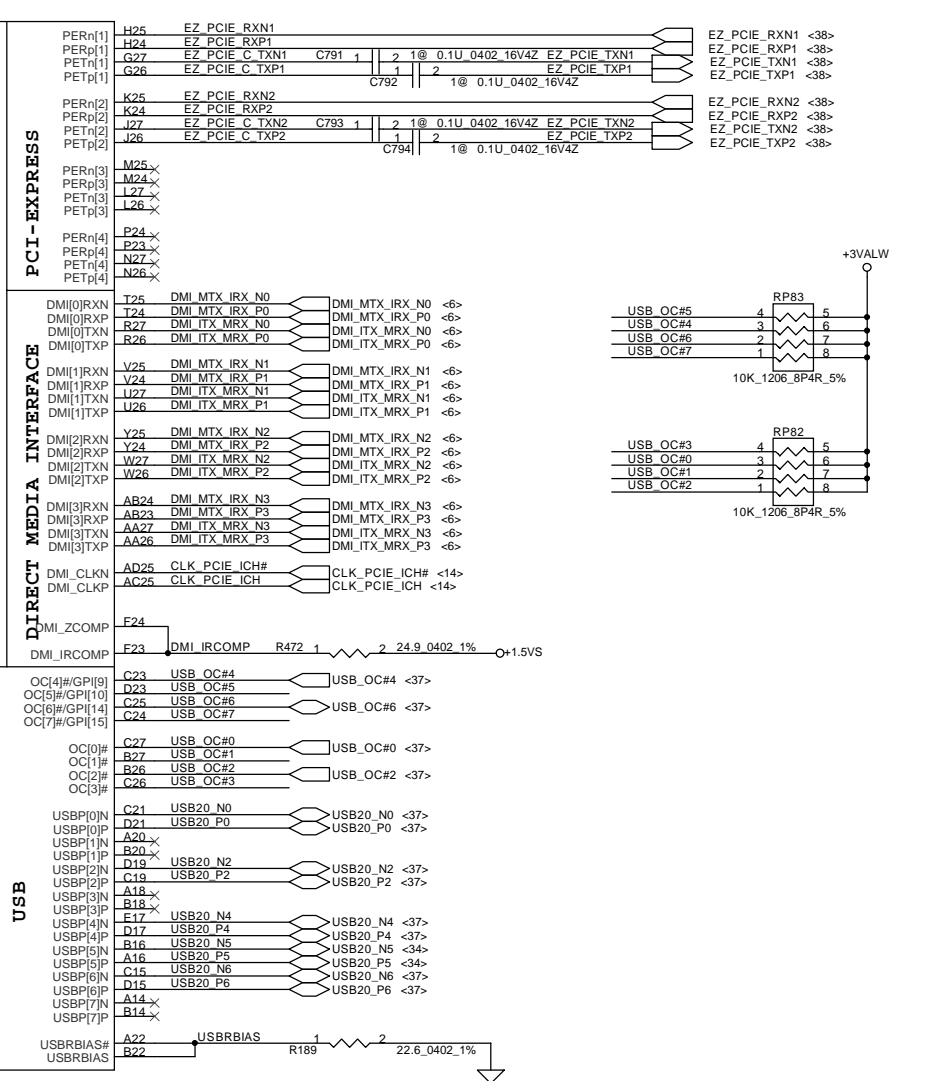
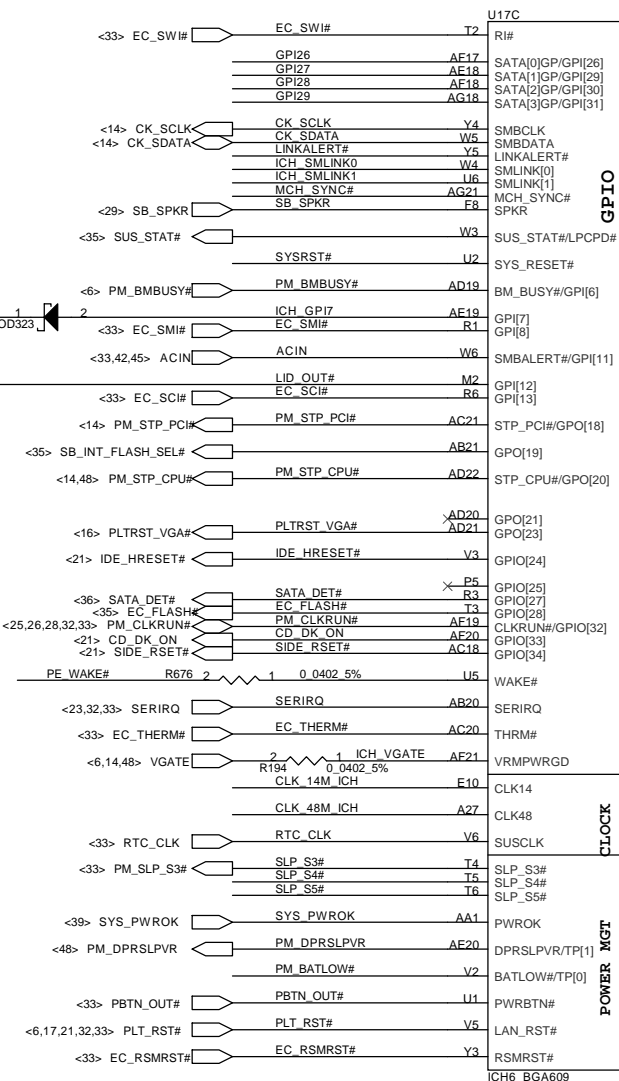
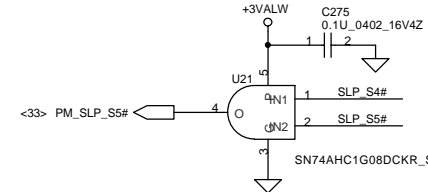
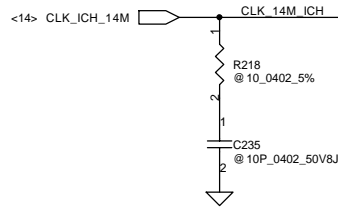
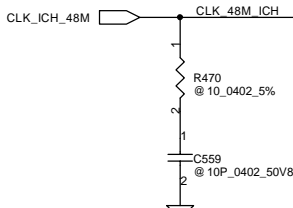
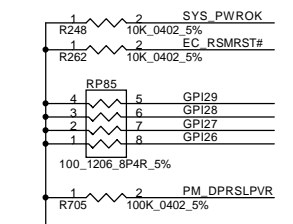
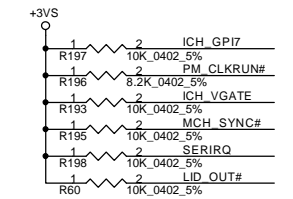
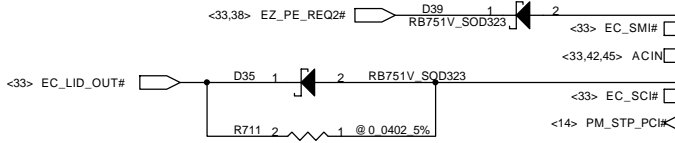
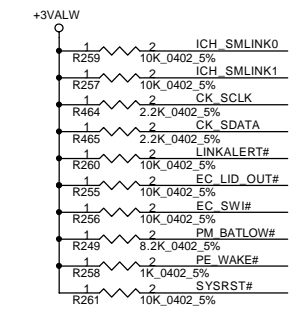


Place near ICH6 side.



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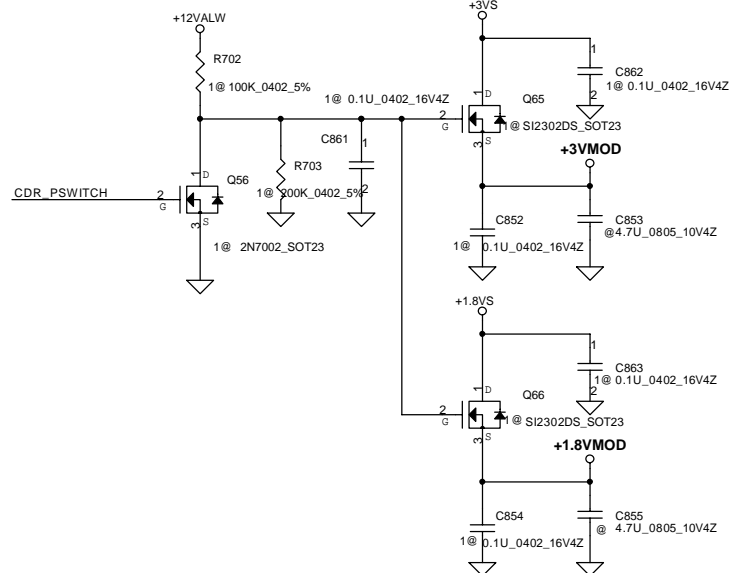
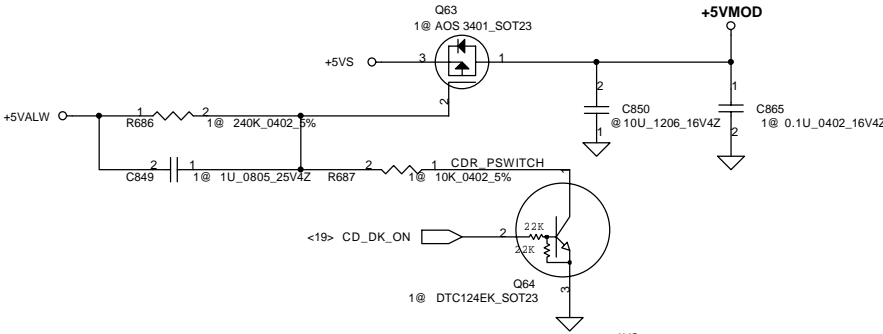
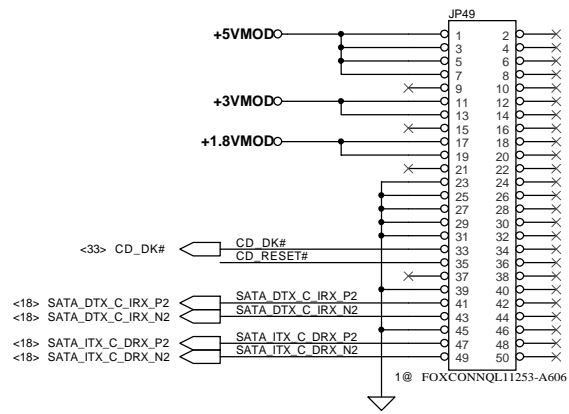


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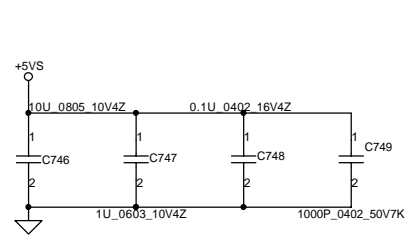
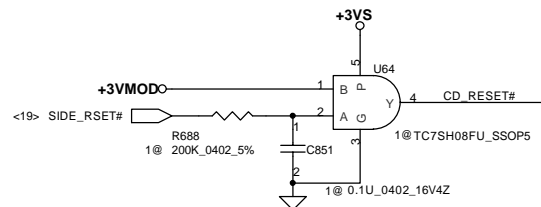
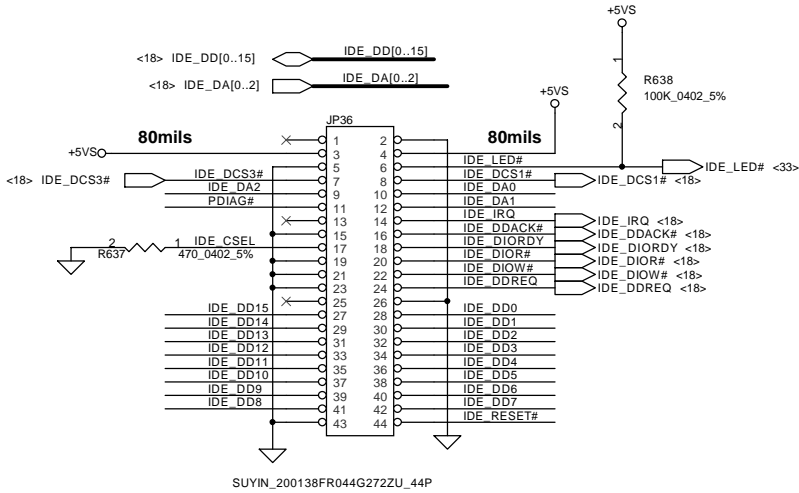
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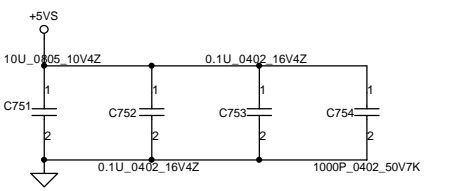
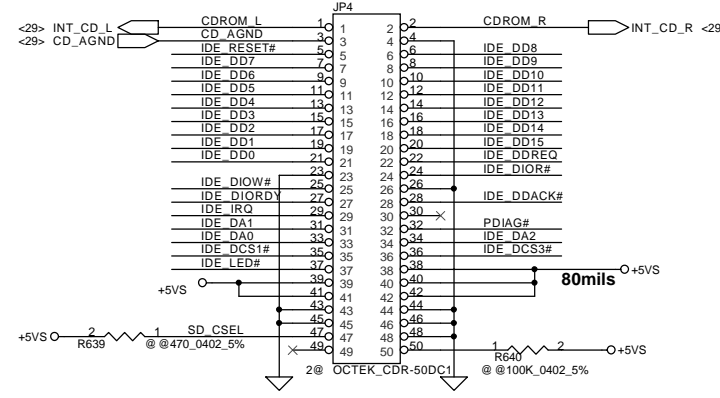
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### HDD CONN

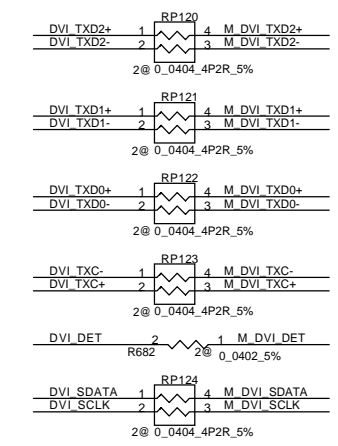
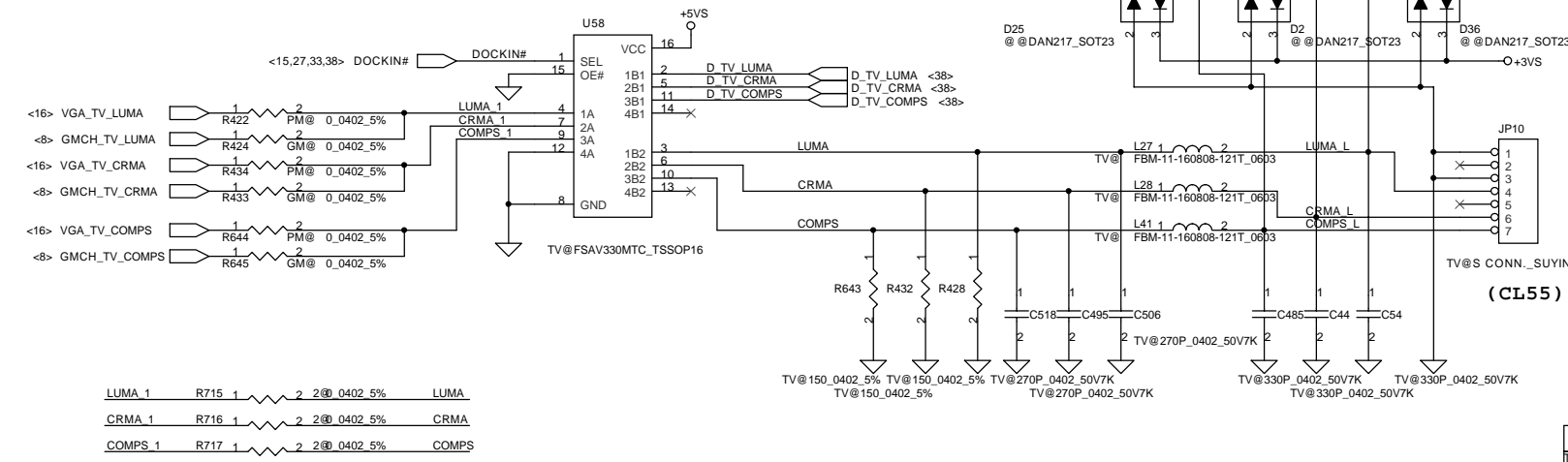
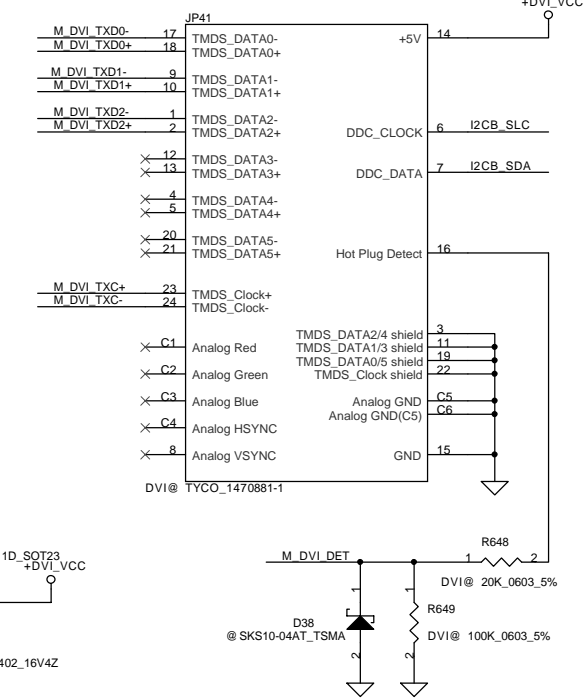
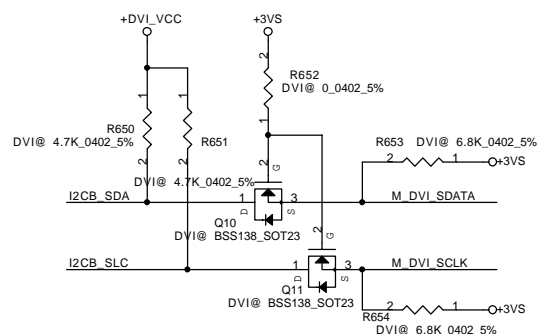
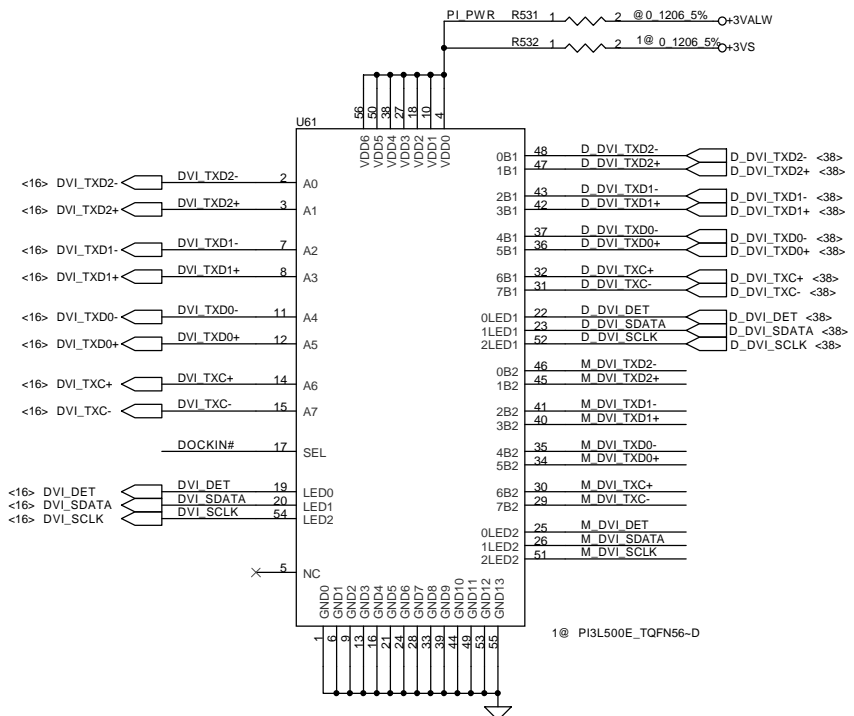


### CDROM CONN



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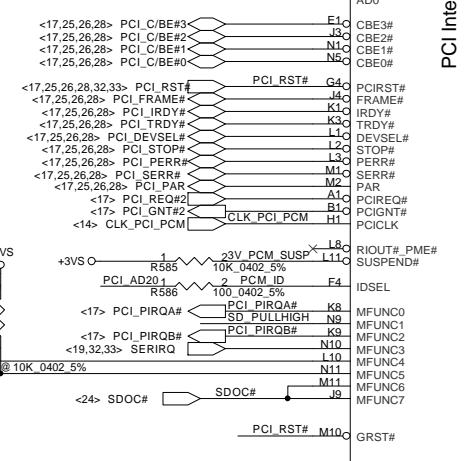
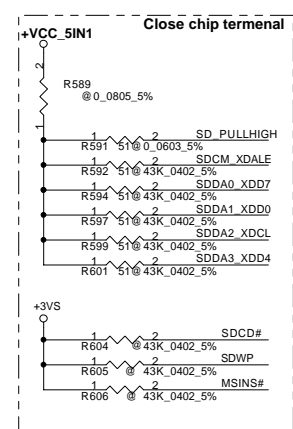
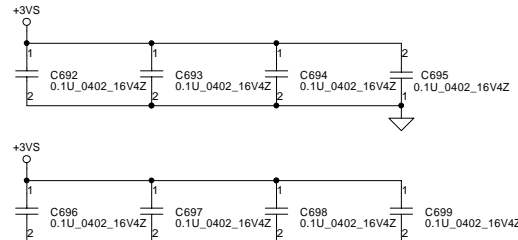
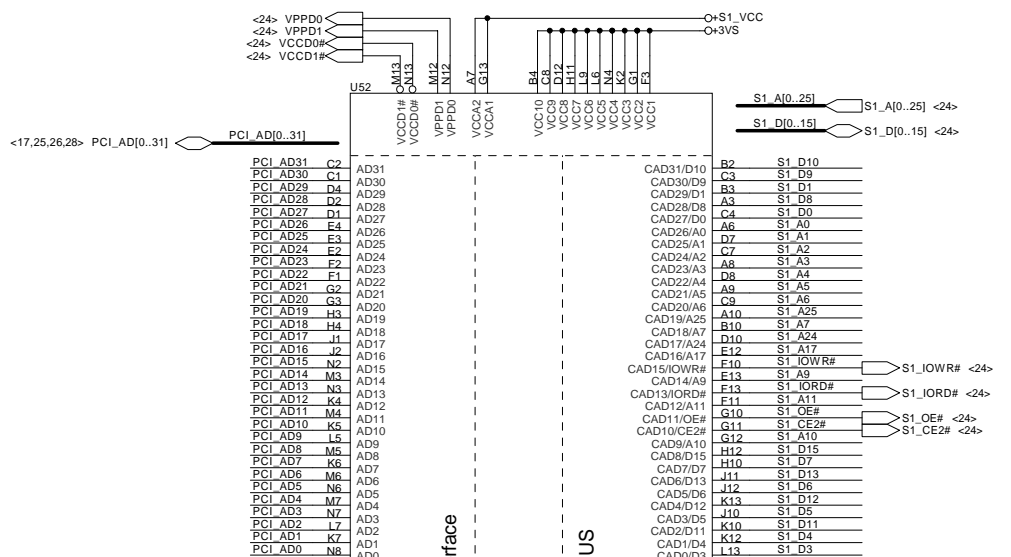
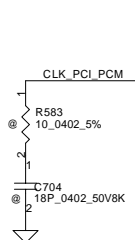
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LUMA 1	R715	1	2	2@ 0.402 5%	LUMA
CRMA 1	R716	1	2	2@ 0.402 5%	CRMA
COMPS 1	R717	1	2	2@ 0.402 5%	COMPS

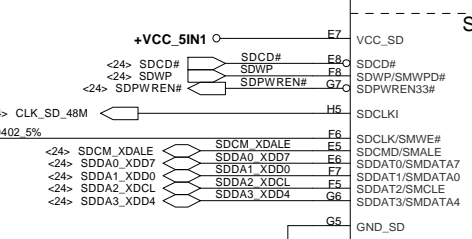
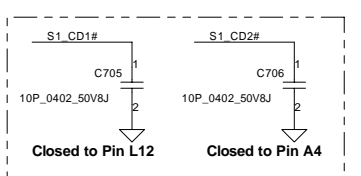
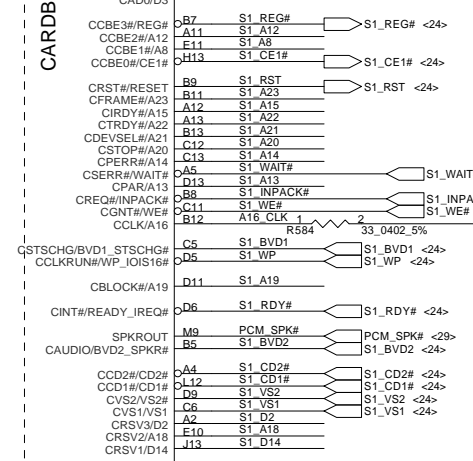
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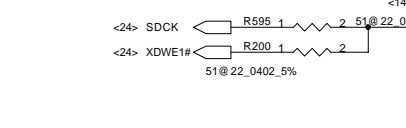
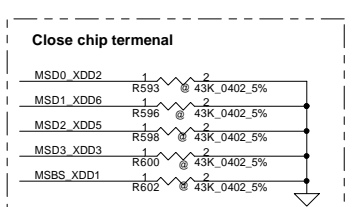
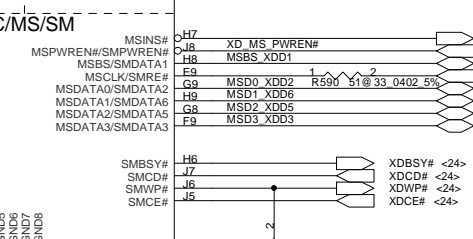


PCI Interface

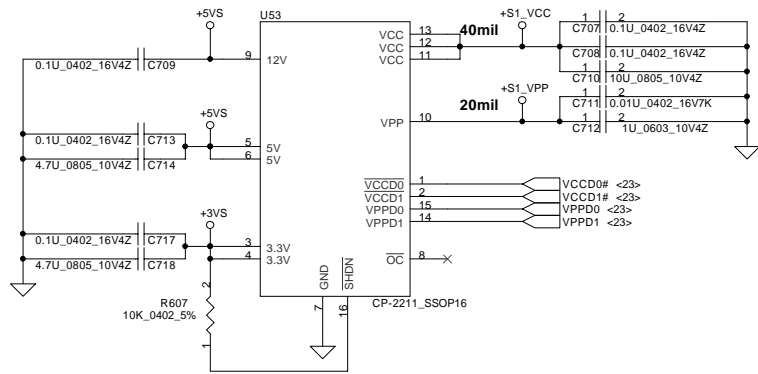
CARDBUS



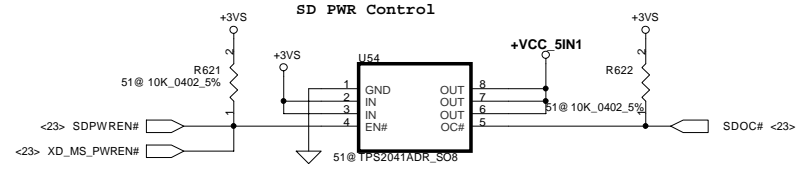
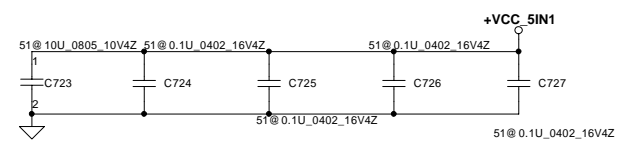
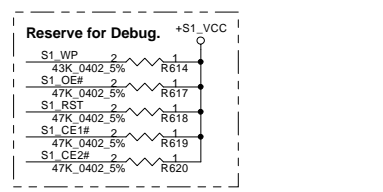
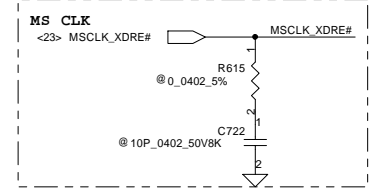
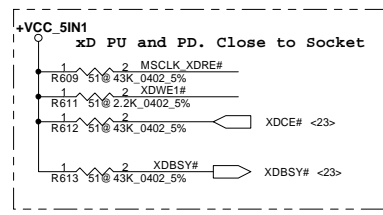
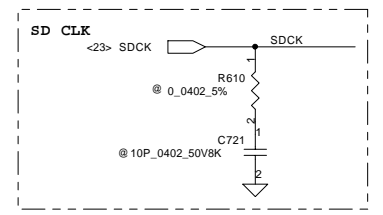
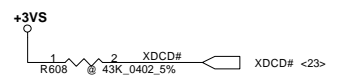
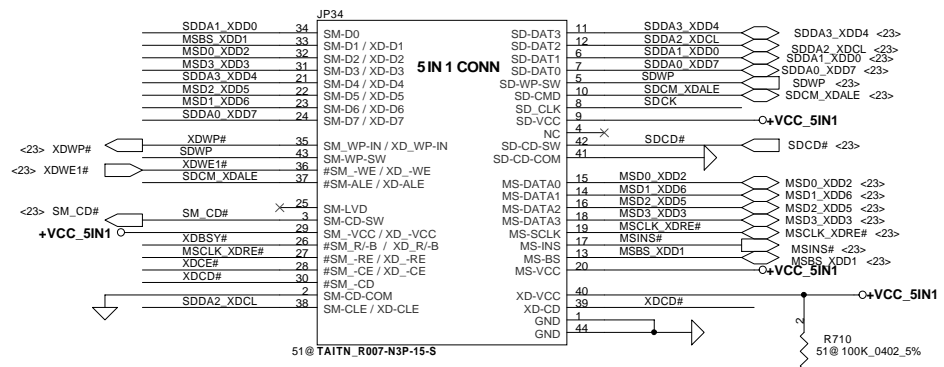
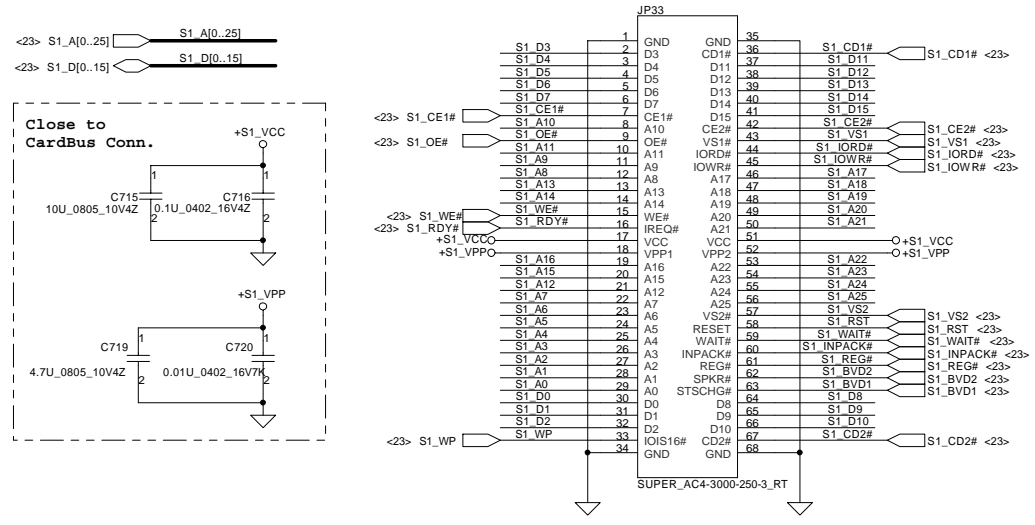
SD/MMC/MS/SM



PCMCIA Power Controller



CardBus Socket



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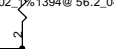
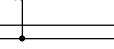
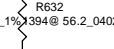
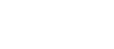
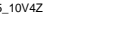
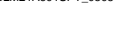
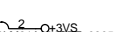
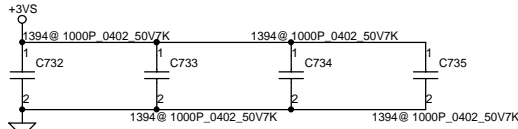
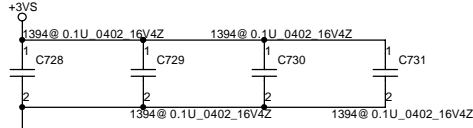
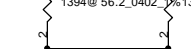
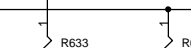
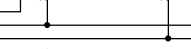
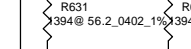
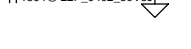
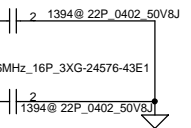
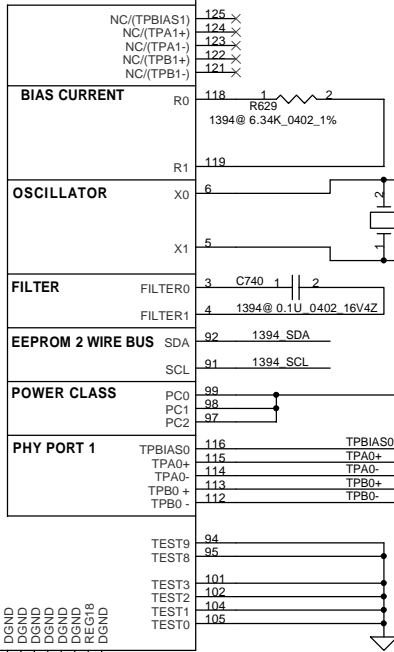
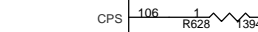
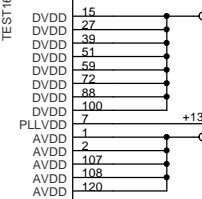
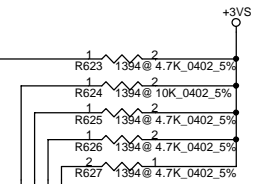
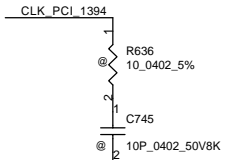
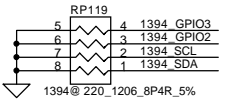
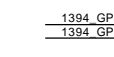
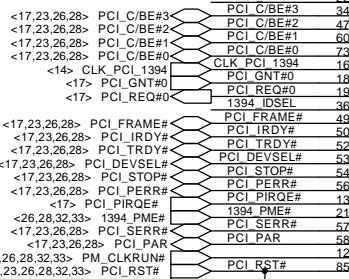
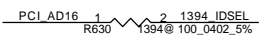


**TSB43AB21  
(TSB43AB22)**

**PCI BUS INTERFACE**

PCI_AD0	84	PCI_AD0	
PCI_AD1	82	PCI_AD1	
PCI_AD2	81	PCI_AD2	
PCI_AD3	80	PCI_AD3	
PCI_AD4	79	PCI_AD4	
PCI_AD5	77	PCI_AD5	
PCI_AD6	76	PCI_AD6	
PCI_AD7	74	PCI_AD7	
PCI_AD8	71	PCI_AD8	
PCI_AD9	70	PCI_AD9	
PCI_AD10	69	PCI_AD10	
PCI_AD11	67	PCI_AD11	
PCI_AD12	66	PCI_AD12	
PCI_AD13	63	PCI_AD13	
PCI_AD14	61	PCI_AD14	
PCI_AD15	61	PCI_AD15	
PCI_AD16	46	PCI_AD16	
PCI_AD17	45	PCI_AD17	
PCI_AD18	43	PCI_AD18	
PCI_AD19	42	PCI_AD19	
PCI_AD20	41	PCI_AD20	
PCI_AD21	40	PCI_AD21	
PCI_AD22	38	PCI_AD22	
PCI_AD23	37	PCI_AD23	
PCI_AD24	32	PCI_AD24	
PCI_AD25	31	PCI_AD25	
PCI_AD26	29	PCI_AD26	
PCI_AD27	28	PCI_AD27	
PCI_AD28	26	PCI_AD28	
PCI_AD29	25	PCI_AD29	
PCI_AD30	24	PCI_AD30	
PCI_AD31	22	PCI_AD31	
PCI_C/BE#3	34	PCI_C/BE#3	
PCI_C/BE#2	47	PCI_C/BE#2	
PCI_C/BE#1	60	PCI_C/BE#1	
PCI_C/BE#0	73	PCI_C/BE#0	
CLK_PCI	1394	16	PCI_CLK
PCI_GNT#0	18	PCI_GNT	
PCI_REQ#0	19	PCI_REQ	
1394 IDSEL	36	PCI_IDSEL	
PCI_FRAME#	49	PCI_FRAME	
PCI_IRDY#	50	PCI_IRDY	
PCI_TRDY#	52	PCI_TRDY	
PCI_DEVSEL#	53	PCI_DEVSEL	
PCI_STOP#	54	PCI_STOP	
PCI_PERR#	56	PCI_PERR	
PCI_PIRQE#	13	PCI_PIRQE	
1394 PME#	21	PCI_INTA/CINT	
PCI_SERR#	57	PCI_PME/CSTSCHG	
PCI_SERR	58	PCI_SERR	
PCI_PAR	58	PCI_PAR	
PM_CLKRUN#	12	PCI_CLKRUN	
PCI_RST#	85	PCI_RST	

**IDSEL:PCI\_AD16**



(CL56)

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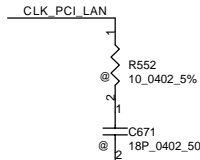
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EN\_WOL# = Low,  
System can wake on LAN  
( keep Low when Power On)

VGS(th) = -0.45V  
IDmax = 2.3A

+3VS for BCM5788  
+3V\_LAN for BCM4401

<17,23,25,28> PCI\_AD[0..31]



Pin	Signal	Pin	Signal
PCI_AD31	B8	AD31	TRD3+/(NC_E13)
PCI_AD30	A8	AD30	TRD3-/(NC_E14)
PCI_AD29	C7	AD29	TRD2+/(NC_D13)
PCI_AD28	C6	AD28	TRD2-/(NC_D14)
PCI_AD27	B6	AD27	TRD1+(RDP)
PCI_AD26	B5	AD26	TRD1-(RDN)
PCI_AD25	A5	AD25	TRD0+(TDP)
PCI_AD24	B4	AD24	TRD0-(TDN)
PCI_AD23	B4	AD23	
PCI_AD22	B1	AD22	
PCI_AD21	C1	AD21	
PCI_AD20	D3	AD20	
PCI_AD19	D2	AD19	
PCI_AD18	D1	AD18	
PCI_AD17	E3	AD17	
PCI_AD16	E2	AD16	
PCI_AD15	L2	AD15	
PCI_AD14	L1	AD14	
PCI_AD13	M3	AD13	
PCI_AD12	M2	AD12	
PCI_AD11	M1	AD11	
PCI_AD10	N2	AD10	
PCI_AD9	N3	AD9	
PCI_AD8	P3	AD8	
PCI_AD7	N4	AD7	
PCI_AD6	P4	AD6	
PCI_AD5	M5	AD5	
PCI_AD4	N5	AD4	
PCI_AD3	P5	AD3	
PCI_AD2	P6	AD2	
PCI_AD1	M7	AD1	
PCI_AD0	N7	AD0	

BCM5788M  
/(BCM4401)

unpop R554 when use BCM4401

unpop R554 when use BCM4401

1.24K for BCM5788  
1.27K for BCM4401

AT93C46 for BCM4401

24C256 for BCM5788  
Unpop when use BCM4401

	5788	4401
L33		Pop
L34	Pop	
Q61	Pop	
Q60	Pop	
R560	1.24K	1.27K
U50		Pop
C678		Pop
U51	Pop	
R561	Pop	
C677	Pop	
R562	Pop	

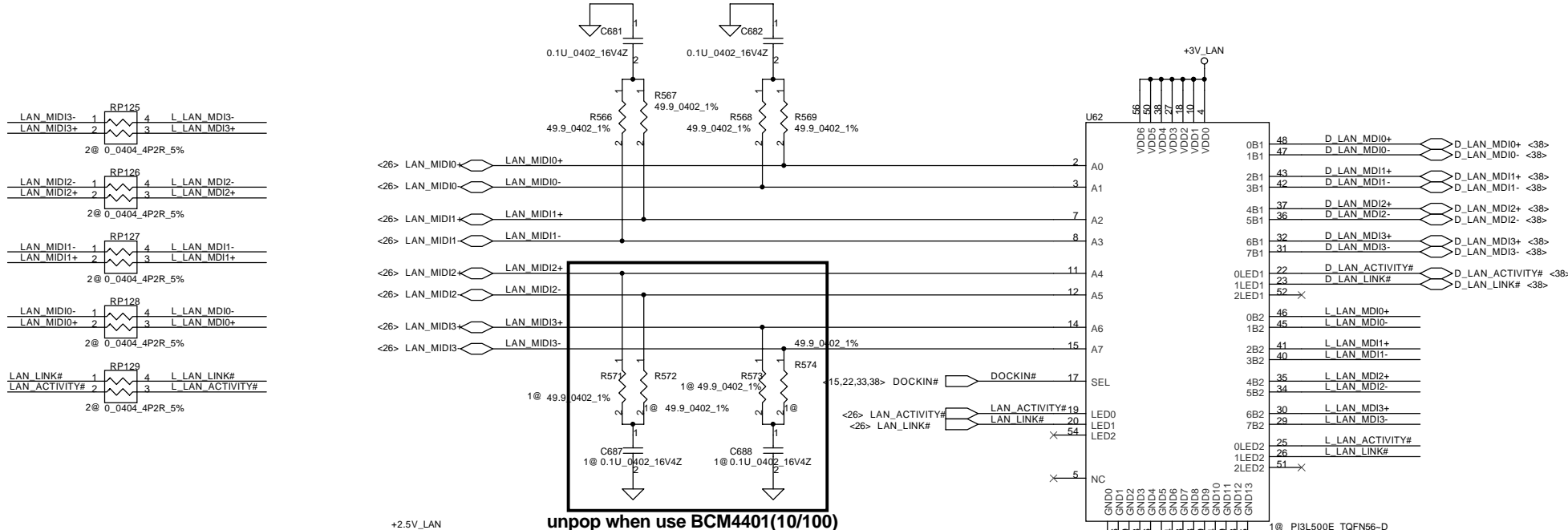
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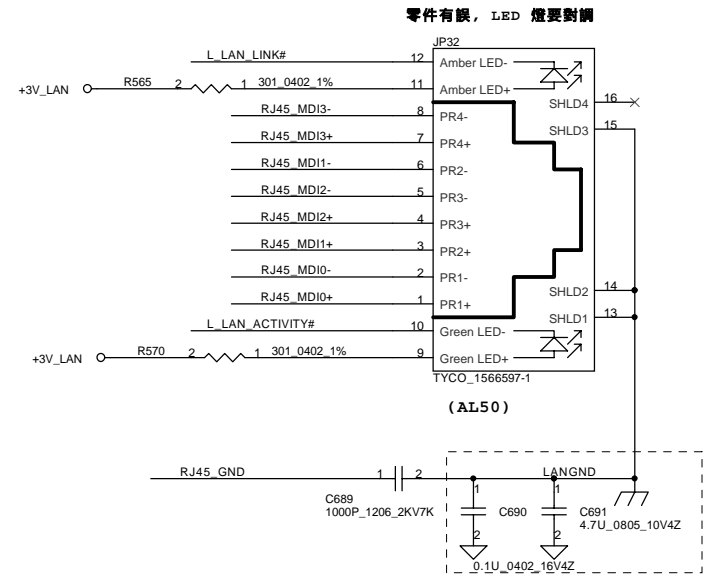
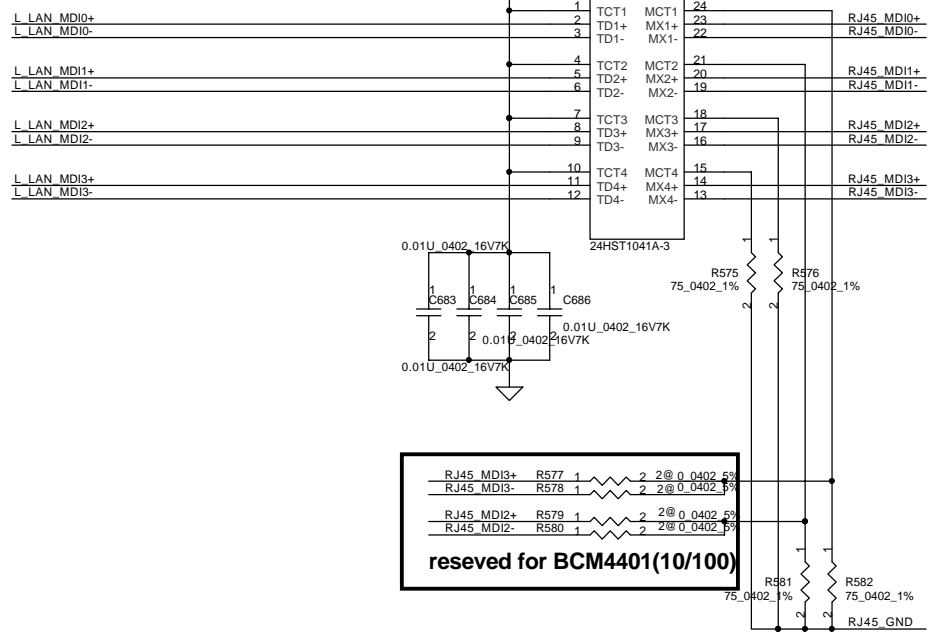
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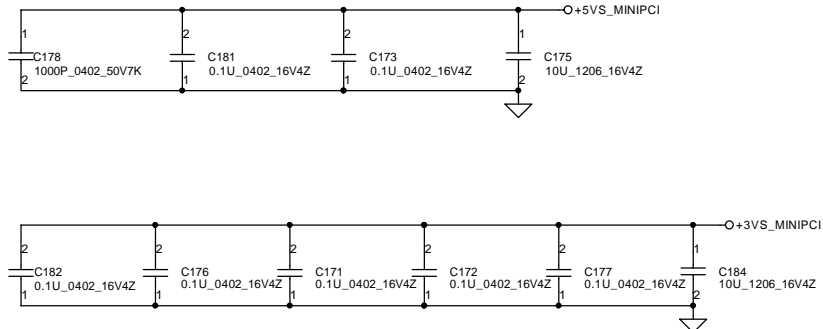
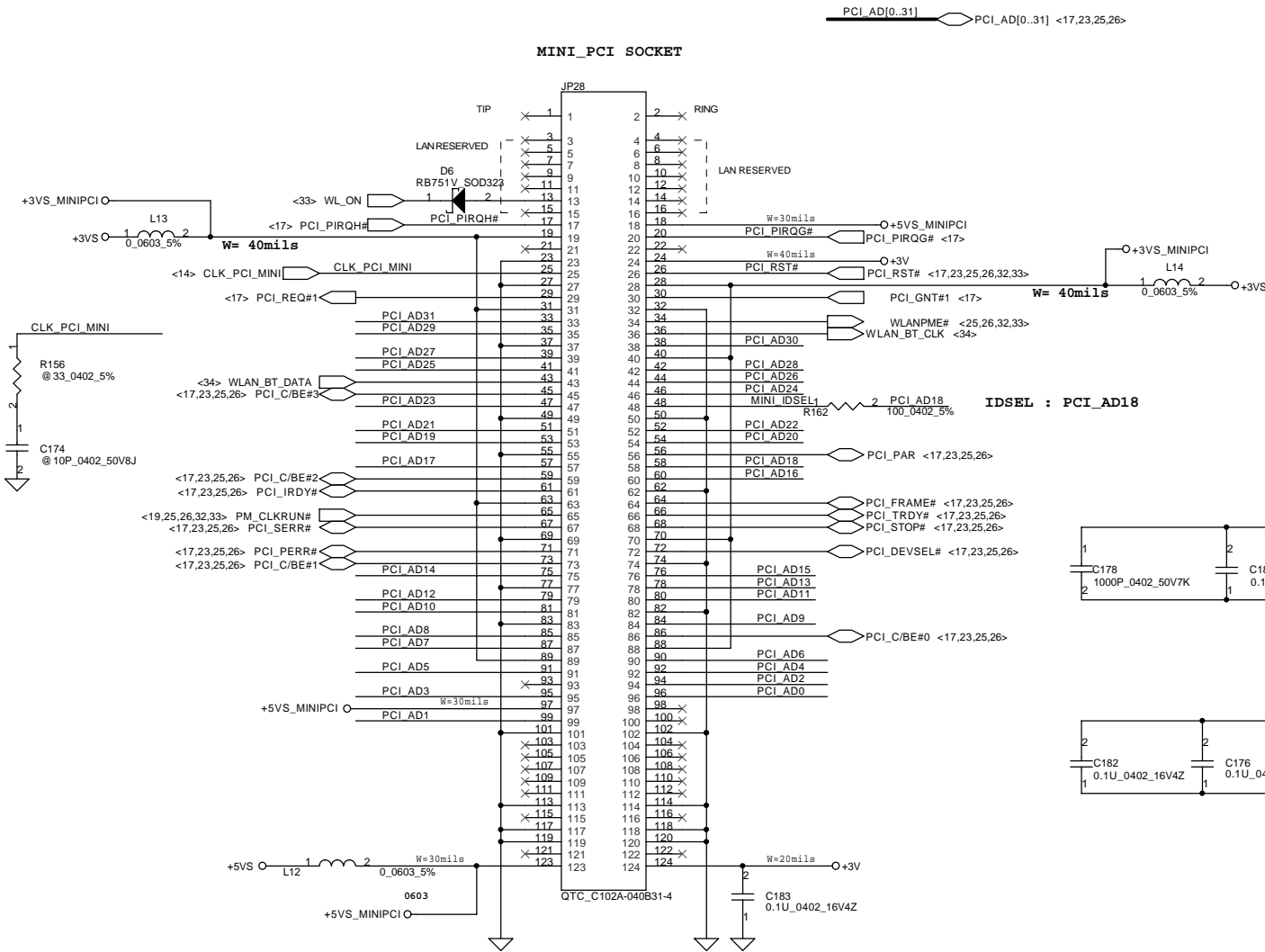
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 24HST1041A-3(SP050002110) for BCM5788M(GbE)



**LAN BCM5788M/BCM4401KFB**

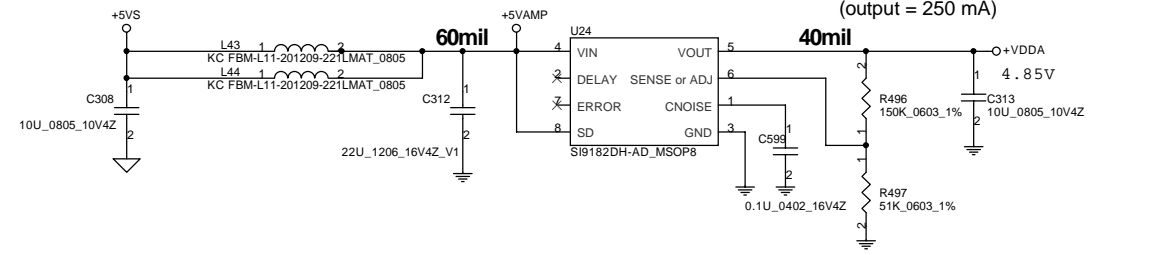
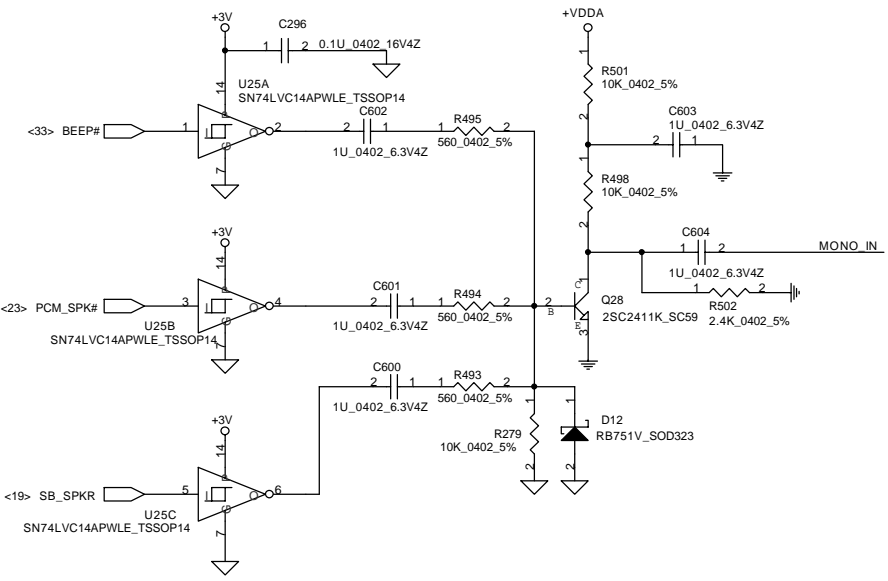
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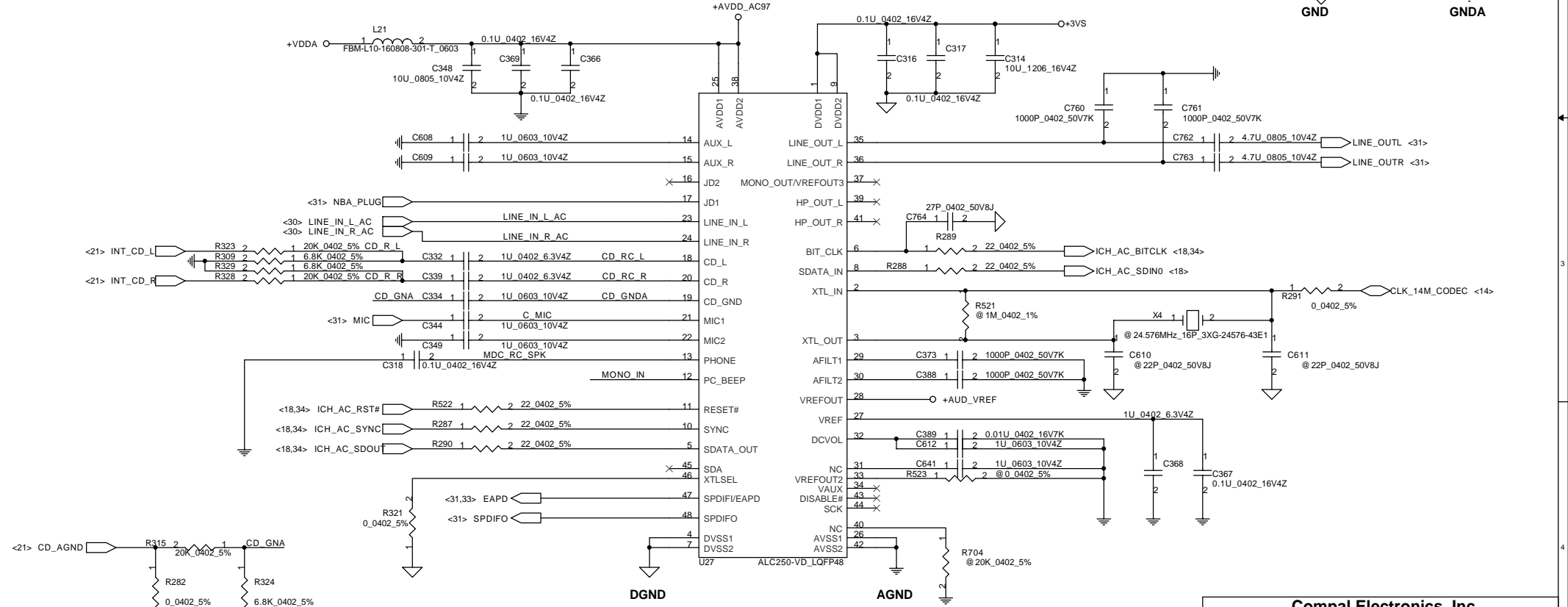
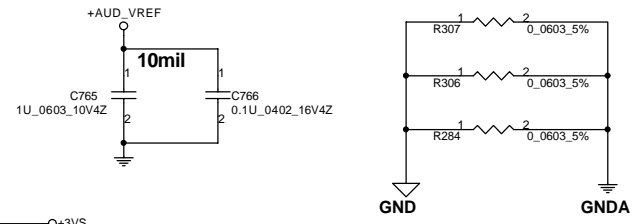
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28.7K for Module Design (VDDA = 4.702)  
(output = 250 mA)

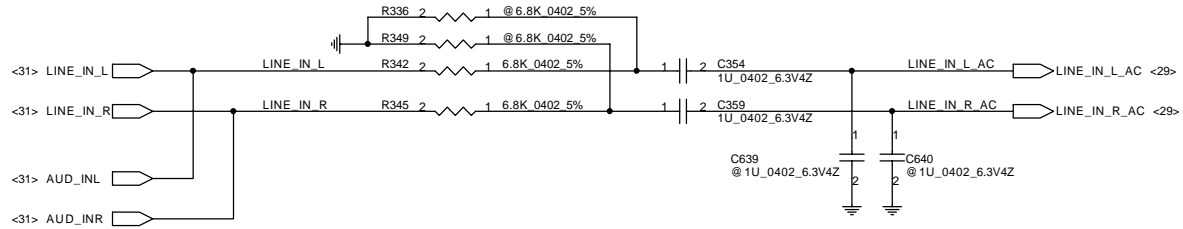
### AC97 Codec



With 14.318Mhz : R321 POP  
With 24.576Mhz : R321 DEPOP

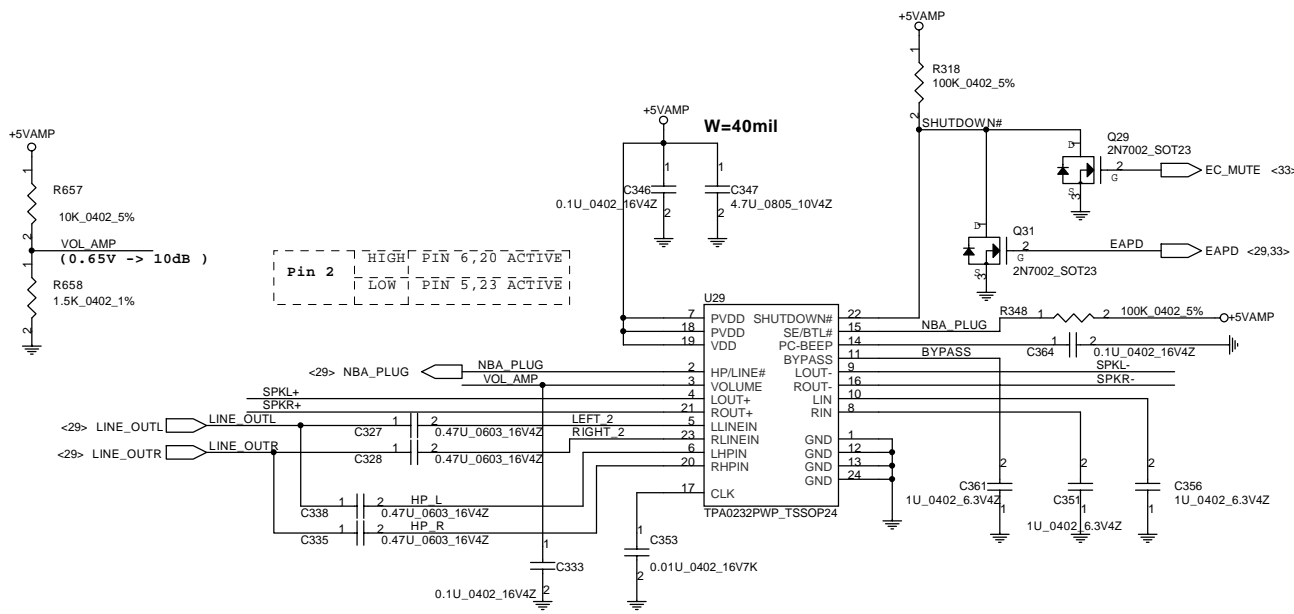
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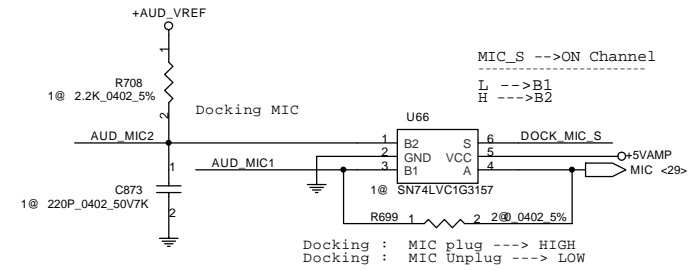
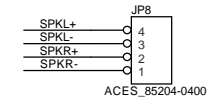


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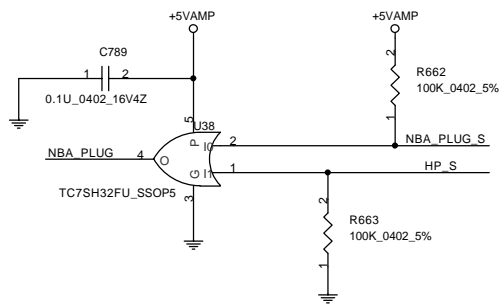
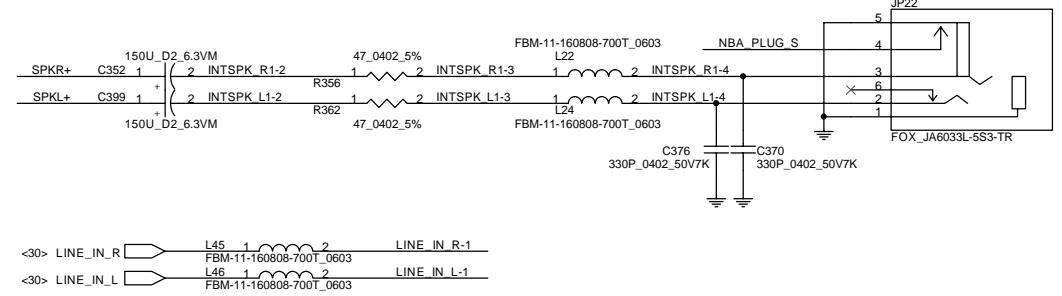
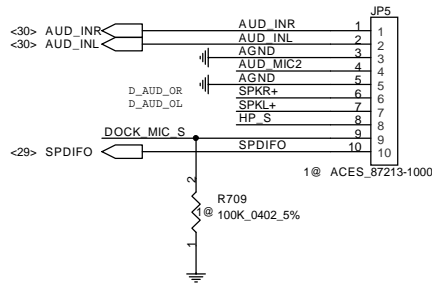
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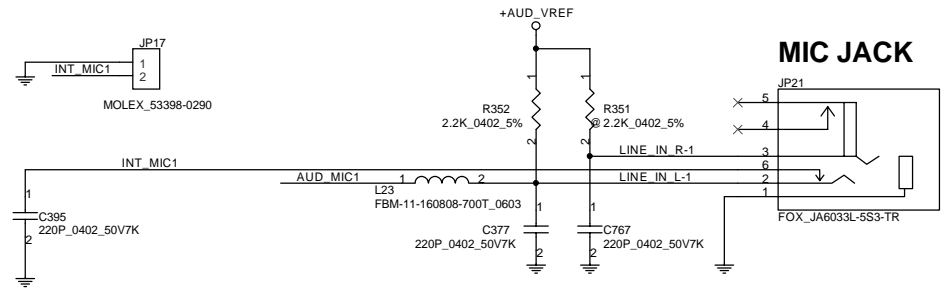
### Speaker Conn.



### HeadPhone JACK



### MIC JACK

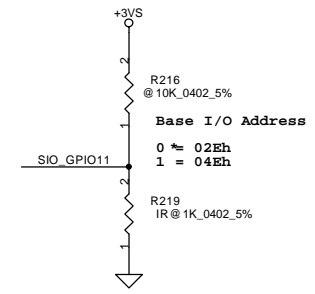
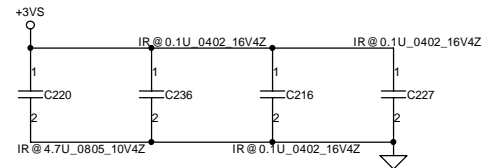
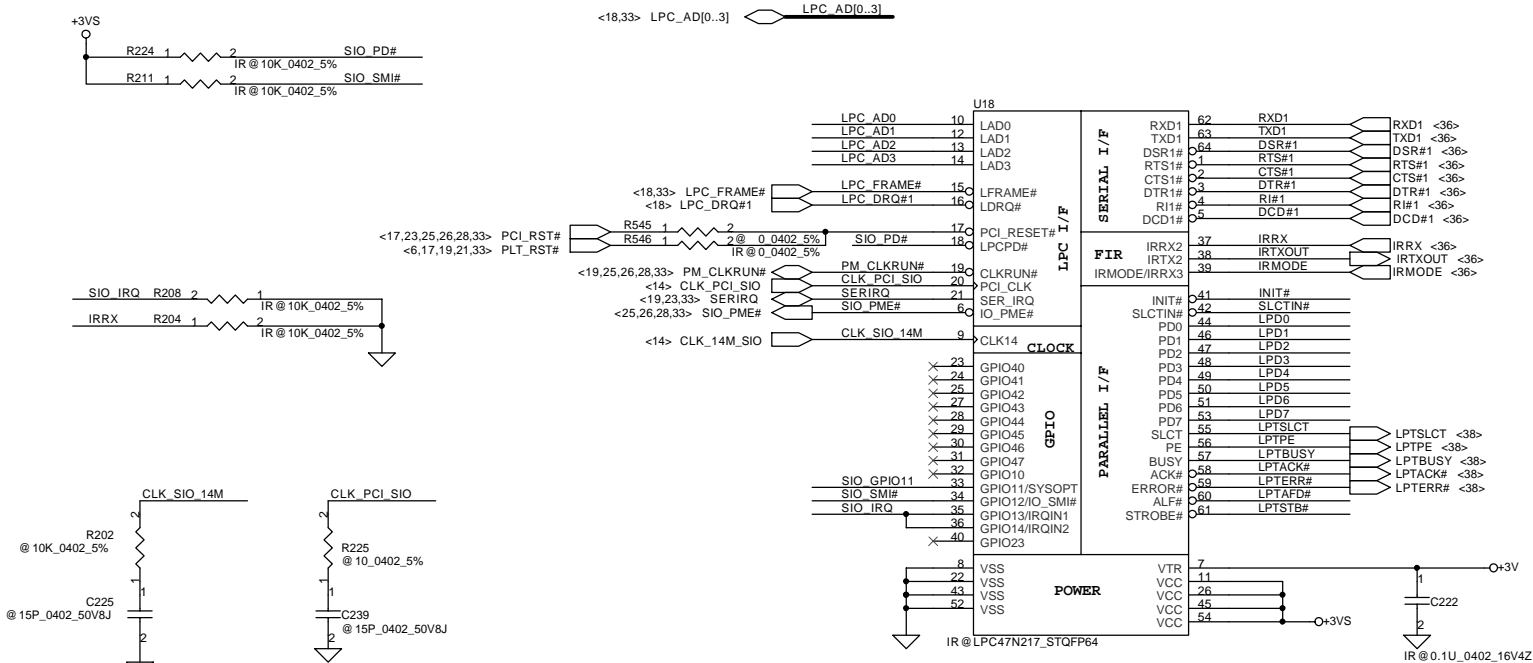


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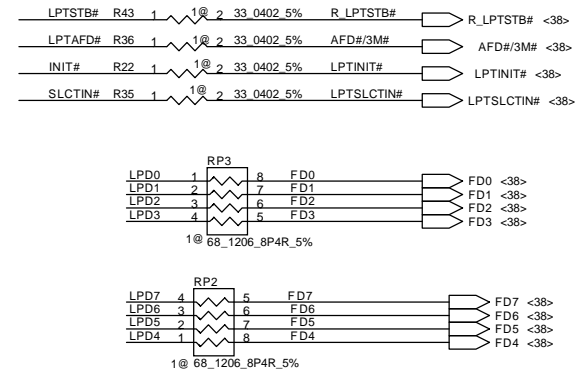
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# SUPER I/O SMsC LPC47N217



## Close to Docking



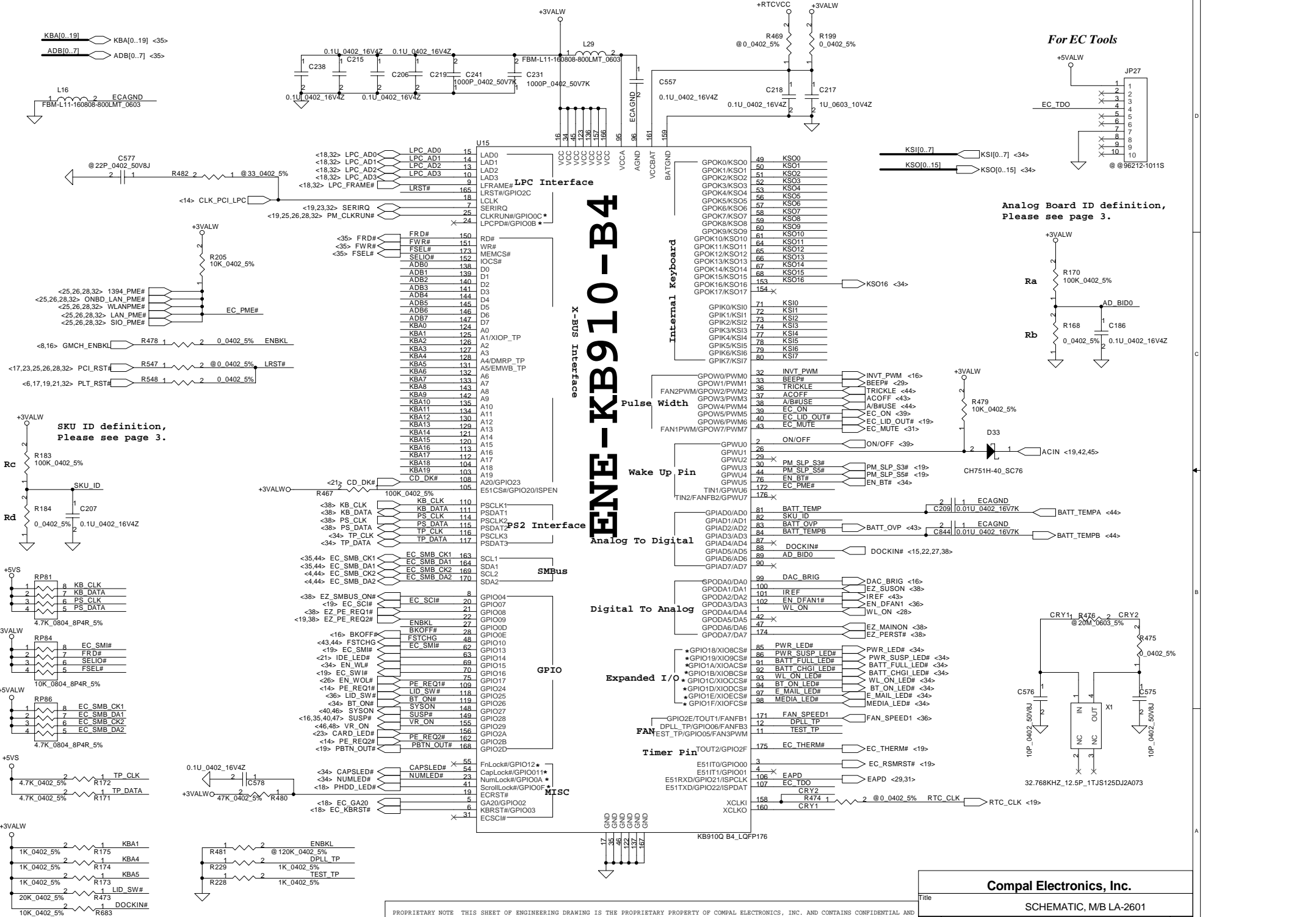
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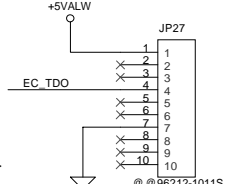


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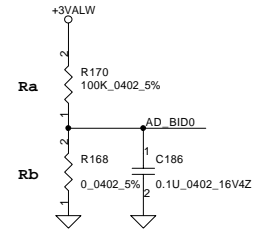
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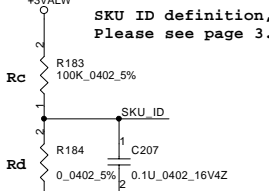
For EC Tools



Analog Board ID definition, please see page 3.



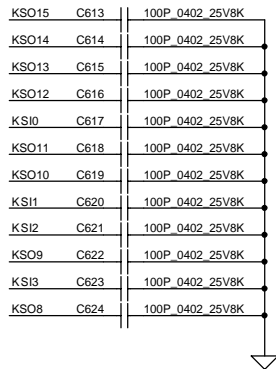
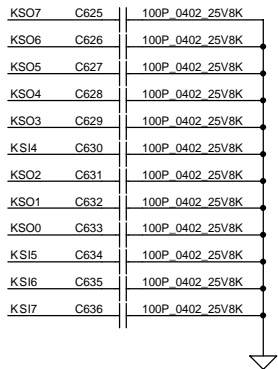
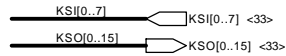
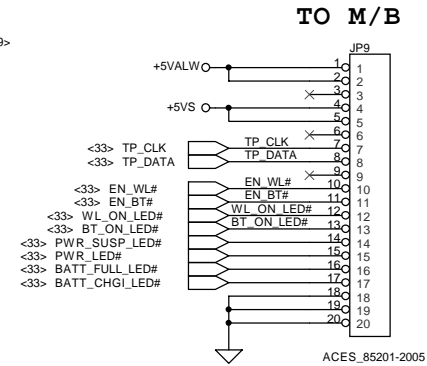
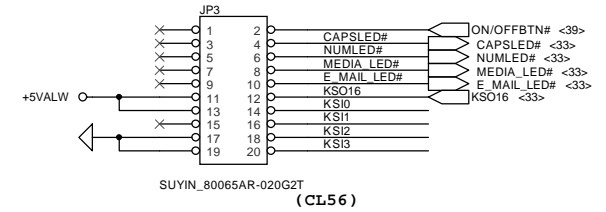
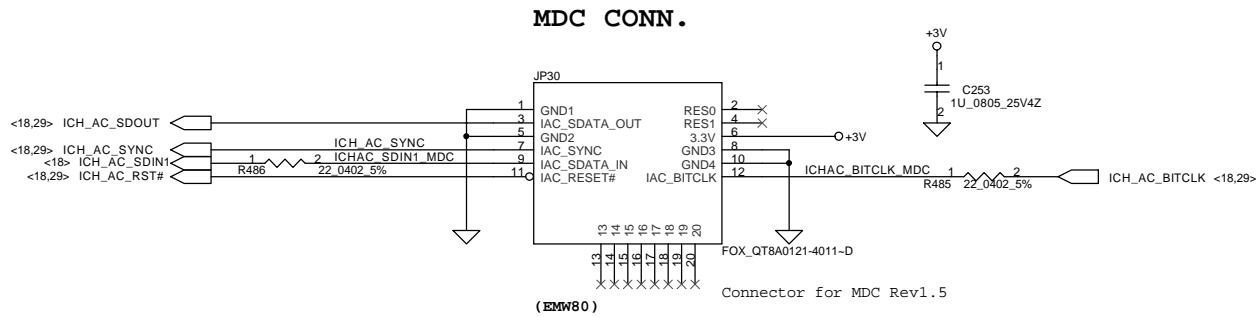
SKU ID definition, please see page 3.



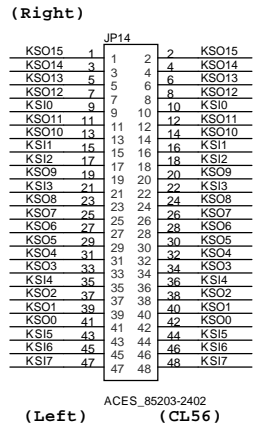
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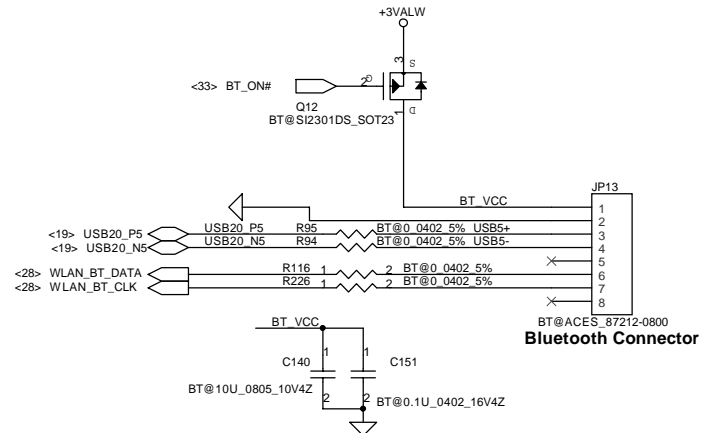
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### INT\_KBD CONN.



### BlueTooth Interface

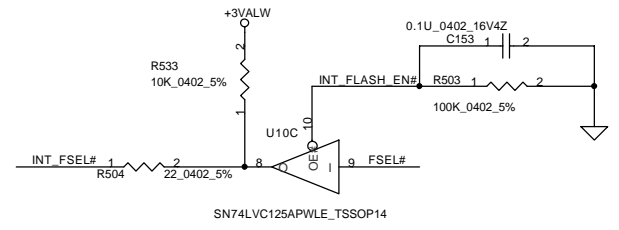
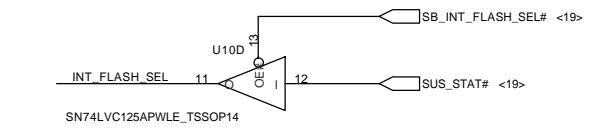
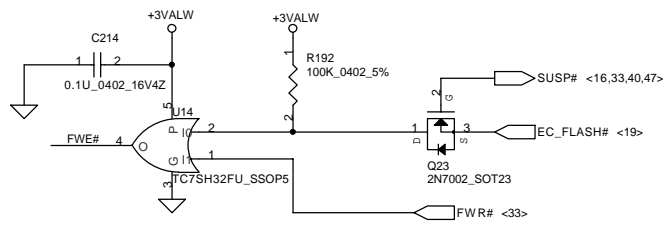
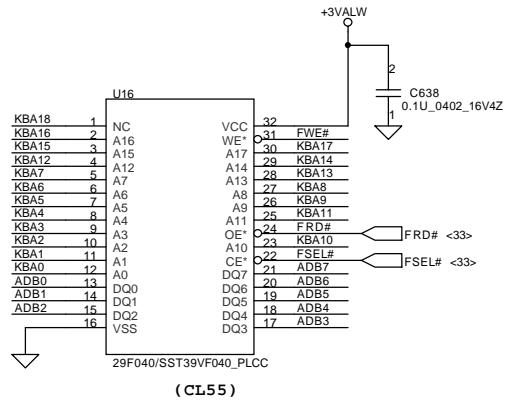


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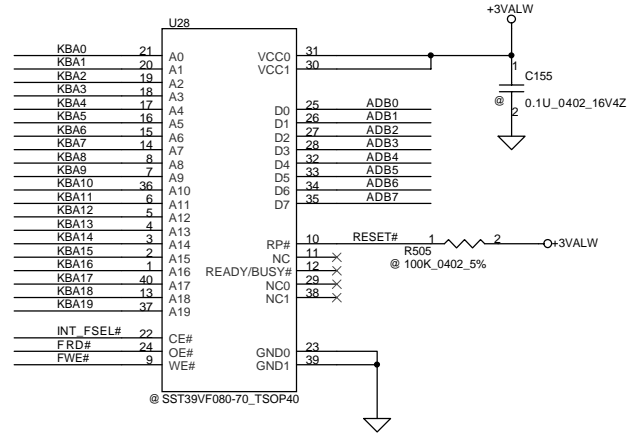
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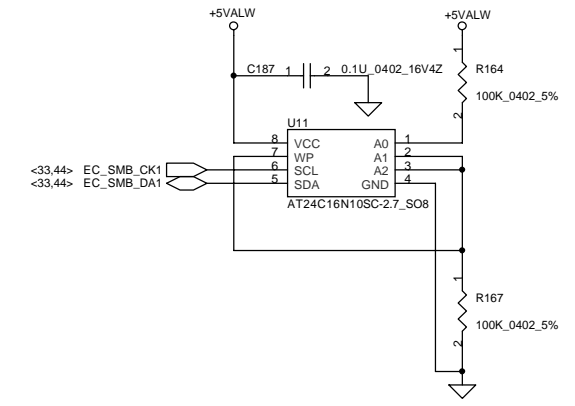
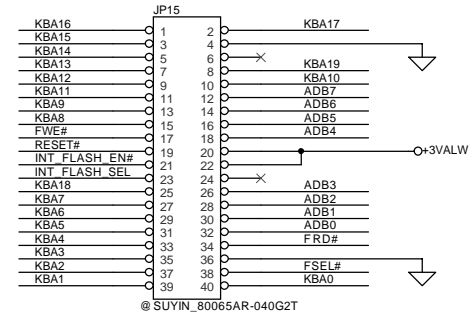
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 <33> ADB[0..7] ← ADB[0..7]



### 1MB Flash ROM



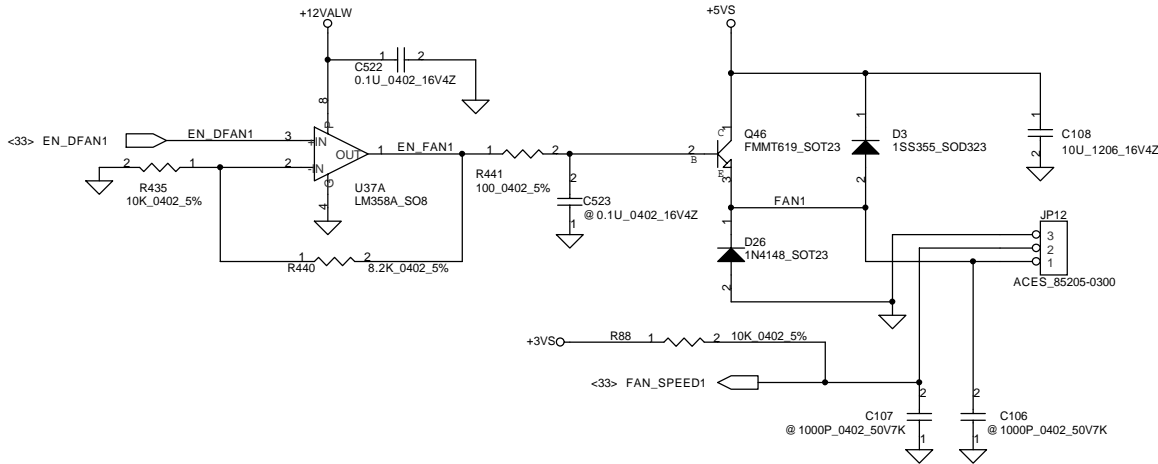
### 1MB ROM Socket



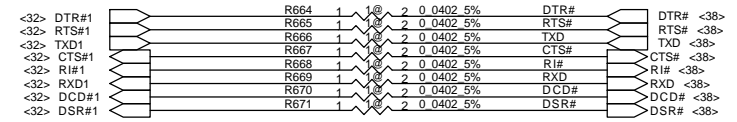
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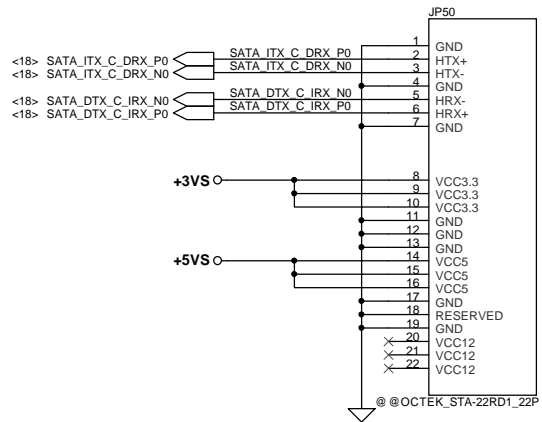
# FAN Conn



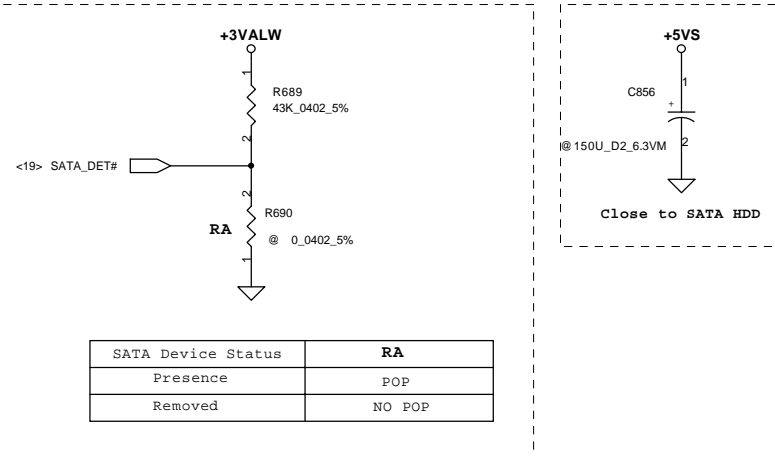
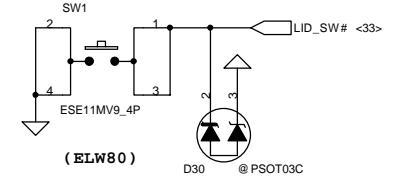
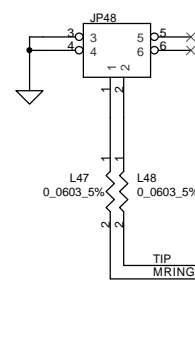
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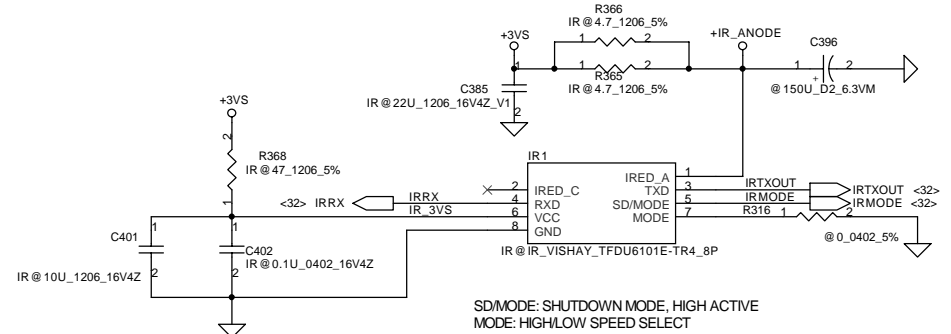
# SATA HDD CONN



# FOXCONN\_JM34613-L002-TR



# FIR Module

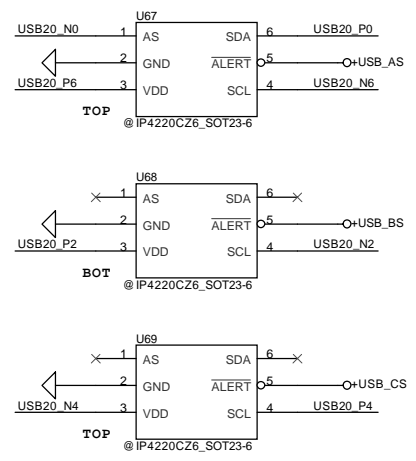
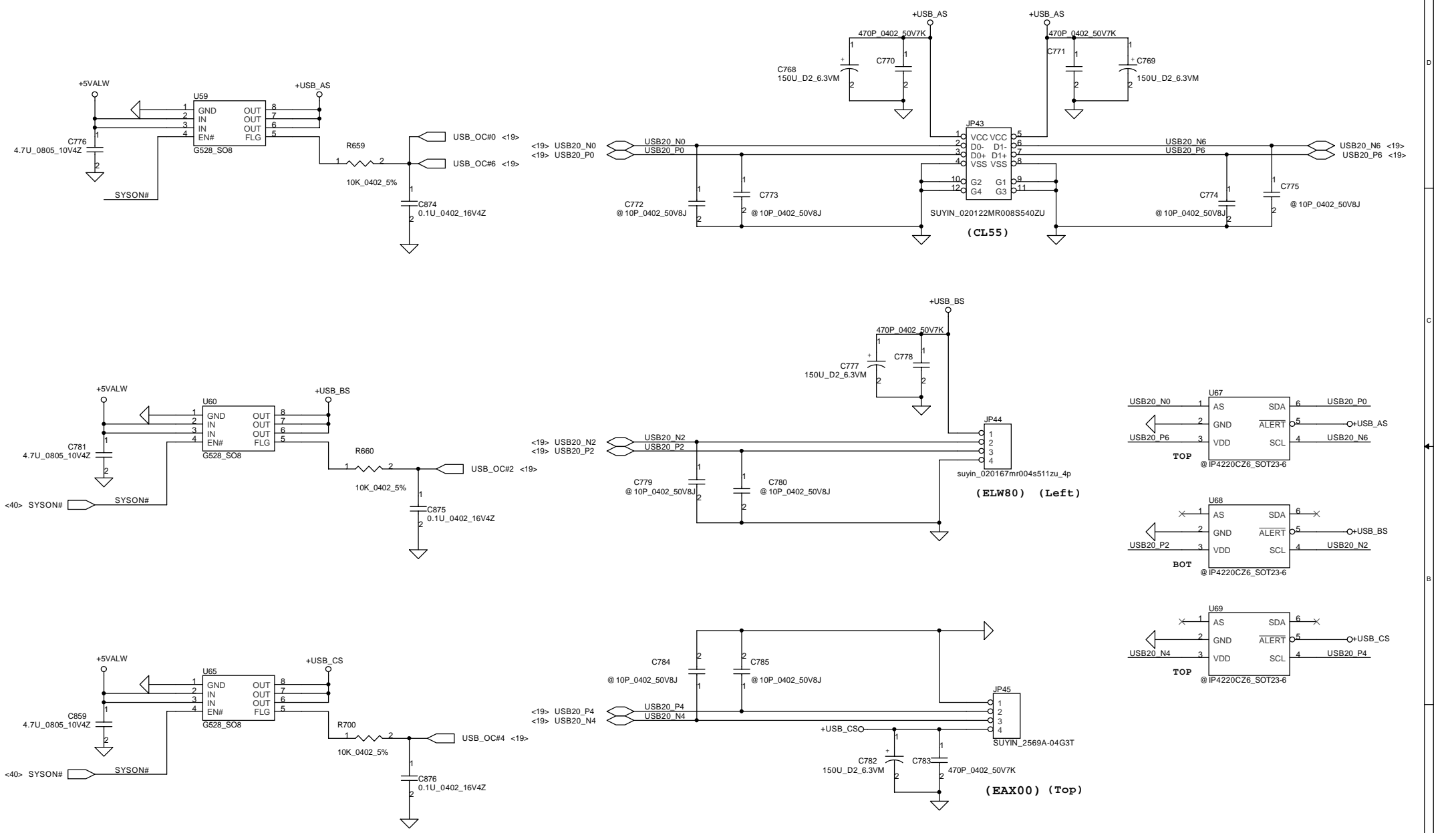


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SCHEMATIC, M/B LA-2601

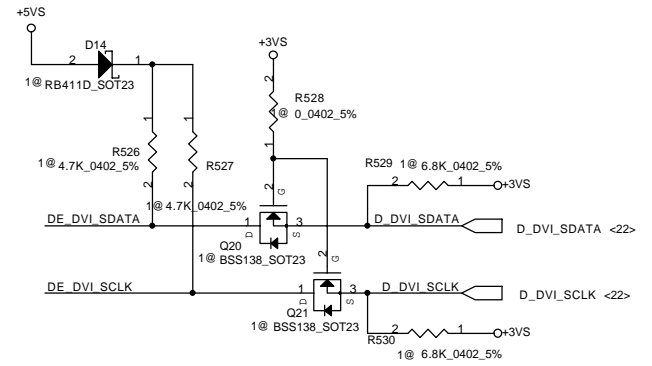
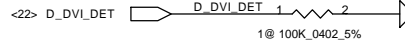
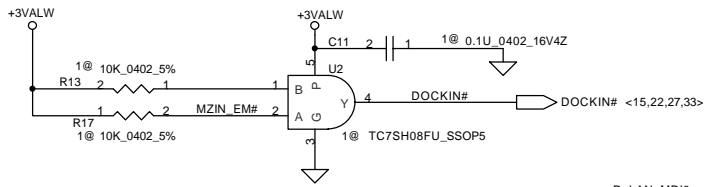
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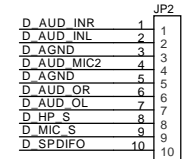
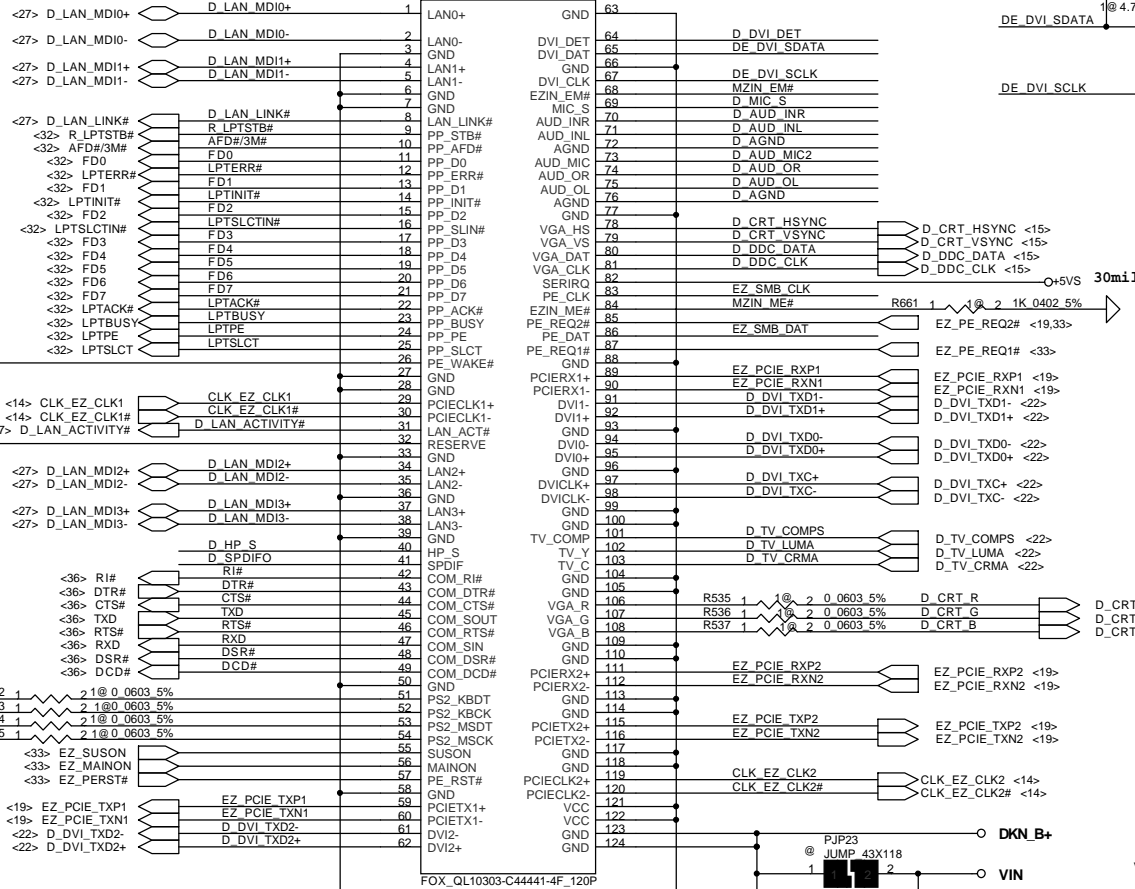


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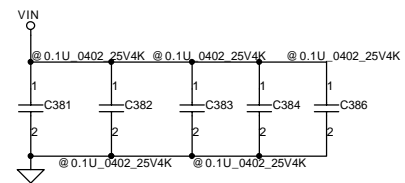
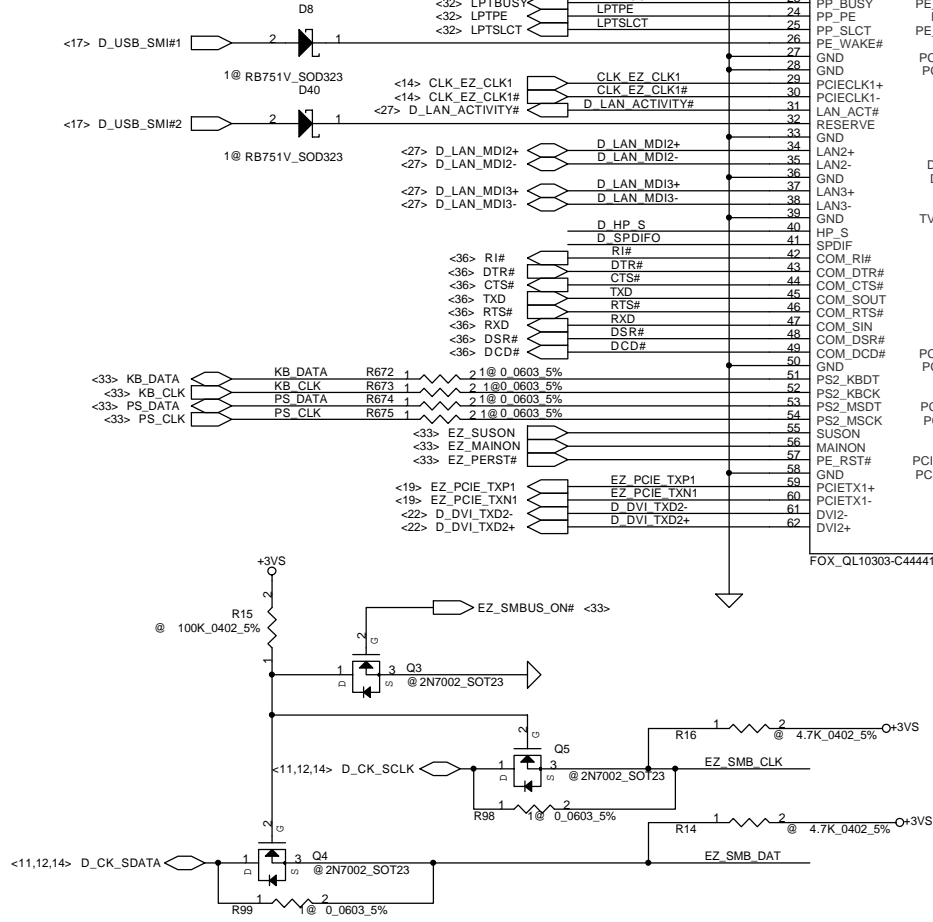
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### Docking Conn.

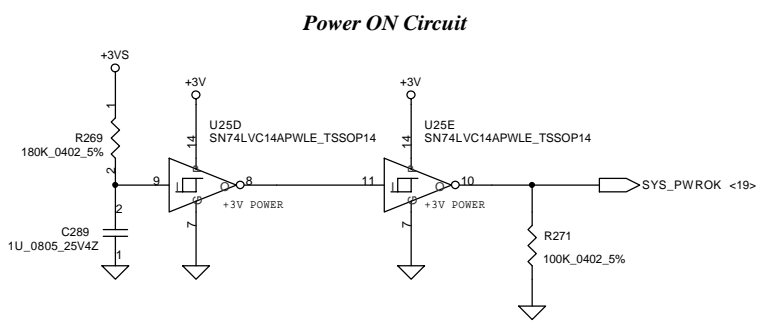
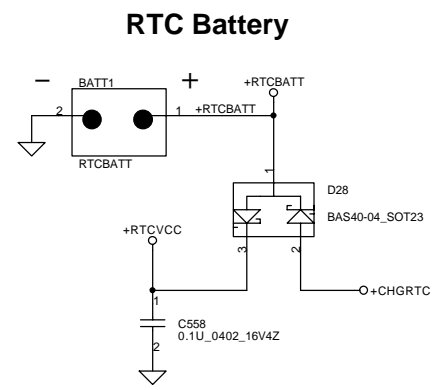
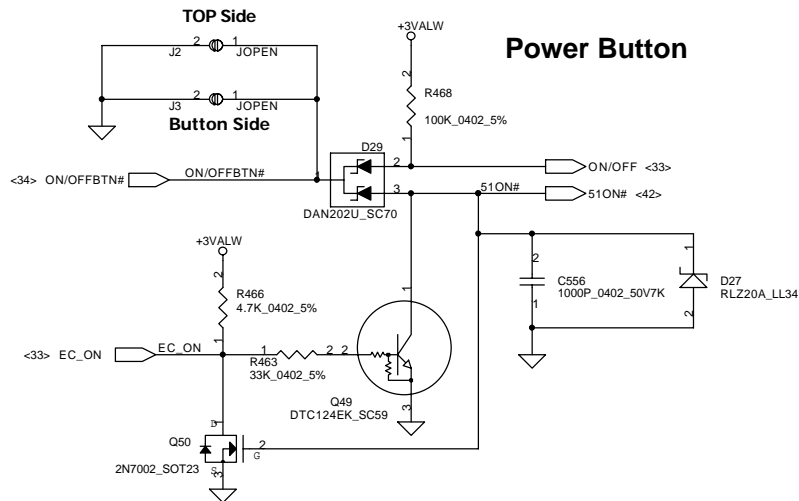


1 @ ACES\_87213-1000



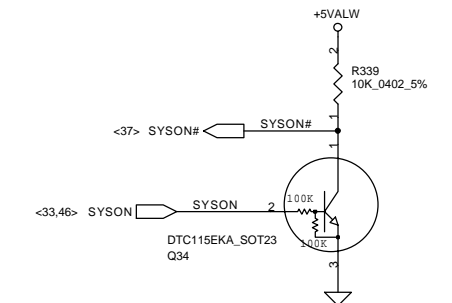
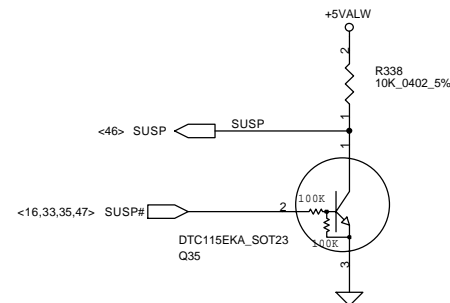
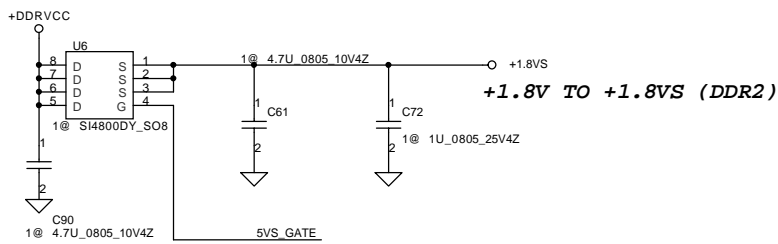
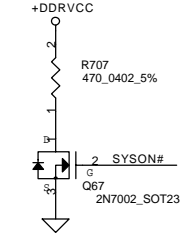
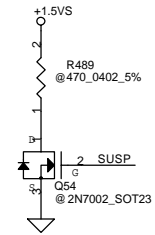
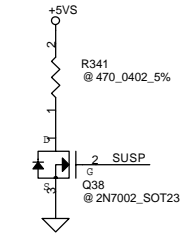
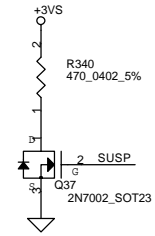
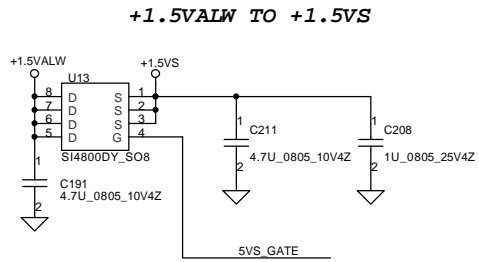
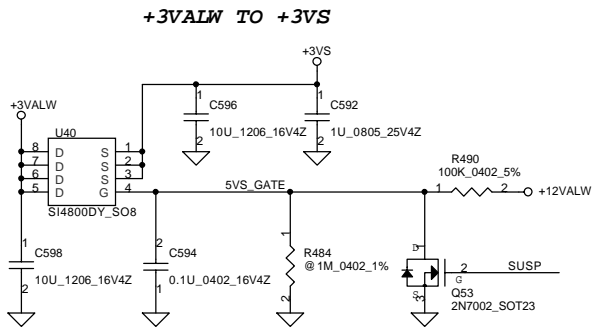
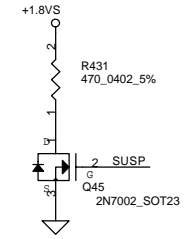
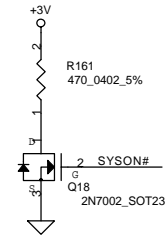
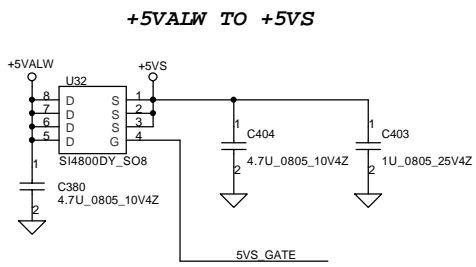
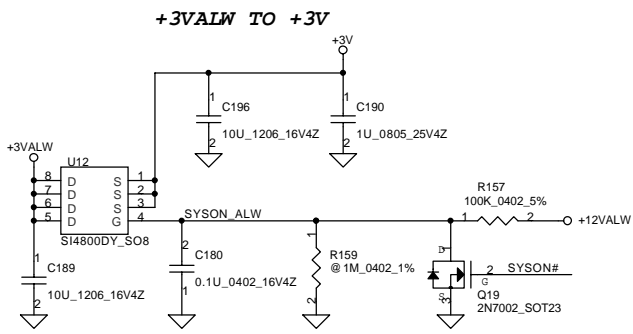
<b>Compal Electronics, Inc.</b>		
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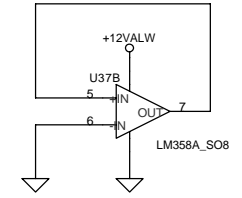
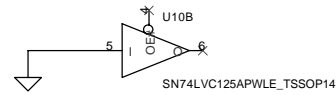
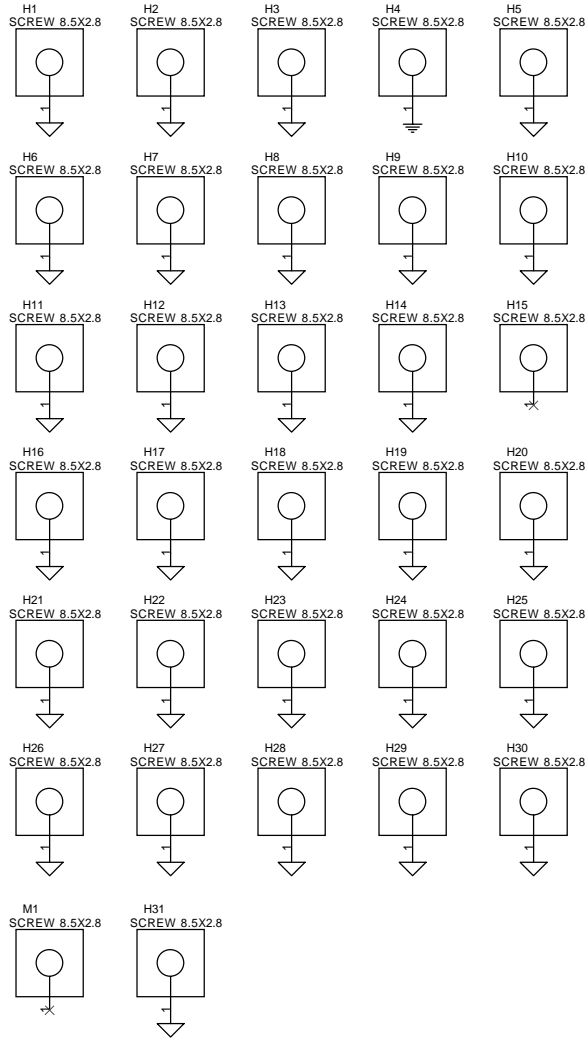
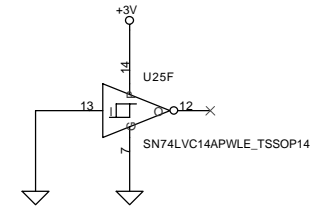
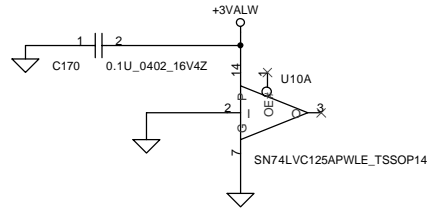
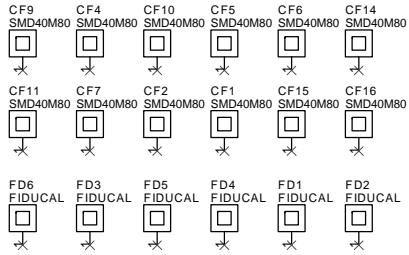
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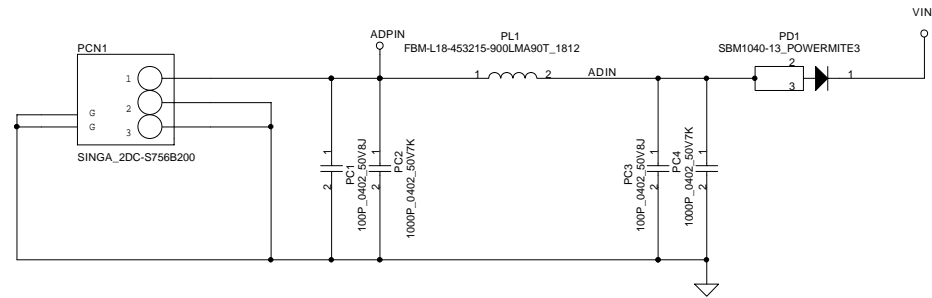
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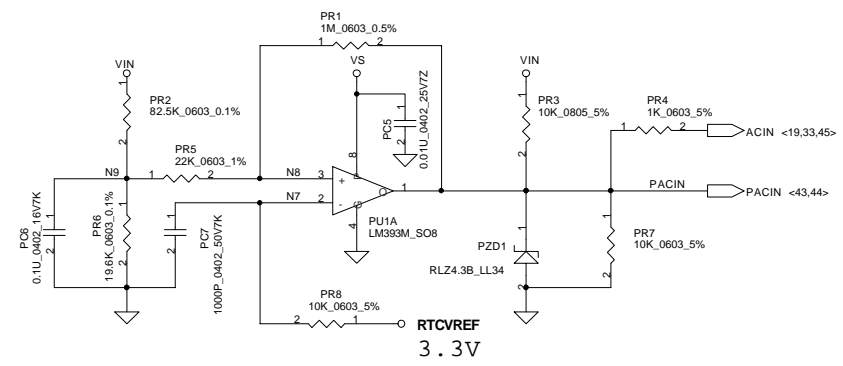


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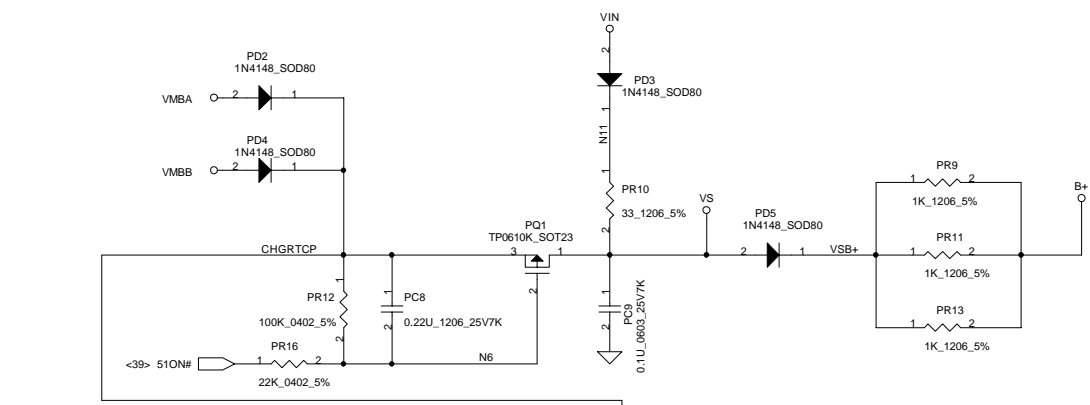
<b>Compal Electronics, Inc.</b>		
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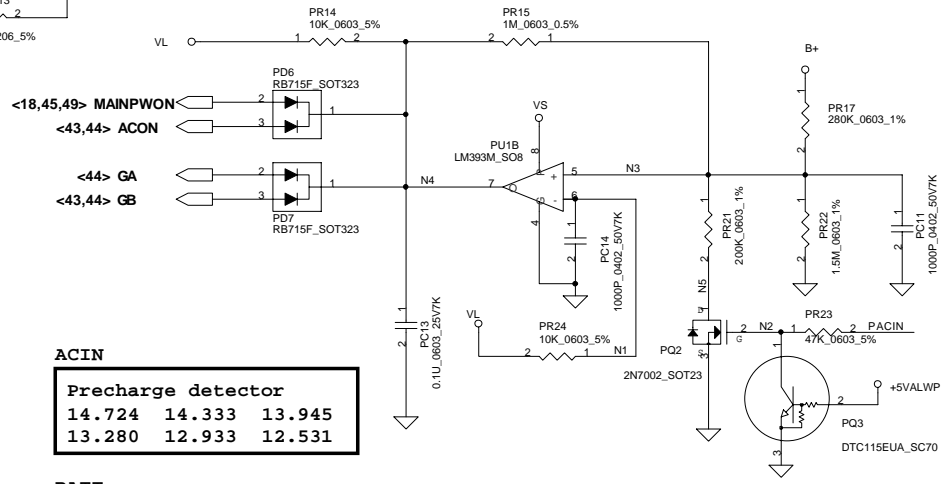
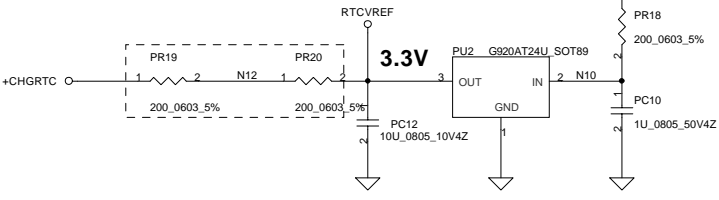
Vin Detector		
18.234	17.841	17.449
17.597	17.210	16.813



RTCVREF  
3.3V

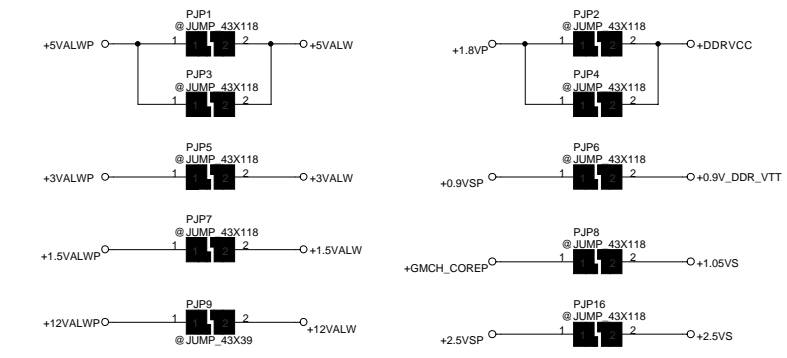


3.3V



ACIN		
14.724	14.333	13.945
13.280	12.933	12.531

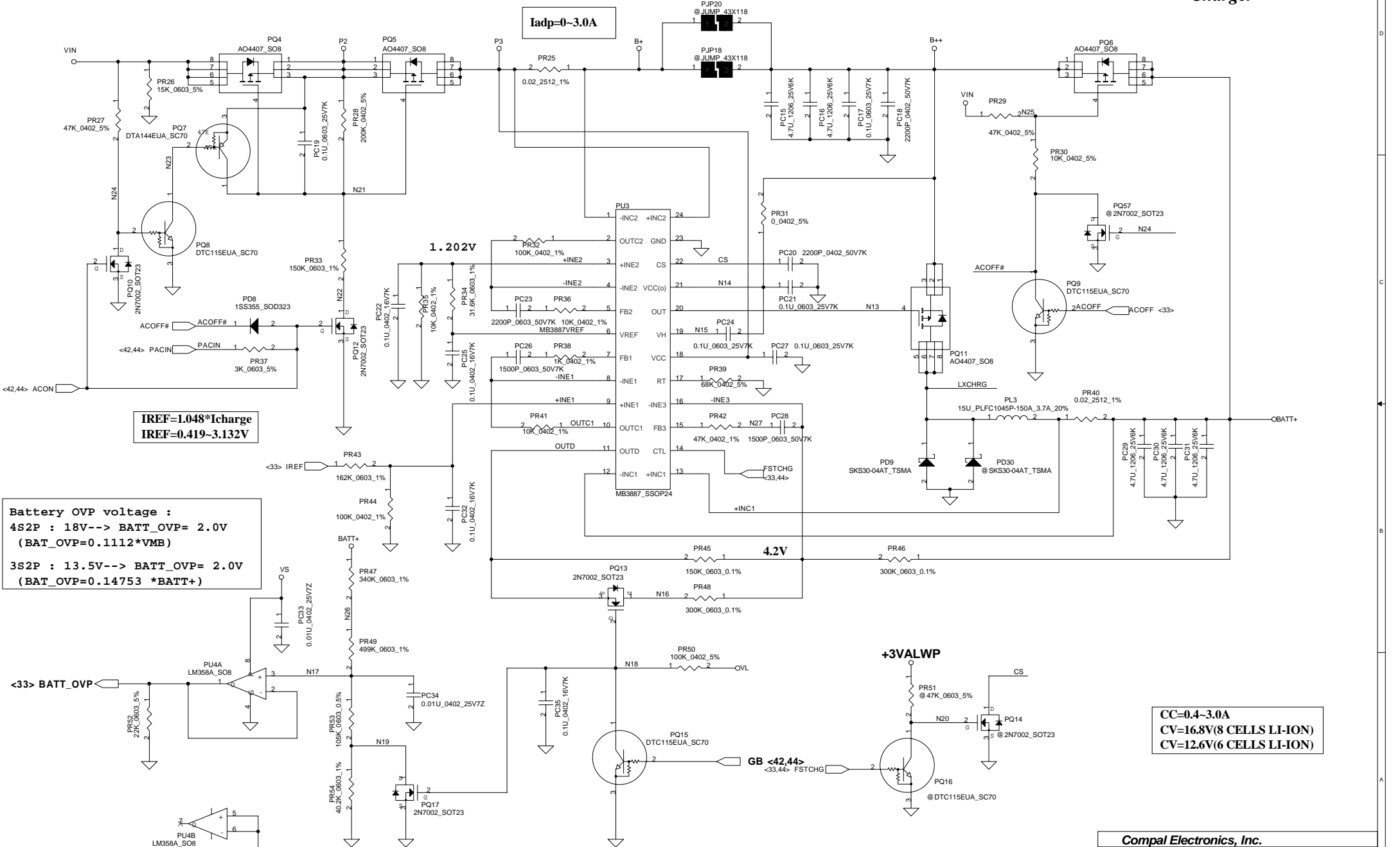
BATT		
7.558	7.333	7.112
6.108	5.933	5.704



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# Charger



I<sub>adp</sub>=0~3.0A

IREF=1.048\*I<sub>charge</sub>  
IREF=0.419~3.132V

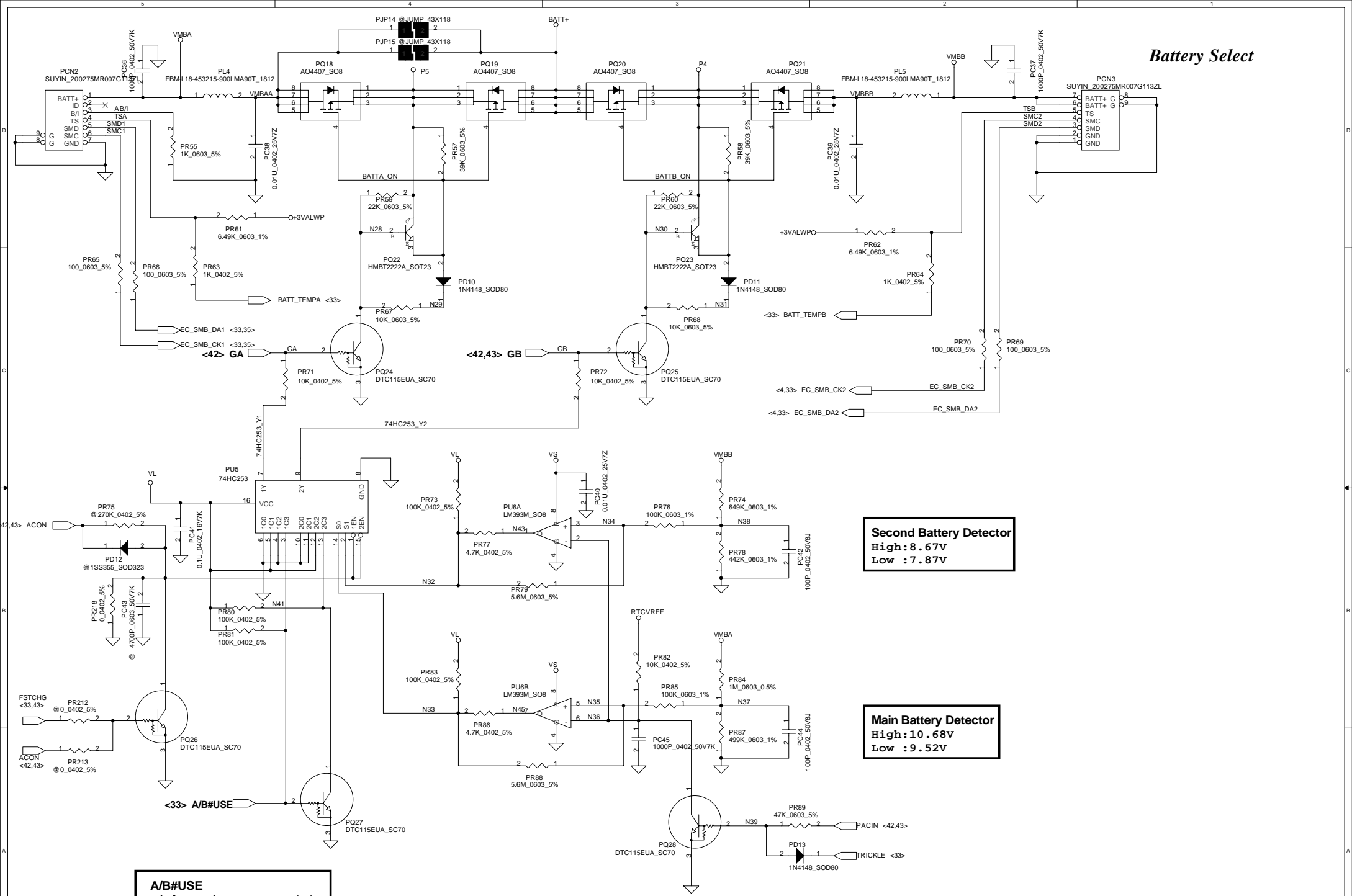
Battery OVP voltage :  
4S2P : 18V--> BATT\_OVP= 2.0V  
(BATT\_OVP=0.1112\*V<sub>MB</sub>)  
3S2P : 13.5V--> BATT\_OVP= 2.0V  
(BATT\_OVP=0.14753 \*BATT+)

CC=0.4~3.0A  
CV=16.8V(8 CELLS LI-ION)  
CV=12.6V(6 CELLS LI-ION)

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# Battery Select



**A/B#USE**  
 High: Main Battery (A)  
 Low : Second Battery (B)

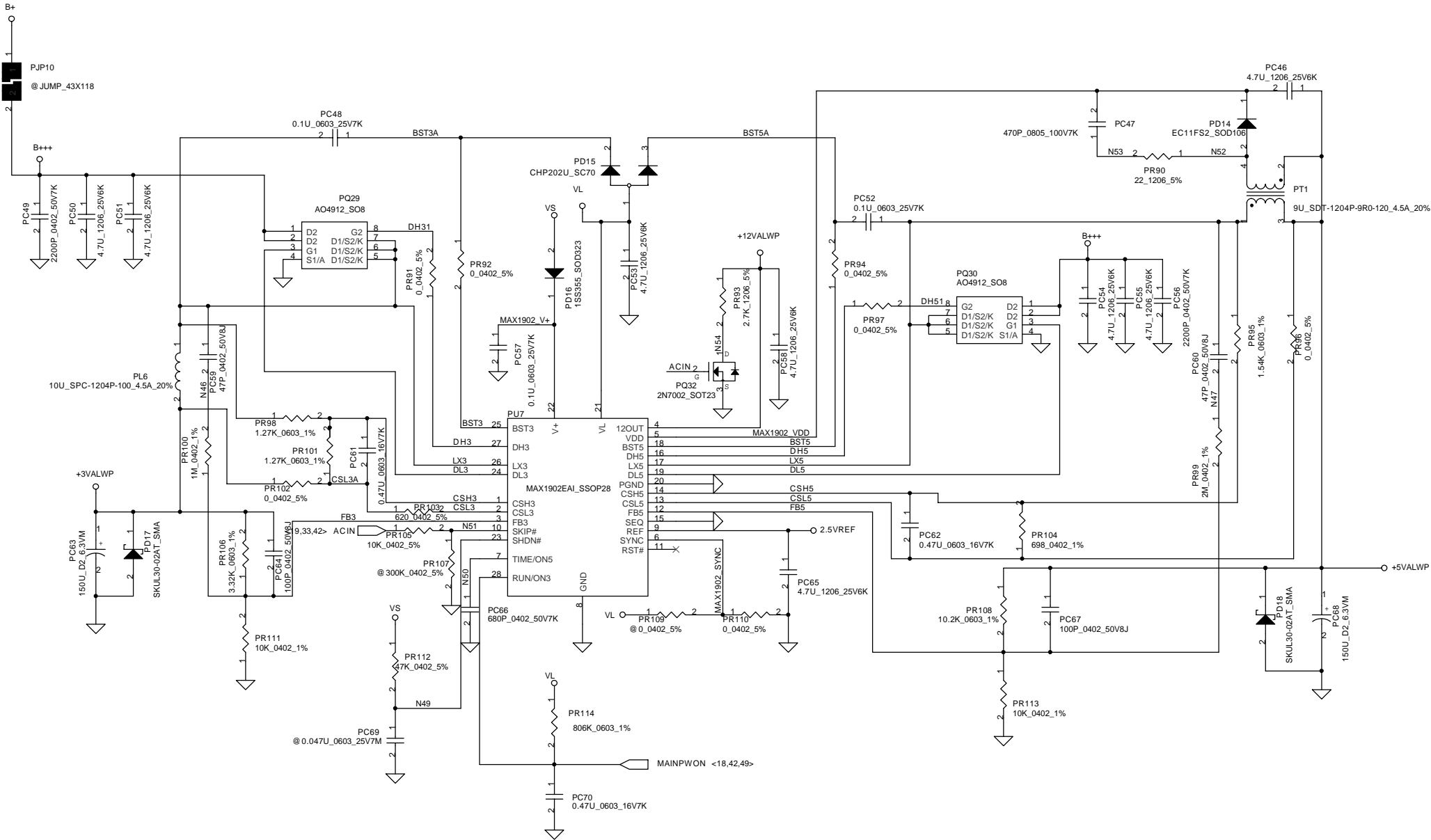
**Second Battery Detector**  
 High: 8.67V  
 Low : 7.87V

**Main Battery Detector**  
 High: 10.68V  
 Low : 9.52V

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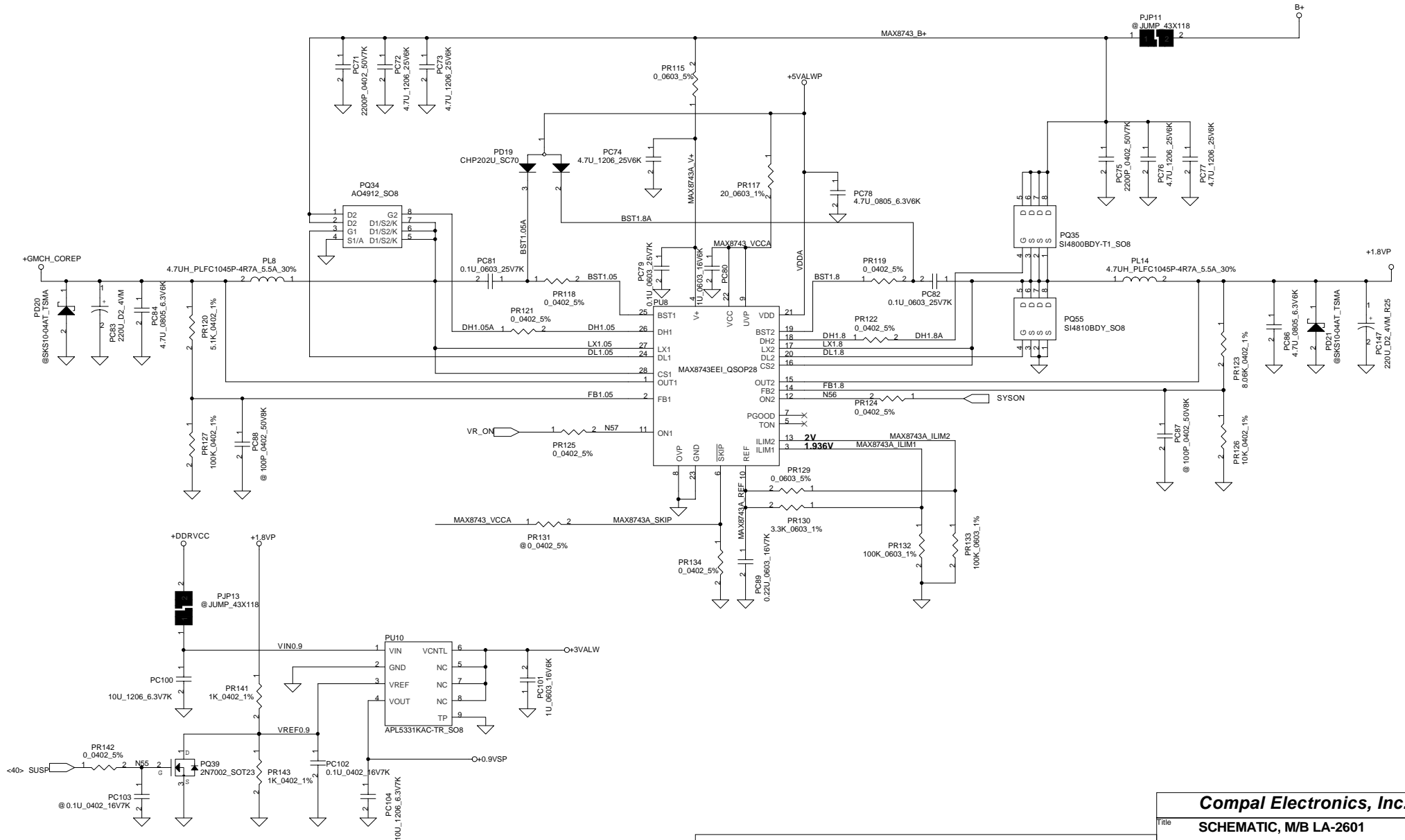
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**+3VALWP/+5VALWP/+12VALWP**



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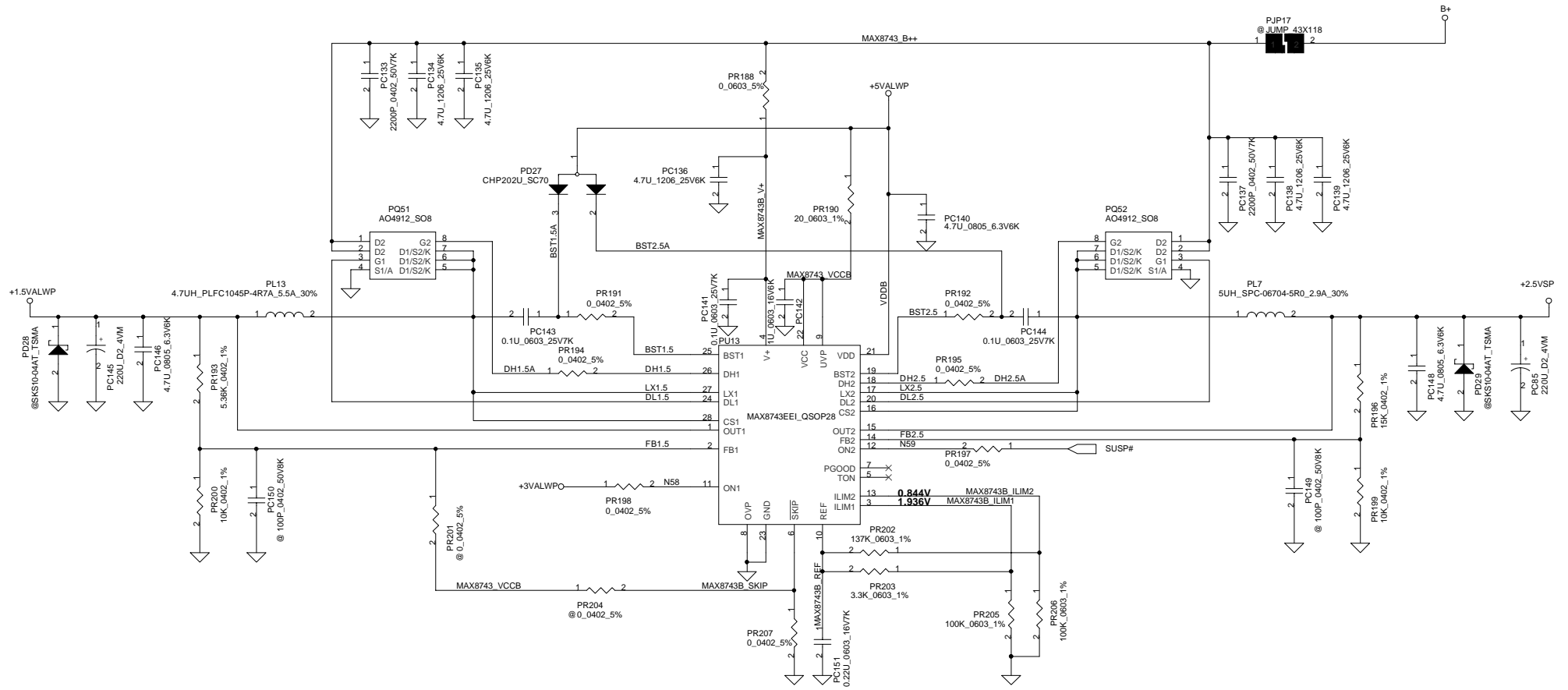
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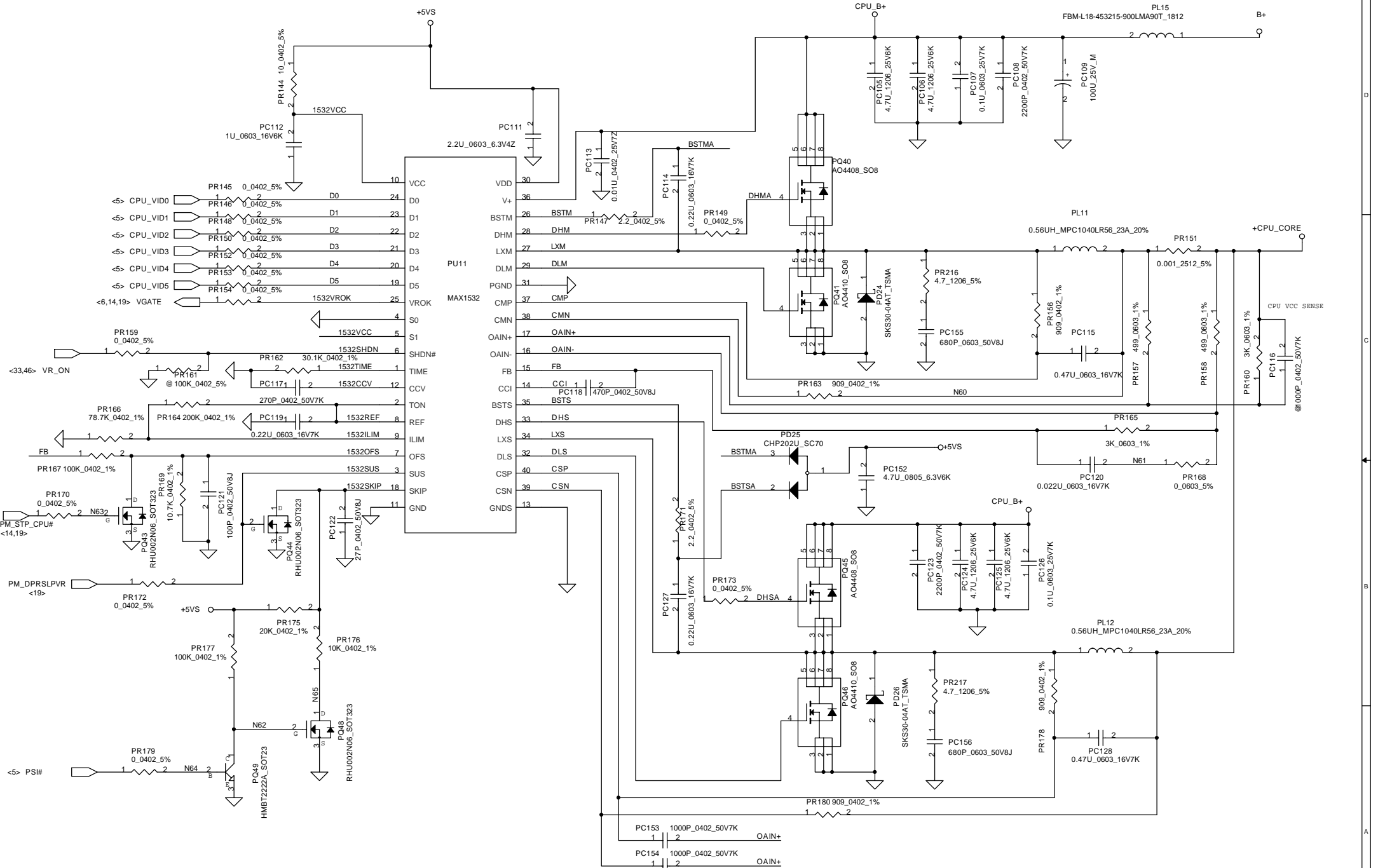
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**+2.5VSP/+1.5VALWP**



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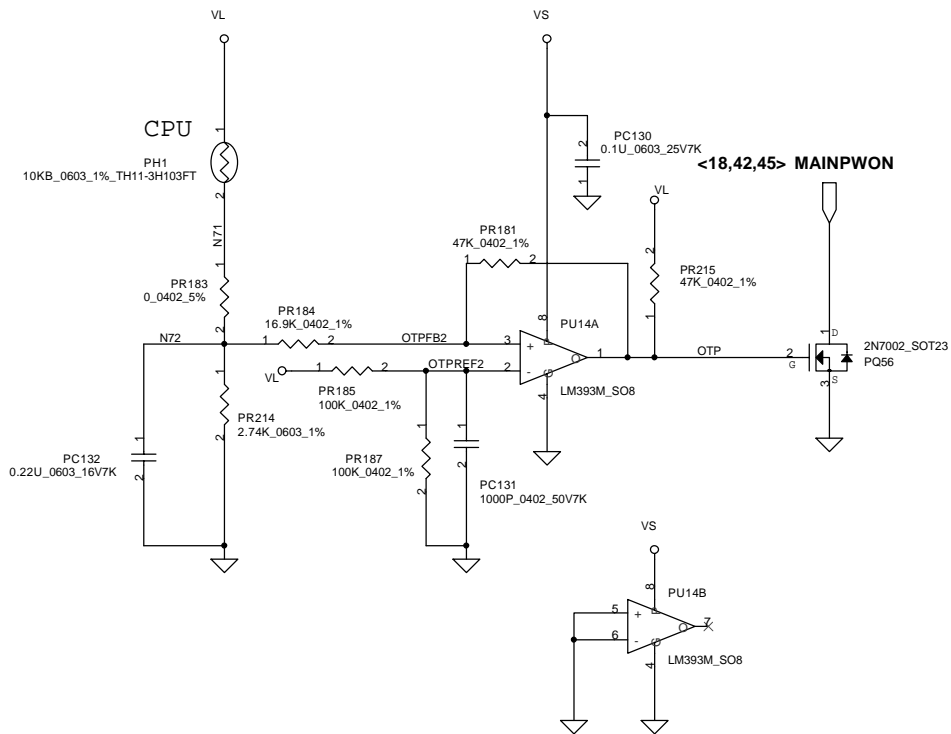


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**PH1 under CPU botten side :**  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 50 +-3 degree C



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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Change DC JAcK and second battery connect.	42,44	Change DC JAcK from DC231105200 to DC231000500. Change second battery connect from	2004.10.28	
2	Modify OTP schematic.	45,49	Change PR114 from 47K_0402_5% to 806K_0603_1%; Change PR183 from 0.0402_5% to 1.37K_0402_1%; Change PR184 from 16.9K_0402_1% to 10K_0402_1%; Change PC132 from 0.22u_0603_16V to 1U_0603_16V; Change PC70 from 0.047uF to 0.47uF; Delete PR186, PR182, PU12 and PQ50.	2004.11.30	
3	To increase the pre-charge current.	42	Change PR21 from 169K_0603_1% to 200K_0603_1%; Change PR10 from 47_1206_5% to 33_1206_5%; Change PR9,PR11 and PR13 from 1.5K_1206_5% to 1K_1206_5%.	2004.12.28	
4	Change OTP schematic to EVT design.	49	Change PR183 from 1.37K_0402_1% to 0.0402_5%; Change PR184 from 10K_0402_1% to 16.9K_0402_1%; Change PC132 from 1U_0603_16V to 0.22u_0603_16V; Add PR215 47K_0402_1%; Add PR214 2.74K_0603_1%; Add PU14 LM393 and PQ56 2N7002.	2005.01.05	
5	For EMI request.	48	Add PR216 and PR217, 4.7_1206_5%; Add P155 and PC156, 680P_0603_50V; Add PL15, FBM-L18-453215-900LMA90T.	2005.01.10	
6	To increase 1.5V power plan to 1.57V by H/W request.	47	Delete PR201; Add PR200 10K_0402_1%; Add PR193 5.36K_0402_1%.	2005.01.10	

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# EAT10 PIR List

\*\*\*\*\* Rev:0.2 PIR List 2004/08/10 Writer by Jason \*\*\*\*\*

P05 : Add @ in R63  
Del @ in R56

P06 : Del @ in R54  
Del JP9

P18: New add R512

P21 : New add R513  
New add X3  
New add C607

P21 : New add R534, R535

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