

Compal Confidential

JALA0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

(With Ati & nVidia MXM/B)

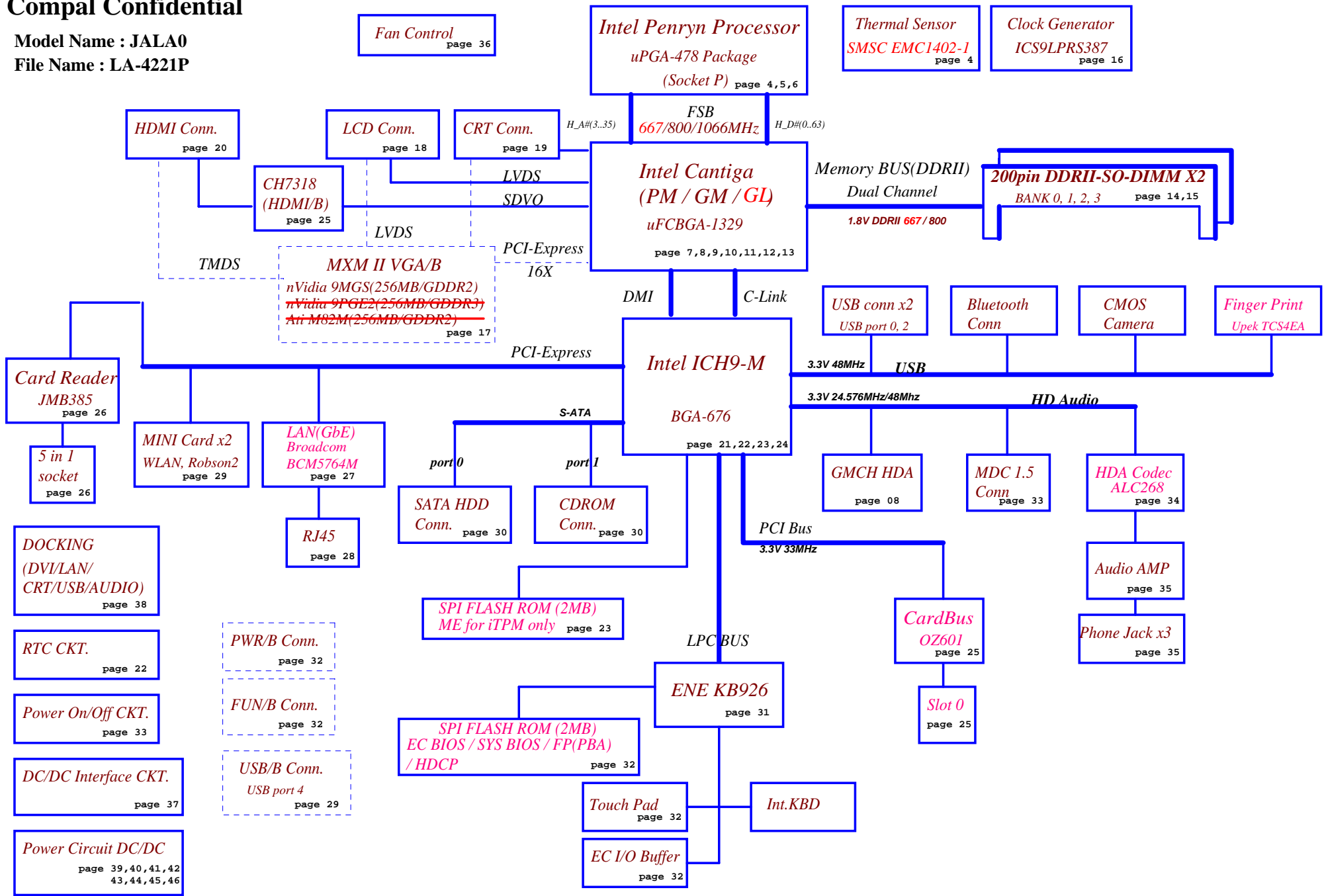
2008-04-18

REV:1.0

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	SCHEMATIC MB A4221	
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Model Name : JALAO
File Name : LA-4221P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Cardbus OZ601	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GPU(MXM/B)	1001 111X b

EC SM Bus2 address

Device	Address
ADT7421	1001 100X b
(LAN BCM5764M)	Reserved

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
LAN BCM5764M	Reserved
(MINI CARD_WL_Robson)	Reserved

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

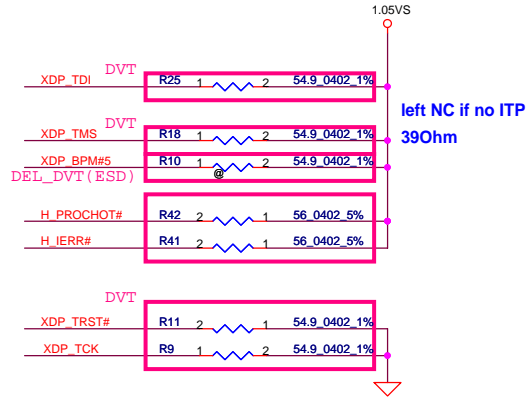
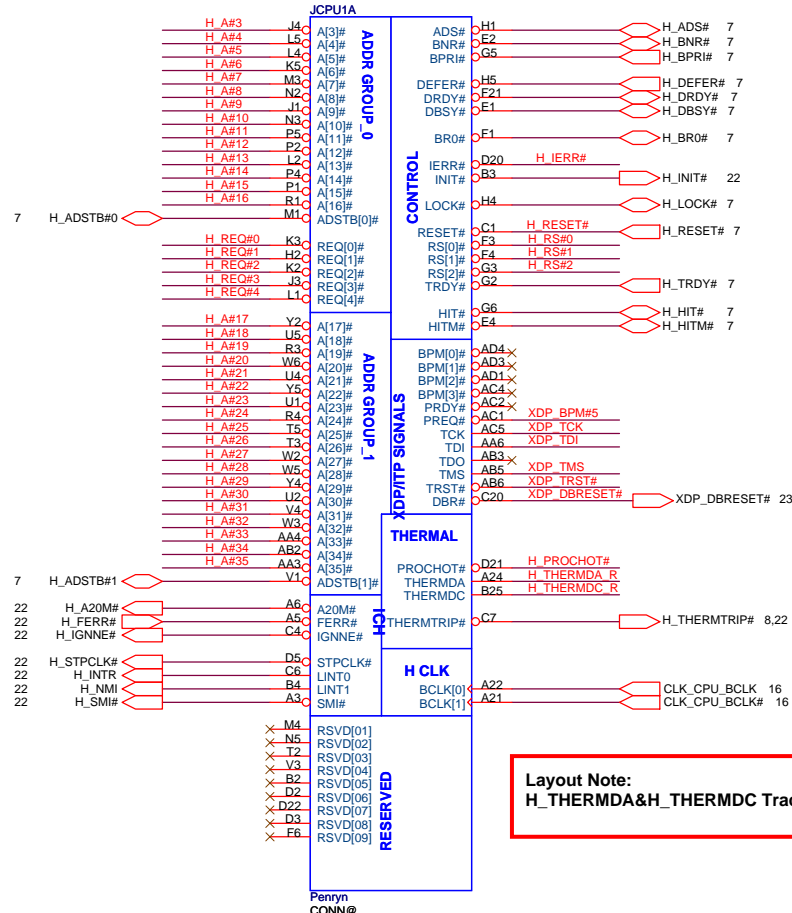
BTO Option Table

BTO Item	BOM Structure
Discrete_H	PM@
UMA	GM@
UMA_H	UMAGM@
UMA_L	UMAGL@
Kinabalu_H	MAIN@
Kinabalu_L	VALUE@
RTC Batt	45@
ICH9M BASE	ICH9MB@
ICH9M ENHANCE	ICH9ME@
SB ROM(2MB)	SPI2MB@
SB ROM(4MB)	SPI4MB@

Kinabalu_L : UMA(GL) & w/o Dock & w/o Mini card 2 & w/o iTPM

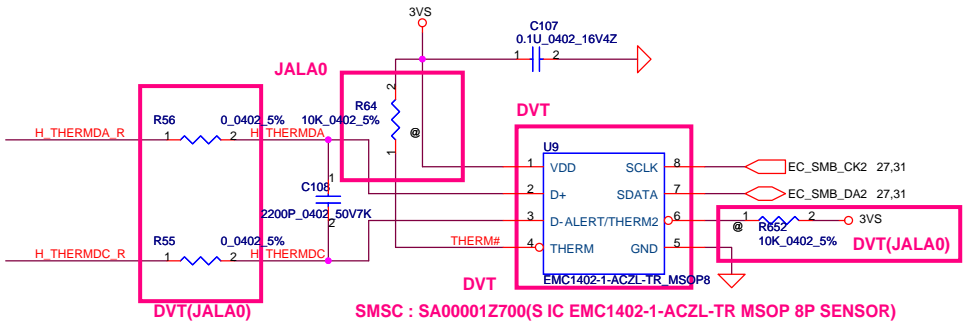
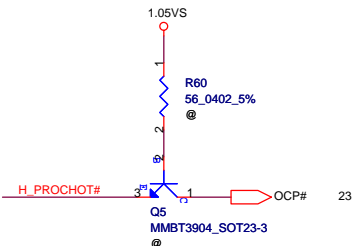
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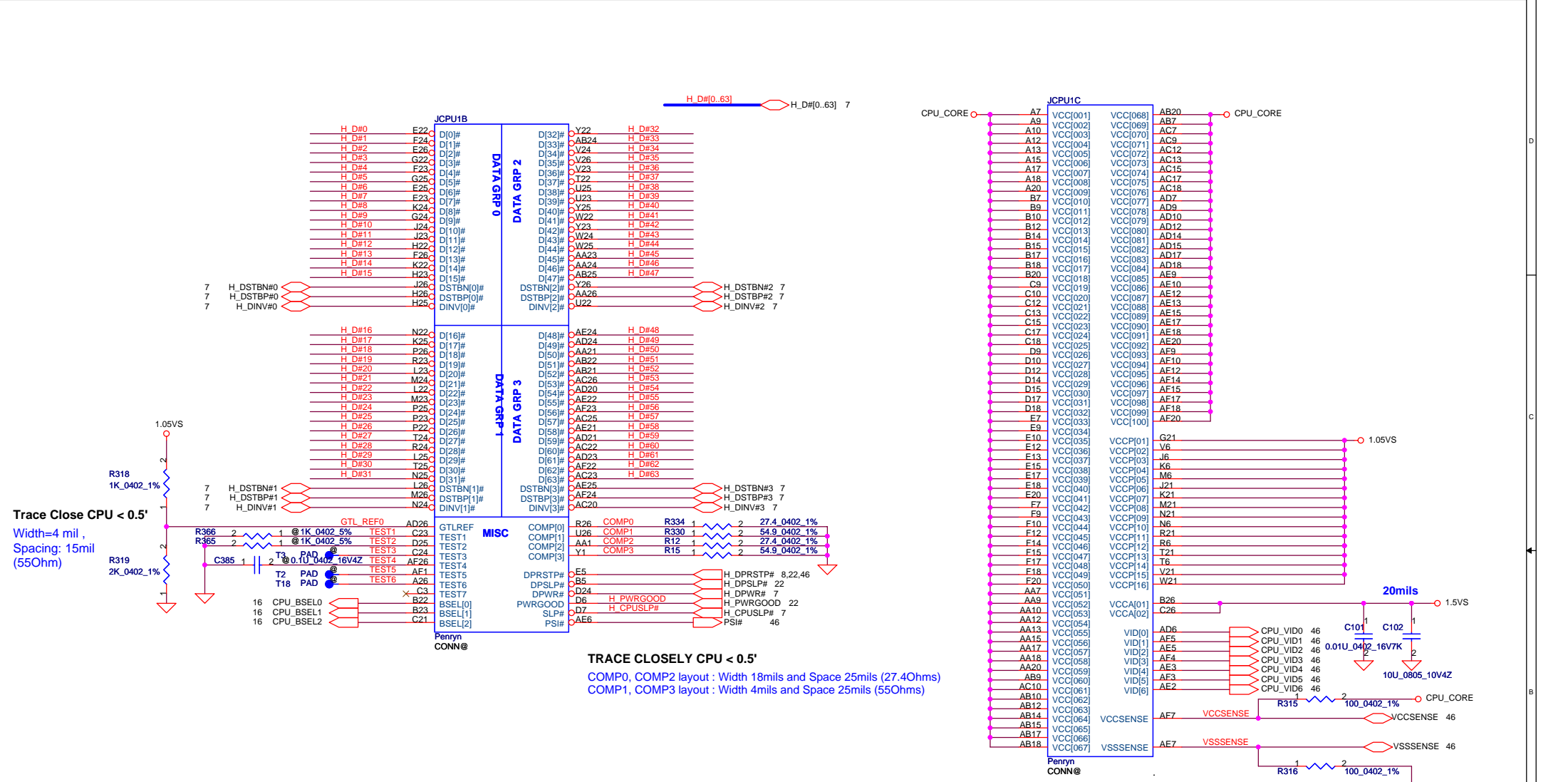
- 7 H_A#[3..35] H_A#[3..35]
- 7 H_REQ#[0..4] H_REQ#[0..4]
- 7 H_RS#[0..2] H_RS#[0..2]



Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

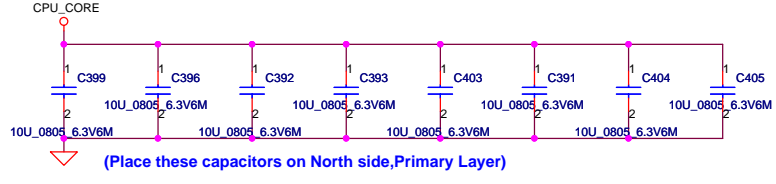
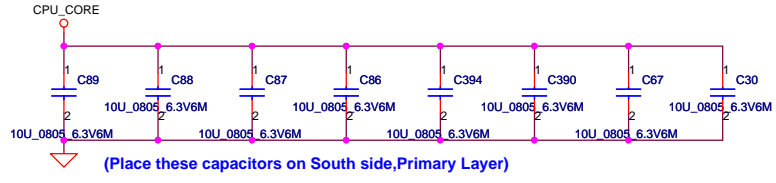
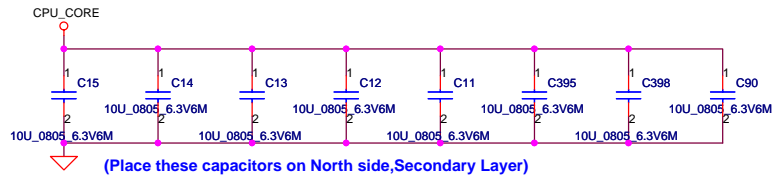
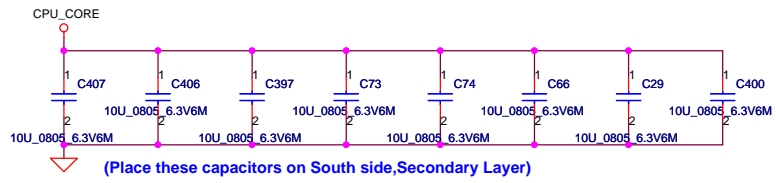
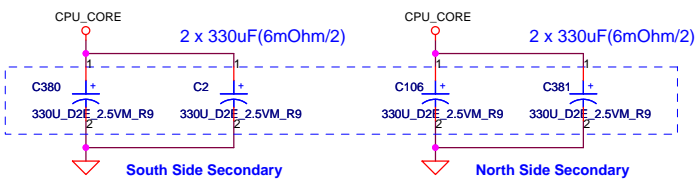




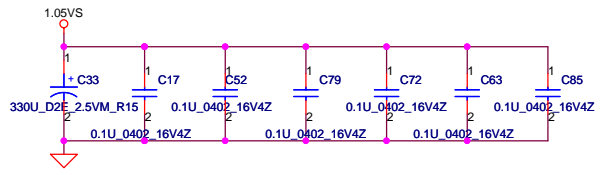
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JCPU1D		
A4	VSSJ001	VSSJ082
A8	VSSJ002	VSSJ083
A11	VSSJ003	VSSJ084
A14	VSSJ004	VSSJ085
A16	VSSJ005	VSSJ086
A19	VSSJ006	VSSJ087
A23	VSSJ007	VSSJ088
AF2	VSSJ008	VSSJ089
B6	VSSJ009	VSSJ090
B8	VSSJ010	VSSJ091
B11	VSSJ011	VSSJ092
B13	VSSJ012	VSSJ093
B16	VSSJ013	VSSJ094
B19	VSSJ014	VSSJ095
B21	VSSJ015	VSSJ096
B24	VSSJ016	VSSJ097
C5	VSSJ017	VSSJ098
C8	VSSJ018	VSSJ099
C11	VSSJ019	VSSJ100
C14	VSSJ020	VSSJ101
C16	VSSJ021	VSSJ102
C19	VSSJ022	VSSJ103
C2	VSSJ023	VSSJ104
C22	VSSJ024	VSSJ105
C25	VSSJ025	VSSJ106
D1	VSSJ026	VSSJ107
D4	VSSJ027	VSSJ108
D8	VSSJ028	VSSJ109
D11	VSSJ029	VSSJ110
D13	VSSJ030	VSSJ111
D16	VSSJ031	VSSJ112
D19	VSSJ032	VSSJ113
D23	VSSJ033	VSSJ114
D26	VSSJ034	VSSJ115
E3	VSSJ035	VSSJ116
E6	VSSJ036	VSSJ117
E8	VSSJ037	VSSJ118
E11	VSSJ038	VSSJ119
E14	VSSJ039	VSSJ120
E16	VSSJ040	VSSJ121
E19	VSSJ041	VSSJ122
E21	VSSJ042	VSSJ123
E24	VSSJ043	VSSJ124
F5	VSSJ044	VSSJ125
F8	VSSJ045	VSSJ126
F11	VSSJ046	VSSJ127
F13	VSSJ047	VSSJ128
F16	VSSJ048	VSSJ129
F19	VSSJ049	VSSJ130
F2	VSSJ050	VSSJ131
F22	VSSJ051	VSSJ132
F25	VSSJ052	VSSJ133
G4	VSSJ053	VSSJ134
G1	VSSJ054	VSSJ135
G23	VSSJ055	VSSJ136
G26	VSSJ056	VSSJ137
H3	VSSJ057	VSSJ138
H6	VSSJ058	VSSJ139
H21	VSSJ059	VSSJ140
H24	VSSJ060	VSSJ141
J2	VSSJ061	VSSJ142
J22	VSSJ062	VSSJ143
J25	VSSJ063	VSSJ144
J25	VSSJ064	VSSJ145
K1	VSSJ065	VSSJ146
K4	VSSJ066	VSSJ147
K23	VSSJ067	VSSJ148
K26	VSSJ068	VSSJ149
L3	VSSJ069	VSSJ150
L6	VSSJ070	VSSJ151
L21	VSSJ071	VSSJ152
L24	VSSJ072	VSSJ153
M2	VSSJ073	VSSJ154
M5	VSSJ074	VSSJ155
M22	VSSJ075	VSSJ156
M25	VSSJ076	VSSJ157
N1	VSSJ077	VSSJ158
N4	VSSJ078	VSSJ159
N23	VSSJ079	VSSJ160
N26	VSSJ080	VSSJ161
P3	VSSJ081	VSSJ162
		VSSJ163

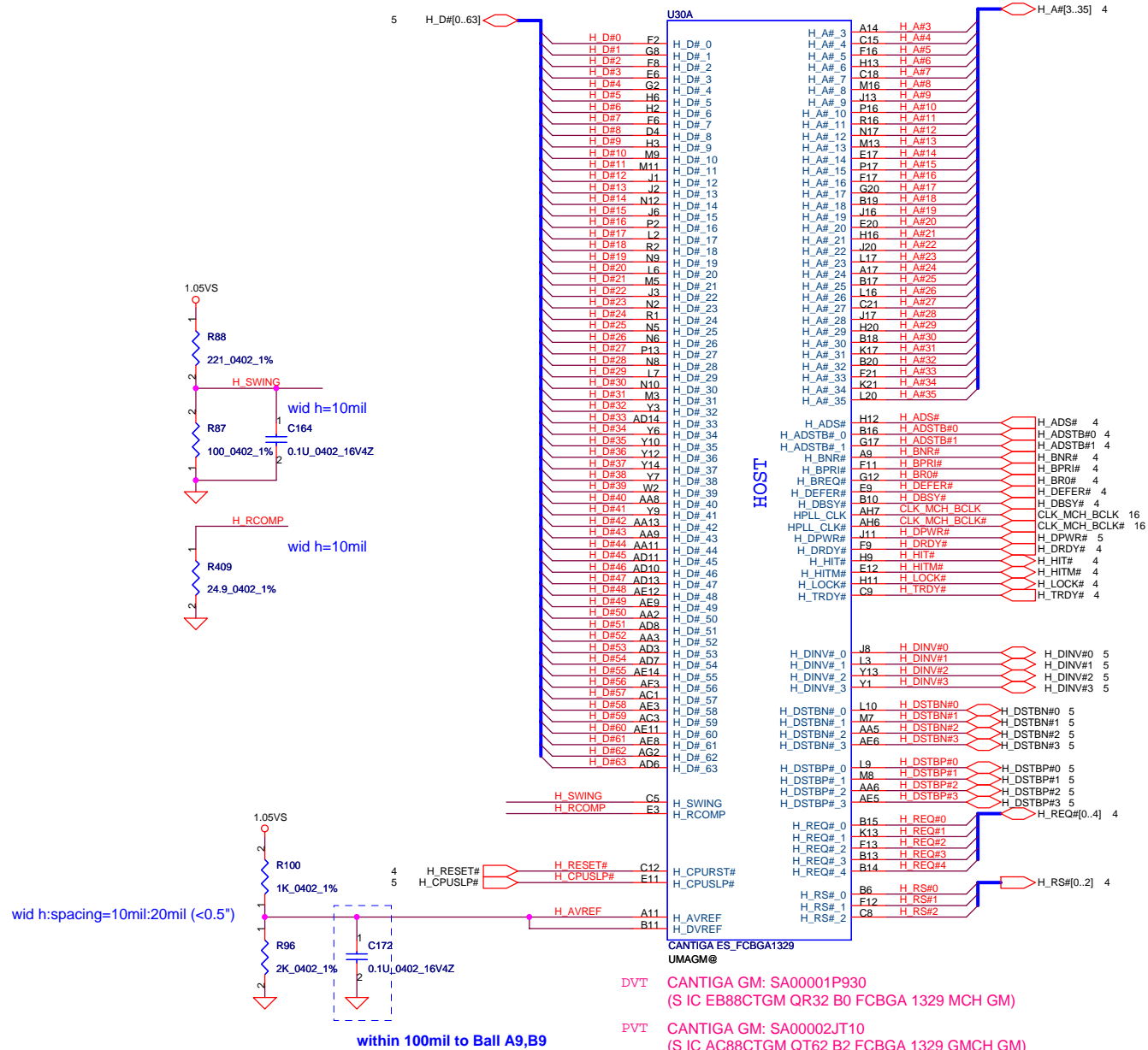
Penryn
CONN@



+CPU-CORE Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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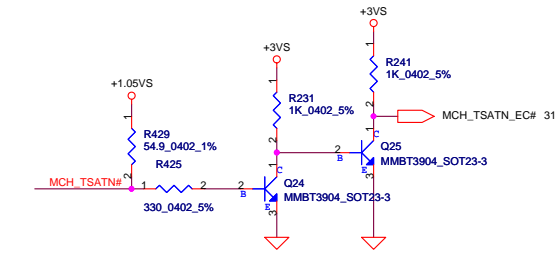
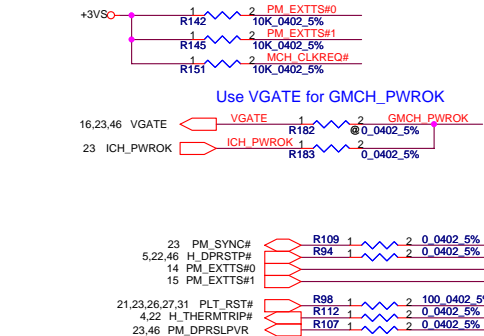
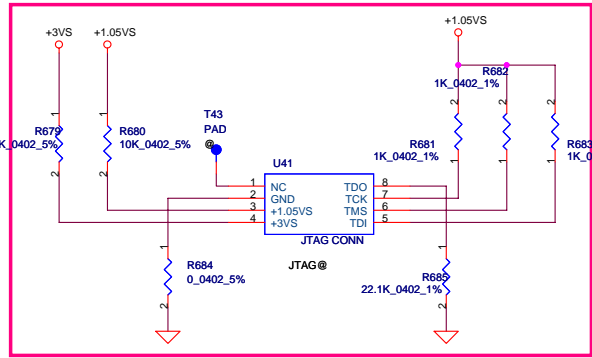


- DVT CANTIGA GM: SA00001P930
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)
- PVT CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)
- PVT2 CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)
- Pre-MP CANTIGA GM: SA00002JTB0
(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABOI)

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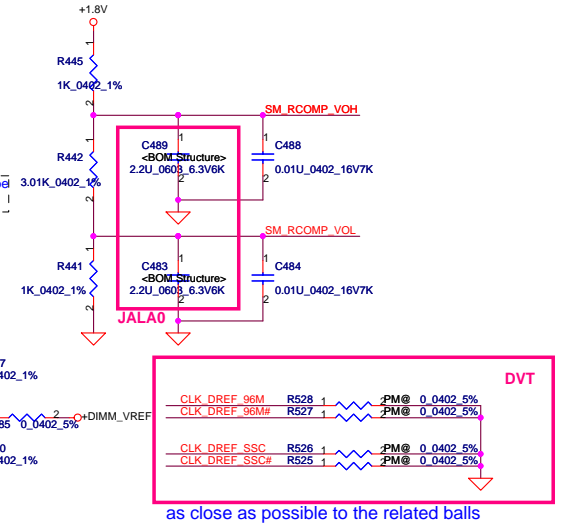
PVT2 JALAO (Add Management Engine JTAG pins)

All RSVD balls on GMCH should be left No Connect.



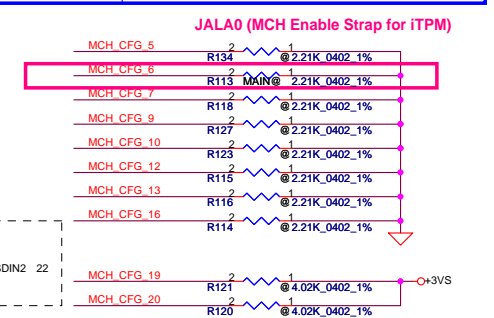
- M36 RSVD1
- N36 RSVD2
- X33 RSVD3
- T33 SB_CK_0
- AH9 RSVD5
- AH10 RSVD6
- AH12 RSVD7
- AH13 RSVD8
- K12 RSVD9
- AL34 RSVD10
- AK34 RSVD11
- AN35 RSVD12
- AM35 RSVD13
- T24 RSVD14
- B31 RSVD15
- B2 RSVD16
- M1 RSVD17
- AV21 RSVD20
- BC23 RSVD22
- BE23 RSVD23
- BH18 RSVD24
- BE18 RSVD25
- BC23 RSVD22
- BE23 RSVD23
- BH18 RSVD24
- BE18 RSVD25
- MCH_CLKSEL0 MCH_CLKSEL0 R25
- MCH_CLKSEL1 MCH_CLKSEL1 R25
- MCH_CLKSEL2 MCH_CLKSEL2 R25
- MCH_CFG_5 MCH_CFG_5 C25
- MCH_CFG_6 MCH_CFG_6 N24
- MCH_CFG_7 MCH_CFG_7 N24
- MCH_CFG_9 MCH_CFG_9 C23
- MCH_CFG_10 MCH_CFG_10 C24
- MCH_CFG_12 MCH_CFG_12 N21
- MCH_CFG_13 MCH_CFG_13 T21
- MCH_CFG_16 MCH_CFG_16 M20
- MCH_CFG_19 MCH_CFG_19 P29
- MCH_CFG_20 MCH_CFG_20 R28
- PM_SYNC# PM_SYNC# R29
- PM_DPRSTP# PM_DPRSTP# B7
- PM_EXT_TSN_0 PM_EXT_TSN_0 N33
- PM_EXT_TSN_1 PM_EXT_TSN_1 P32
- GMCH_PWROK GMCH_PWROK AT40
- MCH_RSTIN# MCH_RSTIN# AT11
- THERMTRIP# THERMTRIP# T20
- DPRSLPVR DPRSLPVR R32
- NC_1 NC_1 BG48
- NC_2 NC_2 BF48
- NC_3 NC_3 BD48
- NC_4 NC_4 BC48
- NC_5 NC_5 BH47
- NC_6 NC_6 BG47
- NC_7 NC_7 SH46
- NC_8 NC_8 BF46
- NC_9 NC_9 BG45
- NC_10 NC_10 GH45
- NC_11 NC_11 BH44
- NC_12 NC_12 SH43
- NC_13 NC_13 BH6
- NC_14 NC_14 BH5
- NC_15 NC_15 BG4
- NC_16 NC_16 BH3
- NC_17 NC_17 BE3
- NC_18 NC_18 BH2
- NC_19 NC_19 BG2
- NC_20 NC_20 BE2
- NC_21 NC_21 BE1
- NC_22 NC_22 BC1
- NC_23 NC_23 F1
- NC_24 NC_24 NC_24
- NC_25 NC_25 NC_25
- NC_26 NC_26 NC_26
- NC_1 NC_1 BG48
- NC_2 NC_2 BF48
- NC_3 NC_3 BD48
- NC_4 NC_4 BC48
- NC_5 NC_5 BH47
- NC_6 NC_6 BG47
- NC_7 NC_7 SH46
- NC_8 NC_8 BF46
- NC_9 NC_9 BG45
- NC_10 NC_10 GH45
- NC_11 NC_11 BH44
- NC_12 NC_12 SH43
- NC_13 NC_13 BH6
- NC_14 NC_14 BH5
- NC_15 NC_15 BG4
- NC_16 NC_16 BH3
- NC_17 NC_17 BE3
- NC_18 NC_18 BH2
- NC_19 NC_19 BG2
- NC_20 NC_20 BE2
- NC_21 NC_21 BE1
- NC_22 NC_22 BC1
- NC_23 NC_23 F1
- NC_24 NC_24 NC_24
- NC_25 NC_25 NC_25
- NC_26 NC_26 NC_26

- SA_CK_0 AP24 DDRD_CLK0 14
- SA_CK_1 AT21 DDRD_CLK1 14
- AV24 AV24 DDRB_CLK0 15
- SA_CK_0 AR24 DDRD_CLK0# 14
- SA_CK_1 AR21 DDRD_CLK1# 14
- SA_CK_0 AV24 AV24 DDRB_CLK# 15
- SA_CK_1 AV20 AV20 DDRB_CLK# 15
- SA_CKE_0 BC28 DDRD_CKE0 14
- SA_CKE_1 AY28 DDRD_CKE1 14
- SA_CKE_0 AY36 DDRB_CKE0 15
- SA_CKE_1 BB36 DDRB_CKE1 15
- SA_CSE_0 BA17 DDRD_SCS0# 14
- SA_CSE_1 AY16 DDRD_SCS1# 14
- SA_CSE_0 AV16 AV16 DDRB_SCS0# 15
- SA_CSE_1 AR13 AR13 DDRB_SCS1# 15
- SA_ODT_0 BD17 DDRD_ODT0 14
- SA_ODT_1 AY17 DDRD_ODT1 14
- SA_ODT_0 BF15 DDRB_ODT0 15
- SA_ODT_1 AY13 AY13 DDRB_ODT1 15
- SM_RCAMP SM_RCAMP BG22 80.6 0402 1%
- SM_RCAMP# SM_RCAMP# BH21 80.6 0402 1%
- SM_RCAMP_VOH SM_RCAMP_VOH BF28 80.6 0402 1%
- SM_RCAMP_VOL SM_RCAMP_VOL BH28 80.6 0402 1%
- SM_PWROK SM_PWROK AR36 2 0 0402 5%
- SM_REXT SM_REXT BF17 2 499 0402 1%
- SM_DRAMRST# SM_DRAMRST# BC36
- DPLL_REF_CLK B38 CLK_DREF_96M CLK_DREF_96M 16
- DPLL_REF_CLK# A38 CLK_DREF_96M# CLK_DREF_96M# 16
- DPLL_REF_SSCLK F41 CLK_DREF_SSC# CLK_DREF_SSC# 16
- DPLL_REF_SSCLK# E41 CLK_DREF_SSC# CLK_DREF_SSC# 16
- PEG_CLK F43 CLK_MCH_3GPLL CLK_MCH_3GPLL 16
- PEG_CLK# E43 CLK_MCH_3GPLL# CLK_MCH_3GPLL# 16
- DMI_RXN_0 AE41 DMI_ITX_MR_X0 DMI_ITX_MR_X0 23
- DMI_RXN_1 AE37 DMI_ITX_MR_X1 DMI_ITX_MR_X1 23
- DMI_RXN_2 AE47 DMI_ITX_MR_X2 DMI_ITX_MR_X2 23
- DMI_RXN_3 AH39 DMI_ITX_MR_X3 DMI_ITX_MR_X3 23
- DMI_RXP_0 AE40 DMI_ITX_MR_X0 DMI_ITX_MR_X0 23
- DMI_RXP_1 AE38 DMI_ITX_MR_X1 DMI_ITX_MR_X1 23
- DMI_RXP_2 AE48 DMI_ITX_MR_X2 DMI_ITX_MR_X2 23
- DMI_RXP_3 AH40 DMI_ITX_MR_X3 DMI_ITX_MR_X3 23
- DMI_TXN_0 AE35 DMI_MTX_IR_X0 DMI_MTX_IR_X0 23
- DMI_TXN_1 AE43 DMI_MTX_IR_X1 DMI_MTX_IR_X1 23
- DMI_TXN_2 AE46 DMI_MTX_IR_X2 DMI_MTX_IR_X2 23
- DMI_TXN_3 AH42 DMI_MTX_IR_X3 DMI_MTX_IR_X3 23
- DMI_TXP_0 AD35 DMI_MTX_IR_X0 DMI_MTX_IR_X0 23
- DMI_TXP_1 AE44 DMI_MTX_IR_X1 DMI_MTX_IR_X1 23
- DMI_TXP_2 AE46 DMI_MTX_IR_X2 DMI_MTX_IR_X2 23
- DMI_TXP_3 AH43 DMI_MTX_IR_X3 DMI_MTX_IR_X3 23
- GFX_VID_0 B33
- GFX_VID_1 B32
- GFX_VID_2 G33
- GFX_VID_3 F33
- GFX_VID_4 E33
- GFX_VR_EN C34
- CL_CLK AH37 CL_CLK0 23
- CL_DATA AH36 CL_DATA0 23
- ICH_PWROK AN38 ICH_PWROK
- CL_RST# AH34 CL_RST# 23
- CL_VREF AH34 CL_VREF
- DDPC_CTRLCLK M28
- SDVO_CTRLCLK G36 SDVO_SCLK 17
- SDVO_CTRLDATA E36 SDVO_SDATA 17
- SDVO_CTRLDATA H36 MCH_CLKREQ# 16
- ICH_SYNC# H36 MCH_ICH_SYNC# 23
- MCH_TSN# B12 MCH_TSN#
- HDA_BCLK B28 HDA_BITCLK_MCH HDA_BITCLK_MCH 22
- HDA_RST# B30 HDA_RST_MCH# HDA_RST_MCH# 22
- HDA_SDI B29 HDA_SDI2_MCH HDA_SDI2_MCH 22
- HDA_SDO C29 HDA_SDO2_MCH HDA_SDO2_MCH 22
- HDA_SYNC A28 HDA_SYNC_MCH HDA_SYNC_MCH 22



Strap Pin Table

CFG[2 0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIE Loopback Enable 1 = Disable * (Default)
CFG[13 12]	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L DDC DATA	0 = LFP Disable 1 = LFP Card Present PCIE disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

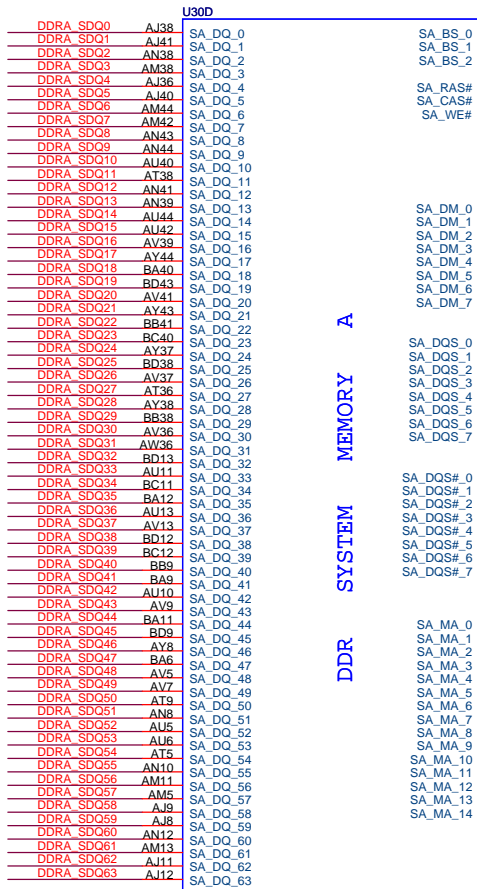
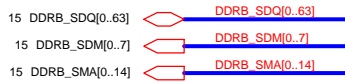
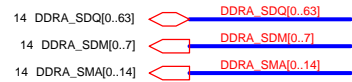


Notice: Please check HDA power rail to select HDA controller.

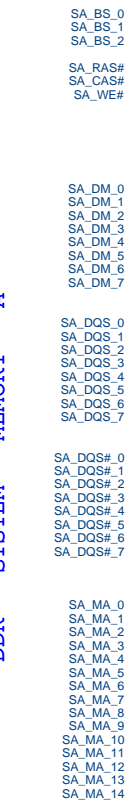
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PVT2 CANTIGA GM: SA00002JT50 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM) PVT CANTIGA GM: SA00002JT10 (S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

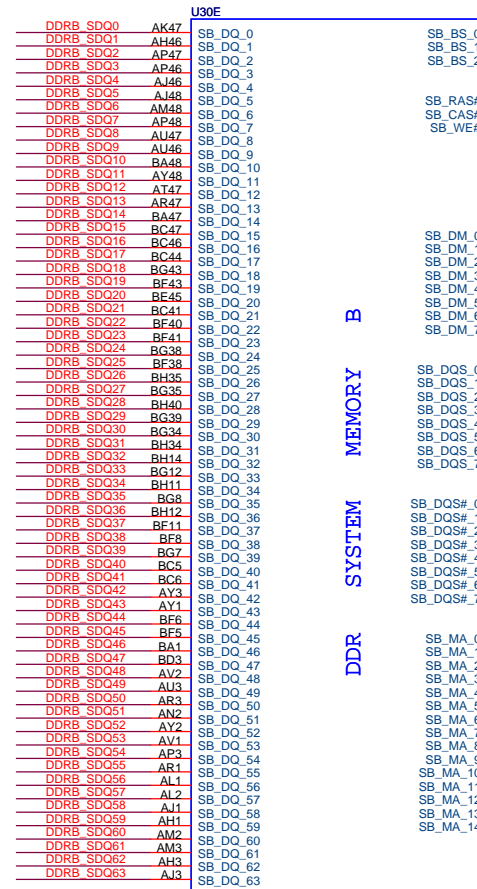
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Date: Friday, May 16, 2008 Sheet: 8 of 50				



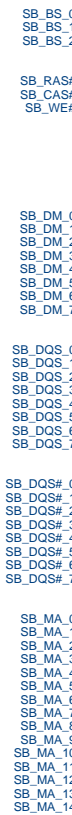
DDR SYSTEM MEMORY A



CANTIGA ES_FCBGA1329
UMAGM@



DDR SYSTEM MEMORY B



CANTIGA ES_FCBGA1329
UMAGM@

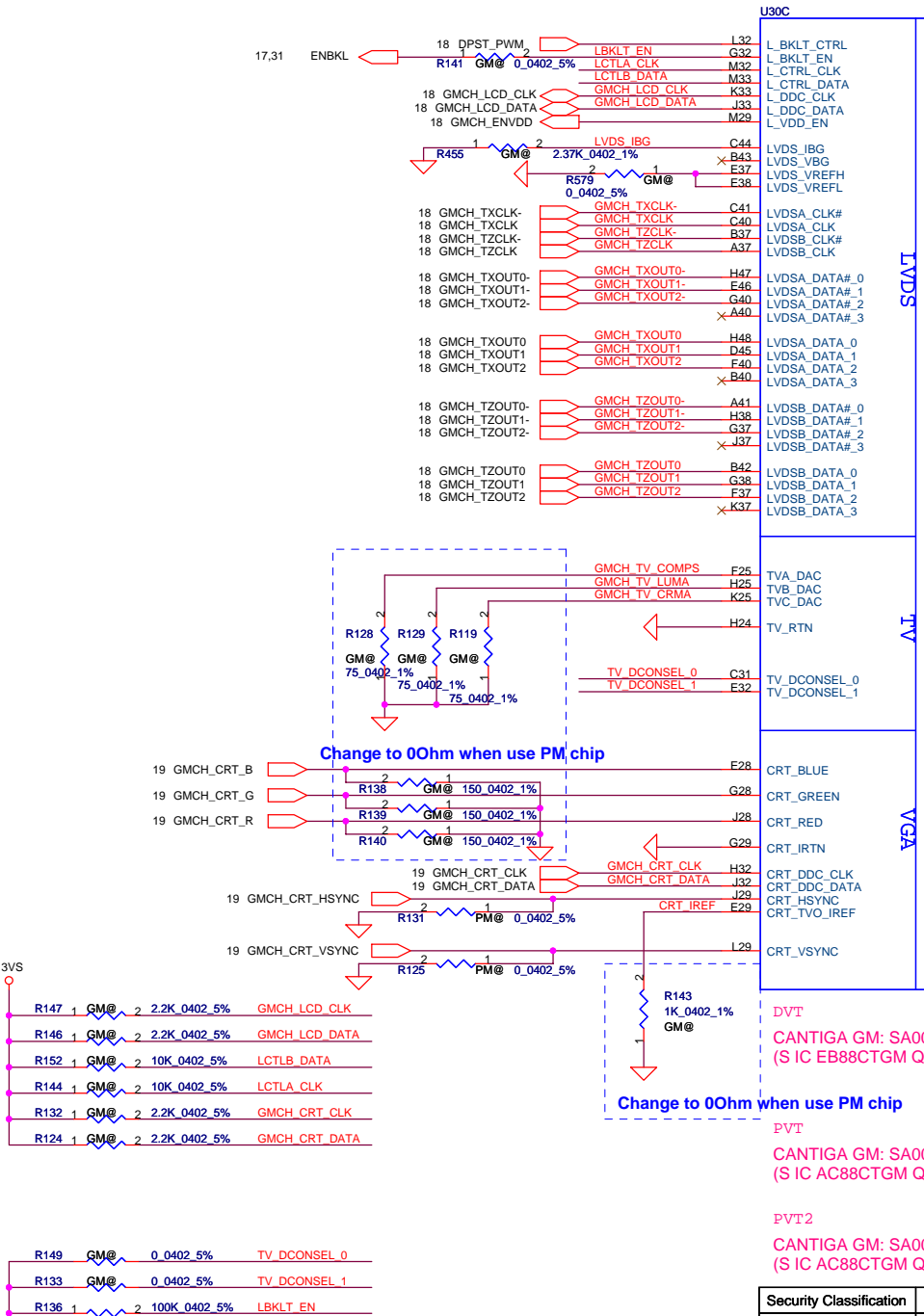
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Pre-MP CANTIGA GM: SA00002JTBO (S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO!)

PVT CANTIGA GM: SA00002JT10 (S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

PVT2 CANTIGA GM: SA00002JT50 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

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SCAT

LVDS

PCI-EXPRESS

GRAPHICS

AI

VGA

CANTIGA ES_FCBGA1329
UMAGM@

DVT

CANTIGA GM: SA00001P930
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)

Pre-MP

CANTIGA GM: SA00002JTBO
(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO!)

PVT

CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

PVT2

CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

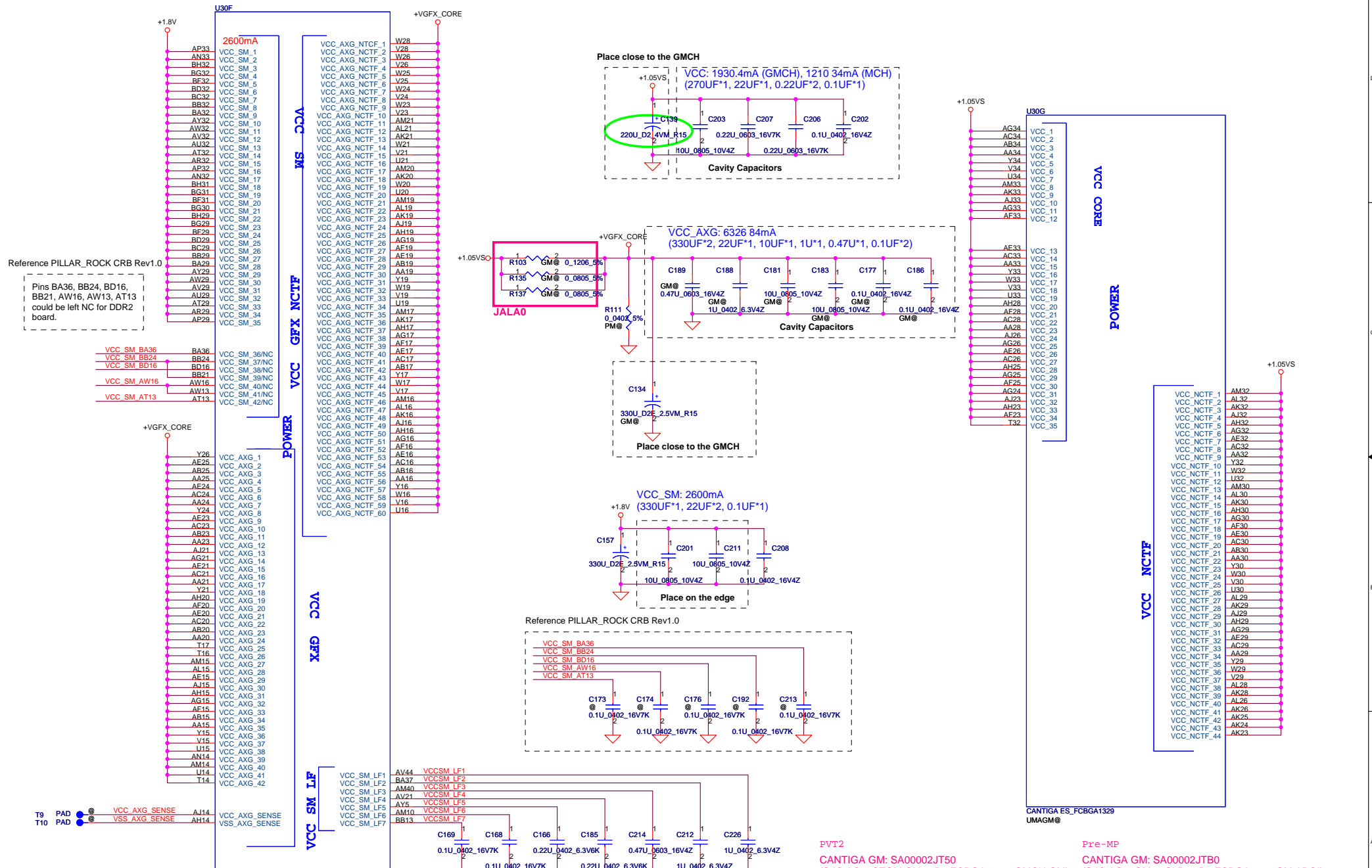
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T37 PEG_COMP 1 2 49.9_0402_1% 1.05VS
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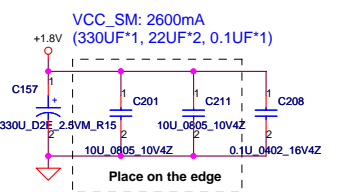
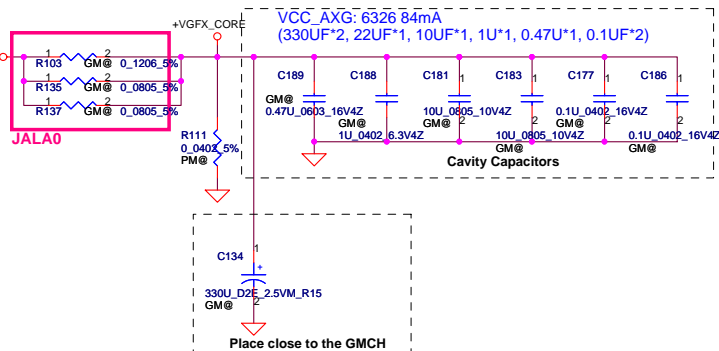
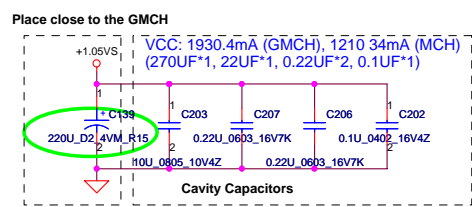
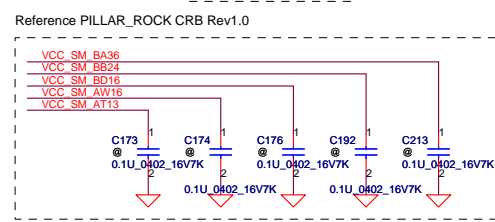
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 PEG_RX#_2 L44 PCIE GTX C MRX N2
 PEG_RX#_3 L40 PCIE GTX C MRX N3
 PEG_RX#_4 N41 PCIE GTX C MRX N4
 PEG_RX#_5 P48 PCIE GTX C MRX N5
 PEG_RX#_6 N44 PCIE GTX C MRX N6
 PEG_RX#_7 T43 PCIE GTX C MRX N7
 PEG_RX#_8 U43 PCIE GTX C MRX N8
 PEG_RX#_9 Y43 PCIE GTX C MRX N9
 PEG_RX#_10 Y48 PCIE GTX C MRX N10
 PEG_RX#_11 Y36 PCIE GTX C MRX N11
 PEG_RX#_12 AA43 PCIE GTX C MRX N12
 PEG_RX#_13 AD37 PCIE GTX C MRX N13
 PEG_RX#_14 AC47 PCIE GTX C MRX N14
 PEG_RX#_15 AD39 PCIE GTX C MRX N15

PEG_TX#_0 H43 PCIE GTX C MRX P0
 PEG_TX#_1 J44 PCIE GTX C MRX P1
 PEG_TX#_2 L43 PCIE GTX C MRX P2
 PEG_TX#_3 L41 PCIE GTX C MRX P3
 PEG_TX#_4 N40 PCIE GTX C MRX P4
 PEG_TX#_5 P47 PCIE GTX C MRX P5
 PEG_TX#_6 N43 PCIE GTX C MRX P6
 PEG_TX#_7 T42 PCIE GTX C MRX P7
 PEG_TX#_8 U42 PCIE GTX C MRX P8
 PEG_TX#_9 Y42 PCIE GTX C MRX P9
 PEG_TX#_10 W47 PCIE GTX C MRX P10
 PEG_TX#_11 Y37 PCIE GTX C MRX P11
 PEG_TX#_12 AA42 PCIE GTX C MRX P12
 PEG_TX#_13 AD36 PCIE GTX C MRX P13
 PEG_TX#_14 AC48 PCIE GTX C MRX P14
 PEG_TX#_15 AD40 PCIE GTX C MRX P15

PEG_TX#_0	J41	PCIE_MTX_C_GRX_N0	C225	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_N0
PEG_TX#_1	M46	PCIE_MTX_GRX_N1	C236	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_N1
PEG_TX#_2	M47	PCIE_MTX_GRX_N2	C239	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_N2
PEG_TX#_3	M40	PCIE_MTX_GRX_N3	C241	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_N3
PEG_TX#_4	M42	PCIE_MTX_GRX_N4	C243	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N4
PEG_TX#_5	R48	PCIE_MTX_GRX_N5	C246	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N5
PEG_TX#_6	N38	PCIE_MTX_GRX_N6	C251	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N6
PEG_TX#_7	T40	PCIE_MTX_GRX_N7	C255	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N7
PEG_TX#_8	U37	PCIE_MTX_GRX_N8	C257	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N8
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PEG_TX#_11	AA46	PCIE_MTX_GRX_N11	C274	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N11
PEG_TX#_12	AA37	PCIE_MTX_GRX_N12	C286	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_N12
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PEG_TX#_1	L46	PCIE_MTX_GRX_P1	C233	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_P1
PEG_TX#_2	M48	PCIE_MTX_GRX_P2	C238	1	2	0.1U_0402_16V7K	PCIE_MTX_C_GRX_P2
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PEG_TX#_7	T39	PCIE_MTX_GRX_P7	C252	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_P7
PEG_TX#_8	J36	PCIE_MTX_GRX_P8	C253	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_P8
PEG_TX#_9	U39	PCIE_MTX_GRX_P9	C260	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_P9
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PEG_TX#_15	AD46	PCIE_MTX_GRX_P15	C270	1	2	PM@ 0.1U_0402_16V7K	PCIE_MTX_C_GRX_P15



Reference PILLAR_ROCK CRB Rev1.0
 Pins BA36, BB24, BB21, AW16, AT13 could be left NC for DDR2 board.



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 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

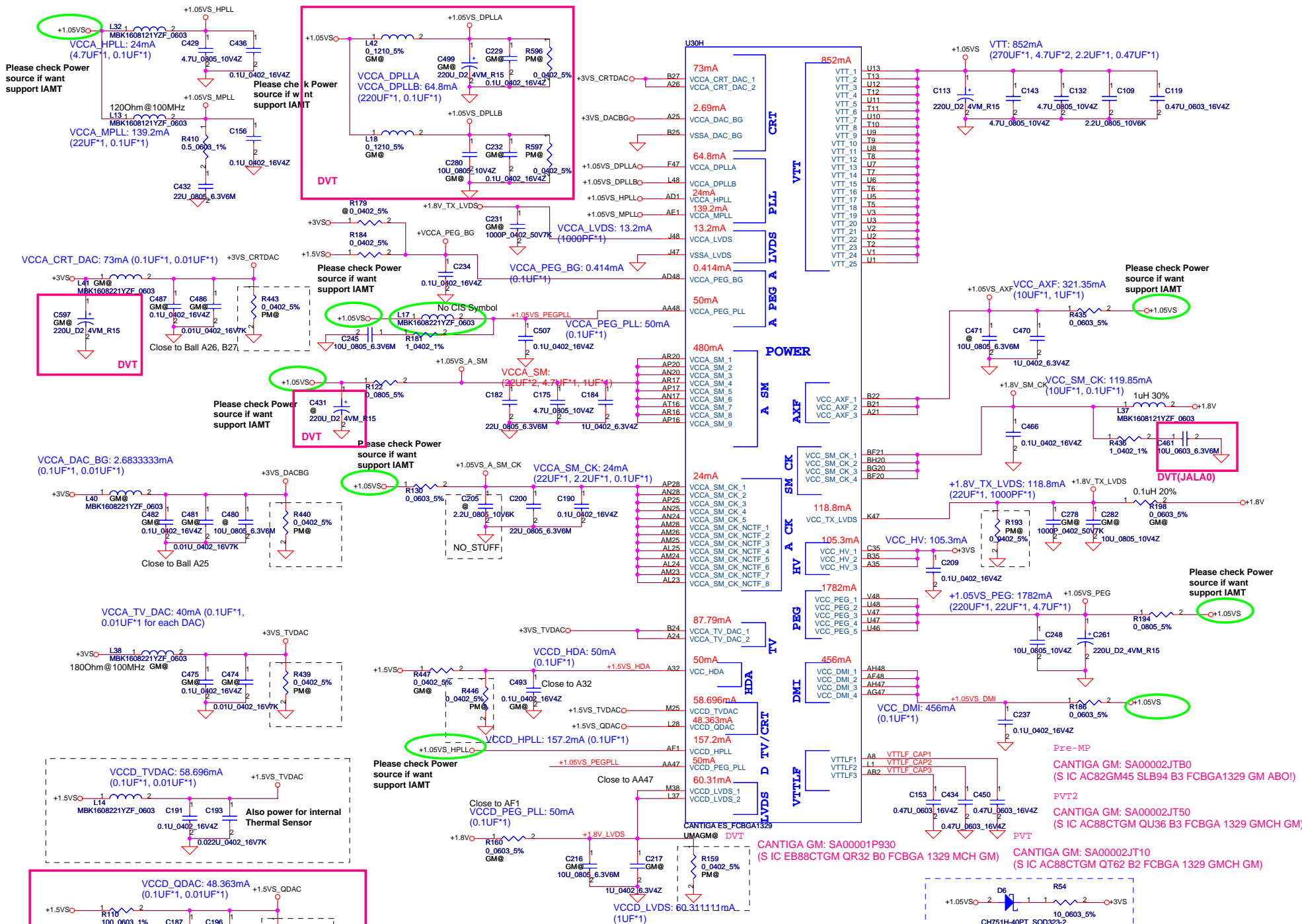
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				Date	Sheet
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DVT
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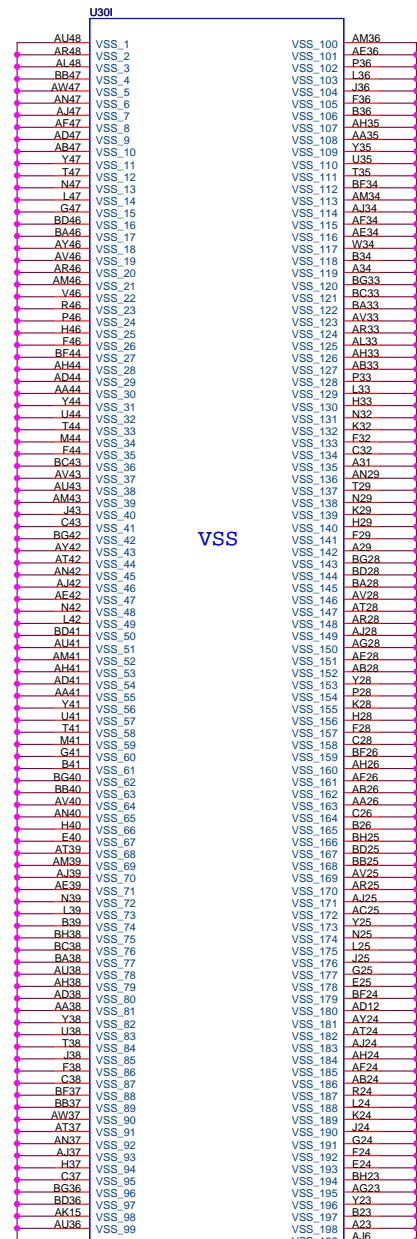
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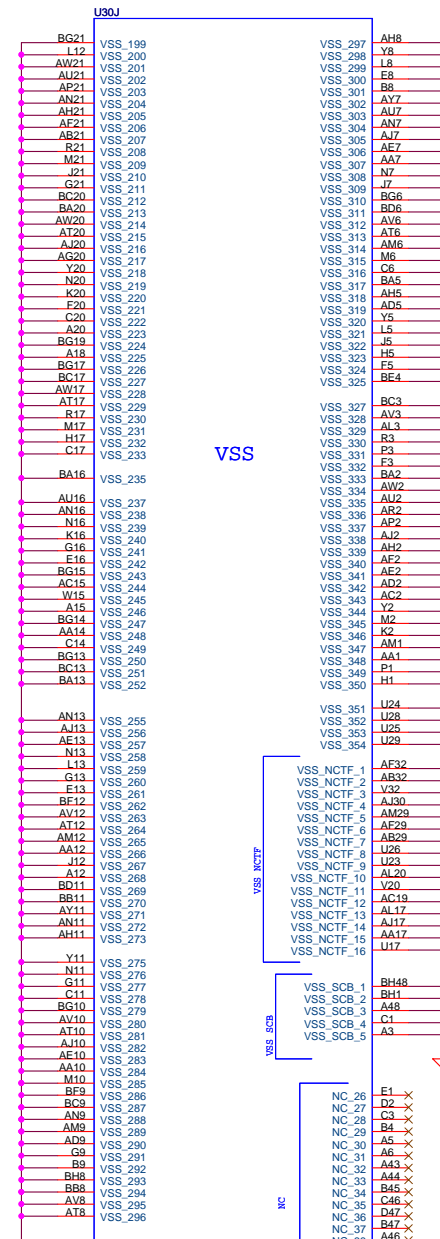
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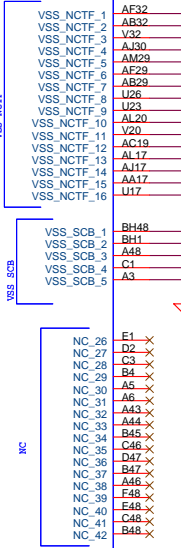
VSS

CANTIGA ES_FCBGA1329
UMAGM®



VSS

CANTIGA ES_FCBGA1329
UMAGM®



VSS_NCTF

VSS_SCB

NC

PVT2
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(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

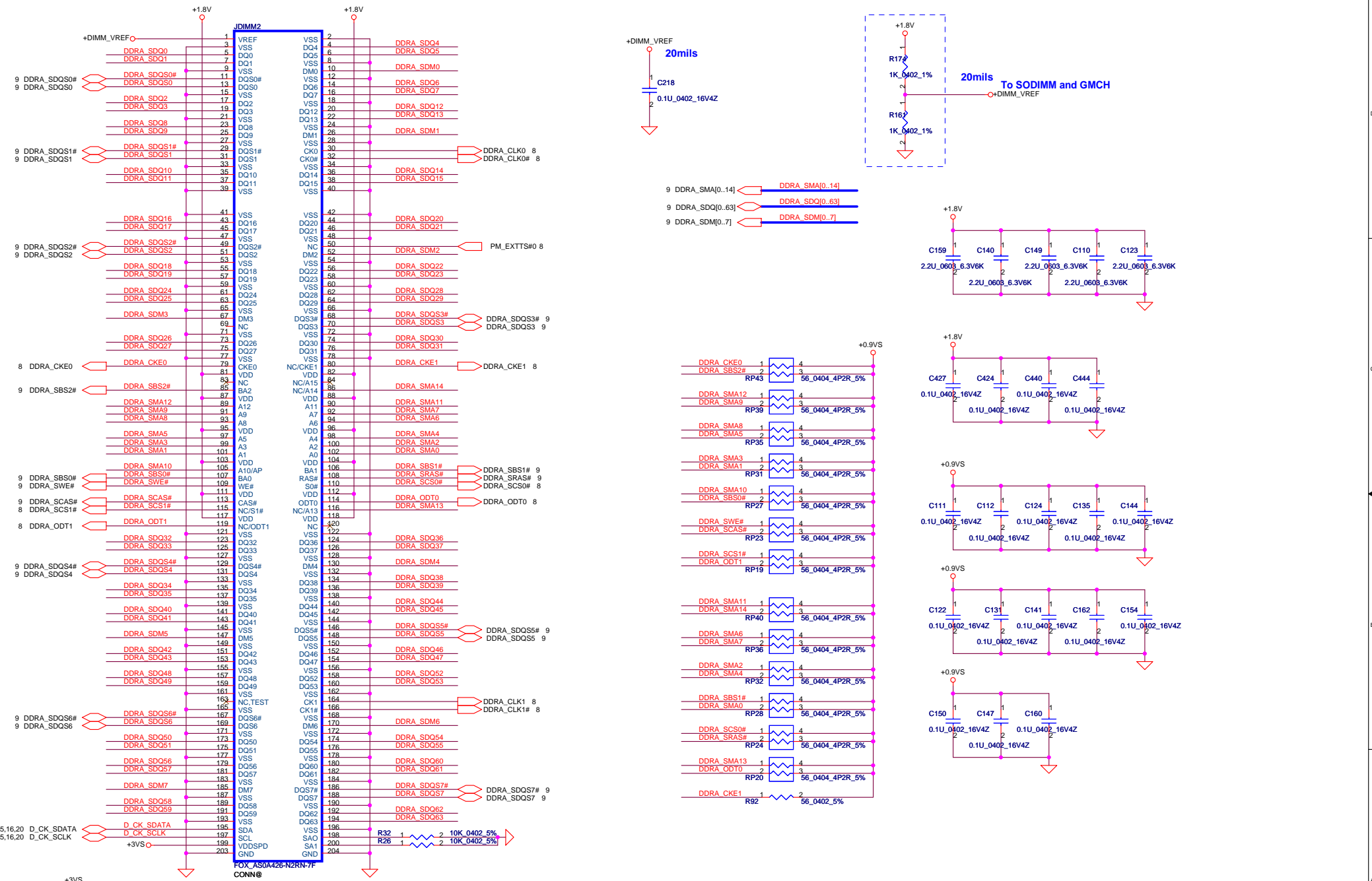
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Pre-MP
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PVT
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(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

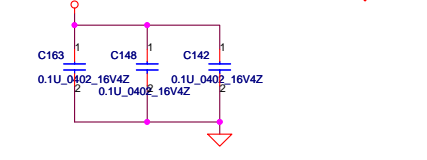
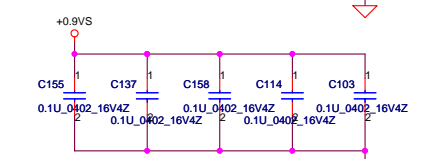
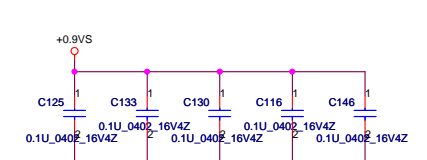
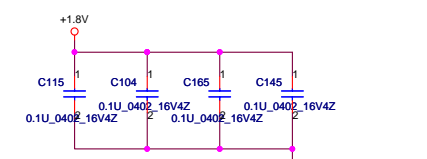
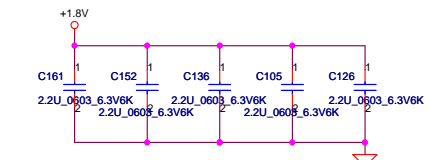
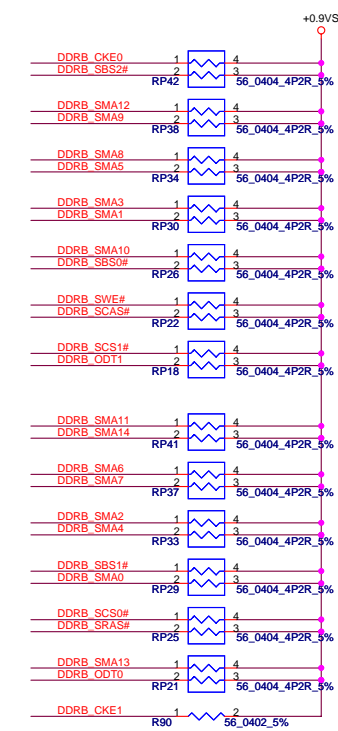
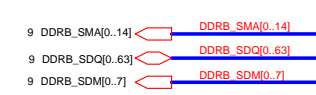
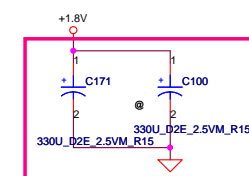
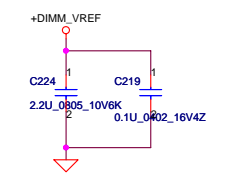
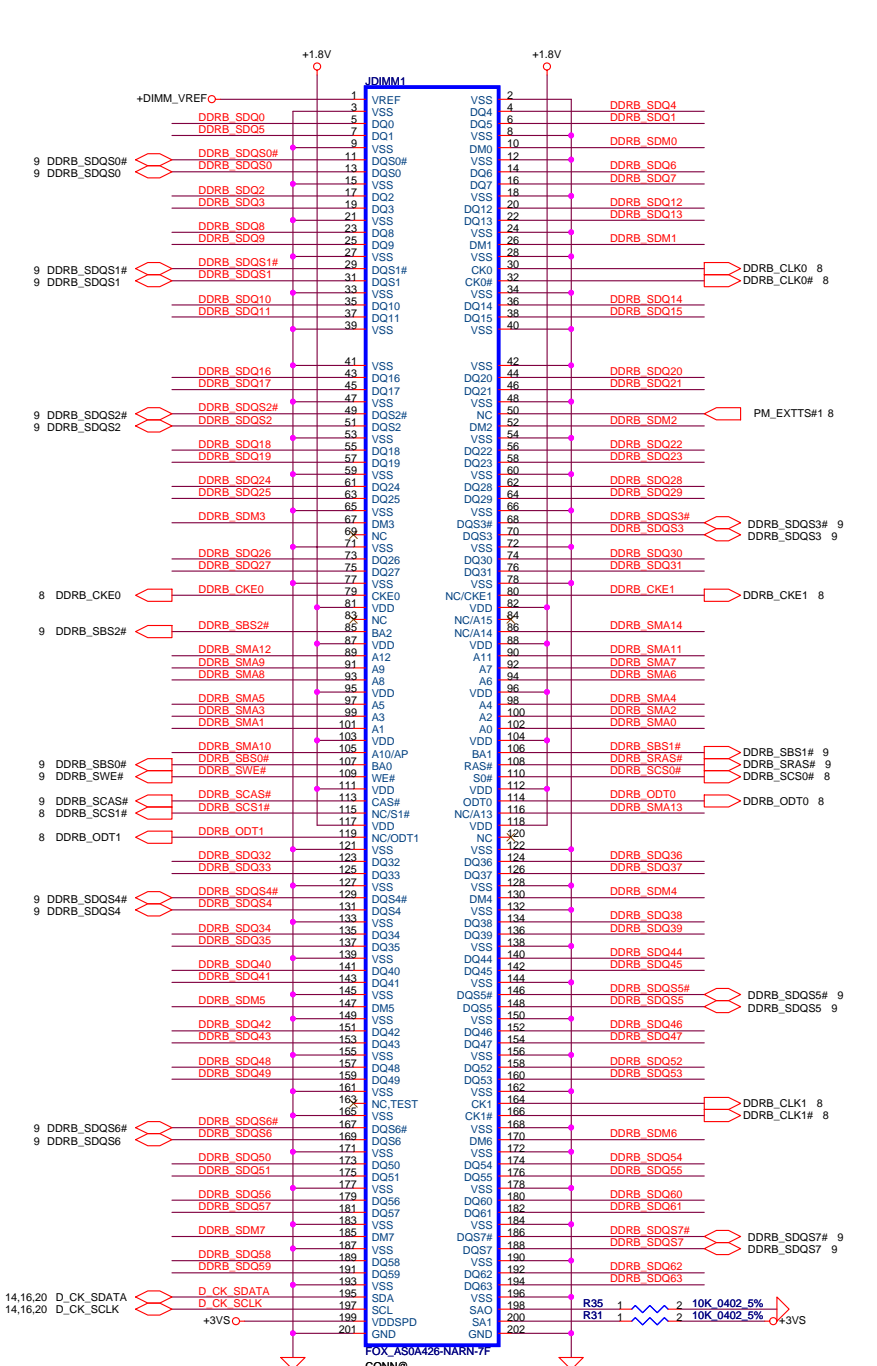
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DIMM0 REV H:5.2mm (BOT)

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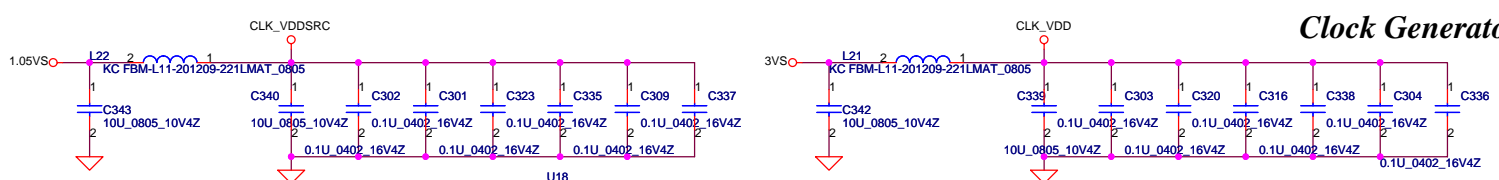
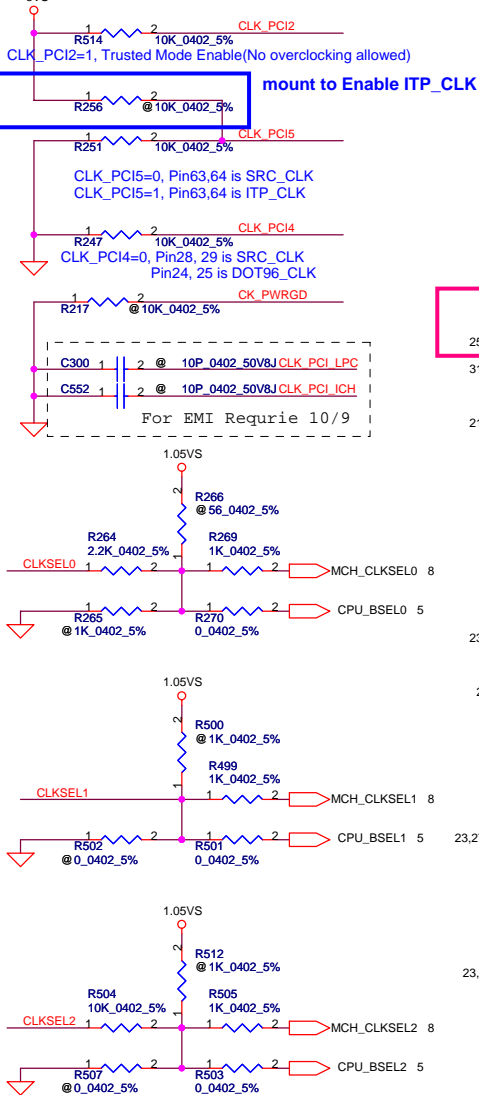
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

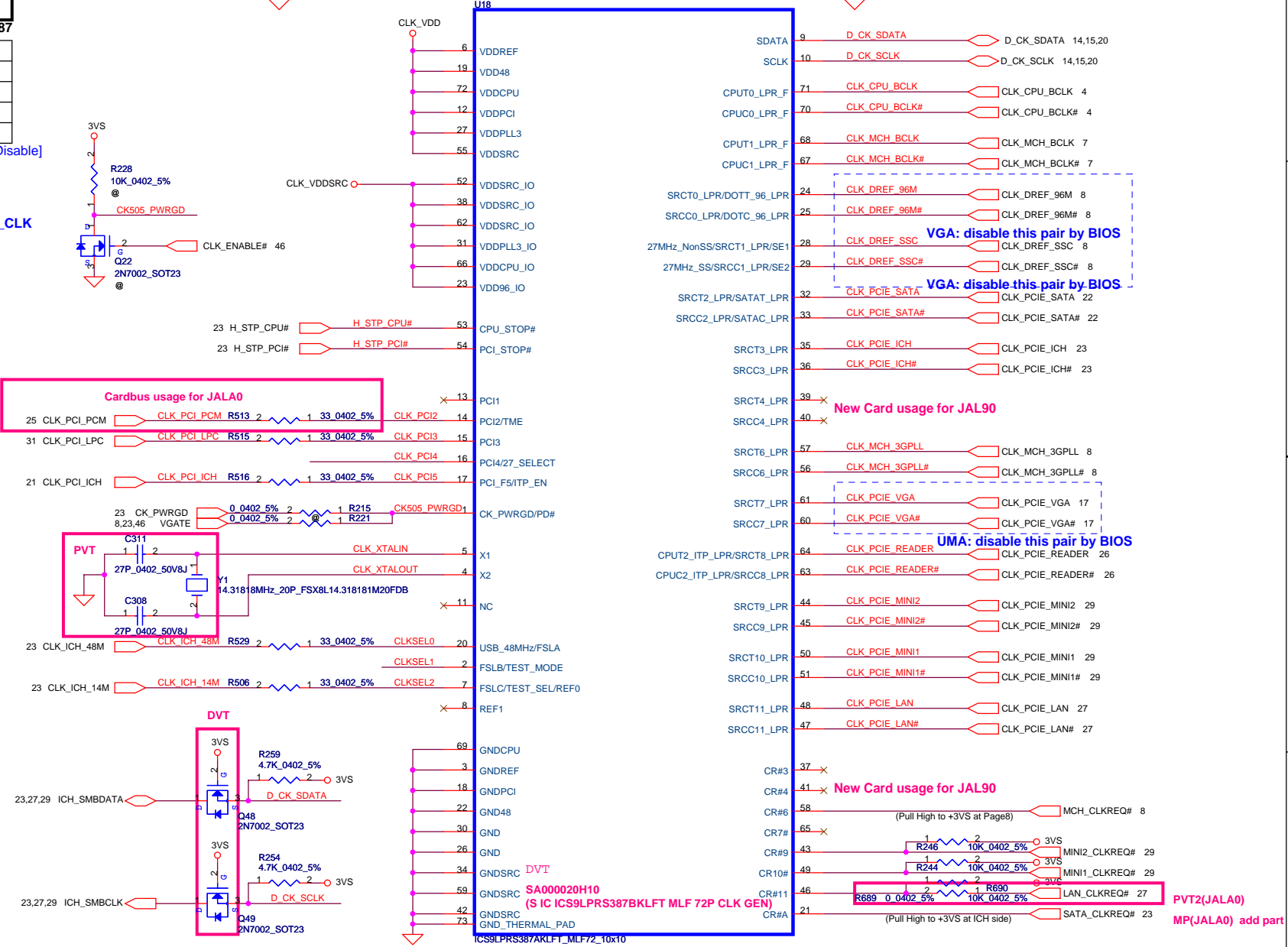
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PC EX0
CR#_6(MCH)	PCIEX6	PC EX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

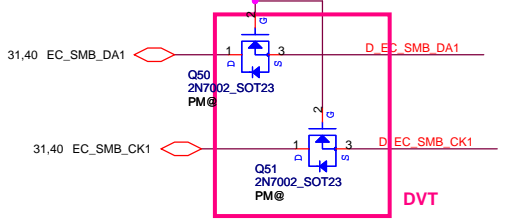
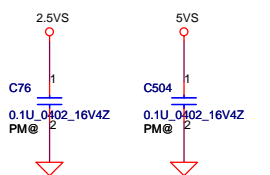
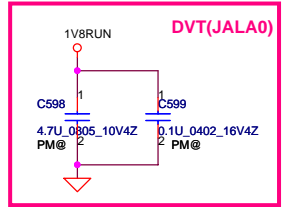
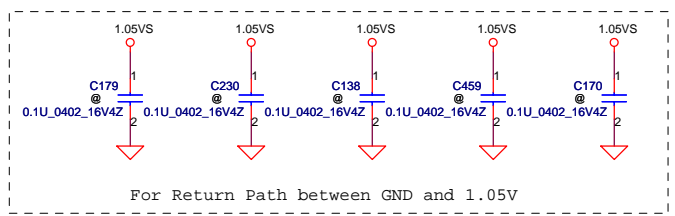
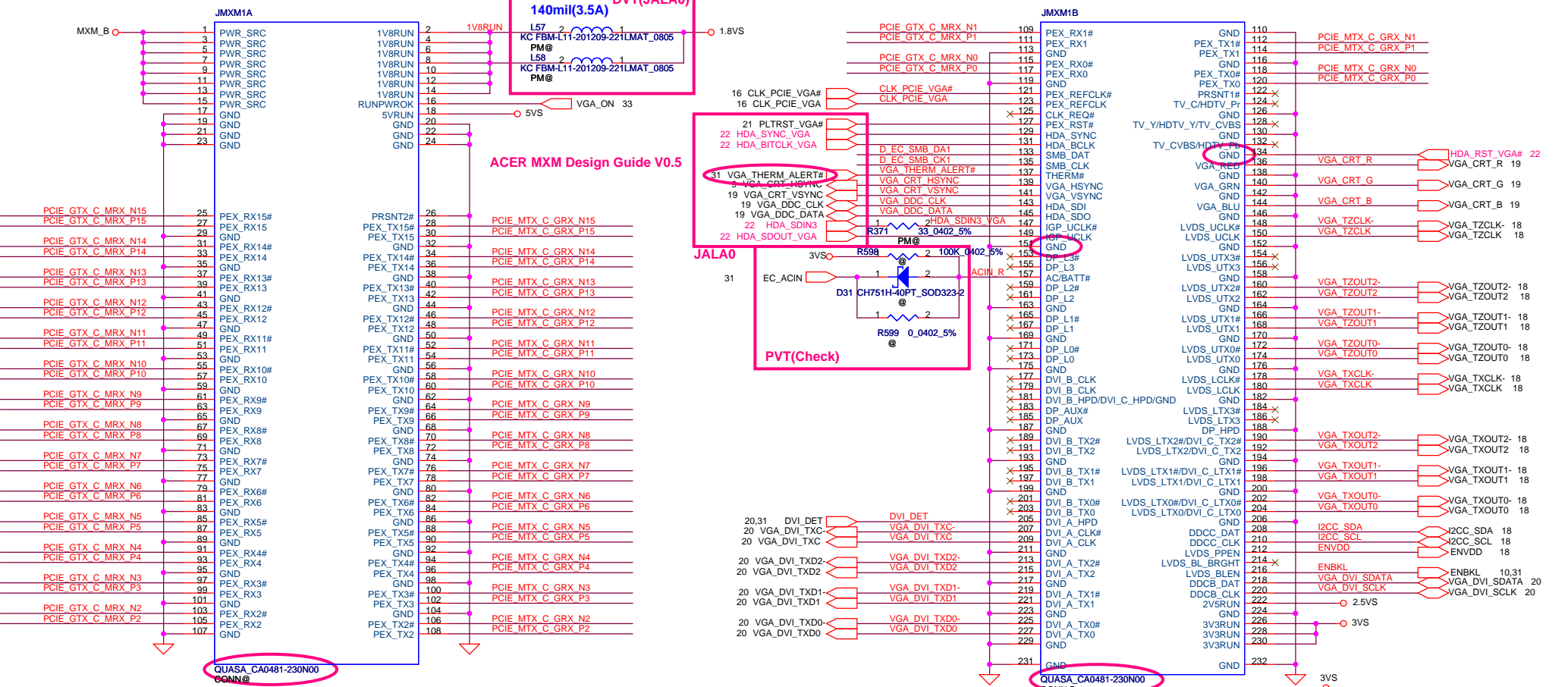


Clock Generator

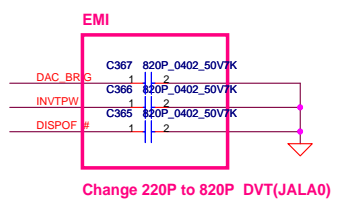
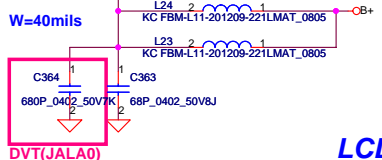
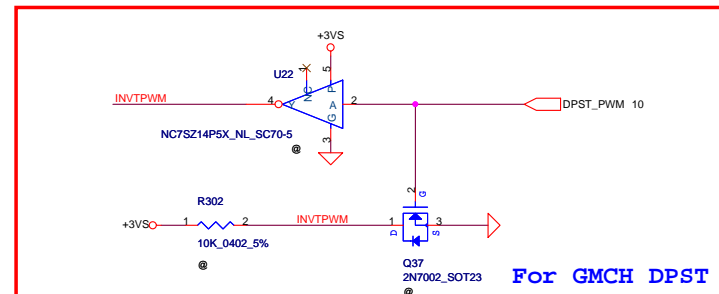
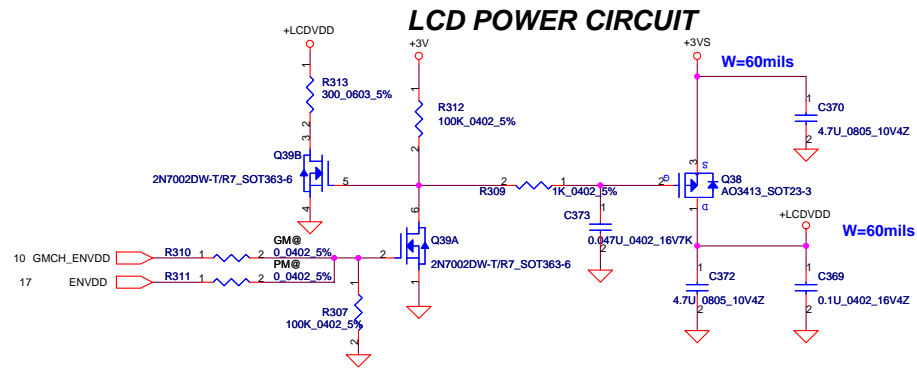


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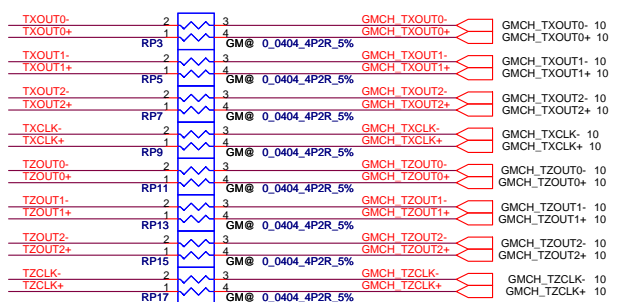
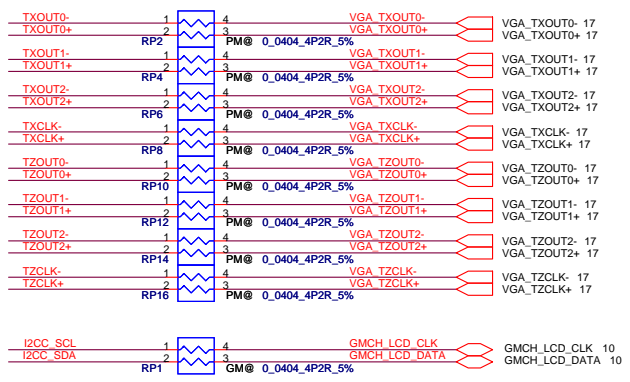
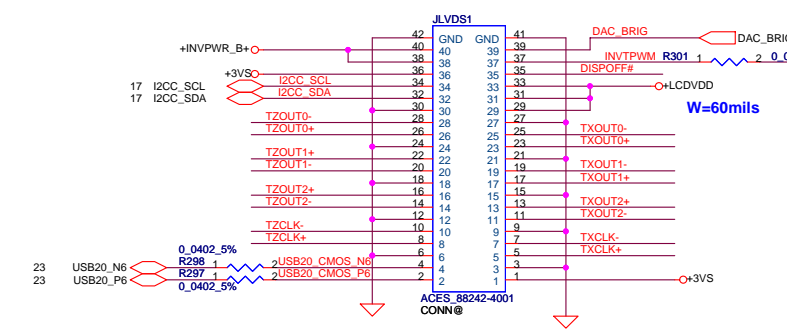
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- 10 PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX P[0..15]I
- 10 PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX NIO.15I
- 10 PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]I



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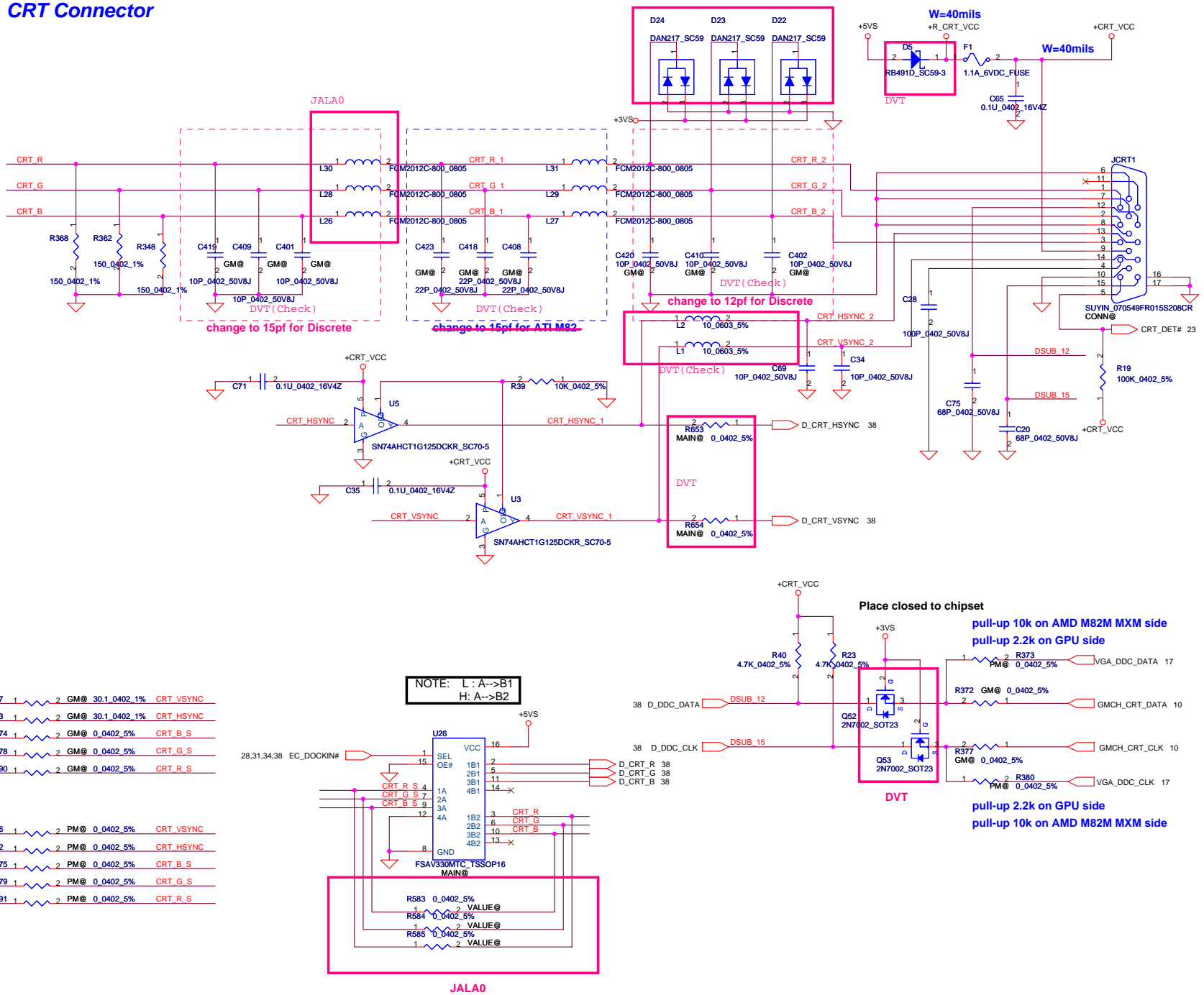


LCD/PANEL BD. Conn.



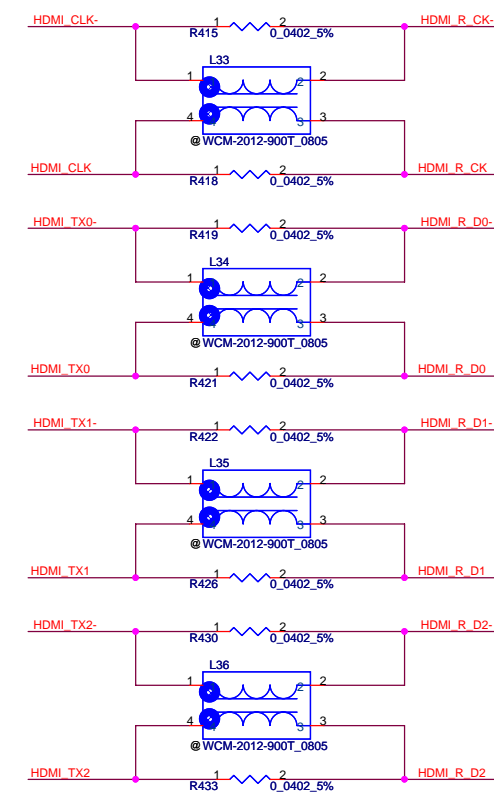
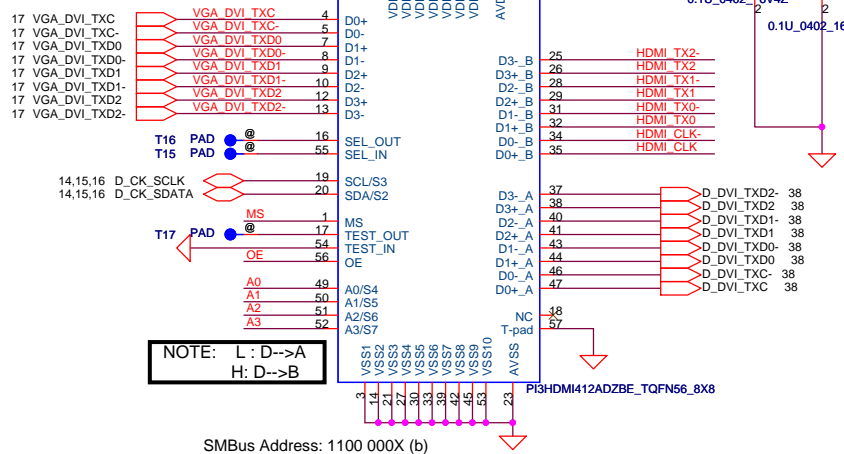
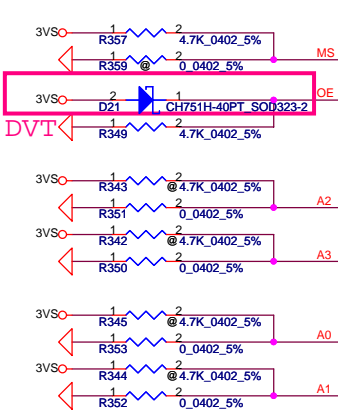
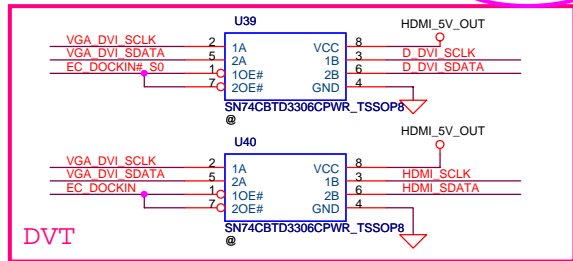
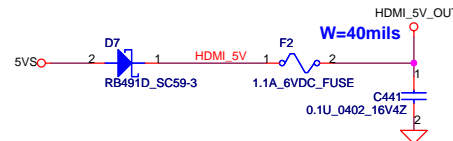
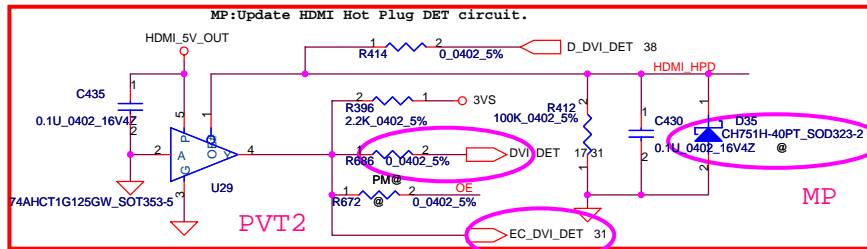
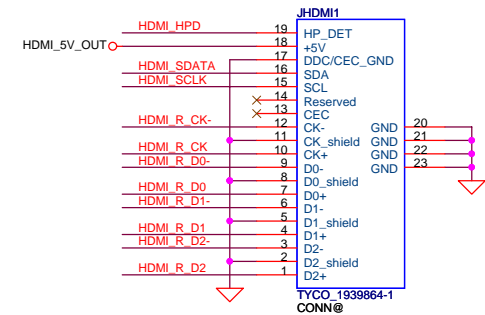
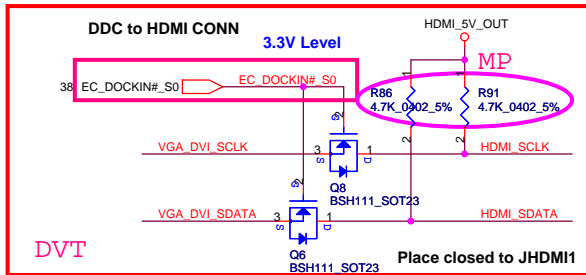
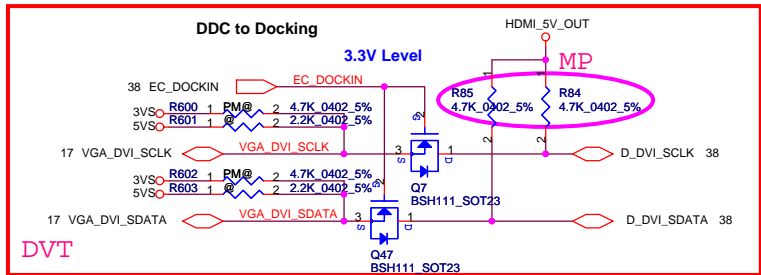
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CRT Connector

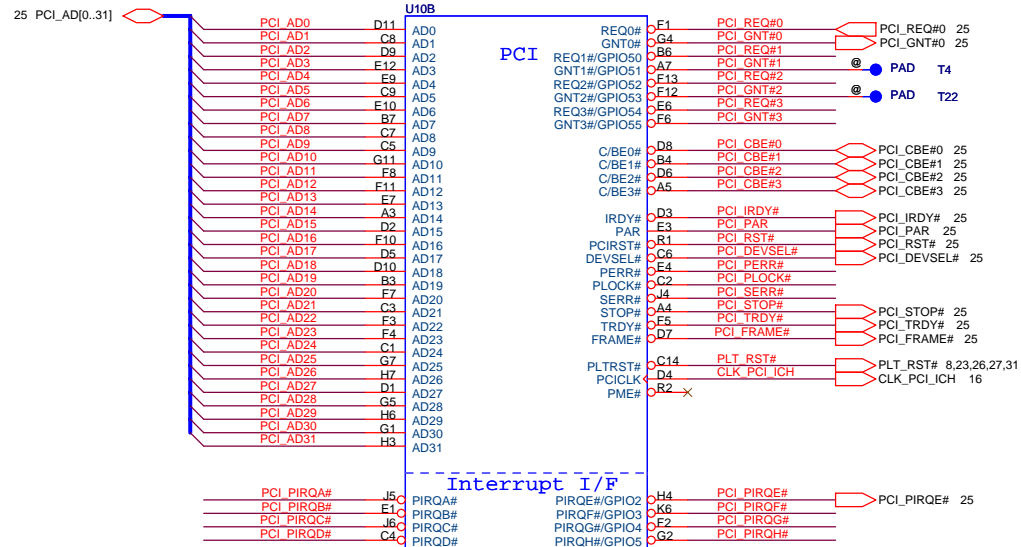
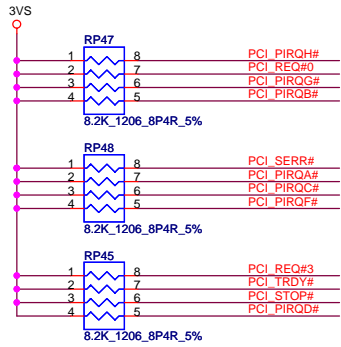
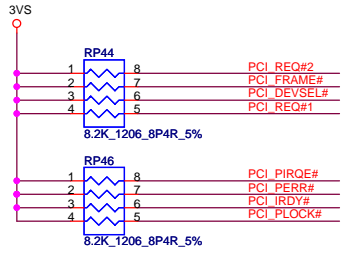


- 10 GMCH_CRT_VSYNC R67 1 2 GM@ 30.1_0402_1% CRT_VSYNC
- 10 GMCH_CRT_HSYNC R83 1 2 GM@ 30.1_0402_1% CRT_HSYNC
- 10 GMCH_CRT_B R374 1 2 GM@ 0_0402_5% CRT_B_S
- 10 GMCH_CRT_G R378 1 2 GM@ 0_0402_5% CRT_G_S
- 10 GMCH_CRT_R R390 1 2 GM@ 0_0402_5% CRT_R_S
- 17 VGA_CRT_VSYNC R66 1 2 PM@ 0_0402_5% CRT_VSYNC
- 17 VGA_CRT_HSYNC R82 1 2 PM@ 0_0402_5% CRT_HSYNC
- 17 VGA_CRT_B R375 1 2 PM@ 0_0402_5% CRT_B_S
- 17 VGA_CRT_G R379 1 2 PM@ 0_0402_5% CRT_G_S
- 17 VGA_CRT_R R391 1 2 PM@ 0_0402_5% CRT_R_S

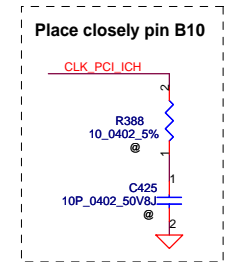
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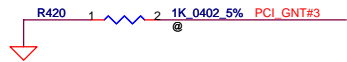
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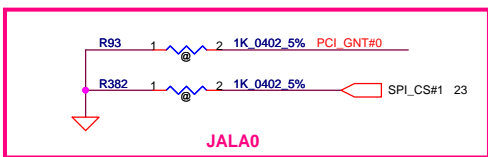
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



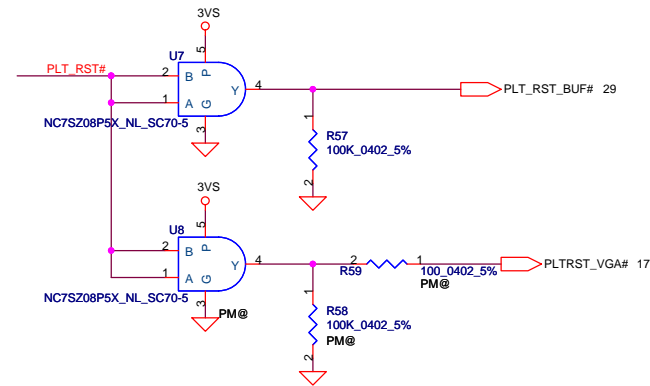
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



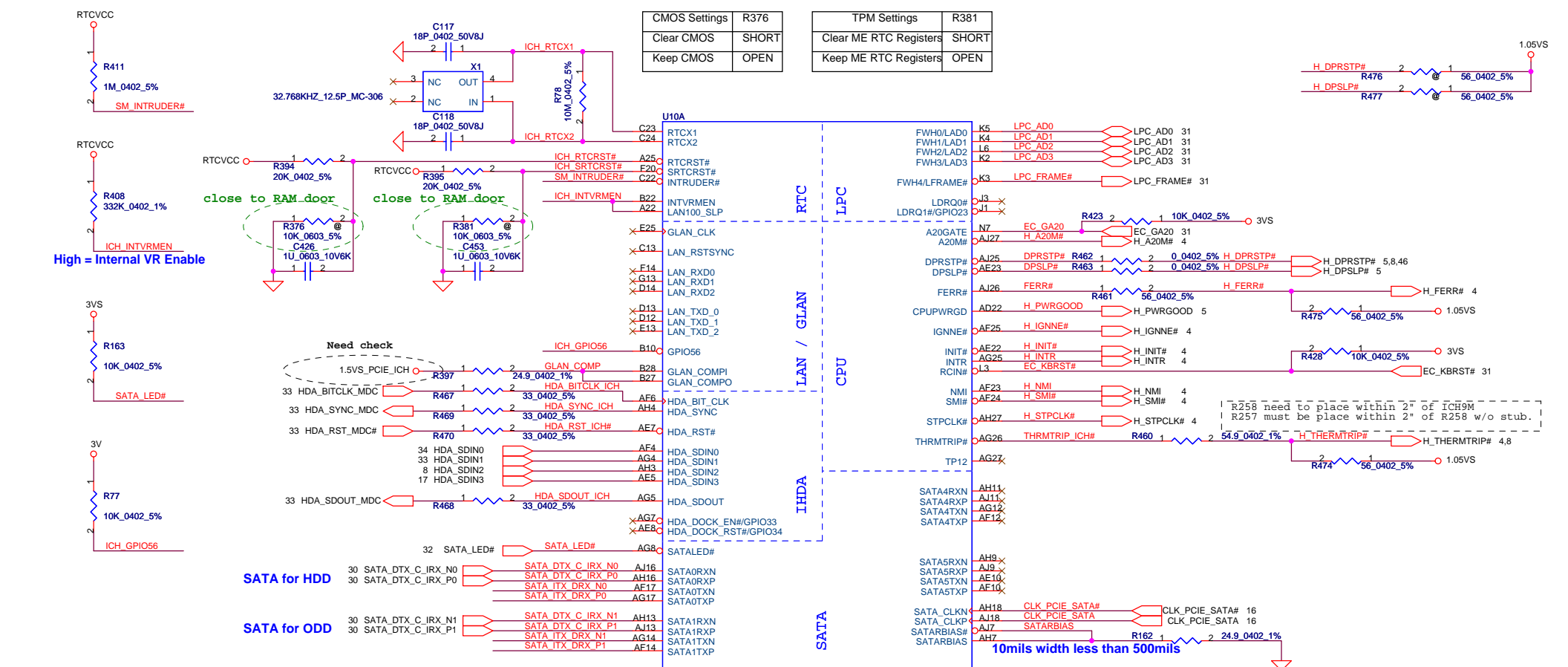
DVT ICH9-M: SA00002AN10
 (S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)
 PVT ICH9-M: SA00002JH00
 (S IC AF82801IBM QT09 A3 PBG 676P ICH9M)
 Pre-MP ICH9-M: SA00002JH70
 (S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)



For VGA/B

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CMOS Settings	R376	TPM Settings	R381
Clear CMOS	SHORT	Clear ME RTC Registers	SHORT
Keep CMOS	OPEN	Keep ME RTC Registers	OPEN



SATA for HDD

SATA for ODD

HDA for AUDIO

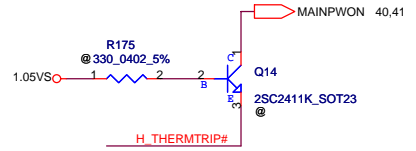
HDA for GMCH

HDA for VGA

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

Flash Descriptor Security Override Strap
 GPIO33 Low= Descriptor Security override
 High= Default* (Internal pull-up)

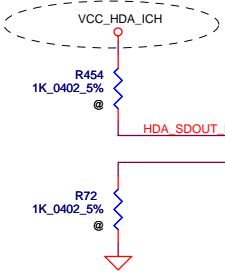
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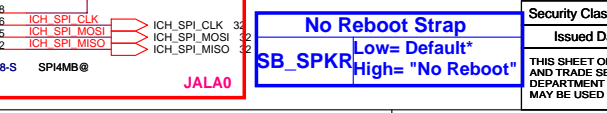
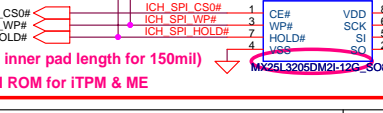
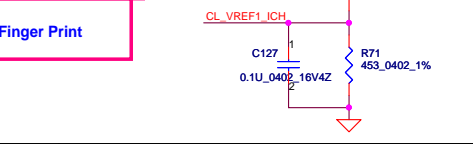
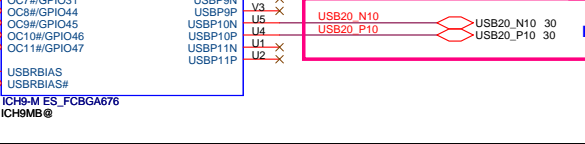
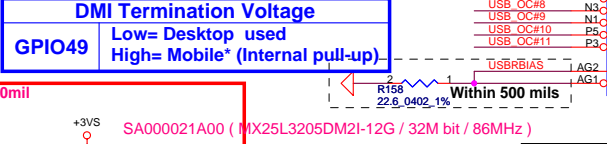
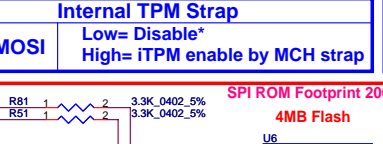
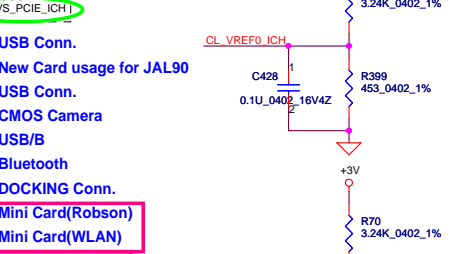
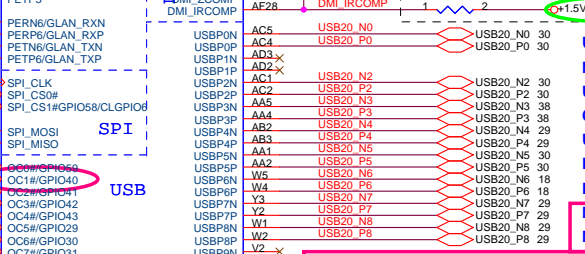
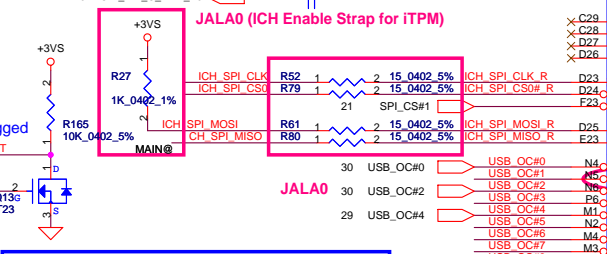
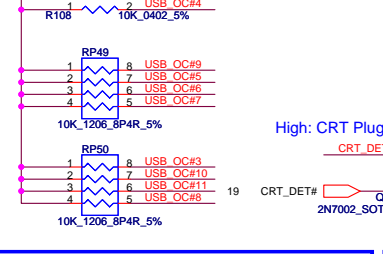
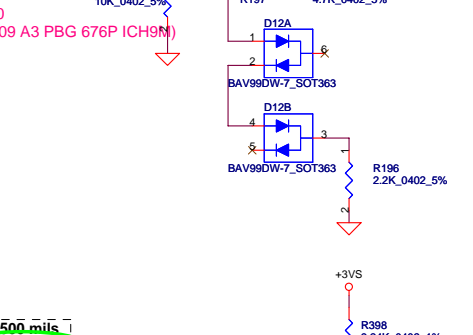
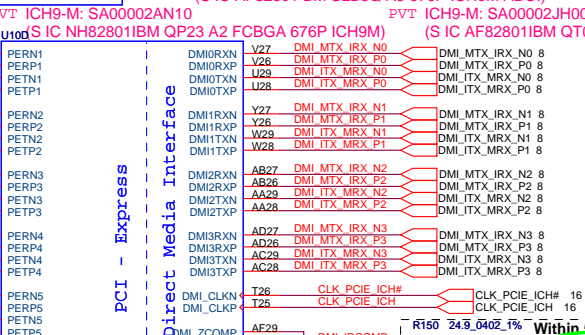
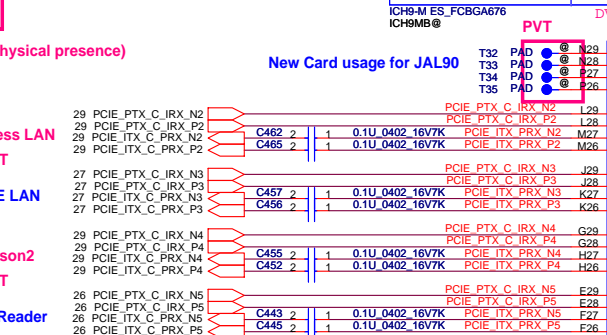
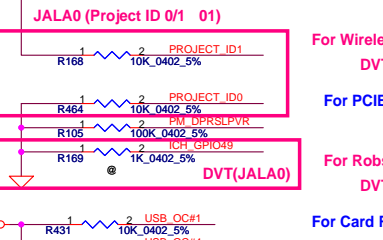
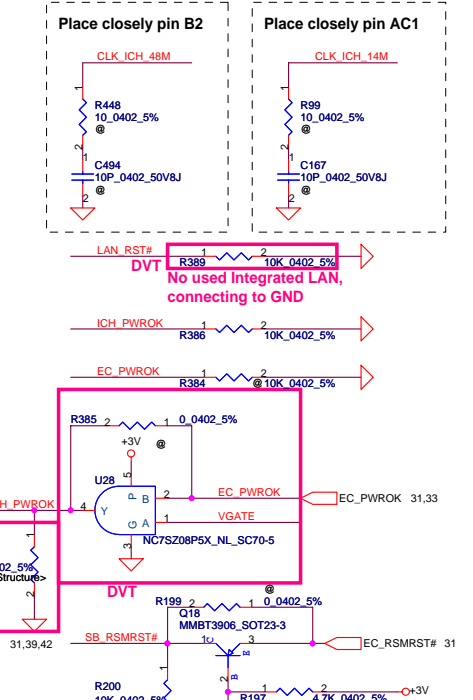
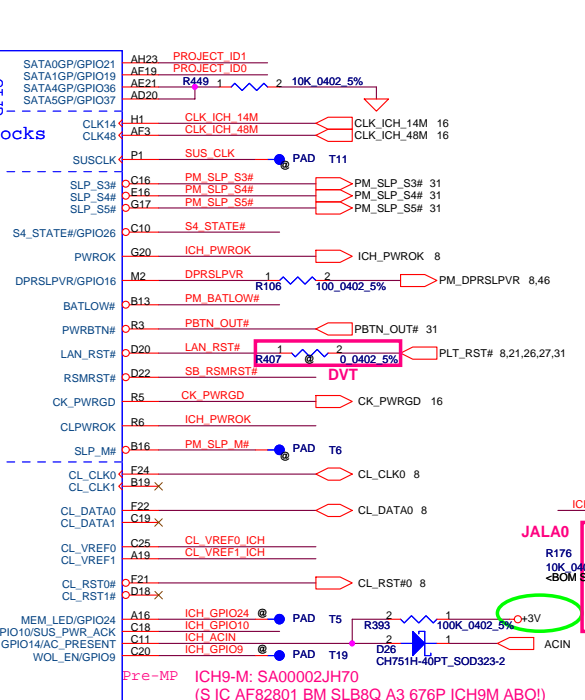
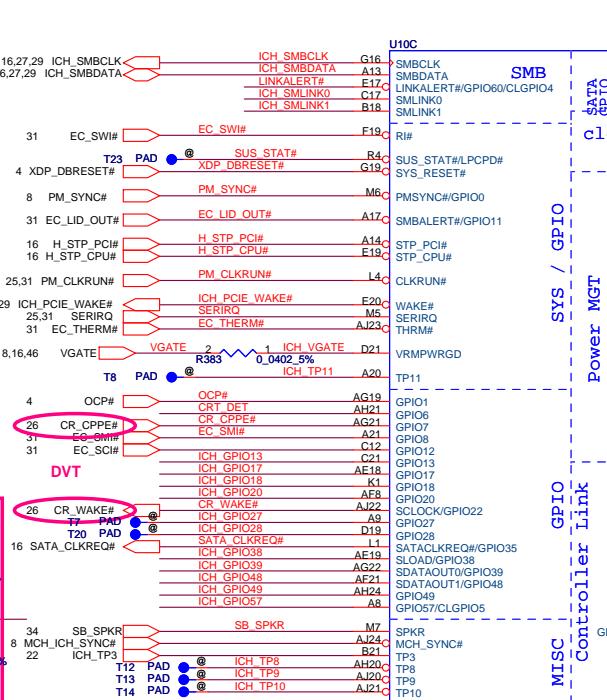
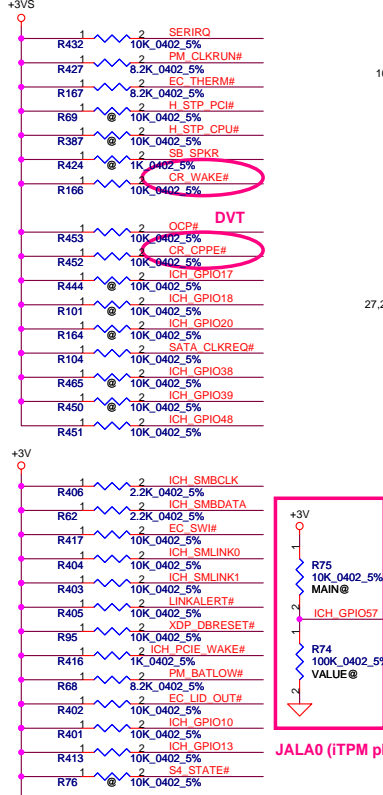


DVT ICH9-M: SA00002AN10 (S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)
 PVT ICH9-M: SA00002JH00 (S IC AF82801IBM QT09 A3 PBG 676P ICH9M)
 Pre-MP ICH9-M: SA00002JH70 (S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)

R258 need to place within 2" of ICH9M
 R257 must be place within 2" of R258 w/o stub.

close ICH9

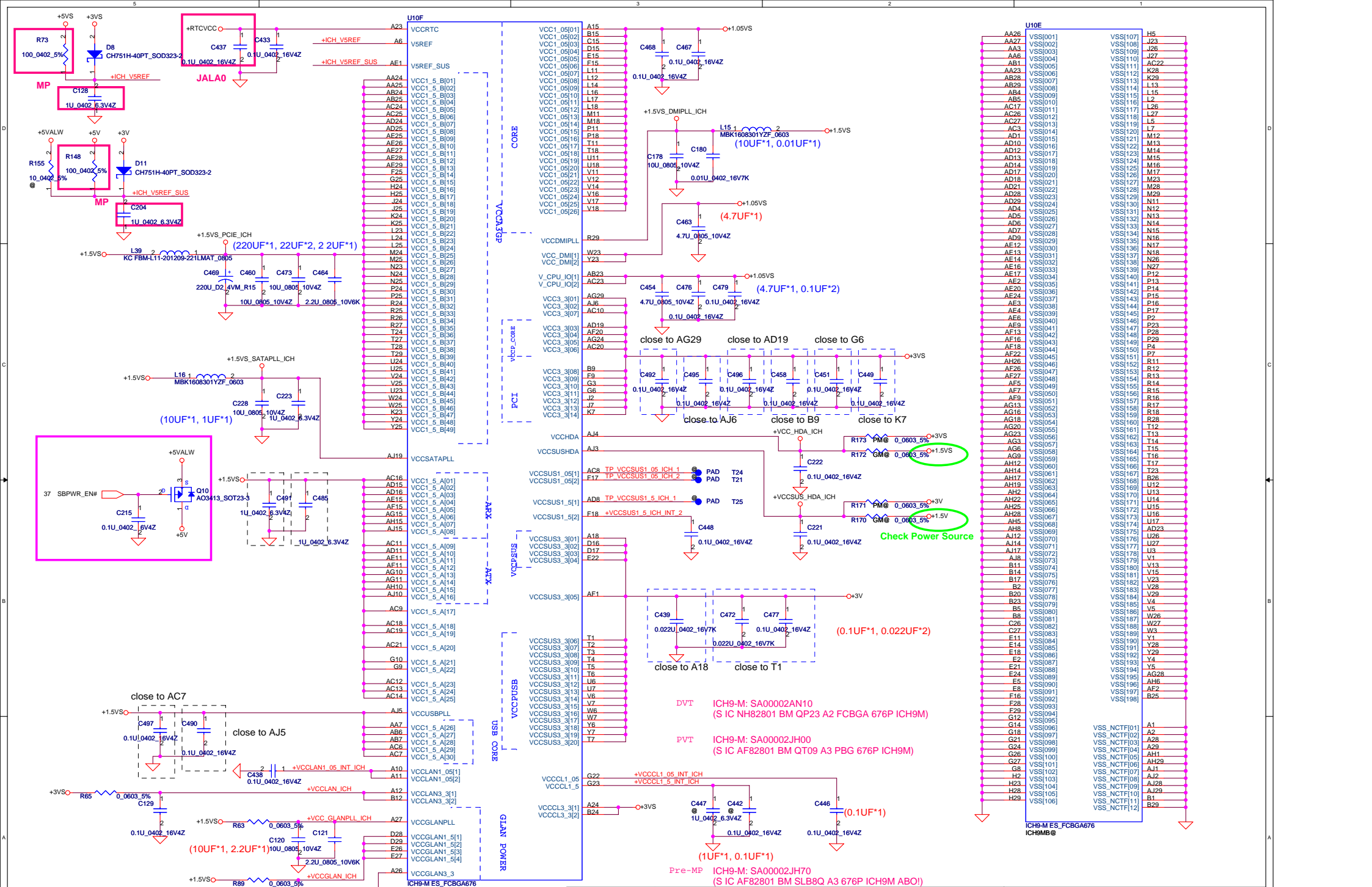




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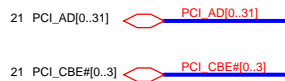
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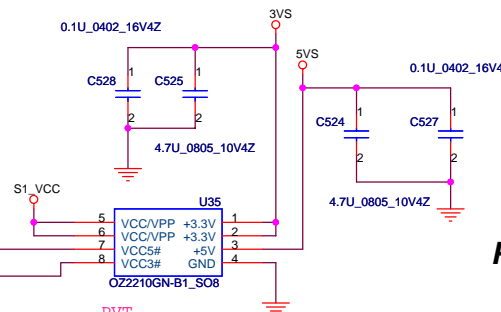
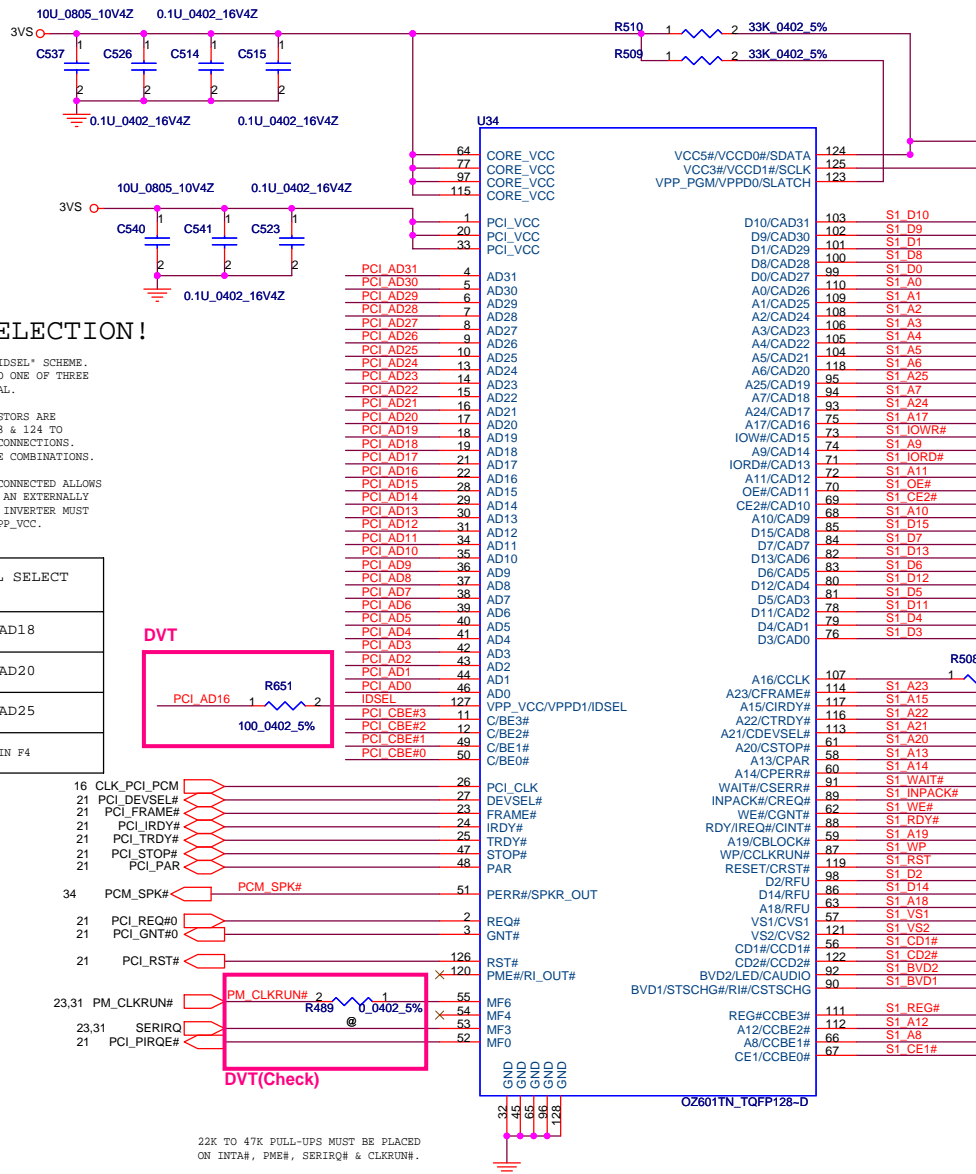


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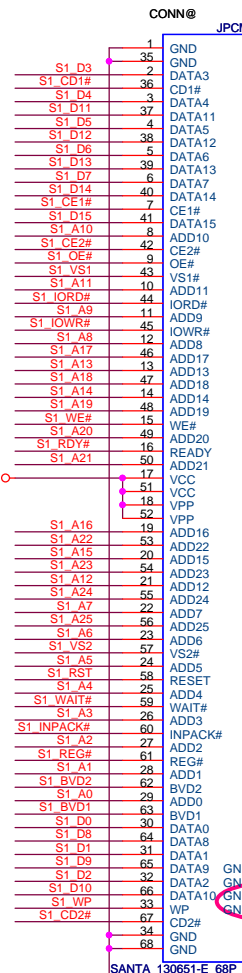
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IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

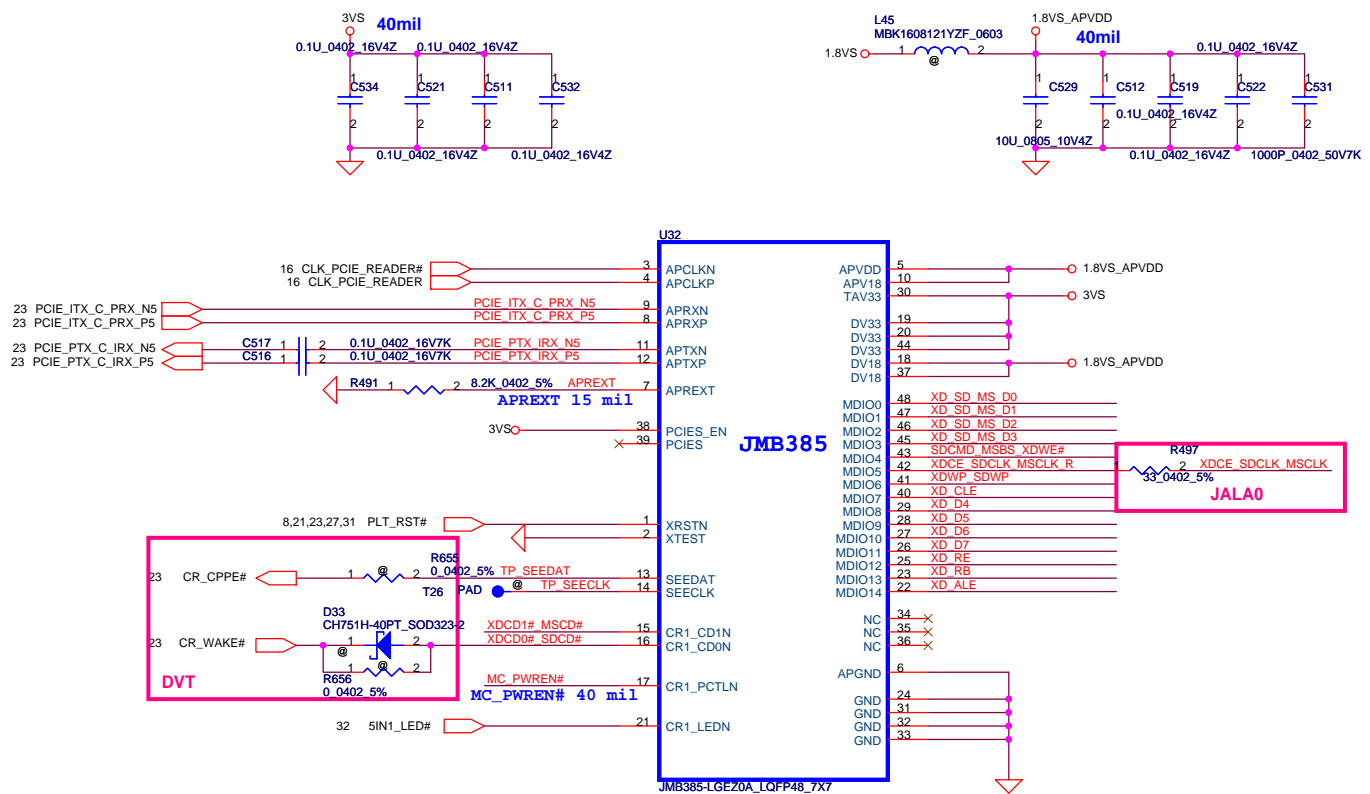


PCMCIA Socket



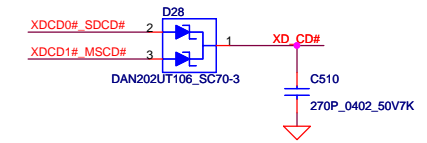
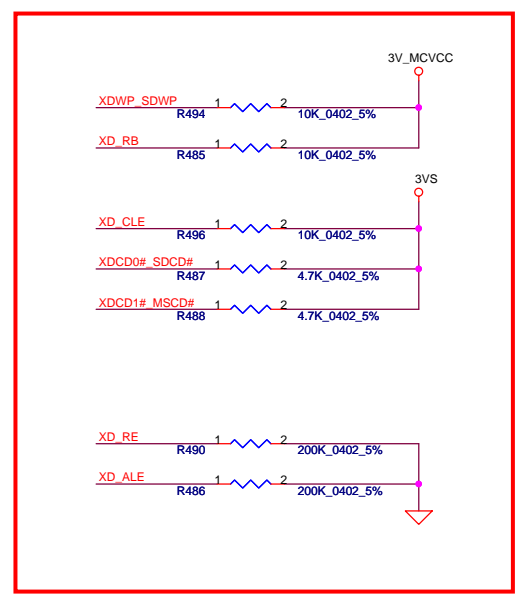
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DVT(JALA0)

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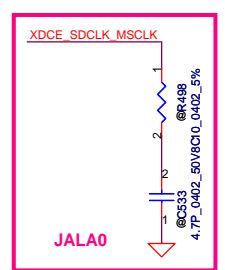
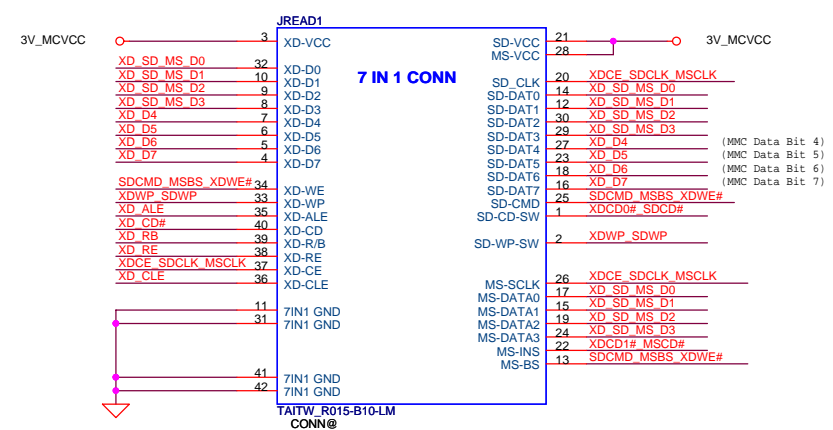
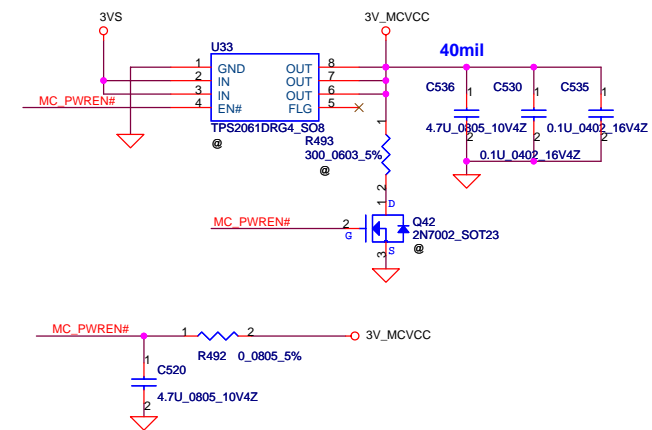
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MDIO PULL HIGH/LOW ?

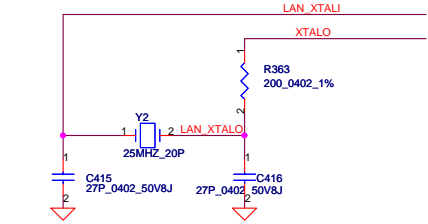
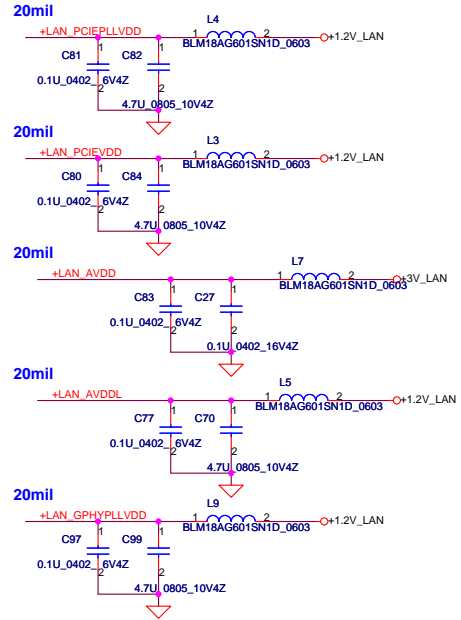
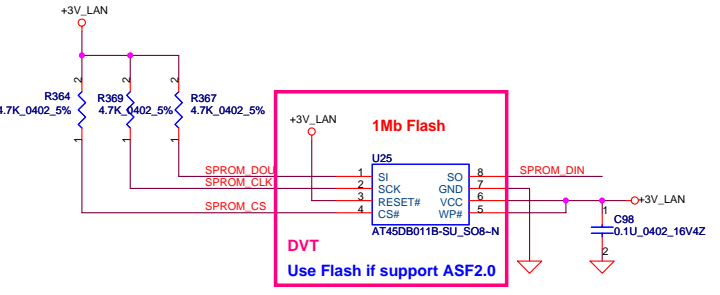
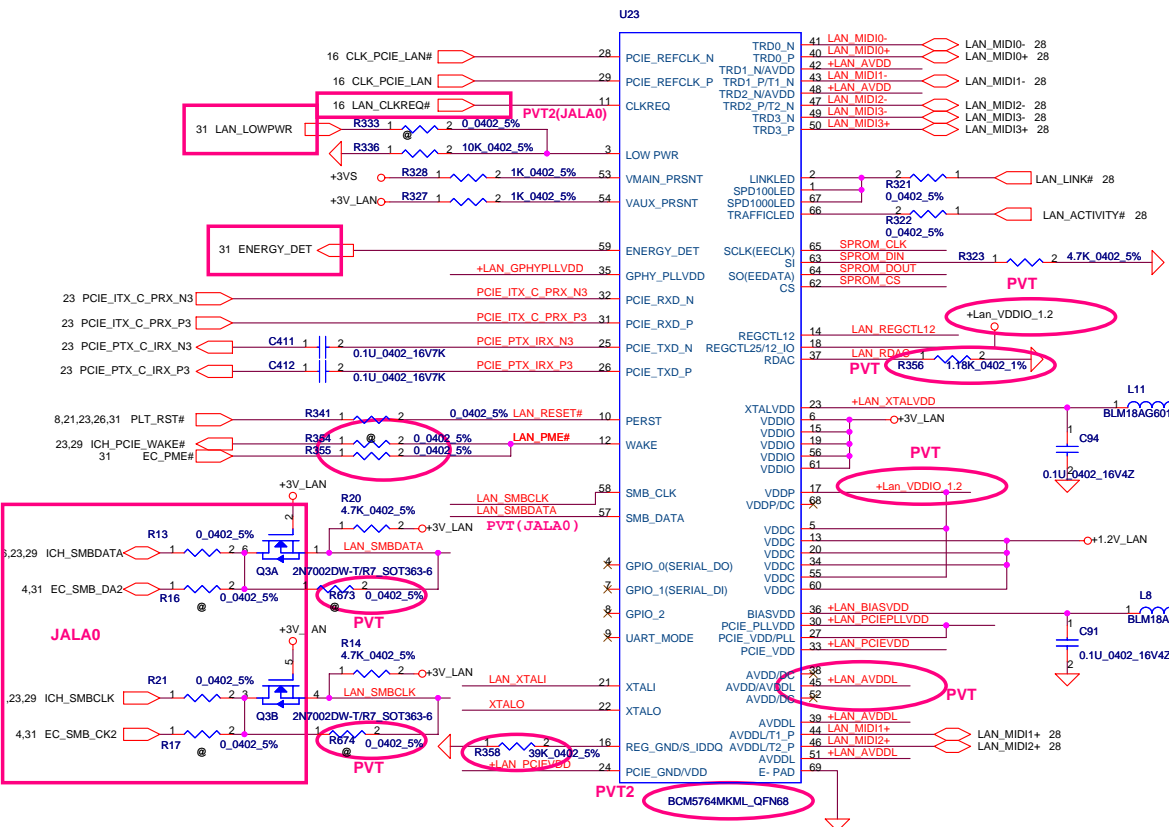
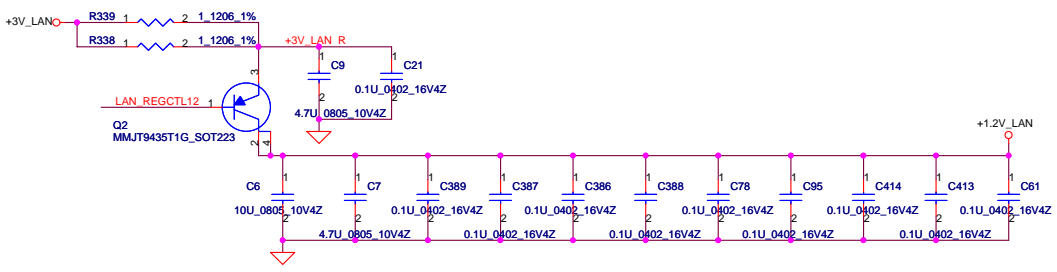
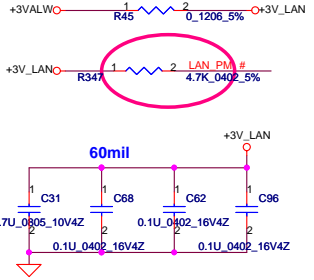


4 IN 1 Socket Push Type(New)

Memory Card Power Switch



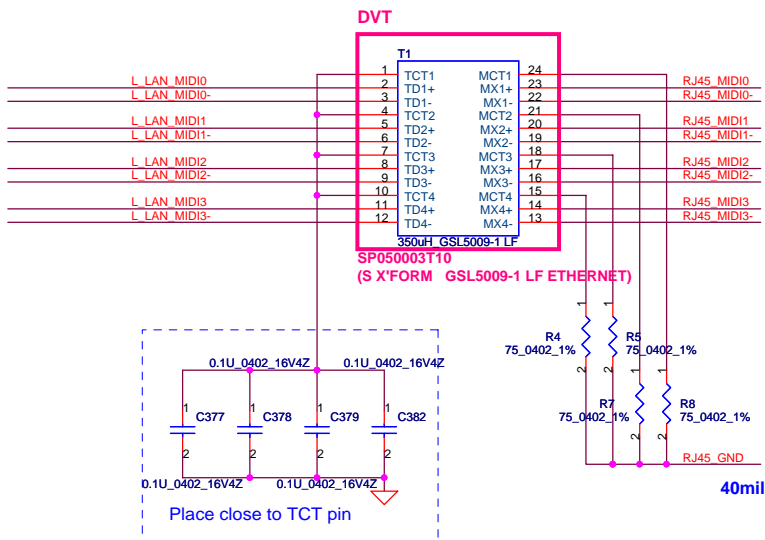
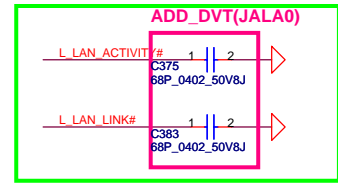
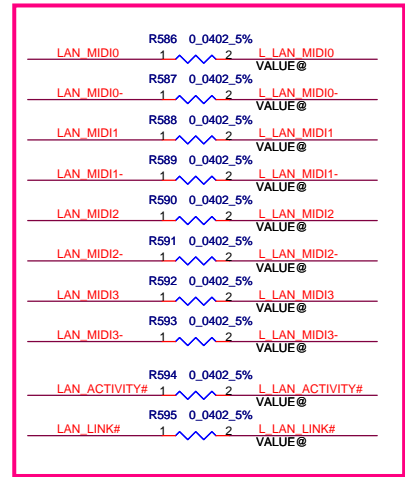
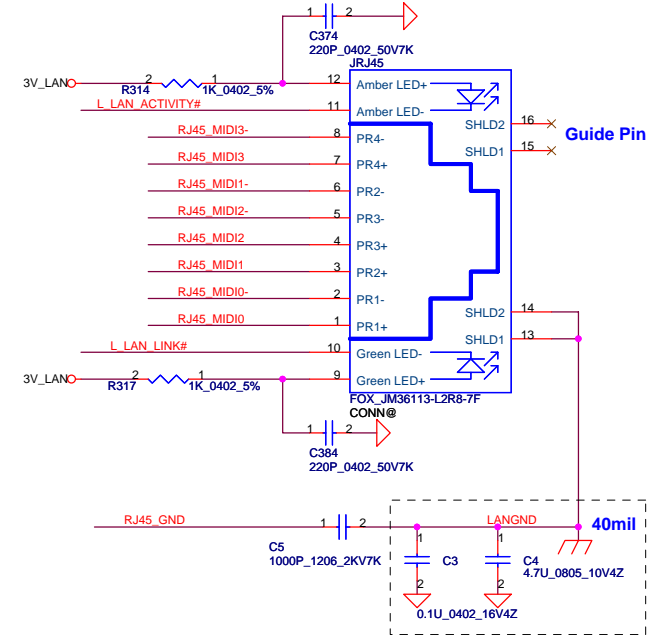
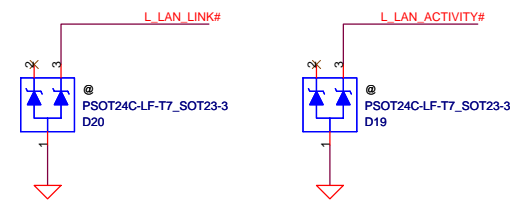
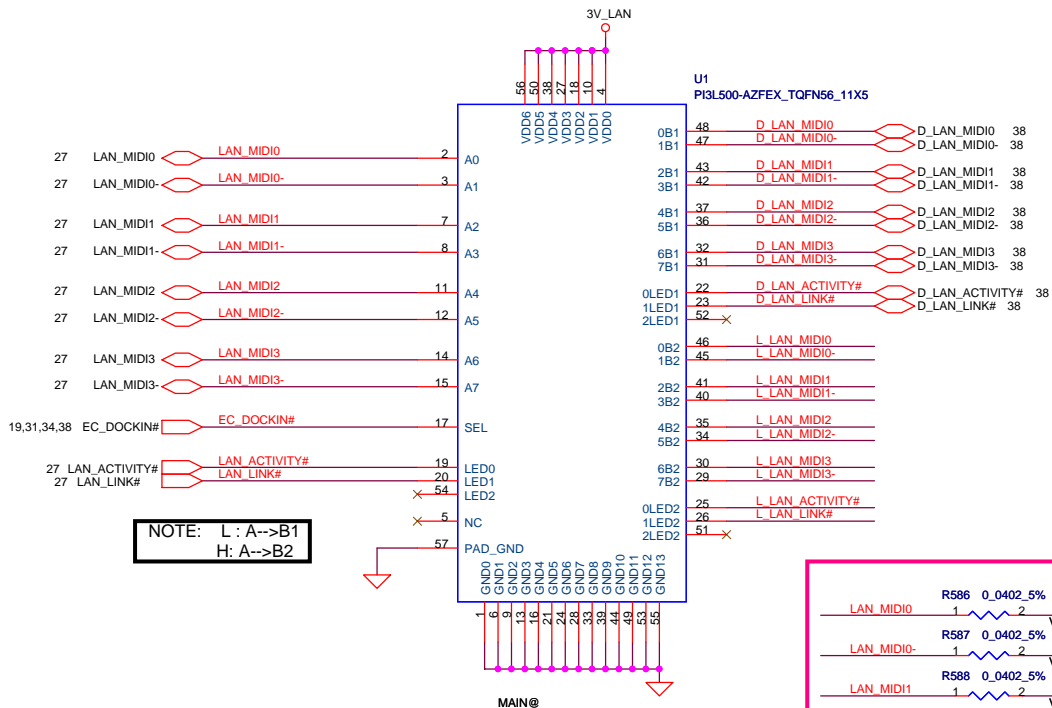
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DVT SA000025P00
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PVT SA000025P20
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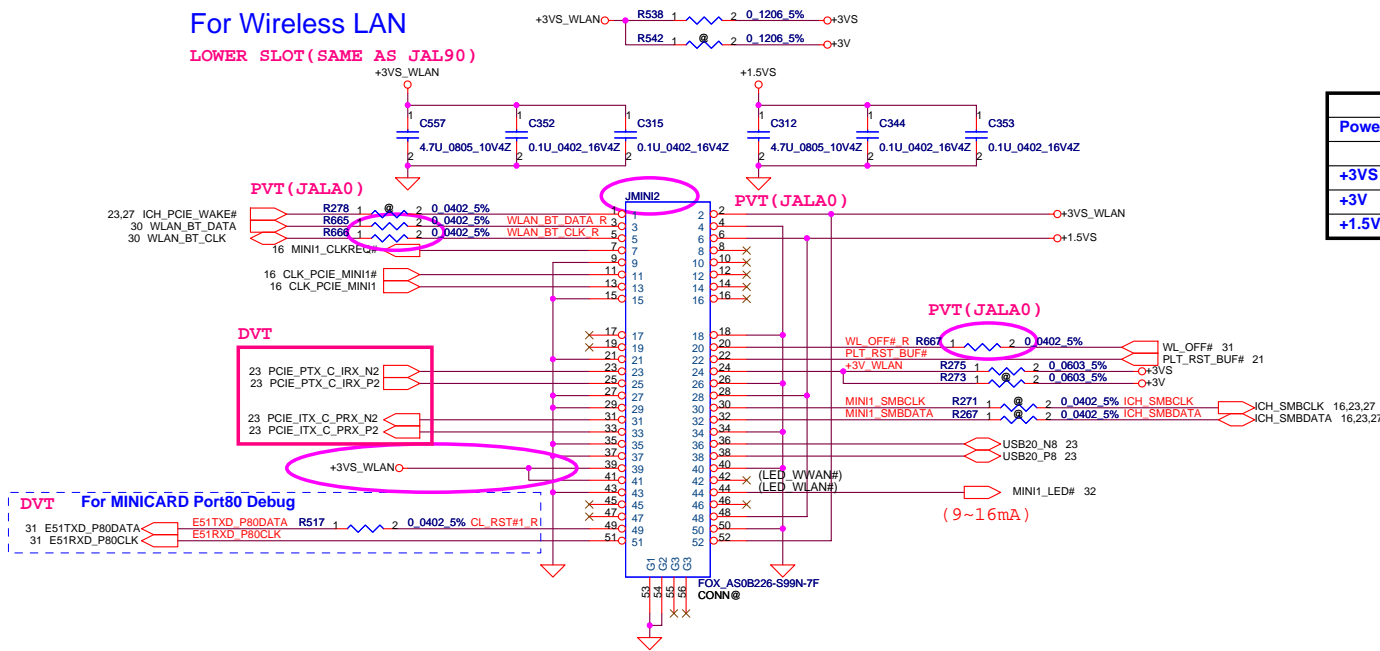
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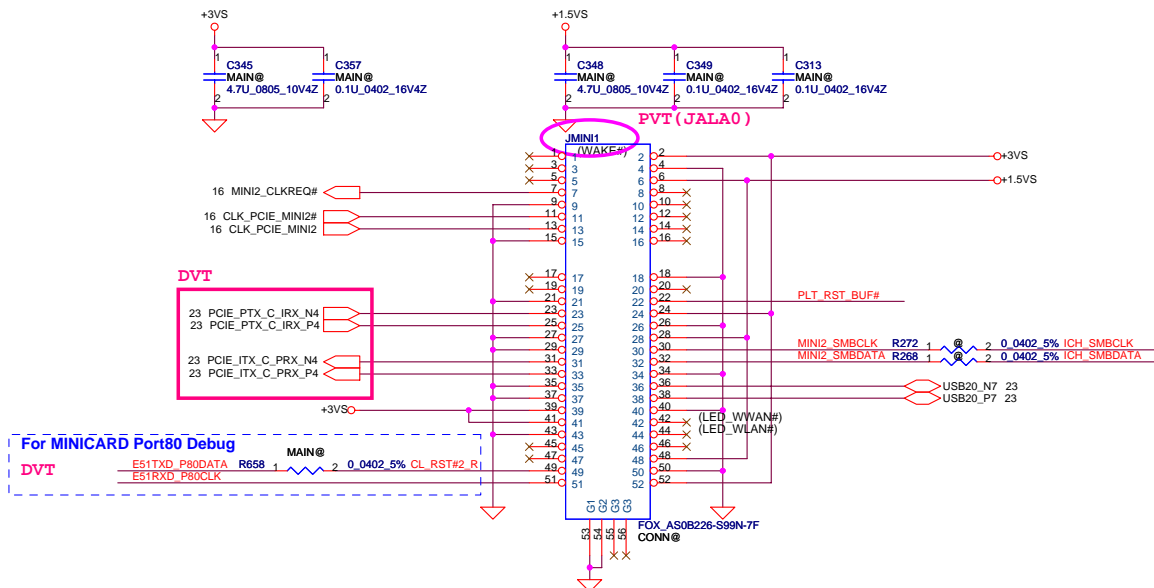
For Wireless LAN

LOWER SLOT(SAME AS JAL90)

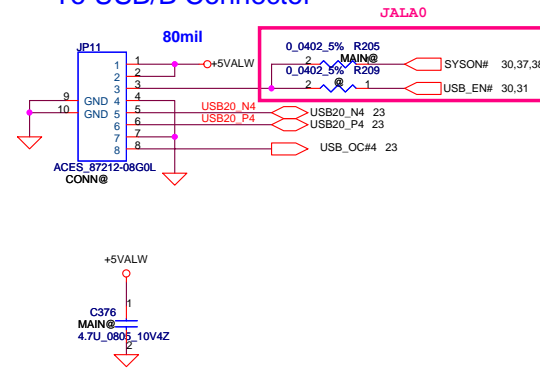


For Robson2

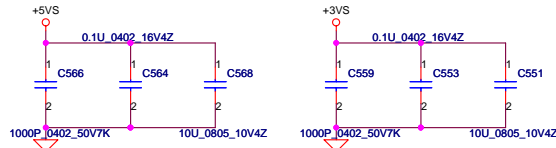
UPPER SLOT(SAME AS JAL90)



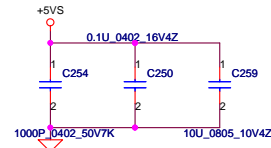
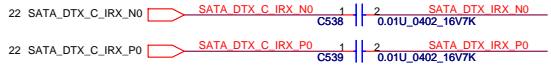
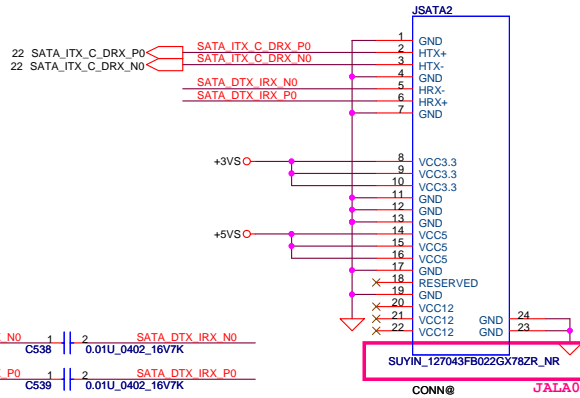
To USB/B Connector



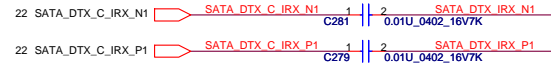
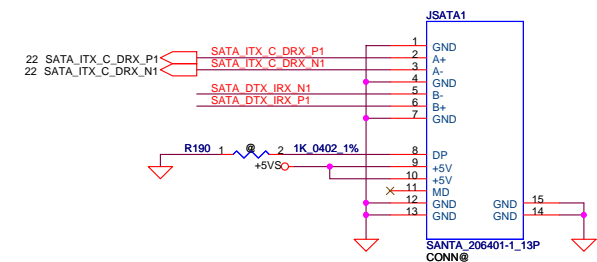
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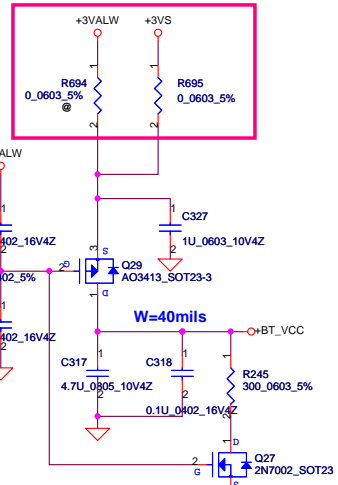
SATA HDD Conn.



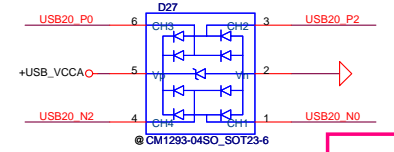
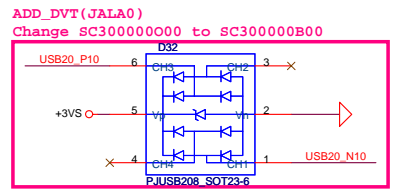
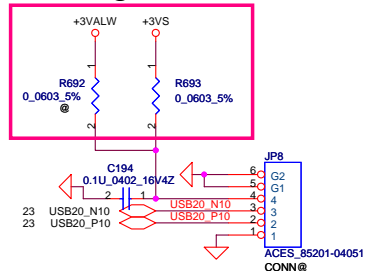
SATA ODD Conn.



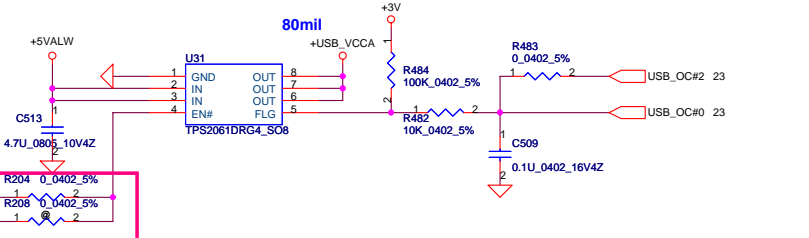
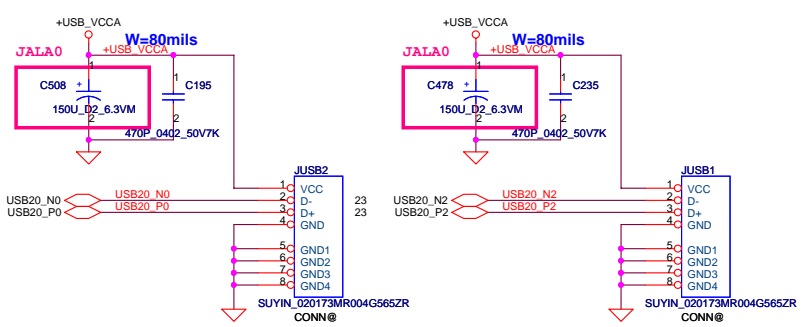
Bluetooth Conn.



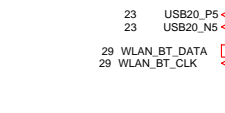
Finger Print Conn.



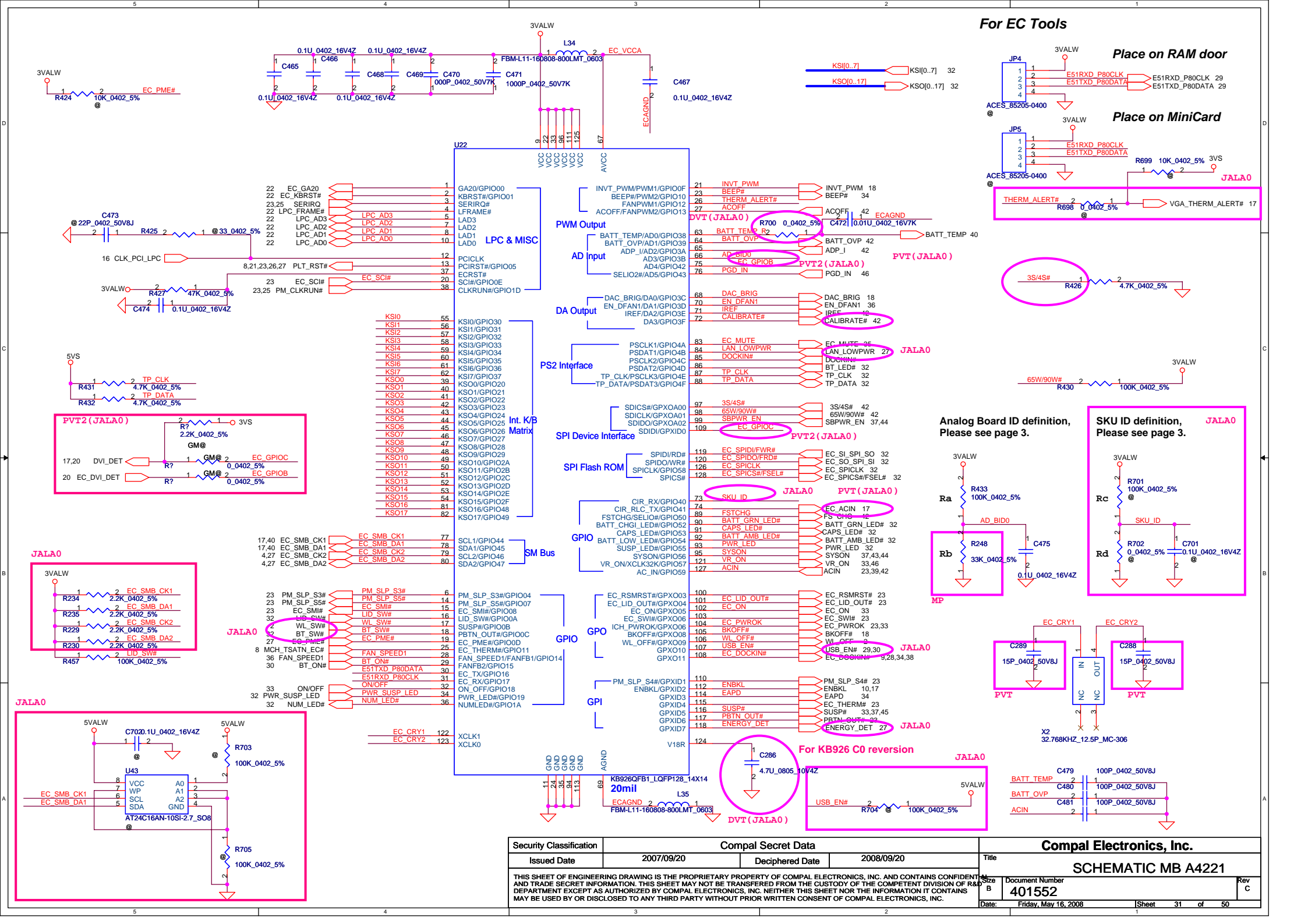
USB CONN. (Stack-up Type)



31

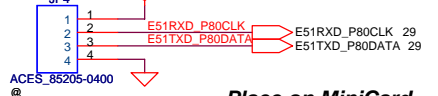


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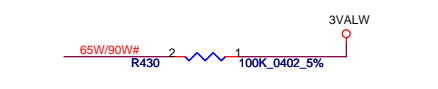
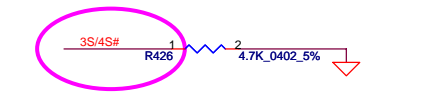
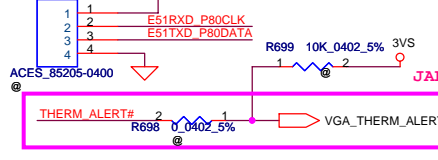


For EC Tools

Place on RAM door

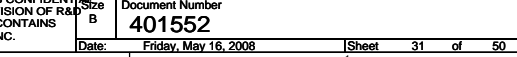
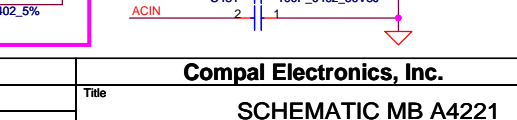
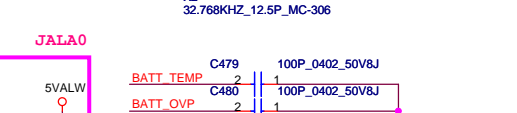
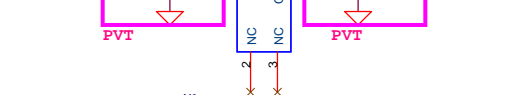
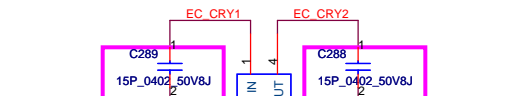
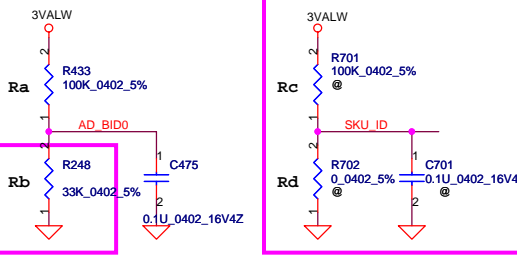


Place on MiniCard

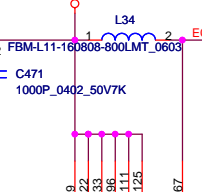


Analog Board ID definition, Please see page 3.

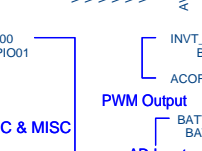
SKU ID definition, Please see page 3.



PWM Output



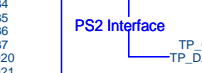
AD Input



DA Output



PS2 Interface



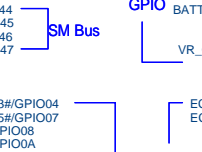
SPI Device Interface



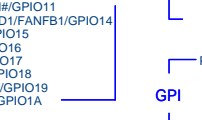
SPI Flash ROM



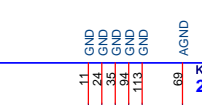
GPIO



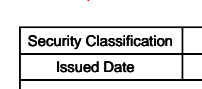
SMB Bus



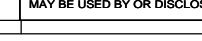
Int. K/B Matrix



LPC & MISC



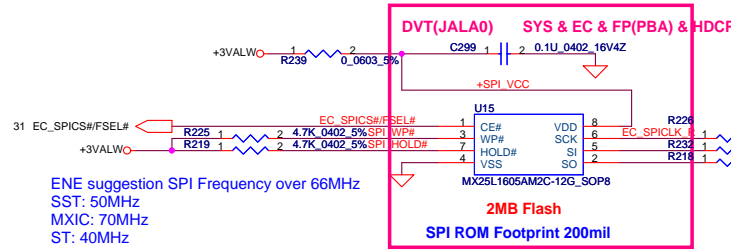
SM Bus



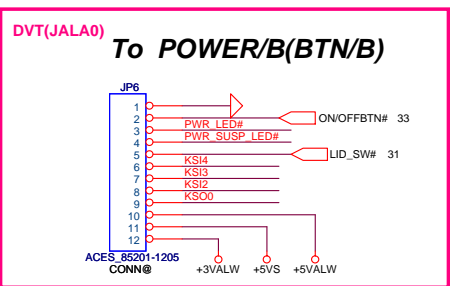
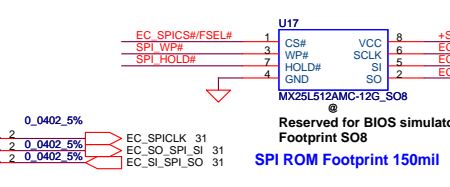
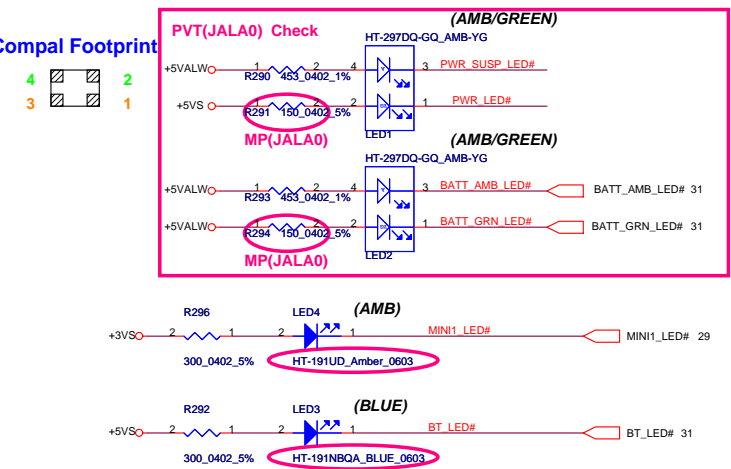
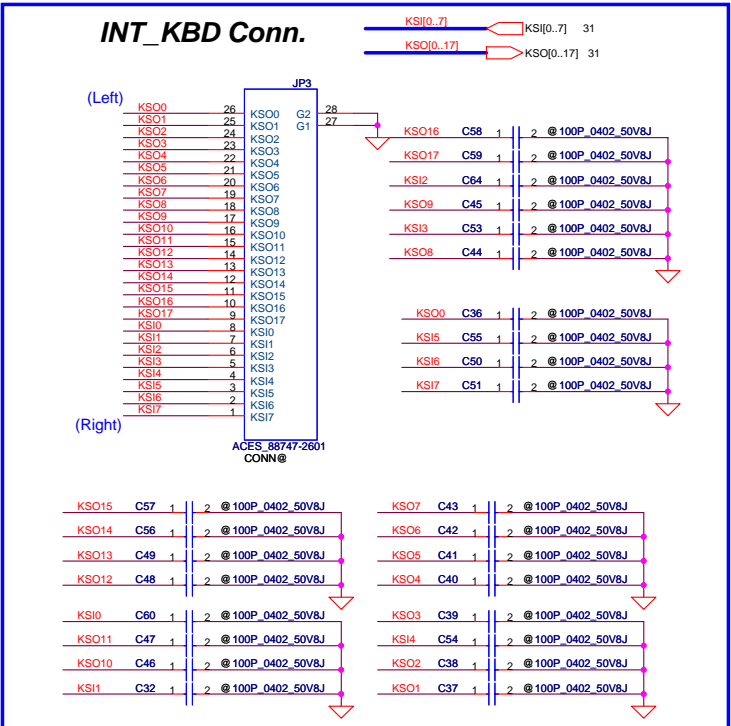
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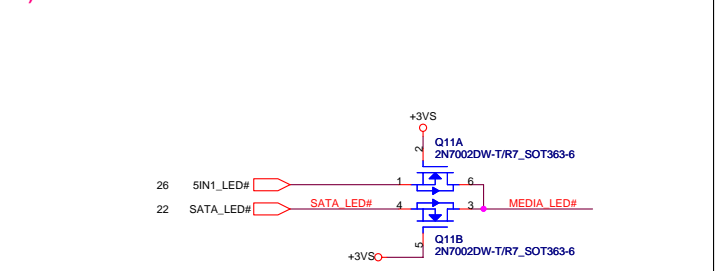
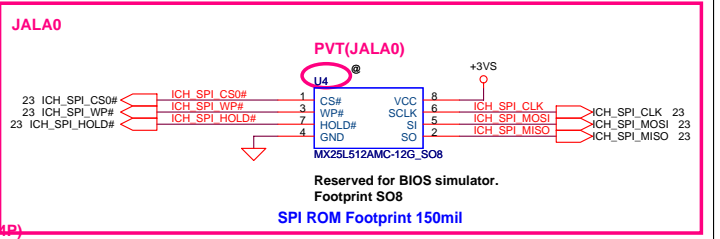
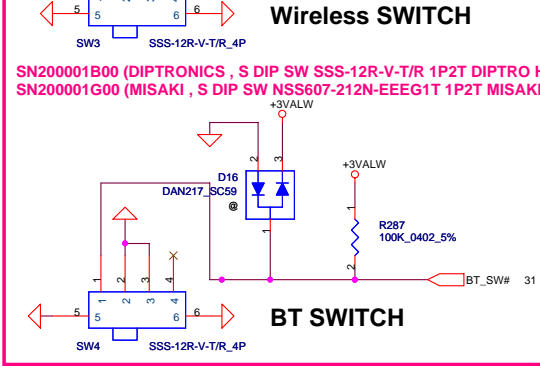
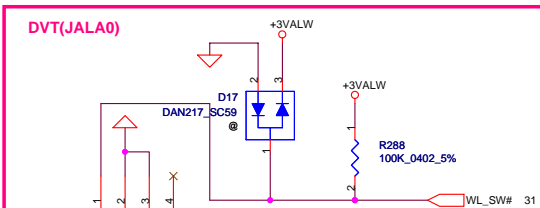
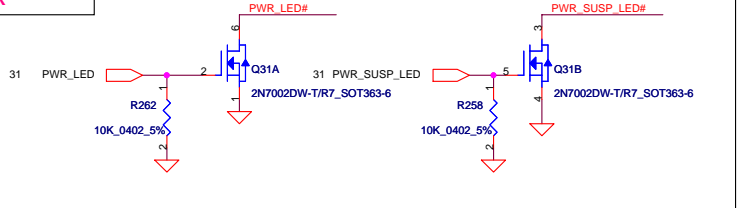
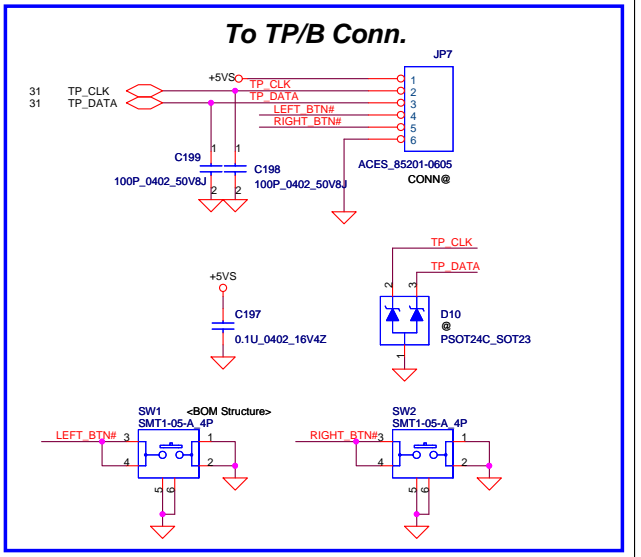
Compal Electronics, Inc.			
Document Number	401552		



ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz



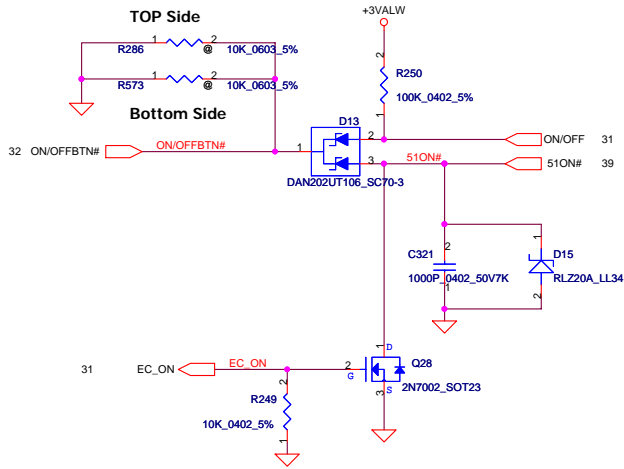
KSO0	
KSI1	PRESENTATION
KSI2	Program BTN#
KSI3	EMAIL BTN#
KSI4	IE BTN#
KSI5	E-KEY BTN#
KSI6	SYNC
KSI7	LOCK



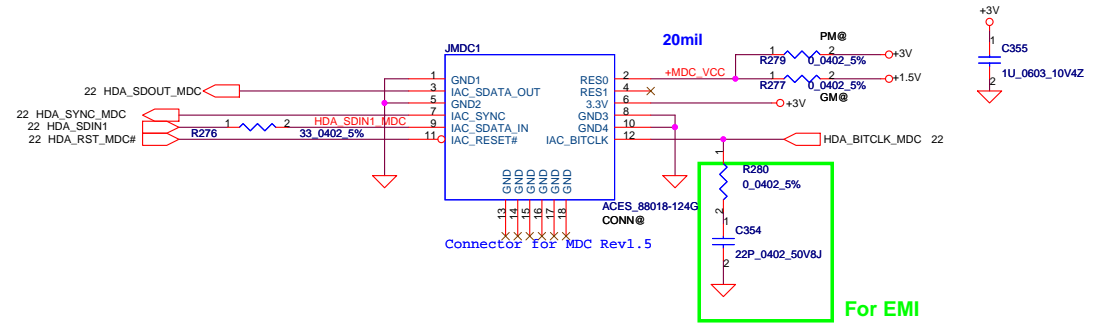
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Power Button

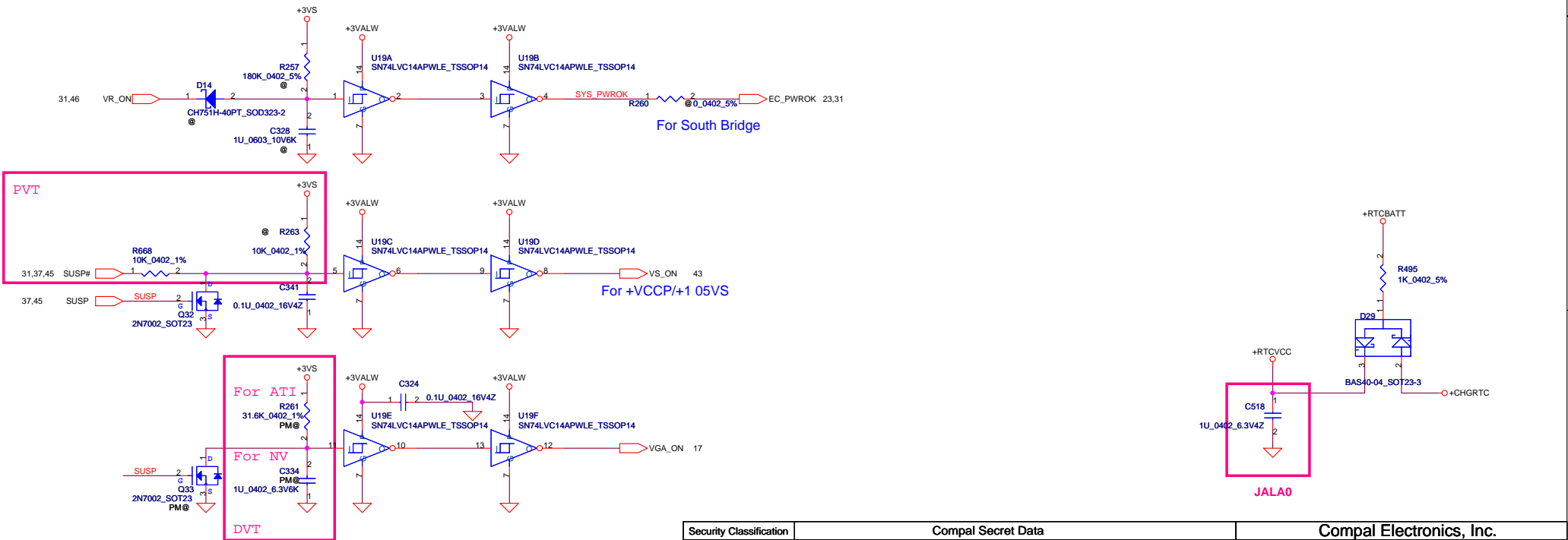
ON/OFF switch



HDA MDC Conn.

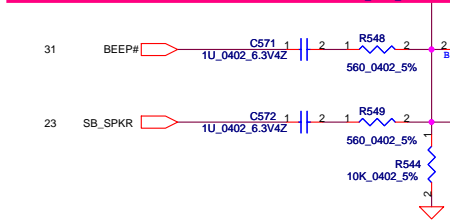


Power ON Circuit



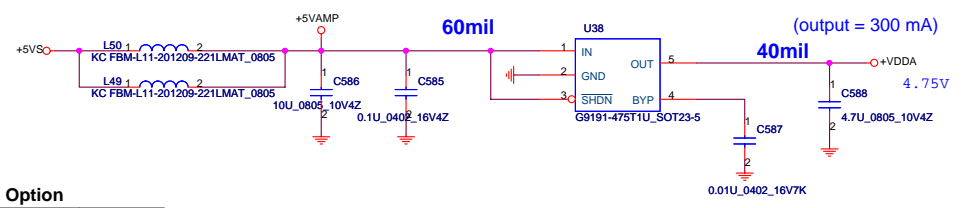
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Cardbus usage for JALA0

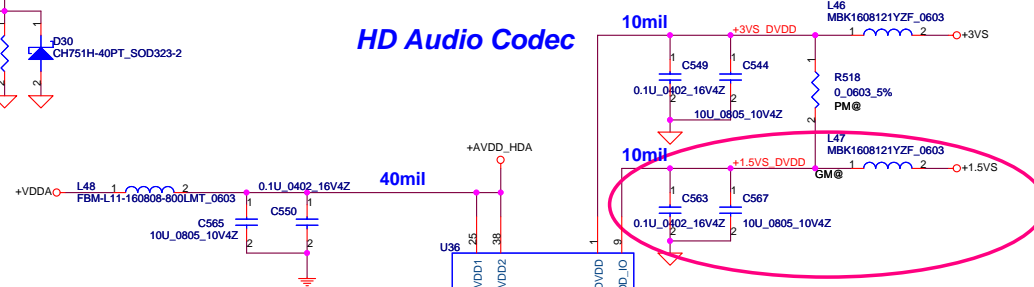


BOM Option

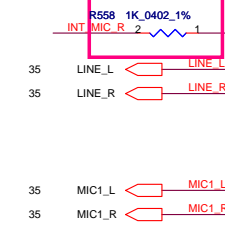
ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@



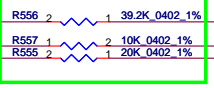
HD Audio Codec



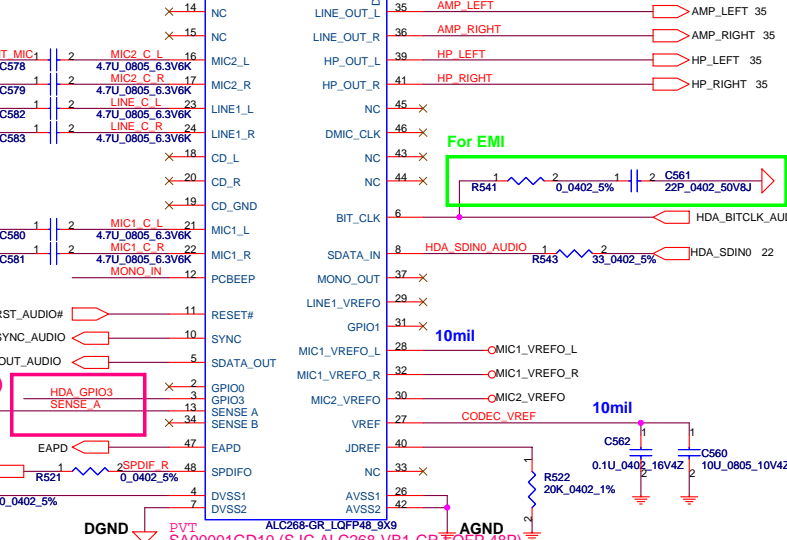
ESD(JALA0)



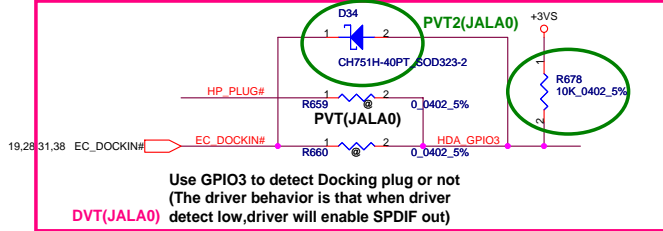
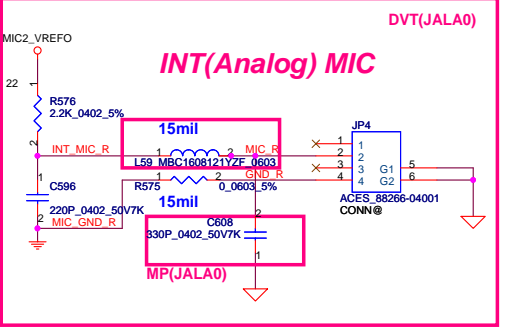
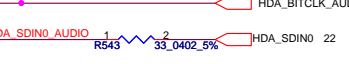
Place close to Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



For EMI

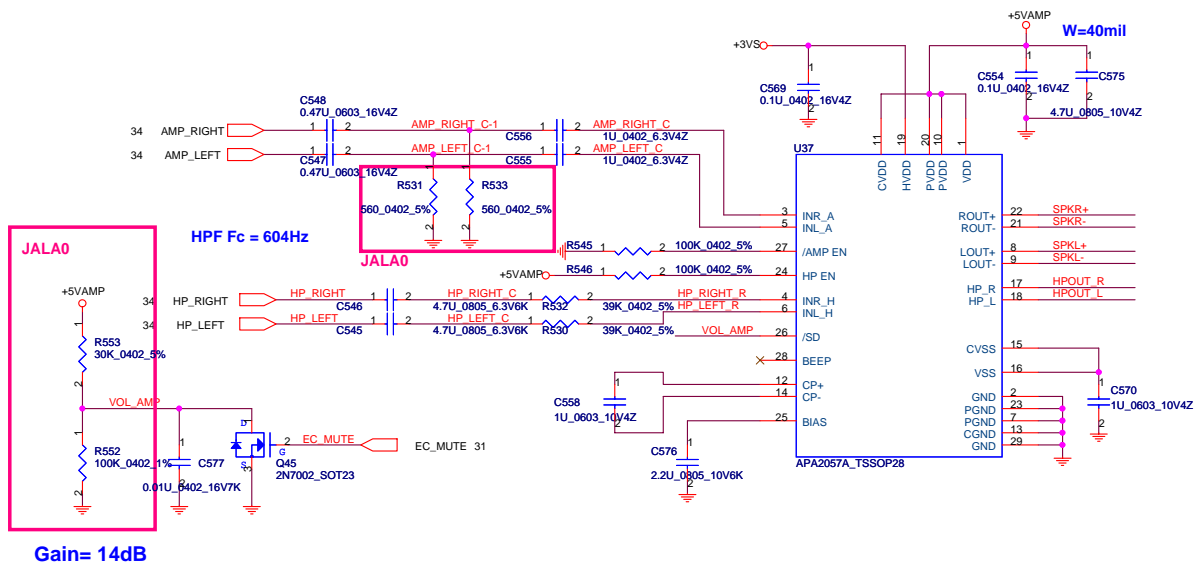


Use GPIO3 to detect Docking plug or not
(The driver behavior is that when driver detect low, driver will enable SPDIF out)

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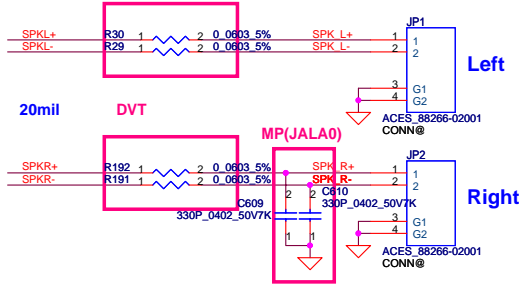
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Title		
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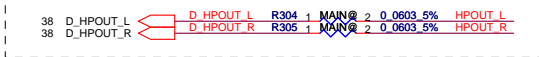


Gain= 14dB

Int. Speaker Conn.



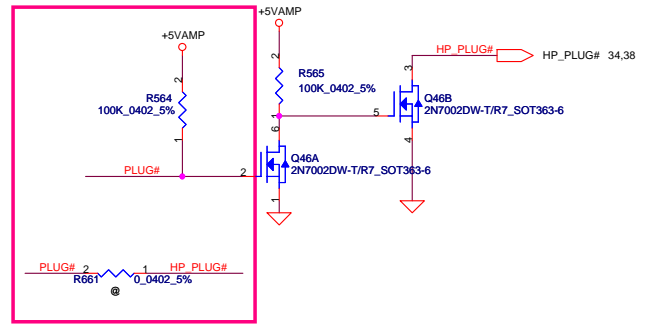
For Docking



For Docking

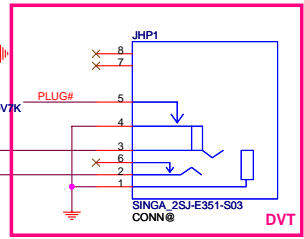
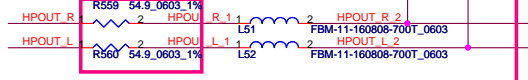


For Docking



DVT(JALAO) LINE Out/HP Out JACK

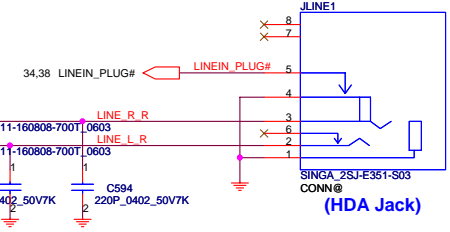
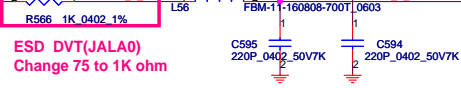
FSOV MP(JALAO)
Change 75 to 54.9 ohm



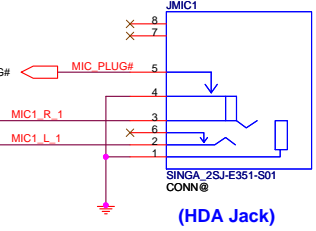
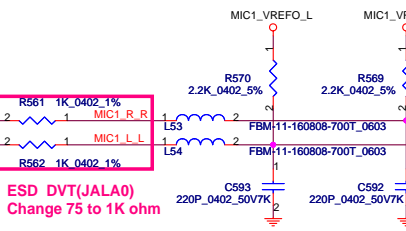
Change part

LINE-IN JACK

ESD DVT(JALAO)
Change 75 to 1K ohm

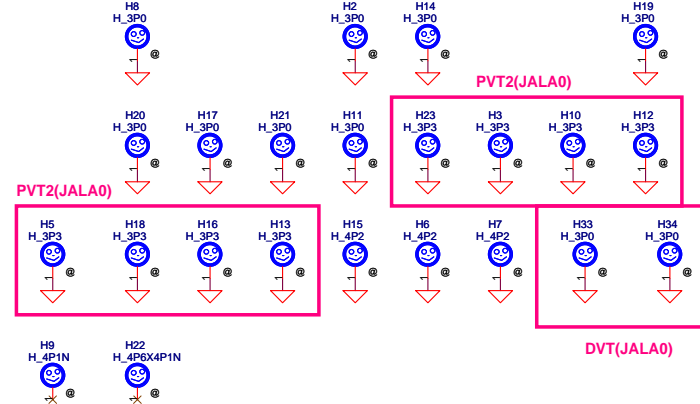
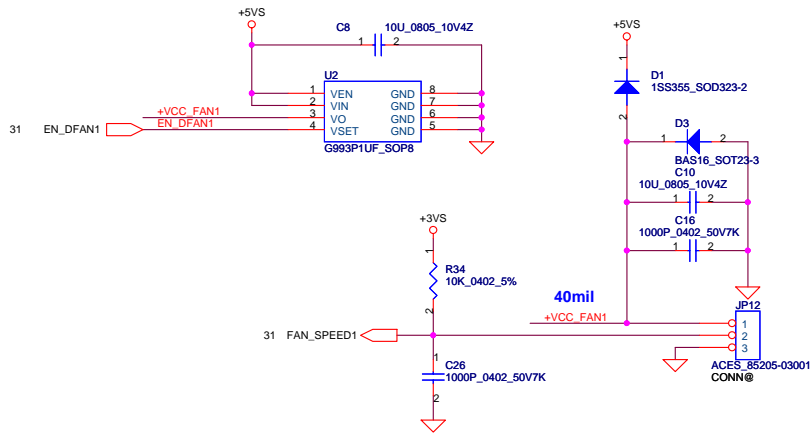


MIC JACK

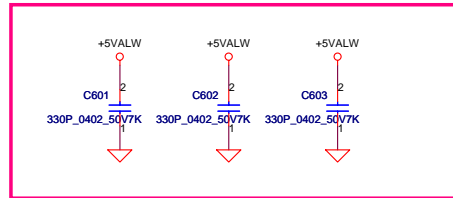


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FAN1 Conn



EMI



ADD DVT(JALA0)

EMI

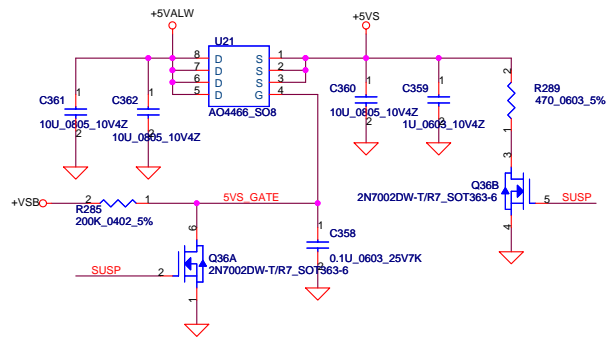


ADD PVT(JALA0)

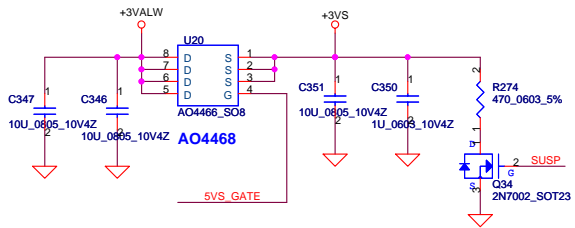


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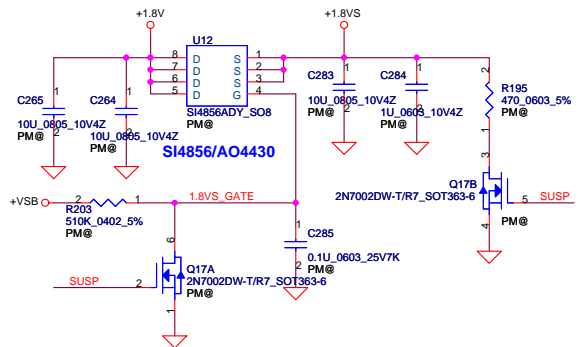
+5VALW TO +5VS



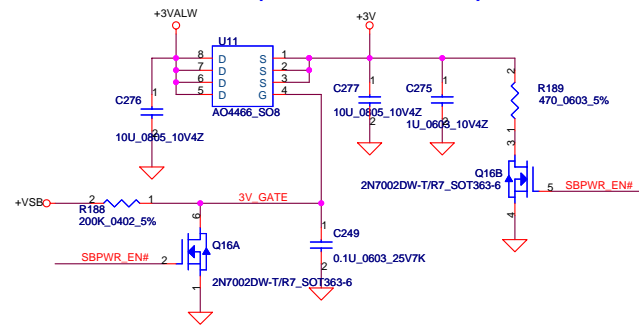
+3VALW TO +3VS



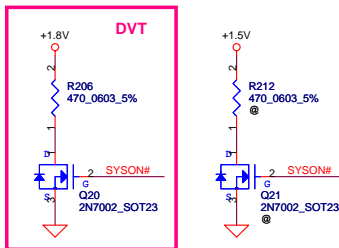
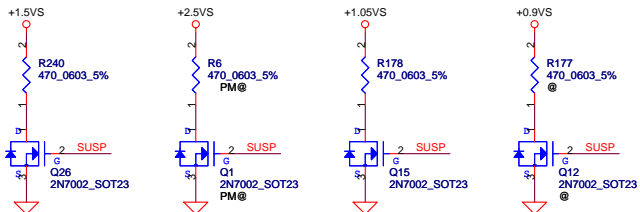
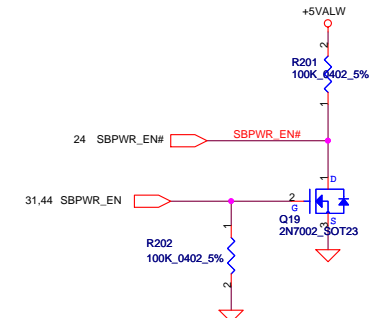
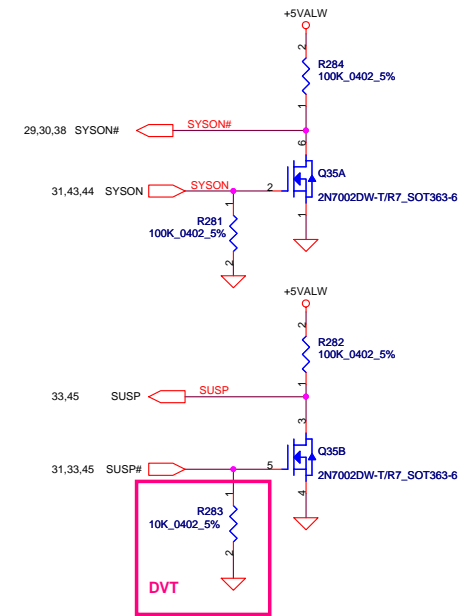
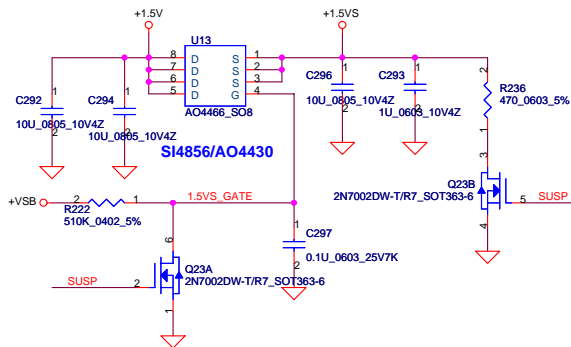
+1.8V to +1.8VS



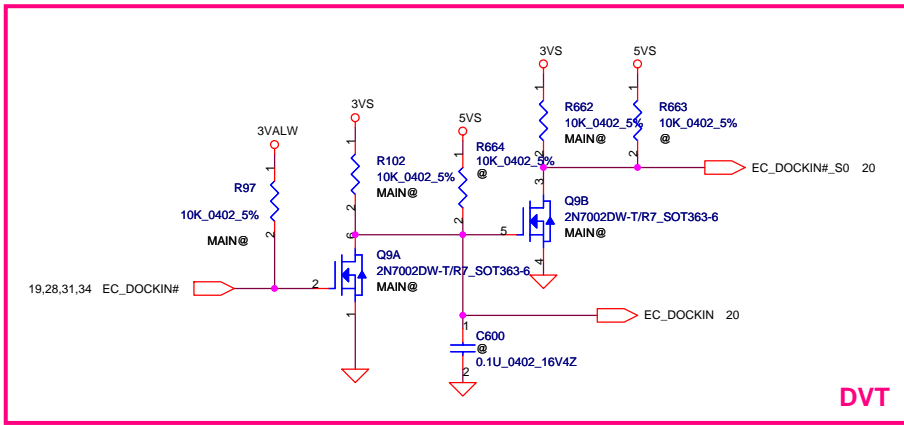
+3VALW TO +3V(ICH9M AUX Power)



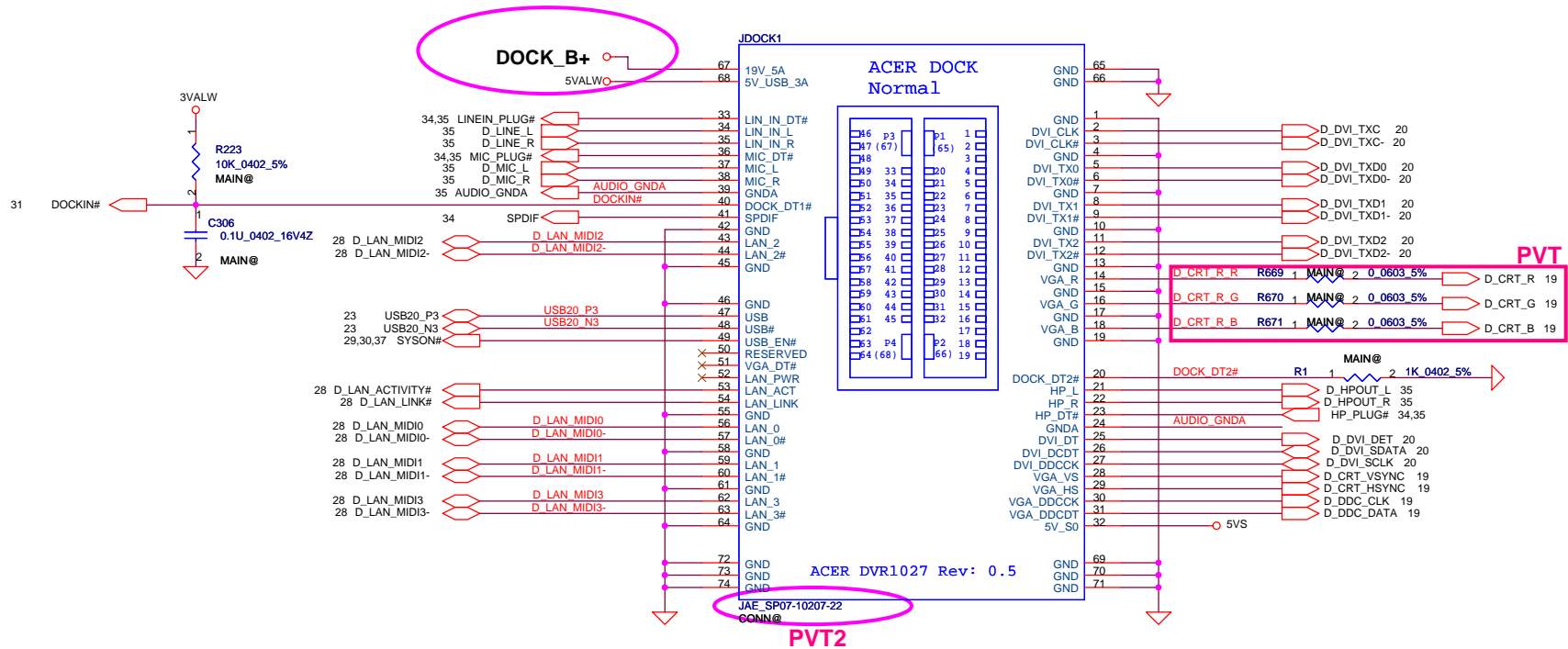
+1.5V to +1.5VS



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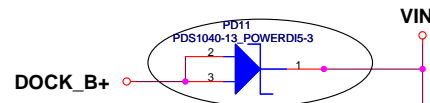


10/15 Acer DVR 1028 Rev0.3

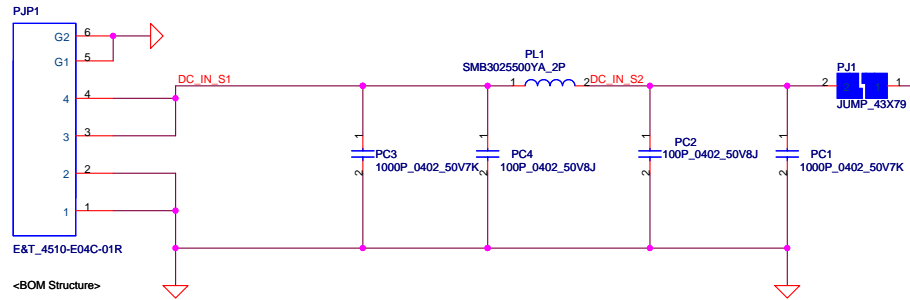


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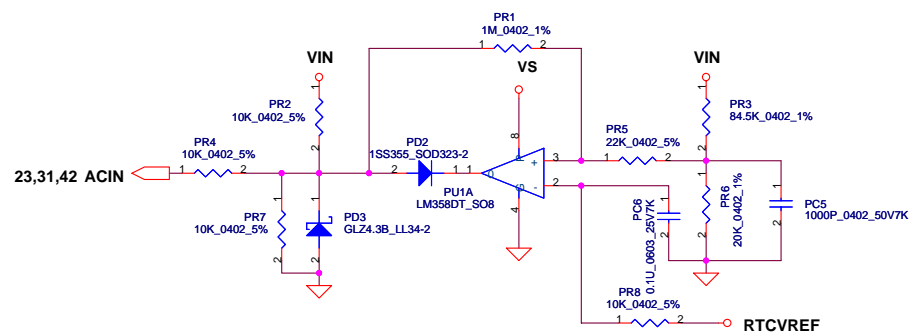
Place at HW side



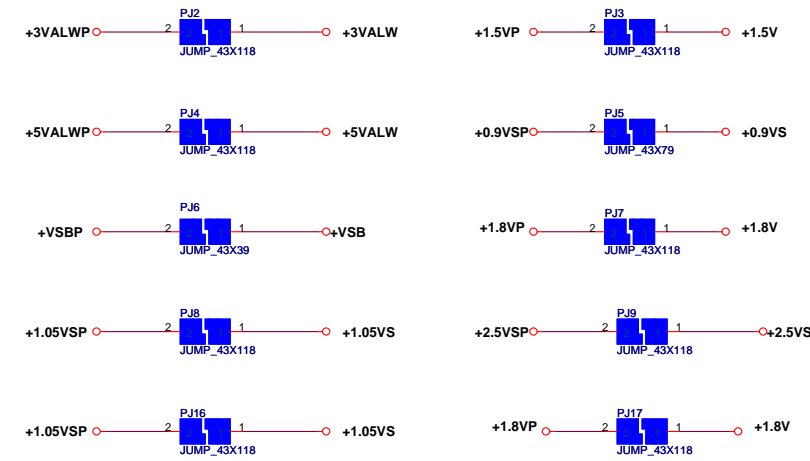
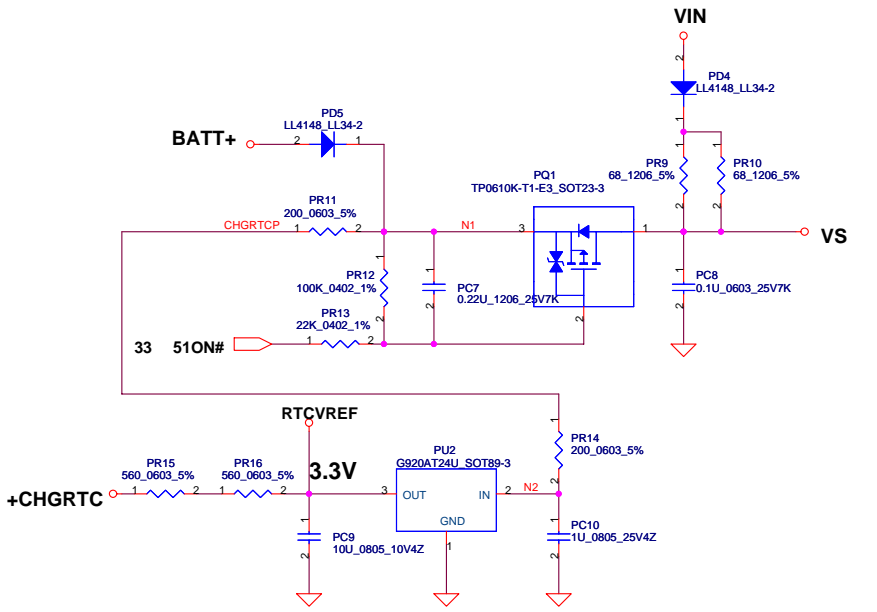
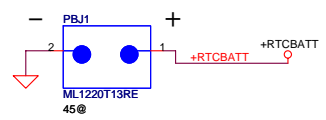
SP02000EF00



<BOM Structure>

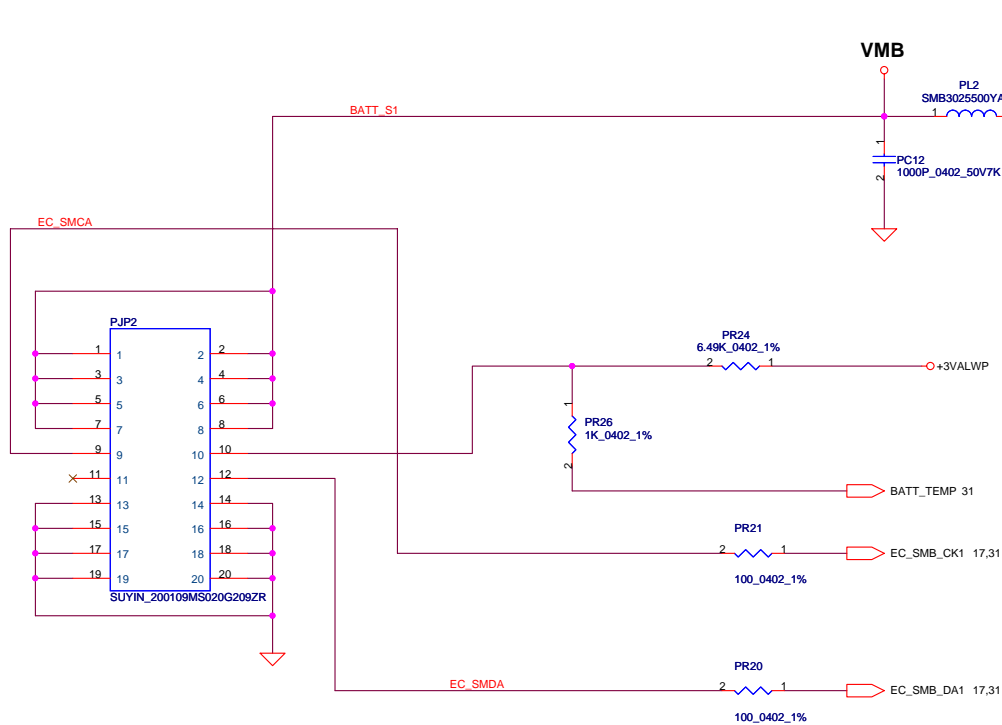


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

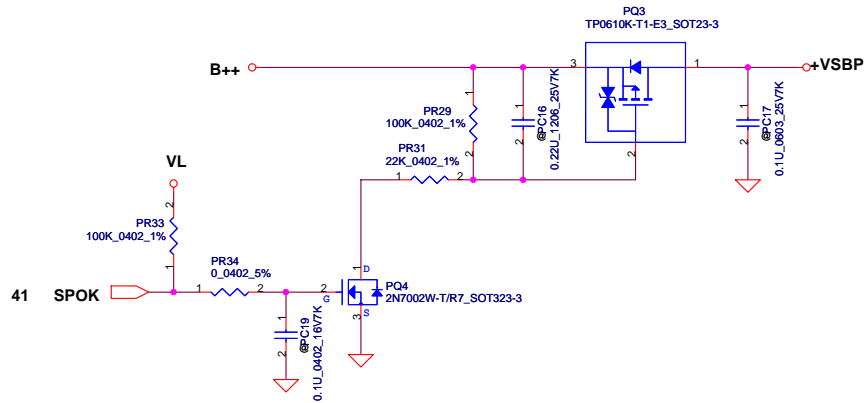
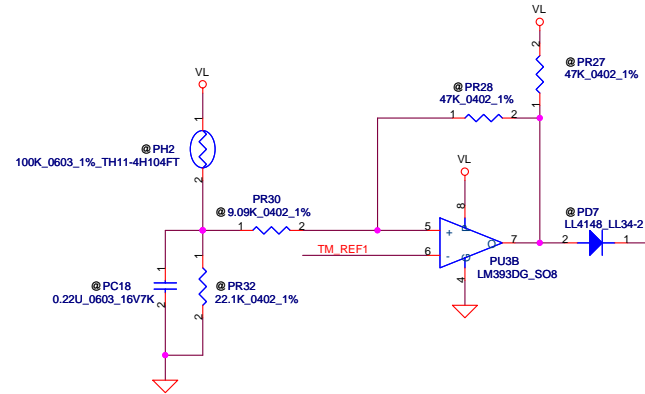


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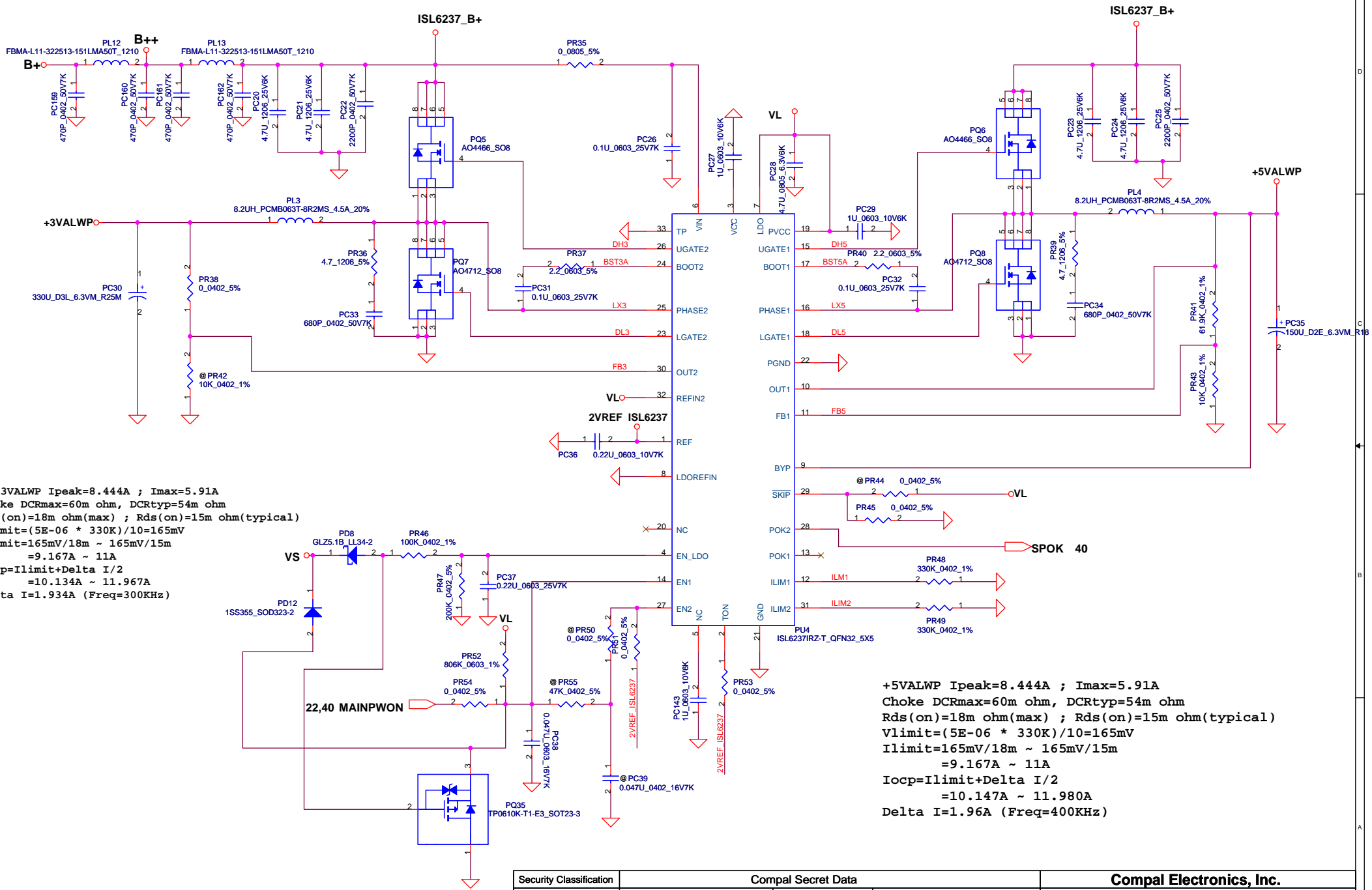
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



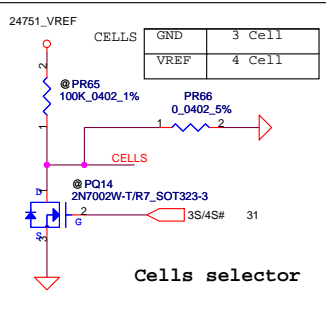
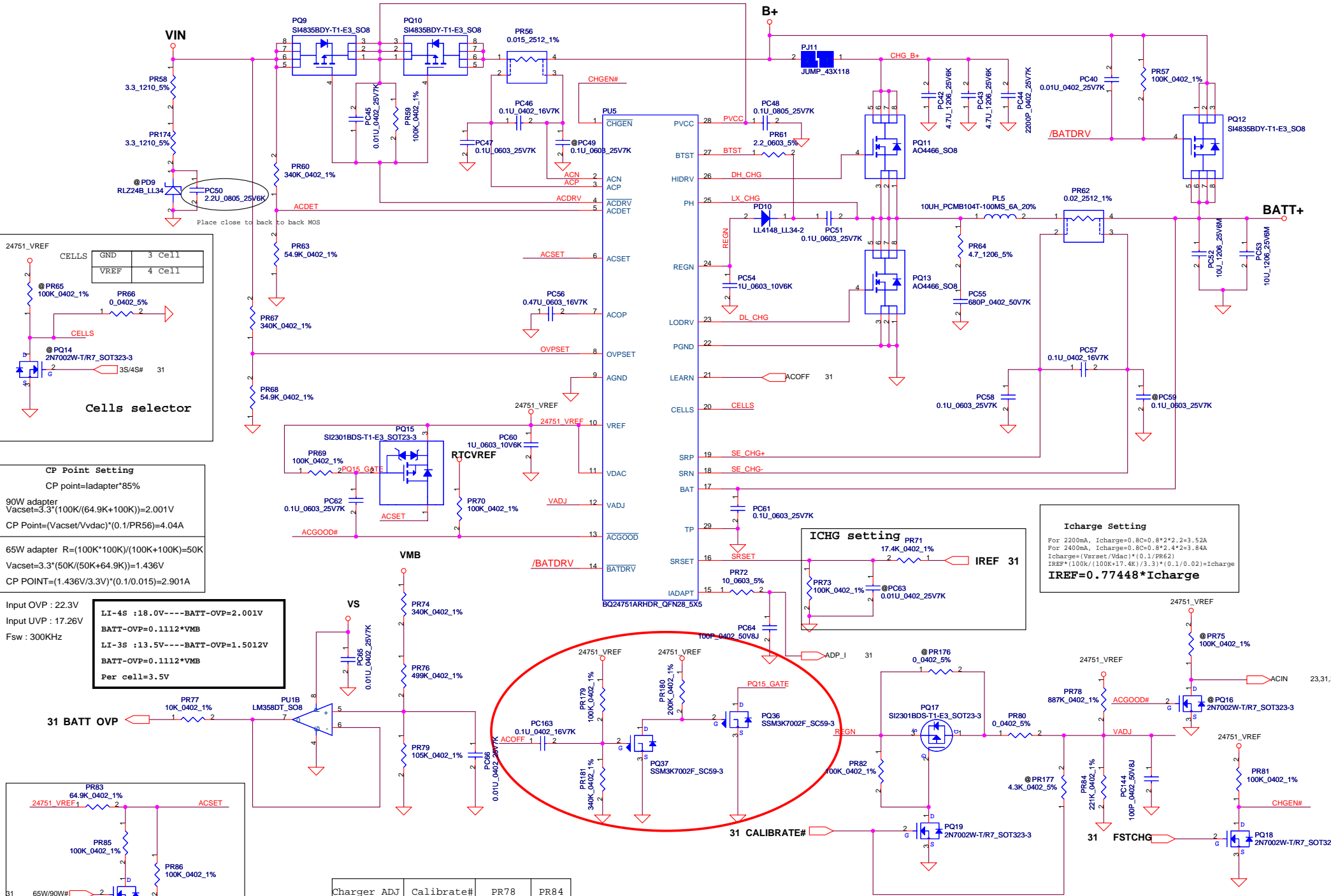
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m = 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2 = 10.134A \sim 11.967A$
 $\Delta I = 1.934A$ (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m = 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2 = 10.147A \sim 11.980A$
 $\Delta I = 1.96A$ (Freq=400KHz)

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CP Point Setting
 CP point=ladapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
 $CP\ Point = (V_{acset} / V_{dacc}) \cdot (0.1 / PR56) = 4.04A$

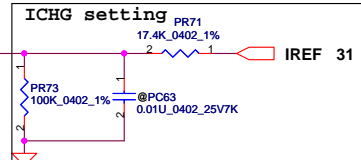
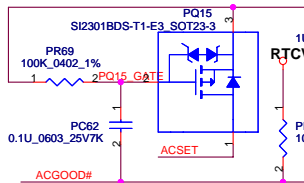
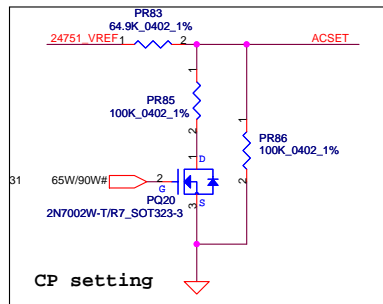
65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V --- BATT-OVP=2.001V
 BATT-OVP=0.1112 * VMB

LI-3S : 13.5V --- BATT-OVP=1.5012V
 BATT-OVP=0.1112 * VMB

Per cell=3.5V



Icharge Setting

For 2200mA, $I_{charge} = 0.8C = 0.8 \cdot 2.2 = 3.52A$
 For 2400mA, $I_{charge} = 0.8C = 0.8 \cdot 2.4 = 3.84A$
 $I_{charge} = (V_{acset} / V_{dacc}) \cdot (0.1 / PR62)$
 $IREF = (100K / (100K + 17.4K)) \cdot (3.3) \cdot (0.1 / 0.02) = I_{charge}$
 $IREF = 0.77448 \cdot I_{charge}$

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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 Deciphered Date: 2008/09/20

Compal Secret Data

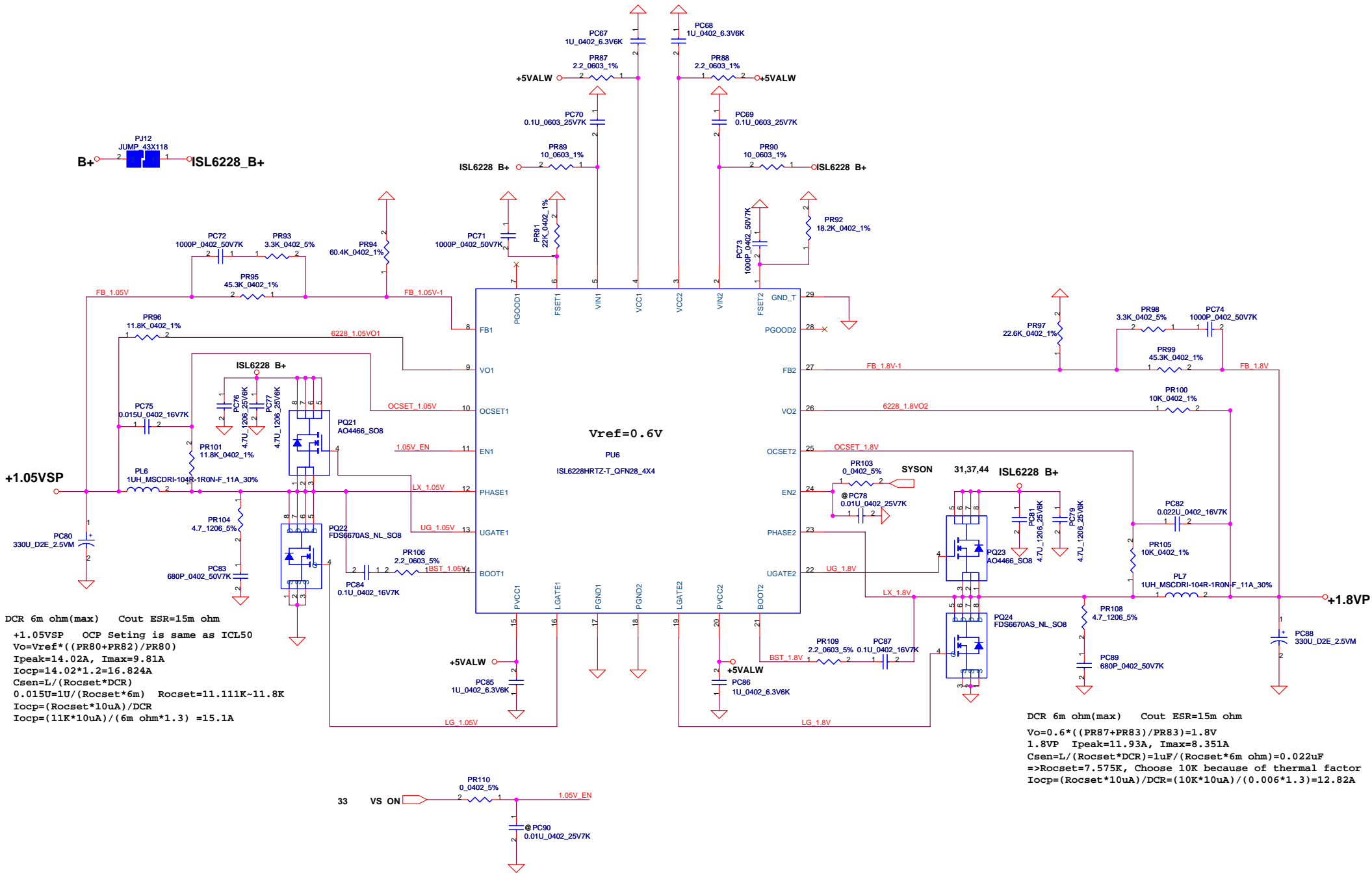
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Schematic MB A4221

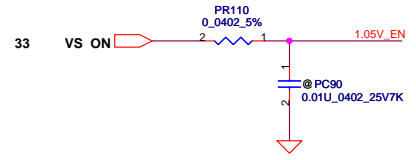
Document Number: **401552**

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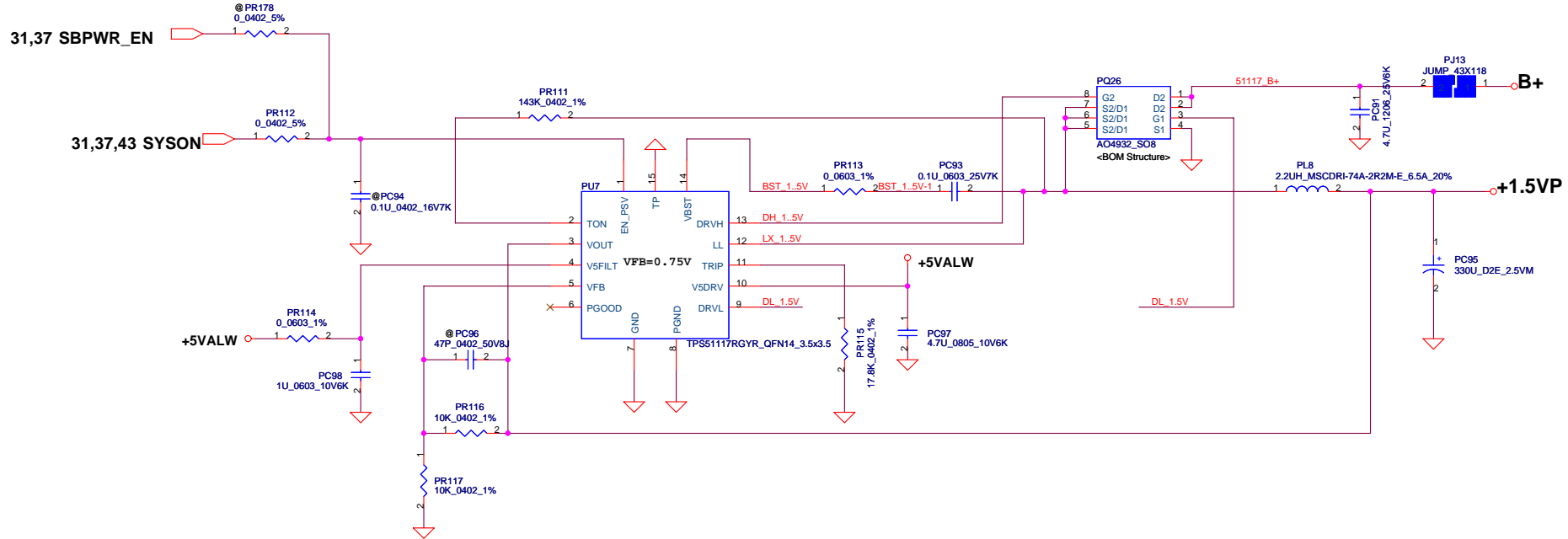


DCR 6m ohm(max) Cout ESR=15m ohm
+1.05VSP OCP Setting is same as ICL50
 $V_o = V_{ref} * ((PR80 + PR82) / PR80)$
 $I_{peak} = 14.02A$, $I_{max} = 9.81A$
 $I_{ocp} = 14.02 * 1.2 = 16.824A$
 $C_{sen} = L / (Rocset * DCR)$
 $0.015u = 1u / (Rocset * 6m)$ Rocset=11.111K-11.8K
 $I_{ocp} = (Rocset * 10uA) / DCR$
 $I_{ocp} = (11K * 10uA) / (6m ohm * 1.3) = 15.1A$

DCR 6m ohm(max) Cout ESR=15m ohm
 $V_o = 0.6 * ((PR87 + PR83) / PR83) = 1.8V$
1.8VP $I_{peak} = 11.93A$, $I_{max} = 8.351A$
 $C_{sen} = L / (Rocset * DCR) = 1uF / (Rocset * 6m ohm) = 0.022uF$
 $\Rightarrow Rocset = 7.575K$, Choose 10K because of thermal factor
 $I_{ocp} = (Rocset * 10uA) / DCR = (10K * 10uA) / (0.006 * 1.3) = 12.82A$



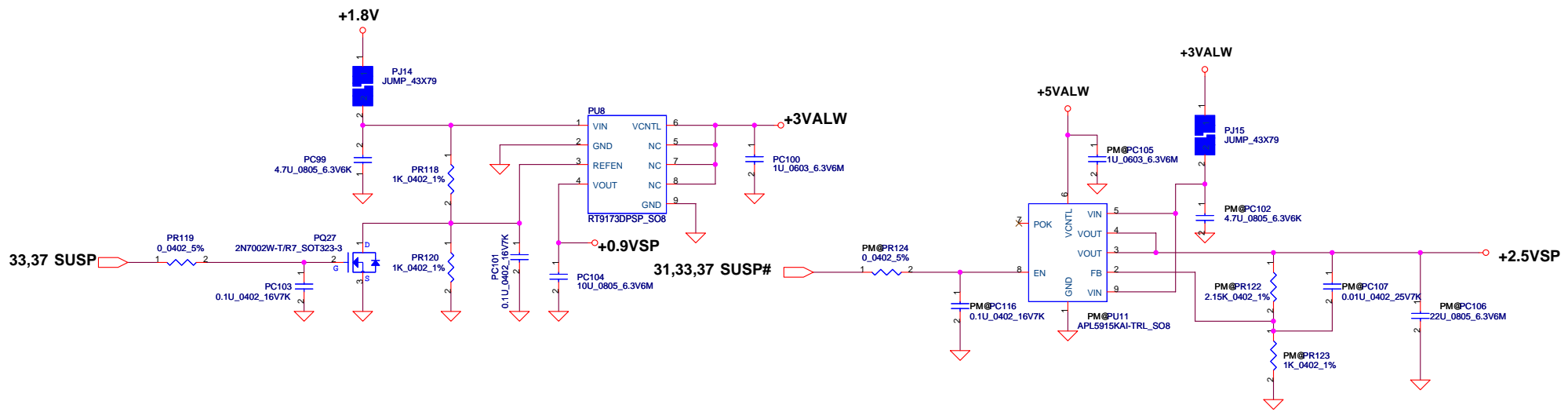
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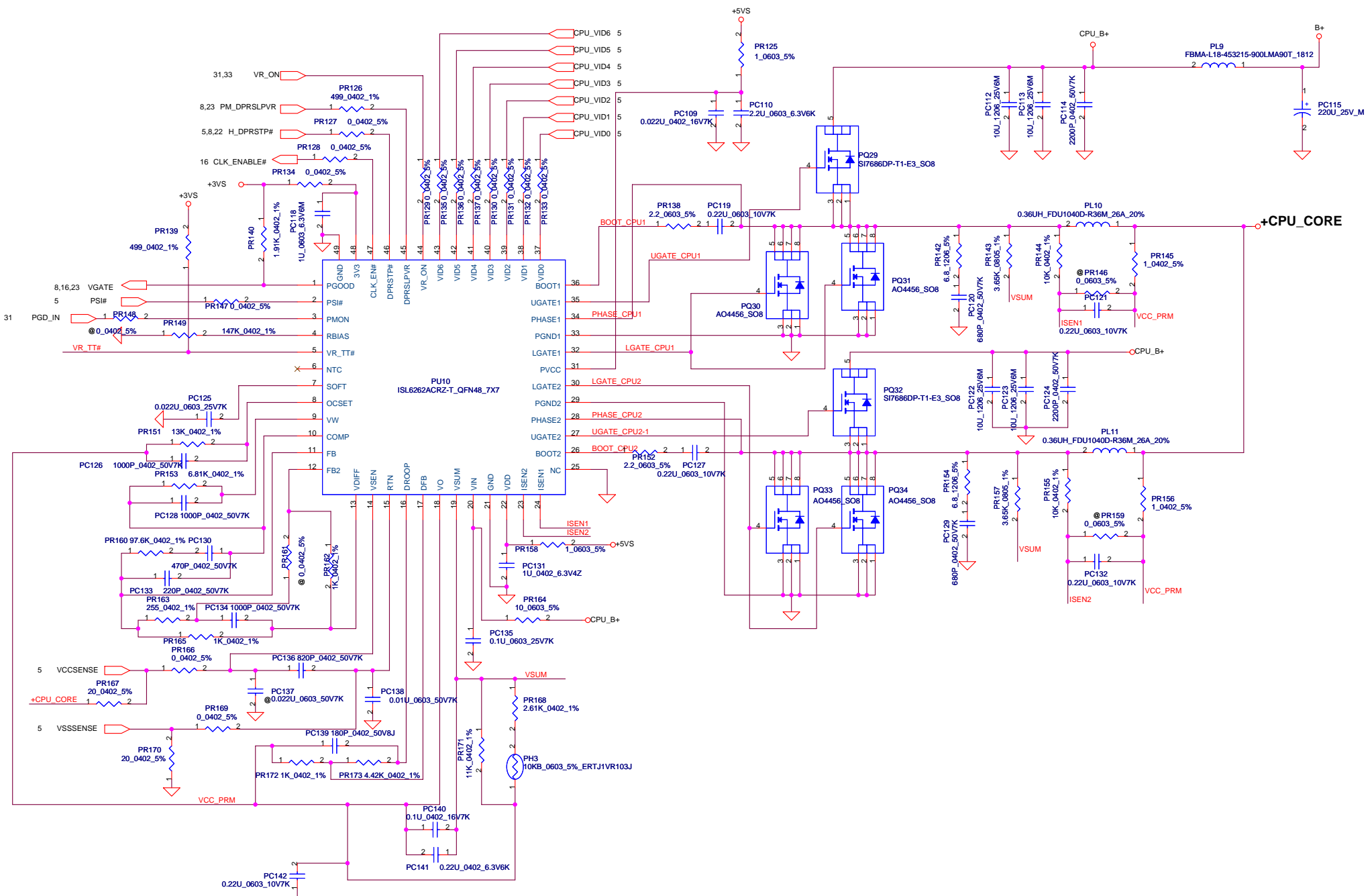
$VFB=0.75V$
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $Ton = 19 * e^{-12} * 143000 * ((2/3) * V_o + 100mV) / 19 + 50ns$
 $= 2.645e-7 \text{ us}$
 $=> V_o / Vin = D = Ton / Ts \Rightarrow Ts = 3.35us$
 $Fsw = 298KHz$

$Cout \text{ ESR} = 15m \text{ ohm}$
 $I_{peak} = 4.71A, I_{max} = 3.297A, I_{ocp} = 5.652A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.107A$
 $=> 1/2 \Delta I = 1.053A$
 $V_{trip} = R_{trip} * I_{ocp} = 17.8K * 10uA = 0.178V$
 $I_{ocpmin} = V_{trip} / R_{sonmax} * 1.2 + 1.053A$
 $= 0.178 / (0.027 * 1.2) + 1.053 = 5.493A + 1.053A = 6.546A$
 $I_{ocpmax} = (0.178 / (0.021 * 1.1)) + 1.053A = 7.705A + 1.053A$
 $= 8.758A$
 $I_{ocp} = 6.546A - 8.758A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Delete PD1.	Because we can cost down and DOCK_B+ has another one.	0.1	39	1 Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071108	EVT
2	3/5V exit on battery mode shutdown.	To prevent 3/5V exit on battery mode shutdown.	0.2	41	Add SC100001K00 (S DIO 1SS355 SOD323 T/R-5K	20071221	DVT
3	PD11 has over temp. issue.	Because PD11 has over temperature issue in JAQ60, we change it to a 10A diode.	0.2	39	Change PD11 from SCSB540C080 to SCS00002F00 .	20071221	DVT
4	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PR36 and PR39 to SD001470B80	20071221	DVT
5	Down size.	Down size. by sourcer request.	0.2	46	Change PC136 from SE025821K80 to SE000003W00	20071221	DVT
6	Down size.	Down size. by sourcer request.	0.2	46	Change PC120 and PC129 from SE024681J80 to SE074681K80	20071221	DVT
7	Down size.	Down size. by sourcer request.	0.2	43	Change PC72 and PC74 from SE068102J80 to SE074102K80	20071221	DVT
8	2nd source trial run TI controller.	2nd source trial run TI controller.	0.2	41	Add PC143 SE080105K80	20071221	DVT
9	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PC33 and PC34 SE074681K80	20071221	DVT
10	To meet Jeta SPEC.	To meet Jeta SPEC.	0.2	42	Add PC144 SE074102K80	20071221	DVT
12	Add EMI solution.	Add 3/5V boost resistor.	0.3	41	Add PR37, PR40 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
13	Add EMI solution.	Add charger boost resistor.	0.3	42	Add PR61 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
14	Add EMI solution.	Add charger snubber.	0.3	42	Add PR64 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC55 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
15	Add EMI solution.	Add 1.05V/1.8V boost resistor.	0.3	43	Add PR106, PR109 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
16	Add EMI solution.	Add 1.05V snubber.	0.3	43	Add PR104 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC83 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
17	Add EMI solution.	Add 1.8V snubber.	0.3	43	Add PR108 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC89 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
18	Add EMI solution.	Add CPU boost resistor.	0.3	46	Add PR138, PR152 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
19	Add EMI solution.	Add 3/5V input capacitor filter..	0.3	41	Add PC159, PC160, PC161, PC162 SE074471K80(S CER CAP 470P 50V K X7R 0402)	20080102	DVT
20	Add EMI solution.	Add 3/5V input beat	0.3	41	Add PL12, PL13 SM010016410(S SUPPRE_ KC FBMA-L11-322513-151LMA50T)	20080102	DVT
21							
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.4	Change R25 , R18 , R11 , R19 from 56 to 54.9 ohm	Reference standard circuit
	P.4	Delete R10	Foe ESD
	P.4	Change CPU temp sensor U9 , R55 / R56 from 100 to 0 ohm , delete R64 / R652	ADI had issue , for SMSC / Fintek temp sensor , no used for OD output
	P.8	Change R525 , R527 connected from +1.05Vs to GND	Reference standard circuit
		Change Cantiga GM U30 as SA00001P930 (Ver:B0)	Revision upgrade
		Change Cantiga PM U30 as SA00001Z030 (Ver:B0)	
	P.12	Change L42 , L18 , C499 , C229 , C280 , C232 as GM@	Reference standard circuit
	P.12	Change R596 , R597 as PM@	For UMA CRT
		Add C597 (220U)	Reserved
	P.12	Add C597 (220U)	Reference standard circuit
	P.12	Change R110 , C187 , C196 as stuff , R117 un-stuff	DFX
	P.12	C461 down size as 10U_0603	NA
	P.16	Change Q30 (dual N-MOS) as Q48 , Q49 (2 single N-MOS)	NA
	P.17	C500 down size as 680P_0402	For BOM
	P.17	Add L57 , L58 , C598 , C599 for +1V8RUN	+1V8RUN ripple (+1V8RUN is for MXM +PEX1V2)
	P.17	Add R599 as 0ohm	Reserve R598 , D31
	P.17	Update JMXM1 footprint	NA
	P.17	Change Q41 (dual N-MOS) as Q50 , Q51 (2 single N-MOS)	NA
	P.18	C364 down size as 680P_0402	For BOM
	P.18	C365 , C366 , C367 change from 220P to 820P	For EMI
	P.19	D5 change as RB411DT146_SOT23-3	Common part
	P.19	Change Q40 (dual N-MOS) as Q52 , Q53 (2 single N-MOS)	NA
	P.19	Change C401 , C409 , C419 as 15P	For DISCRETE CRT
	P.19	Change C402 , C410 , C420 as 12P	For DISCRETE CRT
	P.19	C408 , C418 , C423 (22P) stuff for UMA only	For UMA CRT only
	P.19	Change L1 , L2 from FCM1608C-121T_0603 as 10ohm_0603	For CRT
	P.20	Change Q7 from 2N7002_SOT23(Dual N-MOS) as Q7 & Q47(Single BSH111 N-MOS)	For DVI SMBUS level shifter
	P.20	Add R600 & R602 (4.7K ohm) pull high +3Vs	For DVI SMBUS
	P.20	Reserve R601 & R603 (2.7K ohm) pull high +5Vs	For DVI SMBUS
	P.20	Reserve U39 & U40 (SN74CBTD3306CPWR_TSSOP8)	For DVI & HDMI SMBUS
	P.20	Change D21 from RB751V_SOD323 as CH751H-40PT_SOD323-2	NA
	P.22	Change R478 from 33 ohm as 1K ohm	Customer request
	P.22	LAN_RST# connect to GND	No used Integrated LAN
	P.22	R169 un-stuff	For mobile
	P.22	Add CR_CPPE#(GPIO7) & CR_WAKE#(GPIO22)	For JMB385 power management
	P.22	Swap PCIE(x1) port 2 & port 4	NA
	P.22	R385 un-stuff , U28 stuff	For sequence
	P.25	U34.127 is used as external IDSEL	NA
	P.25	R489 un-stuff	For PCMCIA Lan card not support PM_CLKRUN# function
	P.25	Update JPCM1 footprint	For DFX
	P.26	Reserve R655 , R656 , D33 for CR_CPPE# & CR_WAKE#	For JMB385 power management
	P.26	Cantiga JMB385 U32 as SA00001W910 (Ver:B)	Revision upgrade
	P.27	Delete BCM5787M co-lay schematic	NA
	P.27	Update U25 footprint	For DFX
	P.28	Change T1 from GSL5009 as GSL5009-1(SP050003T10)	NA
	P.28	Add C375 , C383 (68P)	For EMI
	P.29	Add R658	Add 80 port function on JMINI2
	P.30	D32(SC300000B00) stuff	For ESD
	P.31	Add R604	NA
	P.31	R248 change from 0 ohm as 8.2K ohm	Foe Board ID as 1 define

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PHASE	PAGE	MODIFICATION LIST	PURPOSE	
DVT	P.31	C286 change from 3.3U as 4.7U	Stable KB926 internal +1.8V regulator , ENE suggestion value	
	P.32	JP6 pin define reverse	NA	
	P.32	Change SW3 & SW4 type	NA	
	P.32	U15 change from 1MB as 2MB capacity SPI ROM	Add Finger print code	
	P.33	R261 change from 10K as 31.6K	Fix ATI MXM sku can't power on for battery mode issue	
	P.33	C334 change from 0.1U as 1U	Fix nVIDIA MXM sku power on issue	
	P.34	Delete Internal(Digital) MIC reserved circuit	NA	
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI	
	P.34	Add R660 to connect HDA_GPIO3 with DOCKIN#	For docking spdif feature enable	
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI	
	P.35	R559 / R560 change from 47 ohm as 75 ohm	For Audio precision FSOV	
	P.35	R561 / R562 / R566 / R571 change from 75 ohm as 1K ohm	For ESD , Realtek suggestion value	
	P.36	Add C601 , C602 , C603 (330P) on +5VALW	For EMI	
	P.37	R283 change from 100K to 10K	NA	
	P.37	R206 , Q20 stuff	For +1.8V discharge	
	P.38	Add switch to enable/disable EC_DOCKIN#_S0 for HDMI SMBUS	NA	
	P.38	Update JDock1 footprint	NA	
	PVT1	P.16	Change C308 / C311 (33P) as 27P	For RTC accuracy
P.23		Use 4MB SPI ROM	For Kinabalu_High & Kinabalu_Low	
P.23		Add test point T32 / T33 / T34 / T35	Reserved for PCIE(X1) port 1	
P.25		Change U35 as SA000026P10(OZ2210GN-B1)	For B1 version	
P.27		Change U23 as SA000025P20(BCM5764MKMLG P20)	For B0 version	
P.27		Reserved R673 , R674 (0 ohm)	For Lan SMBUS	
P.27		Reserved Lan GPIO0(LAN_ALERT#) / LAN_ALERT#_EC / R675 , R676 , R677 to EC	For Lan ASF workaroud	
P.27		U23 Pin17 / Pin5 / Pin55 connect to U23 Pin18 for power +Lan_VDDIO_1.2	U23 Pin18 is power source +Lan_VDDIO_1.2 for U23 Pin17 / Pin5 / Pin55	
P.27		U23 Pin38 / Pin52 NC	NA	
P.29		Change JMINI1 for Robson2 , chnagne JMINI2 for Wireless	NA	
P.31		Add LAN_ALERT#_EC & EC_ACIN for EC	Reserved for ASF workrund & Nvidia MXM power saving	
P.33		Add R668(10K) & reserved R263(10K)	Fine tune +1.05VS timing for UMA boot display flash	
P.34		Change U36 as ALC268-VB1-GR(SA00001GD10)	Version upgrade	
P.34		Stuff R659 & un-stuff R660	For SPDIF feature on docking	
P.36		Add C604 , C605 (820P_0402)	For EMI	
P.50		Chipset change as GM(SA00002JT10) / PM(SA00002JJ00) / ICH9M(SA00002JH00)	Version upgrade	
PVT2		P.27	Update U23 CIS symbol	U23 Pin38 , 52 can't be changed as NC
		P.34	Add D34 , R678	For ACER docking SPDIF feature (No SPDIF on board)
		P.38	Update JDock1 CIS symbol	Docking connector modify (add boss x 2) for DFX
		P.35	Delete D2 , D4 (Int SPK ESD diode)	NA
	P.34	Delete D9 (Int MIC ESD diode)	NA	
	P.35	Add C609 , C610 (330P_0603) on Right SPK	For EMI	
	P.34	Add C608 (330P_0603) on Int MIC	For EMI	
	P.08	Add Test point (T39 , T40 , T41 , T42)	Add Management Engine JTAG pins	
	P.27	Add C612 , C614 (0.1u_0402) for +LAN_AVDD	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV	
	P.27	Add C615 , C616 , C617 (0.1u_0402) for +LAN_AVDDL	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV	
	P.08	Add U41, R679 , R680 , R681 , R682 , R683 , R684 , R685 , T43	Reserved for Management Engine JTAG debug	
	P.07	Chipset change as GM(SA00002JT50) / PM(SA00002JJ50)	Version upgrade	
	P.20 , P.31	Add EC_DVI_DET , EC_GPIOB , EC_GPIOC , R687 , R688 , R691	Reserved for DVI detect delay control (by EC)	
	MP	P.24	R73 , R148 change from 10_0402 to 100_0402 C128 , C204 change from 0.1U_0402 to 1U_0402	For USB issue on ICH9M A3 stepping
		P.34 , P.35	C608 , C609 , C610 change from 330P_0603 to 330P_0402	For 330P_0402 is standard part
P.31		Change R248 as 33K	Board ID upgrade	
P.30		Add R692 / R693 (0_0603)	Reserved S3 power rail for check finger print sensor S3 resume too slow	

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PHASE


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MODIFICATION LIST



PURPOSE

P.20	Add D35	Reserved for HDMI_HPD
P.30	Add R694 / R695 (0_0603)	Reserved for check
P.27	Delete C612 , C614 , C615 , C616 , C617 (0.1u_0402)	No need
P.16	Stuff R689 / R690	Reserved for LAN power saving
P.35	R559 , R560 change from 75 to 54.9 ohm Chipset change as GM(SA00002JTB0) / PM(SA00002JJA0) / ICH9M(SA00002JH70)	For FSOV between 420mv~480mv Version upgrade
P.32	R291 , R294 change from 300_0402_5% to 150_0402_5%	For ACER Hank's request to fine tune brighter
P.20	R84 , R85 , R86 , R91 change from 2K_0402_5% to 4.7K_0402_5%	For UMA DVI/HDMI monitor P193WA (x) detect issue (On JAL90)

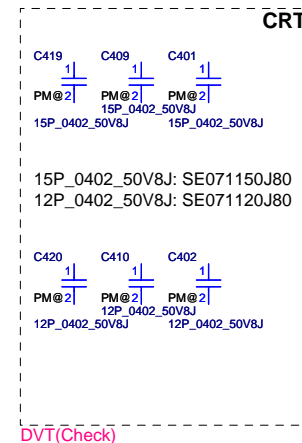
PCB

ZZZ

 LA4221MB Rev0: DA600007R00
 LA4221MB Rev1: DA600007R10
 LA4221MB with Sub/B Rev1: DAZ04800100
 PCB 047 LA-4221P REV1 M/B


IC


U30

 CANTIGA ES_FCBGA1329
 DVT CANTIGA PM: SA00001ZO30 (S IC EB88CTPM QR34 B0 FCBGA 1329 ES)
 PVT CANTIGA PM: SA00002JJ00 (S IC AC88CTPM QT78 B2 FCBGA 1329 PM)
 PVT2 CANTIGA PM: SA00002JJ50 (S IC AC88CTPM QU38 B3 FCBGA 1329 PM)
 Pre-MP CANTIGA PM: SA00002JJA0 (S IC AC82PM45 SLB97 B3 FCBGA1329 PM ABO!)
 U30

 CANTIGA ES_FCBGA1329
 DVT(Check_TBD) CANTIGA GL: SA000023Z00 (S IC CANTIGA ES FCBGA 1329 MCH GL)


For Discrete




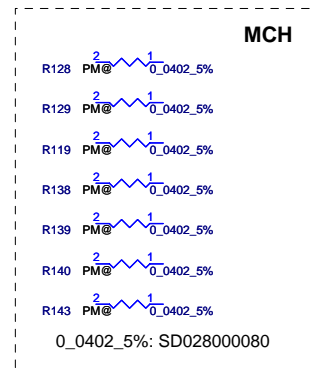
DC Cable

ZZZ

 DC Cable (65W)
 @ PVT(54 Rank)
 DC301003R00(CONN SET 048 DCJACK-MB 2DW-G756-I50 65W)

U10

 ICH9ME@
 ICH9-M ES_FCBGA676
 ICH9-M: SA00002G120
 (S IC AF82801IEM QT10 A3 PBGA 676P ICH9M)

ZZZ

 DC Cable (90W)
 @ PVT(54 Rank)
 DC301003S00(CONN SET 048 DCJACK-MB 2DW-G756-I49 90W)

U6

 SPI2MB@
 W25X16-VSSIG_S08
 MP Winbond: SA00001KN00
 (S IC FL 16MBIT W25X16-VSSIG SOIC 8P)



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