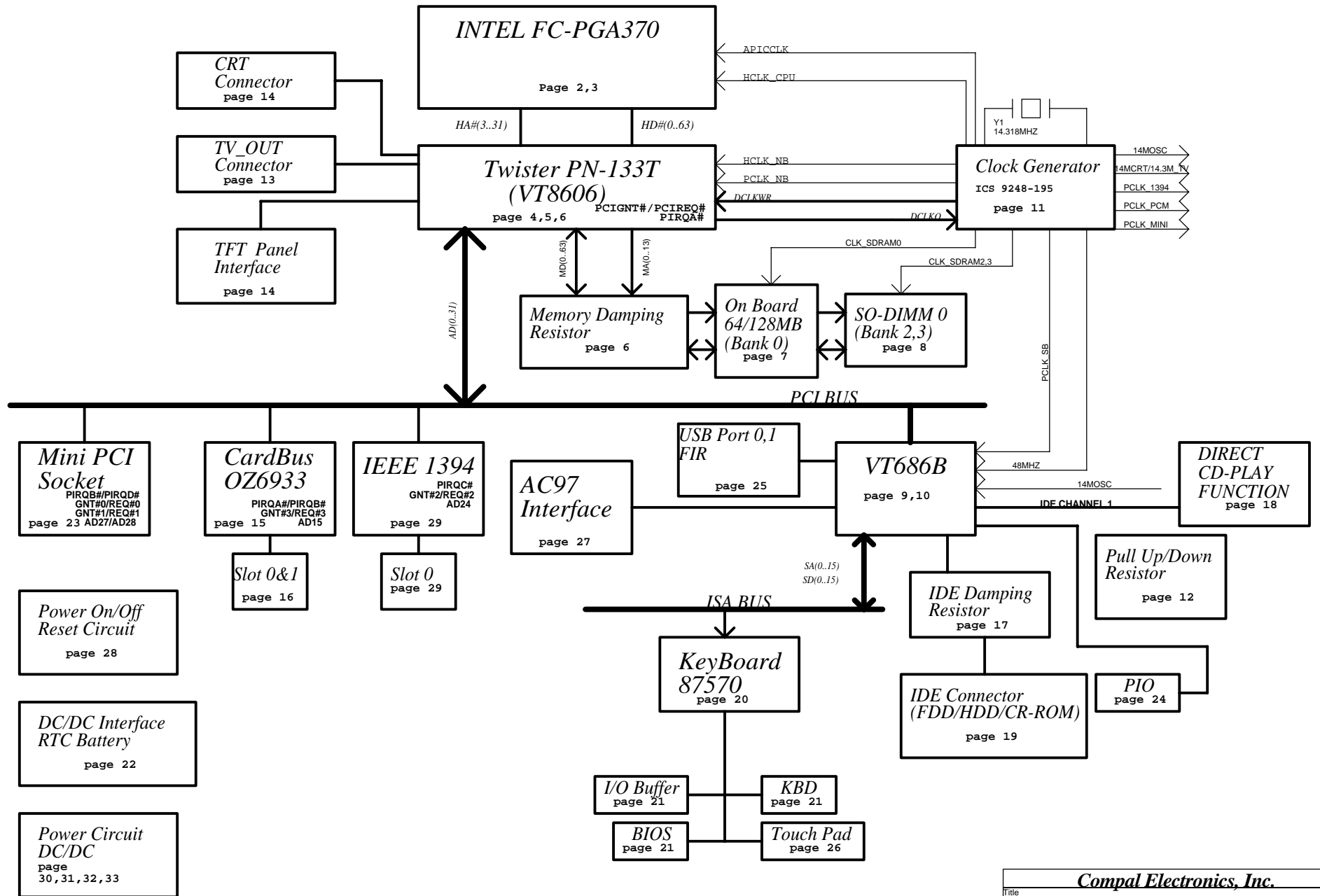


Model Name : CY23 LA-1281 Rev1.0



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Title			Compal Electronics, Inc.		
Size			SCHEMATIC, M/B LA-1281		
Document Number			401202		
Date			星期一, 十月 22, 2001		
Sheet			1 of 34		
Rev			1B		





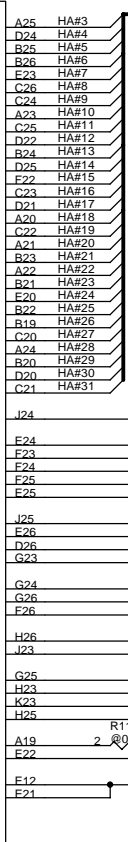
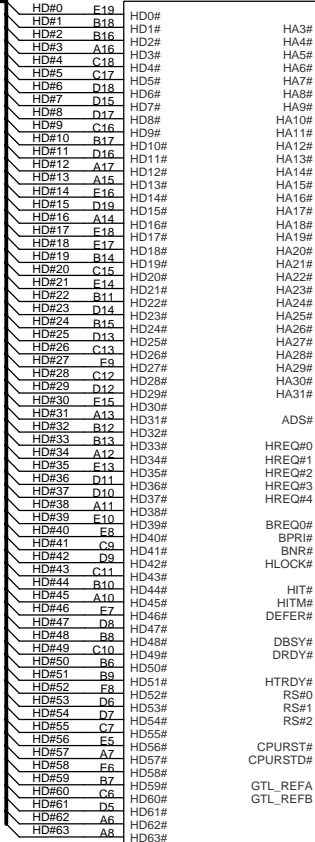
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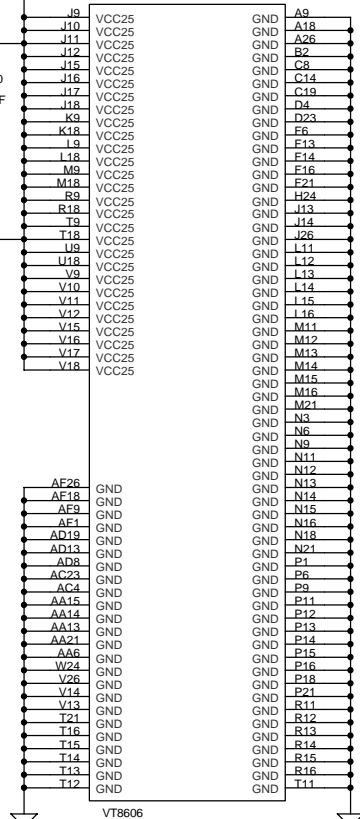
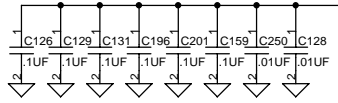
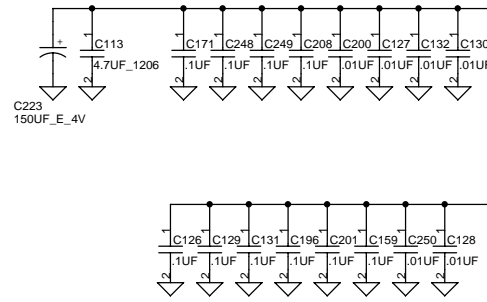
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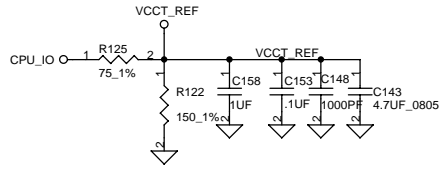
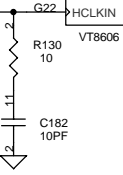


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U14E



11 HCLK\_NB

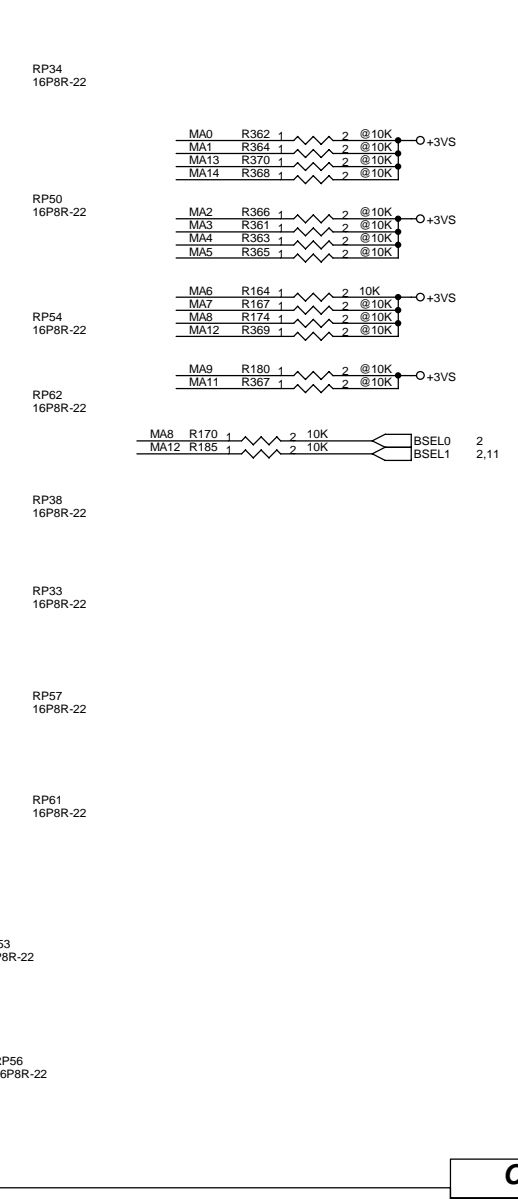
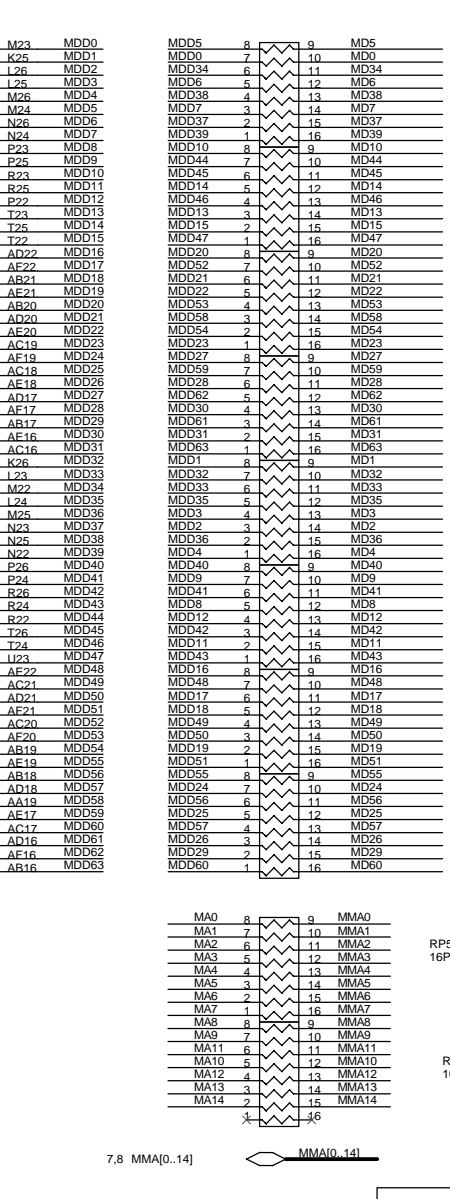
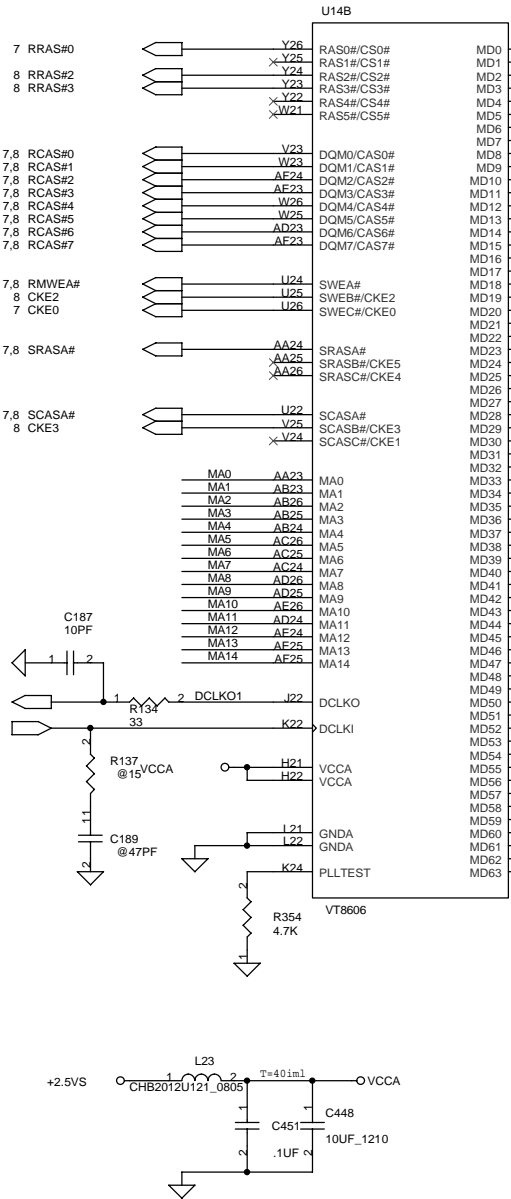


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Title		SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev	
B	401202	1B	
Date:	星期一, 十月 22, 2001	Sheet	4 of 34

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Strap	Description	Setting
MA12,8	CPU Clock Frequency	01=100Mhz 11=133Mhz 00=60Mhz
MA2	PCI Base Address Mapping	0=Map0 1=Map1
MA3	Graphic IO Enable/Disable	0=Enable 1=Disable
MA4	PCI Interrupt	0=Enable 1=Disable
MA7	Graphic Test Mode	0=Normal 1=Test
MA9	VGA Clock Select	0=PLL 1= External
MA11	IOQ Level	0=4Level 1=1Level
MA0,1,13,14	Panel Type	

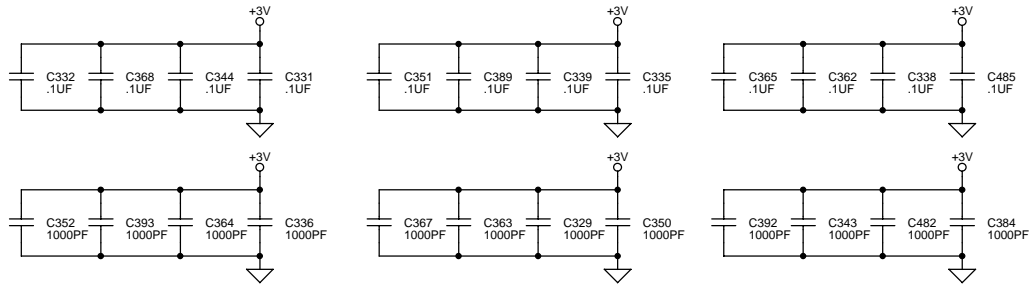
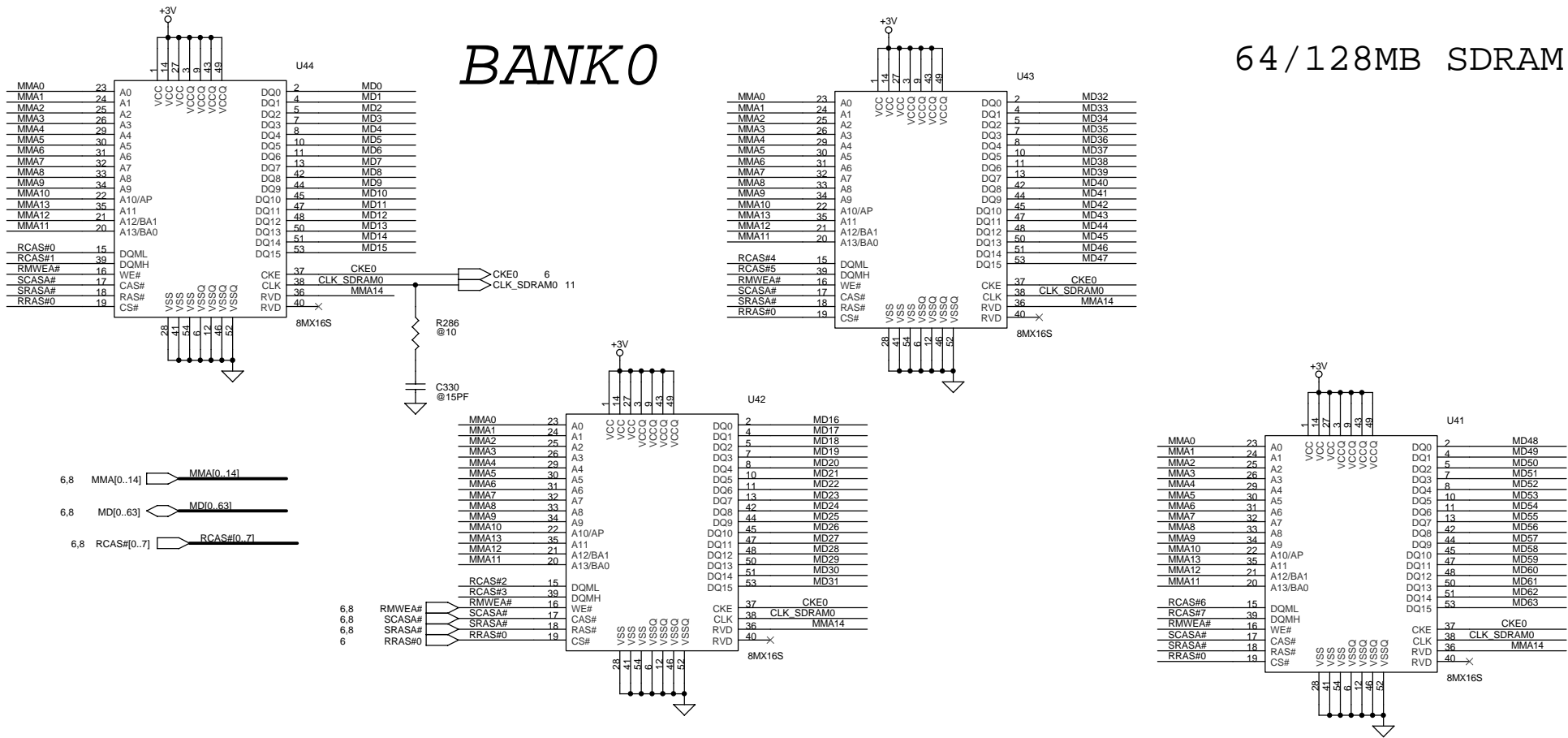
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Size	Document Number	Rev
Custom	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 6 of 34

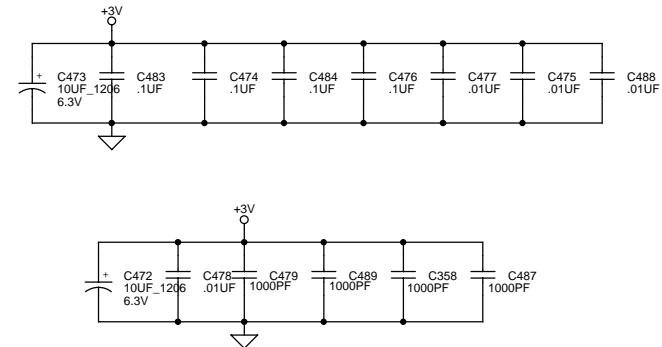
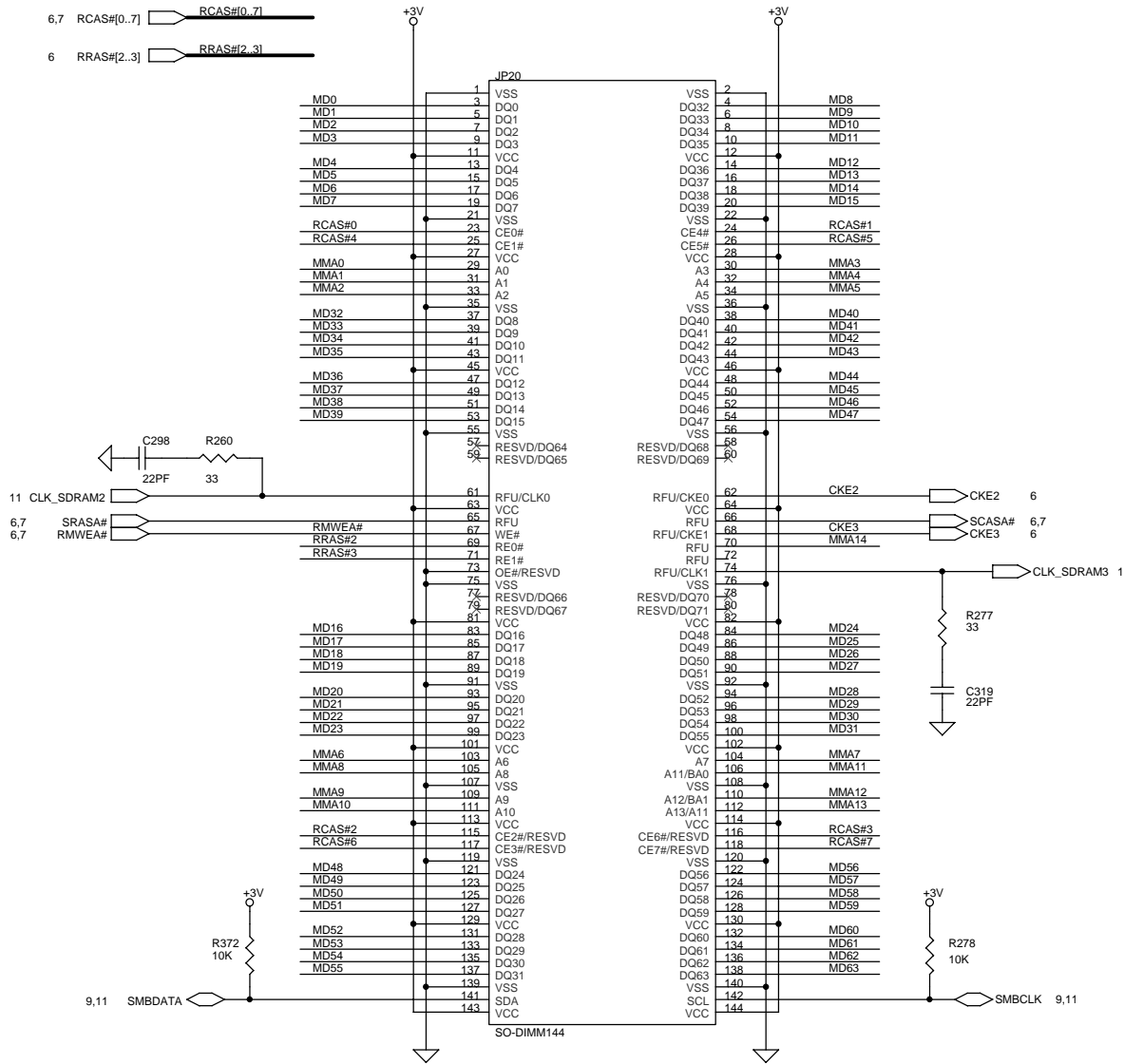
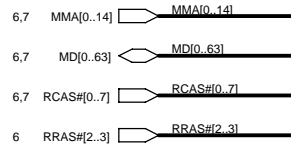
# BANK 0

# 64/128MB SDRAM



SO-DIMM 144 PINS  
RAM MODULE CONN.

# BANK 2 / 3



DIMM1

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Title  
SCHEMATIC, M/B LA-1281

Size  
B  
Document Number  
401202

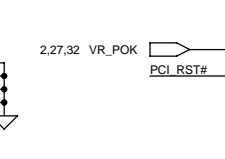
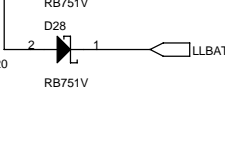
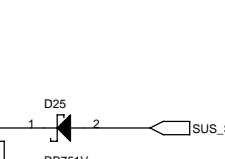
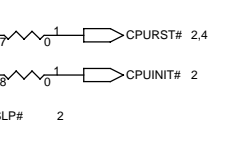
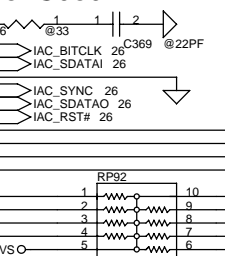
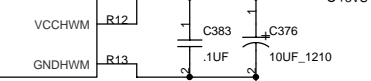
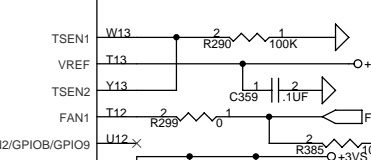
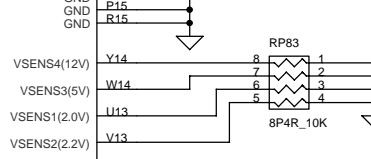
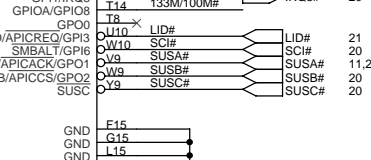
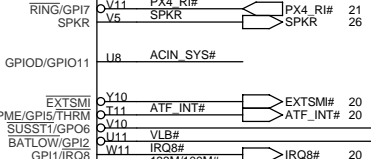
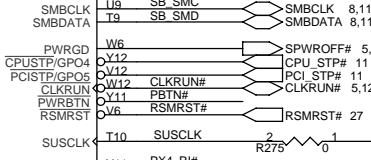
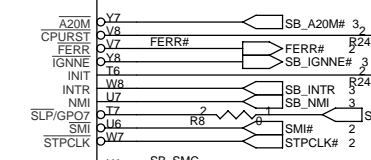
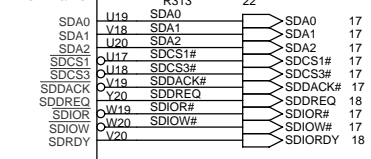
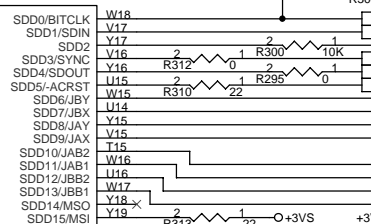
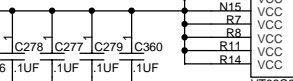
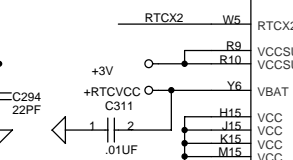
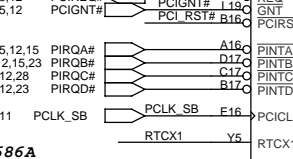
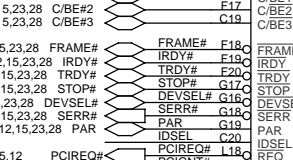
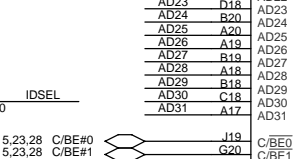
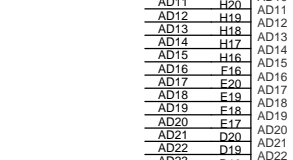
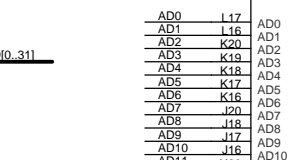
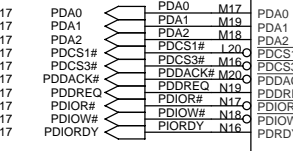
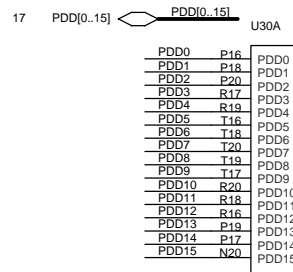
Rev  
1B

Date: 星期一, 十月 22, 2001

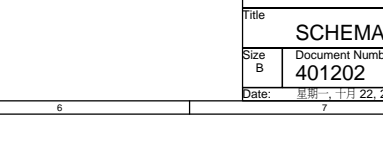
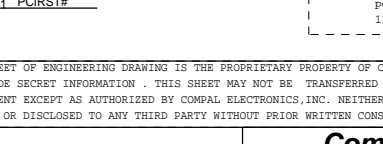
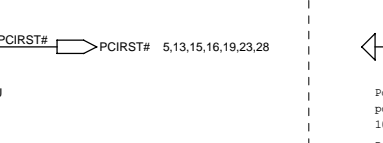
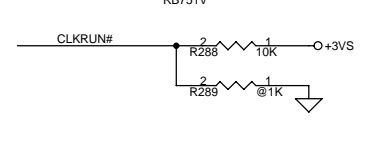
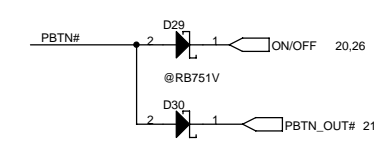
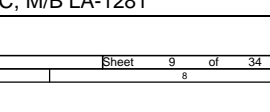
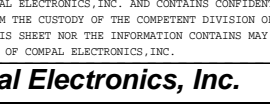
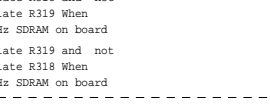
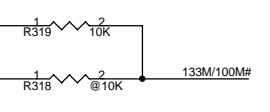
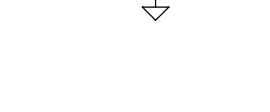
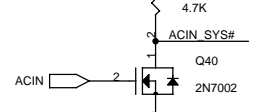
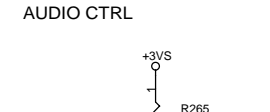
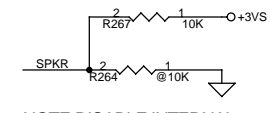
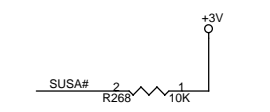
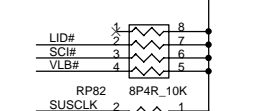
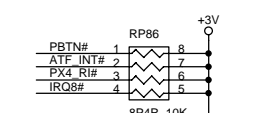
Sheet 8 of 34



# VT82C686A-A



## Signals Pullup



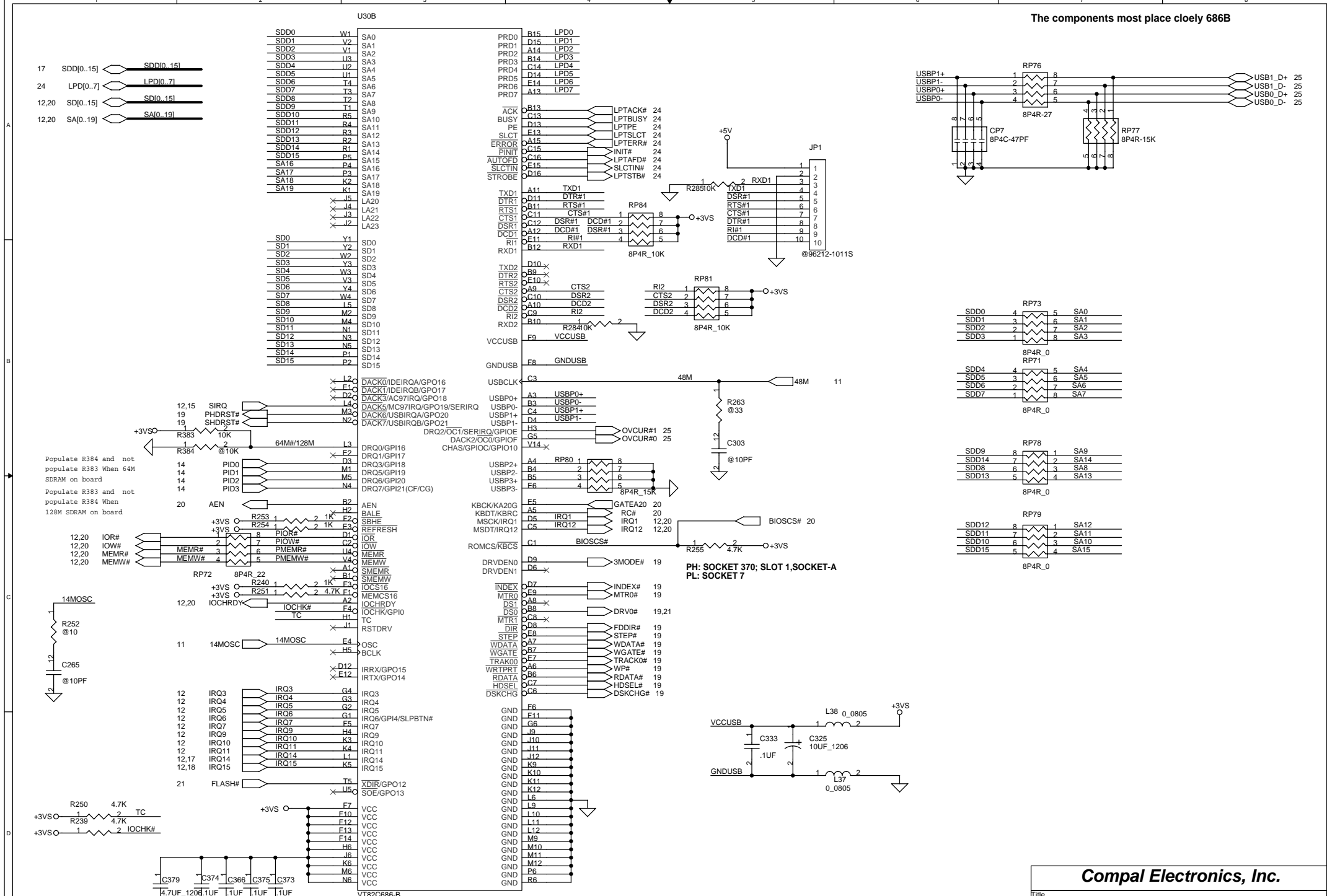
NOTE:DISABLE INTERNAL AUDIO CTRL

Populate R318 and not populate R319 when 100MHz SDRAM on board  
Populate R319 and not populate R318 when 133MHz SDRAM on board

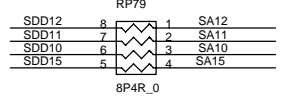
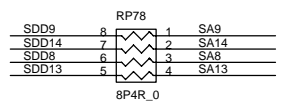
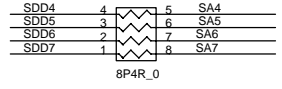
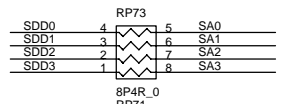
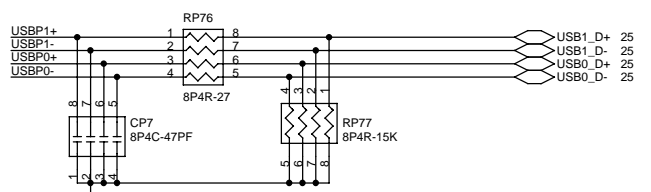
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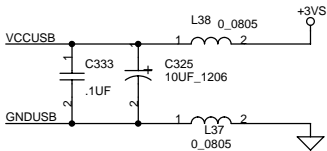
Title	SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev
B	401202	1B
Date:	星期三, 十月 22, 2001	Sheet 9 of 34



**The components most place cloely 686B**



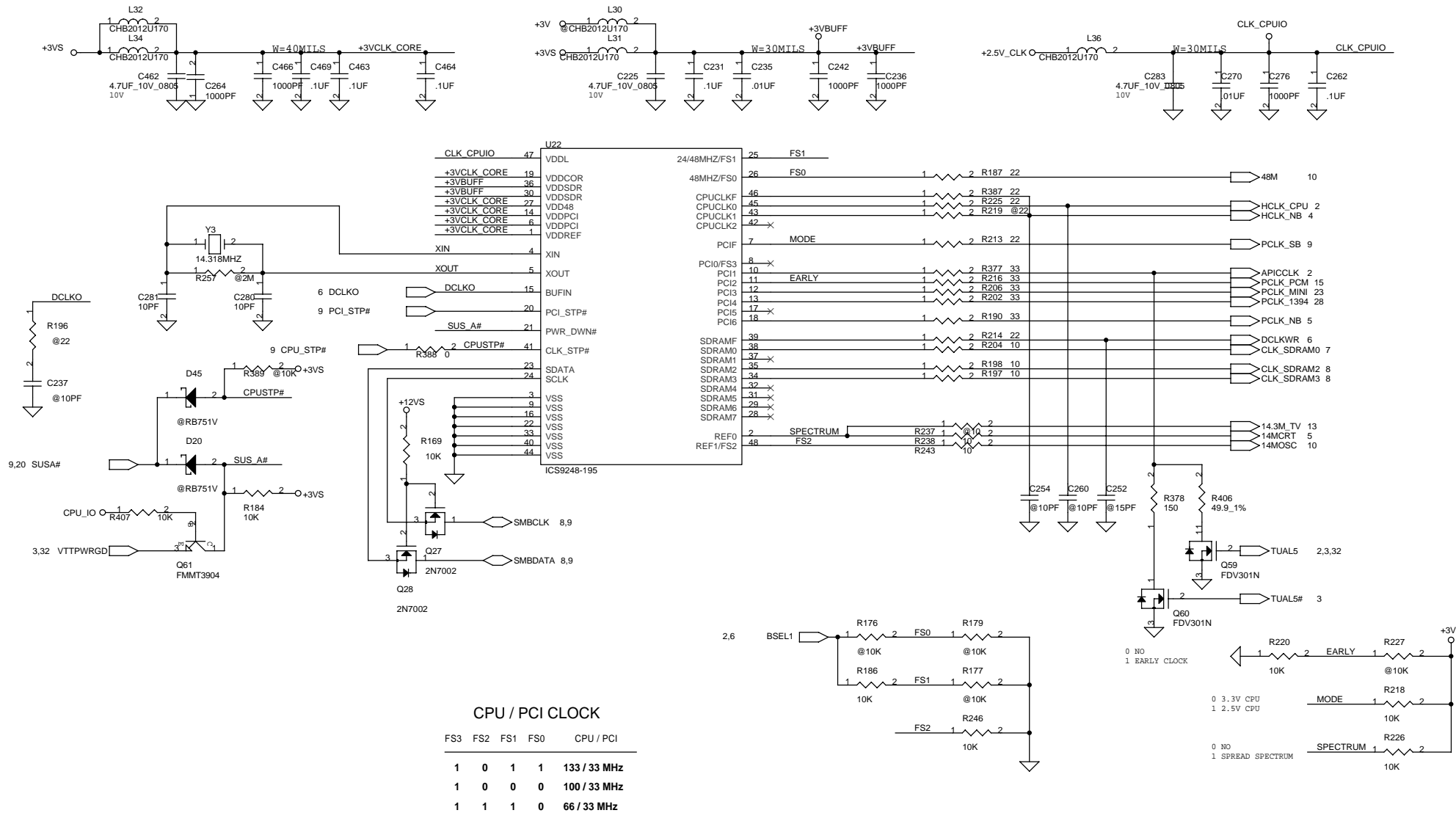
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PL: SOCKET 7**



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Title <b>SCHEMATIC, M/B LA-1281</b>		
Size <b>B</b>	Document Number <b>401202</b>	Rev <b>1B</b>
Date: <b>星期二十月 22, 2001</b>	Sheet <b>10</b>	of <b>34</b>

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# CLOCK GENERATOR & BUFFER



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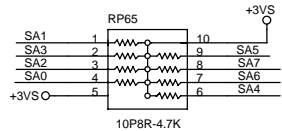
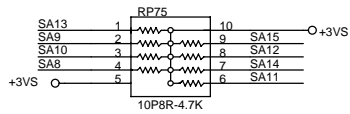
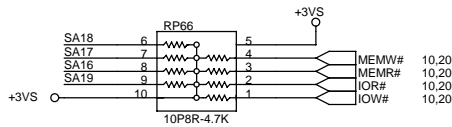
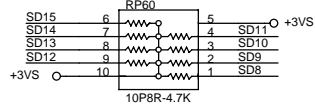
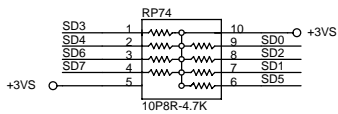
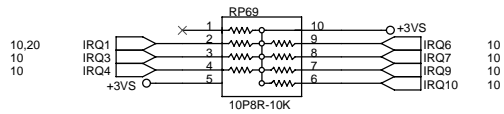
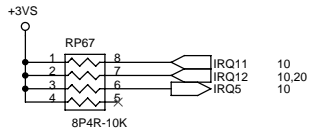
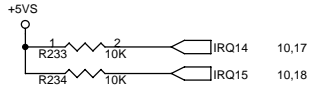
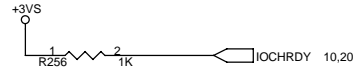
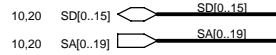
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Size: Document Number: 401202 Rev: 1B

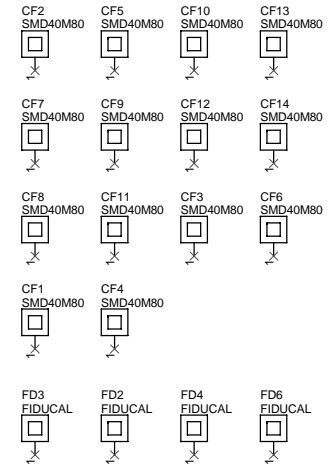
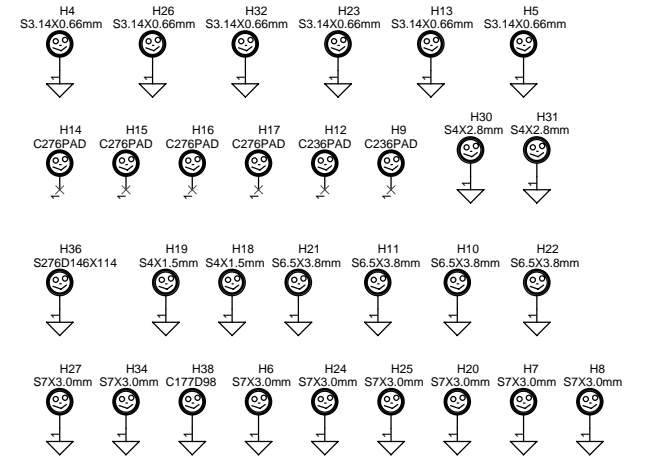
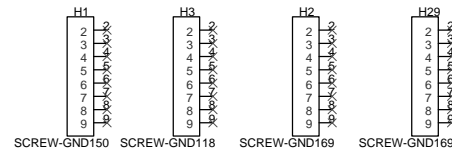
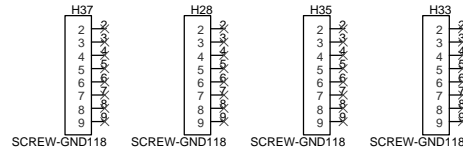
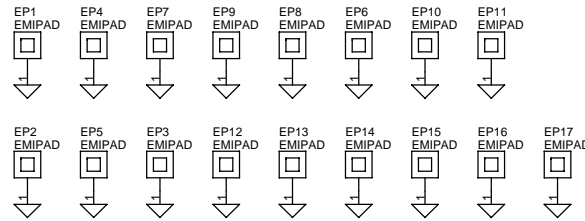
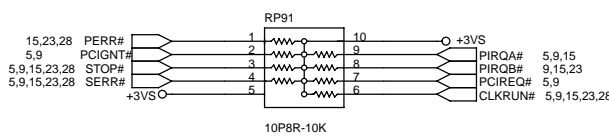
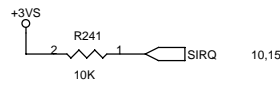
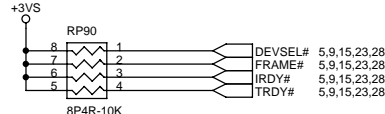
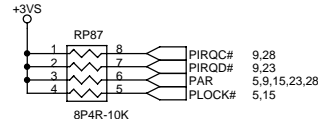
Date: 星期一, 十月 22, 2001 Sheet 11 of 34

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# ISA BUS Pullup



# PCI BUS Pullup

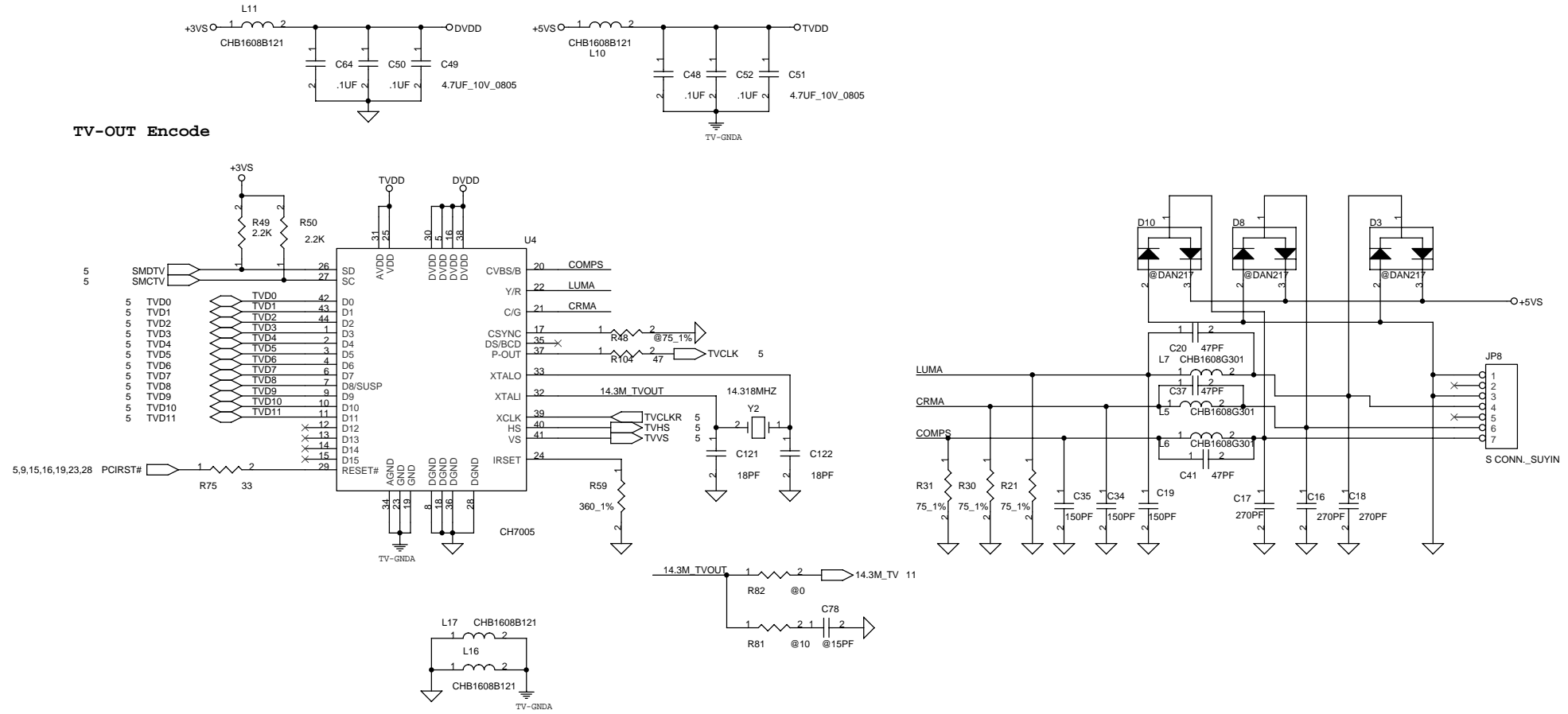


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Title	SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 12 of 34

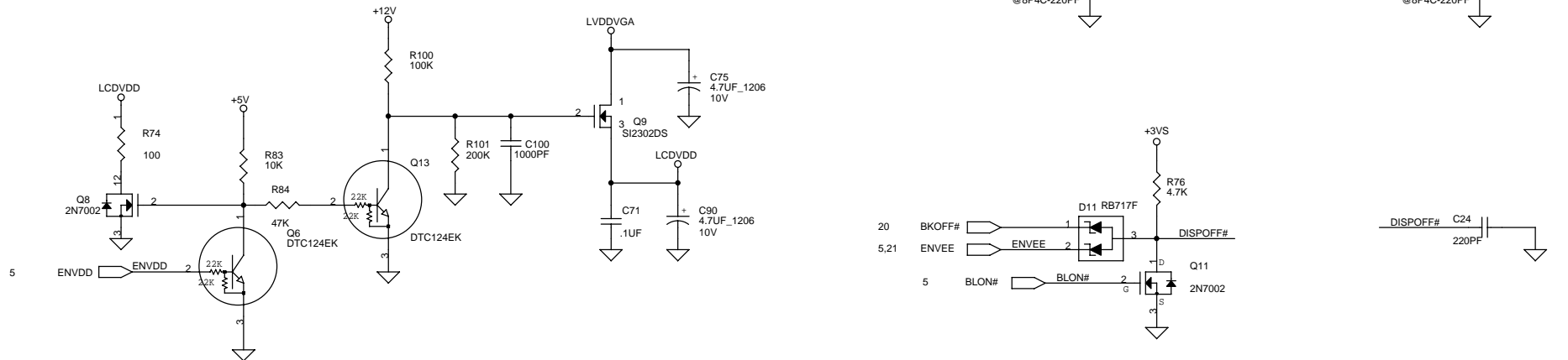
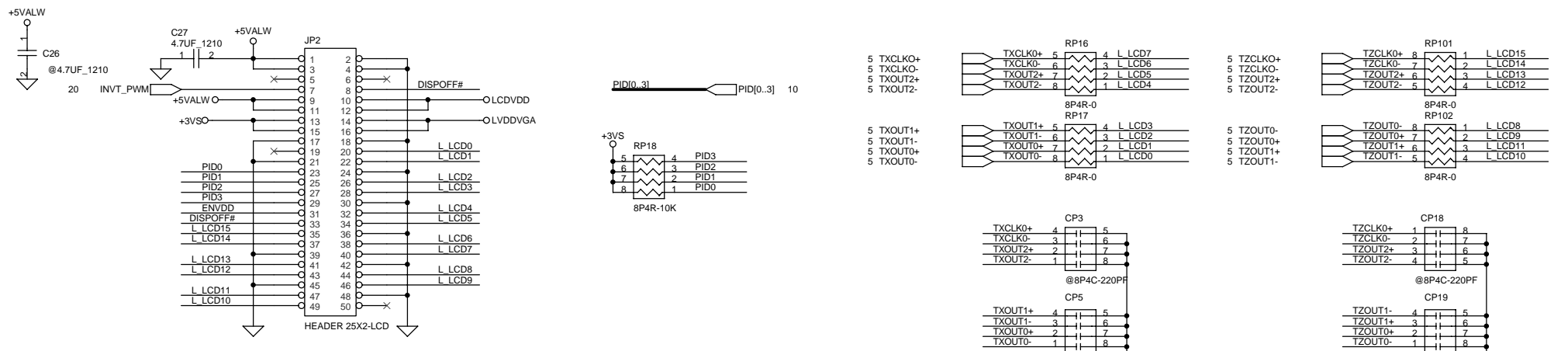
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**TV-OUT Encode**

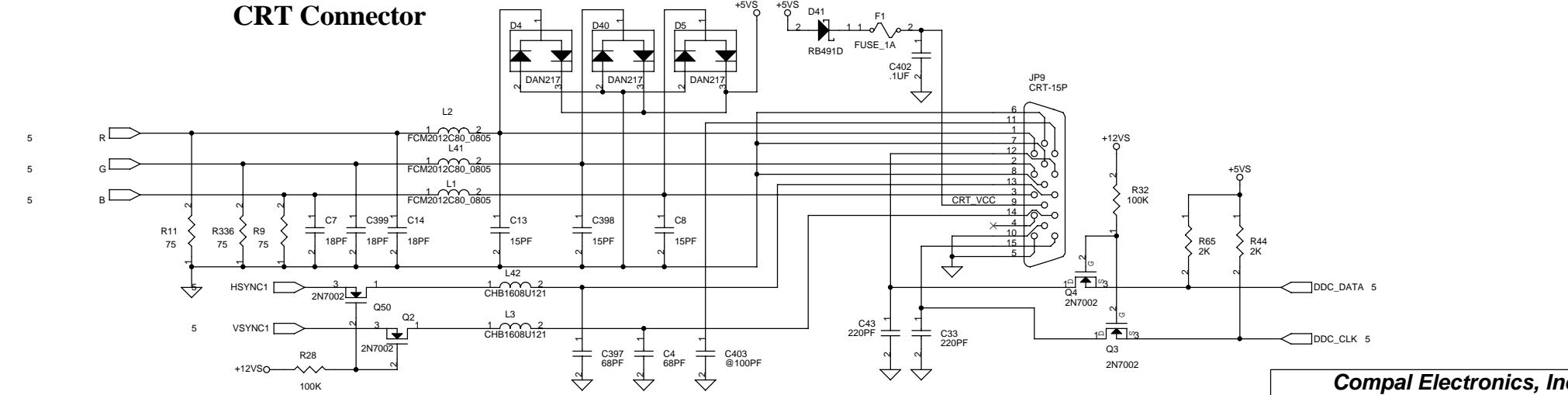


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Title	SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 13 of 34



**CRT Connector**



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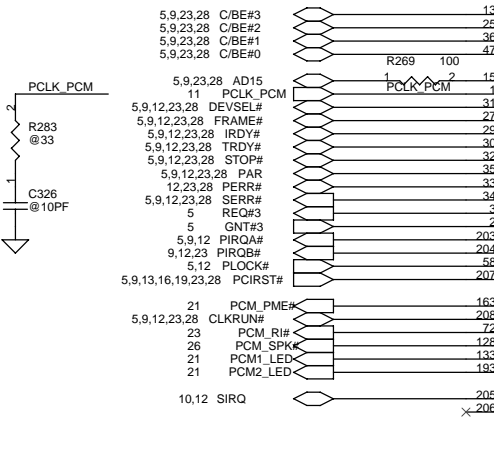
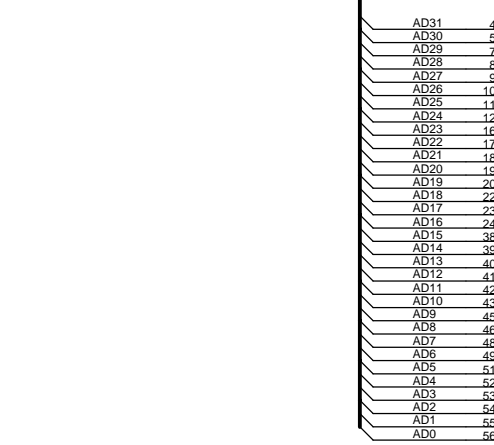
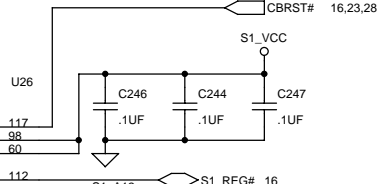
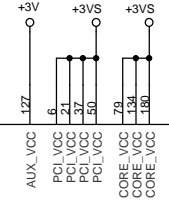
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Title <b>SCHEMATIC, M/B LA-1281</b>		
Size B	Document Number <b>401202</b>	Rev 1B
Date: 星期一, 十月 22, 2001	Sheet 14 of 34	

S1\_IOWR# S1\_IOWR# 16  
 S1\_IORD# S1\_IORD# 16  
 S1\_CE# S1\_CE# 16  
 S1\_CE2# S1\_CE2# 16

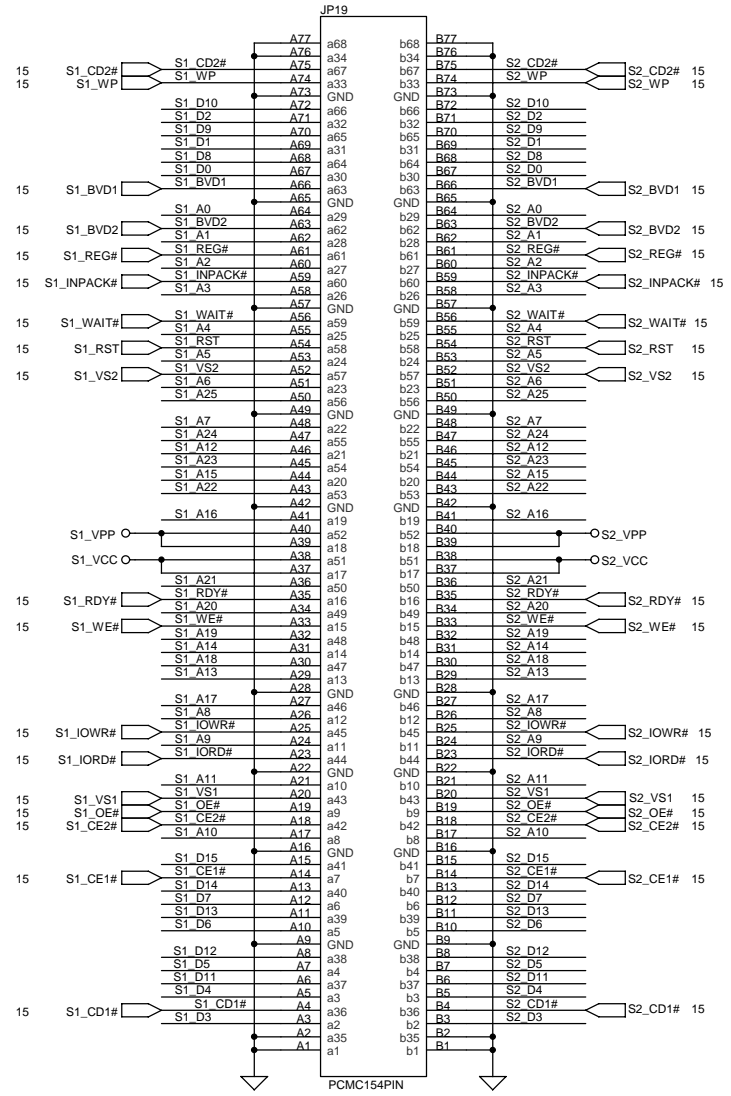
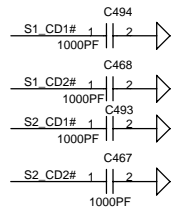
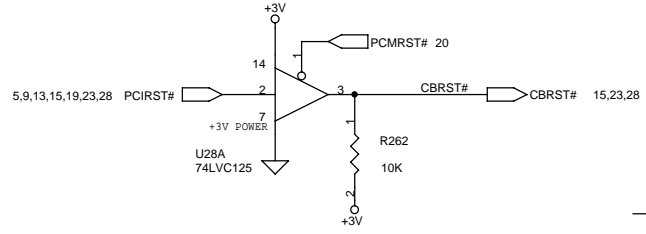
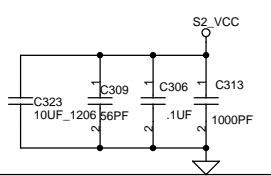
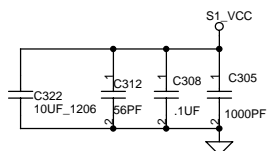
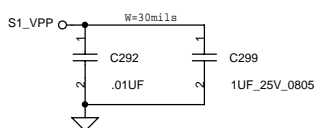
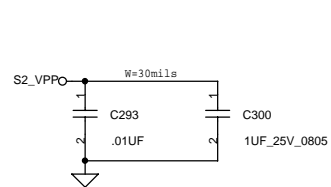
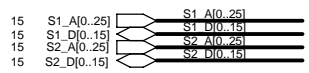
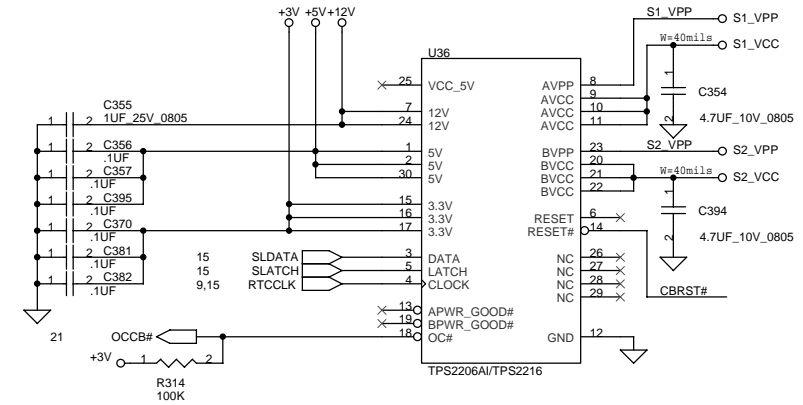
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 S1\_D[0..15] S1\_D[0..15] 16

# CardBus Controller OZ6933T (TQFP)

5,9,23,28 AD[0..31]



# CARDBUS SOCKET

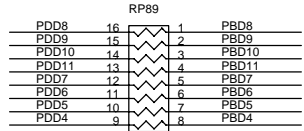
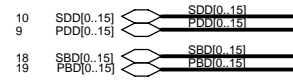


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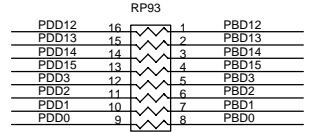
<b>Compal Electronics, Inc.</b>		
Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 16 of 34



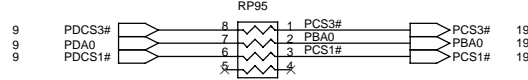
**IDE Series Resistor**  
Place them close SB



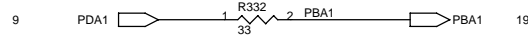
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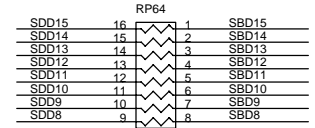
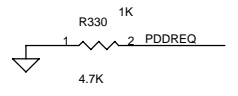
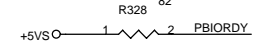
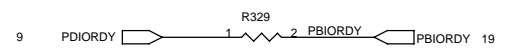
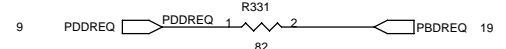
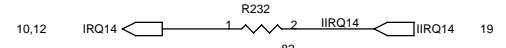
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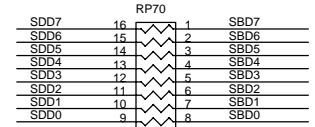
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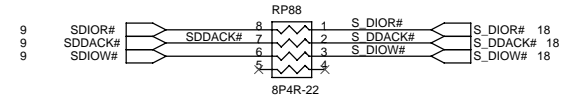
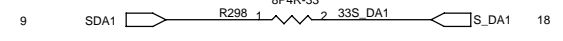
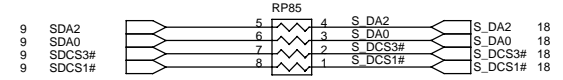
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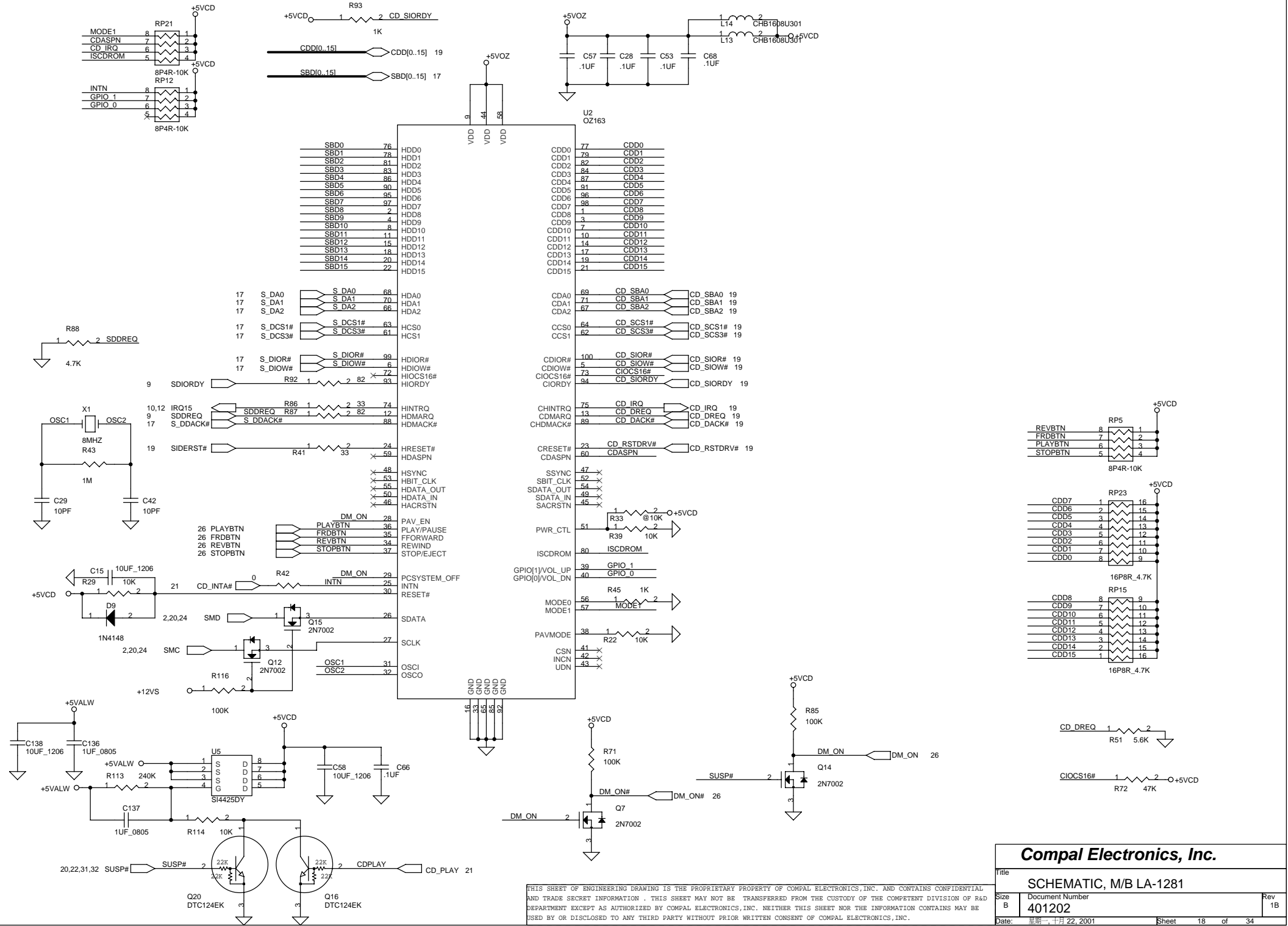
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8P4R-22

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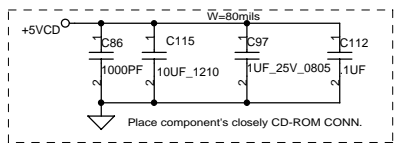
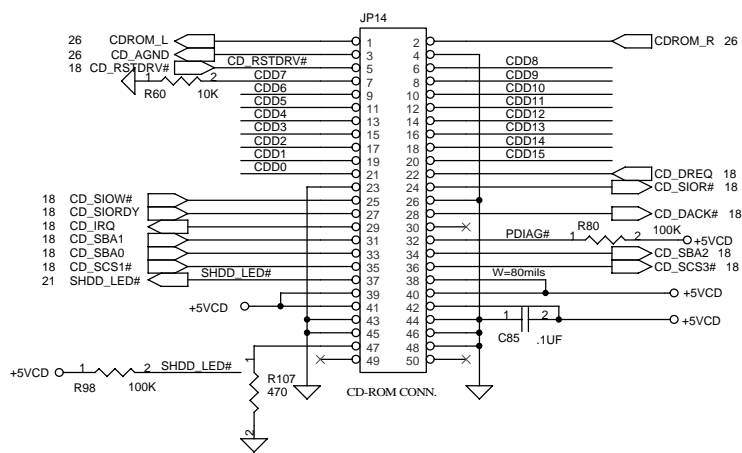
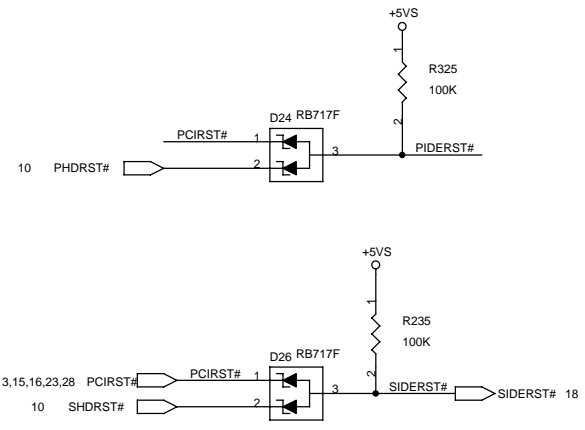
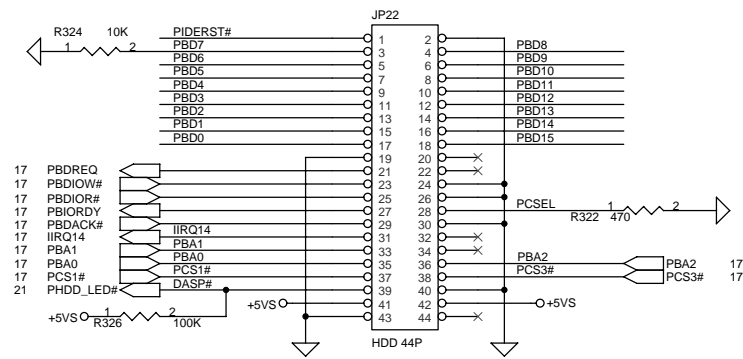
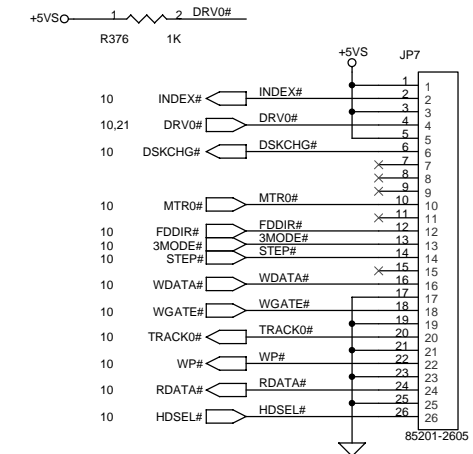
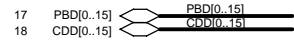
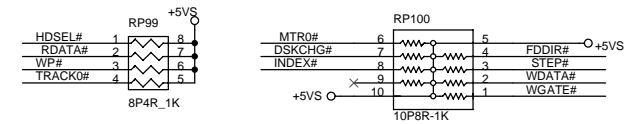
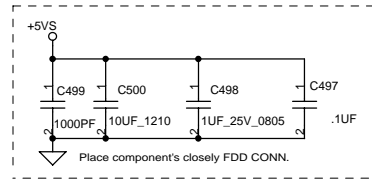
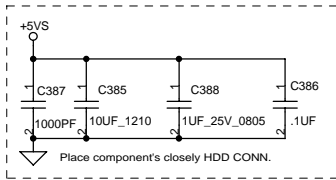
<b>Compal Electronics, Inc.</b>		
Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 17 of 34



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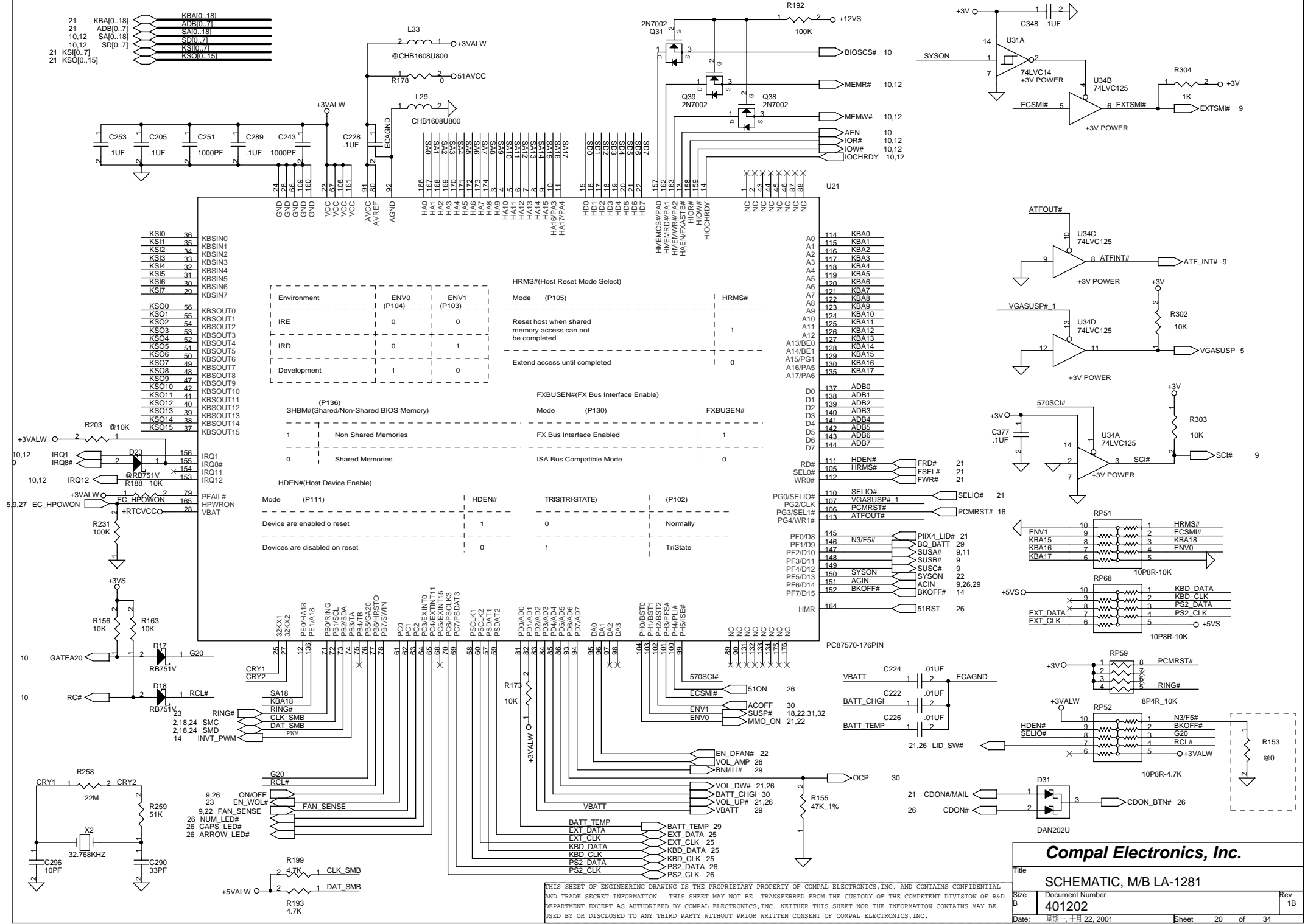
<b>Compal Electronics, Inc.</b>		
Title: SCHEMATIC, M/B LA-1281		
Size B	Document Number: 401202	Rev 1B
Date: 星期一, 十月 22, 2001	Sheet 18	of 34

# IDE, CD-ROM & FDD Module CONN.



<b>Compal Electronics, Inc.</b>		
Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 19 of 34

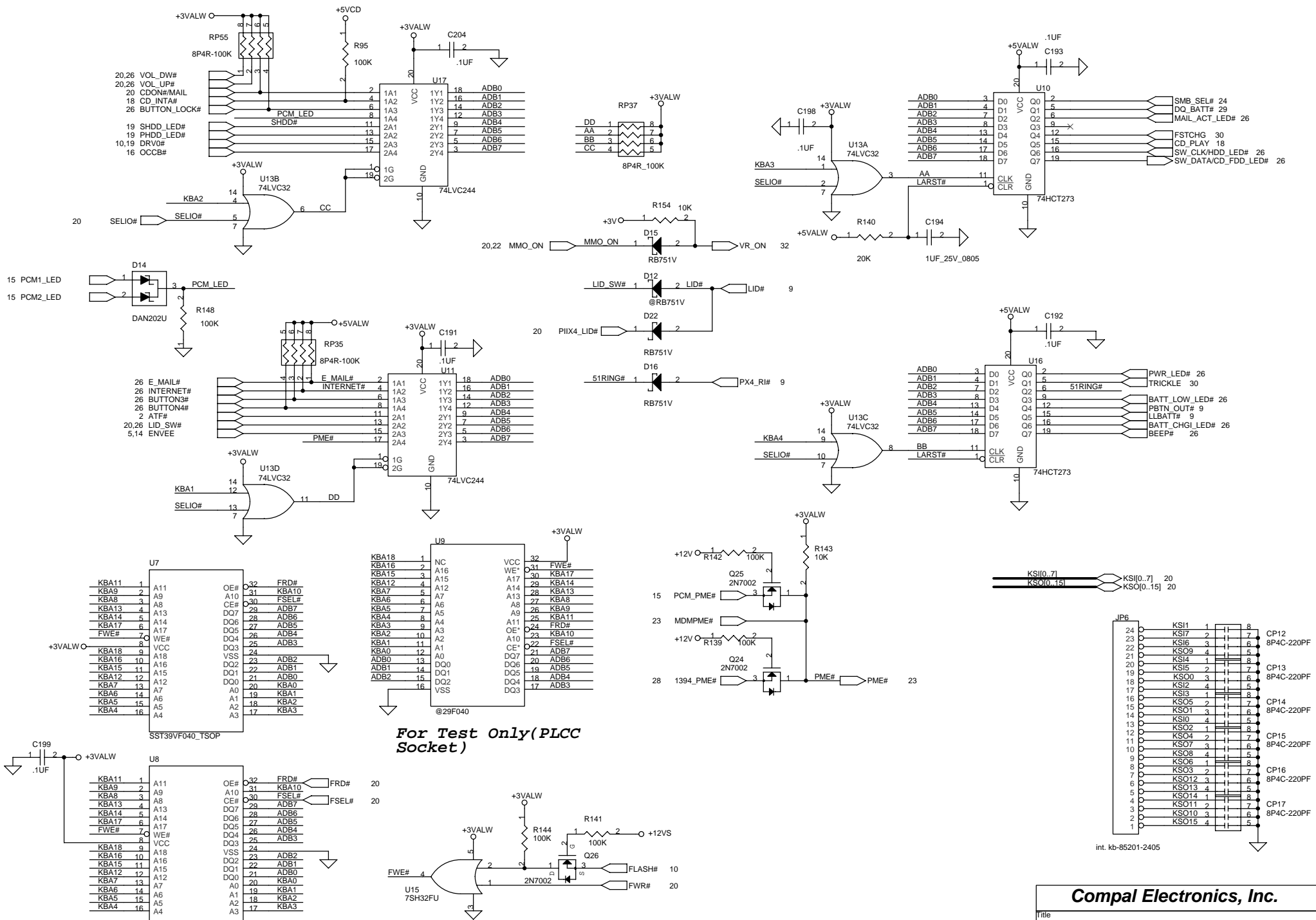
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Title	SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 20 of 34

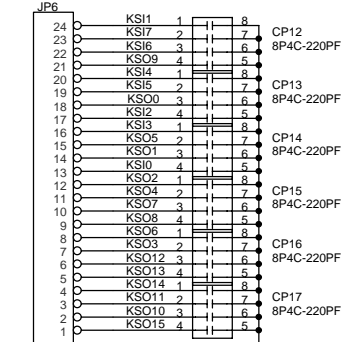
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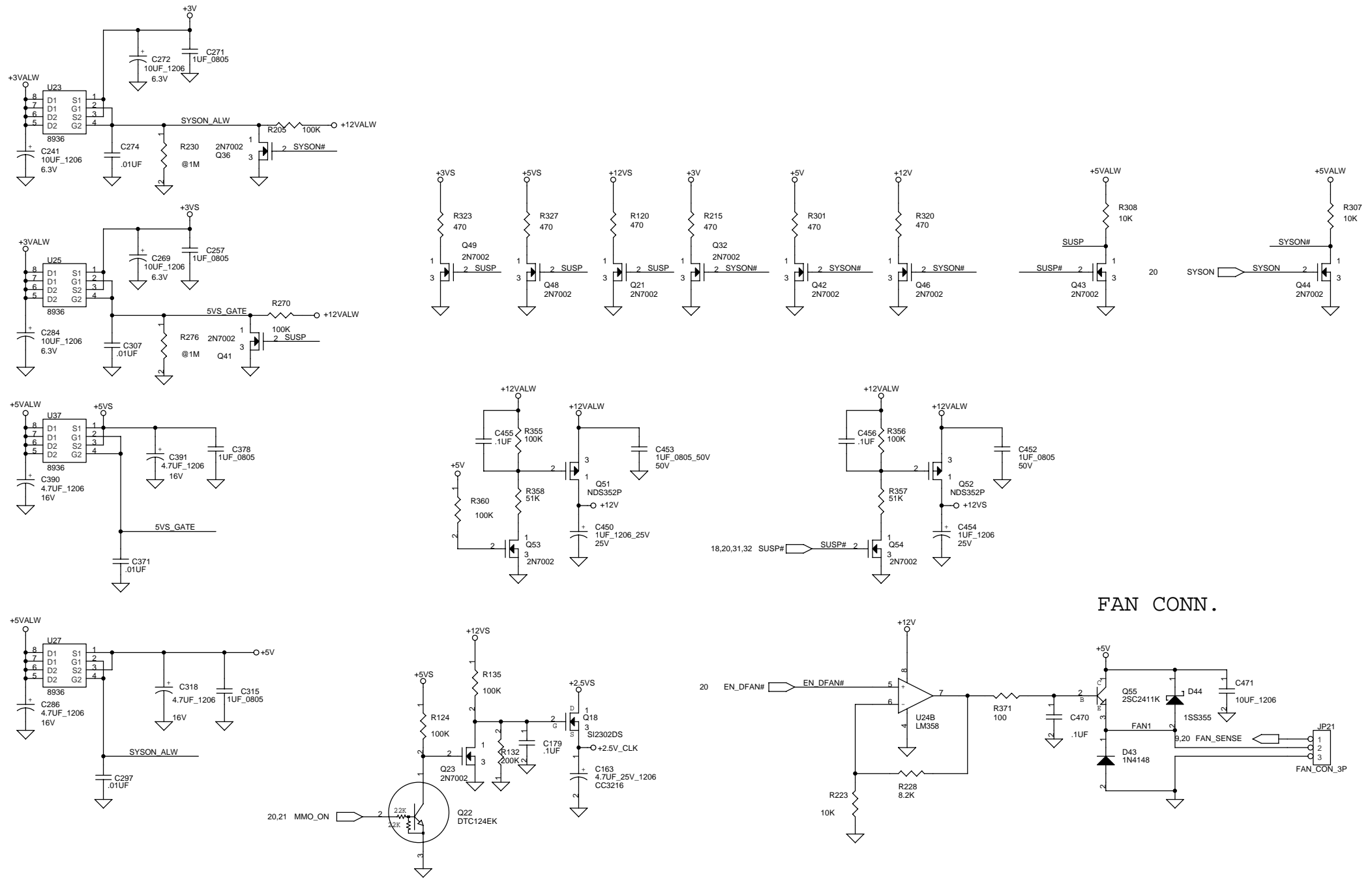
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<b>Compal Electronics, Inc.</b>	
Title: SCHEMATIC, M/B LA-1281	
Size: B	Document Number: 401202
Date: 星期一, 十月 22, 2001	Sheet: 21 of 34



int. kb-85201-2405

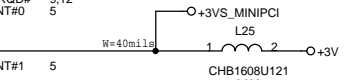
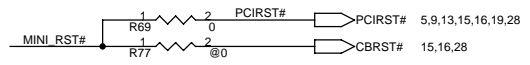
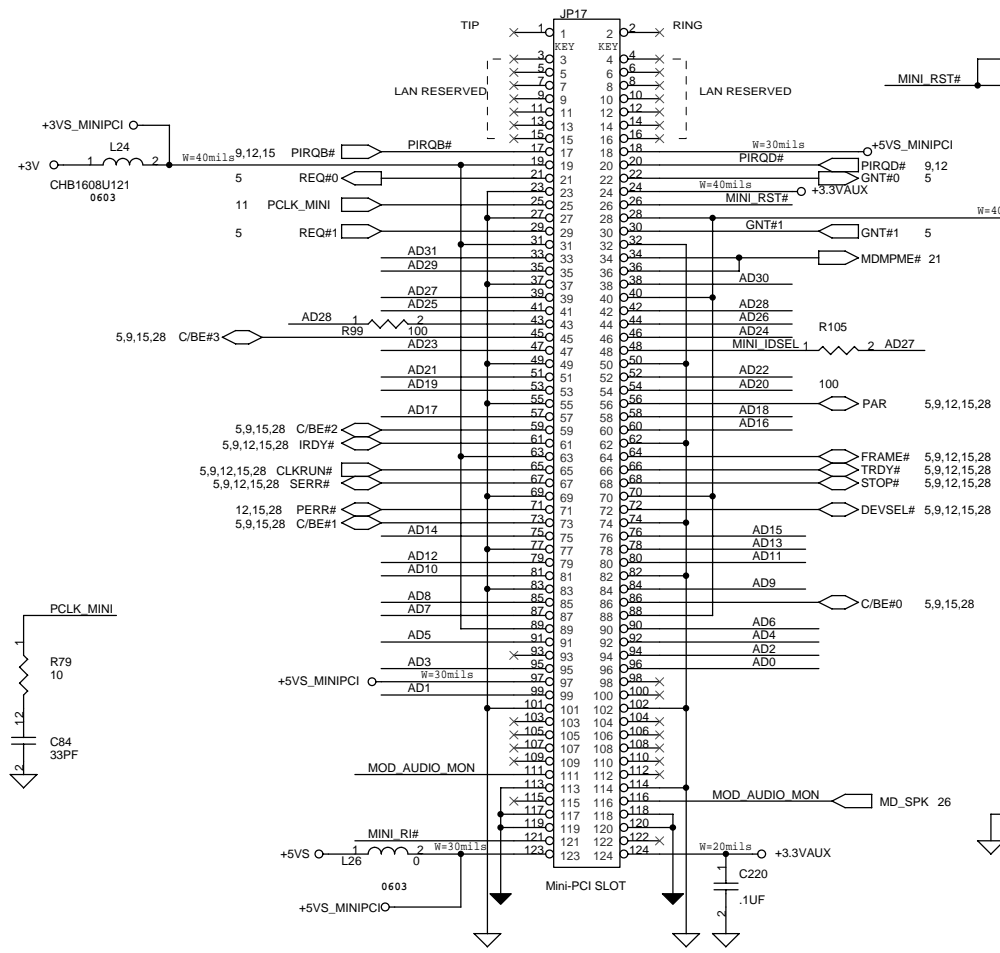
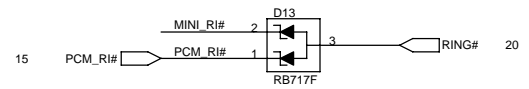
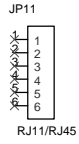
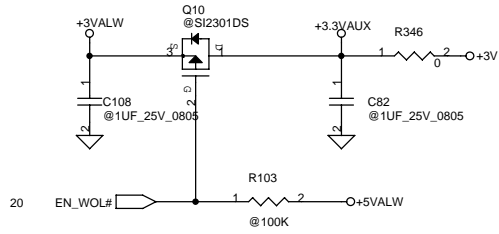


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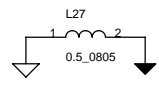
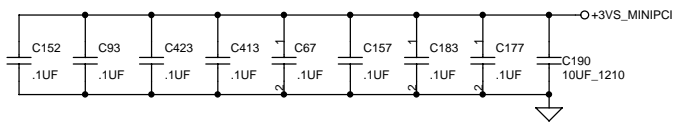
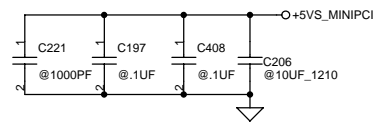
Title: SCHEMATIC, M/B LA-1281

Size	Document Number	Rev
B	401202	1B
Date:	日期: 十月 22, 2001	Sheet 22 of 34

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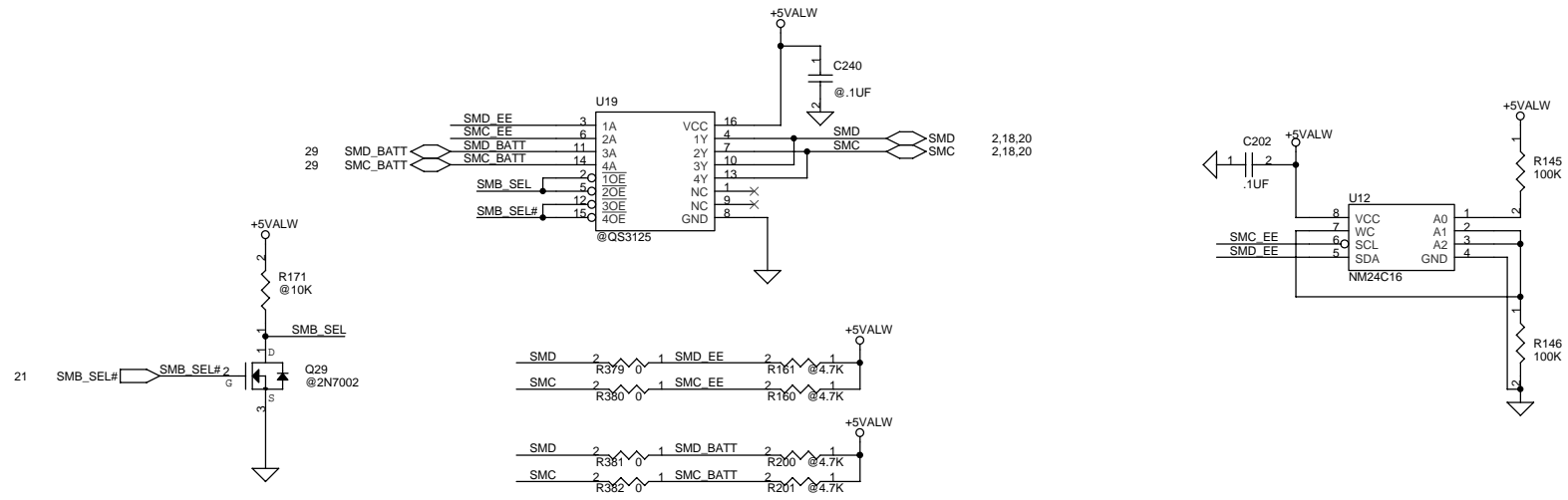
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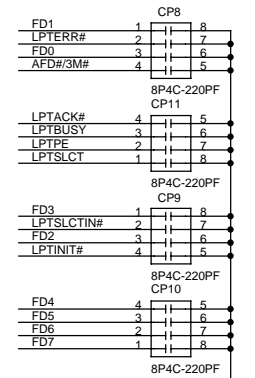
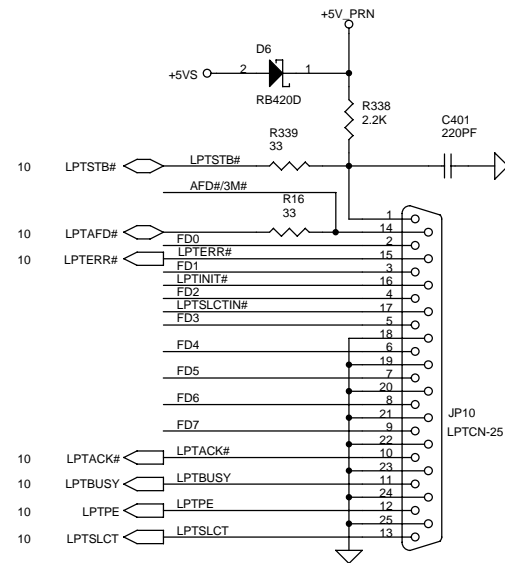
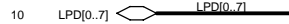
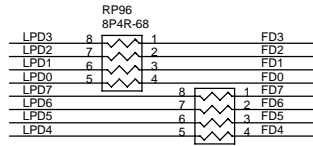
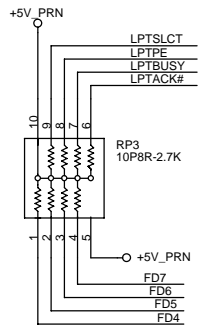
ADIO.31 ADIO.31 5,9,15,28

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Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 23 of 34



### PARALLEL PORT



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title SCHEMATIC, M/B LA-1281

Size Document Number 401202

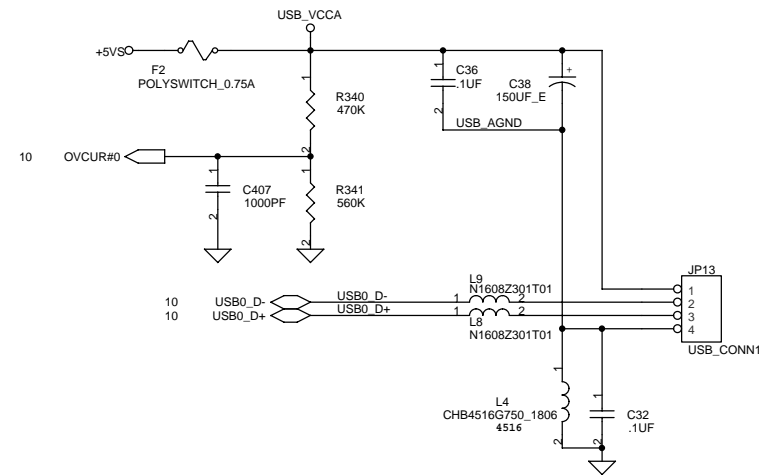
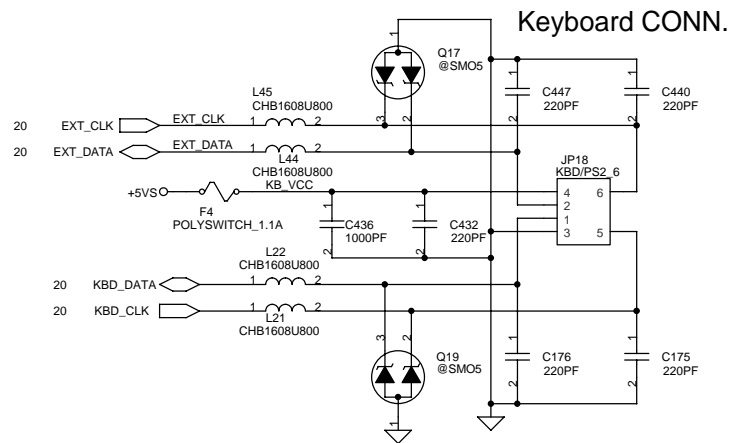
Rev 1B

Date: 星期一, 十月 22, 2001

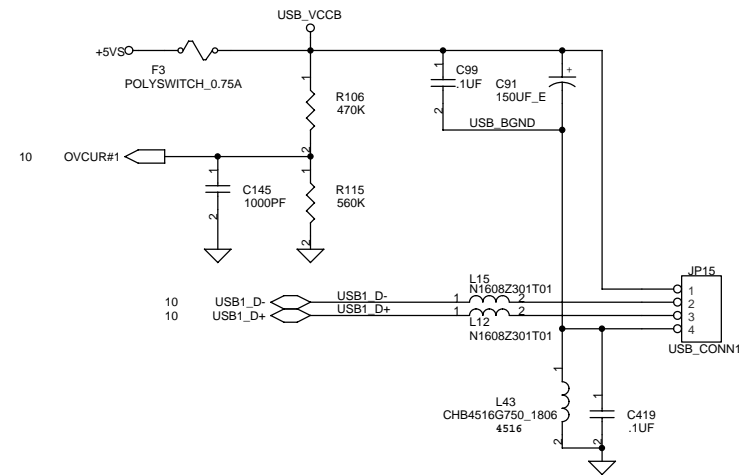
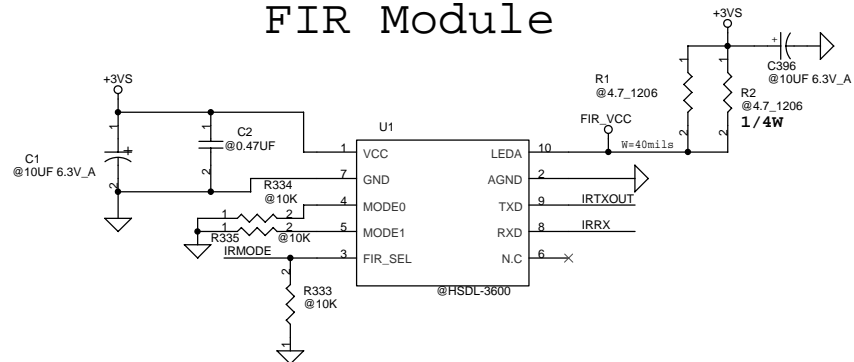
Sheet 24 of 34

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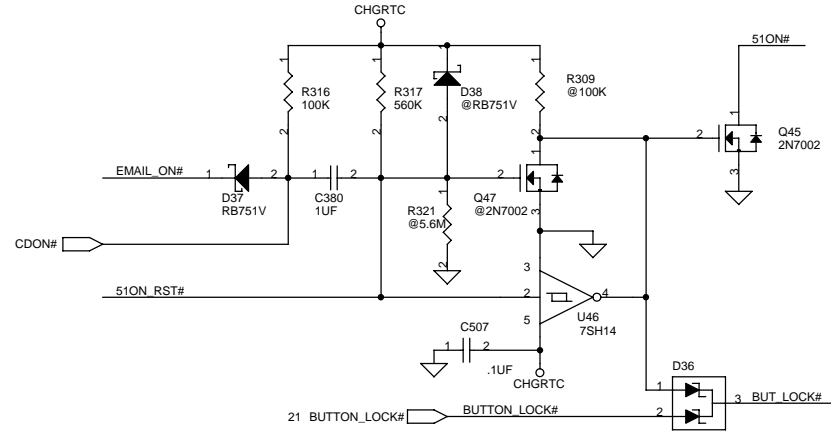
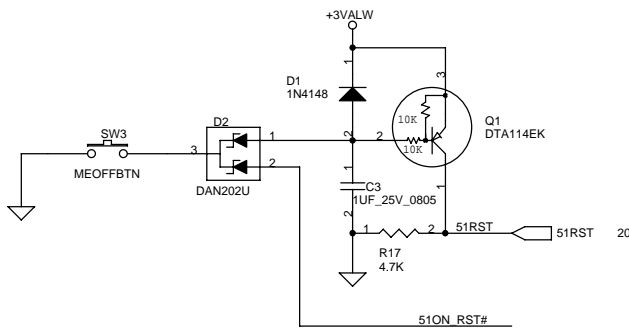
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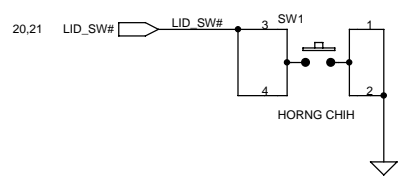
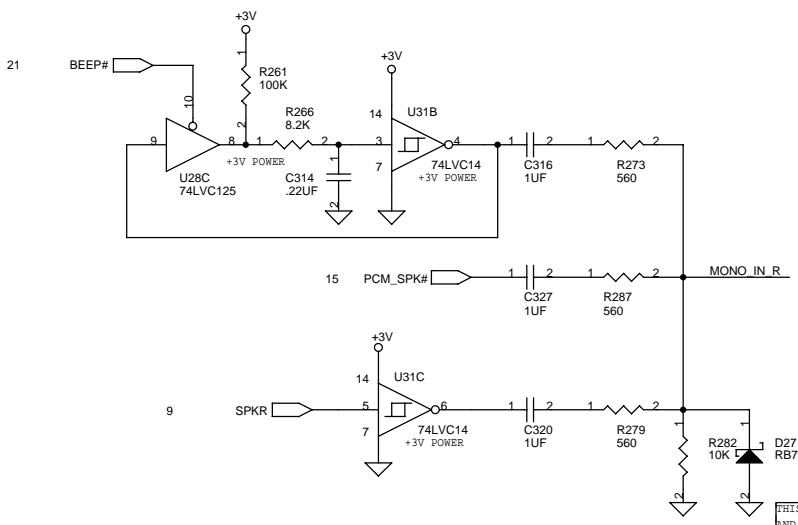
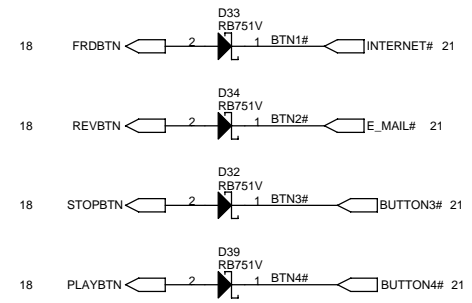
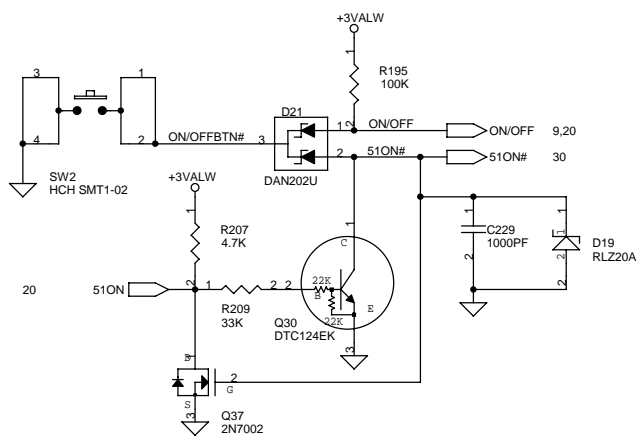
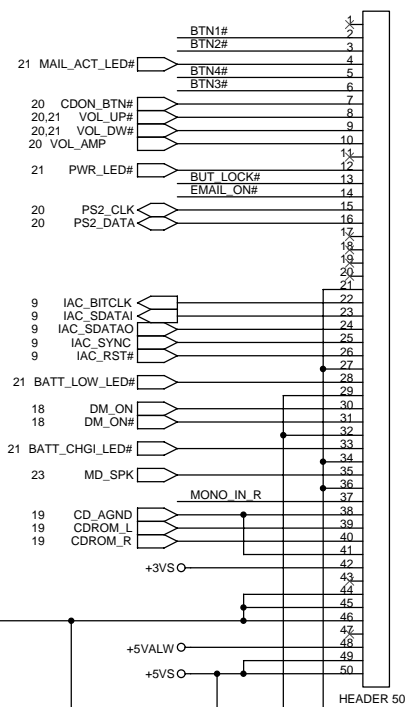
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Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 25 of 34

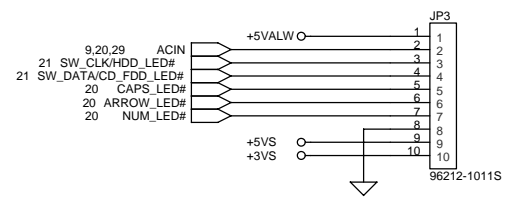
### Reset Button



CDON\_BTN# is Low , enable CD\_PLAY  
MAIL is High , enable  
MAIL



### System Window Connector



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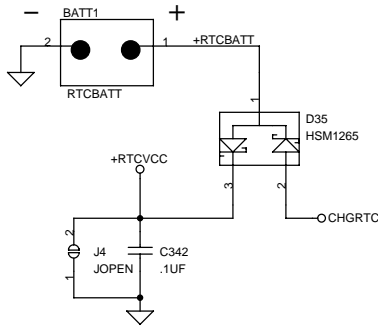
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Title: SCHEMATIC, M/B LA-1281

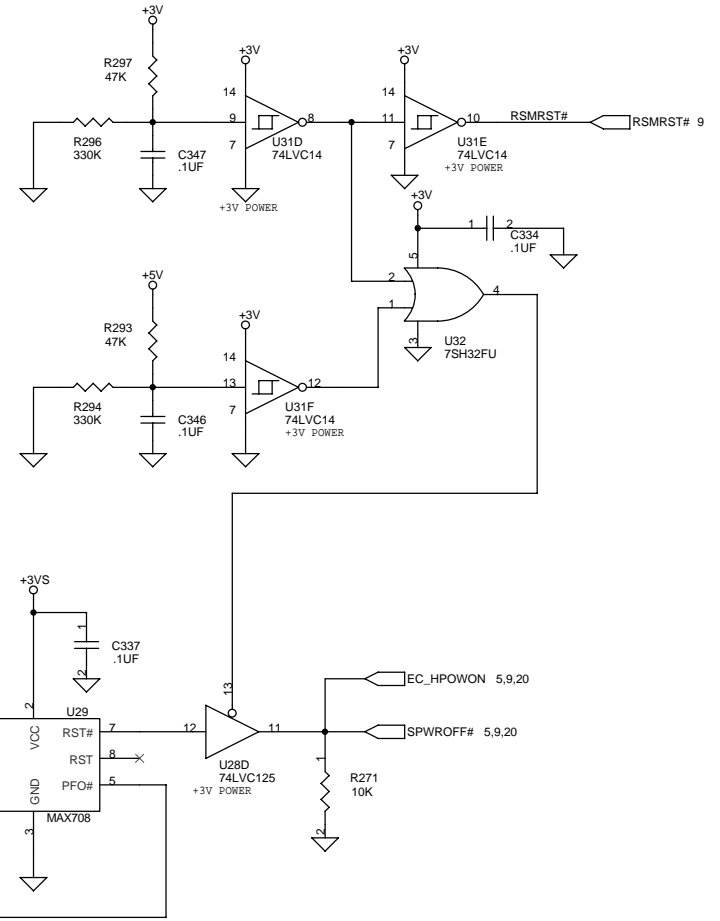
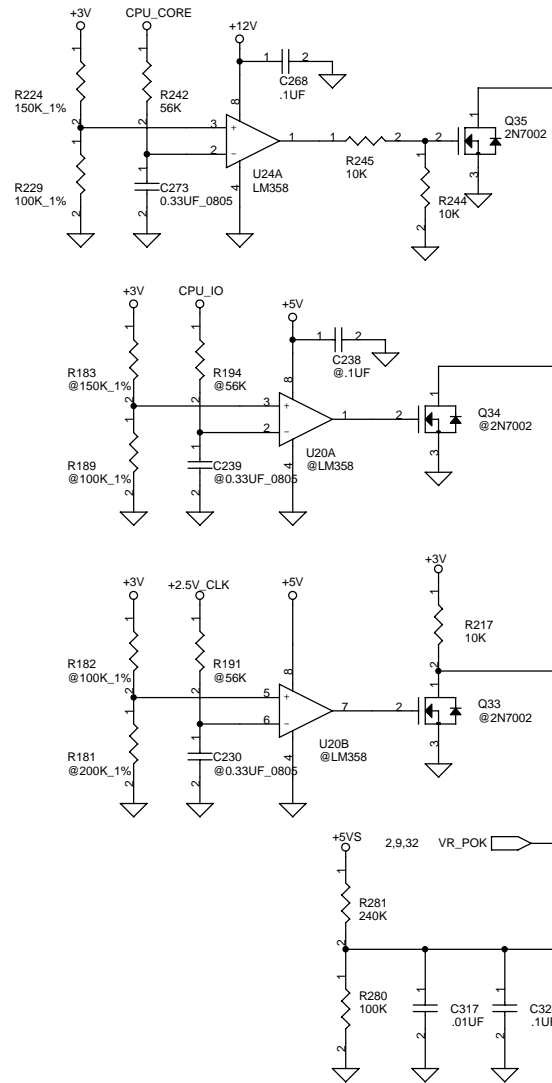
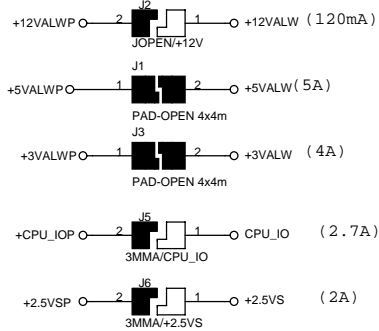
Size: B Document Number: 401202 Rev: 1B

Date: 星期一, 十月 22, 2001 Sheet: 26 of 34

# RTC BATT



# DC/DC INTERFACE



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Title: SCHEMATIC, M/B LA-1281

Size B Document Number 401202

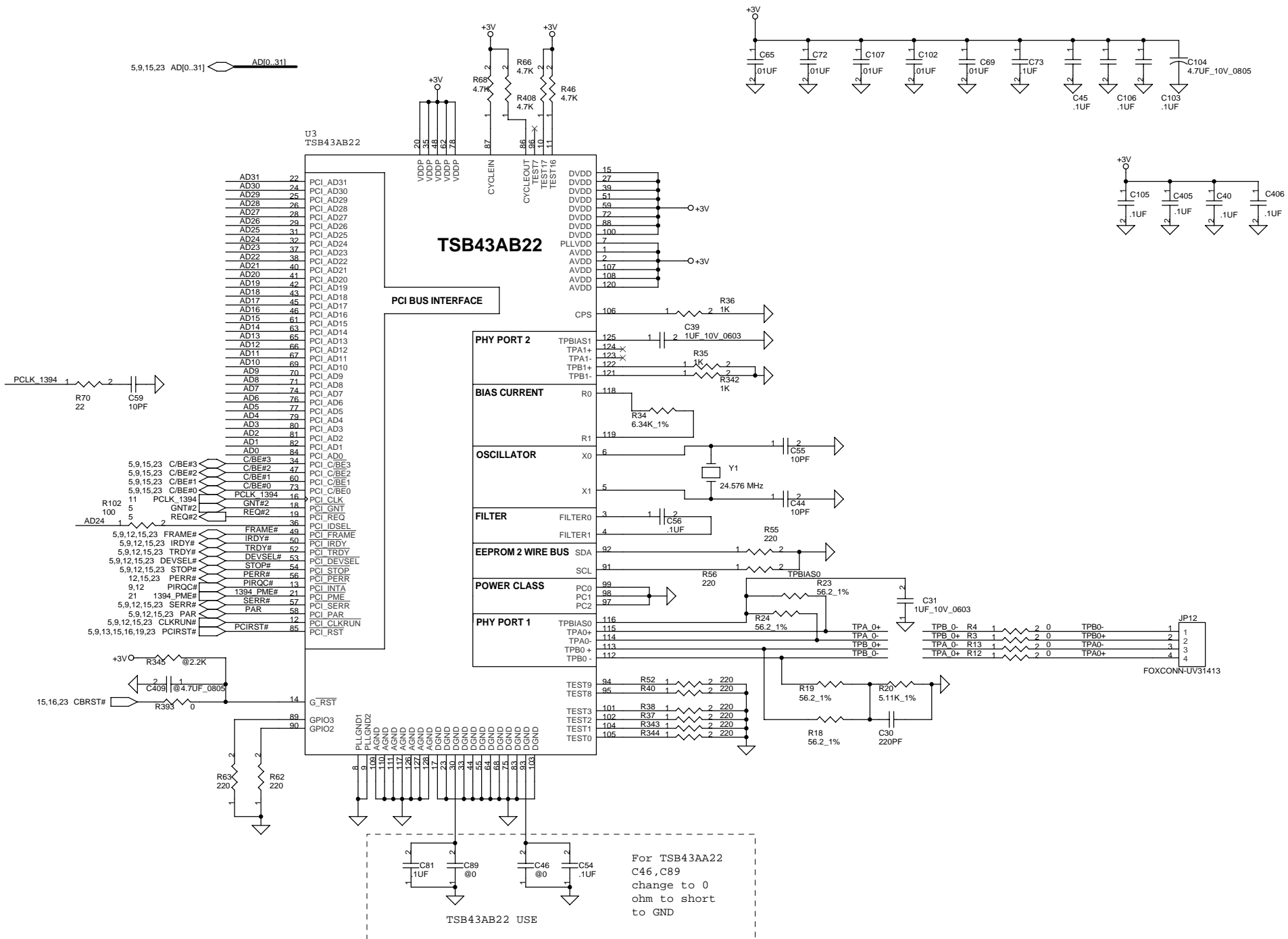
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Date: 星期一, 十月 22, 2001

Sheet 27 of 34

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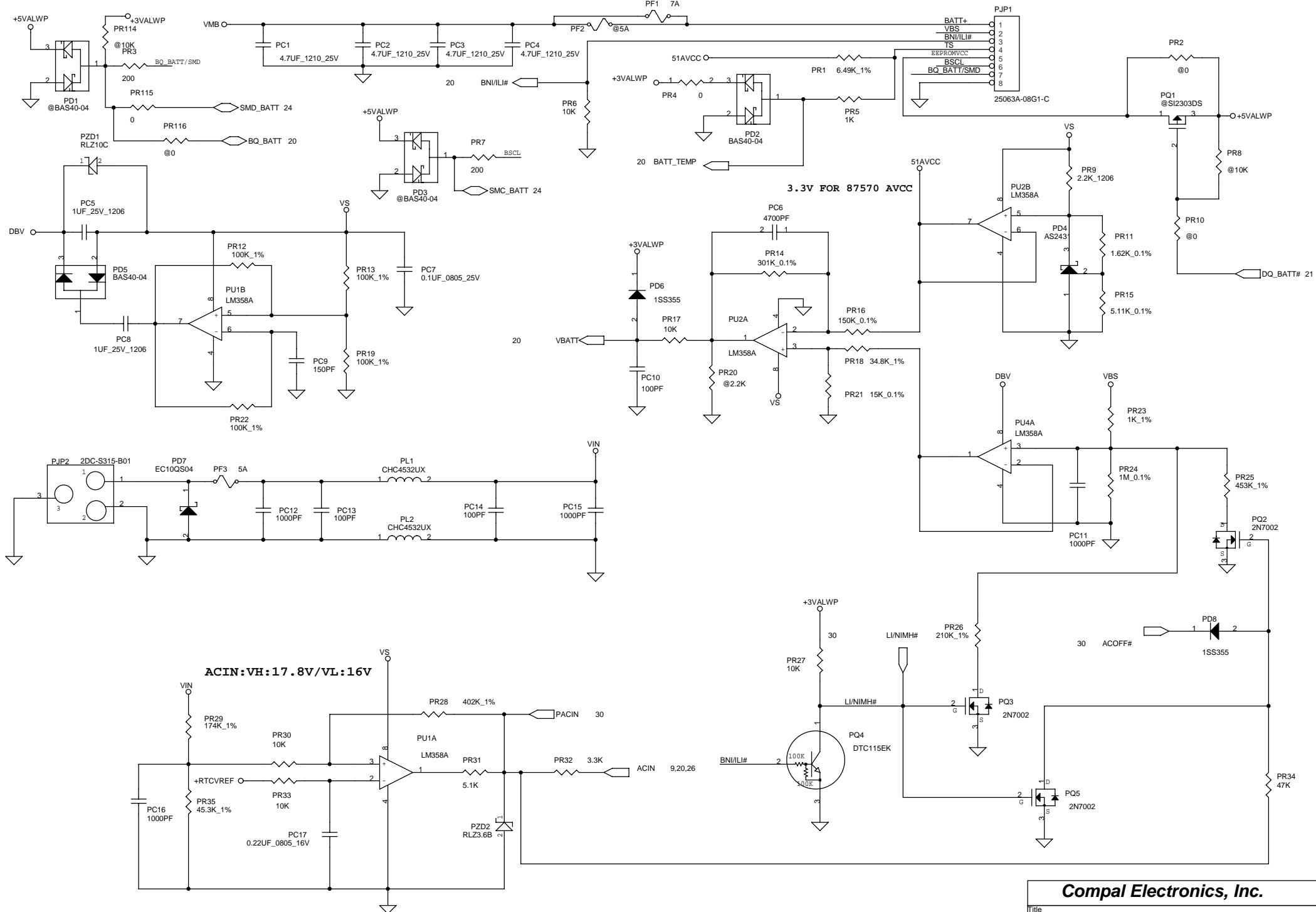


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Size B	Document Number <b>401202</b>	Rev 1B
Date:	星期一, 十月 22, 2001	Sheet 28 of 34

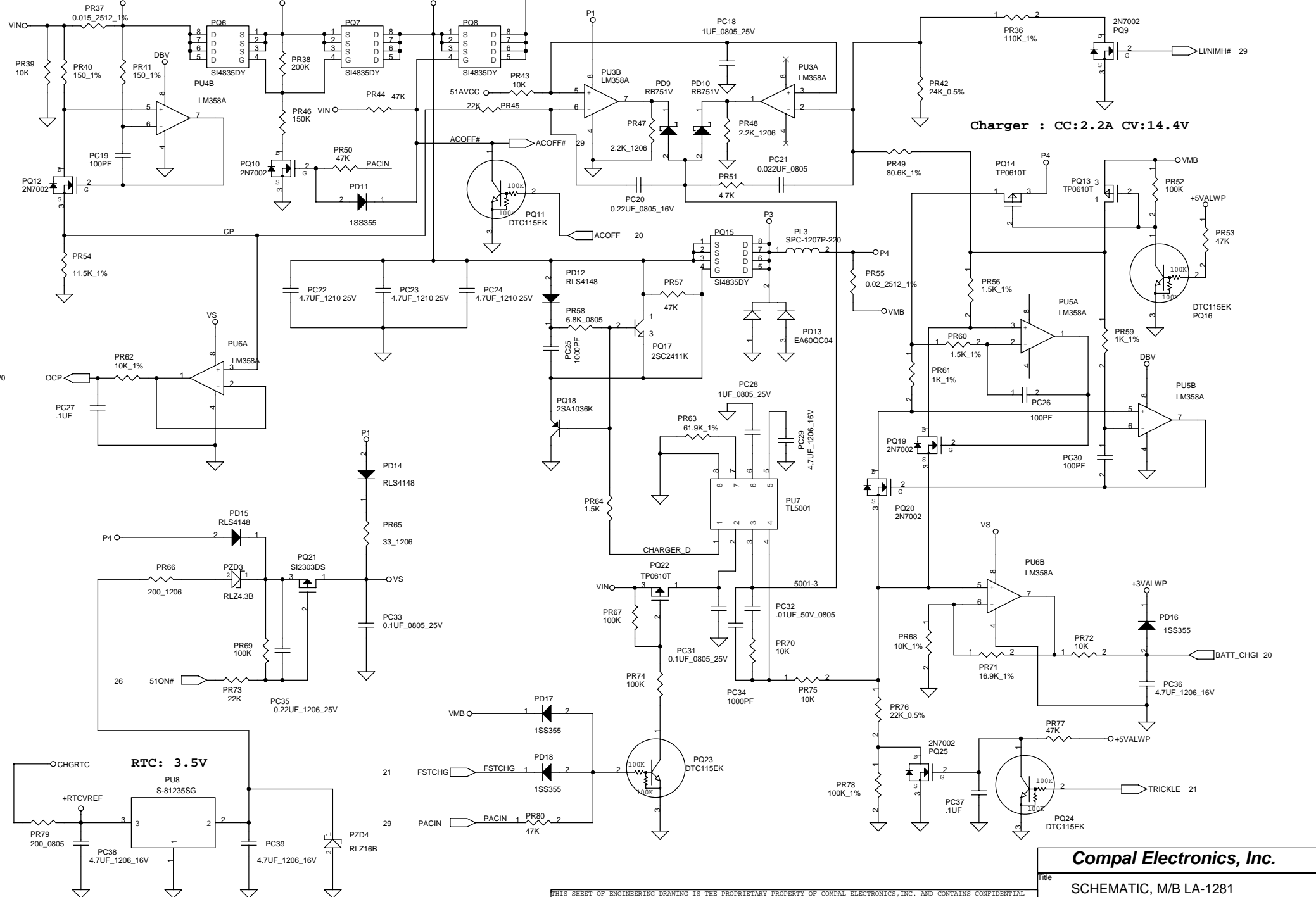


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Title		SCHEMATIC, M/B LA-1281
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 29 of 34

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ACIN: CC:2.87A/ OCP:3.48A

Charger : CC:2.2A CV:16.8V for LI-ION/CV:14.4V for NI-MH

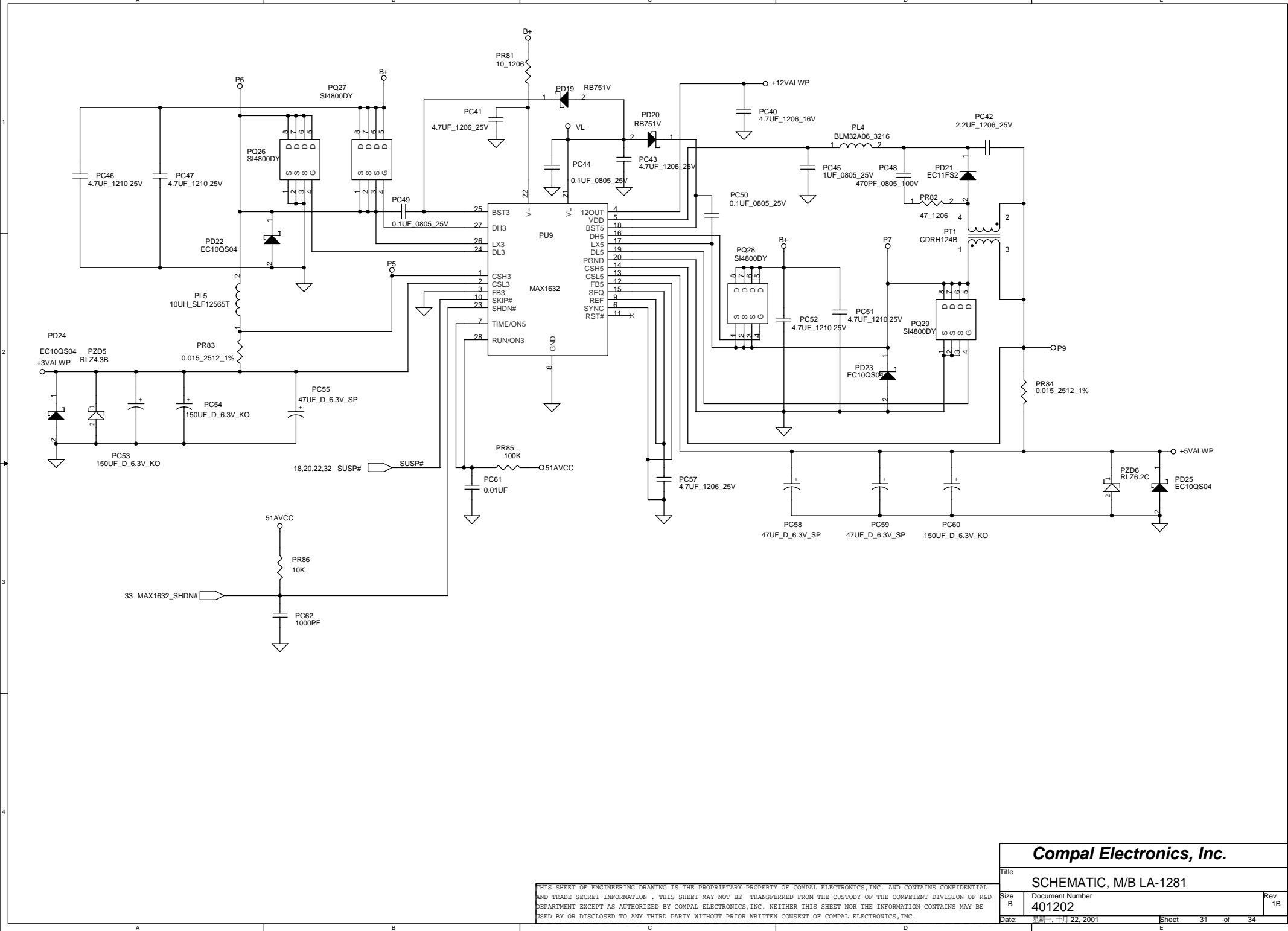


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Title	SCHEMATIC, M/B LA-1281	
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 30 of 34

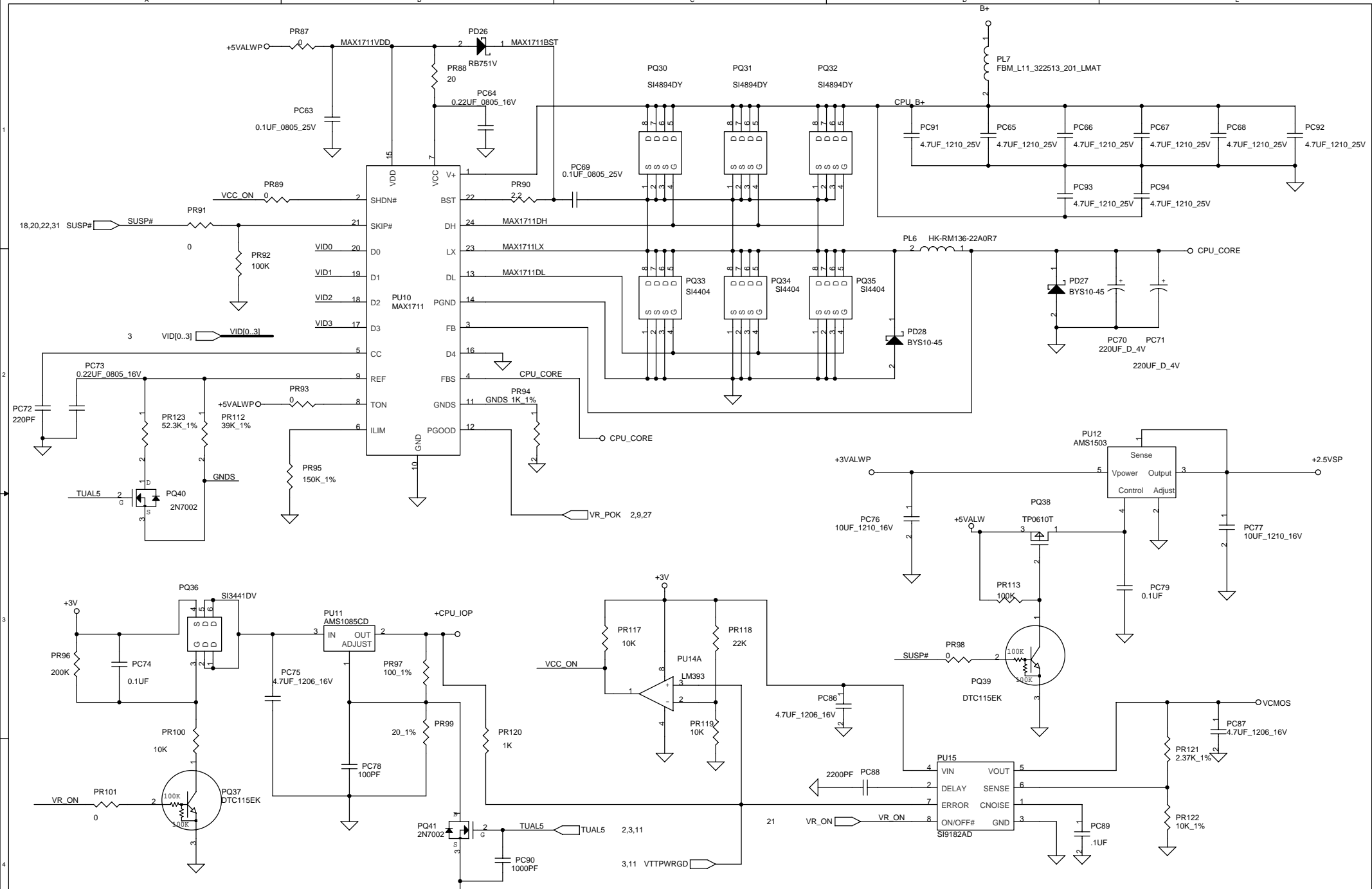


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Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 31 of 34



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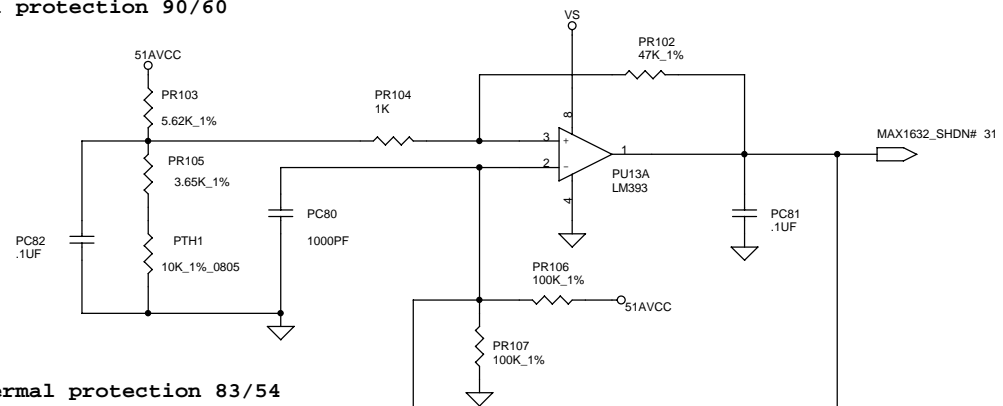
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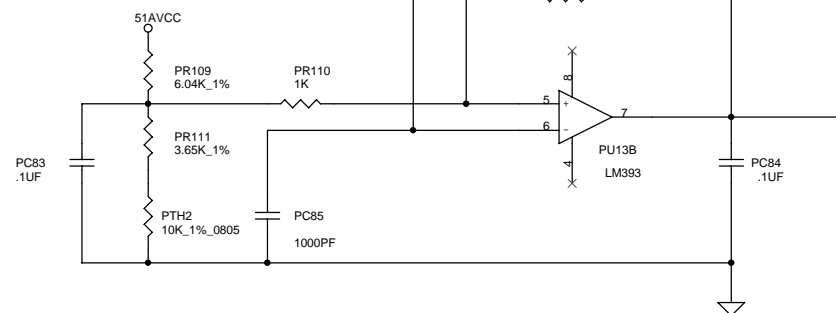
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 32 of 34



For CPU thermal protection 90/60  
度C



For Battery thermal protection 83/54  
度C



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<b>Compal Electronics, Inc.</b>		
Title SCHEMATIC, M/B LA-1281		
Size B	Document Number 401202	Rev 1B
Date: 星期一, 十月 22, 2001	Sheet 33	of 34

# CY23 PIR LIST

08/28/01 Written by Jerry

F11: Add Q61 and R407 for VTPWRGD

\*\*\*\*\* Rev1.0 PIR List \*\*\*\*\*

09/10/01 Written by Jerry

F26: Add @ at R309 and Q47  
Add C507 and U46

Change value of R317 to 510K  
P27: Remove @ at R224, R229, R242, R245, R244, C273, and Q35  
P32: Add PC91, PC92, PC93, and PC94.

09/12/01 Written by Jerry

F06: Change value of RP34, RP50, RP54, RP62, RP38, RP33, RP57,  
RP61, RP53, and RP56 to 16P8R-22  
P26: Change value of R317 to 560K

09/19/01 Written by Jerry

F29: Change value of PR29 to 174K\_1%  
F32: Change value of PR123 to 52.3K\_1%

\*\*\*\*\* Rev2.0 PIR List \*\*\*\*\*

10/03/01 Written by Jerry

F02: Change value of R27 to 180  
Delete R395  
R395's Pin 1 tie to RP98's pin5  
F03: Change value of R353 to 56.2 1%  
F28: Add R408 between +3V and pin 87 of U3

10/08/01 Written by Jerry

F11, P13, P28: Change footprint of Y1, Y2, and Y3  
F23: Change footprint of JP11  
F28: Change footprint of JP12  
F31: Change footprint of PL5  
F26: Change footprint of SW1

10/17/01 Written by Jerry

F02: Add @ at RP25, RP24, RP28, RP27, RP31, RP30, RP 42, RP41,  
RP40, RP43, RP44, RP45, RP46, RP47, RP48, RP49, RP7, RP1, RP6,  
RP14, RP20, RP19, RP22, RP9, RP10, RP11, RP8, RP2, and R7  
F06: Remove @ at R164  
F11: Add @ at R176

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Title		
SCHEMATIC, M/B LA-1281		
Size	Document Number	Rev
B	401202	1B
Date:	星期一, 十月 22, 2001	Sheet 34 of 34

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