

# Compal Confidential

## DCL51 Schematics Document

### Banias uFCBGA/uFCPGA Package with Montara-GM Core Logic

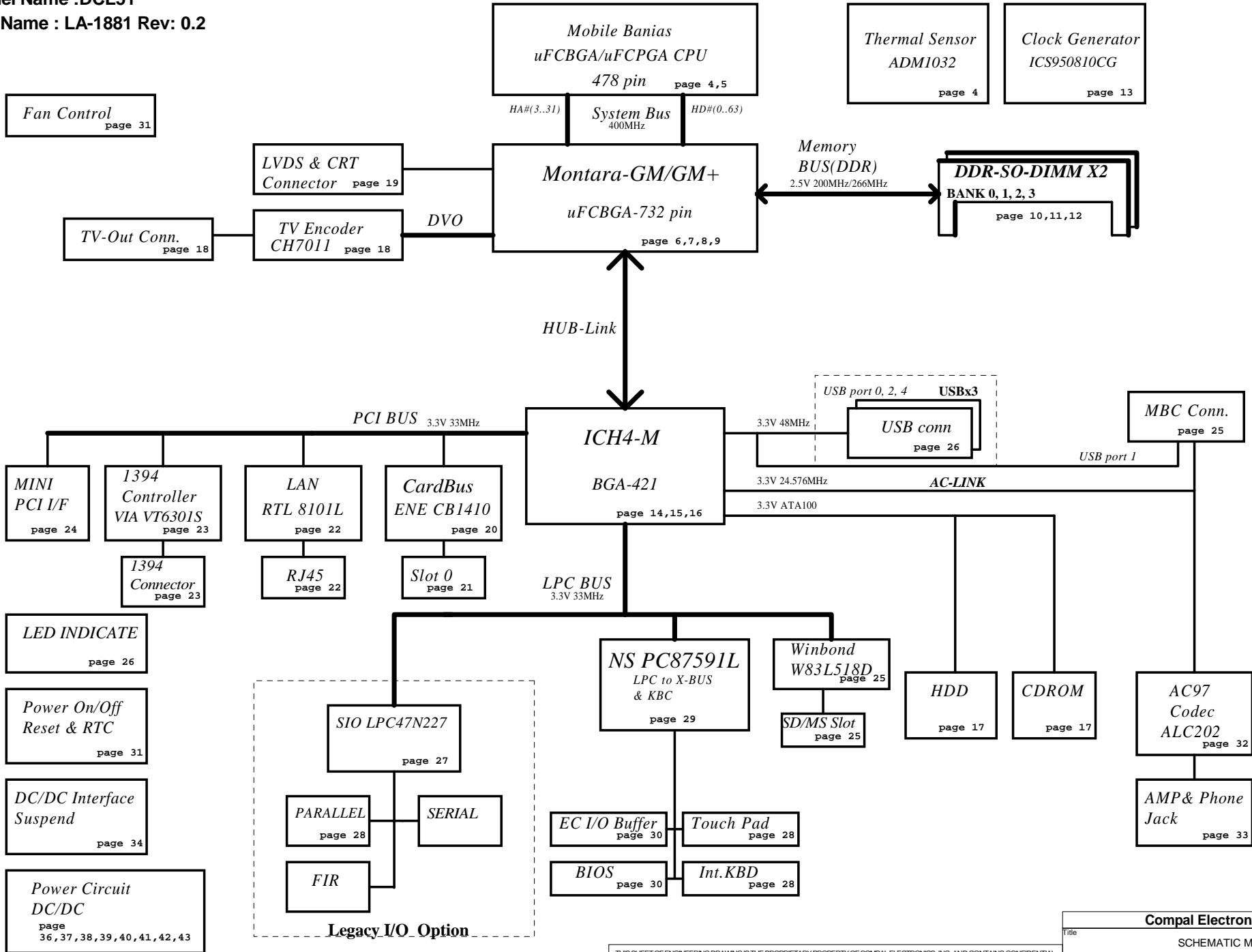
2003-06-12

REV: 1.0

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Title		
SCHEMATIC M/B LA-1881		
Size	Document Number	Rev
	401259	B
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Model Name :DCL51  
 File Name : LA-1881 Rev: 0.2



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## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Board ID Table

BID2	BID1	BID0	PCB Revision
0	0	0	0.1 (For 030)
0	0	1	0.2 (For 030)
0	1	0	0.3 (For 030)
* 0	1	1	1.0 (For 030)
1	0	0	0.1 (For ABO)
1	0	1	0.2 (For ABO)
1	1	0	0.3 (For ABO)
1	1	1	1.0 (For ABO)

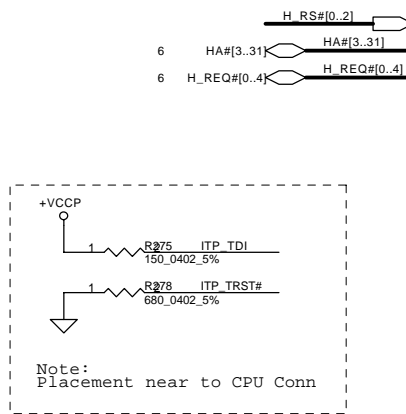
## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

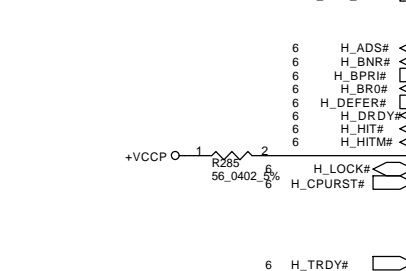
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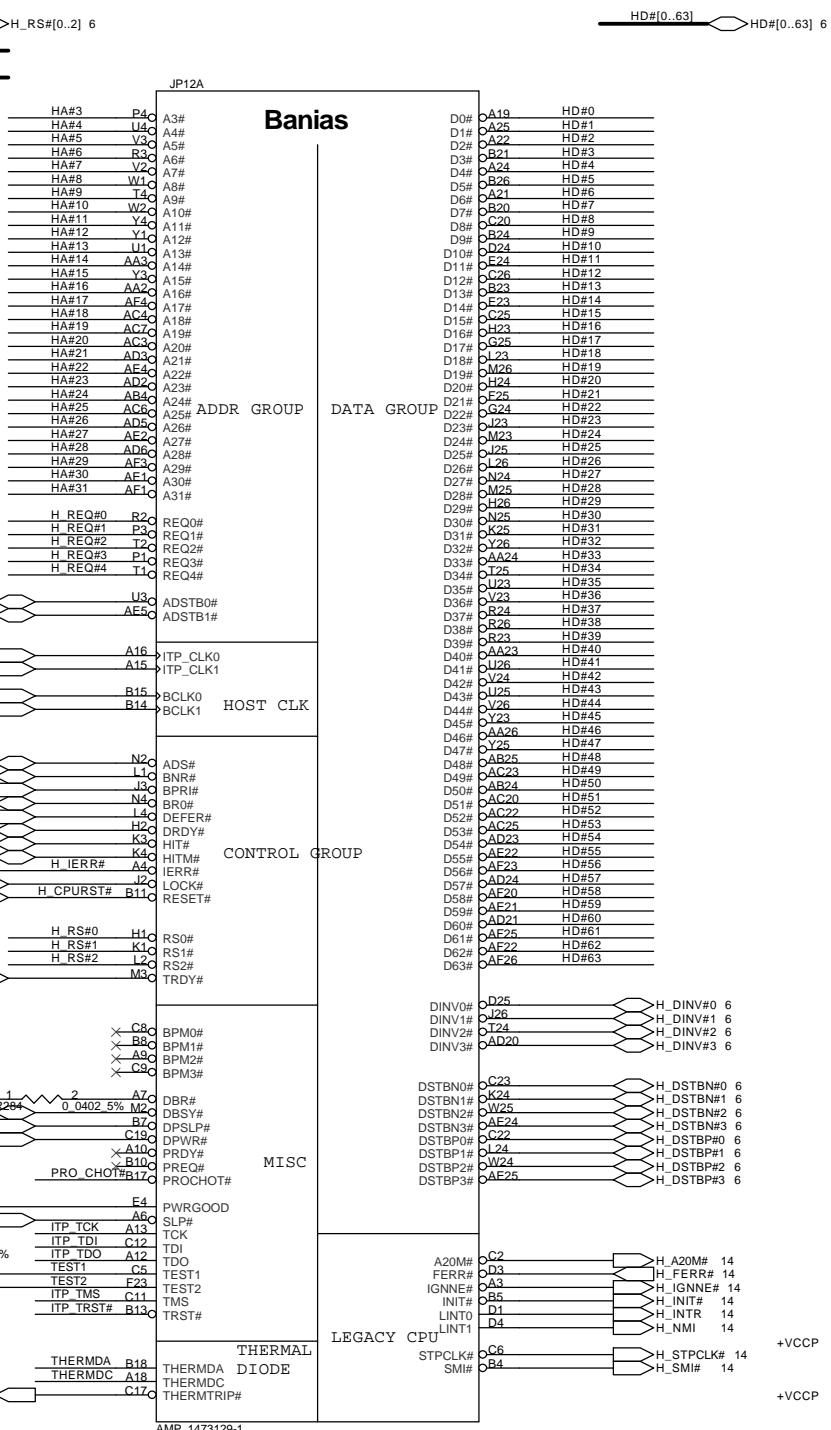
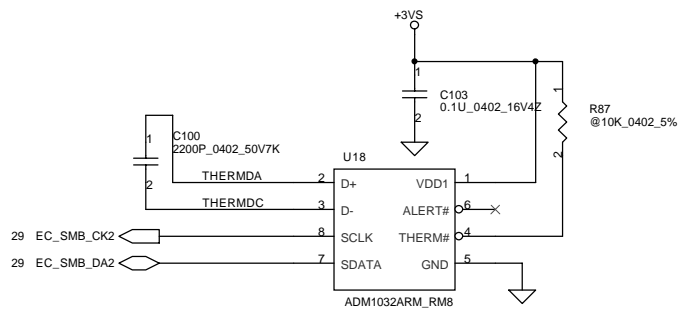
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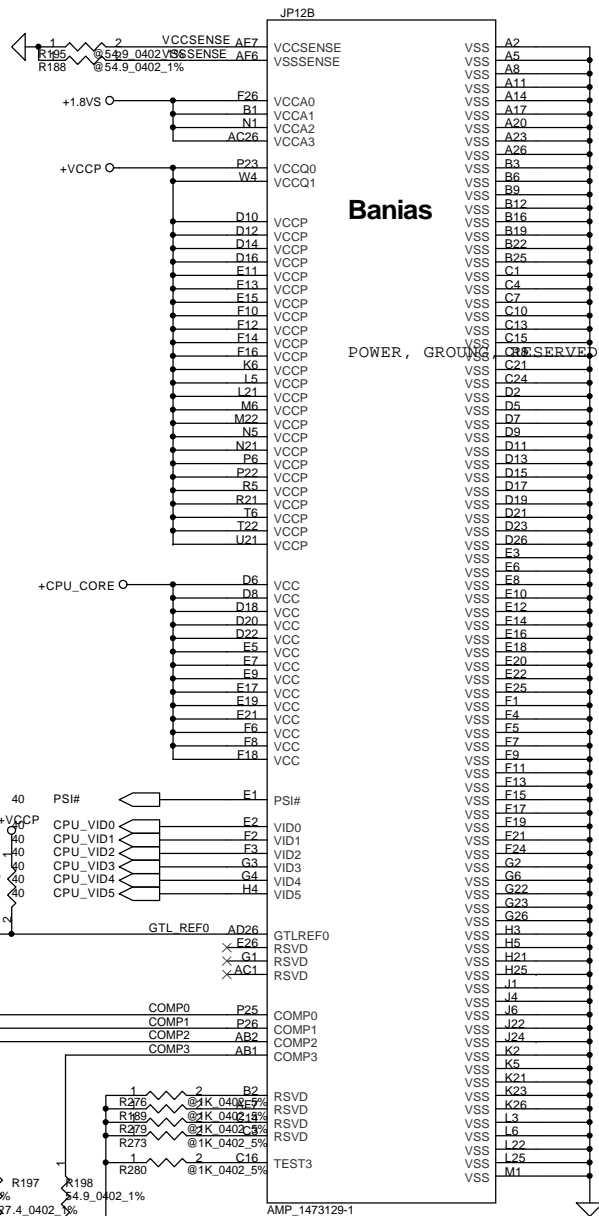


Note:  
Placement near to CPU Conn



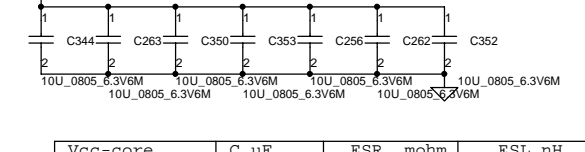
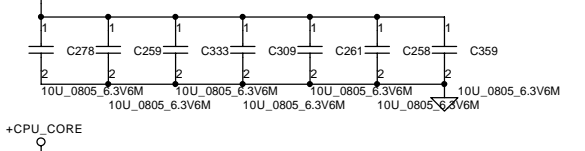
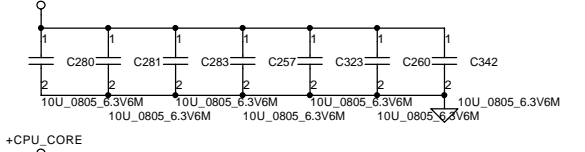
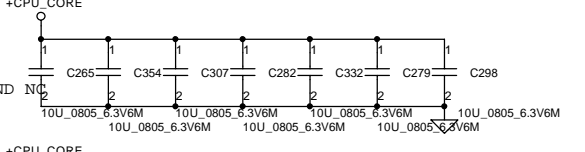
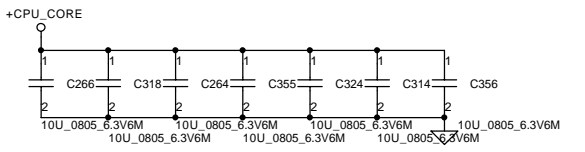
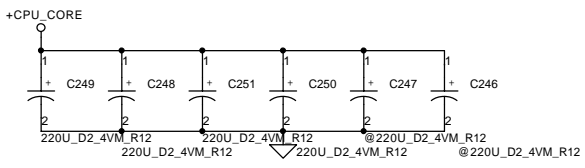
Note:  
Placement near to ITP Conn



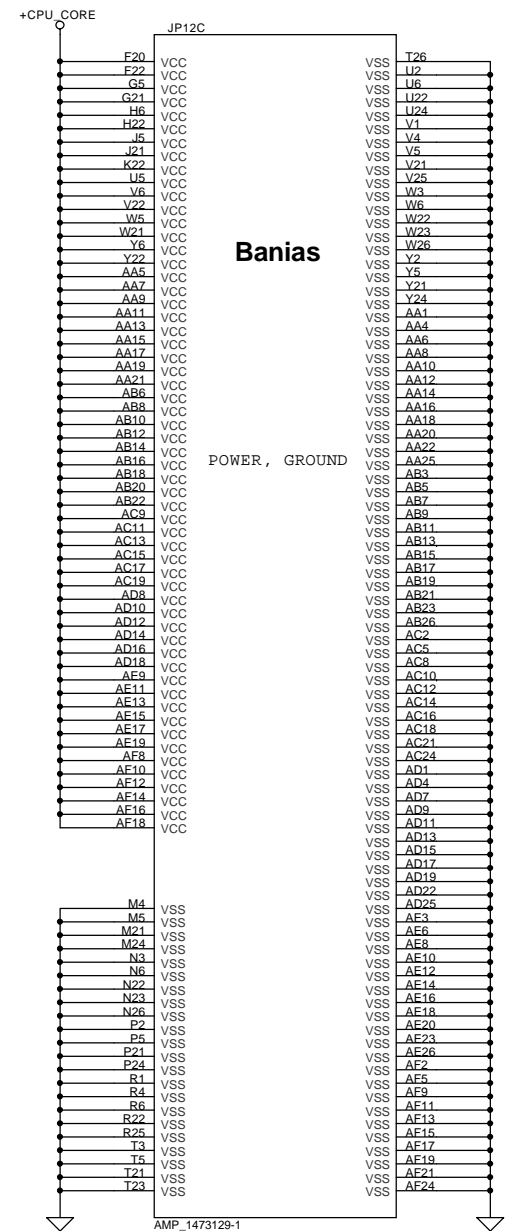
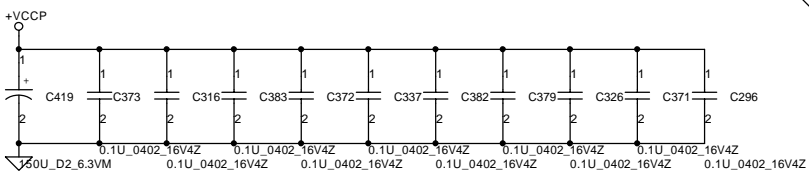
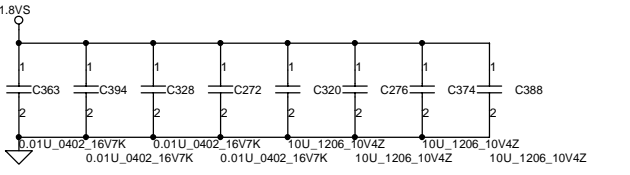


**Banias**

POWER, GROUND RESERVED SIGNALS AND NC



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



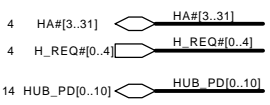
**Banias**

POWER, GROUND

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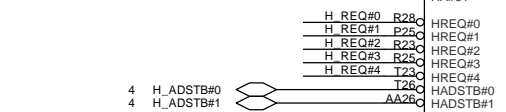
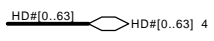
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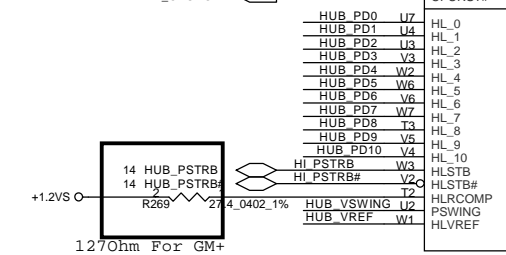
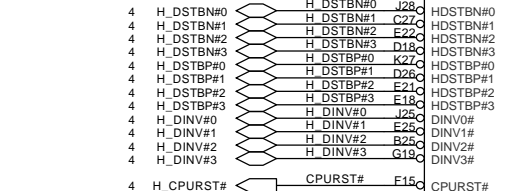
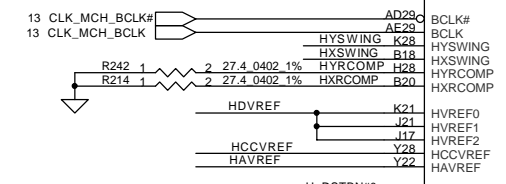
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HA#4	T25C	HA#4
HA#5	T28C	HA#5
HA#6	R27C	HA#6
HA#7	U23C	HA#7
HA#8	U24C	HA#8
HA#9	R24C	HA#9
HA#10	U28C	HA#10
HA#11	V28C	HA#11
HA#12	U27C	HA#12
HA#13	T27C	HA#13
HA#14	U27C	HA#14
HA#15	U25C	HA#15
HA#16	V26C	HA#16
HA#17	Y24C	HA#17
HA#18	V25C	HA#18
HA#19	V23C	HA#19
HA#20	W25C	HA#20
HA#21	Y25C	HA#21
HA#22	AA27C	HA#22
HA#23	W24C	HA#23
HA#24	W23C	HA#24
HA#25	W27C	HA#25
HA#26	Y27C	HA#26
HA#27	AA28C	HA#27
HA#28	W28C	HA#28
HA#29	AB27C	HA#29
HA#30	Y26C	HA#30
HA#31	AB28C	HA#31

### Montara-GM(L)

HD#0	K22	HD#0
HD#1	H27	HD#1
HD#2	K25	HD#2
HD#3	L24	HD#3
HD#4	J27	HD#4
HD#5	G28	HD#5
HD#6	L27	HD#6
HD#7	L23	HD#7
HD#8	L25	HD#8
HD#9	J24	HD#9
HD#10	K23	HD#10
HD#11	K23	HD#11
HD#12	G27	HD#12
HD#13	K26	HD#13
HD#14	J23	HD#14
HD#15	H26	HD#15
HD#16	E25	HD#16
HD#17	E26	HD#17
HD#18	B27	HD#18
HD#19	H23	HD#19
HD#20	E27	HD#20
HD#21	G25	HD#21
HD#22	E28	HD#22
HD#23	D27	HD#23
HD#24	G24	HD#24
HD#25	C28	HD#25
HD#26	B26	HD#26
HD#27	G22	HD#27
HD#28	C26	HD#28
HD#29	E26	HD#29
HD#30	G23	HD#30
HD#31	B21	HD#31
HD#32	G21	HD#32
HD#33	G21	HD#33
HD#34	C24	HD#34
HD#35	C23	HD#35
HD#36	D22	HD#36
HD#37	E24	HD#37
HD#38	D24	HD#38
HD#39	B23	HD#39
HD#40	G20	HD#40
HD#41	E23	HD#41
HD#42	B22	HD#42
HD#43	B23	HD#43
HD#44	E23	HD#44
HD#45	E21	HD#45
HD#46	C20	HD#46
HD#47	C21	HD#47
HD#48	G18	HD#48
HD#49	E19	HD#49
HD#50	E20	HD#50
HD#51	G17	HD#51
HD#52	D20	HD#52
HD#53	E19	HD#53
HD#54	C19	HD#54
HD#55	C17	HD#55
HD#56	E17	HD#56
HD#57	B19	HD#57
HD#58	G16	HD#58
HD#59	E16	HD#59
HD#60	C16	HD#60
HD#61	E17	HD#61
HD#62	D16	HD#62
HD#63	C18	HD#63



### HOST

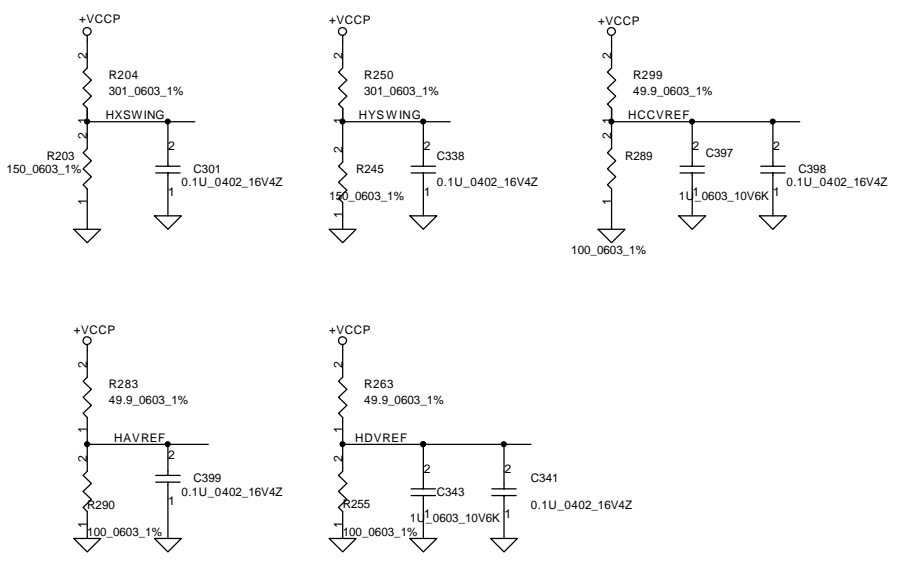


### HUB I/F

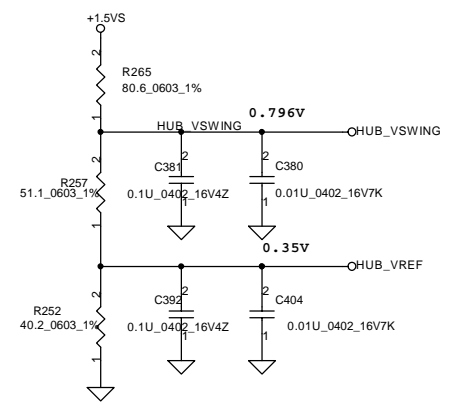
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HL_1	U4	HL_1
HL_2	U3	HL_2
HL_3	V3	HL_3
HL_4	W2	HL_4
HL_5	V6	HL_5
HL_6	V6	HL_6
HL_7	W7	HL_7
HL_8	T3	HL_8
HL_9	V5	HL_9
HL_10	V4	HL_10
H_ADSTB#	W3	H_ADSTB#
H_TRDY#	V2C	H_TRDY#
H_DRDY#	V2C	H_DRDY#
H_DEFER#	V2C	H_DEFER#
H_HIT#	T2	H_HIT#
H_HIT#	T2	H_HIT#
H_LOCK#	U2	H_LOCK#
H_BRO#	U2	H_BRO#
H_BNR#	U2	H_BNR#
H_BPR#	U2	H_BPR#
H_DBSY#	U2	H_DBSY#
H_RS#0	U2	H_RS#0
H_RS#1	U2	H_RS#1
H_RS#2	U2	H_RS#2

RG82G4350M\_uFCBGA732

### HOST REF VOLTAGE

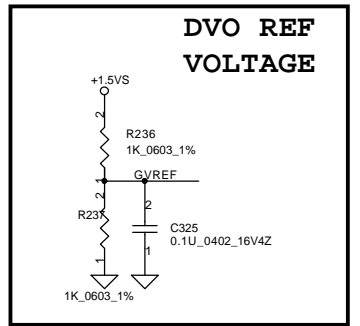
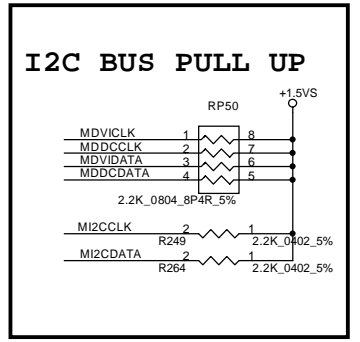
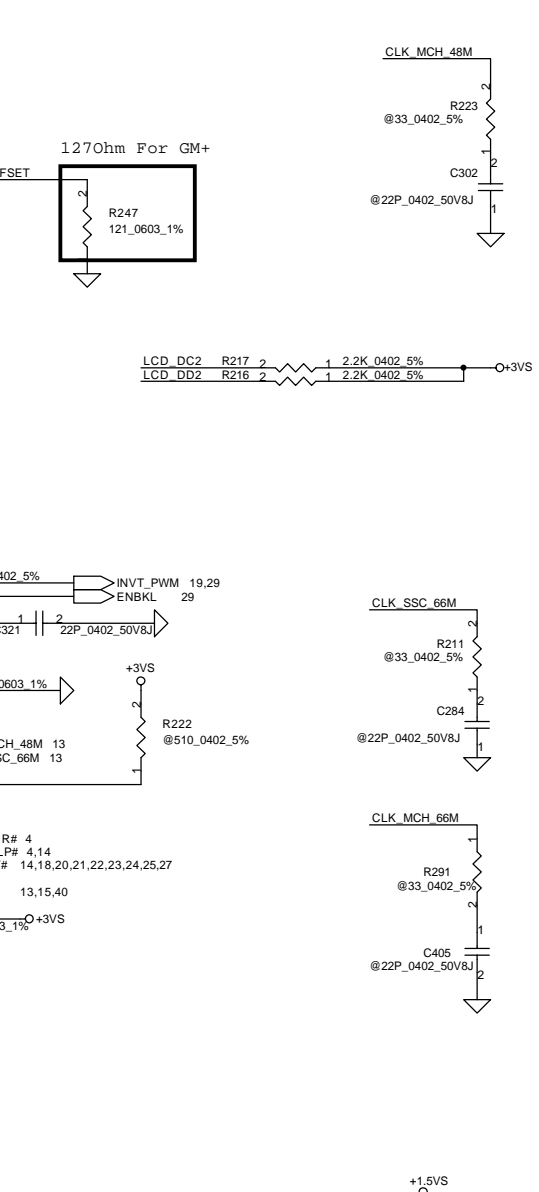
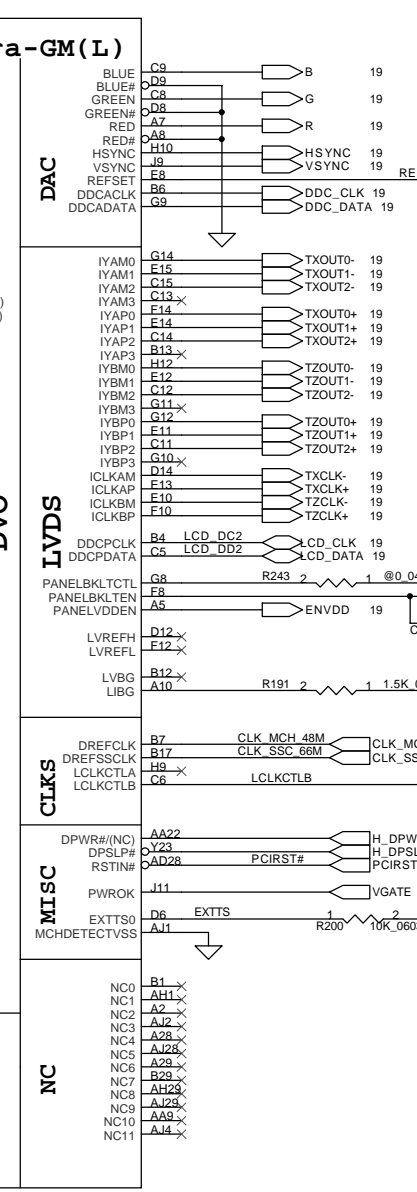
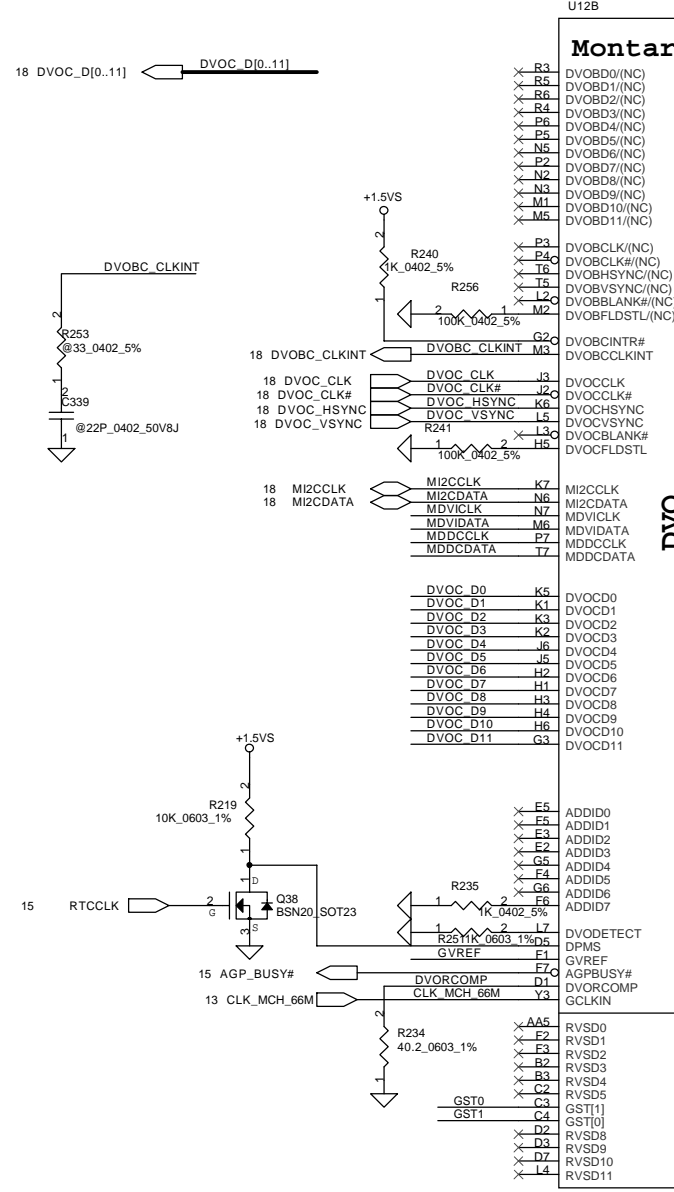


### HUB I/F REF VOLTAGE



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**Starp pin list**

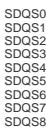
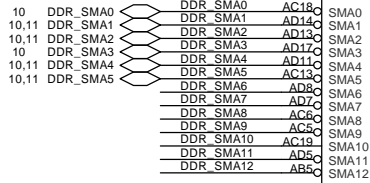
LCLKCTLB: High for P4  
N.C. for Banias (default low)  
DVO DETECT: Low to enable DVO  
High to disable DVO

GST0	GST1	PSB/Sys Mem/ GFX Core
0	0	400/266/200 (default)
0	1	400/200/200
1	0	400/200/133

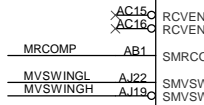
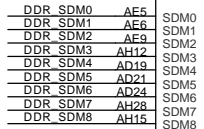
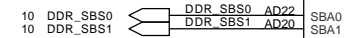
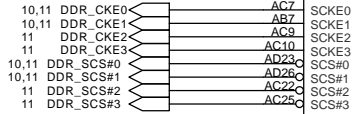
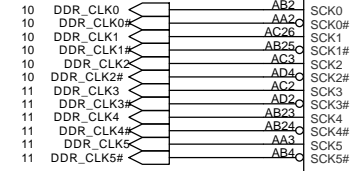
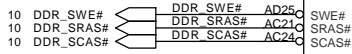
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U12C

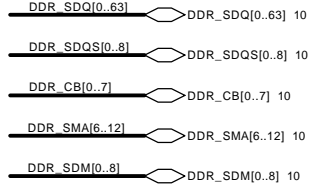
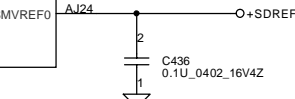
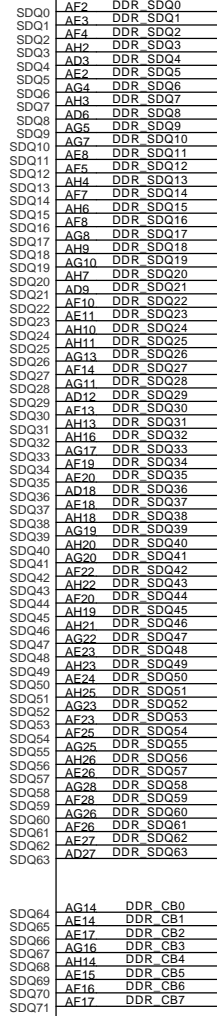
### Montara-GM(L)



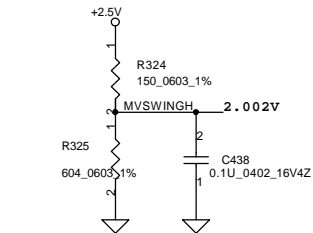
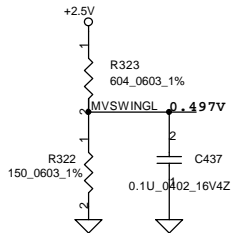
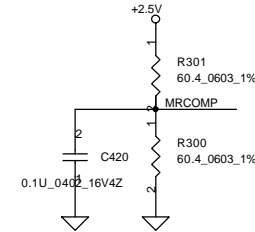
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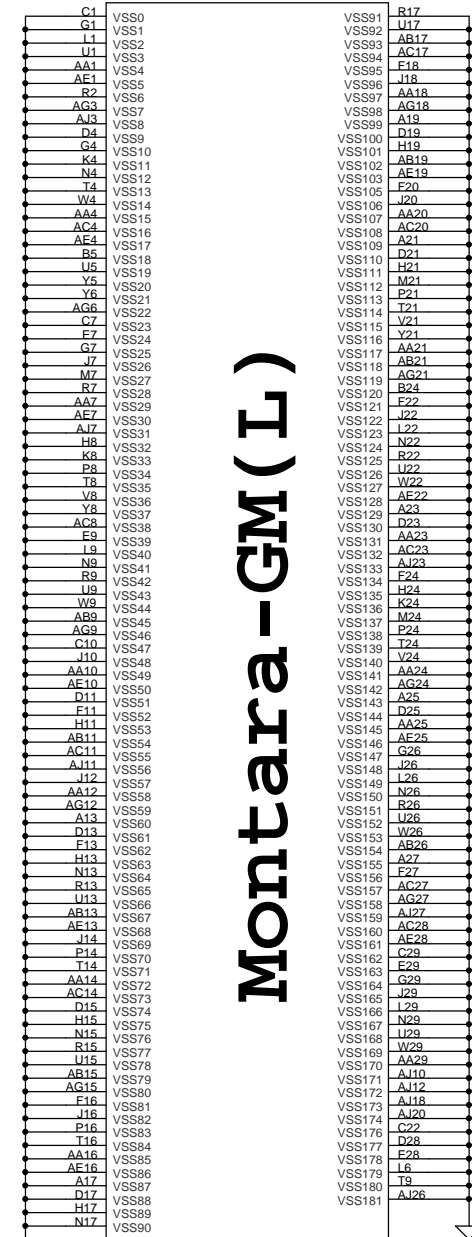
RG82G4350M\_uFCBGA732



### DDR REF & SWING VOLTAGE



U12D



RG82G4350M\_uFCBGA732

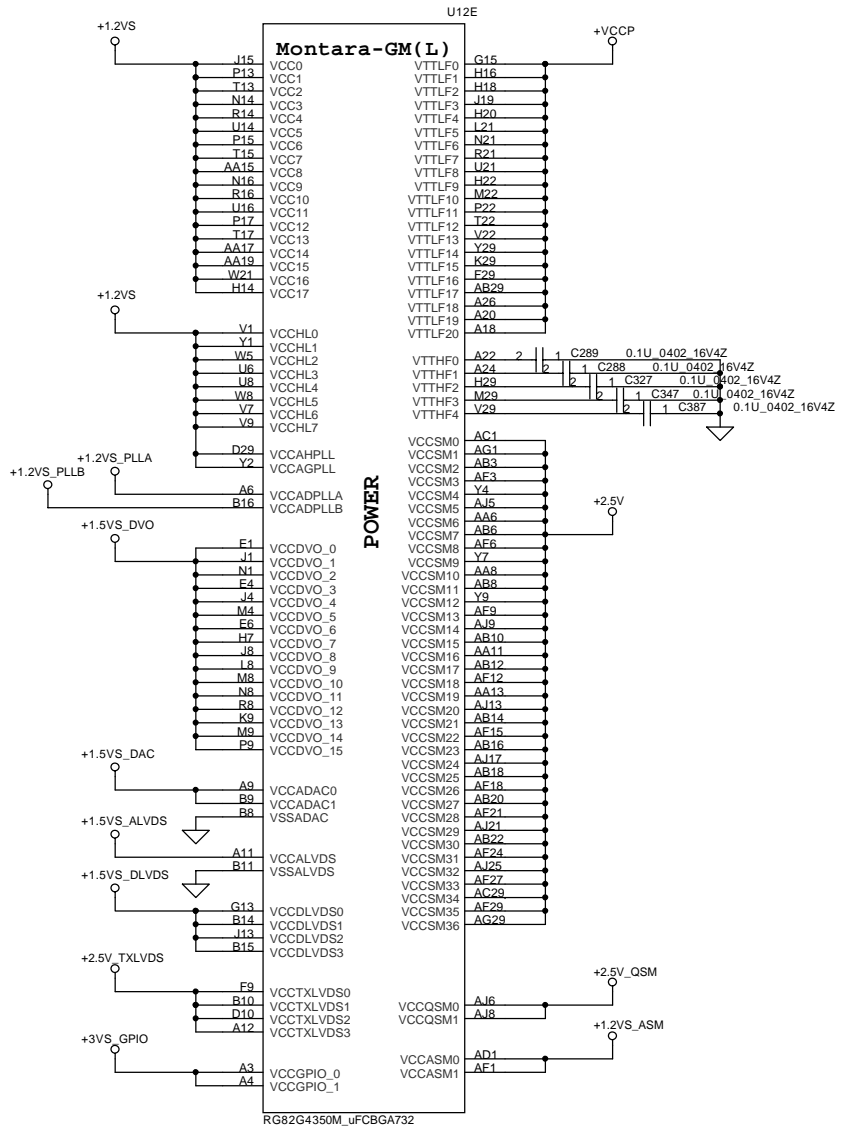
# Montara-GM(L)

Compal Electronics, Inc.

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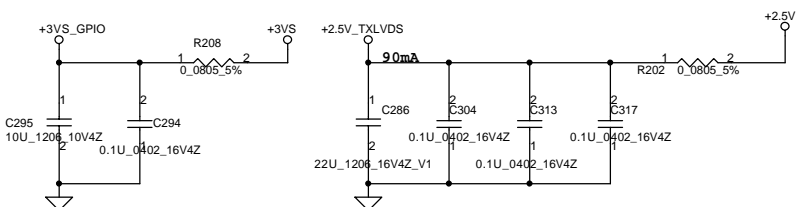
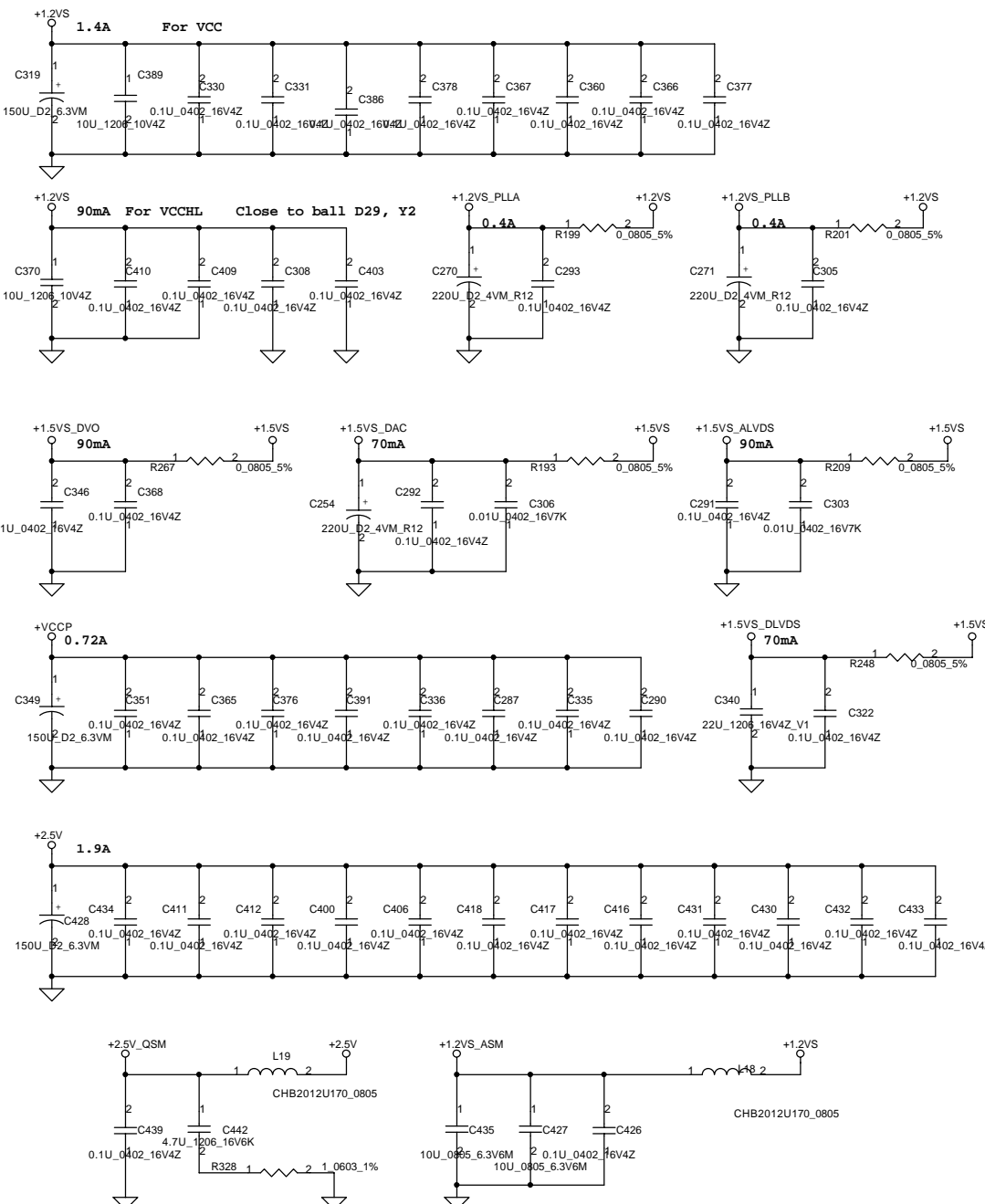


**POWER**

U12E

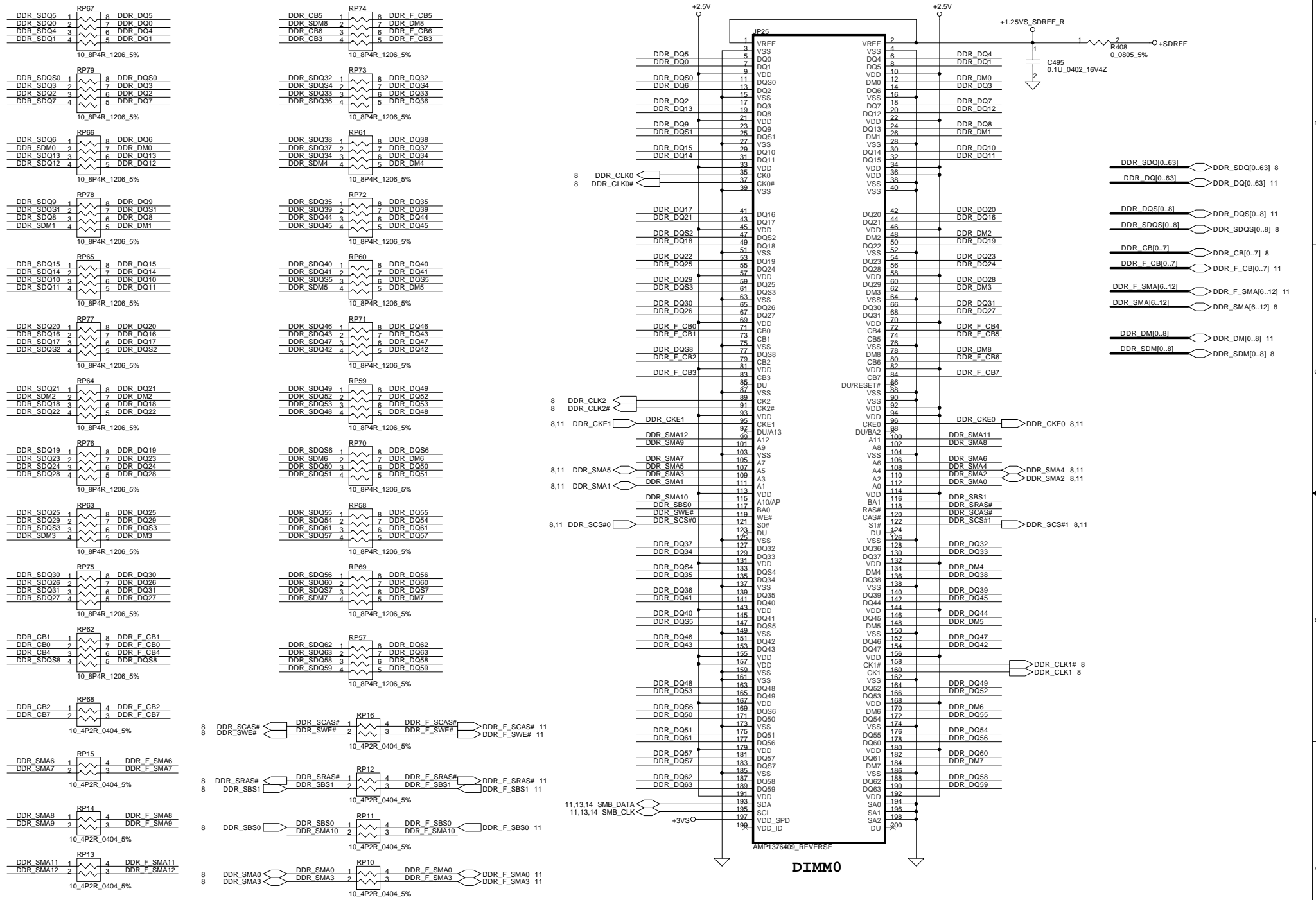
Montara-GM(L)

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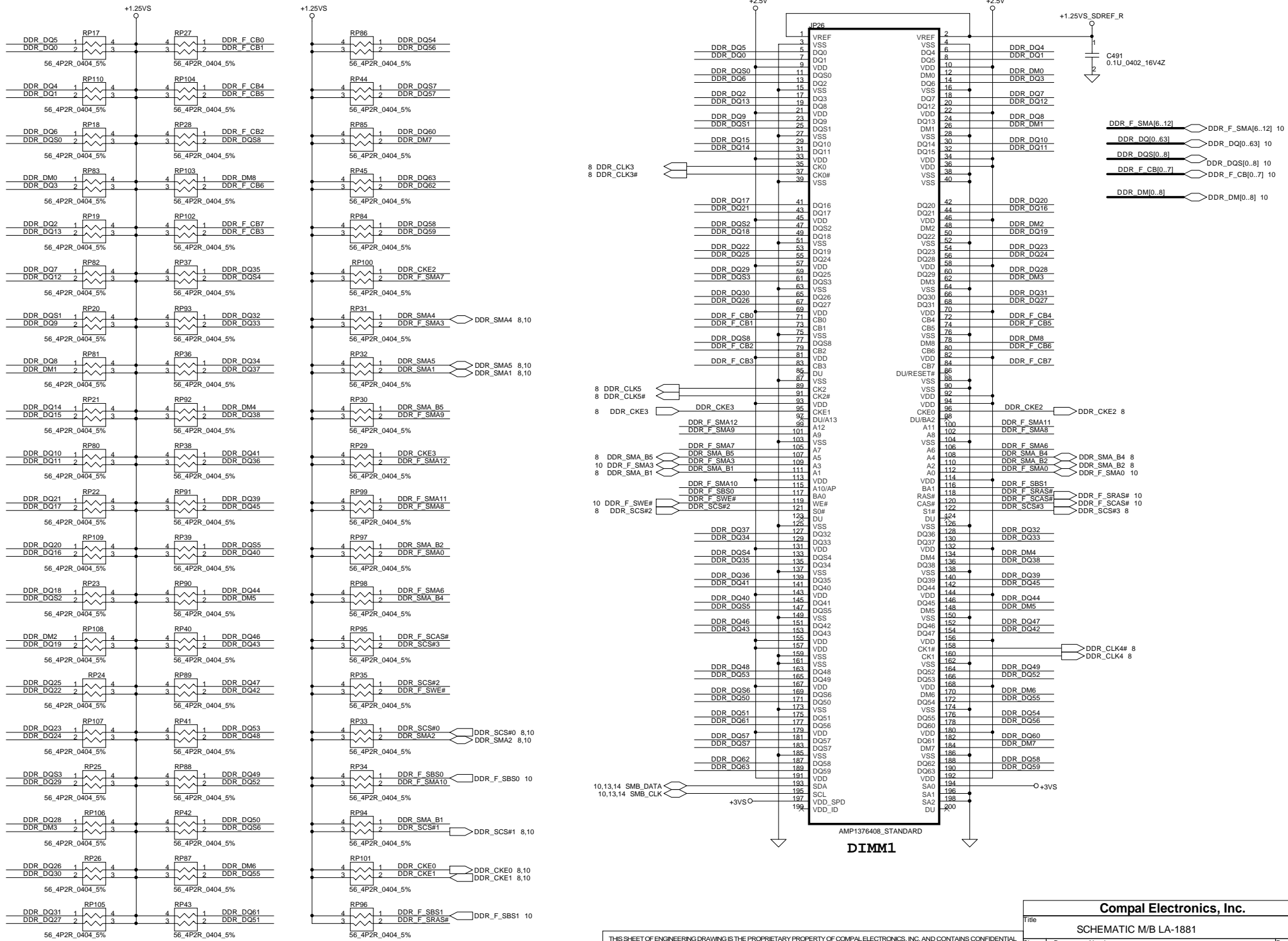
<b>Compal Electronics, Inc.</b>		
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Size	Document Number	Rev
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Date:	~P 星期三, 十二月 29, 2004	Sheet 9 of 45

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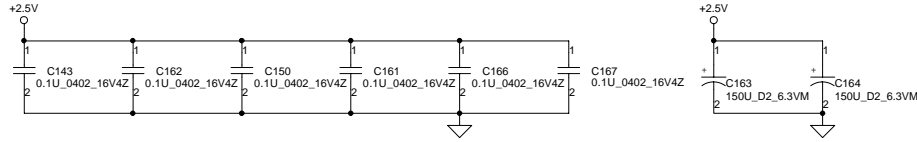
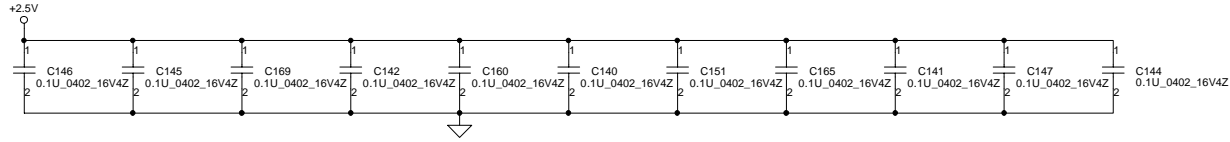
- DDR F\_SMA[6..12] ⇨ DDR\_F\_SMA[6..12] 10
- DDR DQ[0..63] ⇨ DDR\_DQ[0..63] 10
- DDR DQS[0..8] ⇨ DDR\_DQS[0..8] 10
- DDR F\_CB[0..7] ⇨ DDR\_F\_CB[0..7] 10
- DDR DM[0..8] ⇨ DDR\_DM[0..8] 10

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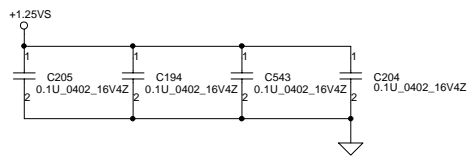
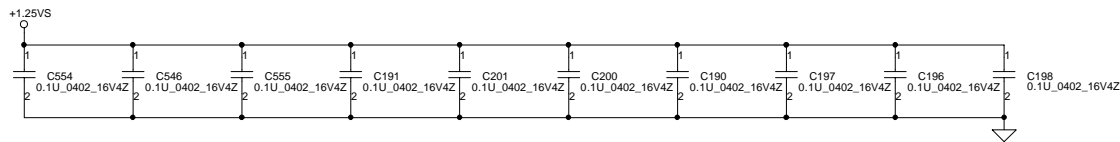
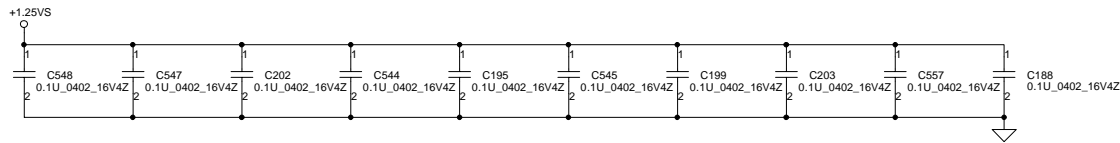
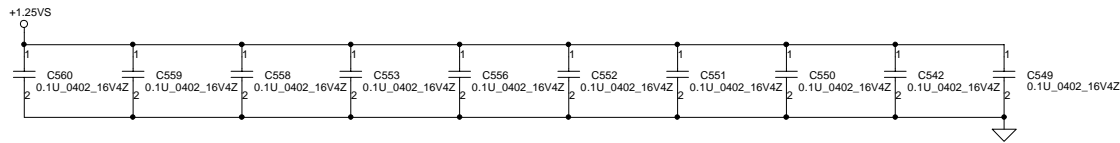
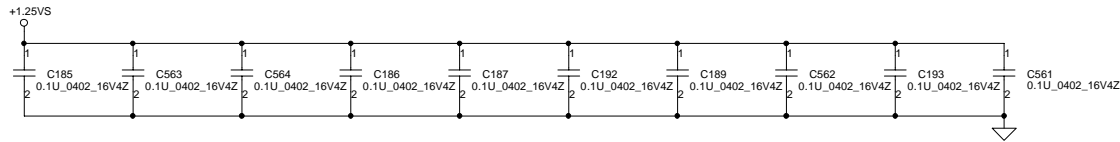
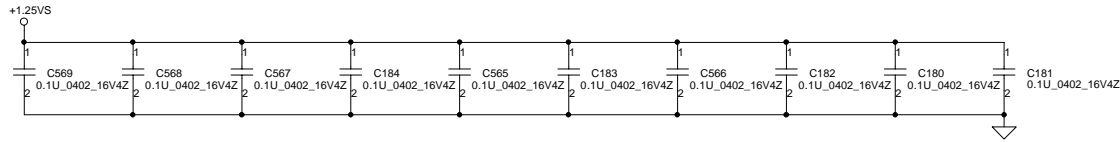
**Layout note :**

Distribute as close as possible to DDR-SODIMM.



**Layout note :**

Place one cap close to every 2 pull up resistors termination to +1.25V



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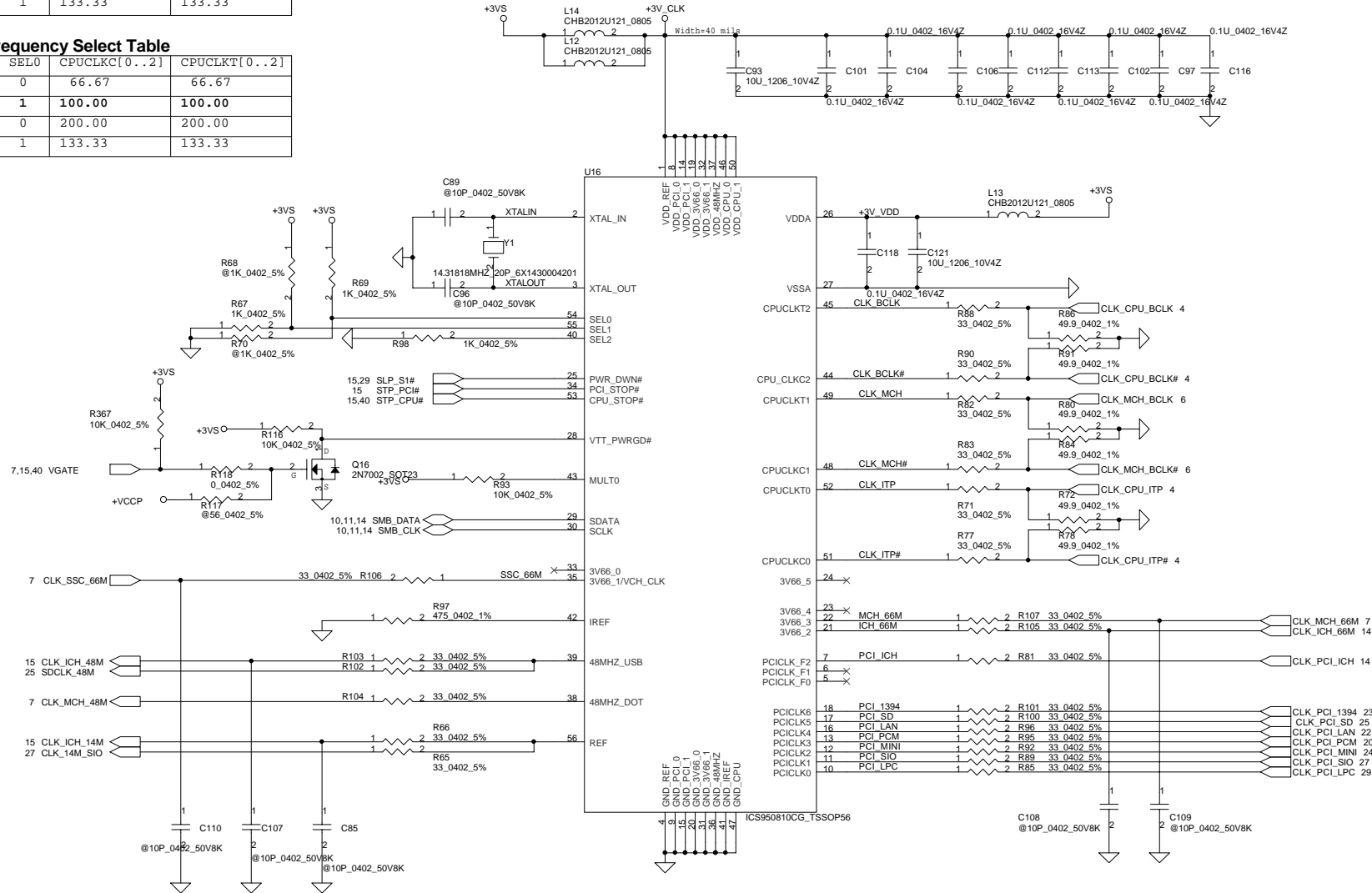
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ICS950810 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

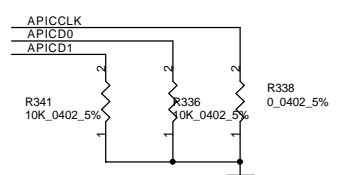
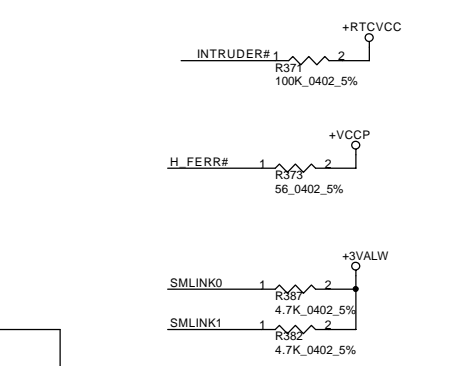
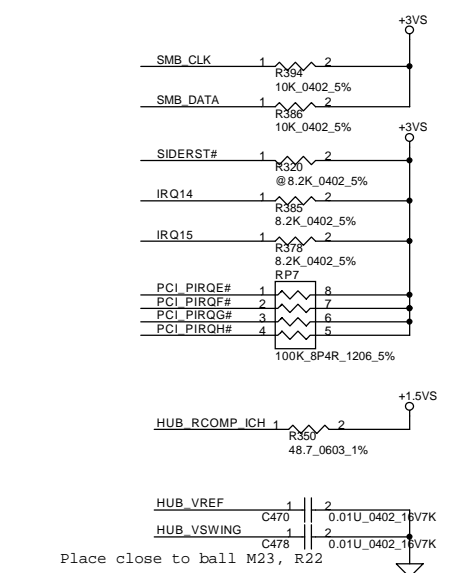
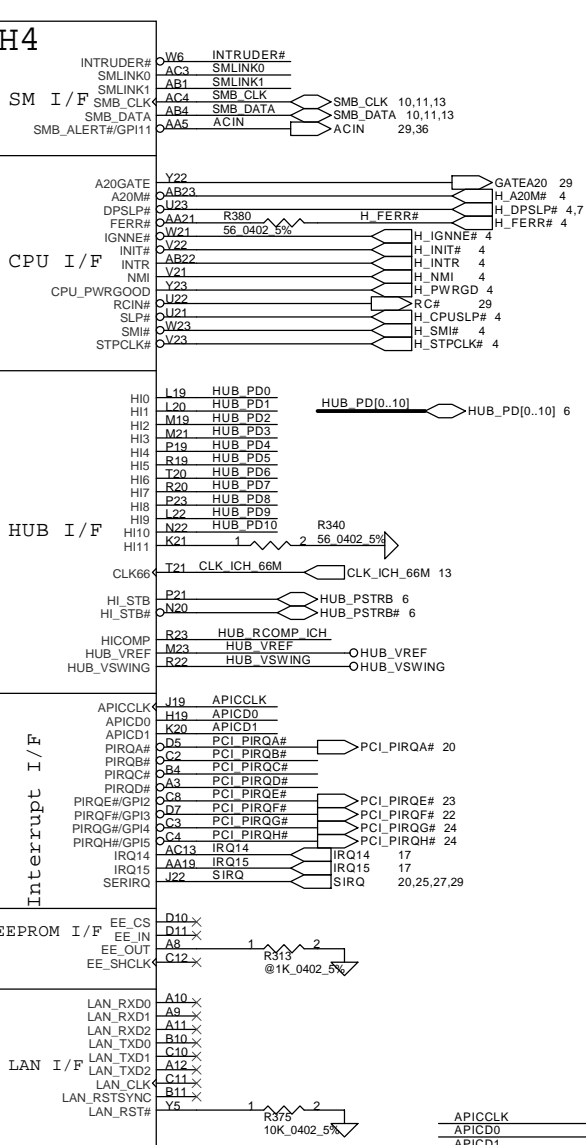
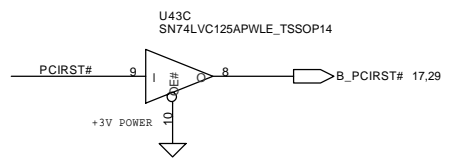
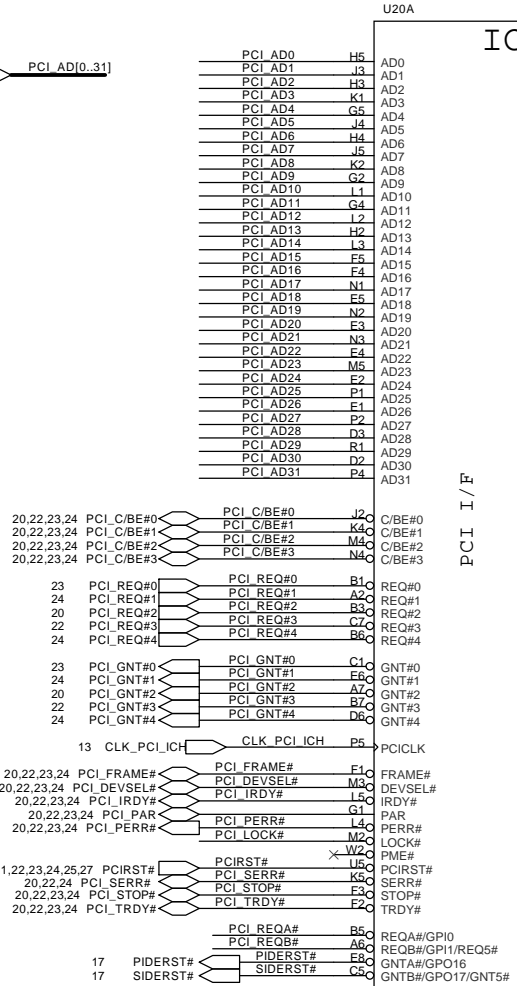
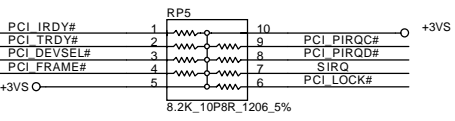
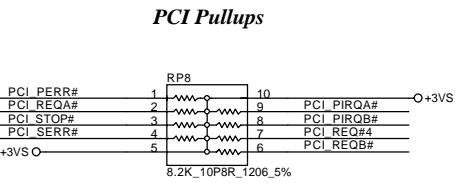
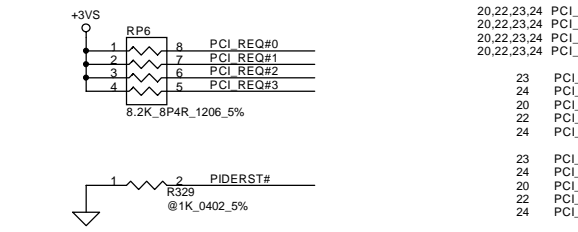
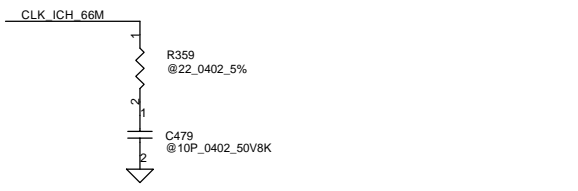
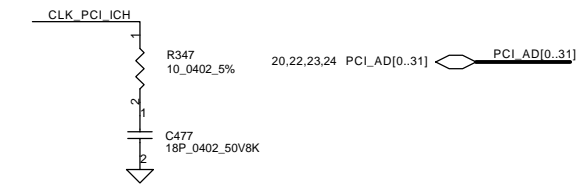
CY28346-2 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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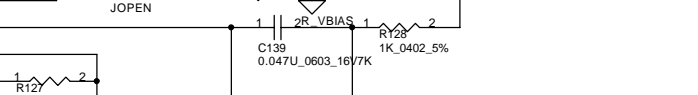
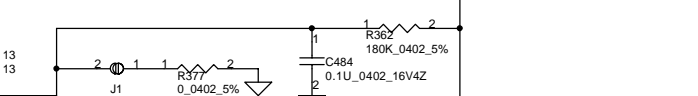
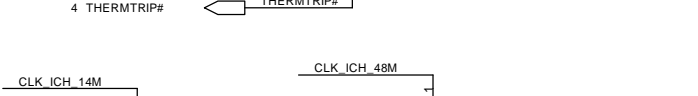
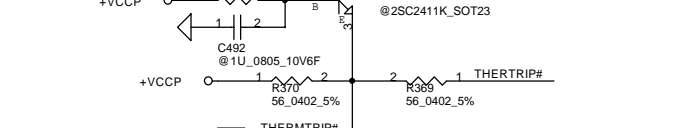
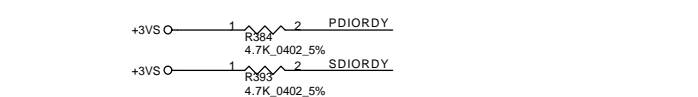
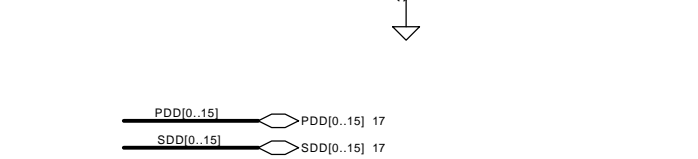
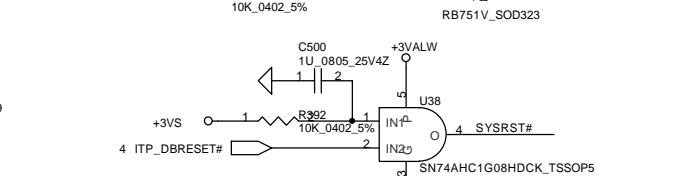
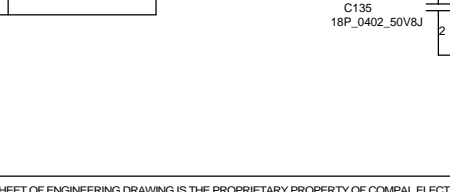
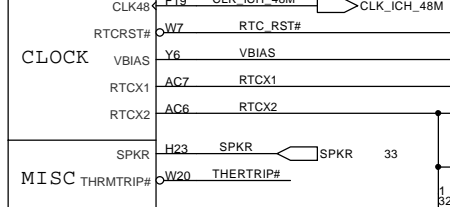
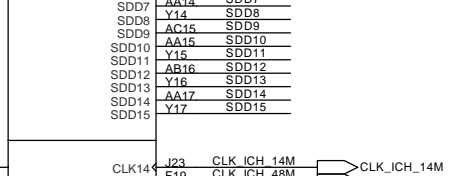
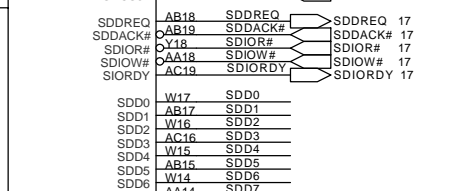
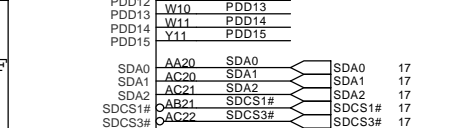
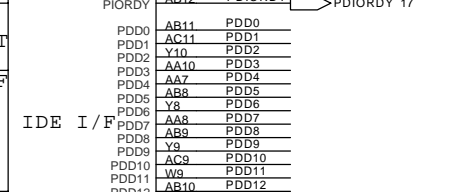
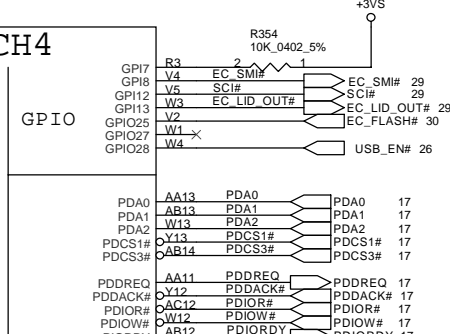
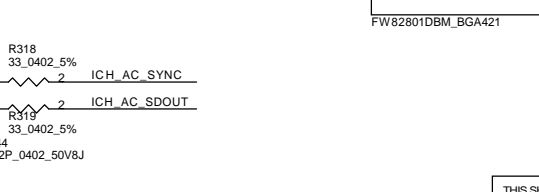
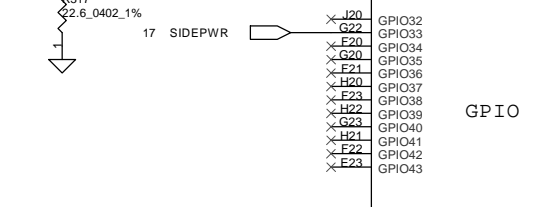
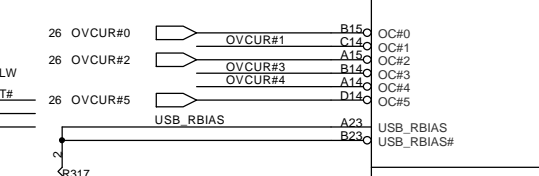
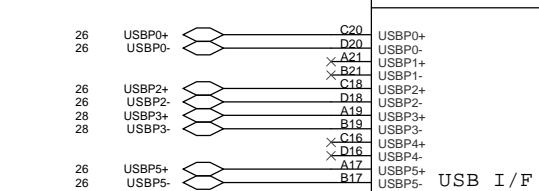
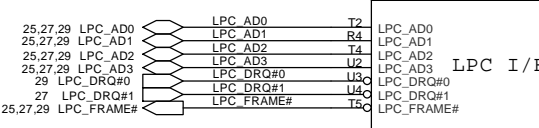
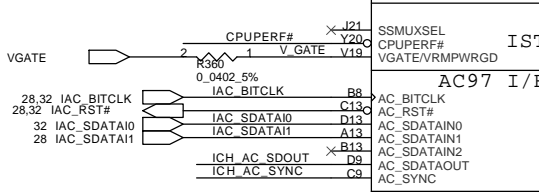
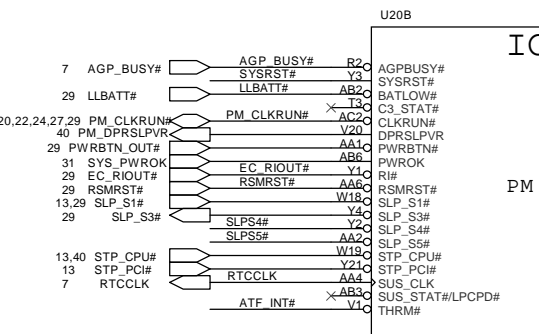
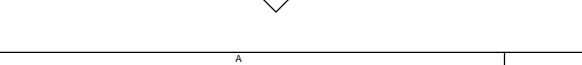
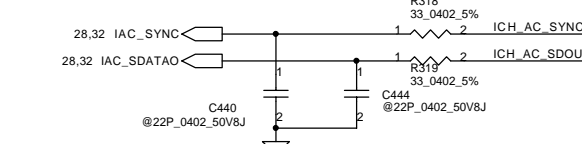
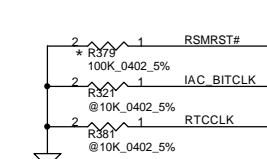
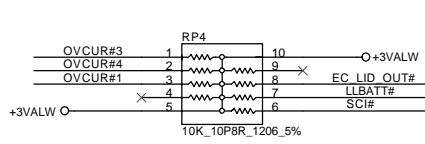
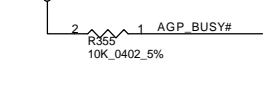
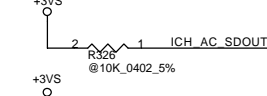
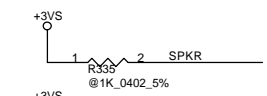
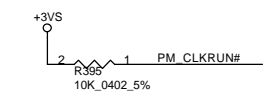
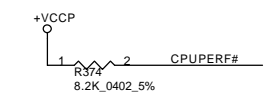
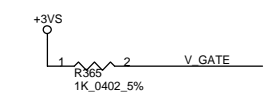
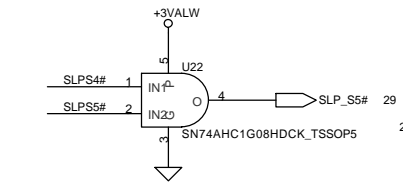
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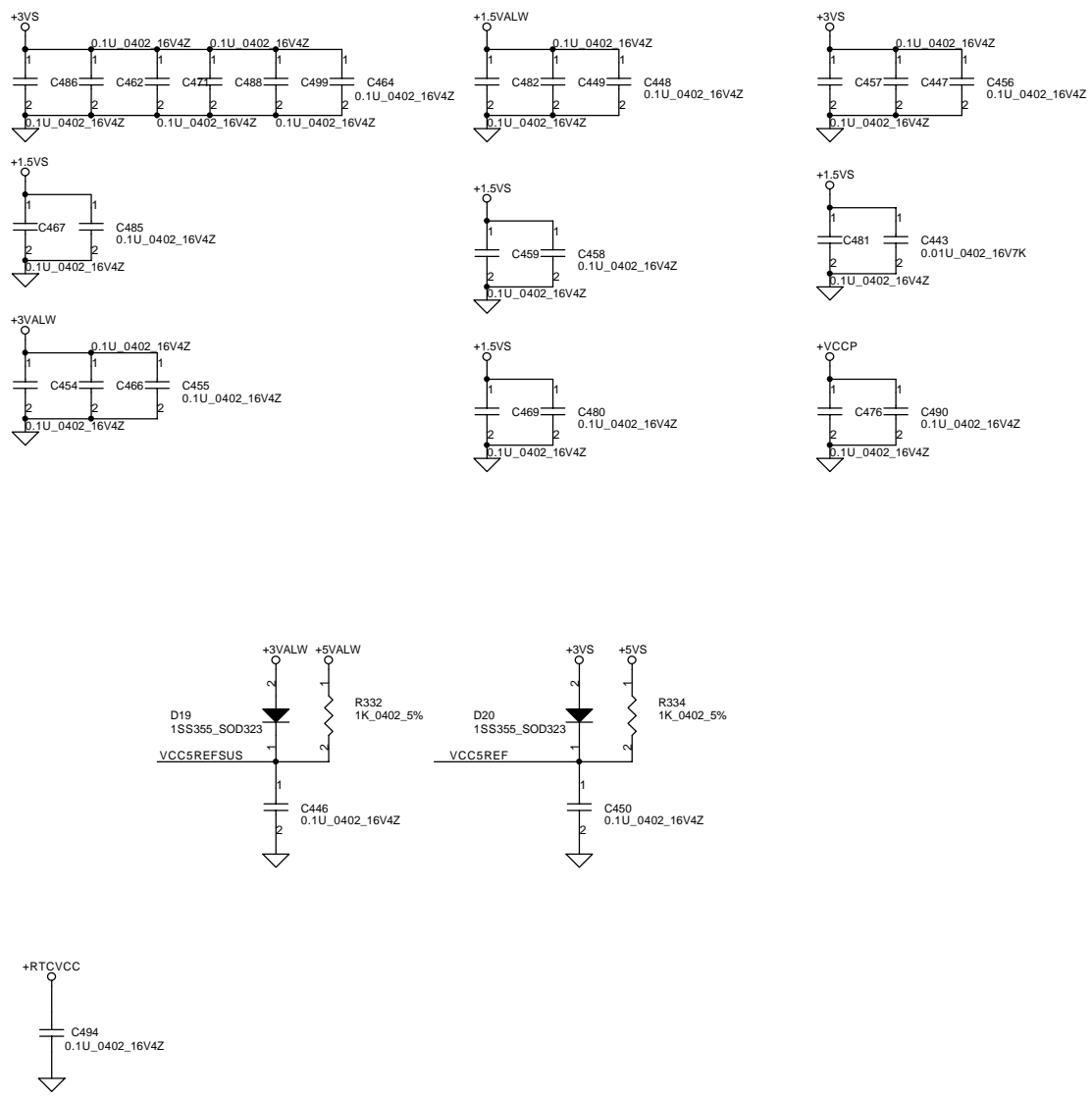
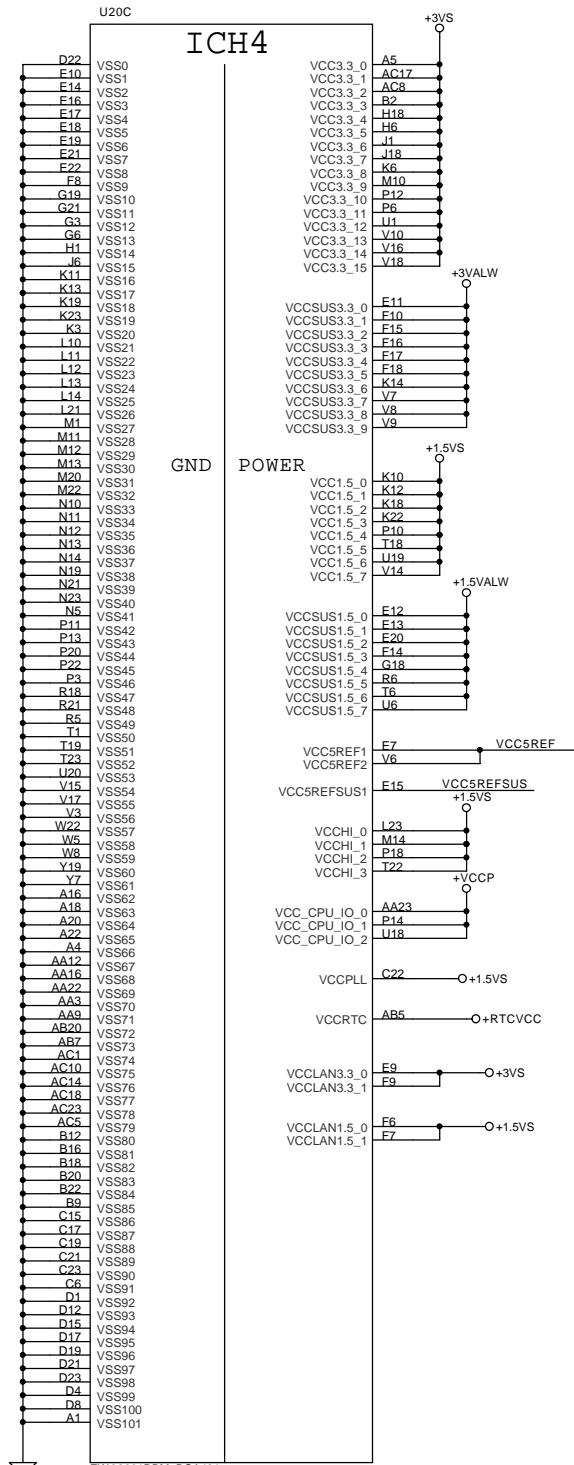
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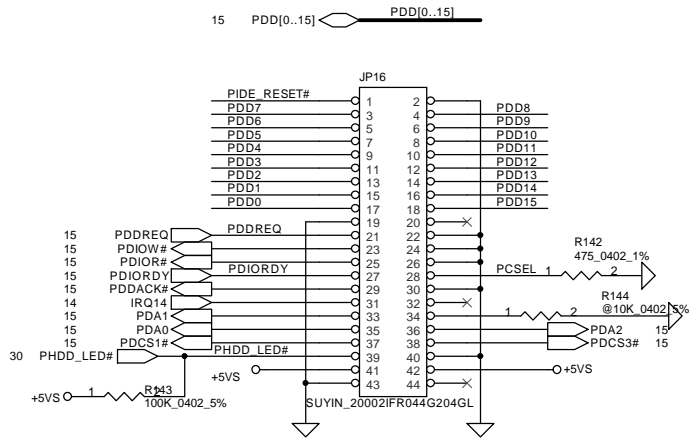


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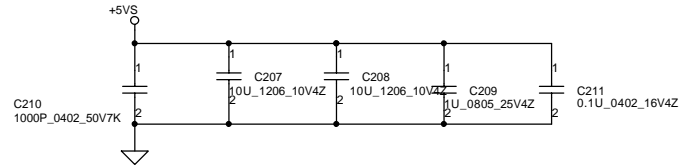
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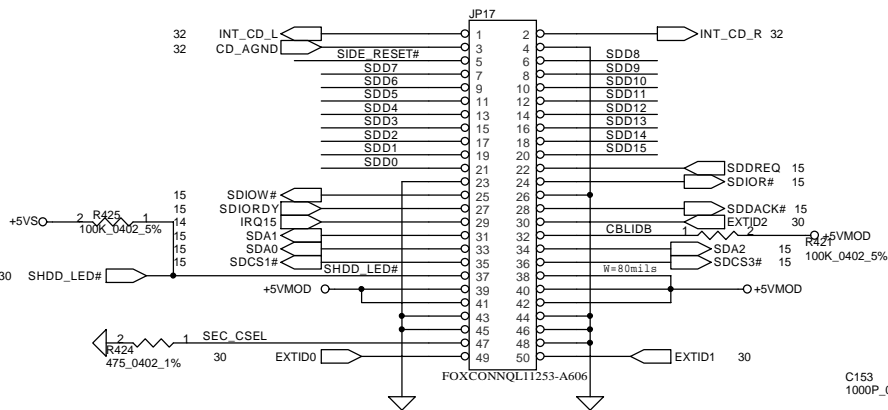
### HDD Connector



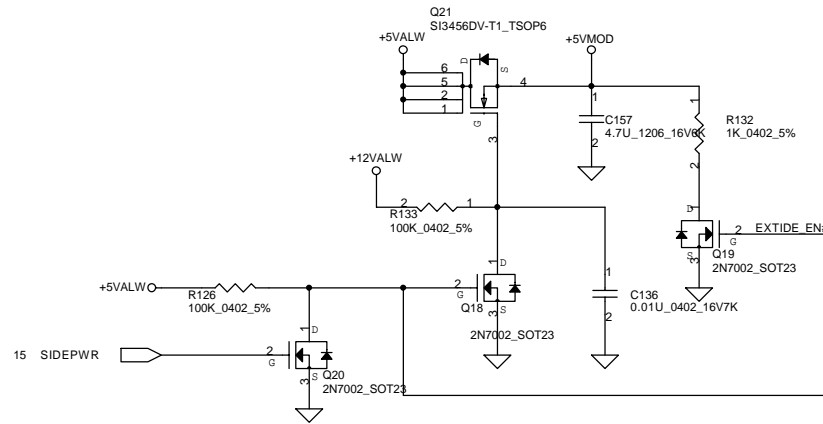
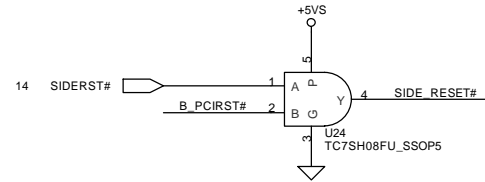
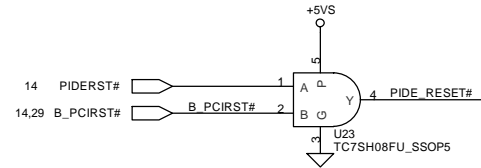
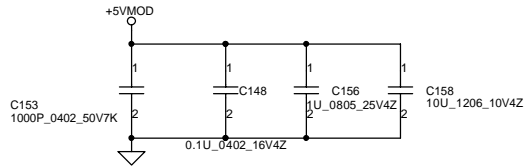
#### Placea caps. near HDD CONN.



### CD-ROM Connector



#### Placea caps. near CDROM CONN.

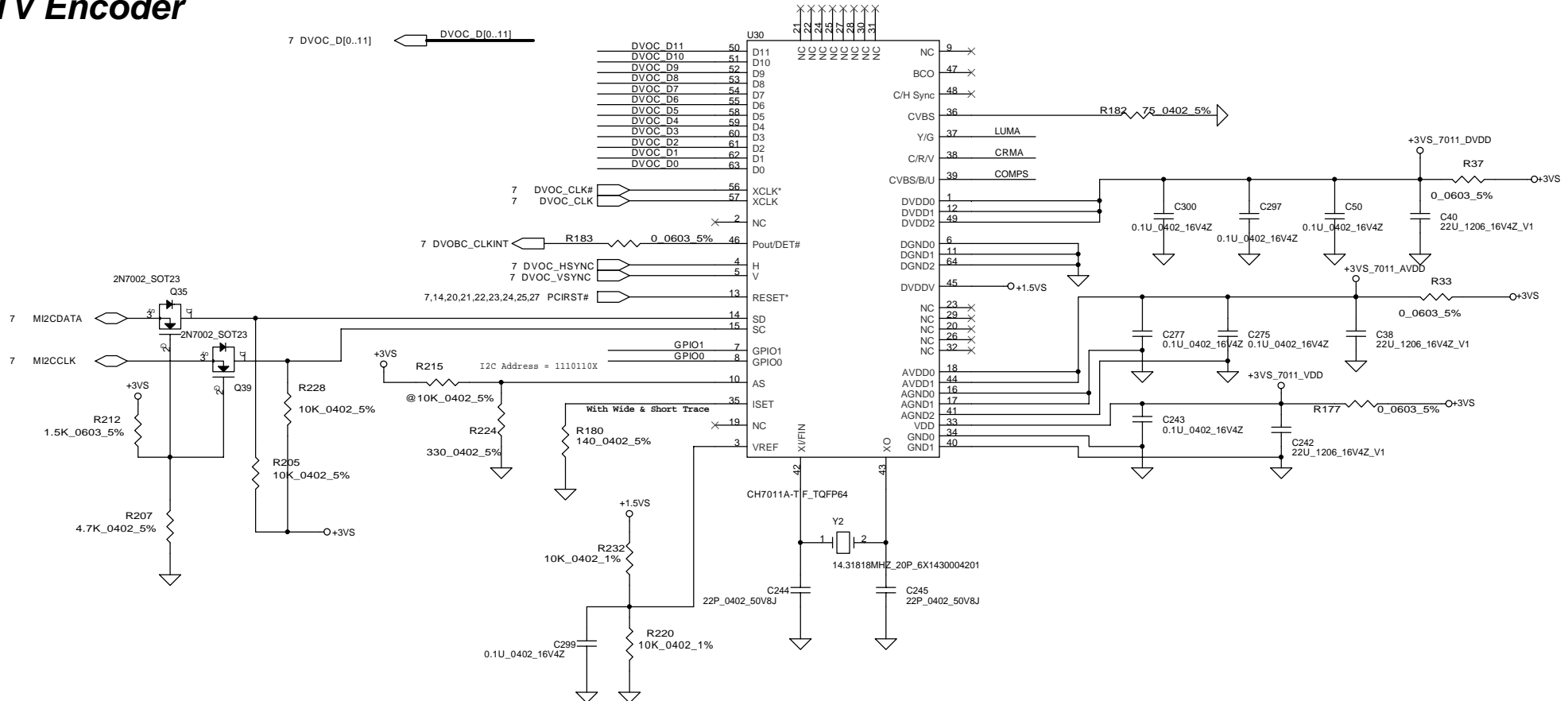


SI3456DV: N CHANNEL  
VGS: 4.5V, RDS: 65 mOHM  
Id(MAX): 5.1A  
VGS,+20V

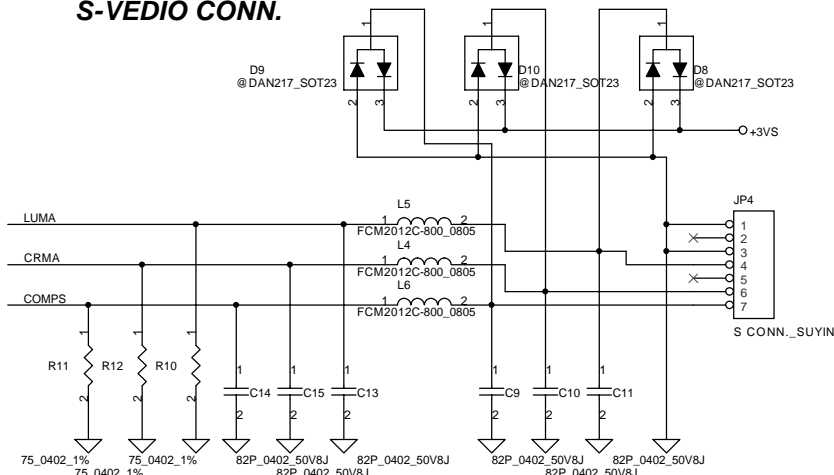
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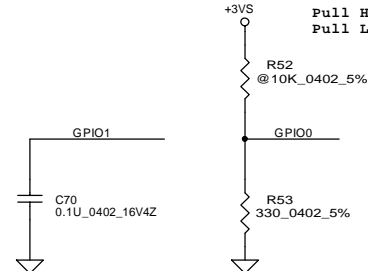
# TV Encoder



## S-VIDEO CONN.



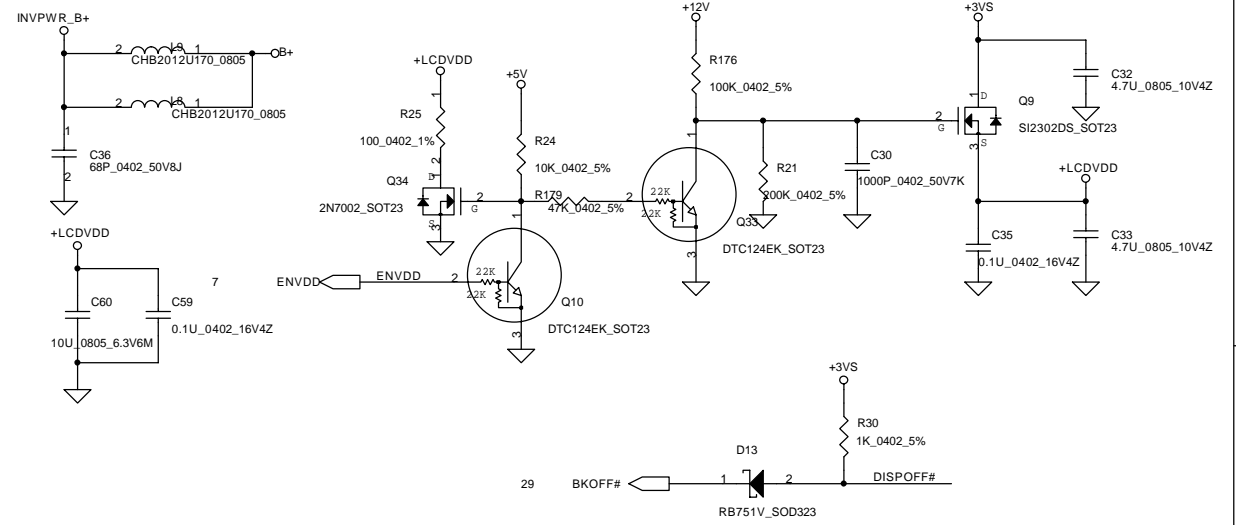
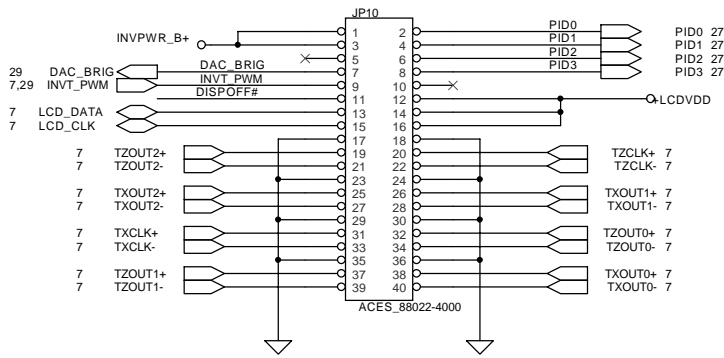
+3VS  
 Pull High: Default PAL  
 Pull Low: Default NTSC



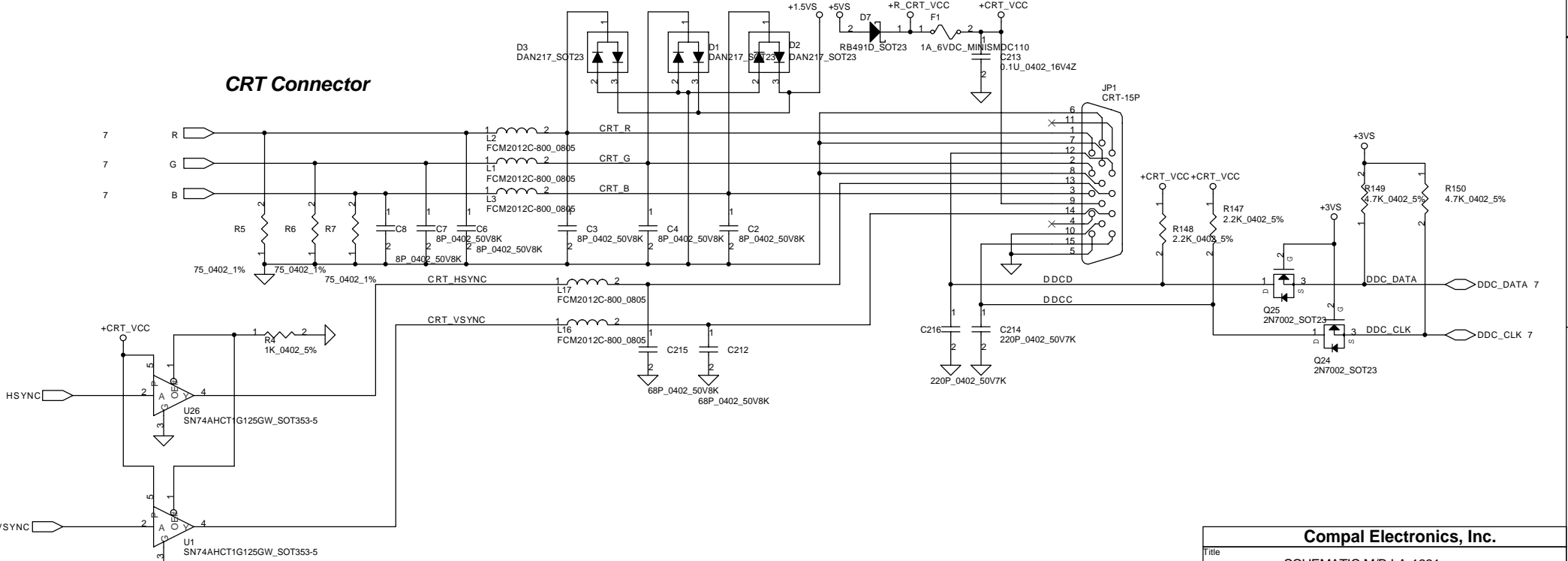
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### LVDS Connector



### CRT Connector



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14,22,23,24 PCI\_AD[0..31] PCI\_AD[0..31]

PCI_AD31	3	AD31
PCI_AD30	4	AD30
PCI_AD29	5	AD29
PCI_AD28	7	AD28
PCI_AD27	8	AD27
PCI_AD26	9	AD26
PCI_AD25	11	AD25
PCI_AD24	10	AD24
PCI_AD23	15	AD23
PCI_AD22	16	AD22
PCI_AD21	17	AD21
PCI_AD20	19	AD20
PCI_AD19	23	AD19
PCI_AD18	24	AD18
PCI_AD17	25	AD17
PCI_AD16	26	AD16
PCI_AD15	38	AD15
PCI_AD14	39	AD14
PCI_AD13	40	AD13
PCI_AD12	41	AD12
PCI_AD11	42	AD11
PCI_AD10	43	AD10
PCI_AD9	46	AD9
PCI_AD8	47	AD8
PCI_AD7	49	AD7
PCI_AD6	51	AD6
PCI_AD5	52	AD5
PCI_AD4	53	AD4
PCI_AD3	54	AD3
PCI_AD2	55	AD2
PCI_AD1	56	AD1
PCI_AD0	57	AD0

PQFP 144  
22.2 X 22.2 X 1.60

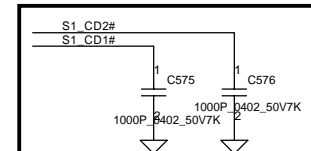
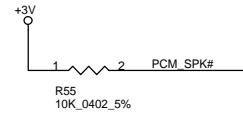
CAD31/D10	144	S1_D10
CAD30/D9	142	S1_D9
CAD29/D1	141	S1_D1
CAD28/D8	140	S1_D8
CAD27/D0	139	S1_D0
CAD26/A0	129	S1_A0
CAD25/A1	128	S1_A1
CAD24/A2	127	S1_A2
CAD23/A3	124	S1_A3
CAD22/A4	121	S1_A4
CAD21/A5	120	S1_A5
CAD20/A6	118	S1_A6
CAD19/A25	116	S1_A25
CAD18/A7	115	S1_A7
CAD17/A24	113	S1_A24
CAD16/A17	98	S1_A17
CAD15/IOVR#	96	S1_IOWR#
CAD14/A9	97	S1_A9
CAD13/IORD#	93	S1_IORD#
CAD12/A11	95	S1_A11
CAD11/OE#	92	S1_OE#
CAD10/CE2#	94	S1_CE2#
CAD9/A10	89	S1_A10
CAD8/D15	87	S1_D15
CAD7/D7	85	S1_D7
CAD6/D13	82	S1_D13
CAD5/D6	83	S1_D6
CAD4/D12	80	S1_D12
CAD3/D5	81	S1_D5
CAD2/D11	77	S1_D11
CAD1/D4	79	S1_D4
CAD0/D3	76	S1_D3

S1\_A[0..25] S1\_A[0..25] 21  
S1\_D[0..15] S1\_D[0..15] 21

14,22,23,24 PCI_C/BE#3	12	C/BE3#
14,22,23,24 PCI_C/BE#2	27	C/BE2#
14,22,23,24 PCI_C/BE#1	37	C/BE1#
14,22,23,24 PCI_C/BE#0	48	C/BE0#
7,14,18,21,22,23,24,25,27 PCIRST#	20	RST#
14,22,23,24 PCI_FRAME#	28	FRAME#
14,22,23,24 PCI_IRDY#	29	IRDY#
14,22,23,24 PCI_TRDY#	31	TRDY#
14,22,23,24 PCI_DEVSEL#	32	DEVSEL#
14,22,23,24 PCI_STOP#	33	STOP#
14,22,23,24 PCI_PERR#	34	PERR#
14,22,24 PCI_SERR#	35	SERR#
14,22,23,24 PCI_PAR#	36	PAR#
14 PCI_REQ#2	1	REQ#
14 PCI_GNT#2	2	GNT#
13 CLK_PCI_PCM	21	CLK

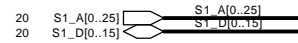
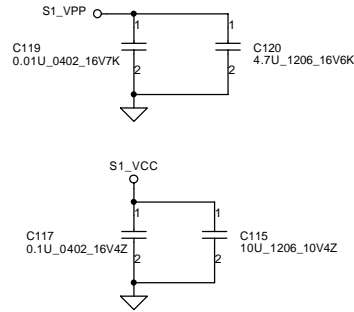
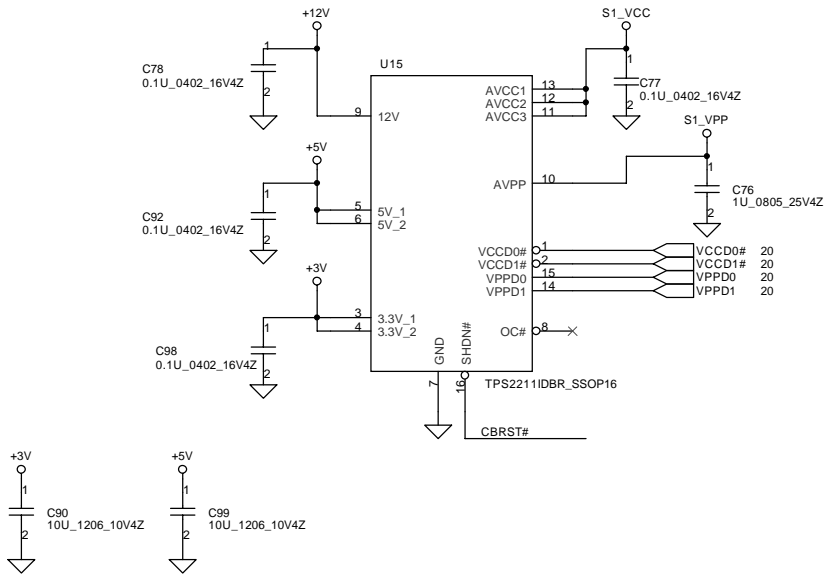
22,23,24,29 PCM_PME#	58	RI_OUT#/PME#
29,30,34,39,42,43 SUSP#	70	SUSPEND#
PCI_AD20	1	IDSEL
100_0402_1% R254	13	PCM_ID
PCI_PIRQA#	60	MFUNC0
100_0402_5% R437	61	MFUNC1
29 PCM_RI#	64	MFUNC2
14,25,27,29 SIRQ	65	MFUNC3
67	67	MFUNC4
68	68	MFUNC5
69	69	MFUNC6
15,22,24,27,29 PM_CLKRUN#	66	VCC/GRST#
21 CBRST#	66	

CC/BE3#/REG#	125	S1_REG#
CC/BE2#/A12	112	S1_A12
CC/BE1#/A8	99	S1_A8
CC/BE0#/CE1#	88	S1_CE1#
119	119	S1_RST
CRST#/RESET	111	S1_A23
CFRAME#/A23	110	S1_A15
CIRDY#/A15	110	S1_A22
CTRDY#/A22	107	S1_A21
CDEVSEL#/A21	105	S1_A20
CSTOP#/A20	104	S1_A14
CPERR#/A14	104	S1_A14
CSERR#/WAIT#	133	S1_WAIT#
CPAR/A13	101	S1_A13
CPAR/A13	101	S1_INPACK#
CREQ#/INPACK#	106	S1_WE#
CGNT#/WE#	108	A16_CLK
CCLK/A16	108	A16_CLK
135	135	S1_BVD1
CSTSCHG/BVD1	136	S1_WP
CLKRUN#/WP	136	S1_WP
103	103	S1_A19
CBLOCK#/A19	103	S1_A19
132	132	S1_RDY#
CINT#/READY	132	S1_RDY#
62	62	PCM_SPK#
SPKOUT	62	PCM_SPK#
134	134	S1_BVD2
CAUDIO/BVD2	134	S1_BVD2
137	137	S1_CD2#
CCD2#/CD2#	137	S1_CD2#
CCD1#/CD1#	125	S1_CD1#
117	117	S1_VS2
CVS2/VS2#	117	S1_VS2
131	131	S1_VS1
CVS1/VS1#	131	S1_VS1

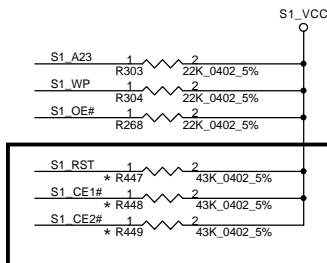
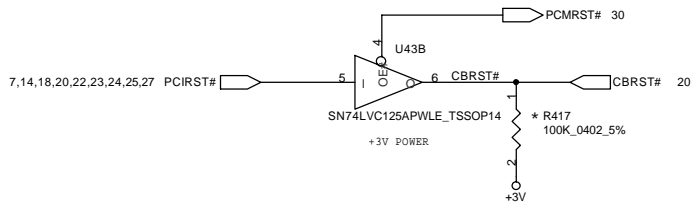
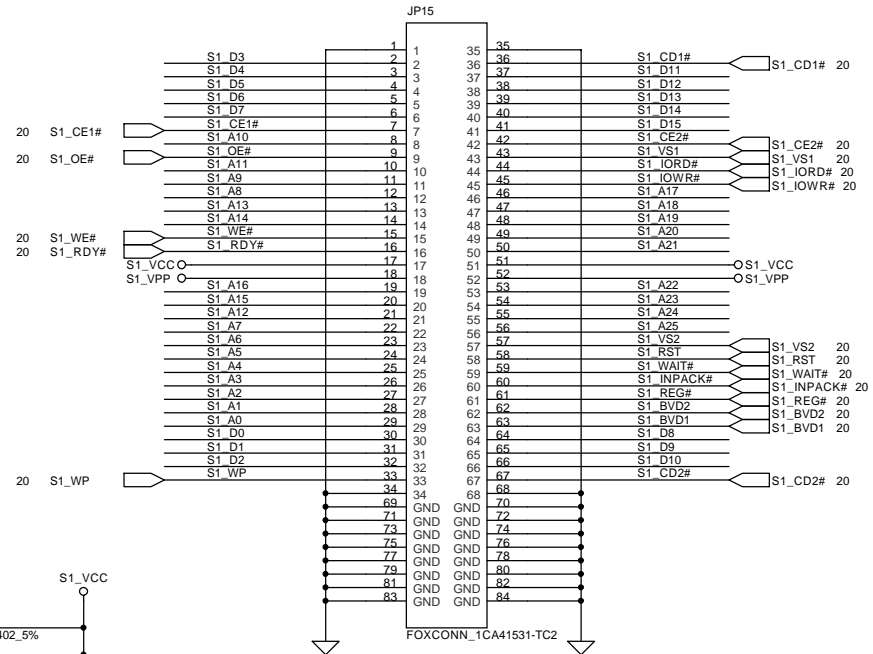


Reserve for CB1410 B0 Version

# PCMCIA Power Controller



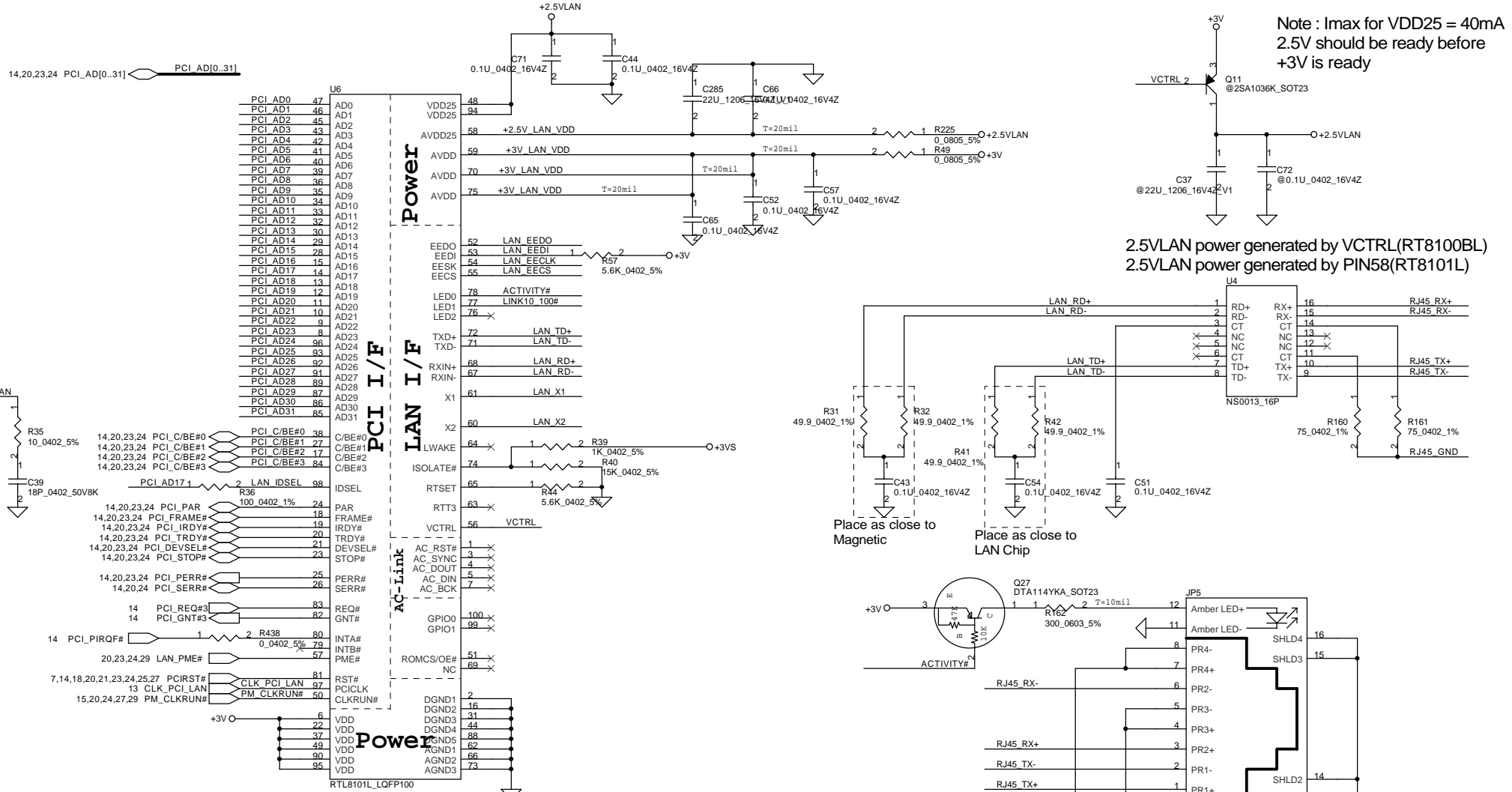
# CardBus Socket



Reserve for CB1410 B0 Version

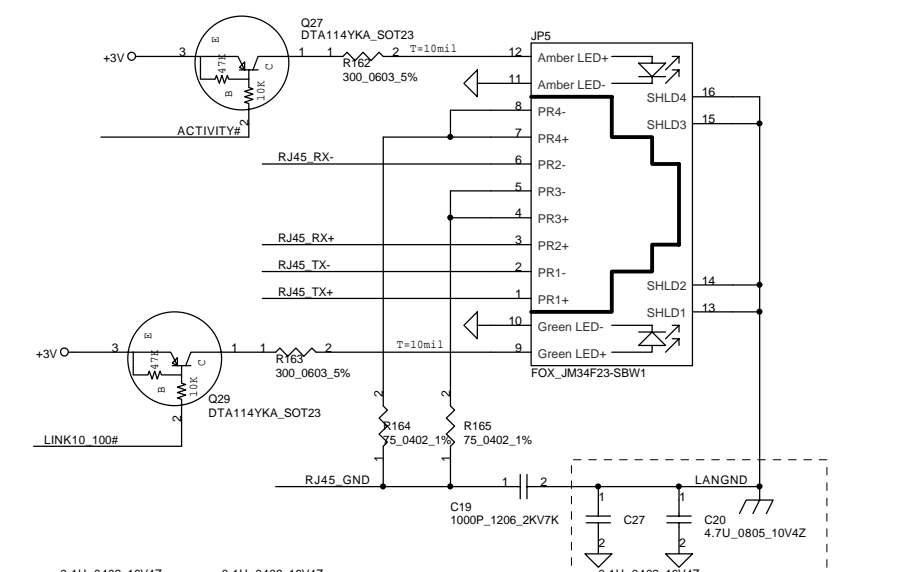
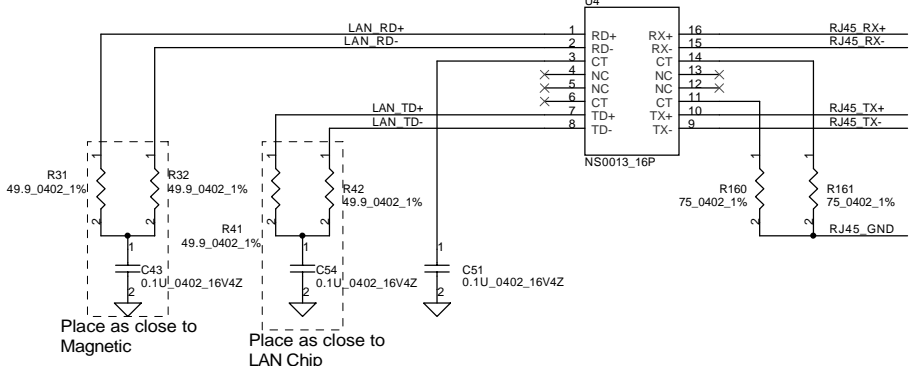
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Note : I<sub>max</sub> for VDD25 = 40mA  
2.5V should be ready before  
+3V is ready

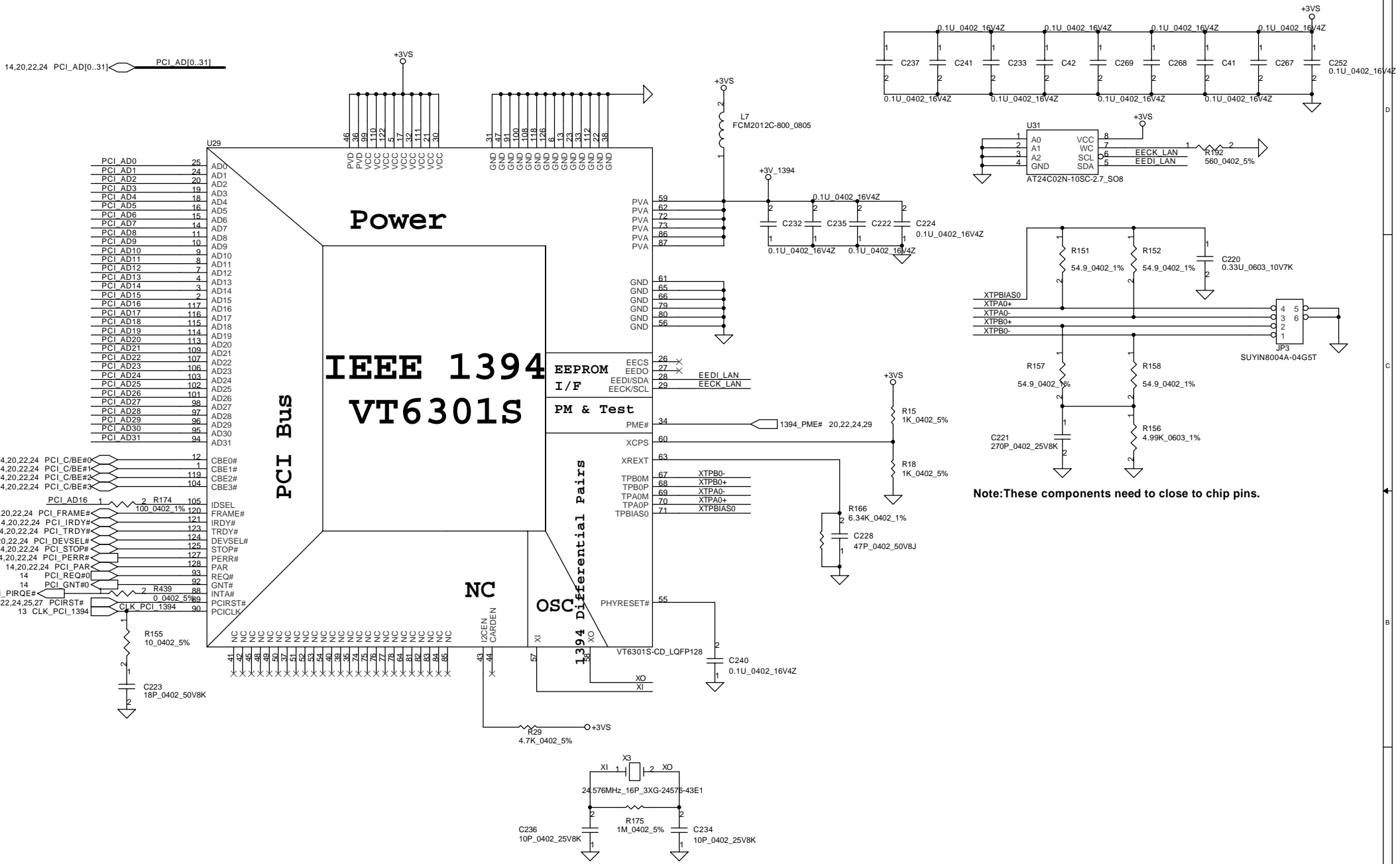
2.5VLAN power generated by VCTRL(RT8100BL)  
2.5VLAN power generated by PIN58(RT8101L)



Termination plane should be copied to chassis ground and also depends on safety concern

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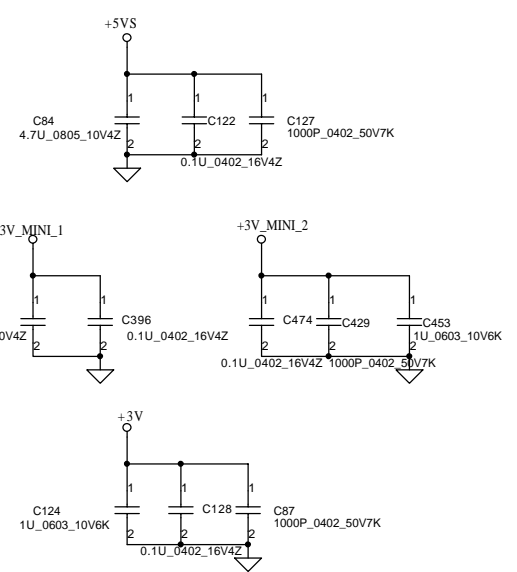
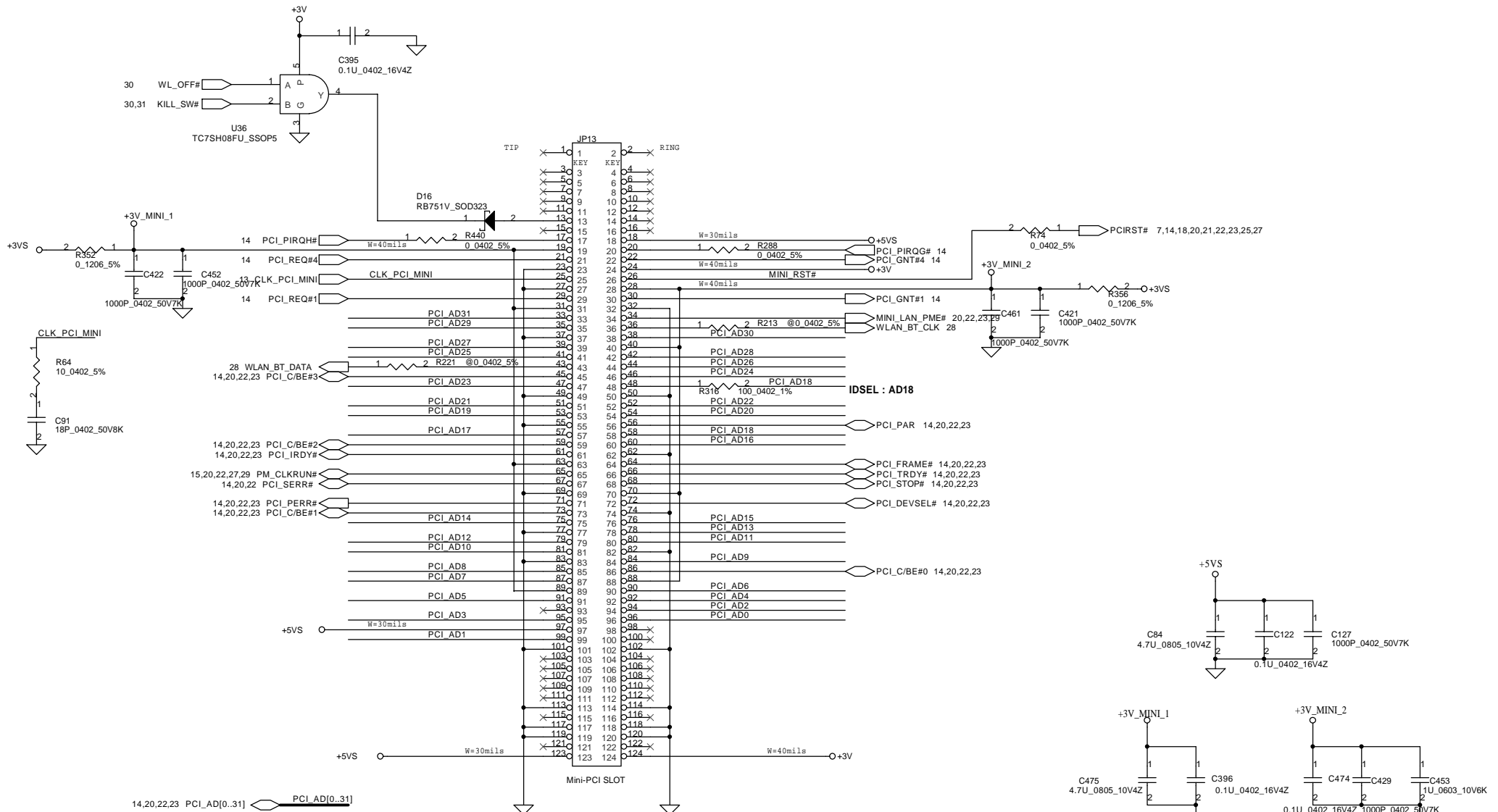
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Note: These components need to close to chip pins.

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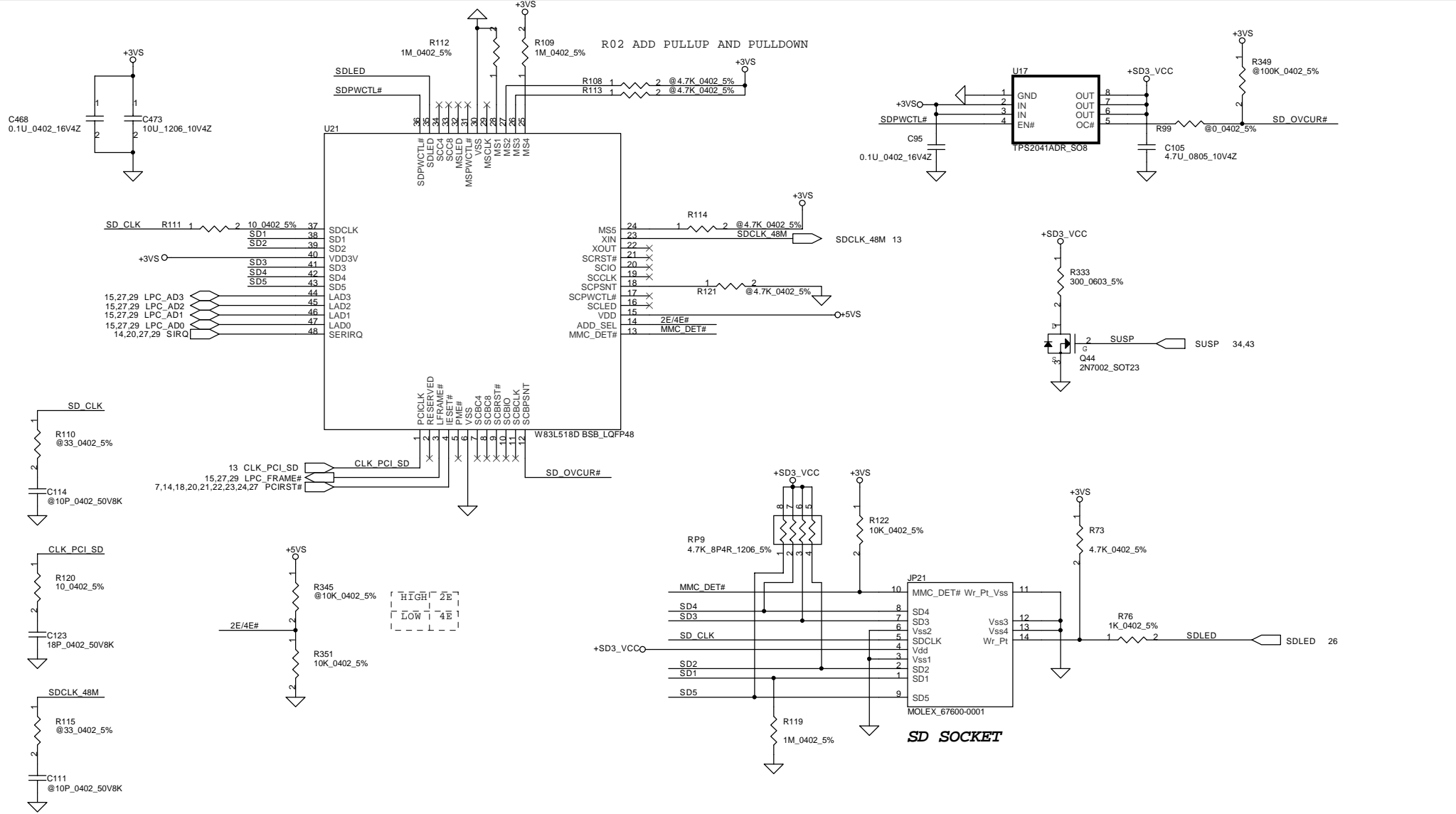
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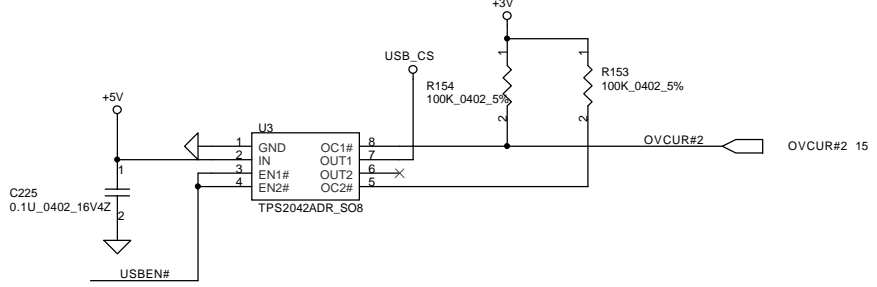
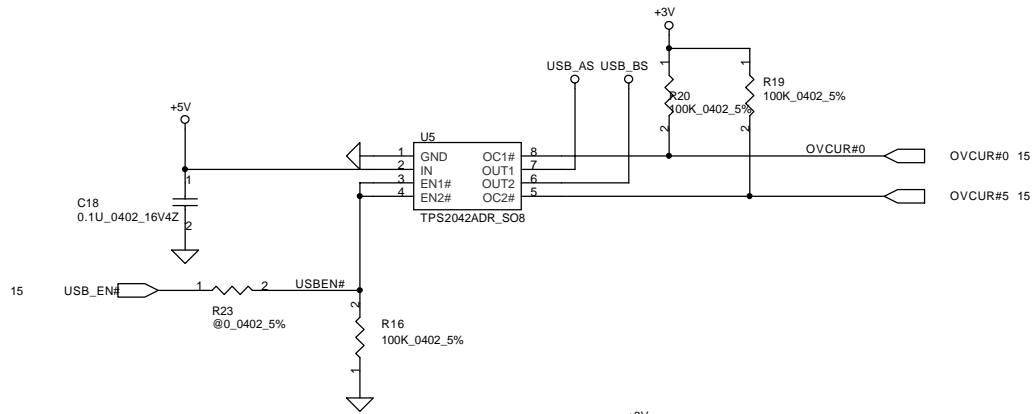
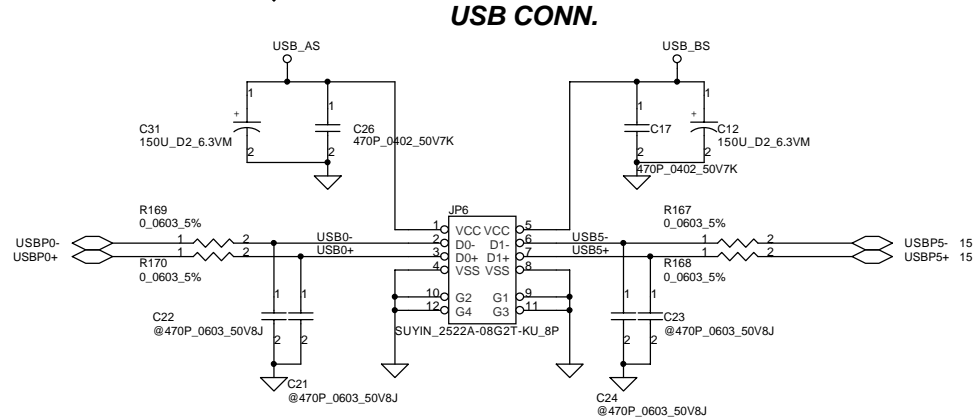
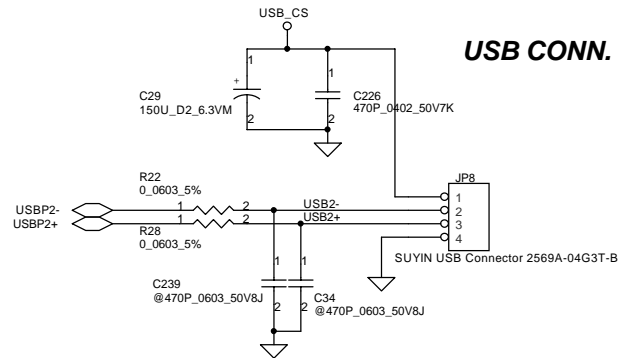


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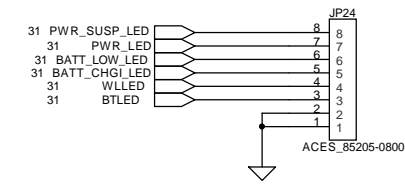
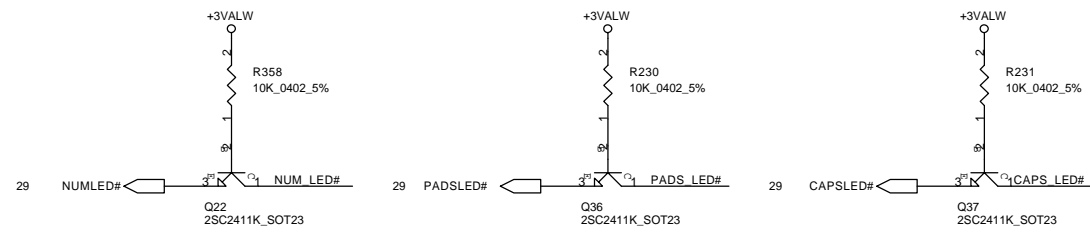
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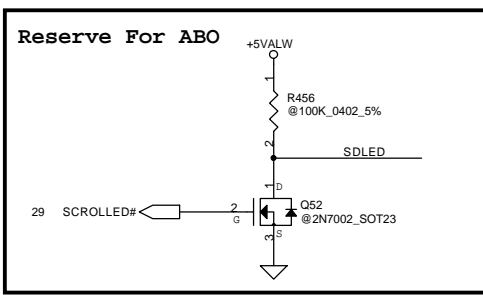
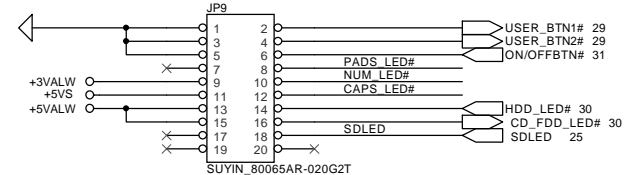




### LED/B CONN.



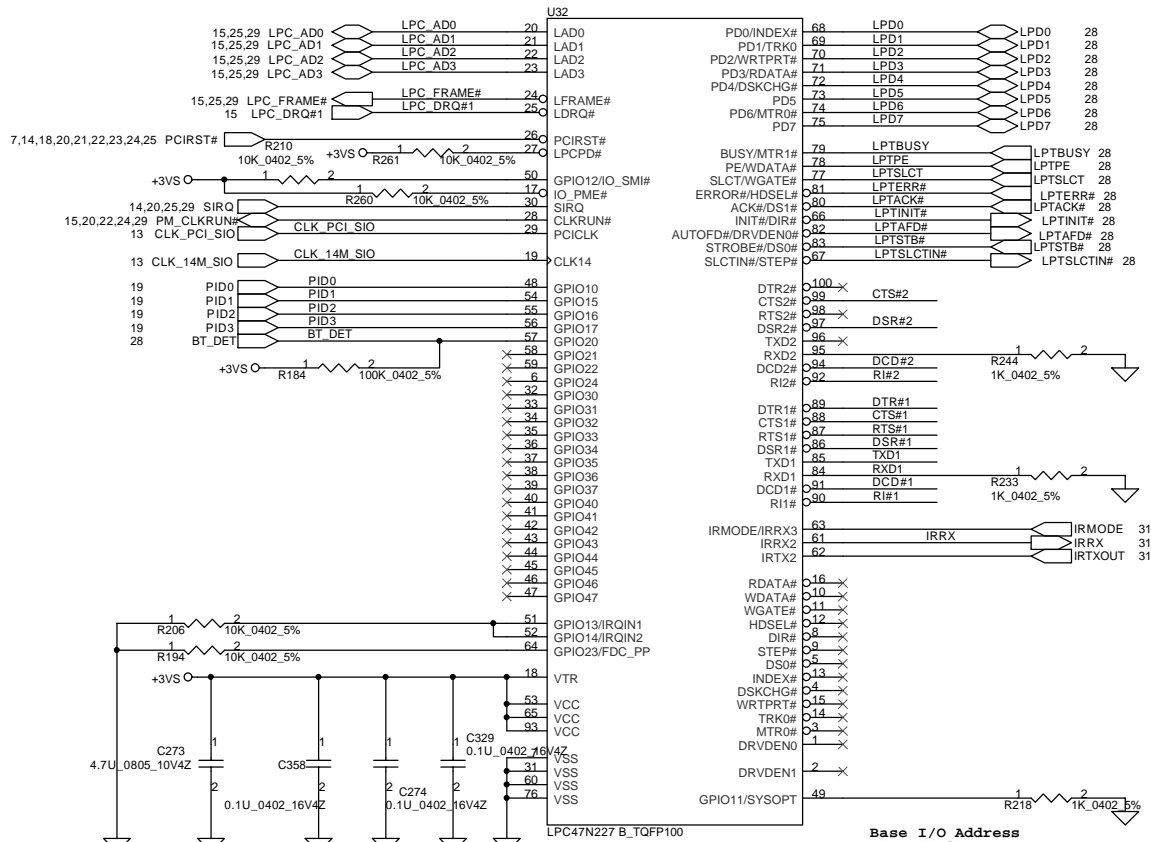
### POWER/B CONN.



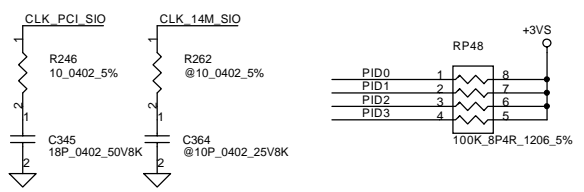
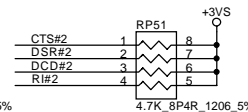
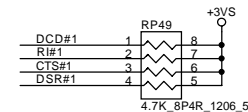
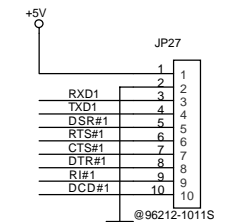
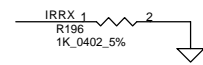
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# SUPER I/O SMC FDC47N227



Base I/O Address  
 \* 0 = 02Eh  
 1 = 04Eh

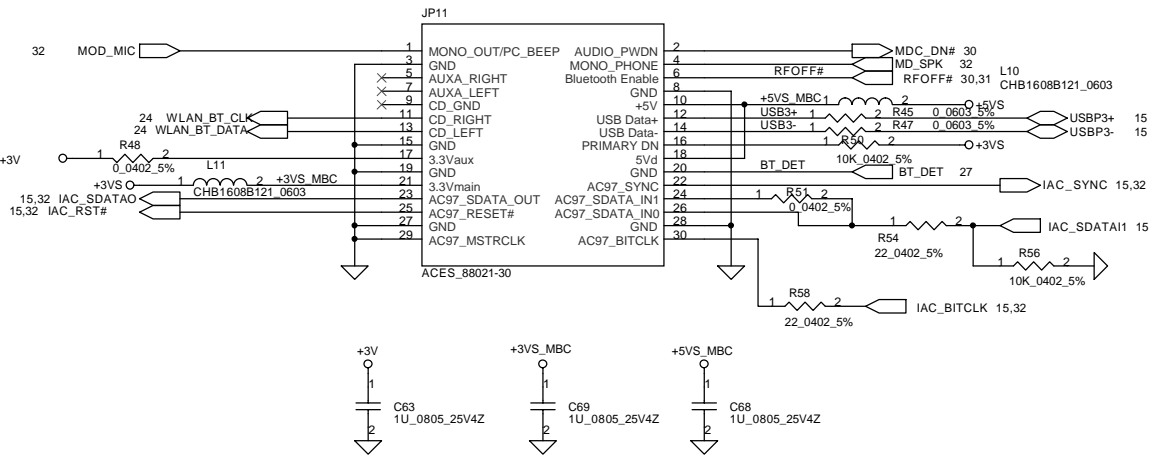


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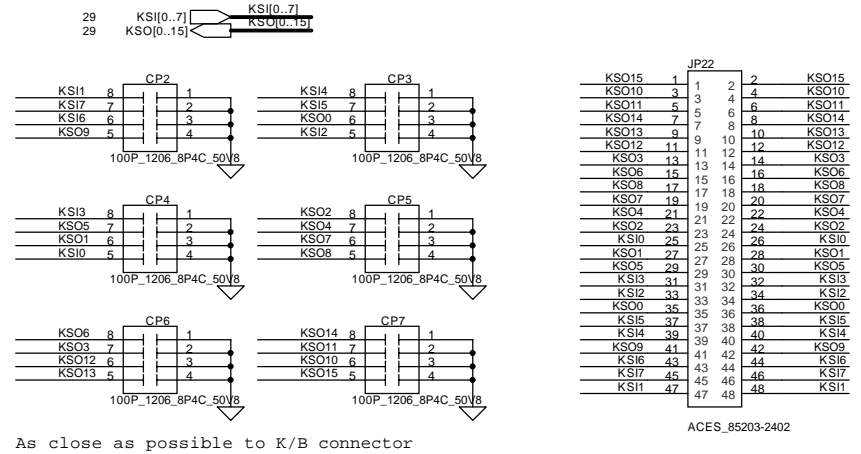
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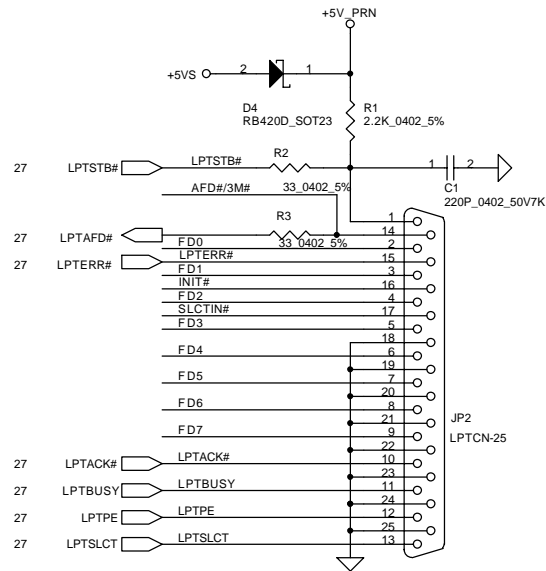
### MBC CONN.



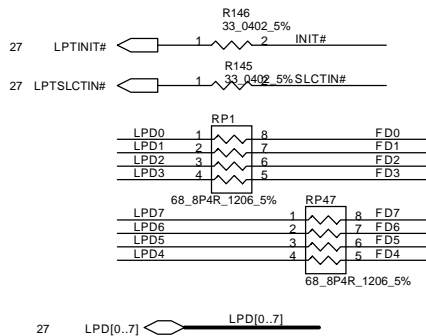
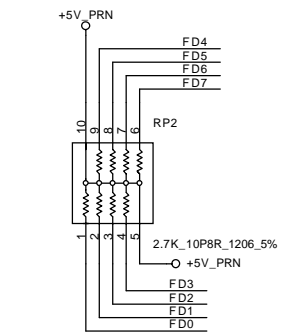
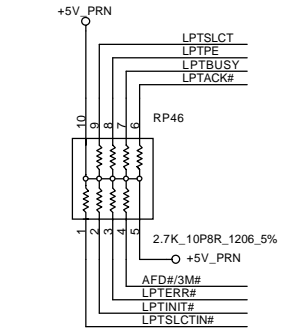
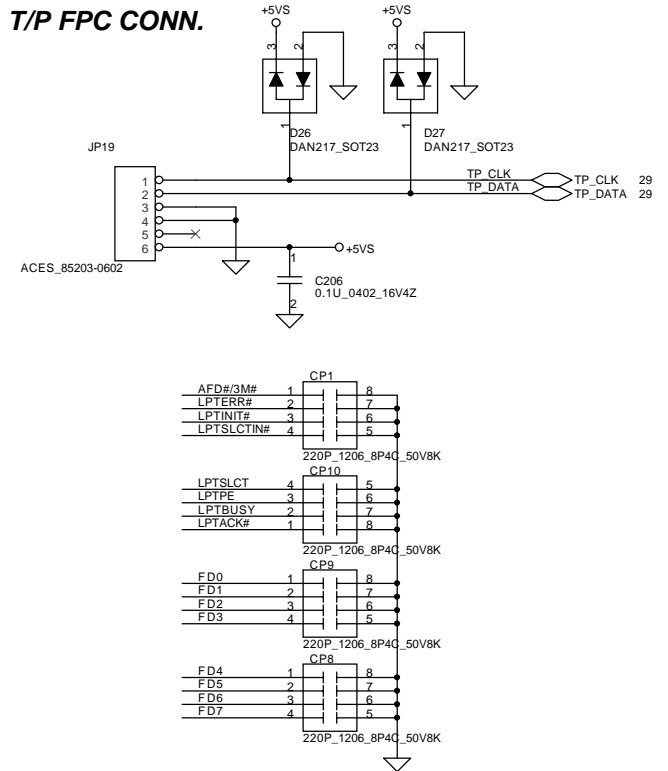
### INT\_KBD CONN.



### PARALLEL PORT



### T/P FPC CONN.

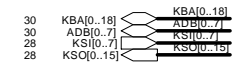
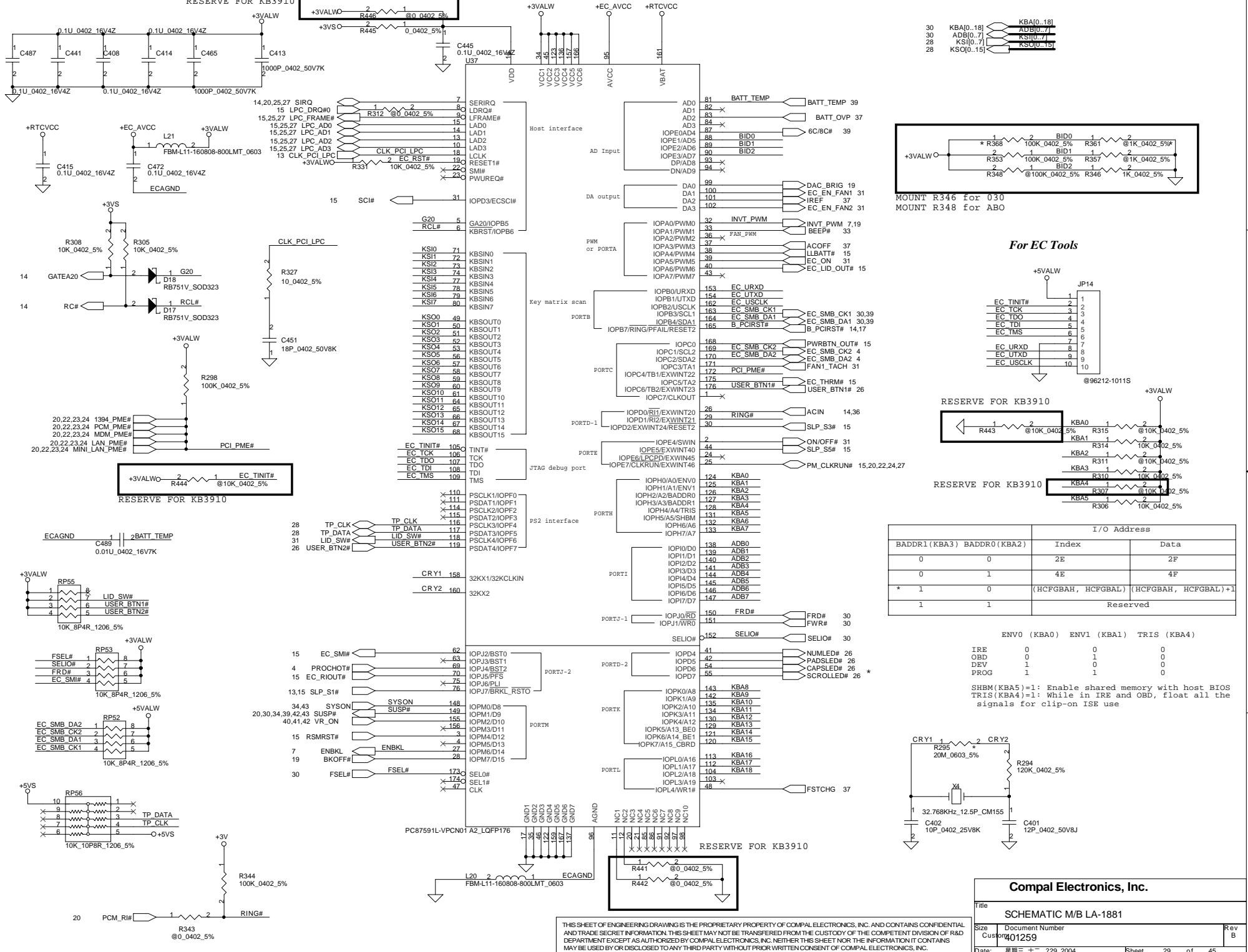


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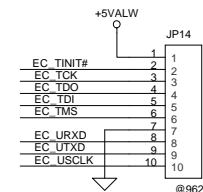
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RESERVE FOR KB3910



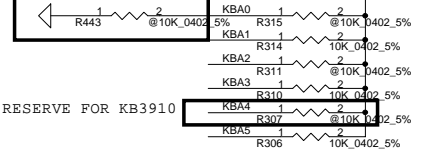
MOUNT R346 for 030  
MOUNT R348 for ABO

**For EC Tools**



@96212-1011S

RESERVE FOR KB3910



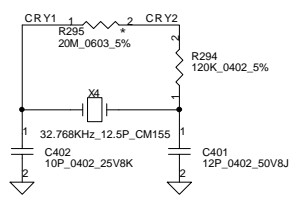
RESERVE FOR KB3910

I/O Address		Index	Data
BADDR1 (KBA3)	BADDR0 (KBA2)	2E	2F
0	0	4E	4F
* 1	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
1	1	Reserved	

ENV0 (KBA0) ENV1 (KBA1) TRIS (KBA4)

IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS  
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on use



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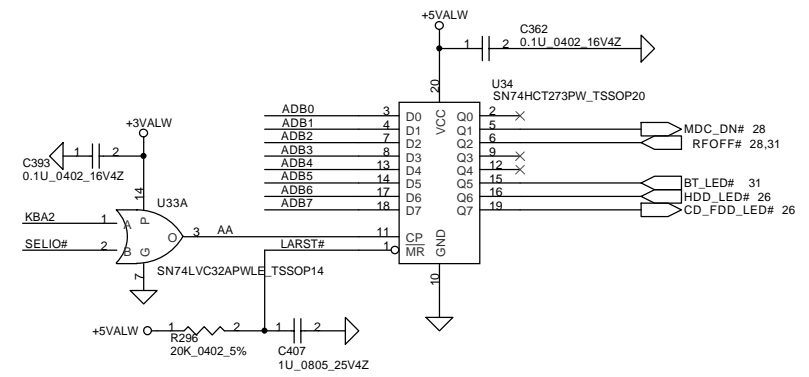
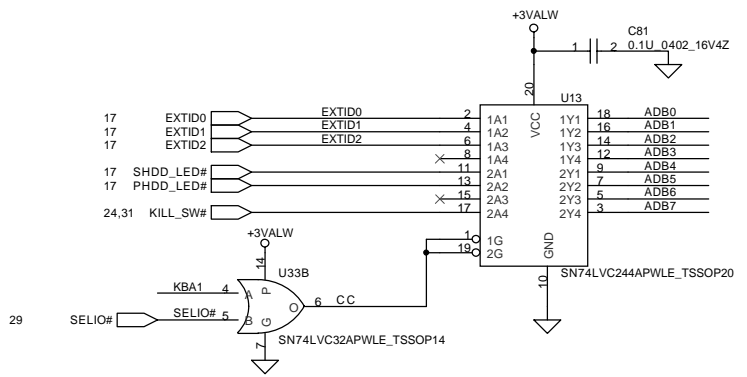
Customer: 401259

Date: 星期二 十二月 29, 2004

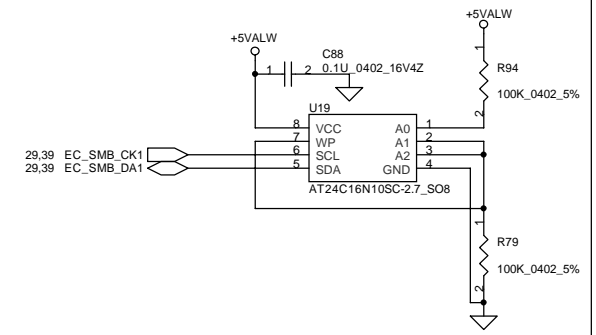
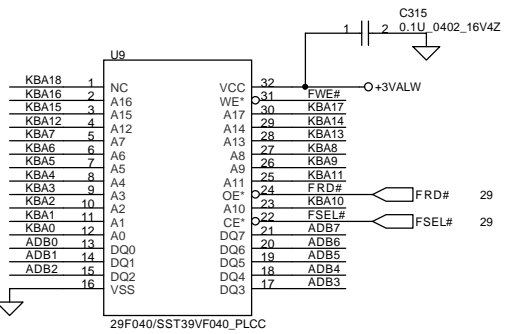
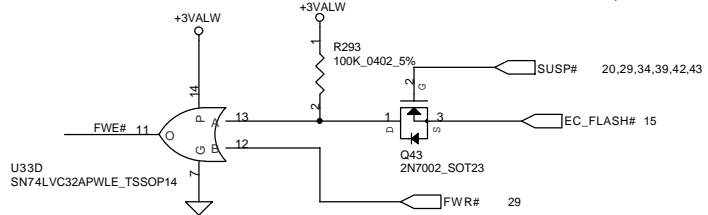
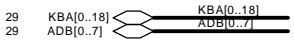
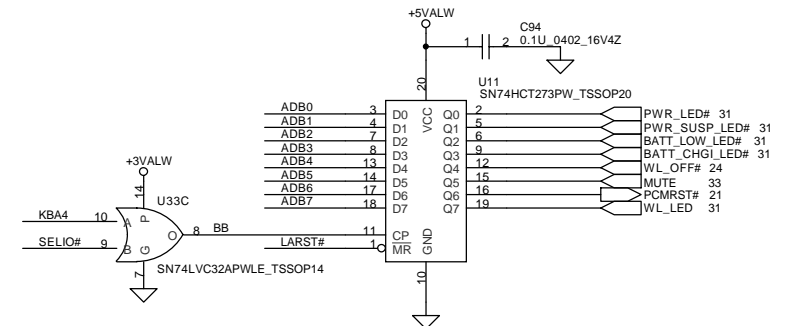
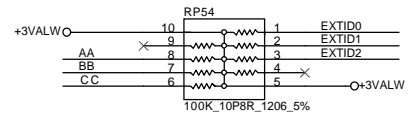
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Rev: B

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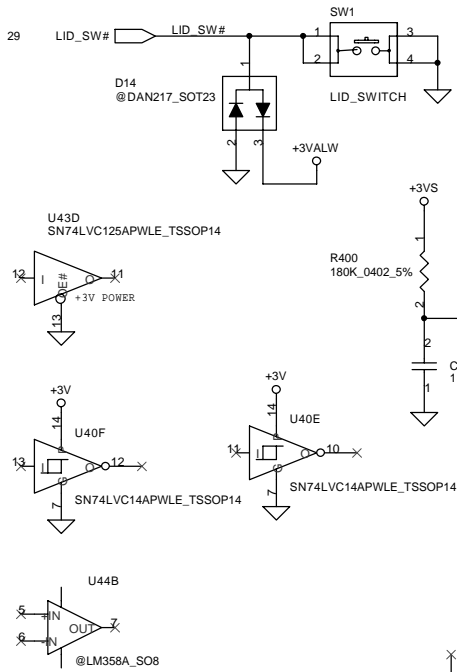


EXTID2	EXTID1	EXTID0	Module
0	0	0	FDD
0	0	1	CDROM
0	1	1	2ndHDD
1	1	1	NO Module

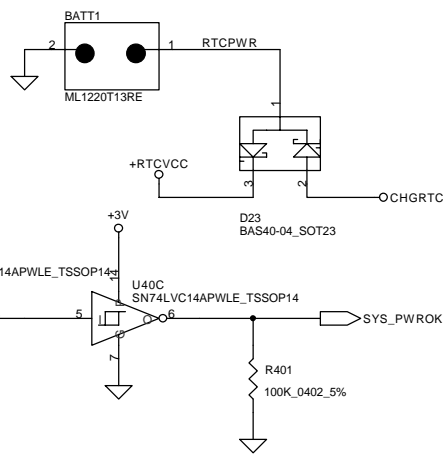


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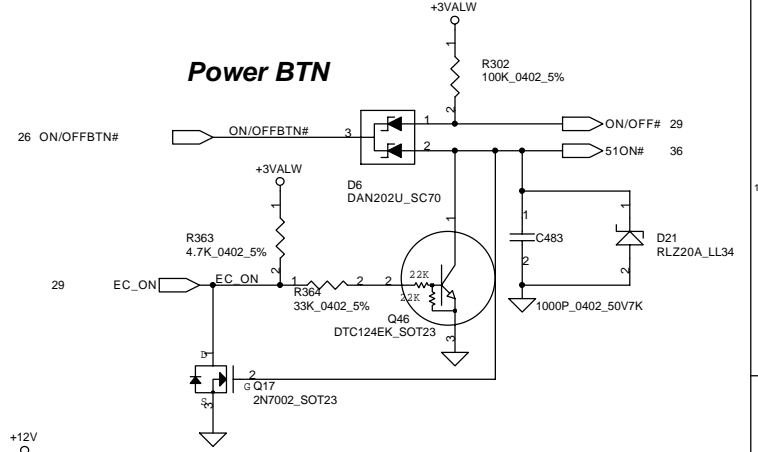
### Power ON Circuit



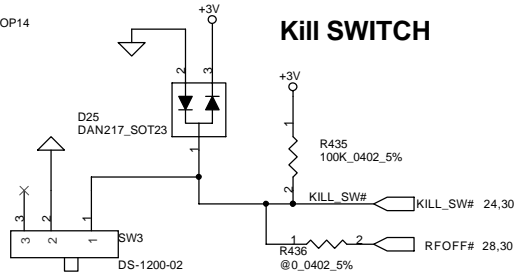
### RTC Battery



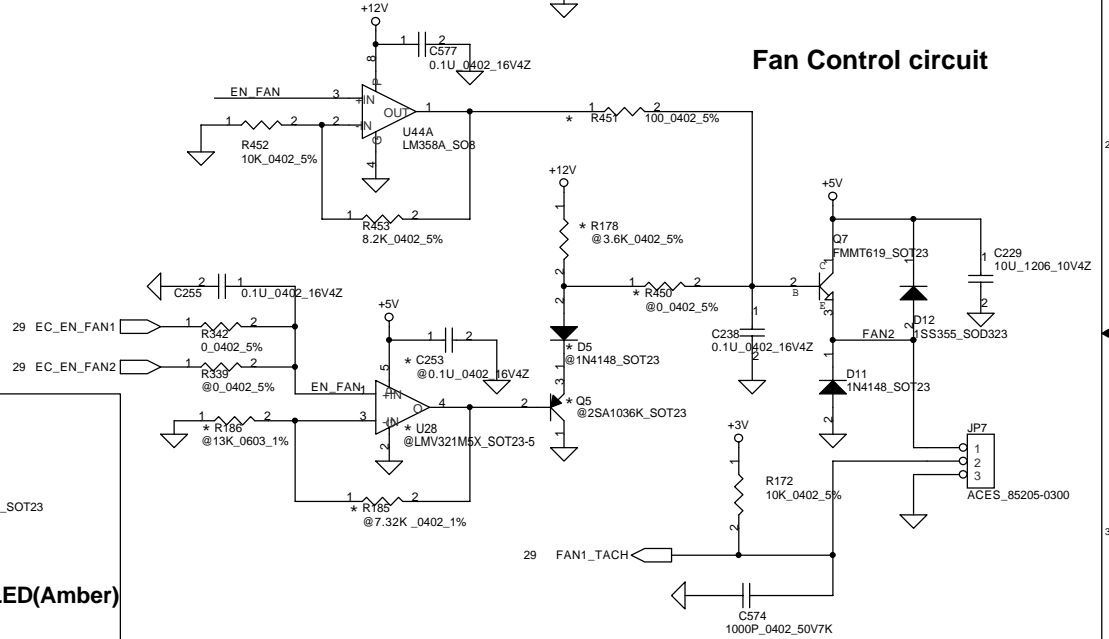
### Power BTN



### Kill SWITCH

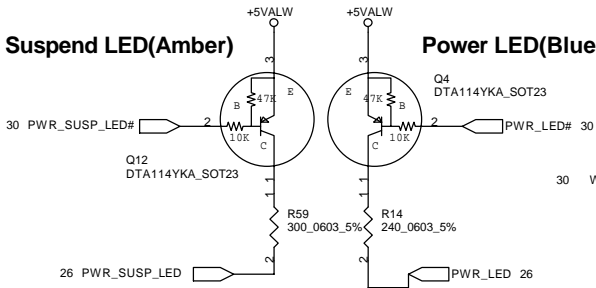


### Fan Control circuit

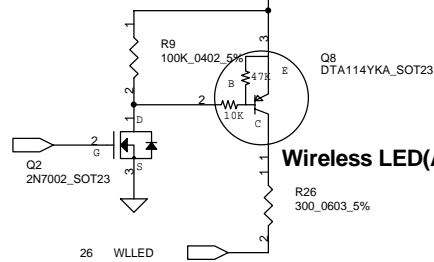


### Suspend LED(Amber)

### Power LED(Blue)

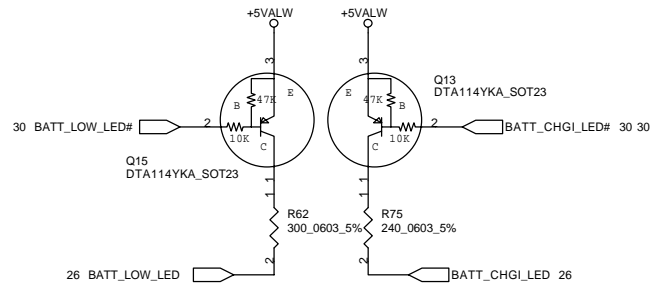


### Wireless LED(Amber)

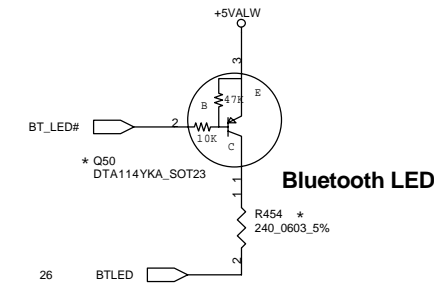


### BATT Low LED(Amber)

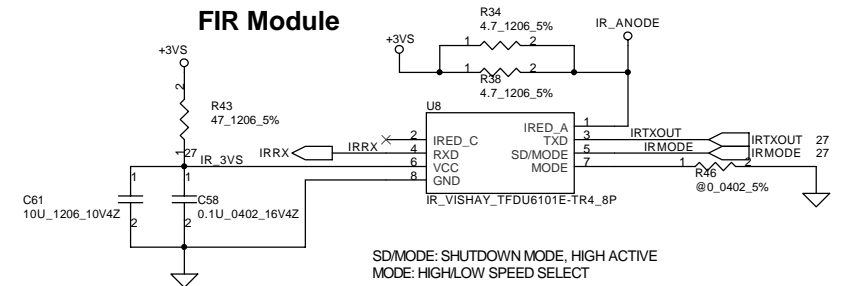
### BATT Charge LED(Blue)



### Bluetooth LED(Blue)



### FIR Module



SD/MODE: SHUTDOWN MODE, HIGH ACTIVE  
MODE: HIGH/LOW SPEED SELECT

### BATT Low LED(Amber)

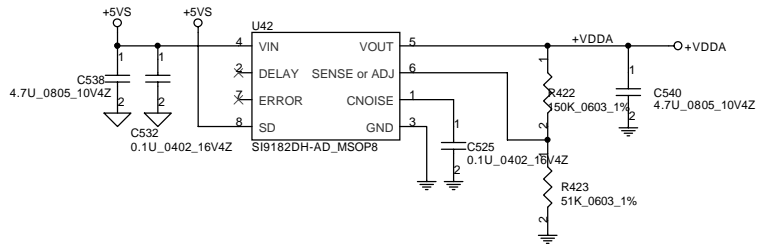
### BATT Charge LED(Blue)

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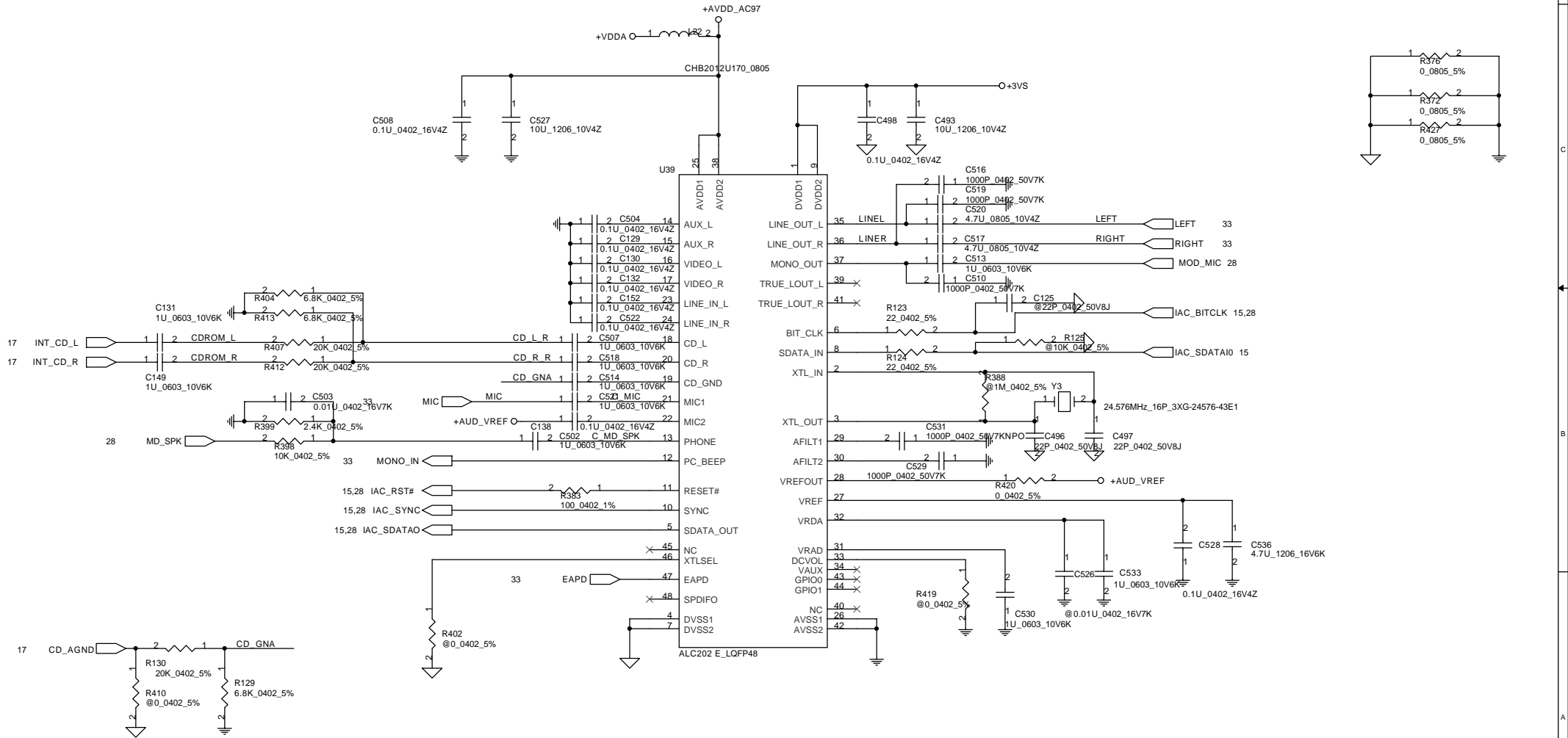
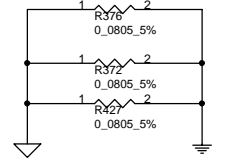
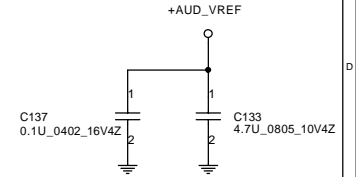
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# AC97 Codec



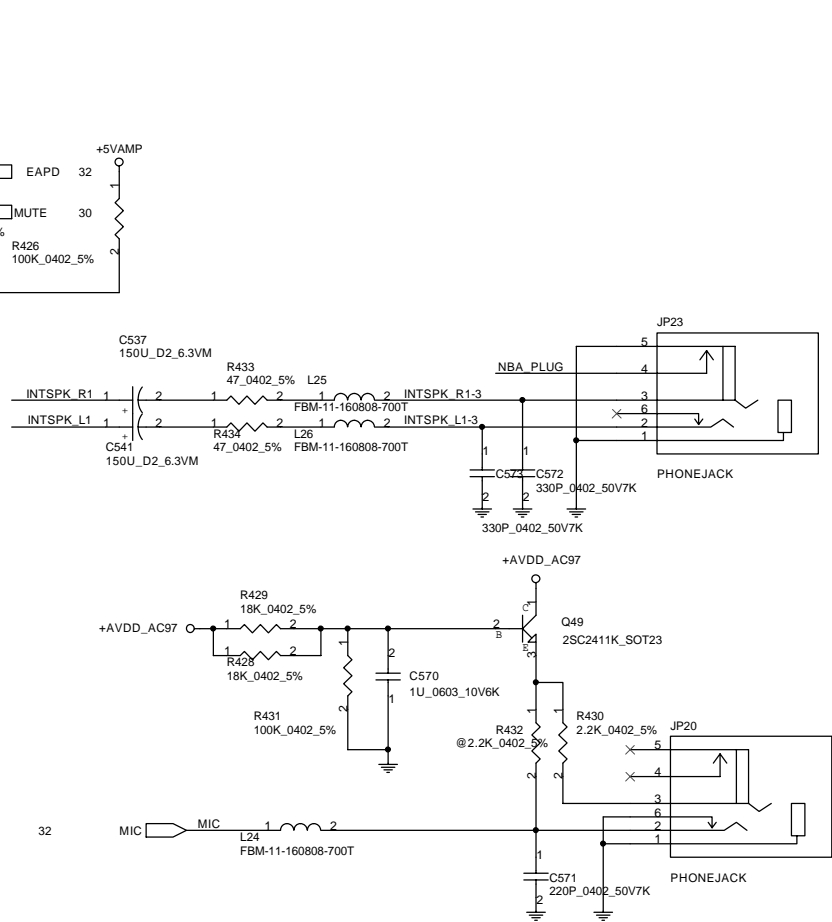
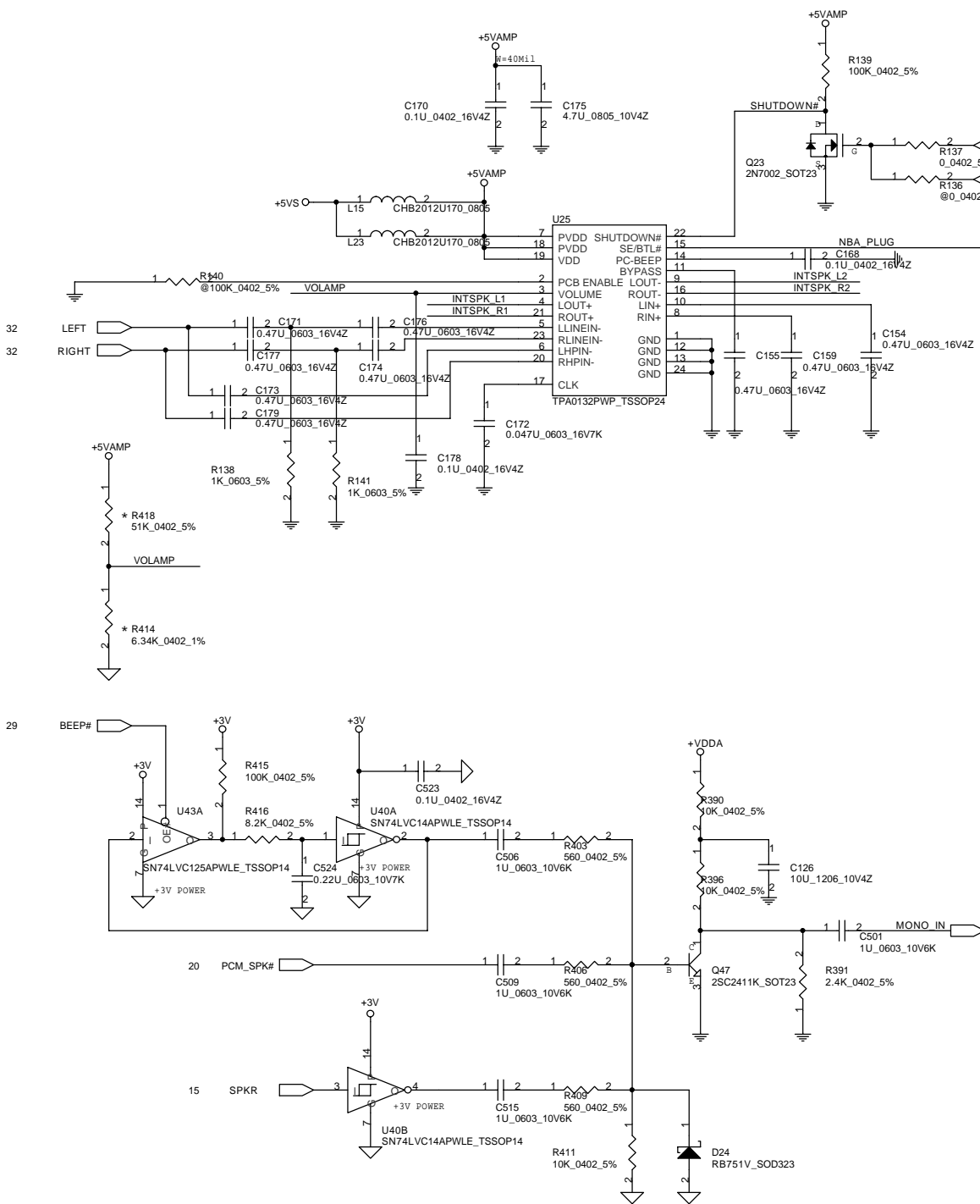
R402	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



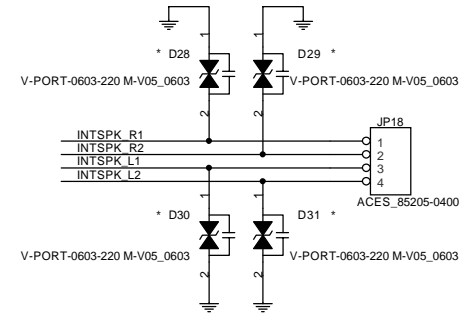
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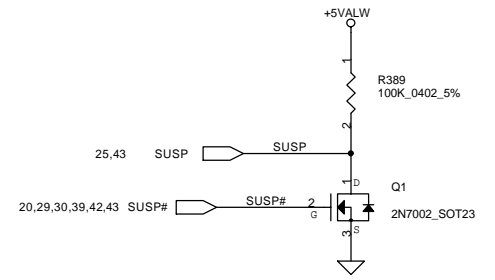
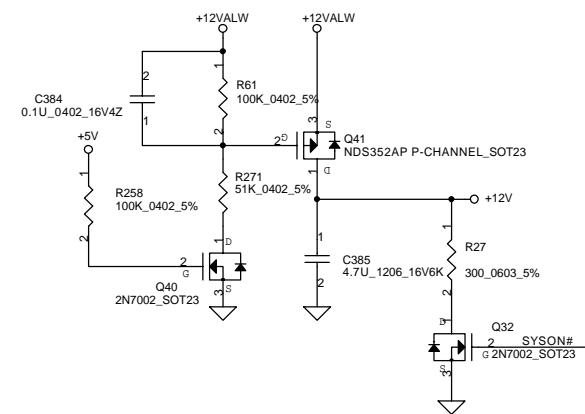
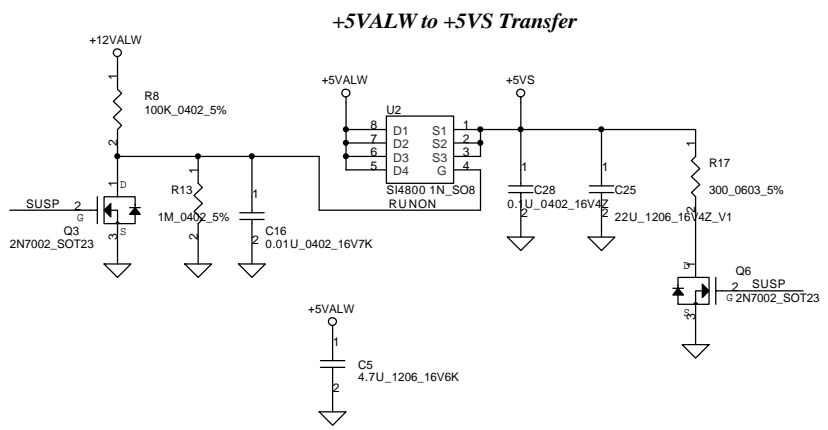
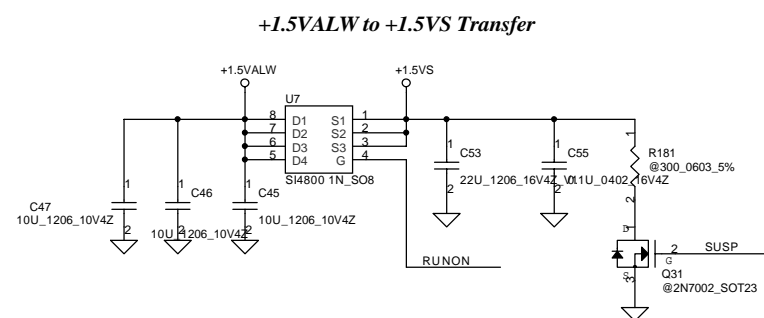
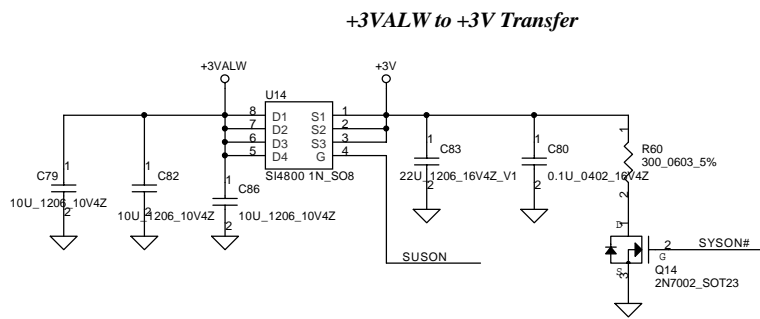
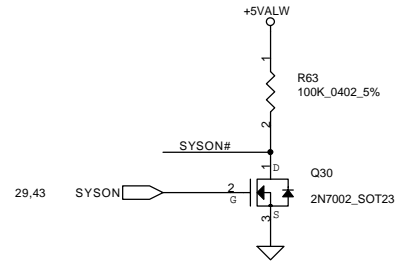
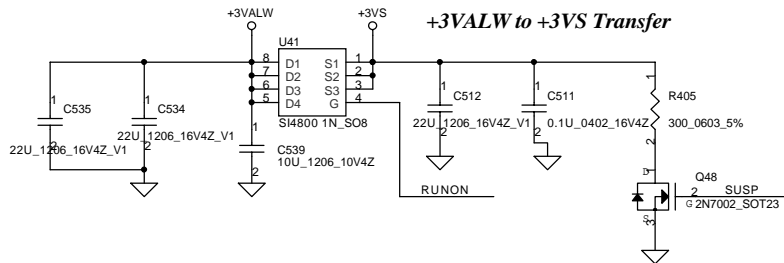
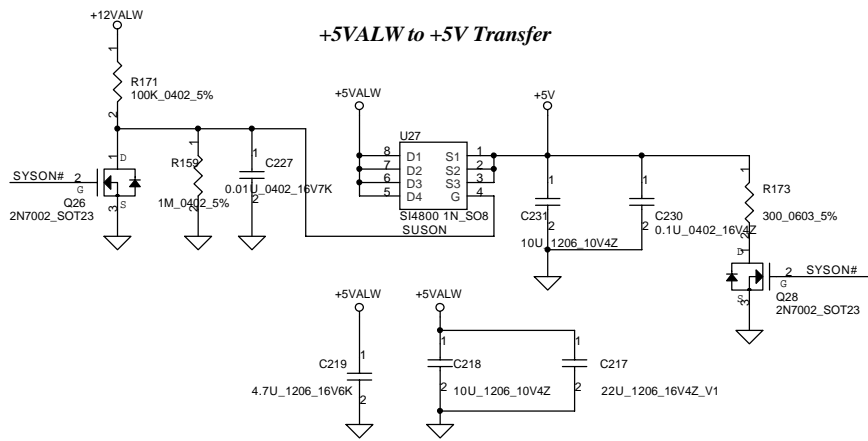


**SPEAKER CONN.**



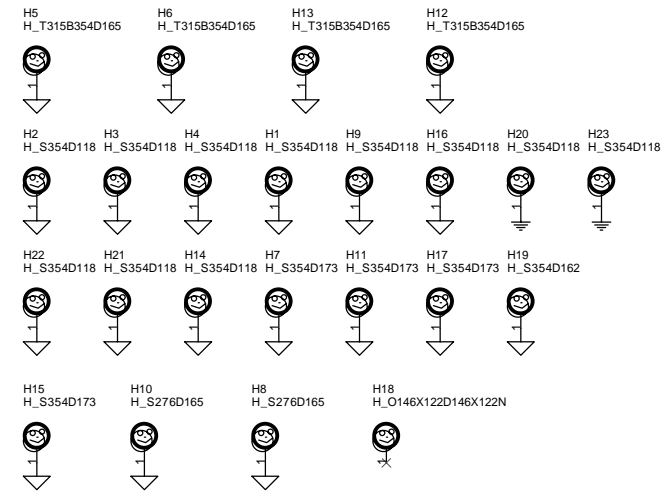
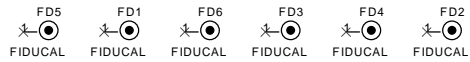
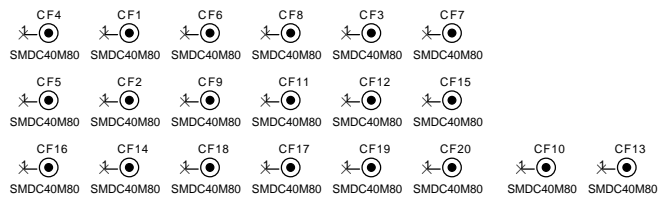
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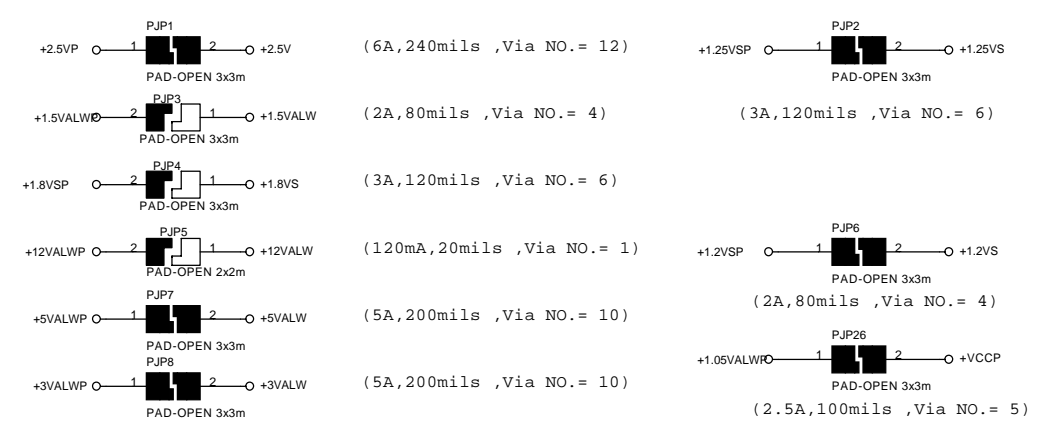
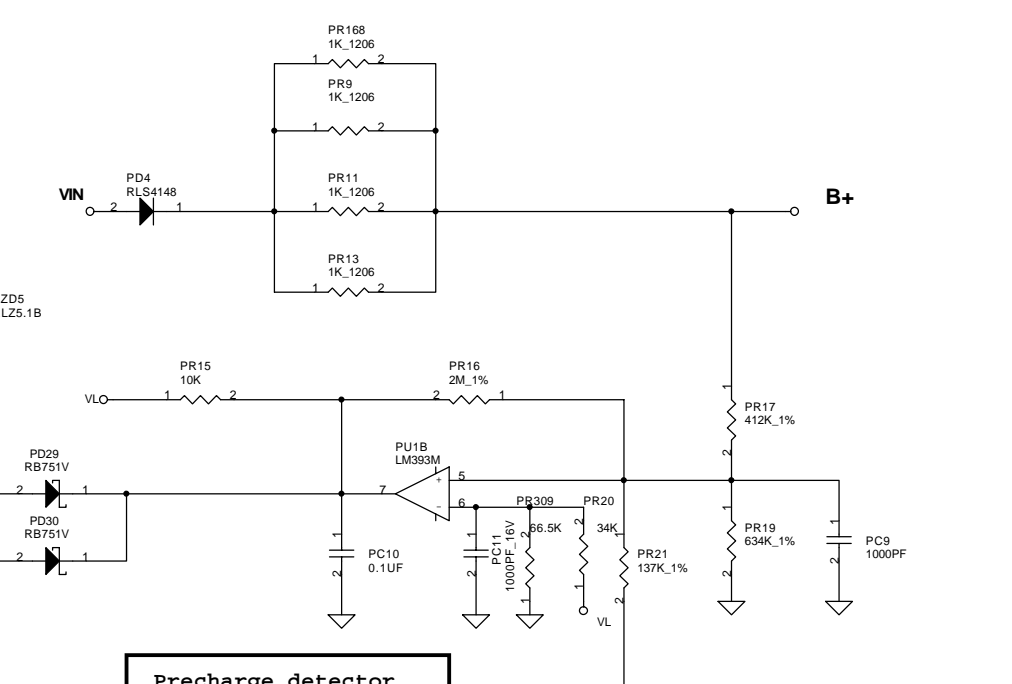
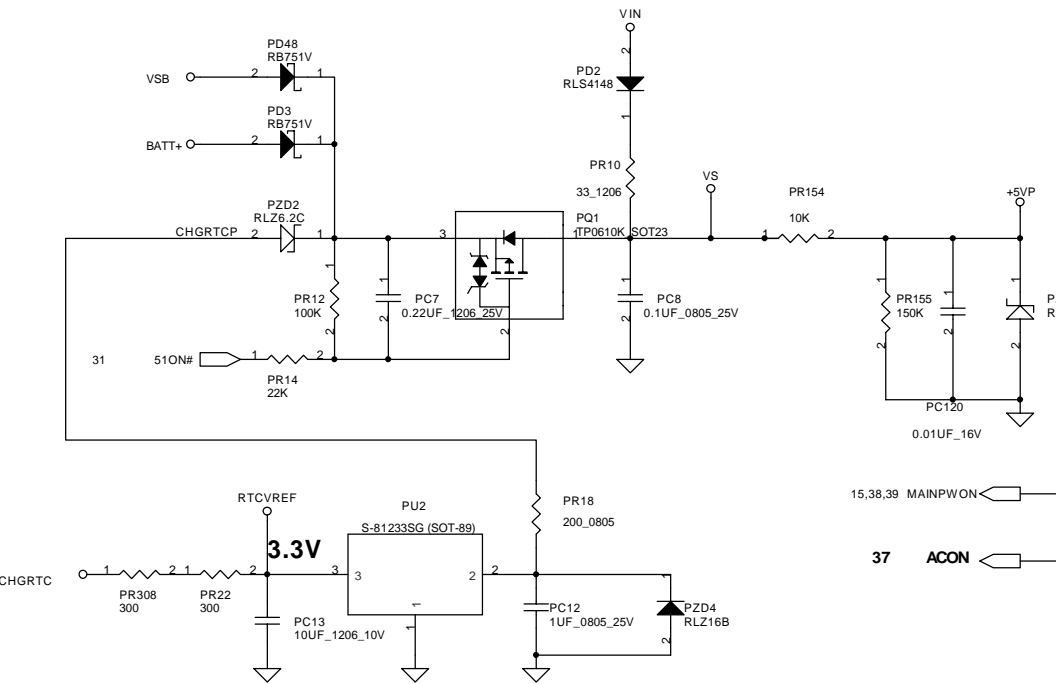
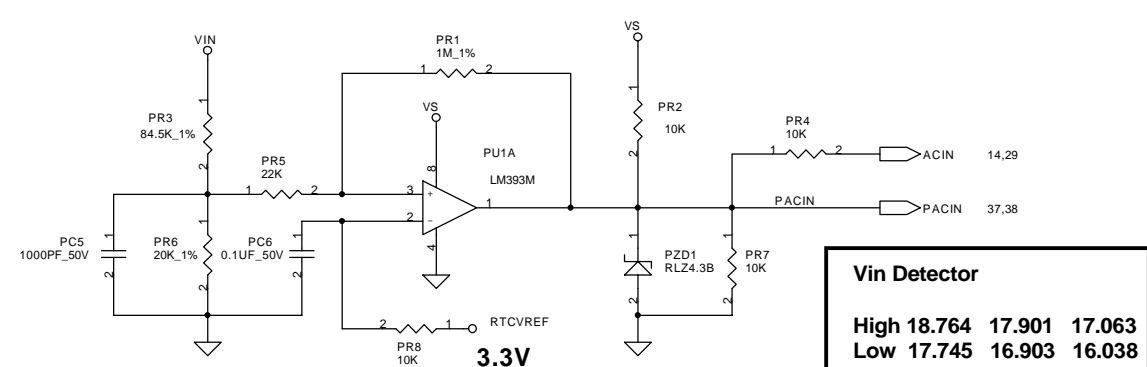
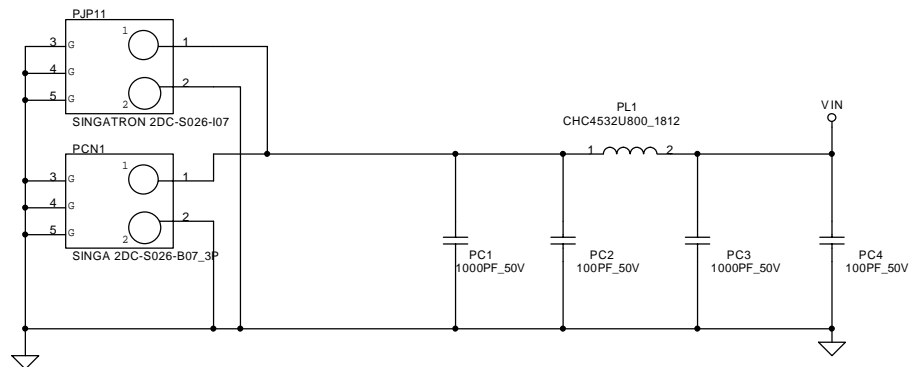
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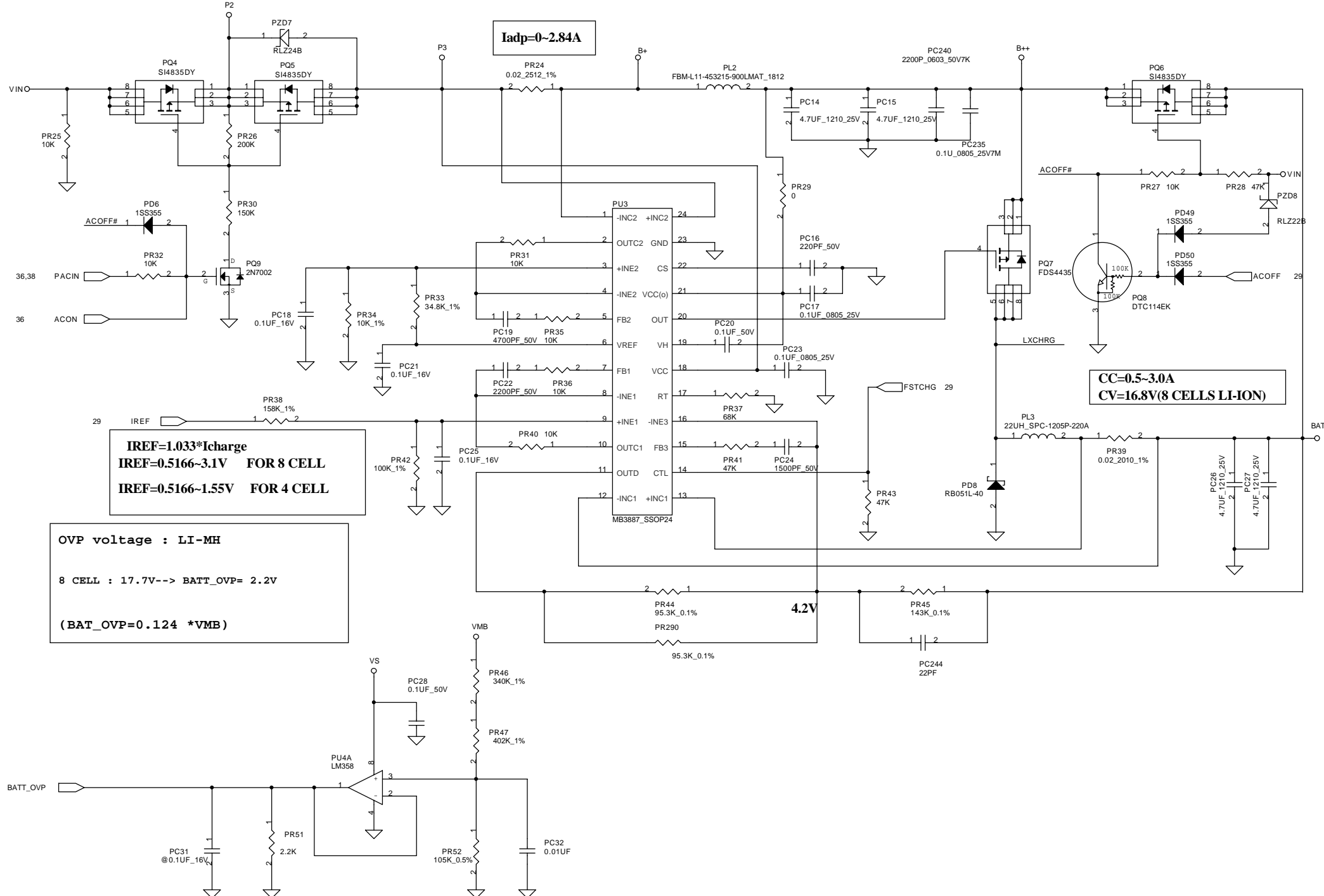
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<b>Precharge detector</b>			
<b>AC ADAPTOR</b>			
16.69	16.05	15.42	
15.6	15.02	14.35	

<b>Precharge detector</b>			
<b>AC ADAPTOR</b>			
6.33	6.12	5.92	
5.227	5.09	4.85	

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**Iadp=0-2.84A**

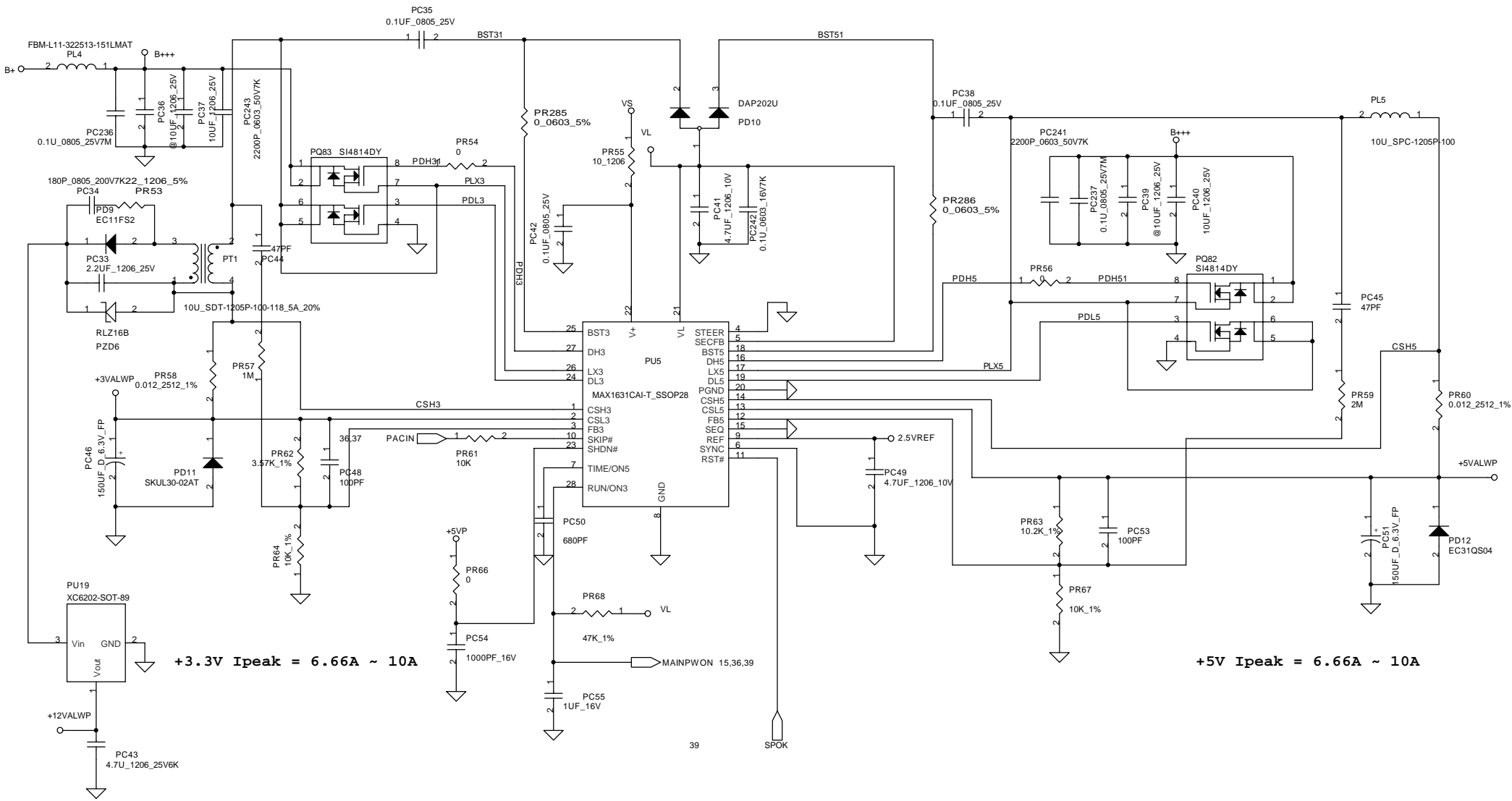
**CC=0.5-3.0A  
CV=16.8V(8 CELLS LI-ION)**

**IREF=1.033\*Icharge  
IREF=0.5166-3.1V FOR 8 CELL  
IREF=0.5166-1.55V FOR 4 CELL**

**OVP voltage : LI-MH  
8 CELL : 17.7V--> BATT\_OVP= 2.2V  
(BAT\_OVP=0.124 \*VMB)**

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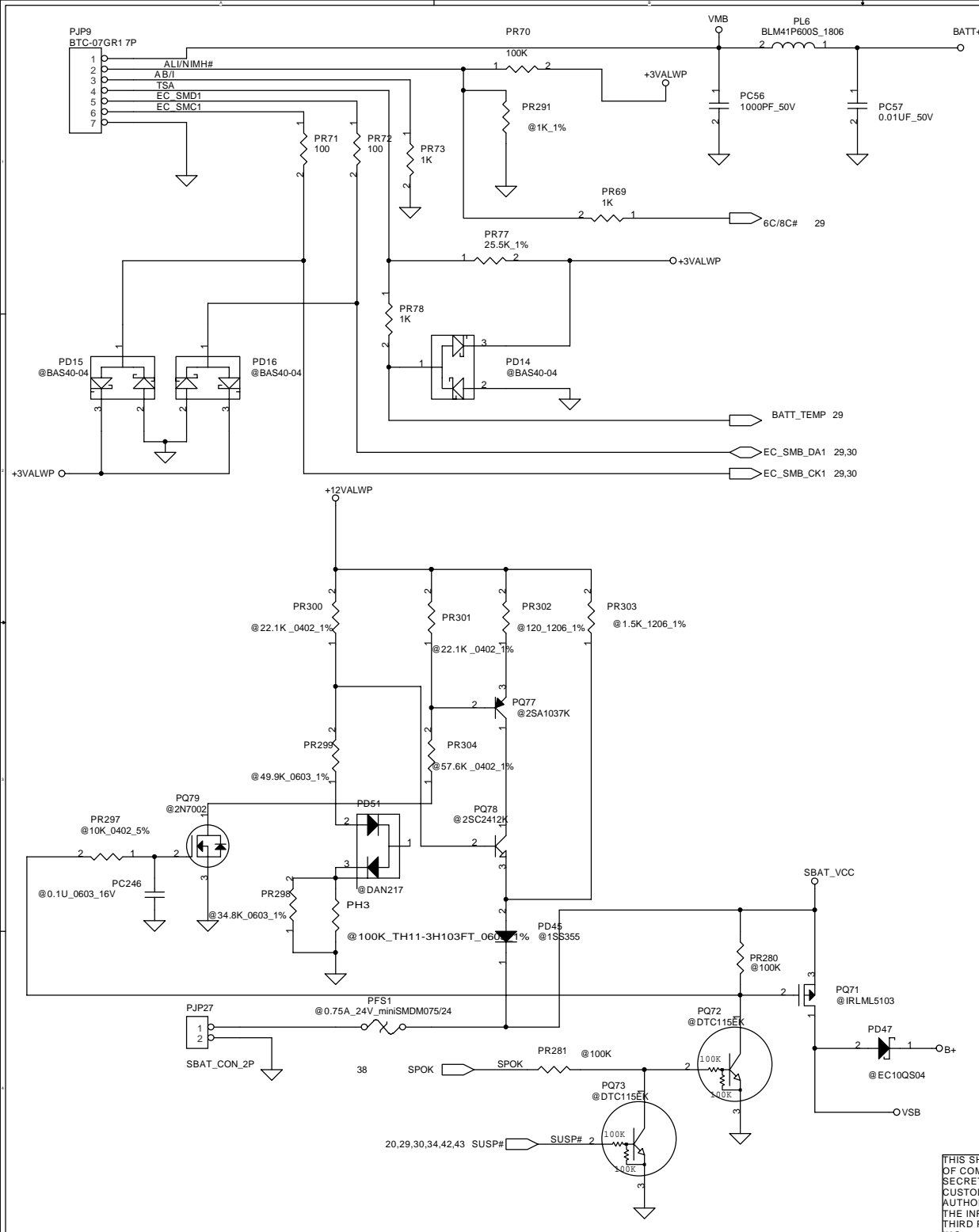


**+3.3V Ipeak = 6.66A ~ 10A**

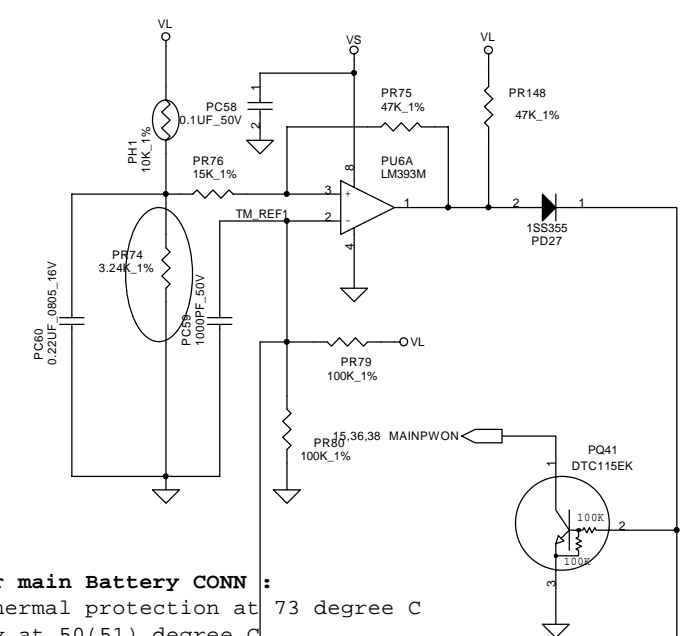
**+5V Ipeak = 6.66A ~ 10A**

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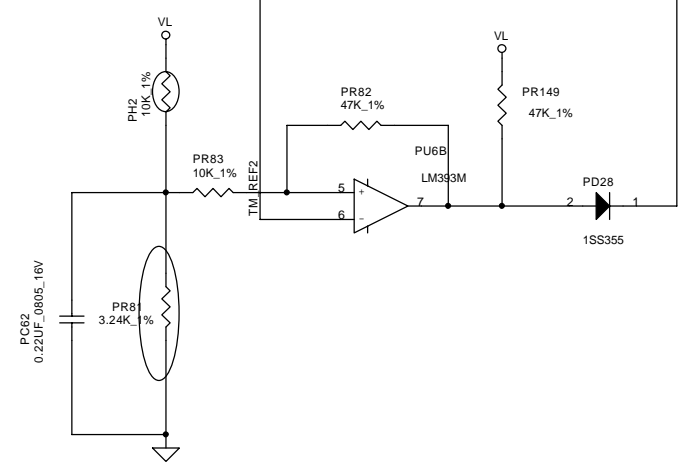
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**PH1 under CPU bottom side :**  
 CPU thermal protection at 82 degree C  
 Recovery at 48 degree C

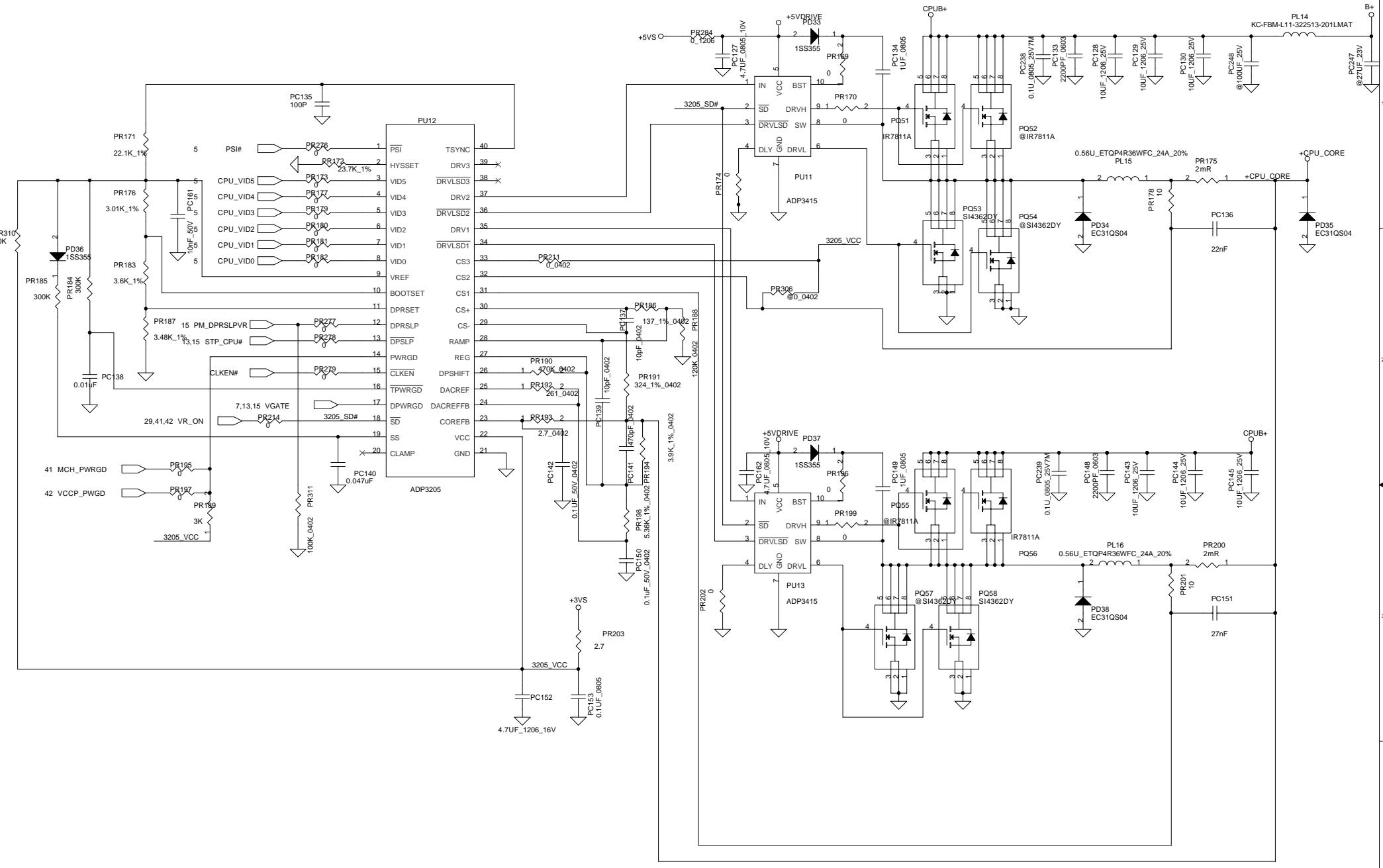


**PH2 near main Battery CONN :**  
 BAT. thermal protection at 73 degree C  
 Recovery at 50(51) degree C



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# CPU-CORE

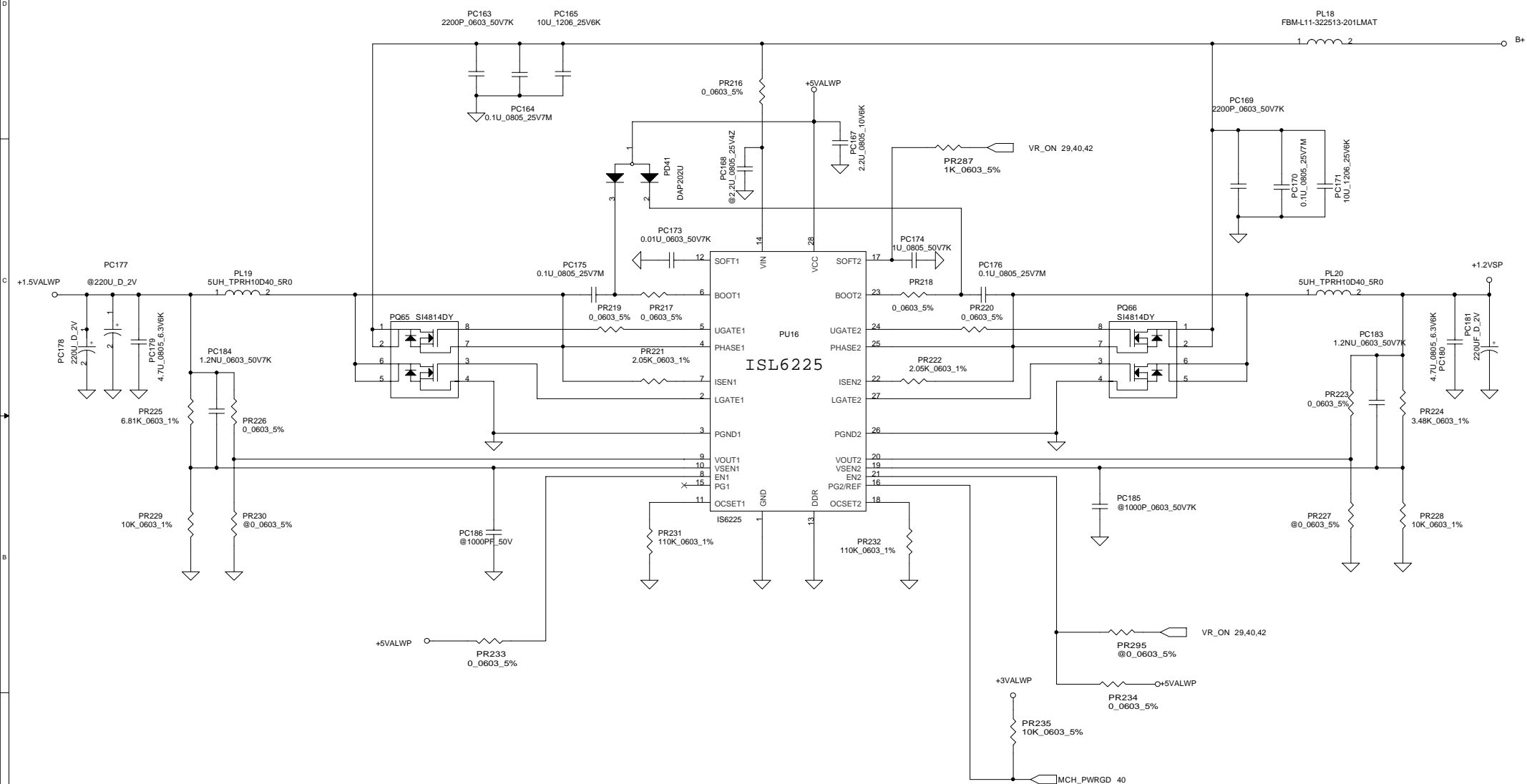


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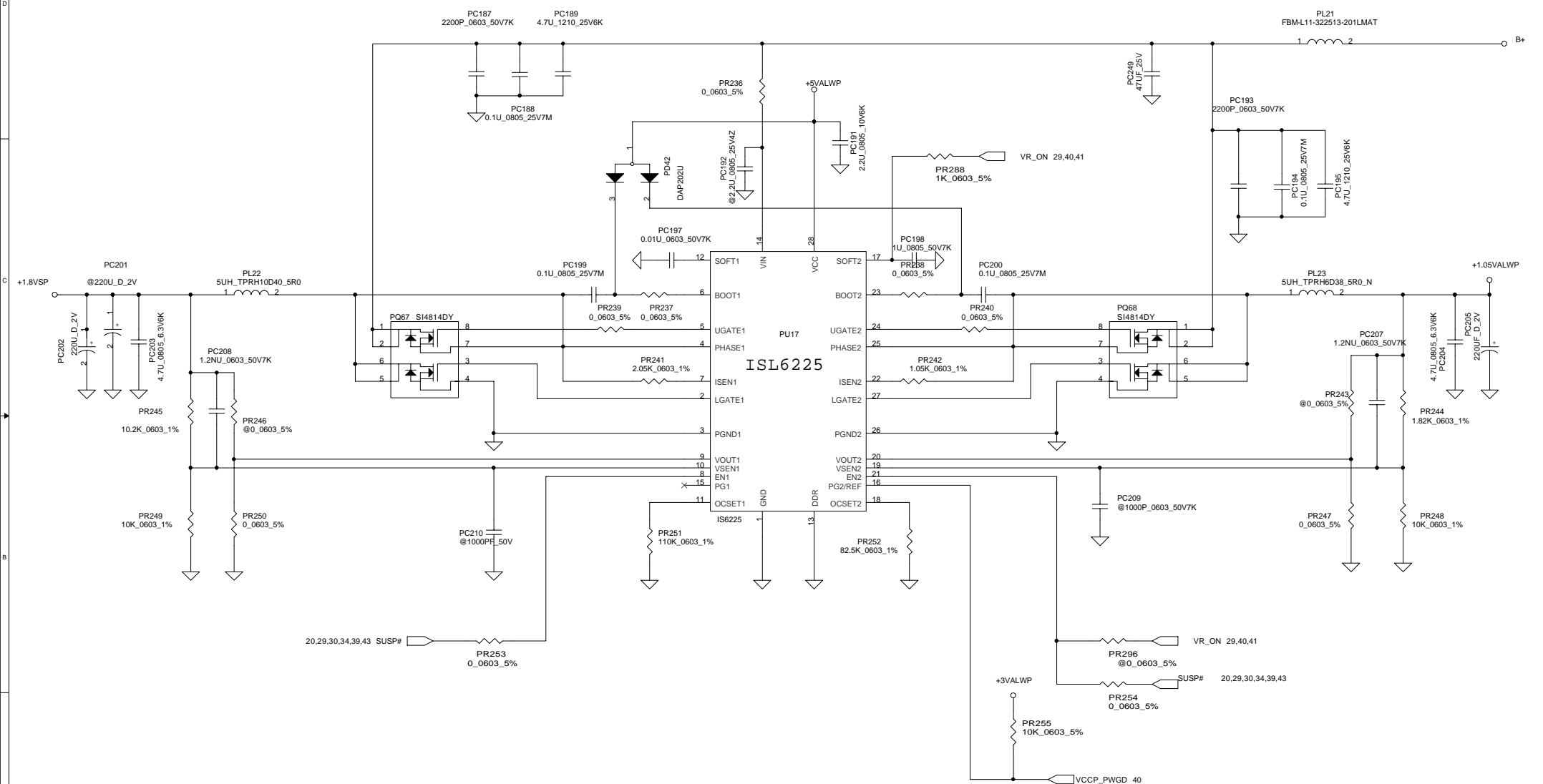
+1.5VALWPV/+1.2VSP



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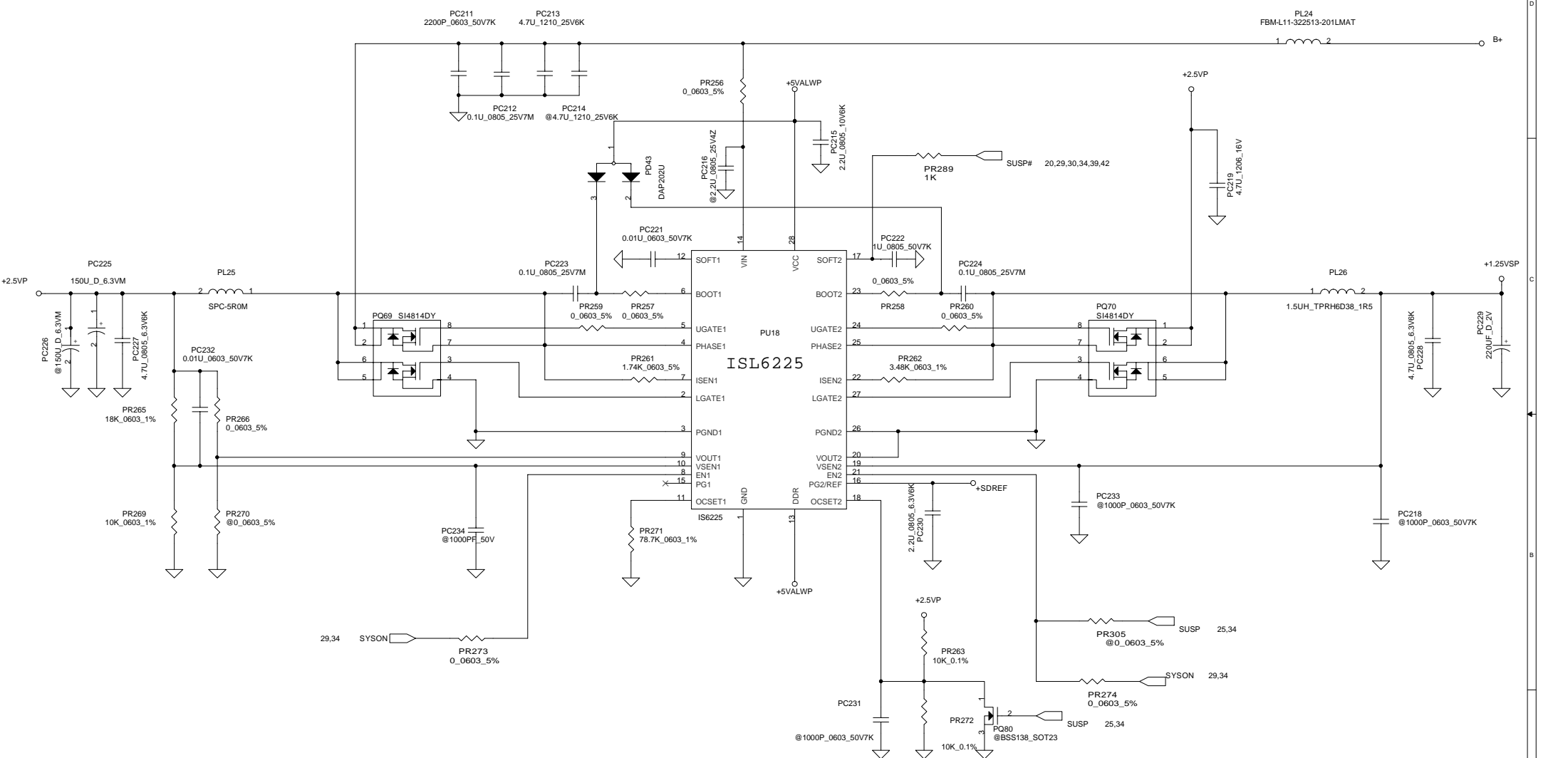
+1.8VALWP/+1.05VALWP



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+2.5VP/+1.25VSP



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1.	+5VMOD leaked when AC-IN	Change EXTIDEPWR# to +5VALW	0.2	P17	Delete EXTIDEPWR# Add +5VALW to R126		DVT
2.	For ESD	For ESD	0.2	P28	Add D26, D27 on TP_DATA, TP_CLK		DVT
3.	For EMI	For EMI	0.2	P31	Add C574 on FAN1_TACH		DVT
4.	Reserve For ENE KB3910	Reserve For ENE KB3910	0.2	P29	Add R441, R442, R443, R444, R445		DVT
5.	Reserve For CB1410 Rev.B0	Reserve For CB1410 Rev.B0	0.2	P20,21	Add C575, C576, R447, R448, R449		DVT
6.	Reserve FAN Control Circuit	Reserve FAN Control Circuit	0.2	P31	Add U44, R450, R451, R452, R453, C577		DVT
7.	Bluetooth LED	Add Bluetooth LED	0.3	P31	Add Q50, R454		PVT
8.	Change LED Wire Connector	Change LED Wire Connector	0.3	P26	Change JP24 Connector Type		PVT
9.	Reserve SCROLL LED Circuit	Add LED Control Circuit	0.3	P26	Add Q51, Q52, R455, R456		PVT
10.	For ESD	For ESD	0.3	P33	Add D28, D29, D30, D31 close to Speaker Connector		PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		delete 6 cell charger voltage		37	1.delete PQ75,PQ74,PR294,PC245		DVT
2		Adjust charger charge voltage:		37	1. change PU3 from MB3878 to MB3887, PR38 from 118K to 174k,PR33 from 26.1k to 34k, PR44 from 120k_1% to 9.3k_0.1%,PR45 from 243k_1% to 143k_1%, PR290 from 243k_1% to 143k_0.1%		
3		modify 1.5UH CHOKE footprint to be the same as all vender		42	Change PL26 fom old version:1.5UH TPRH6D38 to new version 1.5UH_TPRH6D38-N.		DVT
4		add pull low resistor PR311 to ground for hardware		39	add PR311		DVT
5		for cpu core current balance		40	change pc151 from 22n to 27n		PVT
6		for vender require , new DC JACKbe crease		36	increase PJP11		
7		for 1.2vs soft start rise time		41,42,43	change pc174,pc198,pc222, from 4.7u to 1u		
8		cost down		38,39,40,41	delete PC36,PC39,PC247,PC249 CHANGE PC195,PC189 FROM 10U 1206 TO 4.7U 1210		
9		TP0610C will be phase out		36	change TP0610C to TP0610K		

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