

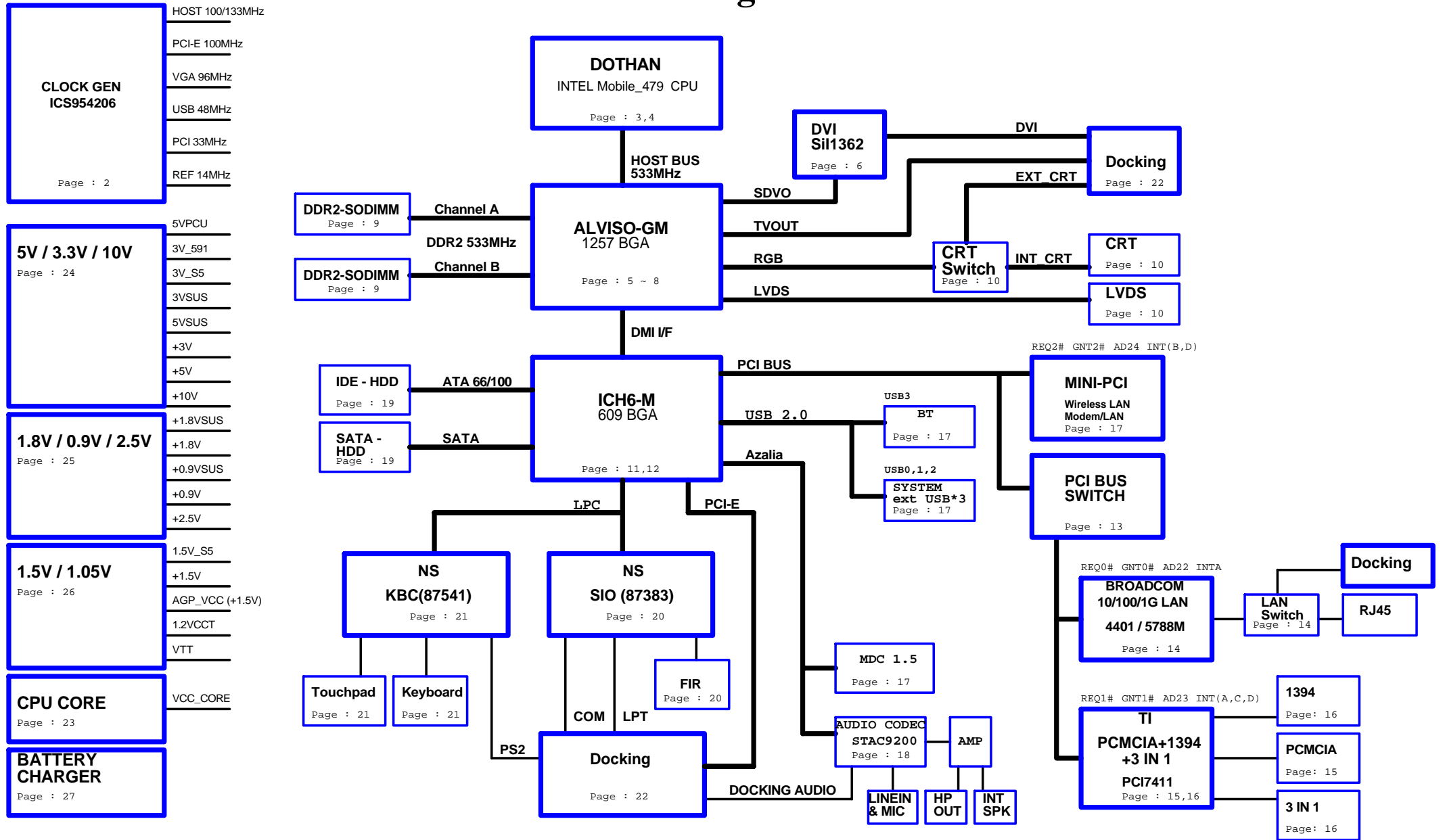
MODEL :	REV :	CHANGE LIST :	MODEL : ZH1 MB																																																																																	
ZH1 MotherBoard	1A	FIRST RELEASE																																																																																		
	2A	PAGE02. 1.MODIFY BSEL0 & BSEL1 2.ADD PCIE CLOCK FOR SATA PAGE03. 1.UN-STUFF R218 PAGE05. 1.MODIFY BSEL0 & BSEL1 2. REMOVE M_OCDCOMP RESISTOR ( Intel Errta ) PAGE06. 1.MODIFY SDVO I2C BUS PULL HIGH TO 5.6K PAGE08. 1.MODIFY CAPACITOR P/N DUE TO ME ISSUE PAGE09. 1.MODIFY SO-DIMM SA0 & SA1 PAGE10. 1.MODIFY Q9,Q10 TO 2N7002 2. MODIFY RGB BEAD VALUE 3. DELETE SYNC BEFORE BUFFER RESISTOR 4. DELETE LCD_ON PULL DOWN RESISTOR 5.MODIFY LVDS CONNECTOR PAGE11. 1.MODIFY ICH-6 PULL HIGH RESISTOR VALUE 2. MODIFY Azalia LAYOUT TOPOLOGY 3.ADD SATA CIRCUIT 4. LAN_RST# CONNECT TO PLTRST# PAGE12. 1.MODIFY LAN POWER TO +1.5V & +3V (S3-S4 OFF) PAGE14. 1.MODIFY LAN RDAC TO 1.18K FOR IEEE TEST PAGE15. 1.MODIFY IDSEL RESISTOR TO 150 OHM PAGE16. 1.MODIFY 1394 POWER CLASS TO 30W 2.MODIFY CRYSTAL CL VALUE 3.ADD MOS FOR 1394 POWER PAGE17. 1.MODIFY IDSEL RESISTOR TO 150 OHM 2. MODIFY Azalia LAYOUT TOPOLOGY 3. MODIFY USE COMMON CHOKE FOOTPRINT & P/N PAGE18. 1.MODIFY Azalia LAYOUT TOPOLOGY 2. DELETE R458 3. ADD DIODE FOR HPS PAGE19. 1.MODIFY LED7,LED8 FOOTPRINT 2.ADD SATA INTERFACE HDD 3.REMOVE R465 , 6648_OV# USE PULL HIGH +3V PAGE20. 1.MODIFY I_rDA C504 LOCATION PAGE21. 1.MODIFY KB MATRIX 2. ADD PME & MAX6648_AL# PAGE22. 1.MODIFY U18 FOOTPRINT PAGE23. 1.MODIFY PR116 FROM 787/F TO 1.54K/F FOR CPU LOAD LINE 2.MODIFY PQ41 FROM SUD50N03-09P TO AOD404 FOR CPU EFFICIENCY PAGE24. 1.REMOVE PQ2,PQ3,PR74 AND MOUNT PR57 FOR POWER SOURCE OF TURN ON MOSFET2.ADD PR136,PR137,PC132,PC133 FOR EMI REQUEST PAGE25. 1.MODIFY PR78 NETNAME S5 ON CHANGE TO NETNAME SUSON 2.MODIFY PR80,PC89 FOR EMI REQUEST 3.MODIFY +VCCP POWER UP SEQUENCE PAGE26. 1.ADD PR138,PR139,PC134,PC135 FOR EMI REQUEST 2.REMOVE JP2,JP3 PAGE27. 1.REMOVE PC98 FOR ME REQUEST 2.MODIFY PR26 FROM 22K/F TO 12K/F FOR CONSTANT CURRENT LIMIT	<table border="1"> <thead> <tr> <th>PAGE</th> <th>FROM</th> <th>TO</th> </tr> </thead> <tbody> <tr><td>1</td><td>1A</td><td></td></tr> <tr><td>2</td><td>2A</td><td></td></tr> <tr><td>3</td><td>2A</td><td></td></tr> <tr><td>4</td><td>1A</td><td></td></tr> <tr><td>5</td><td>2B</td><td></td></tr> <tr><td>6</td><td>2B</td><td>3A</td></tr> <tr><td>7</td><td>2B</td><td></td></tr> <tr><td>8</td><td>2B</td><td></td></tr> <tr><td>9</td><td>2A</td><td>3A</td></tr> <tr><td>10</td><td>2A</td><td>3A</td></tr> <tr><td>11</td><td>2B</td><td></td></tr> <tr><td>12</td><td>2B</td><td></td></tr> <tr><td>13</td><td>2A</td><td>3A</td></tr> <tr><td>14</td><td>2A</td><td>3A</td></tr> <tr><td>15</td><td>2A</td><td>3A</td></tr> <tr><td>16</td><td>2A</td><td>3A</td></tr> <tr><td>17</td><td>2A</td><td>3A</td></tr> <tr><td>18</td><td>2A</td><td>3A</td></tr> <tr><td>19</td><td>2A</td><td></td></tr> <tr><td>20</td><td>2A</td><td></td></tr> <tr><td>21</td><td>2A</td><td>3A</td></tr> <tr><td>22</td><td>2A</td><td>3A</td></tr> <tr><td>23</td><td>2A</td><td>3A</td></tr> <tr><td>24</td><td>2A</td><td>3A</td></tr> <tr><td>25</td><td>2A</td><td>3A</td></tr> <tr><td>26</td><td>2A</td><td>3A</td></tr> </tbody> </table>	PAGE	FROM	TO	1	1A		2	2A		3	2A		4	1A		5	2B		6	2B	3A	7	2B		8	2B		9	2A	3A	10	2A	3A	11	2B		12	2B		13	2A	3A	14	2A	3A	15	2A	3A	16	2A	3A	17	2A	3A	18	2A	3A	19	2A		20	2A		21	2A	3A	22	2A	3A	23	2A	3A	24	2A	3A	25	2A	3A	26	2A	3A
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3A	PAGE 06. ADD DVI SERIAL RESISTORS FOR EMI PAGE 09. MODIFY DDR2 CONNECTOR P/N PAGE 10. MODIFY RGB BEAD FROM 22 TO 30 PAGE 13. MODIFY CRYSTAL SERIAL RESISTOR R354 TO 200 OHM PAGE 14. MODIFY PCI BUS PAGE 15. MODIFY 1394 POWER SWITCH GATE ENABLE SIGNAL PAGE 16. MODIFY USB POWER SWITCH PAGE 17. MODIFY AUDIO POWER & AMP INPUT CIRCUIT PAGE 18. MODIFY FAN & SW ECARD CONNECTOR P/N PAGE 21. MODIFY RGB FOR EMI SOLUTION PAGE 22. MODIFY CAPACITOR FOR NOISE PAGE 23. STUFF SNUBBER CIRCUIT PAGE 24. UN-STUFF PC23 & STUFF SNUBBER CIRCUIT PAGE 25. STUFF SNUBBER CIRCUIT PAGE 26. STUFF SNUBBER CIRCUIT																																																																																			



PROJECT : ZH1	APPROVE BY: JIM HSU	DRAWING BY:JACKY CHENG	REV 3A
MB ASSY'S P/N : 31ZH1MB0001	PROJECT LEADER: JIM HSU	DOCUMENT NO: 204	DATE :2004/12/16

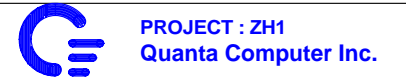
COVER SHEET 1 OF 1

# ZH1 Block Diagram

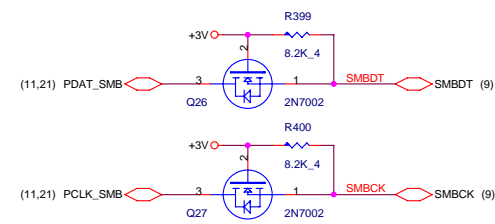
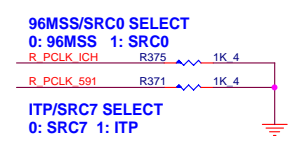
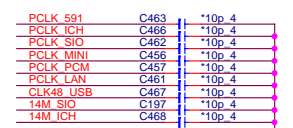
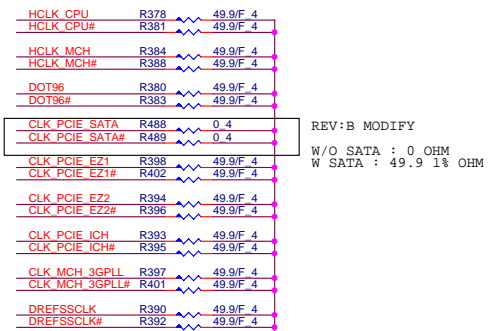
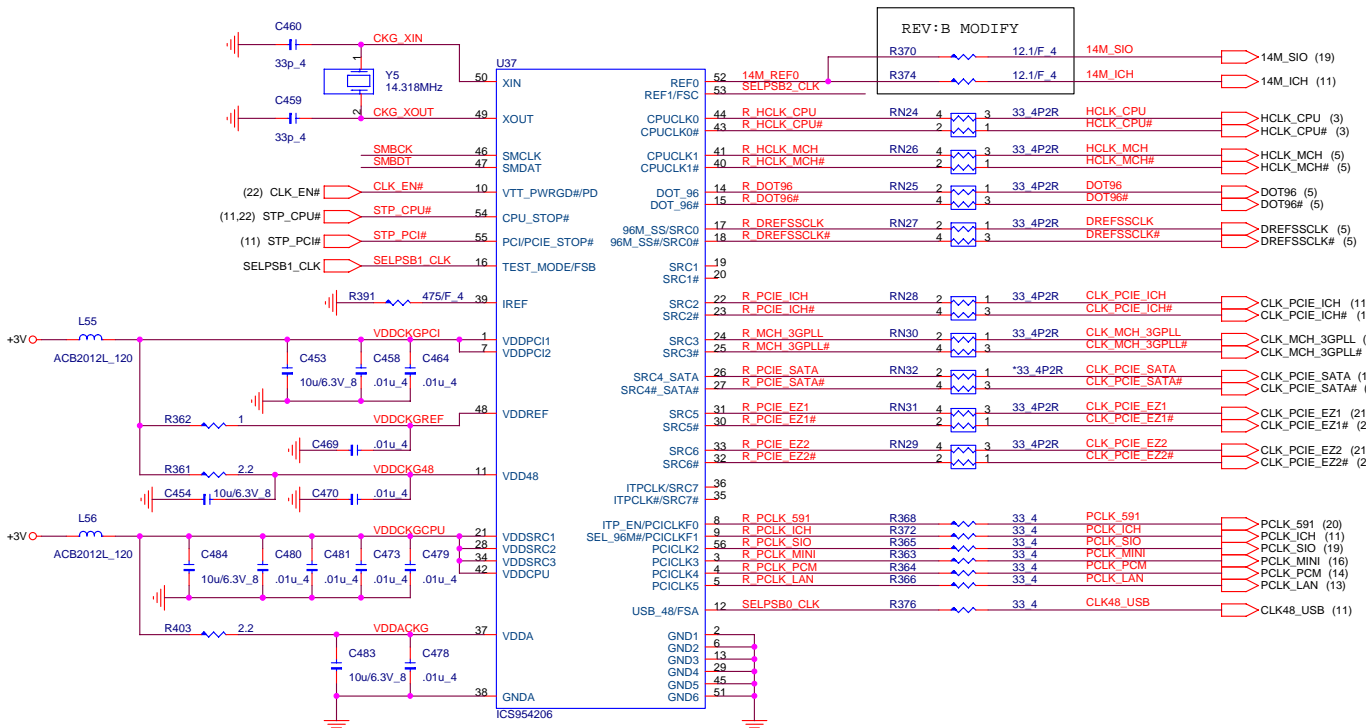


- CLOCK GEN ICS954206  
Page : 2
- HOST 100/133MHz
- PCI-E 100MHz
- VGA 96MHz
- USB 48MHz
- PCI 33MHz
- REF 14MHz
- 5VPCU
- 5V / 3.3V / 10V  
Page : 24
- 3V\_591
- 3V\_S5
- 3VSUS
- 5VSUS
- +3V
- +5V
- +10V
- 1.8V / 0.9V / 2.5V  
Page : 25
- +1.8VSUS
- +1.8V
- +0.9VSUS
- +0.9V
- +2.5V
- 1.5V / 1.05V  
Page : 26
- 1.5V\_S5
- +1.5V
- AGP\_VCC (+1.5V)
- 1.2VCCT
- VTT
- CPU CORE  
Page : 23
- VCC\_CORE
- BATTERY CHARGER  
Page : 27

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD22	INTA#	BROADCOM LAN
REQ2# / GNT2#	AD24	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD23	INTC# , INTD# , INTA#	TI 7411



Size	Document Number	Rev
	<b>BLOCK DIAGRAM</b>	1A
Date: Tuesday, January 11, 2005	Sheet	1 of 27



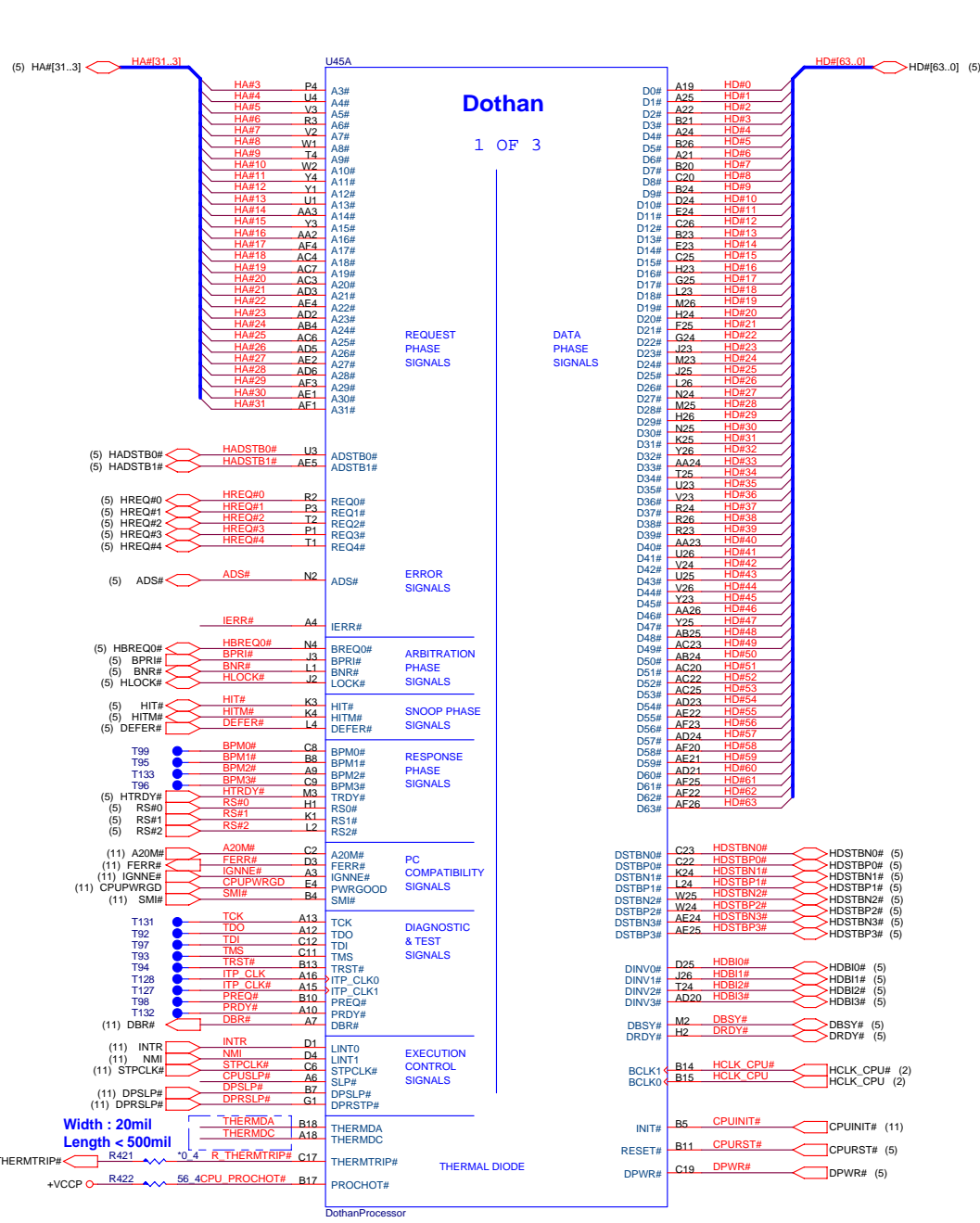
**FSA**

**FSB**

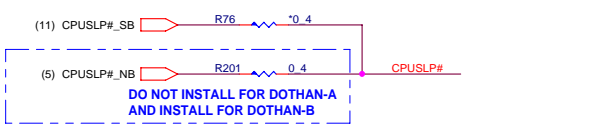
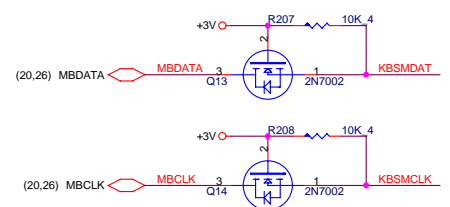
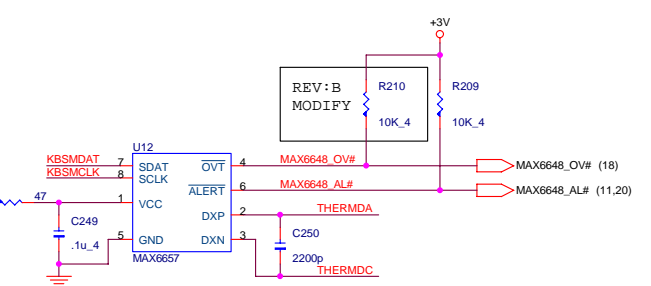
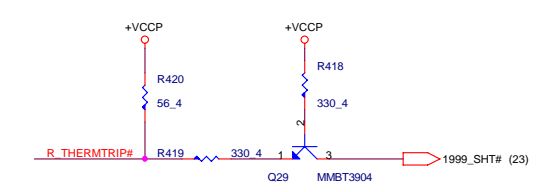
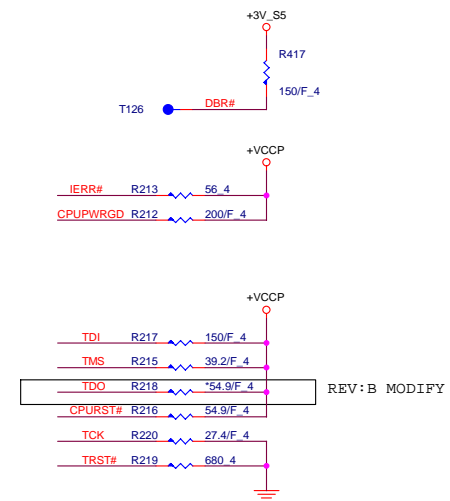
**FSC**

**FSB SETTING**

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

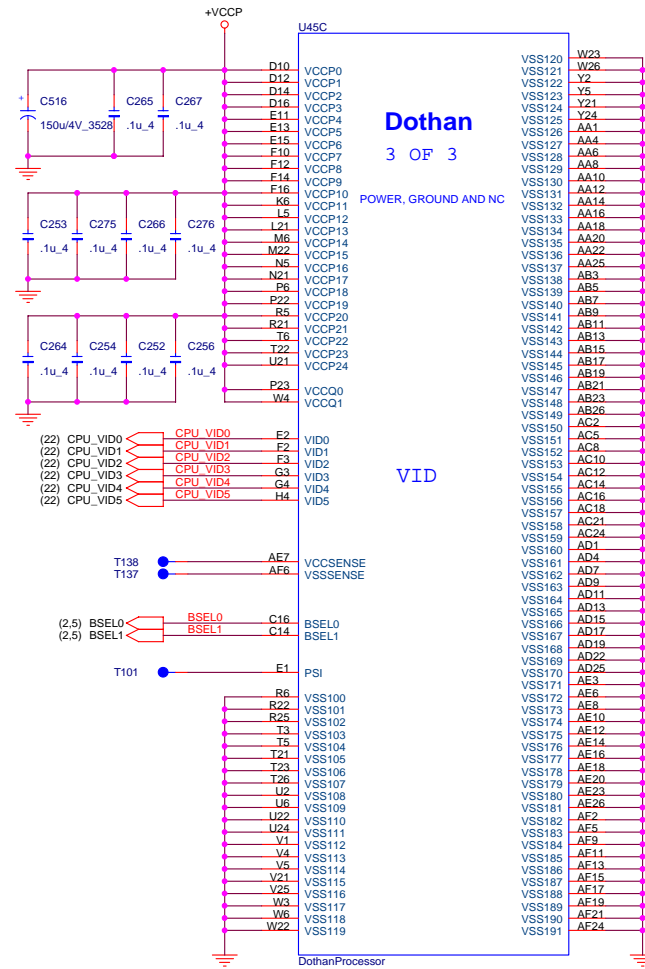
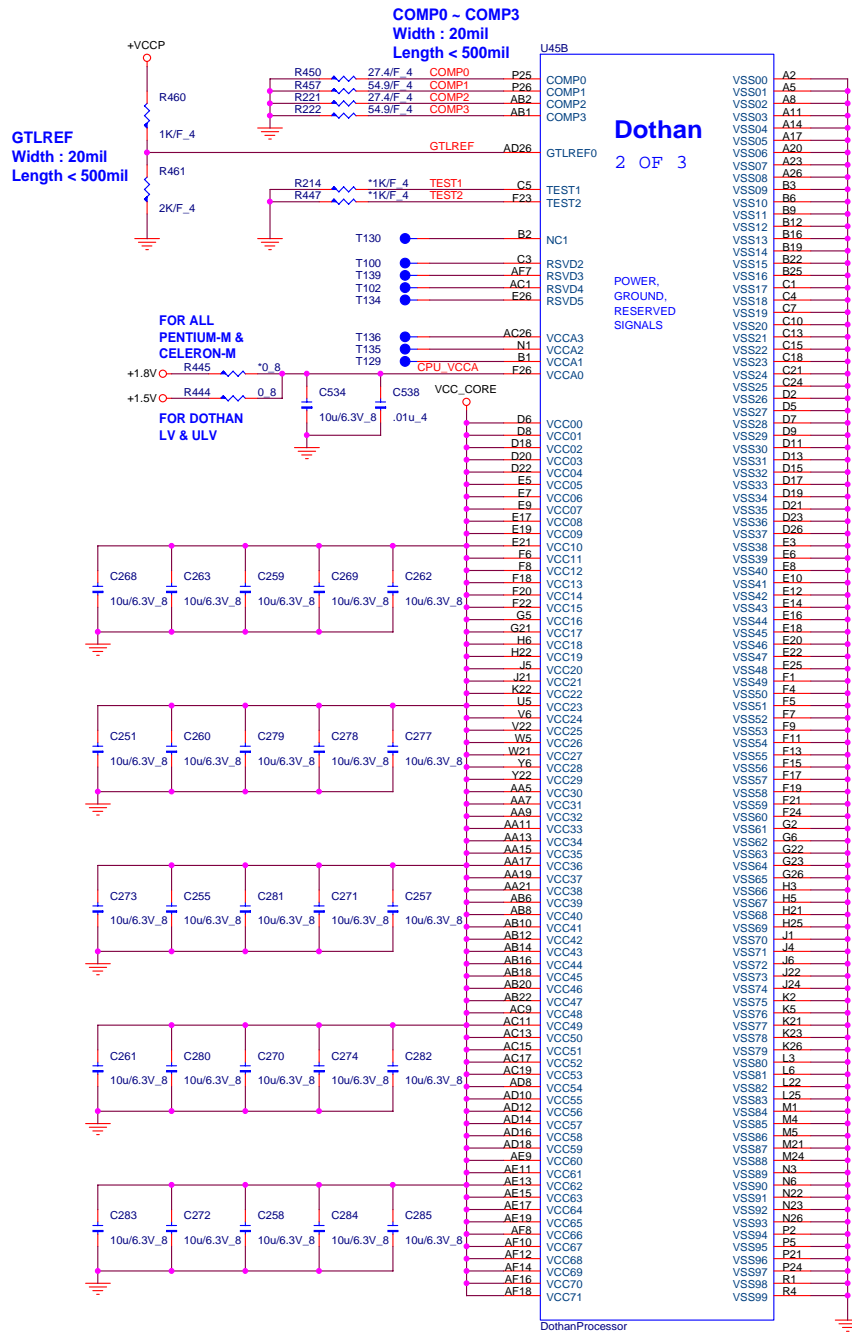


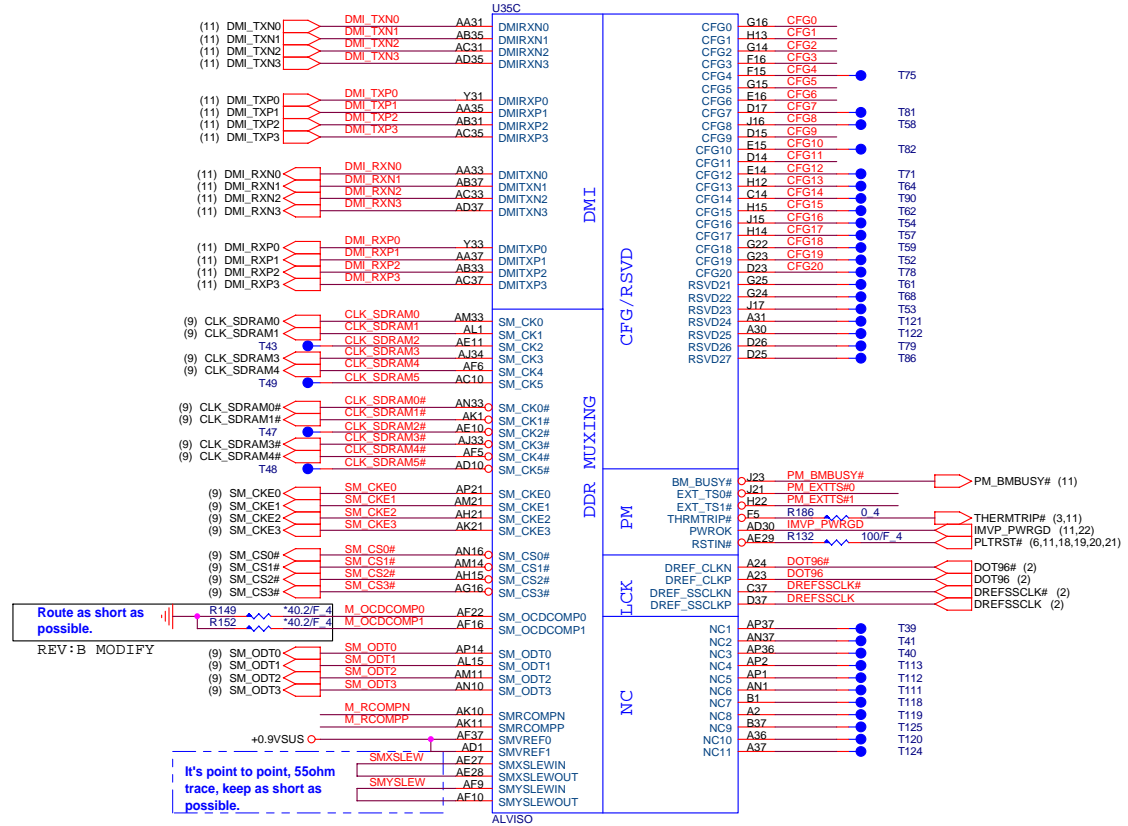
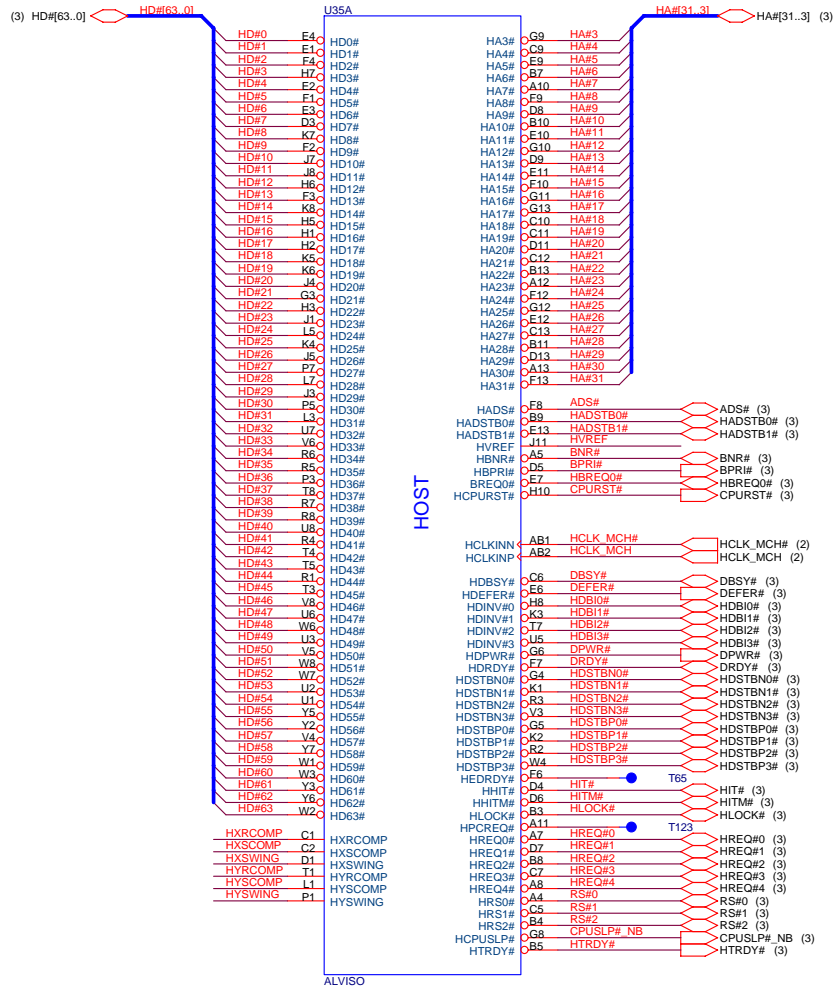
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1 OF 3



DO NOT INSTALL FOR DOTHAN-A AND INSTALL FOR DOTHAN-B

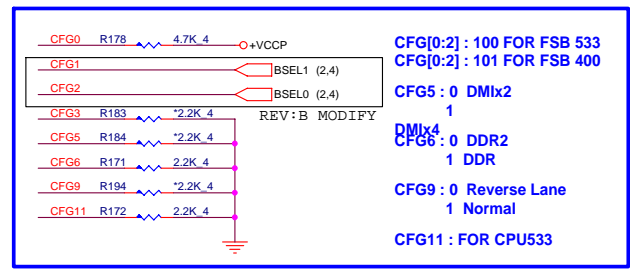
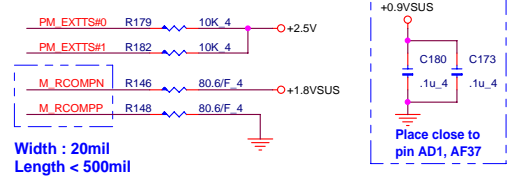
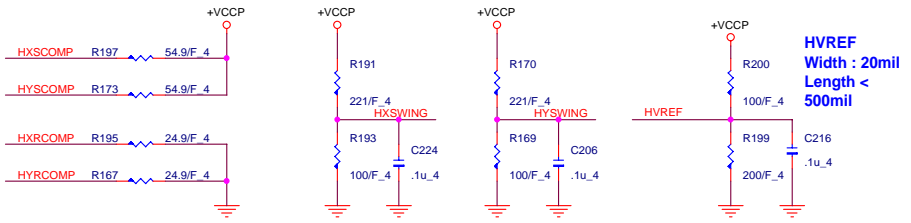
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Quanta Computer Inc.





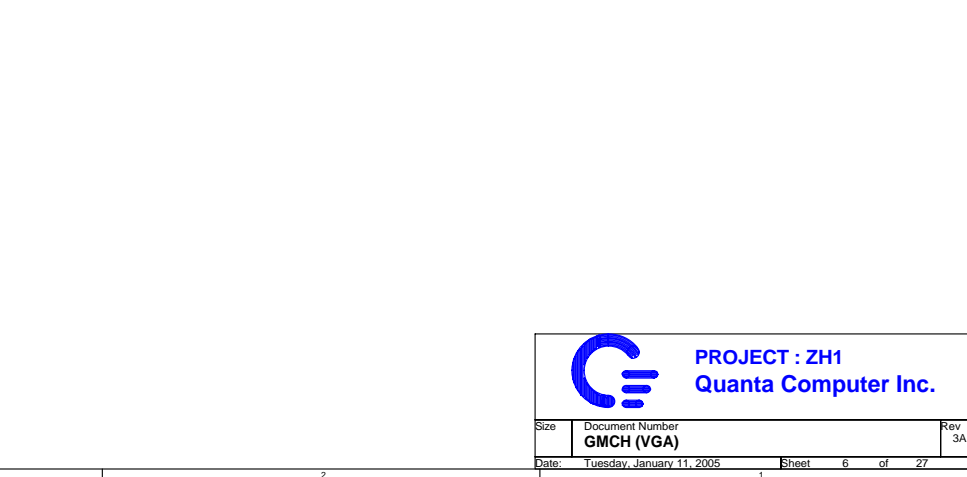
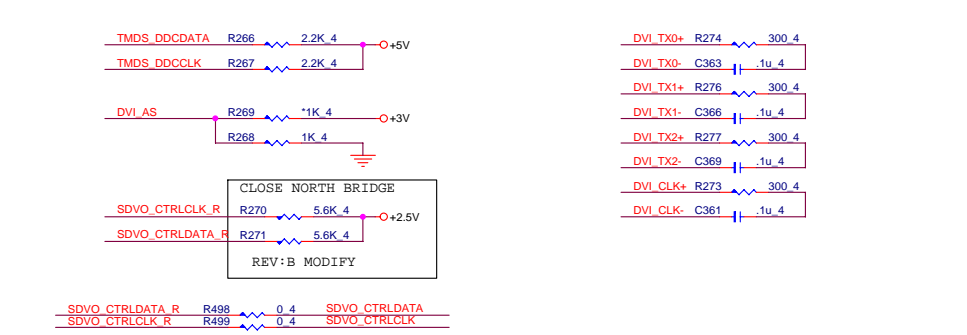
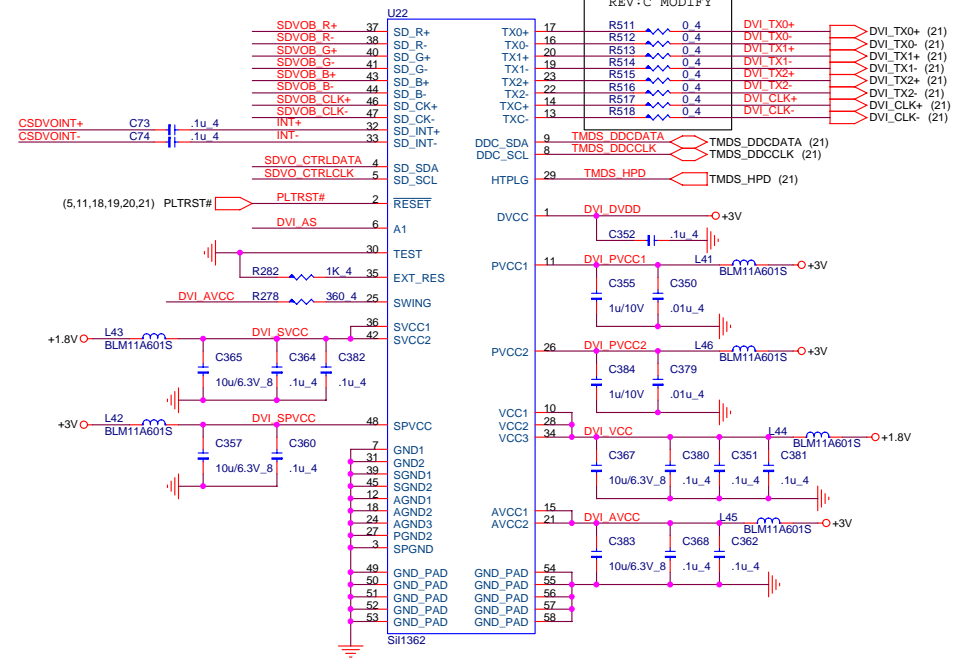
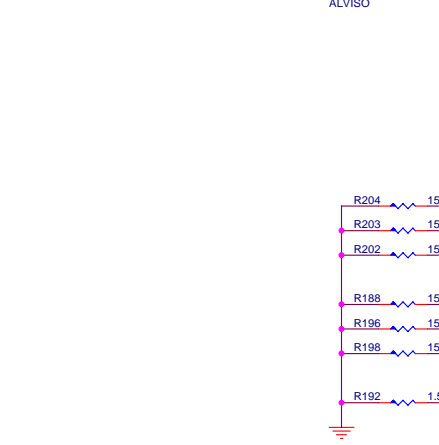
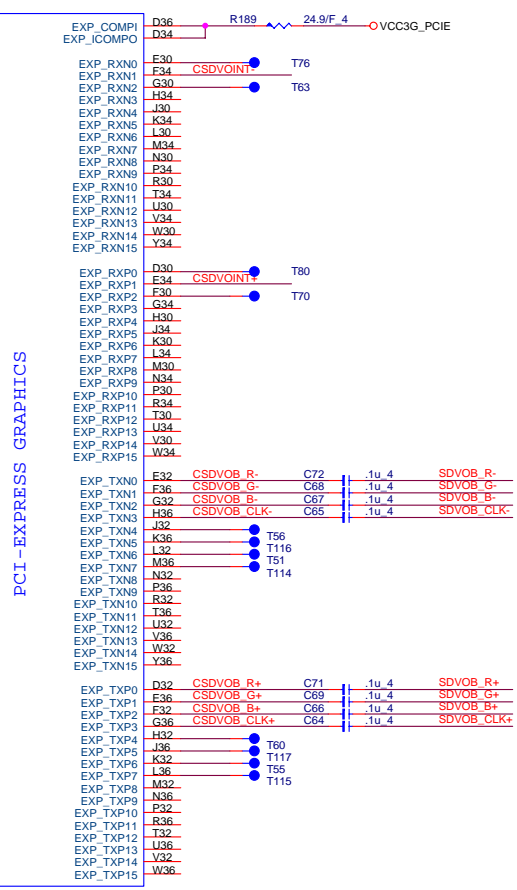
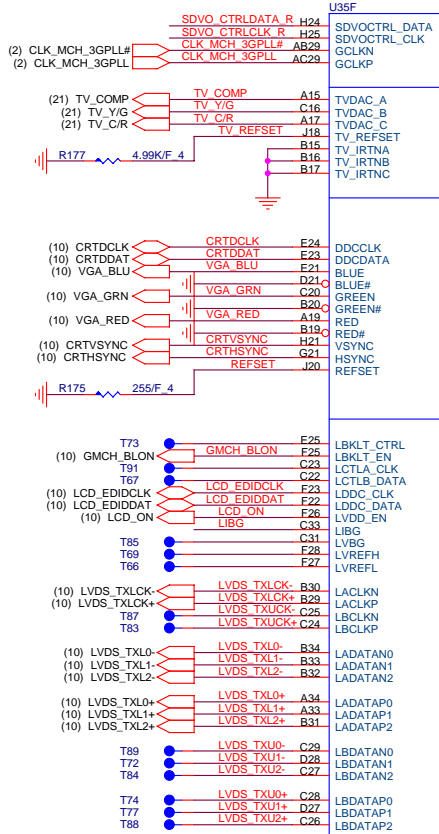
Route as short as possible.  
REV: B MODIFY

It's nice to point, 550ohm trace, keep as short as possible.



CFG0: 100 FOR FSB 533  
CFG0: 2: 101 FOR FSB 400  
CFG5: 0 DMIX2  
CFG6: 0 DDR2  
CFG9: 0 Reverse Lane  
CFG11: FOR CPU533



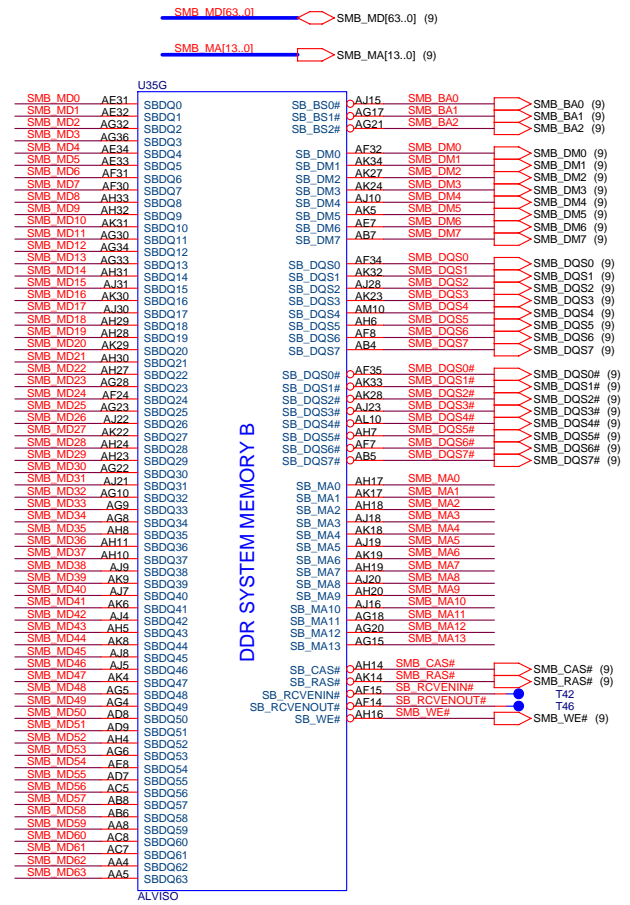
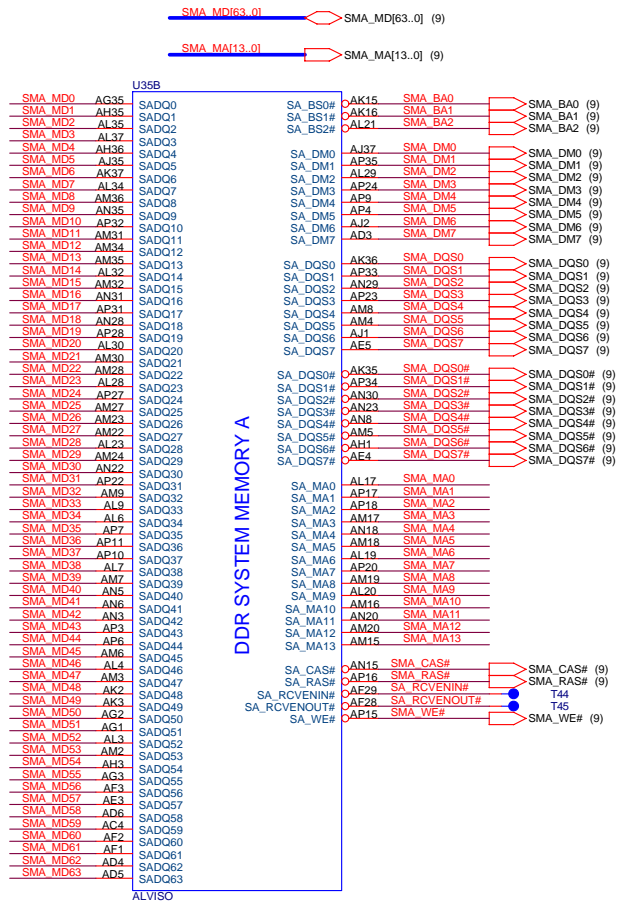


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**Quanta Computer Inc.**

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**GMCH (VGA)**

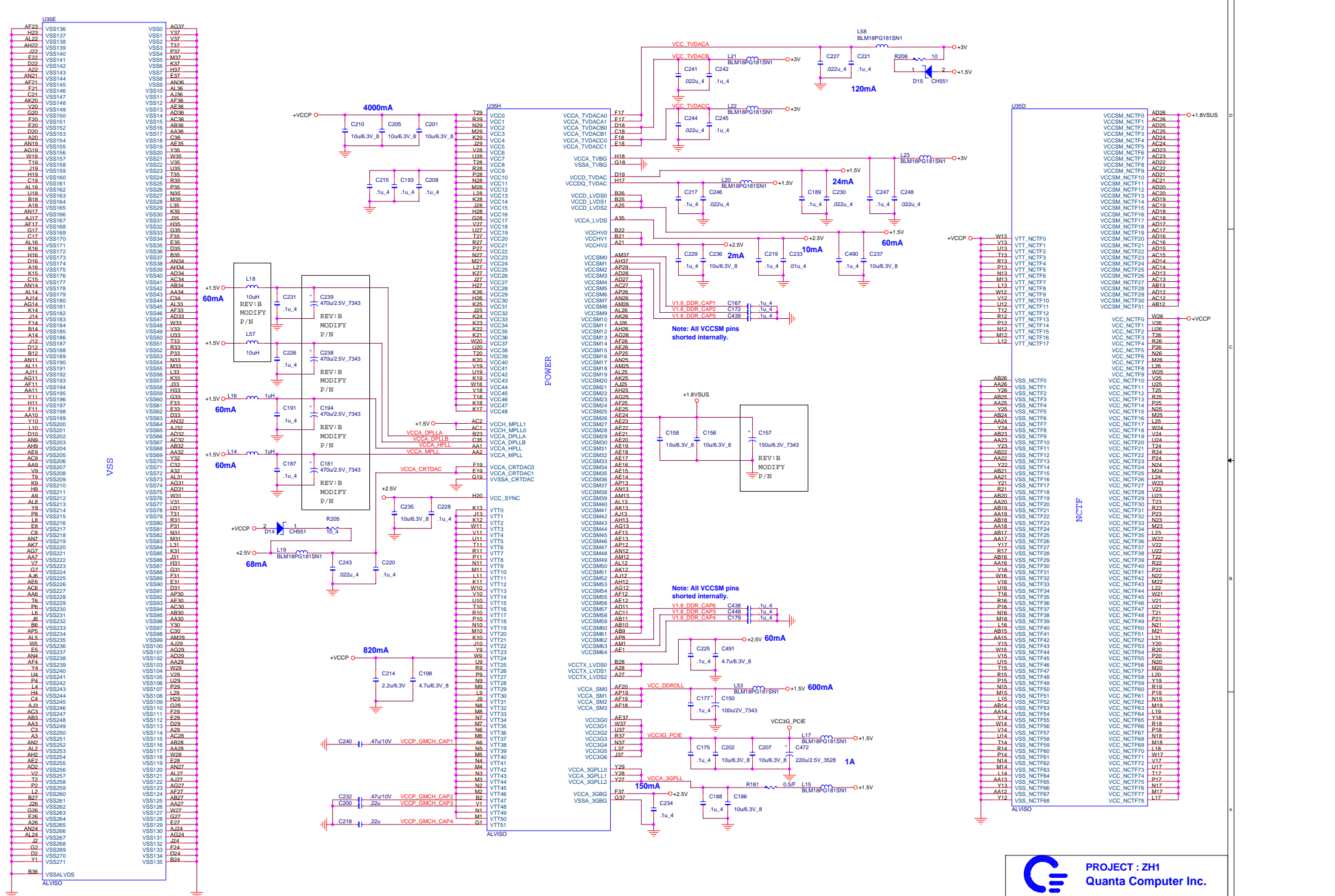
Date: Tuesday, January 11, 2005 Sheet 6 of 27

Rev 3A

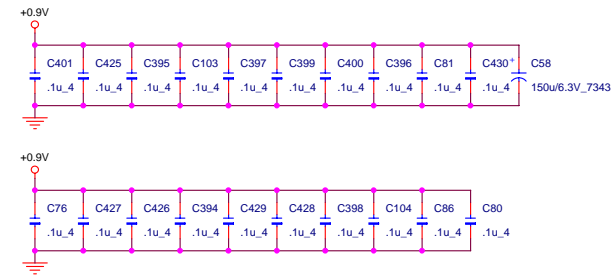


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 Quanta Computer Inc.

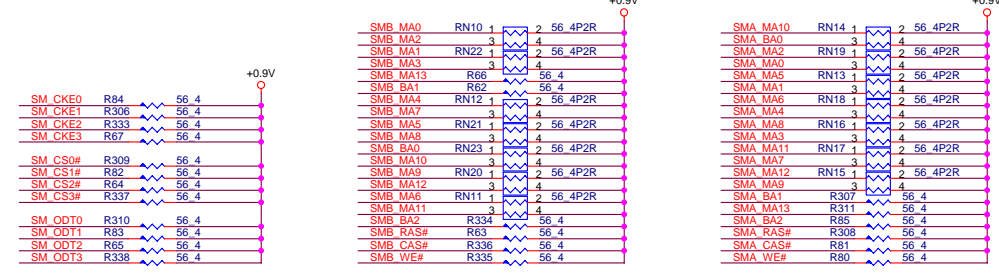




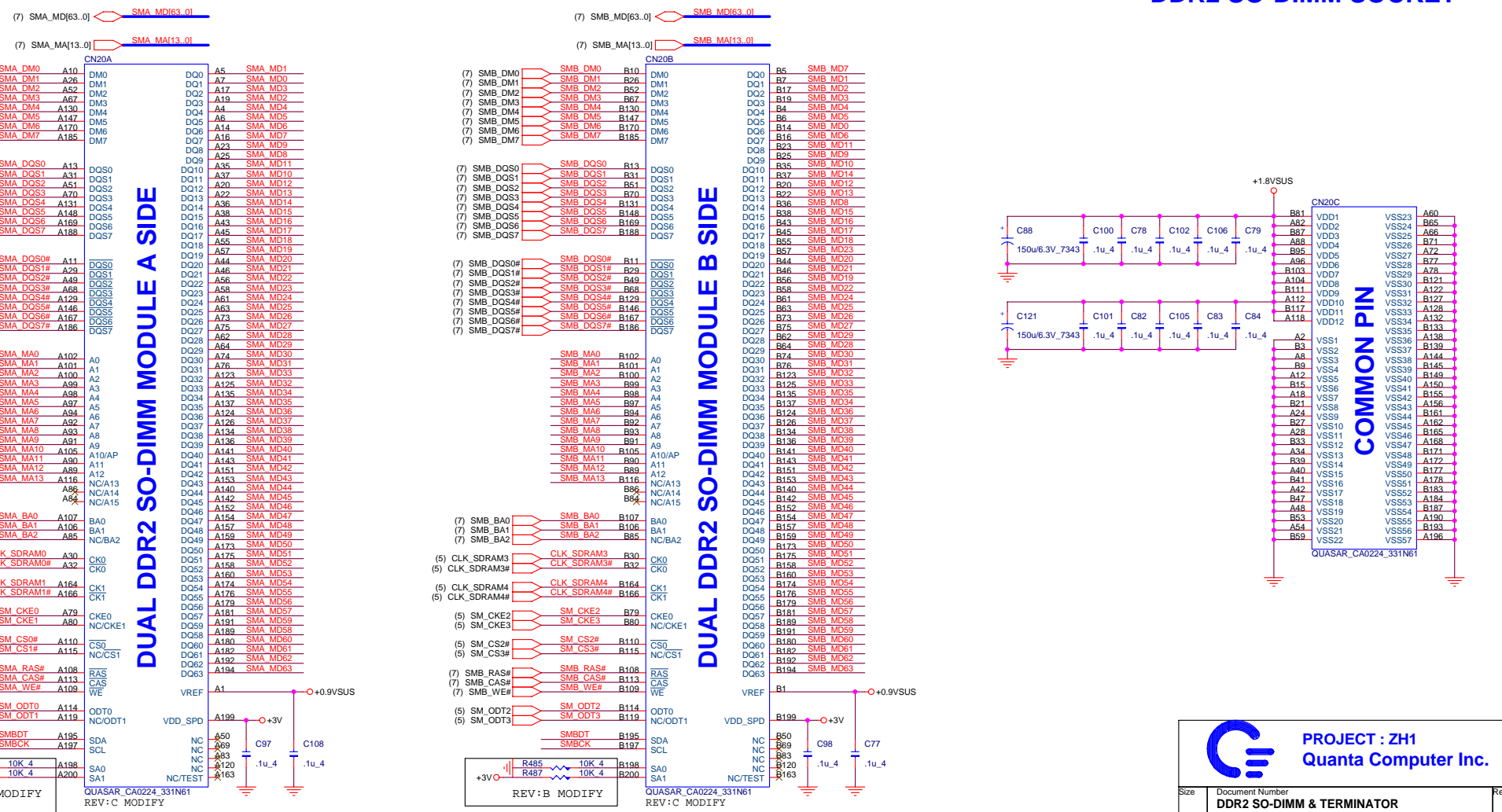
# TERMINATOR DECOUPLING CAPACITOR



# DDR2 TERMINATOR



# DDR2 SO-DIMM SOCKET



**PROJECT : ZH1**  
**Quanta Computer Inc.**

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Sheet: 9 of 27

Date: Tuesday, January 11, 2005

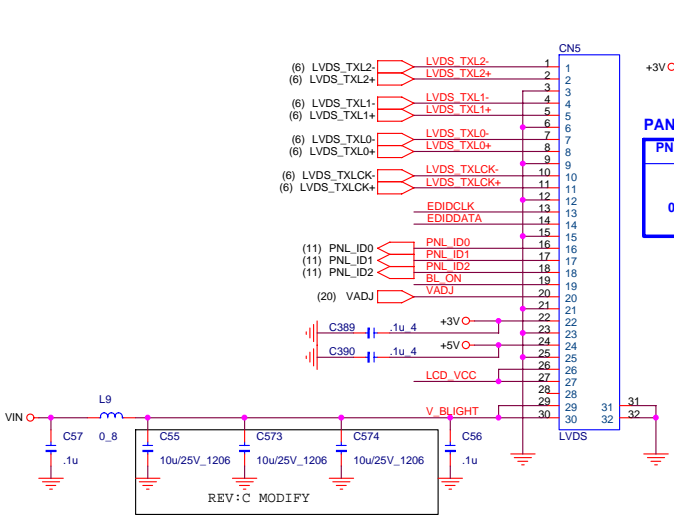
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REV: B MODIFY

REV: C MODIFY

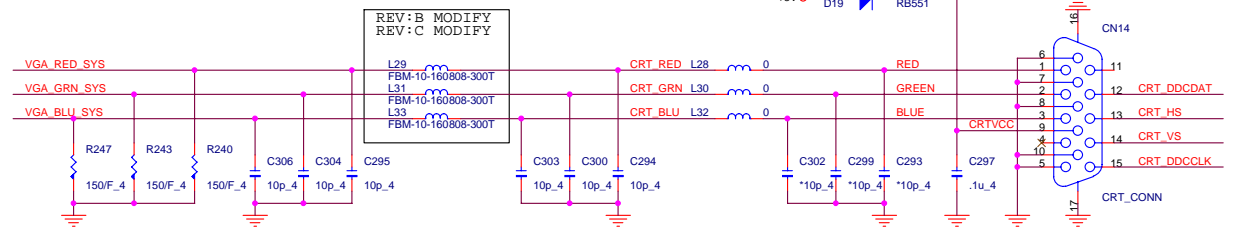
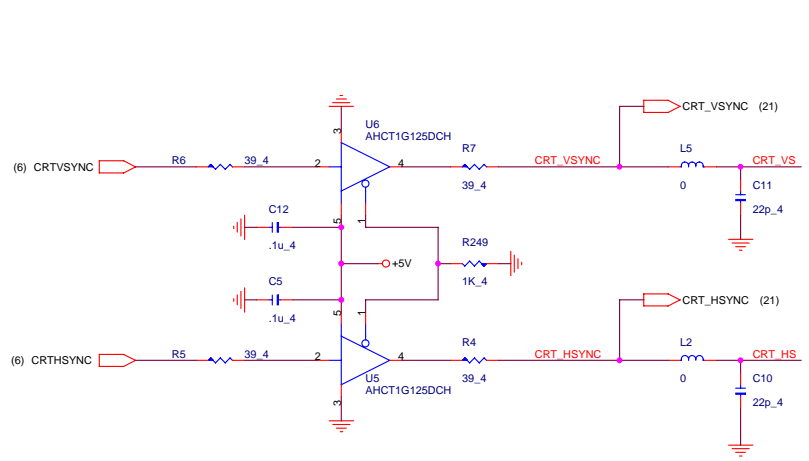
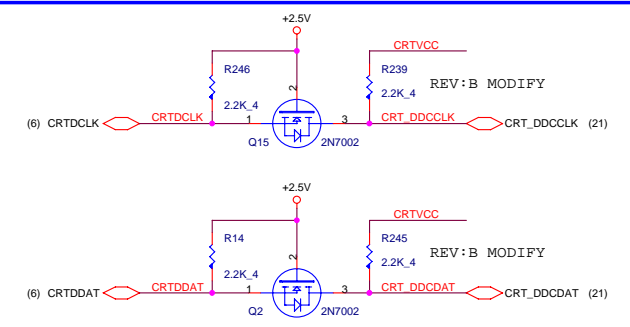
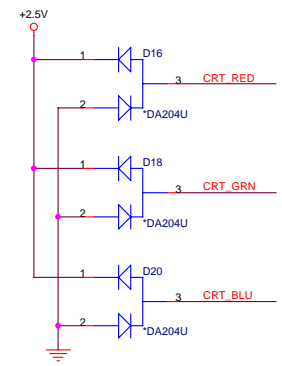
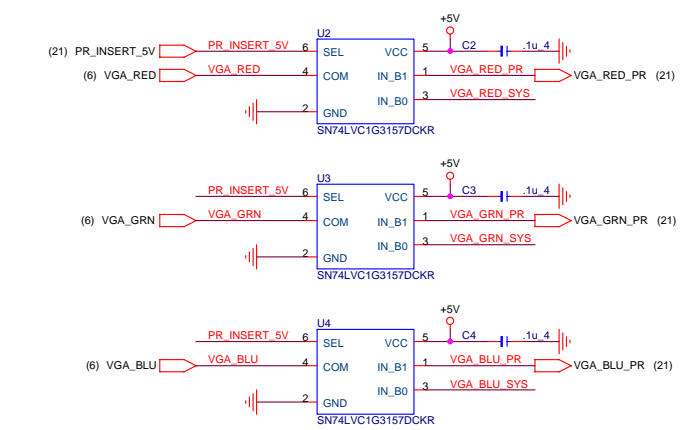
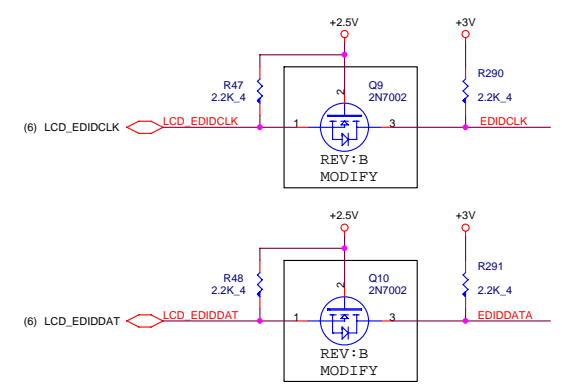
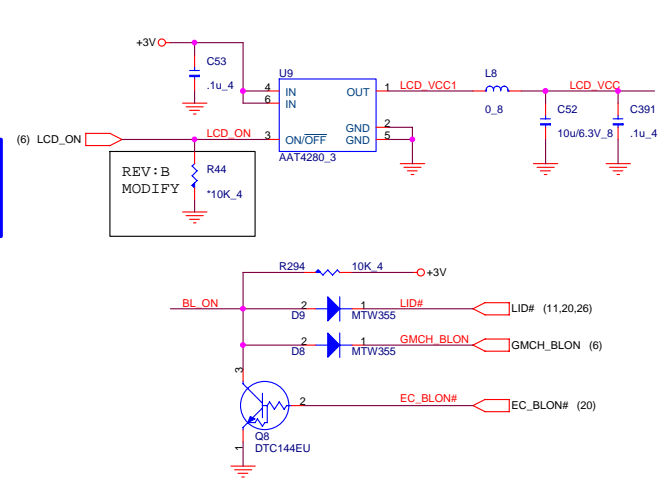
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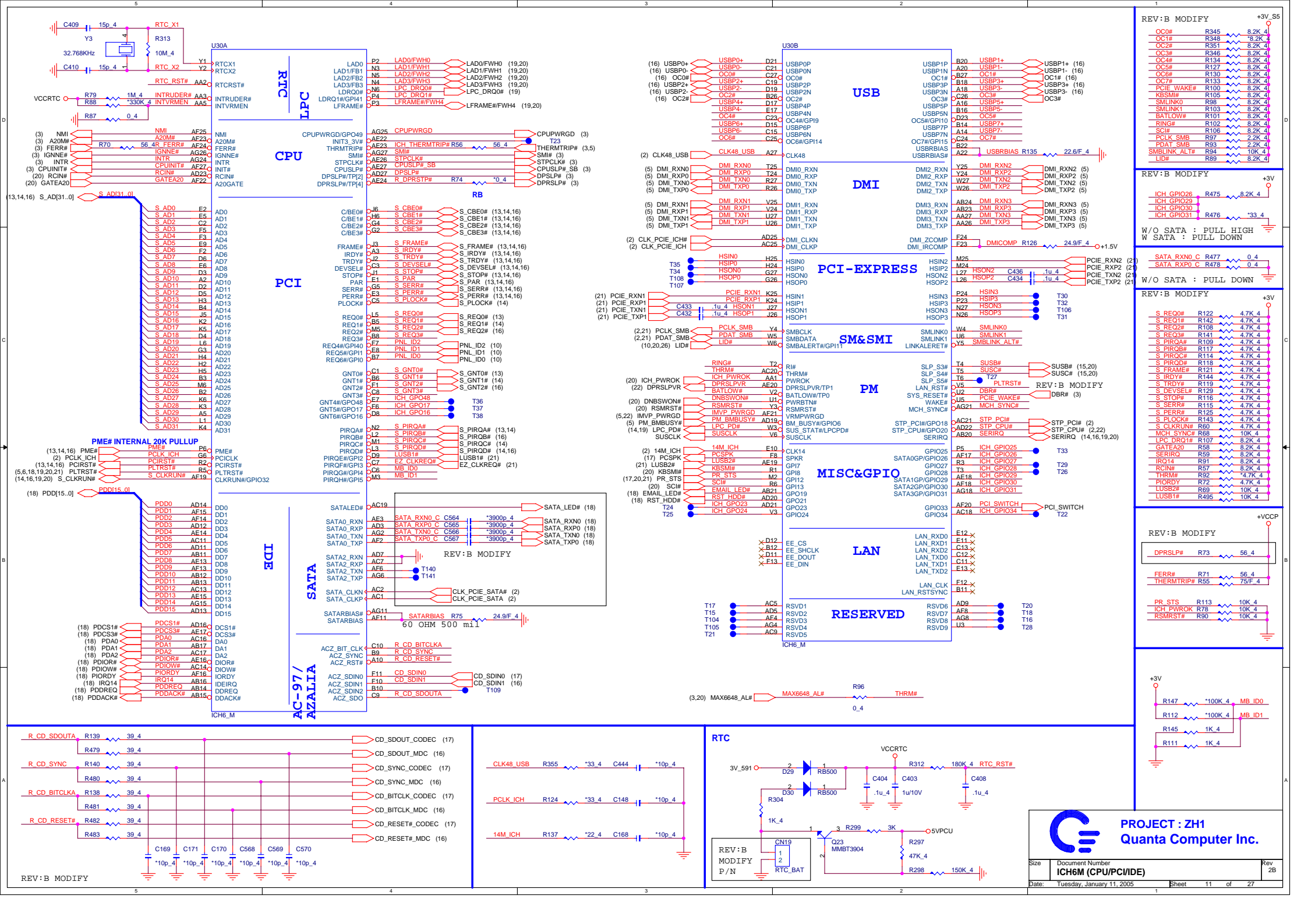
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 REV: C MODIFY



**PANEL ID SETTING**

PNL_ID[2:0]	PANEL TYPE
000	AU B121EW01
001	CMO N121H-L02
010	TOSHIBA LTD121EX1S
011 - 110	RESERVED
111	NO PANEL





REV:B MODIFY

OC0#	R345	8.2K 4
OC1#	R348	8.2K 4
OC2#	R351	8.2K 4
OC3#	R346	8.2K 4
OC4#	R134	8.2K 4
OC5#	R127	8.2K 4
OC6#	R130	8.2K 4
OC7#	R133	8.2K 4
OC8#	R136	8.2K 4
PCIE_WAKE#	R100	8.2K 4
KBSM#	R105	8.2K 4
SMLINK0	R98	8.2K 4
SMLINK1	R103	8.2K 4
BATLOW#	R101	8.2K 4
RING#	R102	8.2K 4
SCH#	R106	8.2K 4
PCLK SMB	R97	2.2K 4
PDAT SMB	R93	2.2K 4
SMLINK_ALTV#	R94	10K 4
LID#	R89	8.2K 4

REV:B MODIFY

ICH_GPIO26	R475	8.2K 4
ICH_GPIO29		
ICH_GPIO30		
ICH_GPIO31	R476	33 4

W/O SATA : PULL HIGH  
W SATA : PULL DOWN

SATA\_RXN0\_C R477 0.4  
SATA\_RXP0\_C R478 0.4

W/O SATA : PULL DOWN

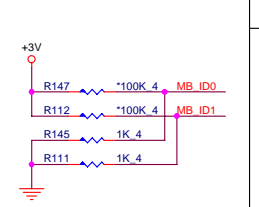
REV:B MODIFY

S_REQ0#	R122	4.7K 4
S_REQ1#	R142	4.7K 4
S_REQ2#	R108	4.7K 4
S_REQ3#	R141	4.7K 4
S_REQ4#	R109	4.7K 4
S_PIRQ0#	R117	4.7K 4
S_PIRQ1#	R114	4.7K 4
S_PIRQ2#	R118	4.7K 4
S_FRAME#	R121	4.7K 4
S_TRDY#	R144	4.7K 4
S_IRDY#	R149	4.7K 4
S_DEVSEL#	R129	4.7K 4
S_STOP#	R116	4.7K 4
S_SERR#	R115	4.7K 4
S_PERR#	R125	4.7K 4
S_PLOCK#	R143	4.7K 4
S_CLKRUN#	R60	4.7K 4
ICH_SYNC#	R68	10K 4
LPC_DRO1#	R107	8.2K 4
GATEA20	R58	8.2K 4
SERIRQ	R59	8.2K 4
IR014	R91	8.2K 4
RCIN#	R57	8.2K 4
THRMA#	R92	4.7K 4
PIORDY	R72	4.7K 4
LUSB2#	R69	10K 4
LUSB1#	R495	10K 4

REV:B MODIFY

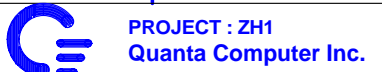
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FERR#	R71	56 4
THERMTRIP#	R55	75F 4

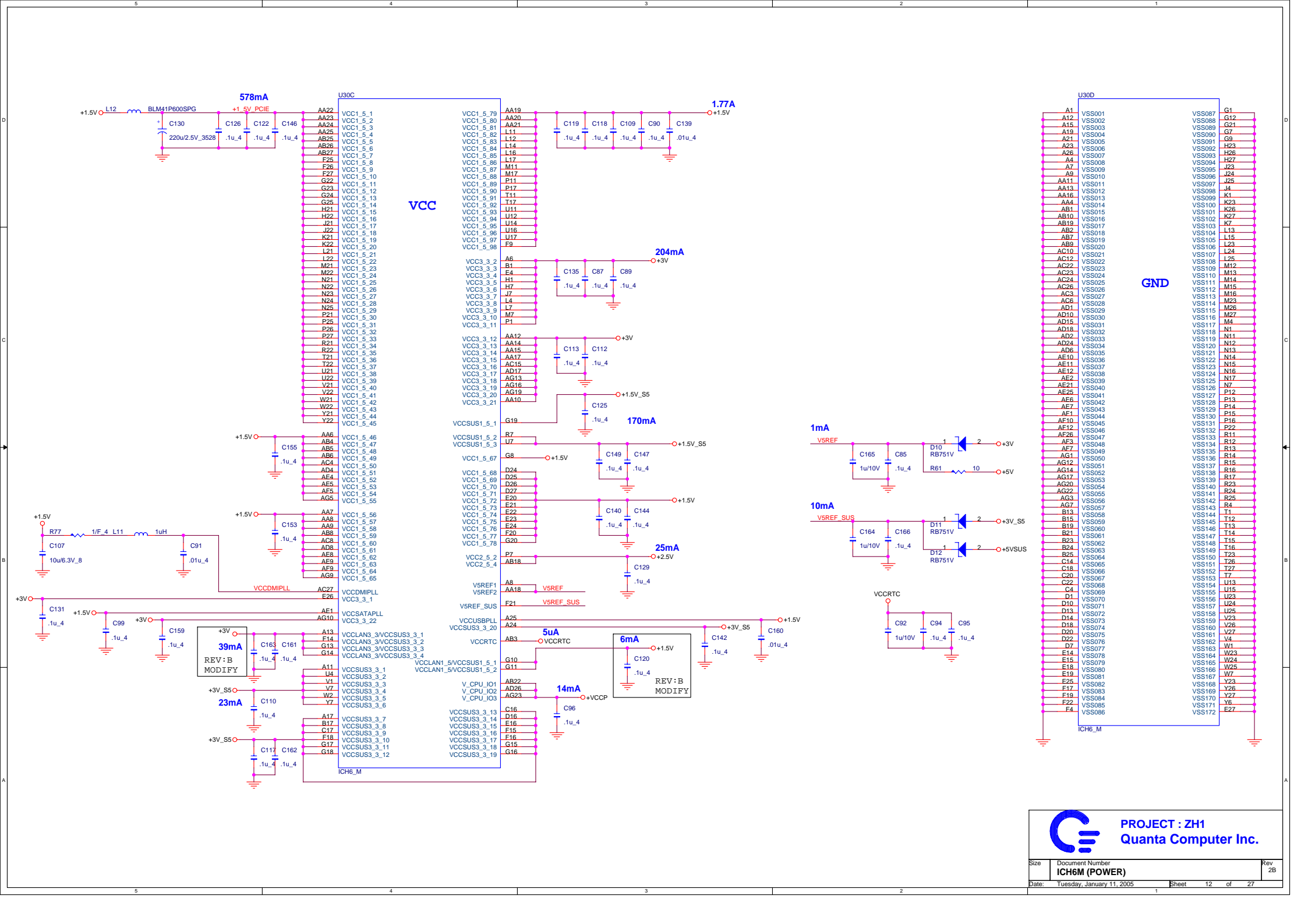
PR\_STS R113 10K 4  
ICH\_PWROK R73 10K 4  
RSMRST# R90 10K 4

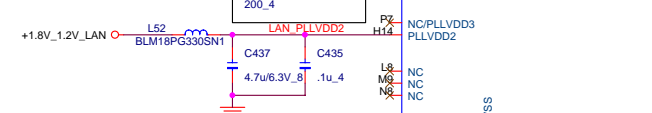
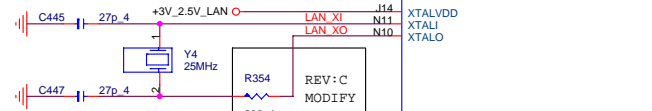
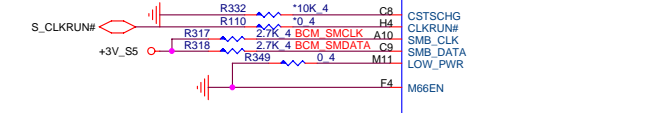
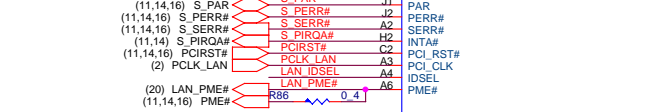
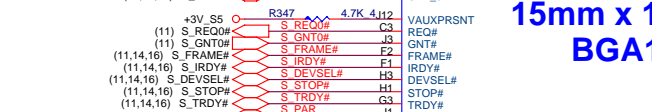
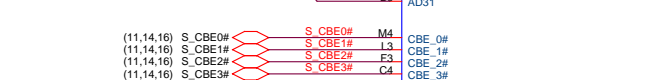
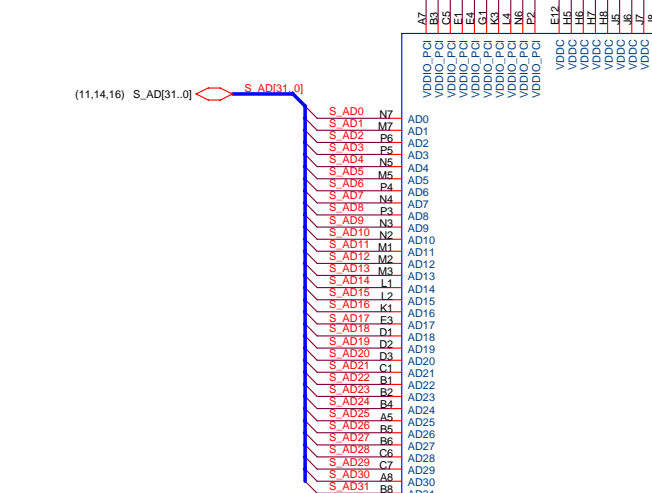
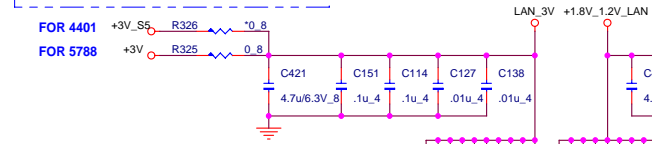


REV:B MODIFY

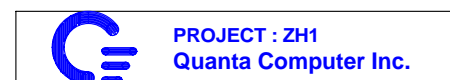
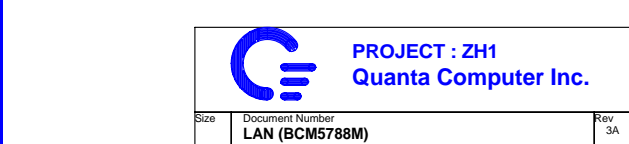
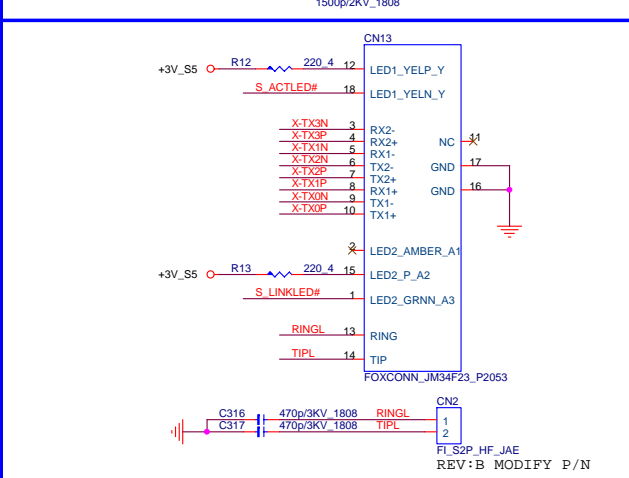
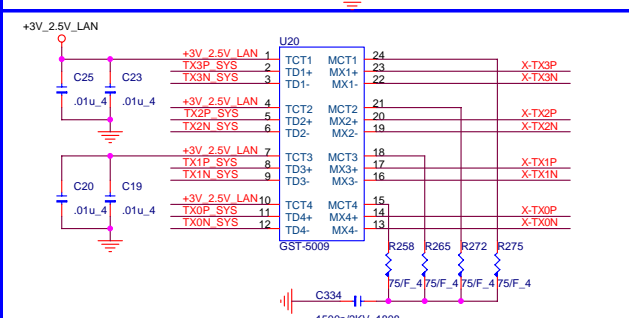
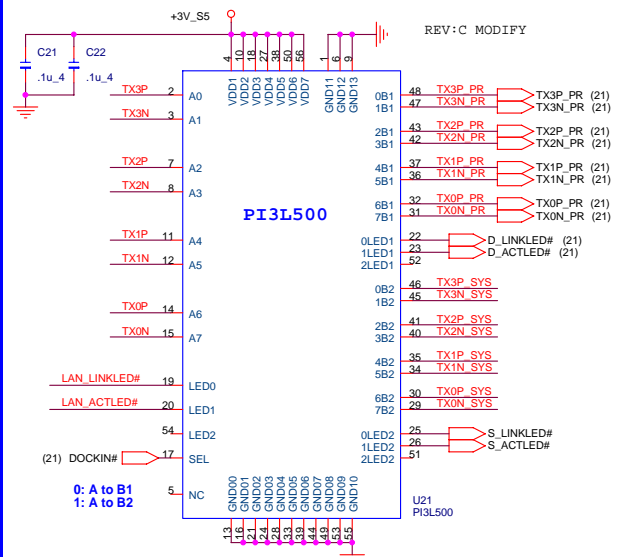
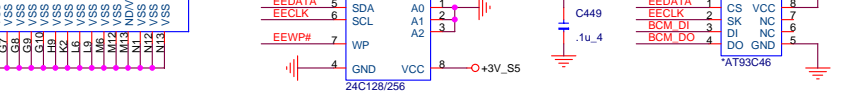
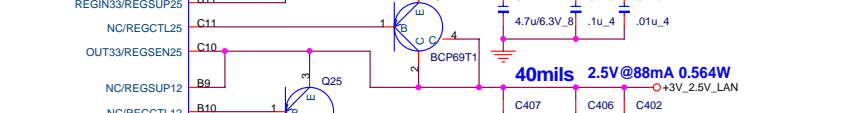
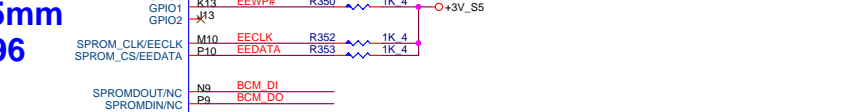
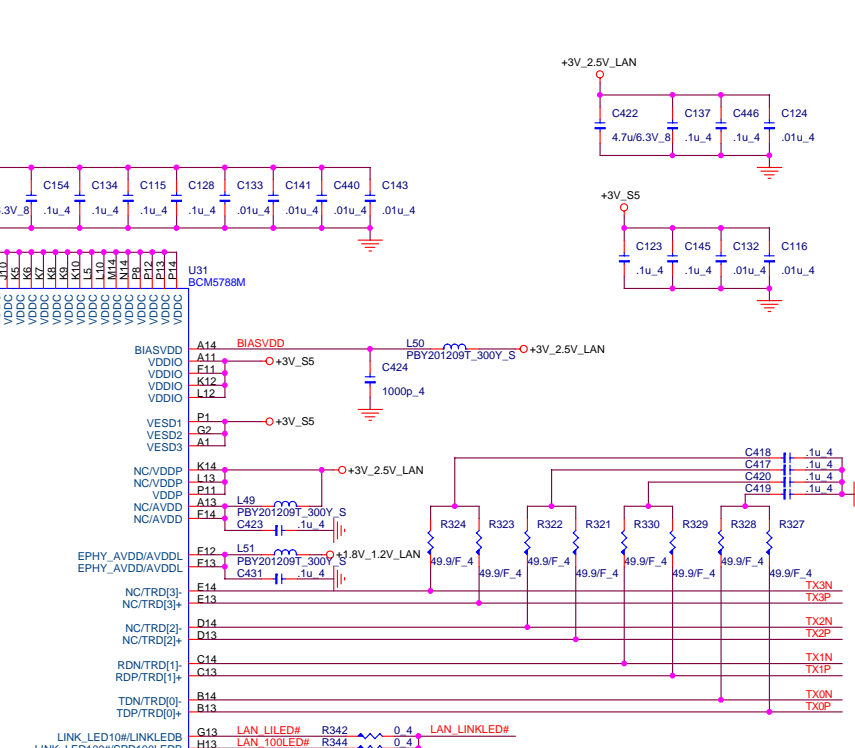
R117	100K 4
R112	100K 4
R145	1K 4
R111	1K 4



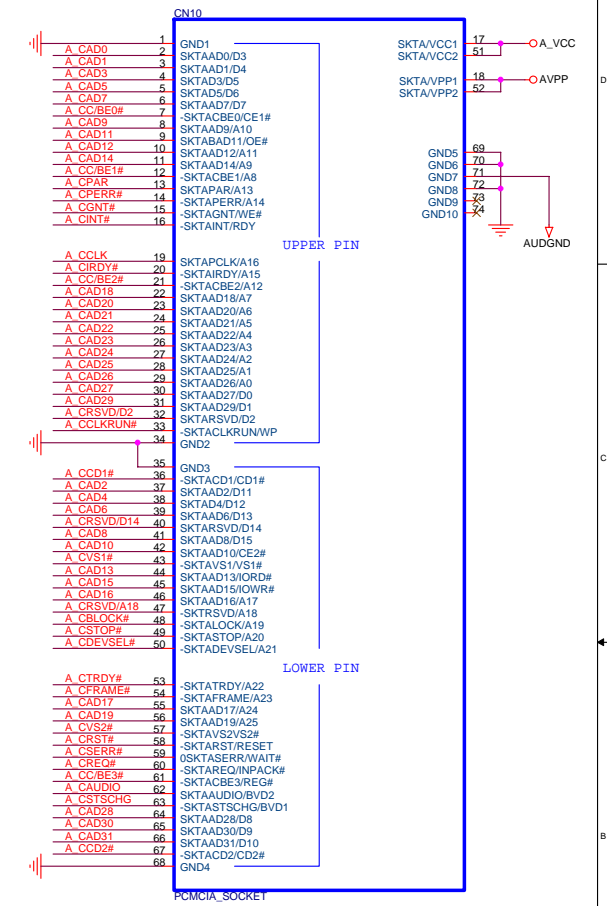
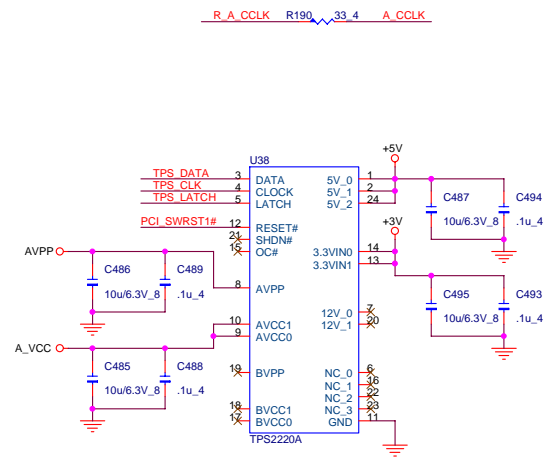
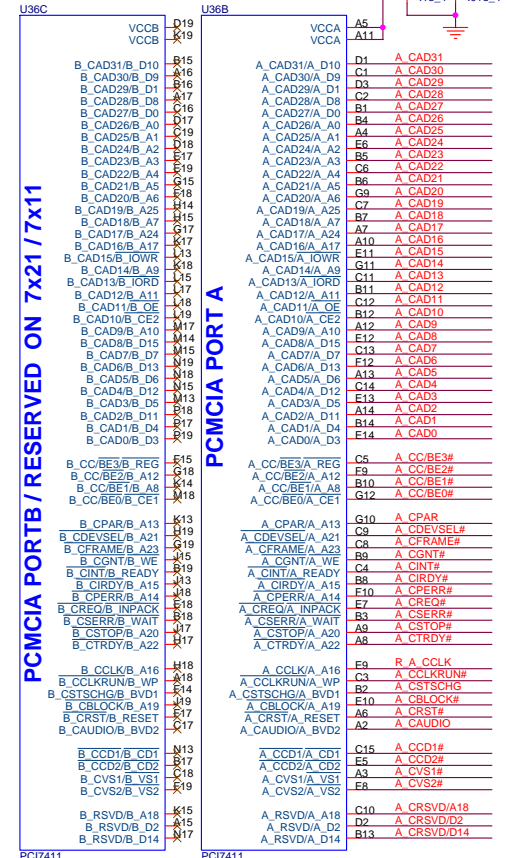
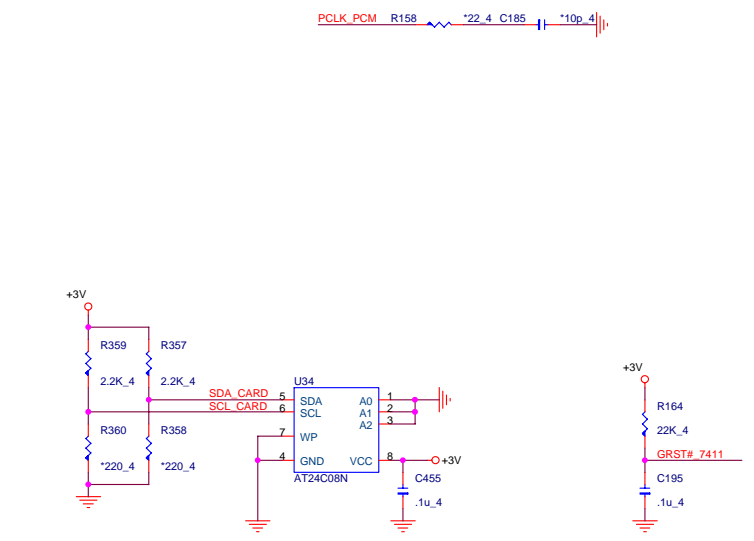
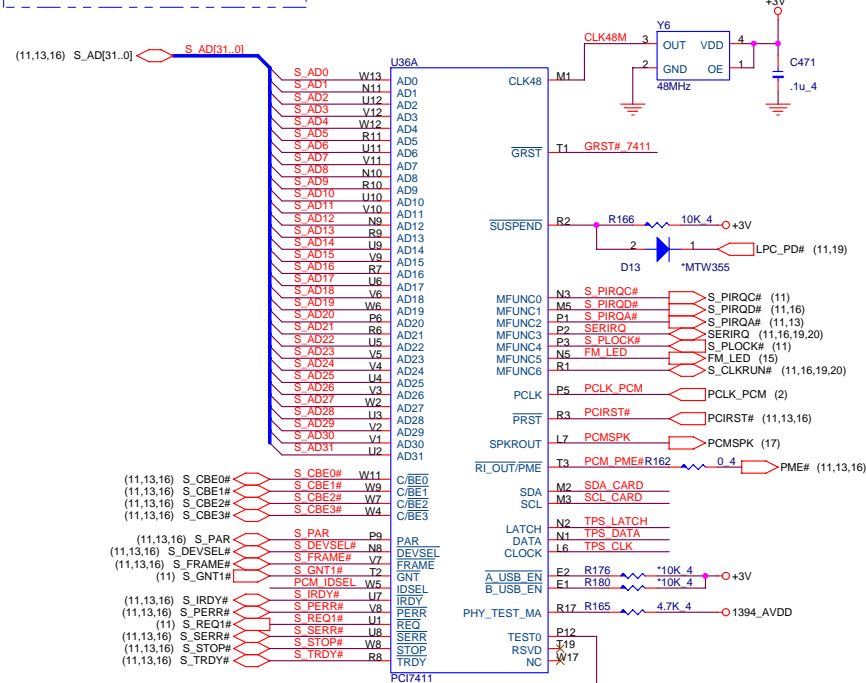




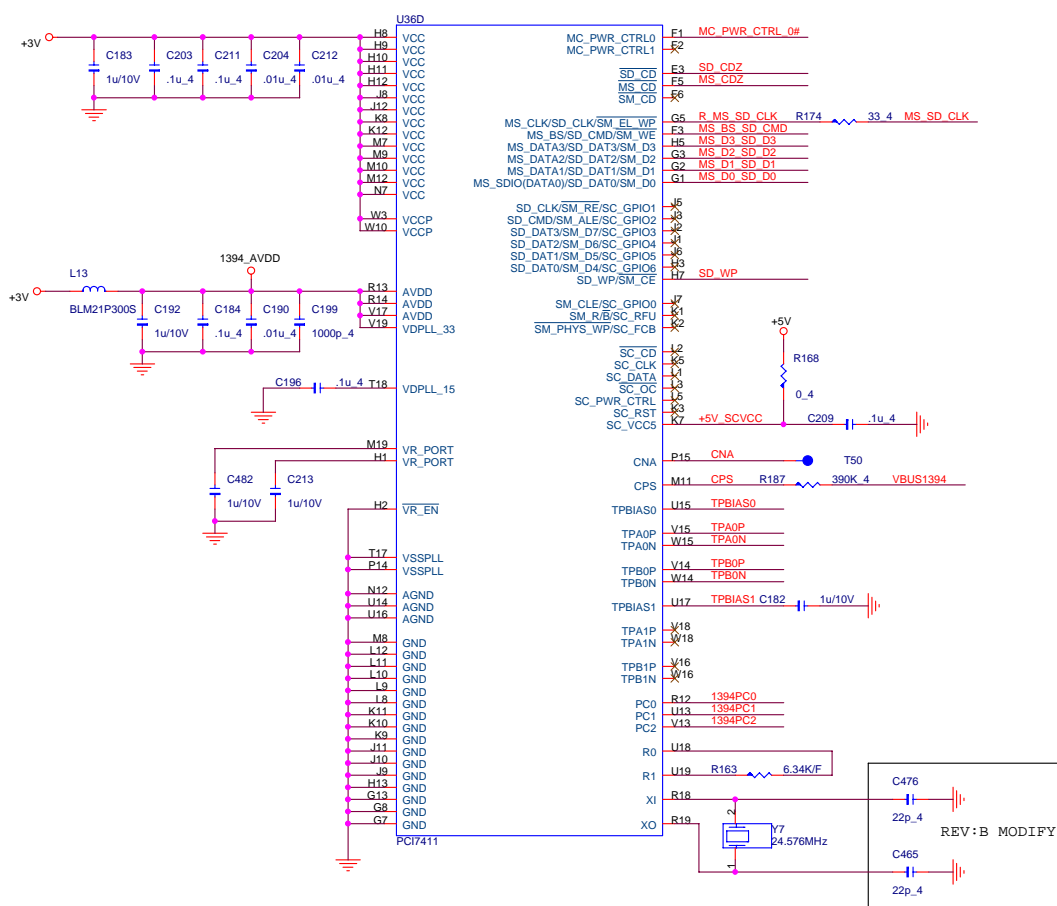
### 15mm x 15mm BGA196



REV: B MODIFY  
 S\_AD23 R159 150/F 4 PCMC\_IDSEL



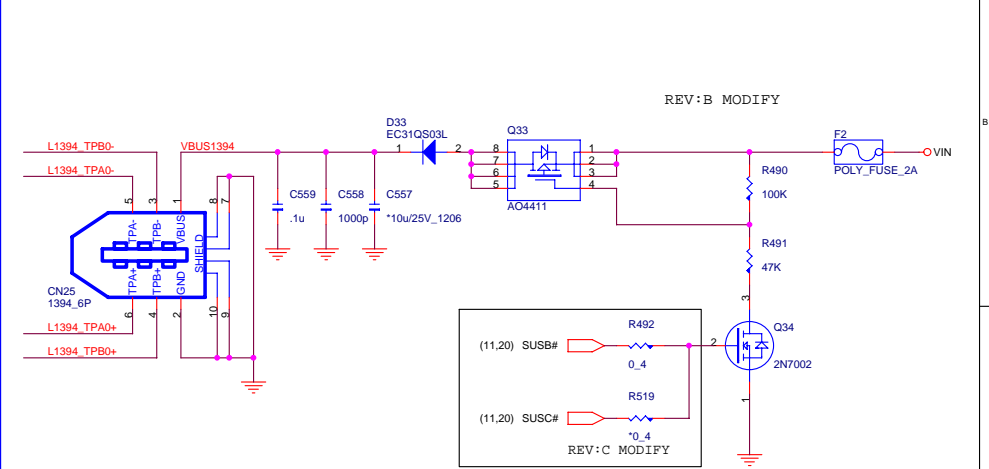
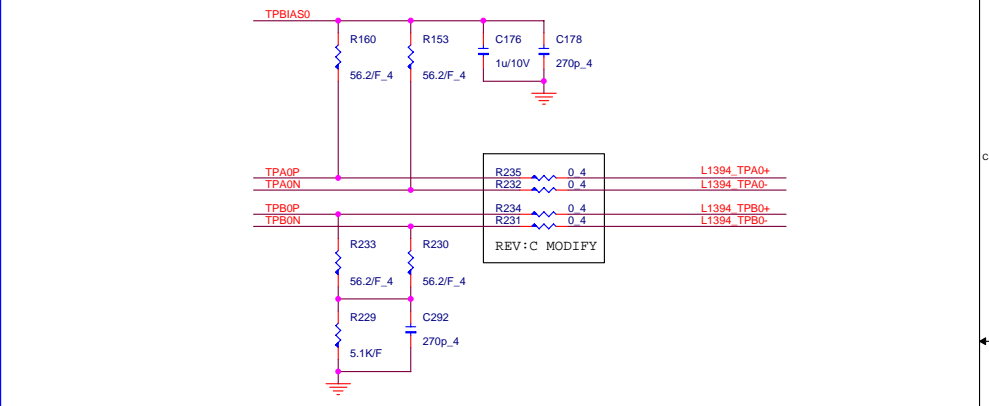
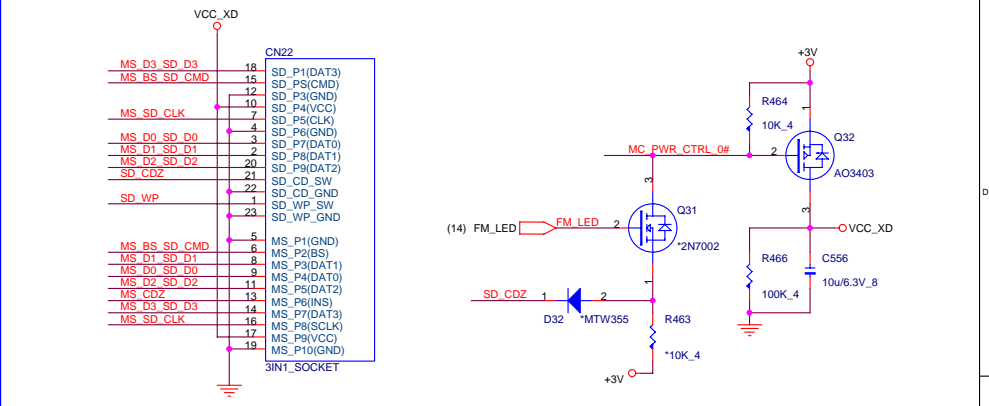
PROJECT : ZH1  
 Quanta Computer Inc.



**Power Class**

PC[2:0]	VBUS POWER
000	No Power
001	15W
010	30W
011	45W

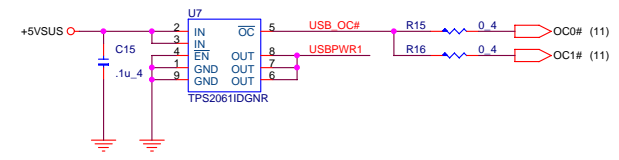
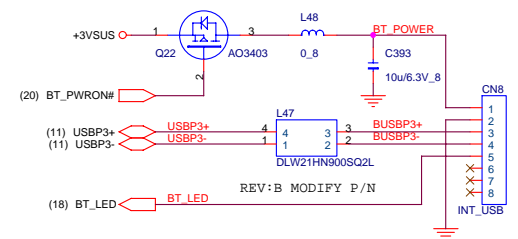
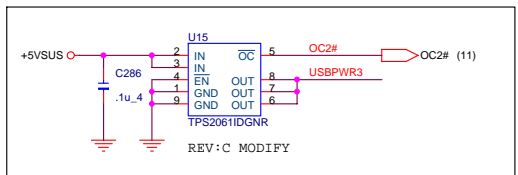
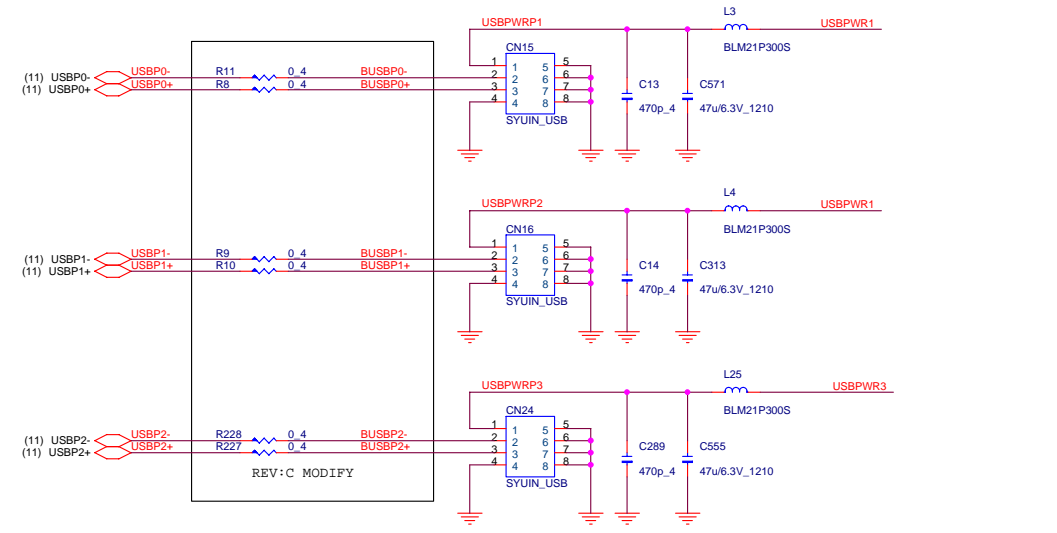
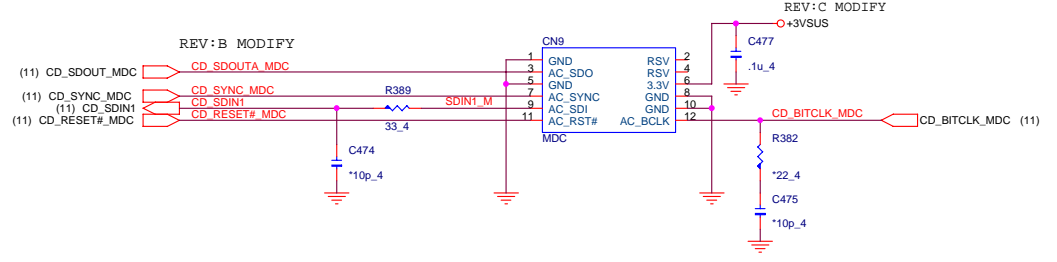
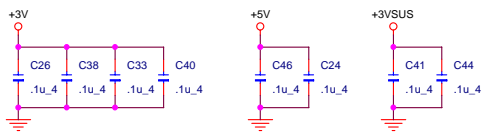
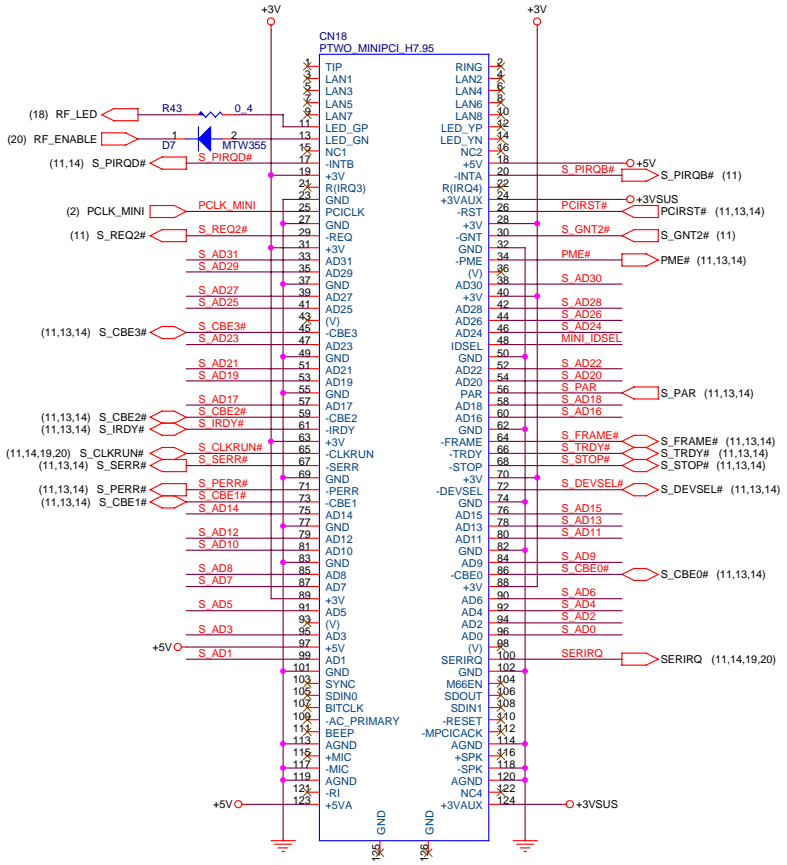
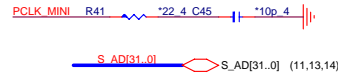
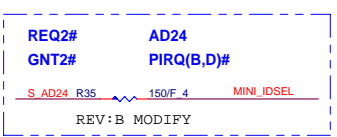
DEFAULT



**PROJECT : ZH1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>PC17411 (1394/3IN1)</b>	3A
Date:	Thursday, January 13, 2005	Sheet 15 of 27



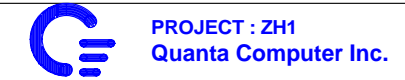
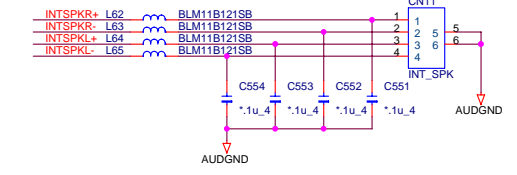
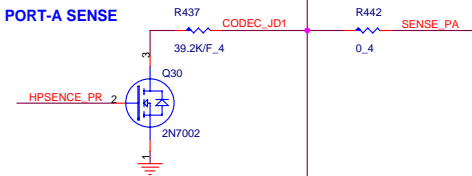
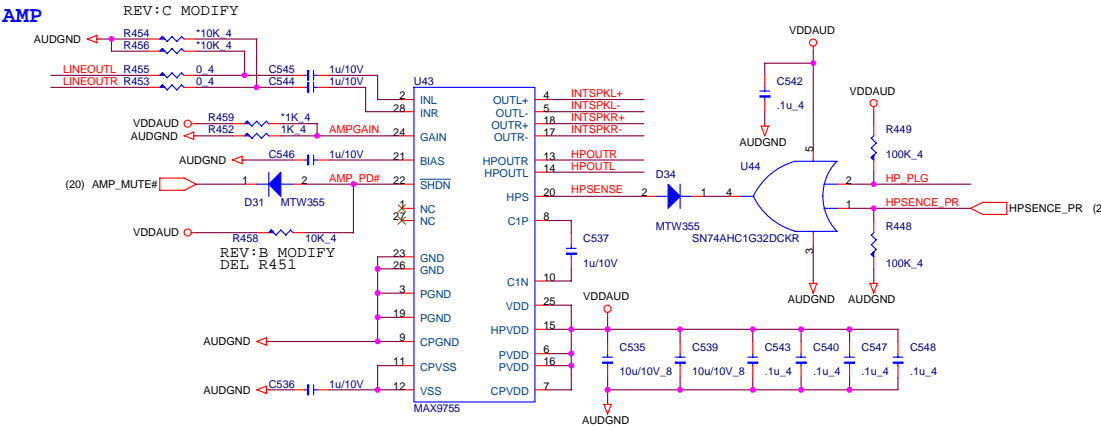
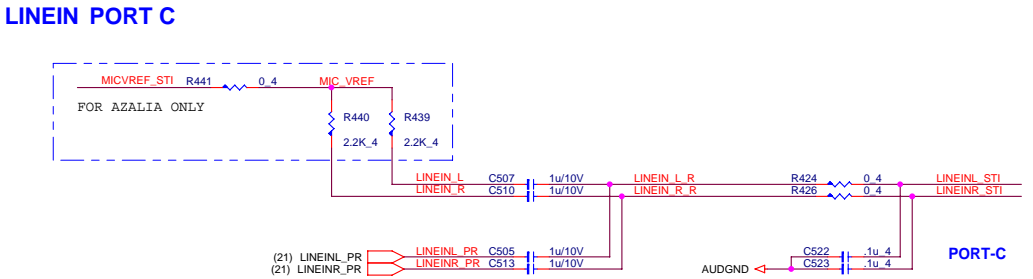
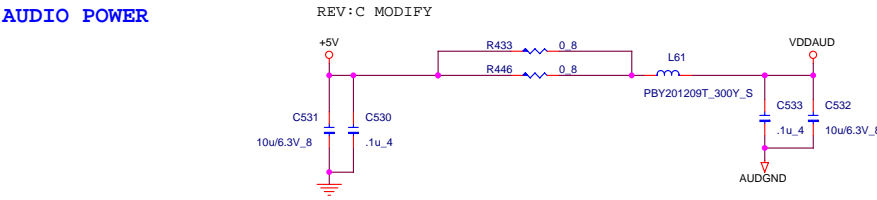
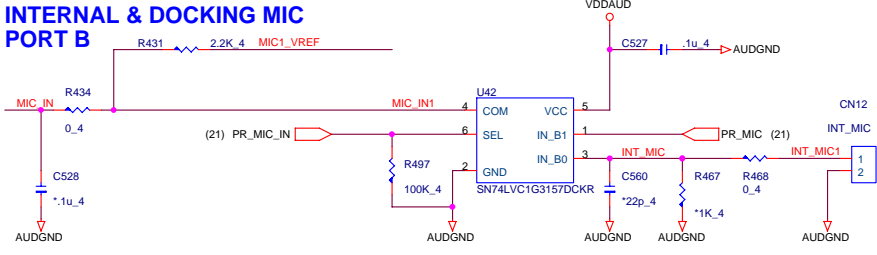
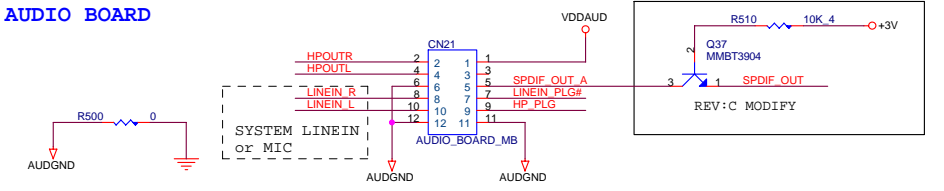
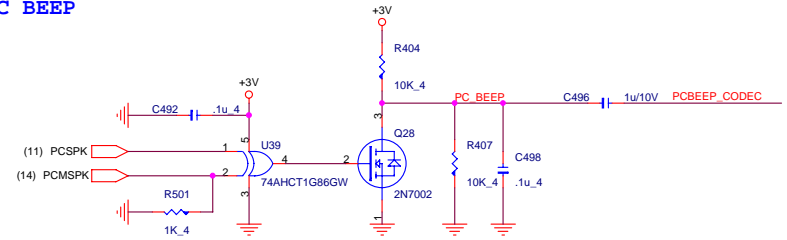
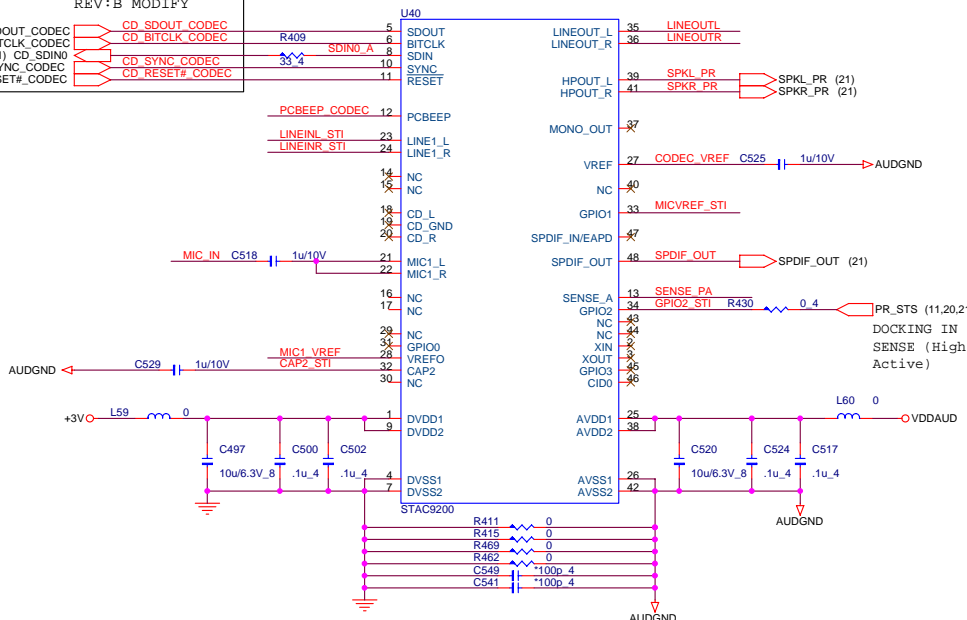


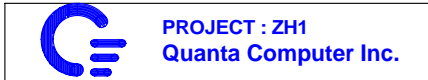
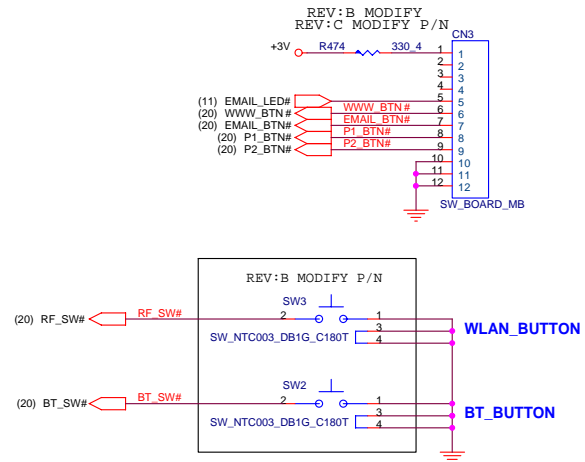
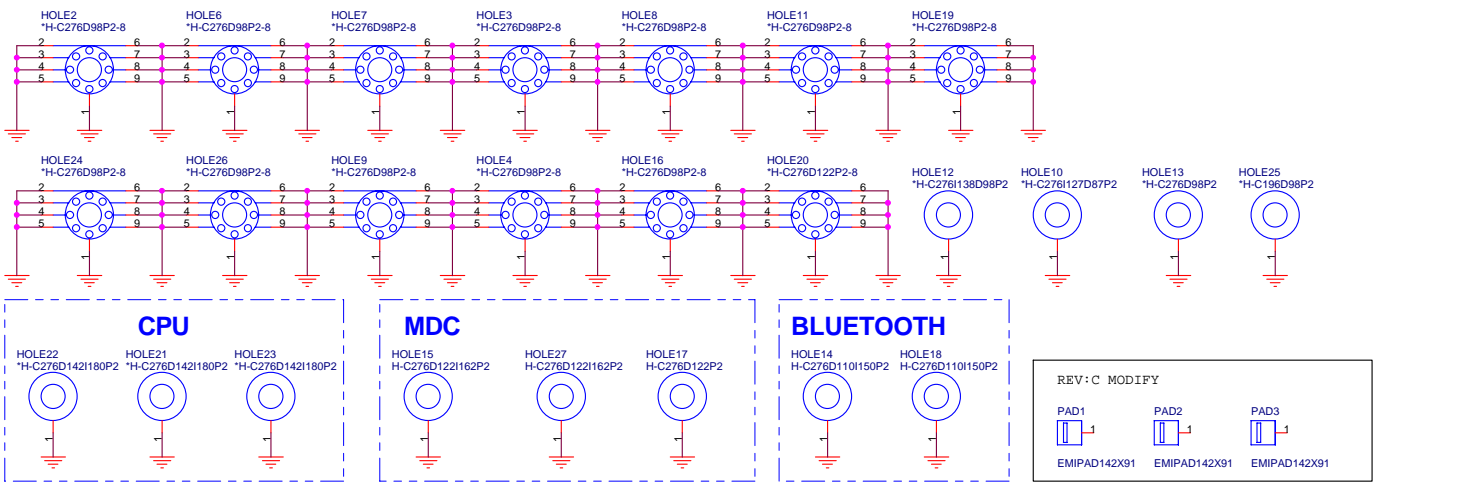
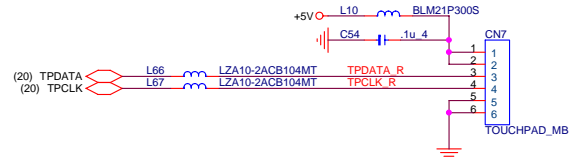
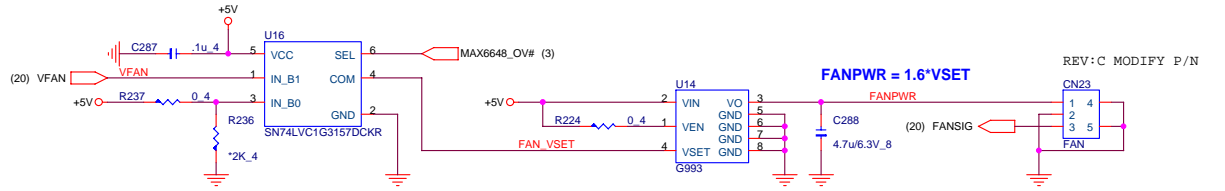
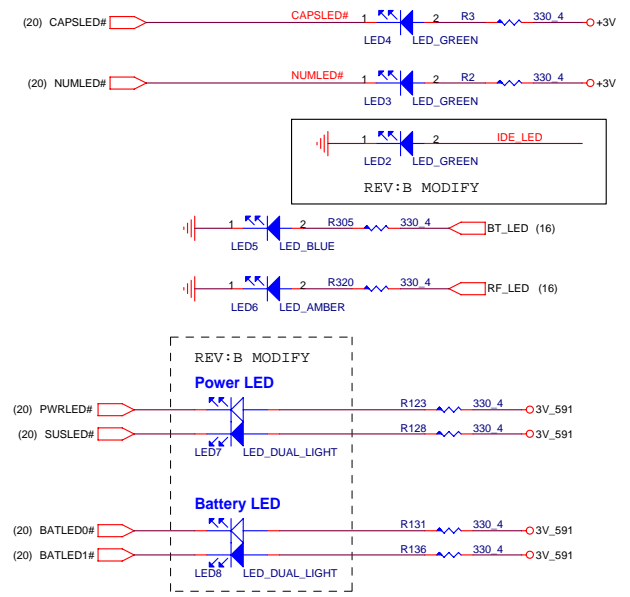
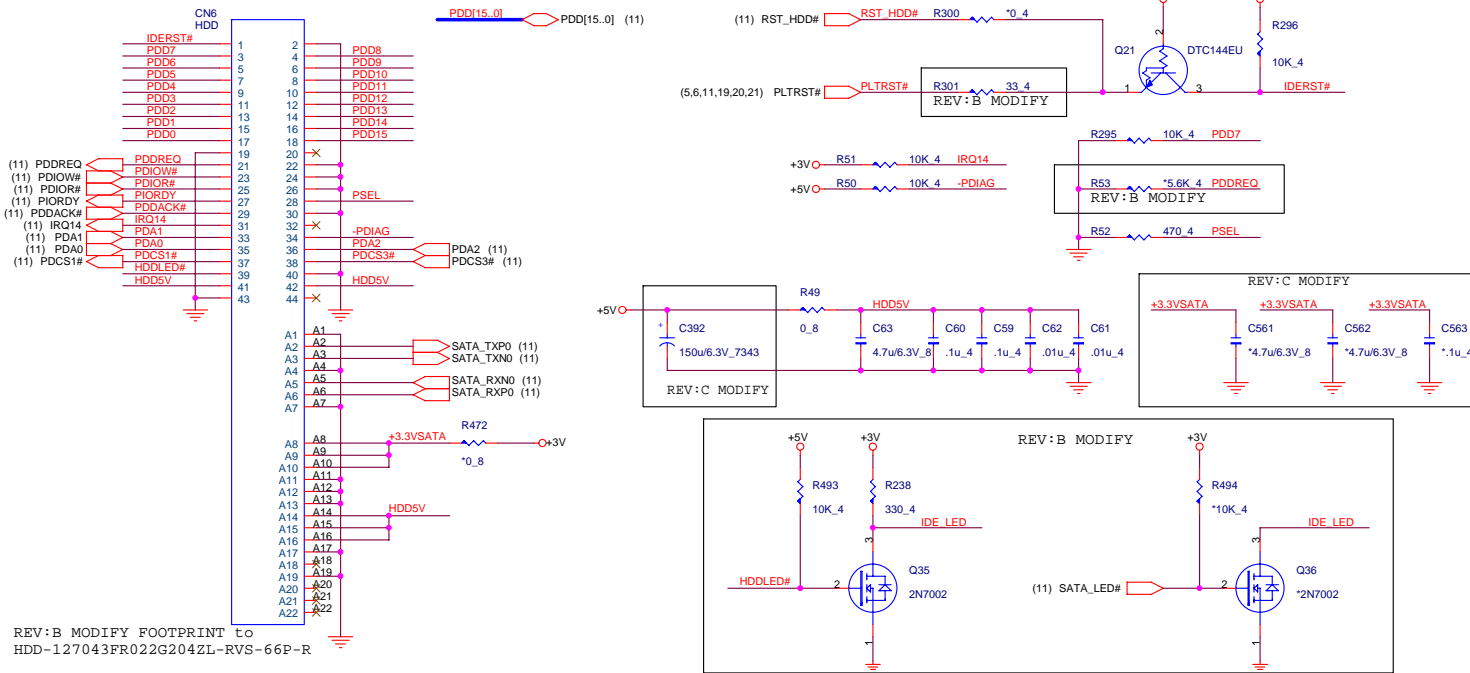
PROJECT: ZH1  
Quanta Computer Inc.

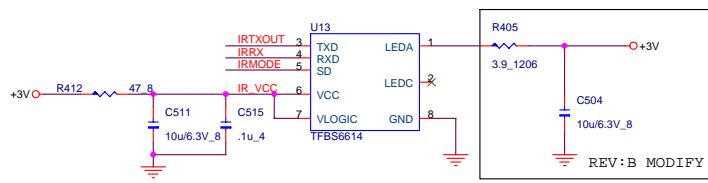
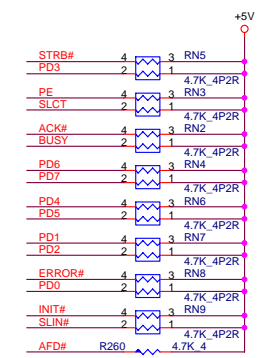
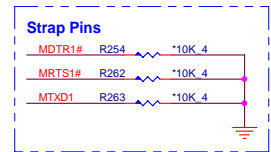
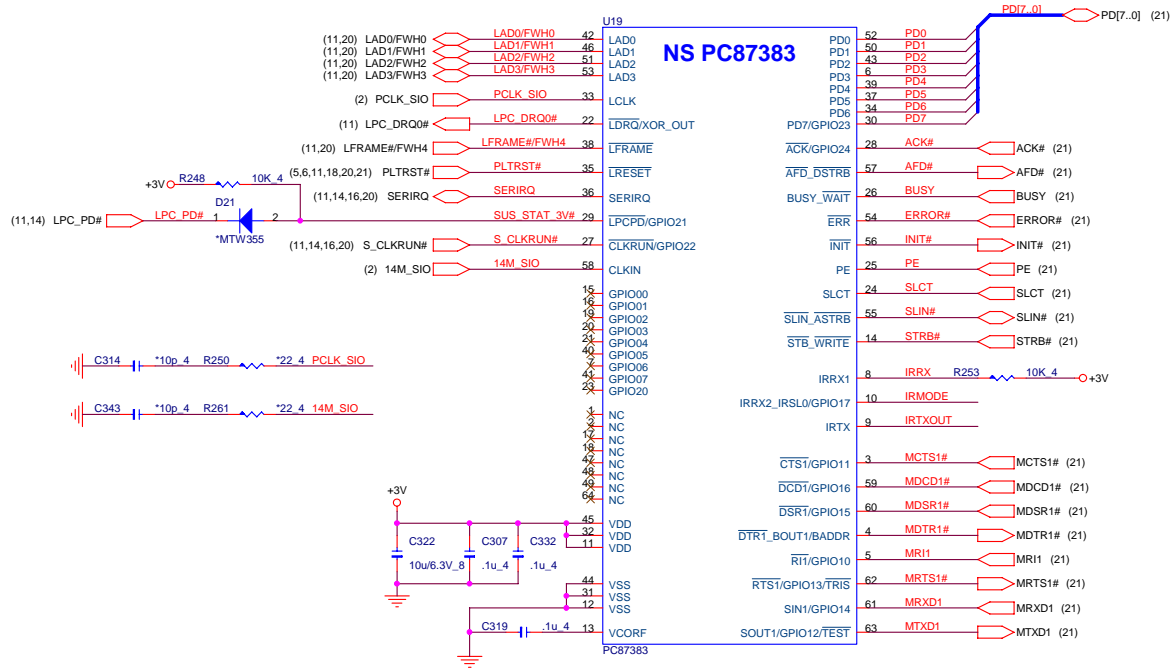
Size	Document Number	Rev
	MINIPCI/USB/MDC	3A
Date:	Tuesday, January 11, 2005	Sheet 16 of 27

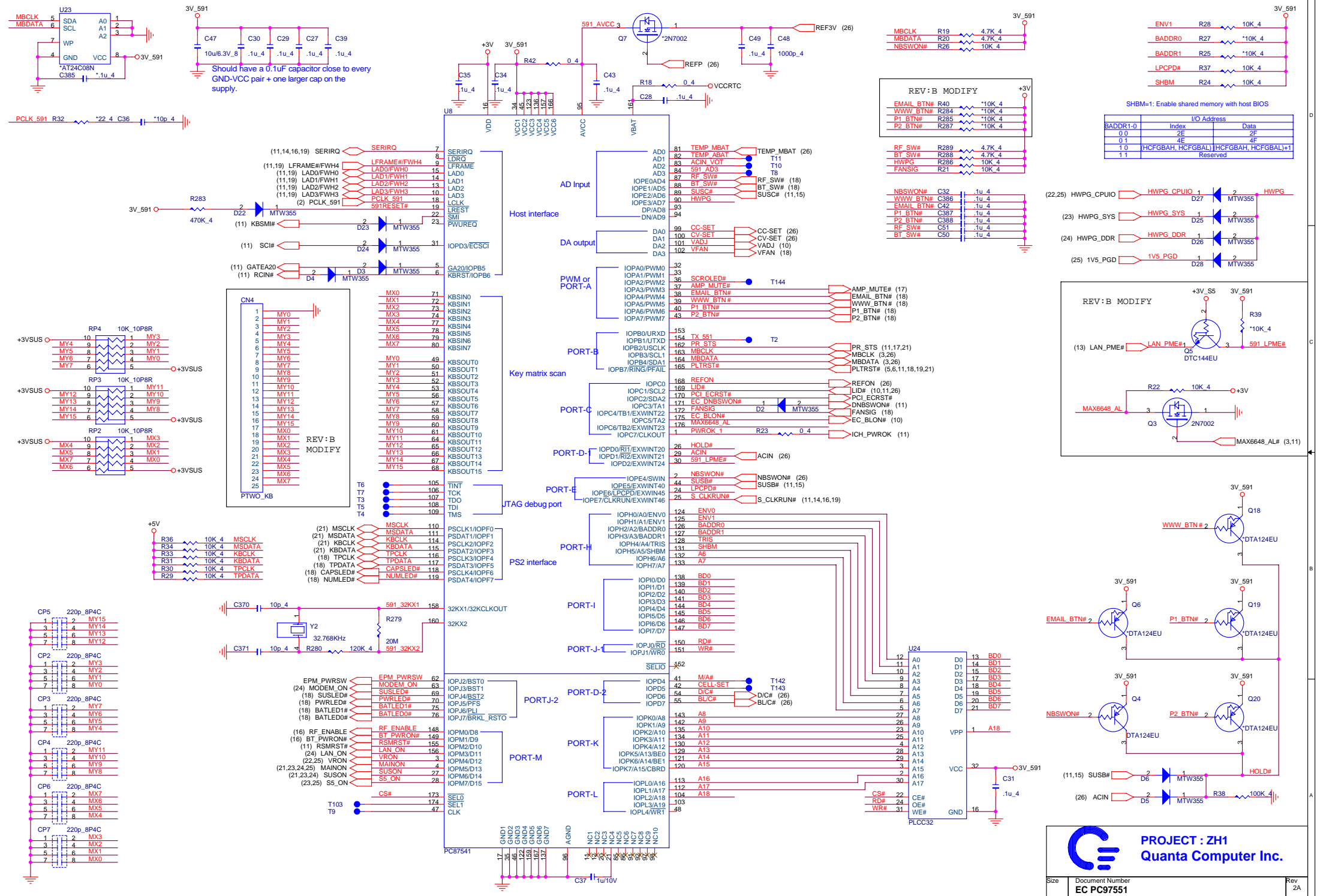
REV: B MODIFY

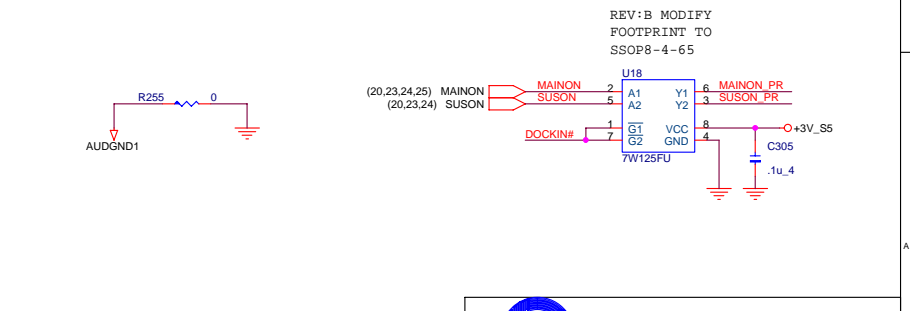
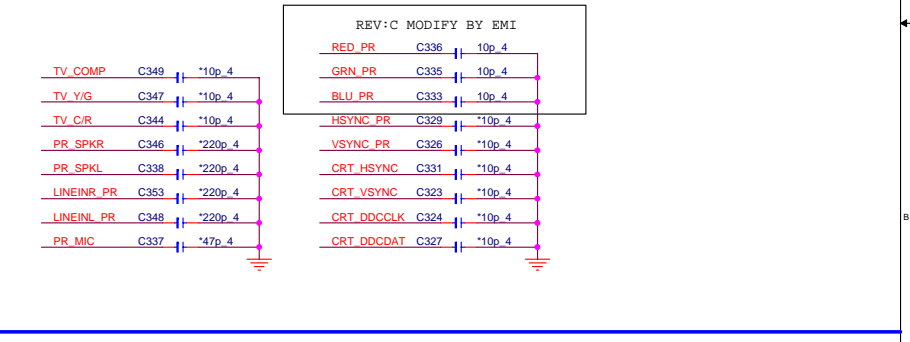
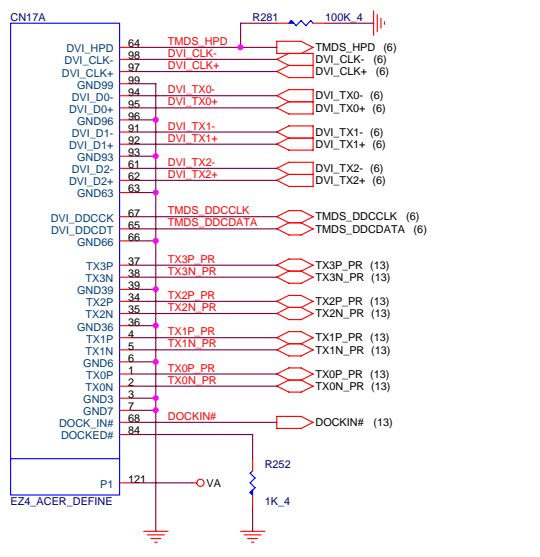
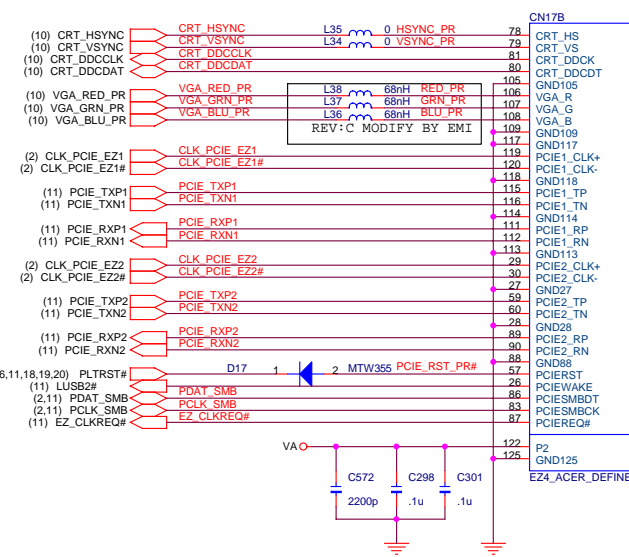
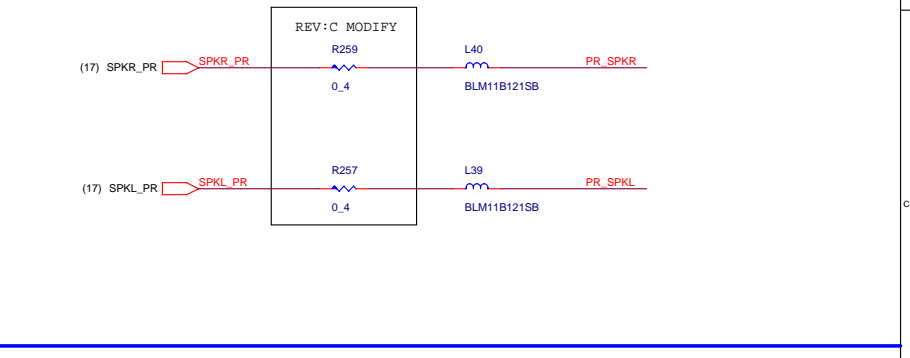
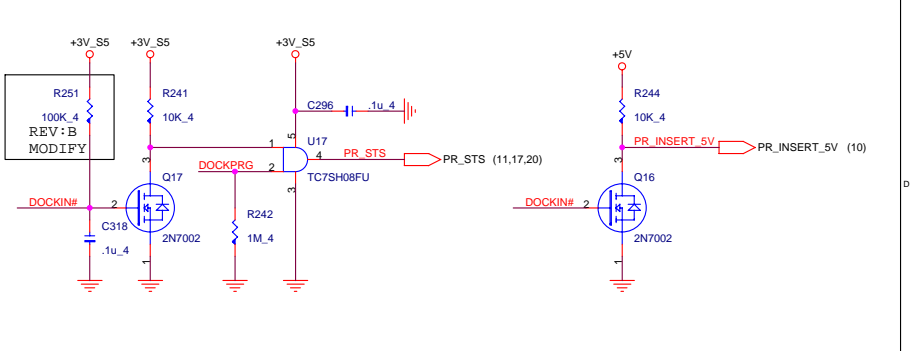
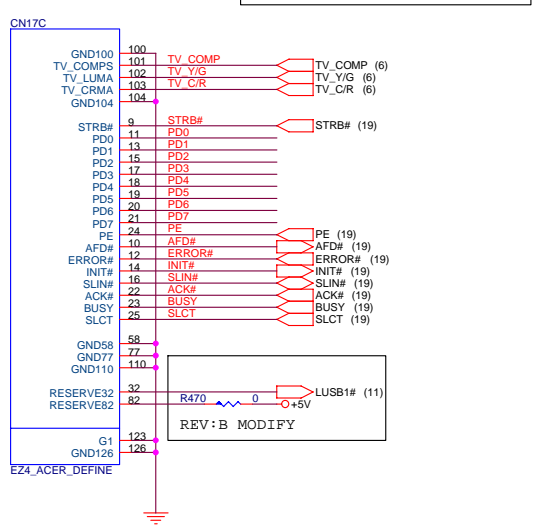
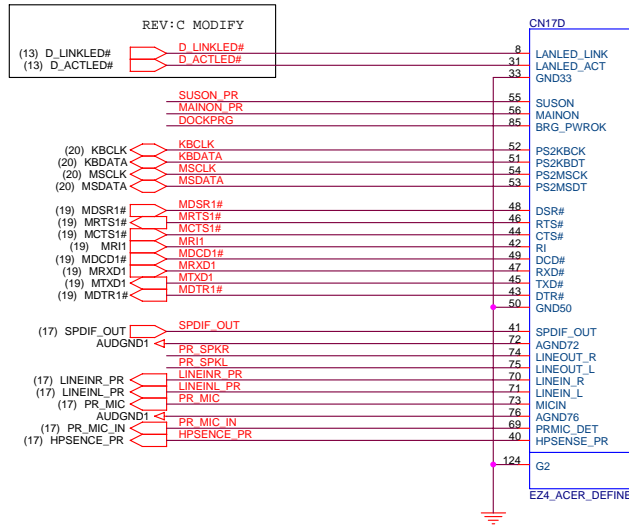
(11) CD_SDOUT_CODEC	CD_SDOUT_CODEC
(11) CD_BITCLK_CODEC	CD_BITCLK_CODEC
(11) CD_SDINO	CD_SYNC_CODEC
(11) CD_SYNC_CODEC	CD_RESET#_CODEC

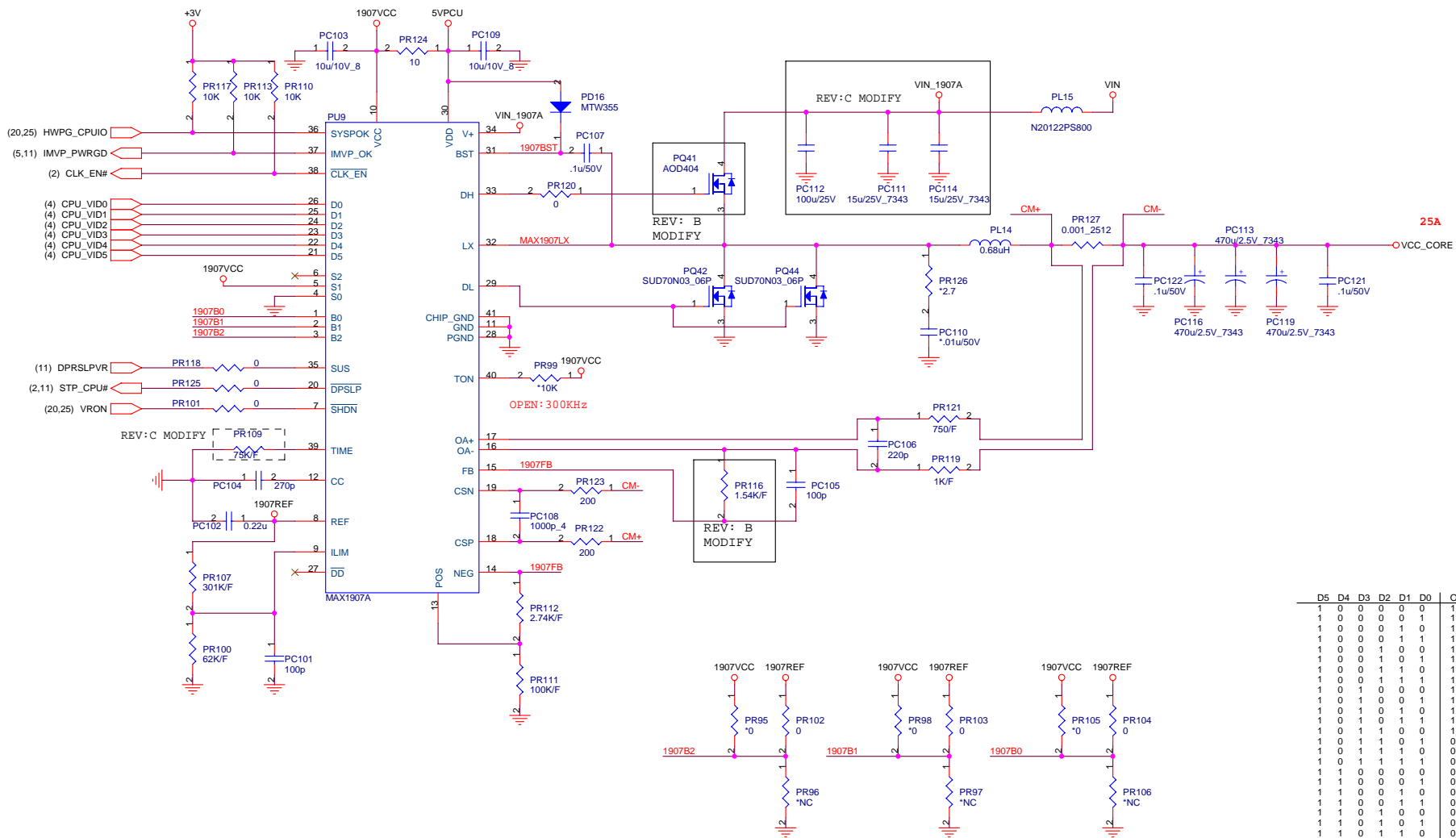












D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.184V	0	0	0	0	0	1	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	0	0	1.612V
1	0	1	0	0	0	1.084V	0	0	0	1	1	0	1.596V
1	0	1	0	0	1	1.068V	0	0	0	1	0	0	1.580V
1	0	1	0	1	0	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	1	1.036V	0	0	1	0	1	0	1.548V
1	0	1	1	0	0	1.020V	0	0	1	0	1	0	1.532V
1	0	1	1	0	1	1.004V	0	0	1	0	0	0	1.516V
1	0	1	1	1	0	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	1	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	0	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output	
✓	OPEN	VCC	GND	0.748V

VCC\_BOOT

B2	B1	B0	Output	
✓	GND	GND	GND	1.708V
	REF	REF	REF	1.372V
	OPEN	OPEN	OPEN	1.036V
	VCC	VCC	VCC	0.700V
	REF	VCC	VCC	1.212V

**PROJECT : ZH1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CPU CORE (MAX1907)</b>	<b>3A</b>
Date:	Tuesday, January 11, 2005	Sheet 22 of 27

