

ZK2 SYSTEM BLOCK DIAGRAM

BOM MARK
 I@: INT VGA
 E@: STUFF FOR EXT VGA
 ND@: STUFF FOR NON-DOCK
 D@: DOCK
 SP@: SPECIAL FOR EXT/INT VGA

CLOCK GENERATOR
 ICS: ICS9LPRS365BGLFT
 SELGO: SLG8SP512K05
 P2

XTAL 14.318MHz

Penryn 479
 uFCPGA
 P3, P4

Thermal Sensor
 (NS LM95245)
 P3

Fan Driver
 (G991)
 P30

DDR PWR TPS5116 P36	CHARGER ISL6251 P32
THERMAL PROTECTION P37	3/5V SYS PWR ISL6237 P33
2.5V/ 1.5V PWR DISCHARGER P38	CPU CORE PWR ISL6262A P34
POWER TREE P39	+1.05V RT8202 P35

DDRII
 SO-DIMM 0
 SO-DIMM 1
 P16

Dual Channel DDR2
 667/800 MHz

NB Cantiga
 (GM45/ PM45/ GL40)
 P5, P6, P7, P8, P9, P10, P11

MXM (n-Vidia) NB9M-GS
 VRAM 512MB
 P17

SWITCH CIRCUIT
 P18

HDMI switch (PS8122)
 P19

CRT
 P18

LVDS
 P18

HDMI
 P19

DOCKING/DVI
 P19

FSB
 667/800/1067 Mhz

X4 DMI interface

MP-Stage
 31ZK2MB0000: ZK2 MB ASSY(GM/UMA)ASSY W/O CPU
 31ZK2MB0010: ZK2 MB ASSY(PM/MXM)ASSY W/O CPU
 31ZK2MB0020: ZK2 MB ASSY(PM/MXM) W/O CPU/E-SATA

HDD (SATA) *2
 P23

ODD (SATA)
 P23

eSATA Conn.
 USB1 P29

eSATA Buffer
 (PI2EQX3021) P29

USB Port x 3
 USB0, 4, 7 P29

Bluetooth
 USB5 P21

CCD
 USB11 P18

FingerPrint
 USB9 P30

Wire Docking
 USB10 P30

Audio CODEC (ALC888S)
 P24

MDC 1.5
 P24

EC (WPC775LDG)
 P31

HDCP ROM (Option)
 P13

SPI ROM
 P31

Touch Pad
 P30

K/B COON.
 P30

MMB
 P28

CIR
 P31

SB ICH9M
 P12, P13, P14, P15

PCI-Express

PCI-E-1

PCI-E-2&4

PCI-E-6

USB8

X'TAL 32.768KHz

X'TAL 25MHz

Media Cardreader (RTS5158E)
 USB2 P27

ATHEROS Giga-LAN (AR8121)
 P20

New Card
 USB6 P26

Mini Card WLAN / TV
 USB2 & 3 P22

Card Reader Connector
 P27

LAN SWITCH (PI3L500)
 P21

DOCK/LAN
 P30

Transformer
 P21

RJ45
 P21

Audio Amplifier
 P24, P25

Sub-Amplifier (MAX9736B)
 P25

Speaker
 P25

S/PDIF
 P25

SUBWOOFER
 P25

Line in
 P25

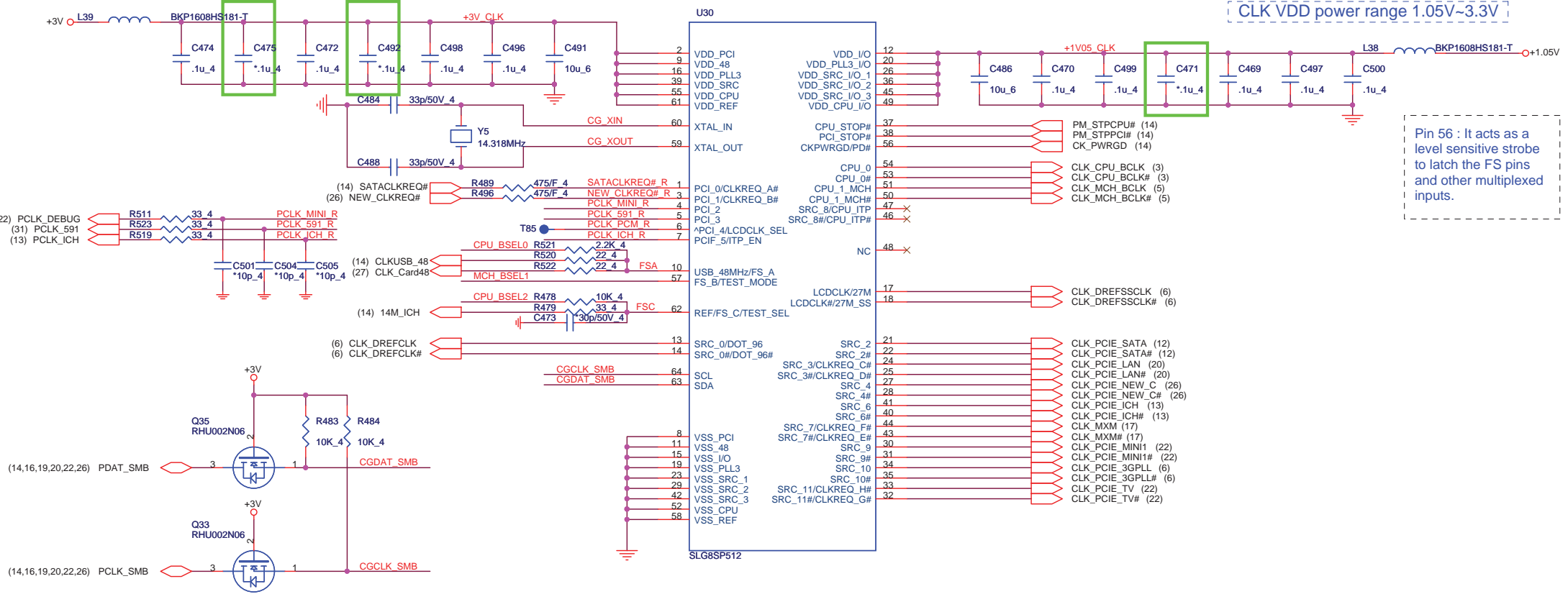
MIC Jack
 P25

Int. D-MIC
 P18, P24

DA0ZK2MB6D0
 DA0ZK2MB6C0
 DA0ZK2MB6B0
 DA0ZK2MB6A0

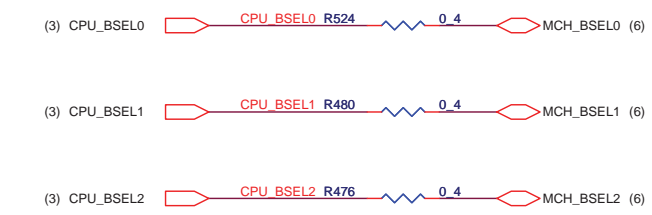
Quanta Computer Inc.
 PROJECT : ZK2
Block Diagram
 Date: Friday, June 27, 2008 Sheet 1 of 39

Clock Generator



CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

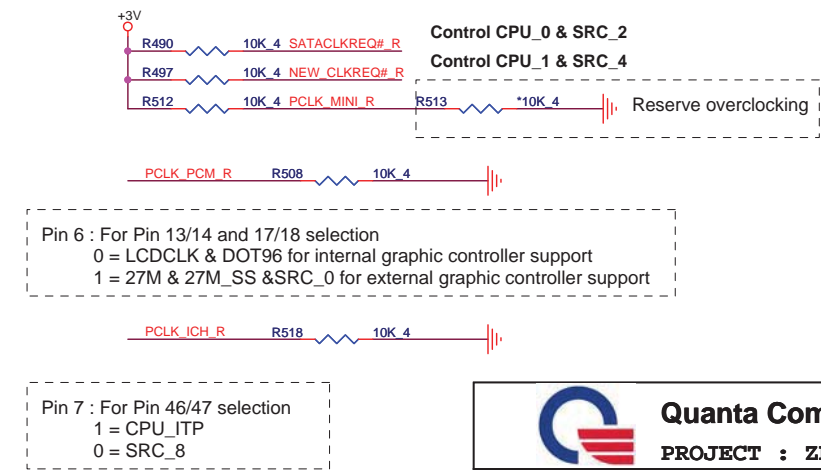


BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

<http://laptop-motherboard-schematic.blogspot.com/>

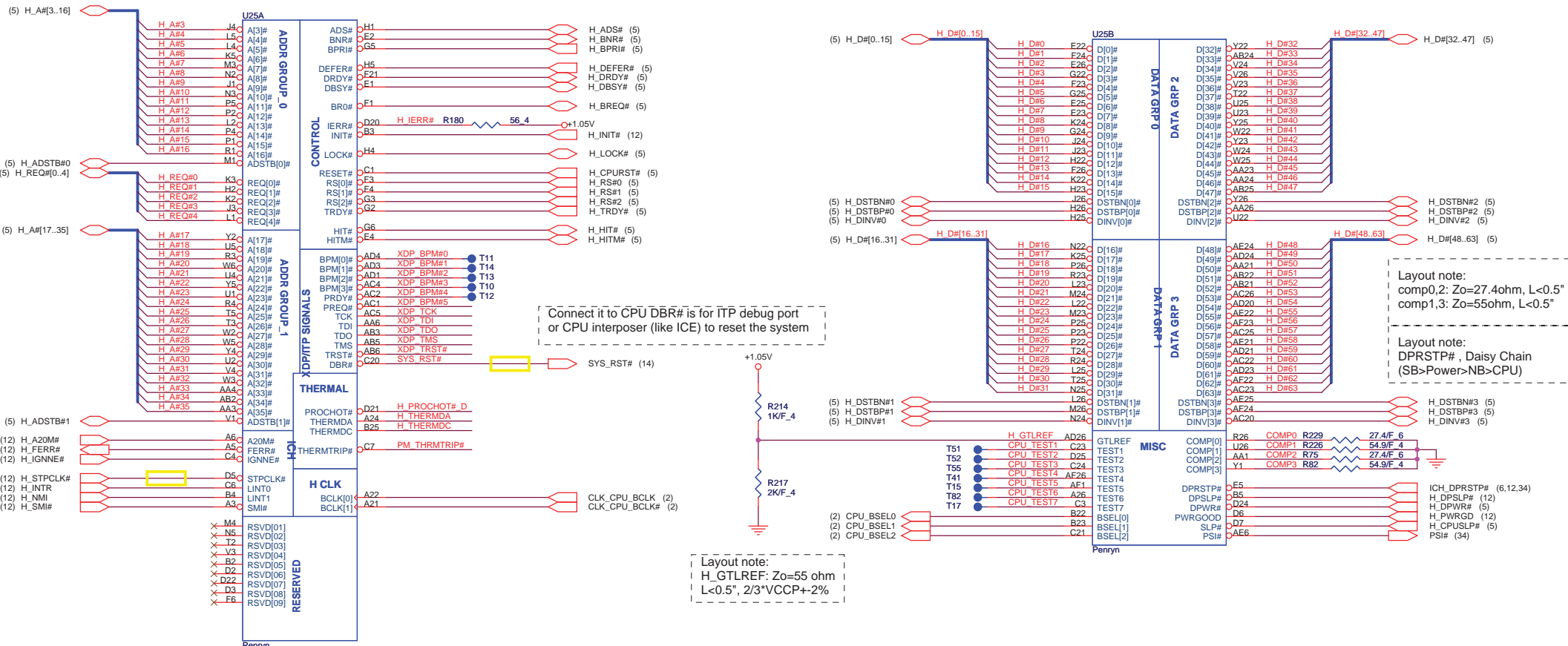


CLOCK GENERATOR

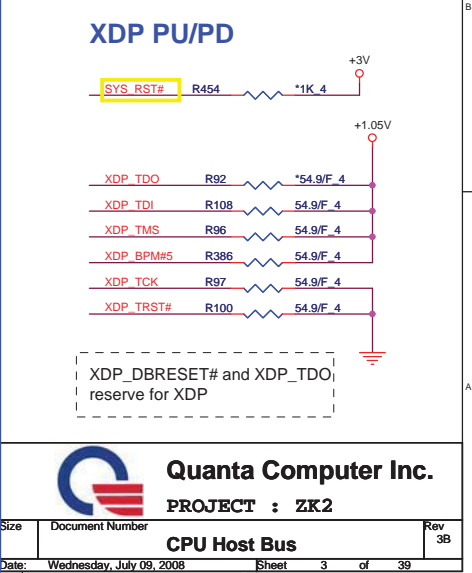
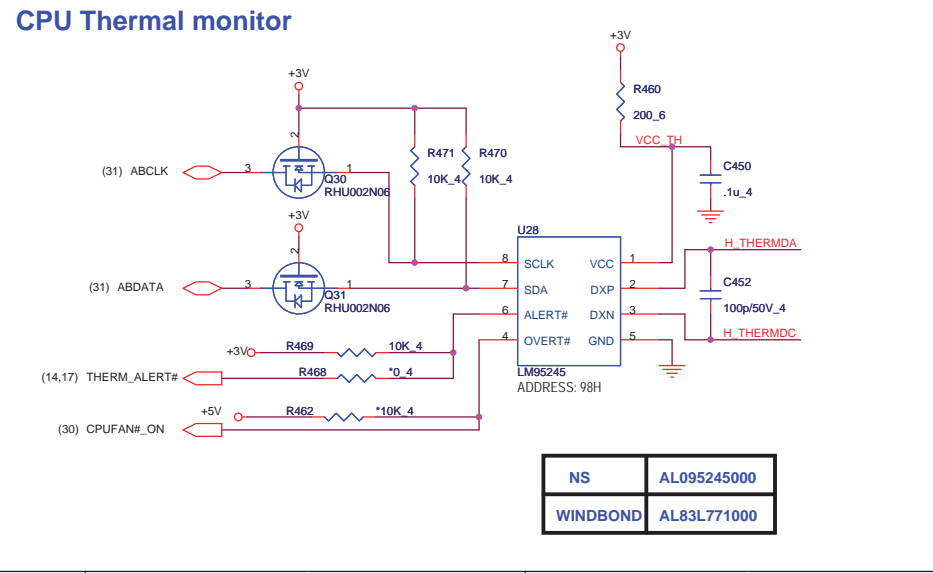
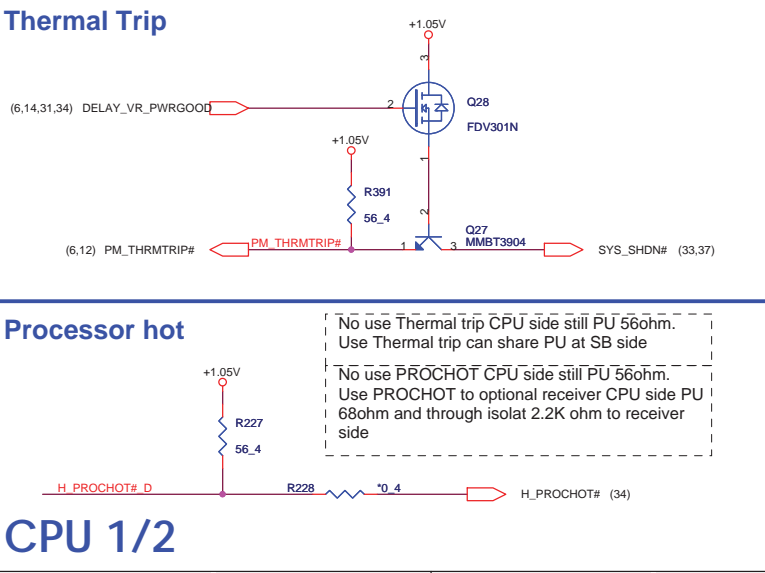
Quanta Computer Inc.

PROJECT : ZK2

Size	Document Number	Rev
	CLOCK GENERATOR	3B
Date:	Wednesday, July 09, 2008	Sheet 2 of 39

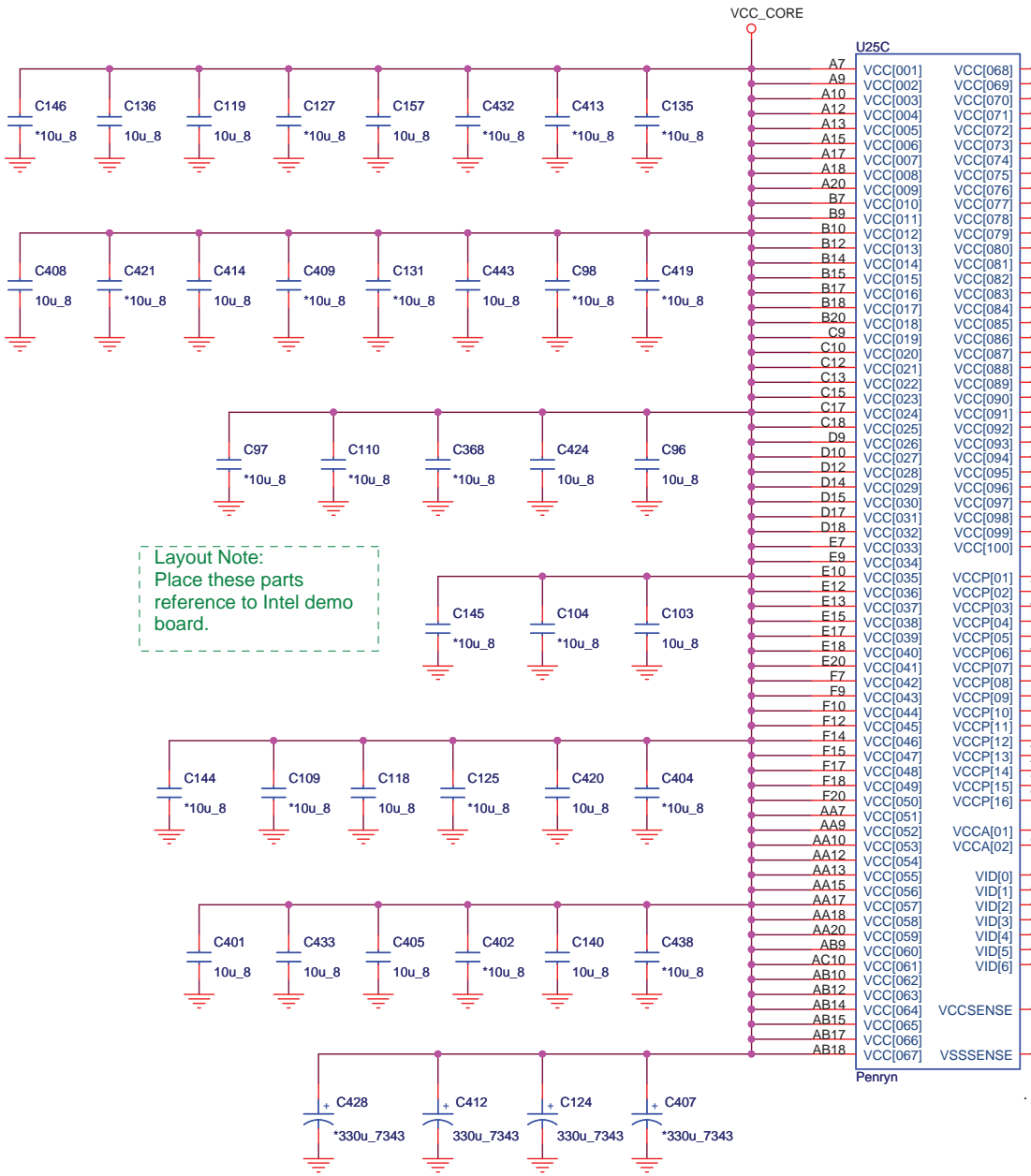


<http://laptop-motherboard-schematic.blogspot.com/>



U25D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F24	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

CPU 2/2

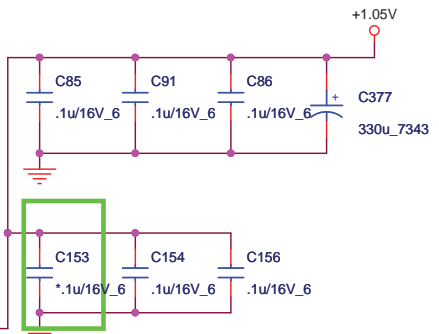


Layout Note:
Place these parts
reference to Intel demo
board.

VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



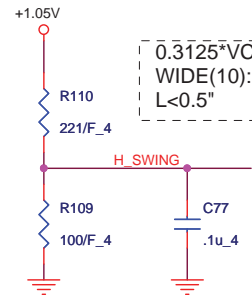
VCCA:130mA
+1.5V

Layout Note:
Z0=27.4,PU/PD L<1"

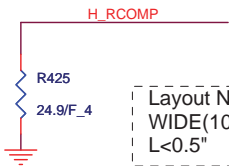
<http://laptop-motherboard-schematic.blogspot.com/>
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

		Quanta Computer Inc.	
		PROJECT : ZK2	
Size	Document Number	CPU Power	
Date:	Friday, June 27, 2008	Sheet	4 of 39
		1	3B

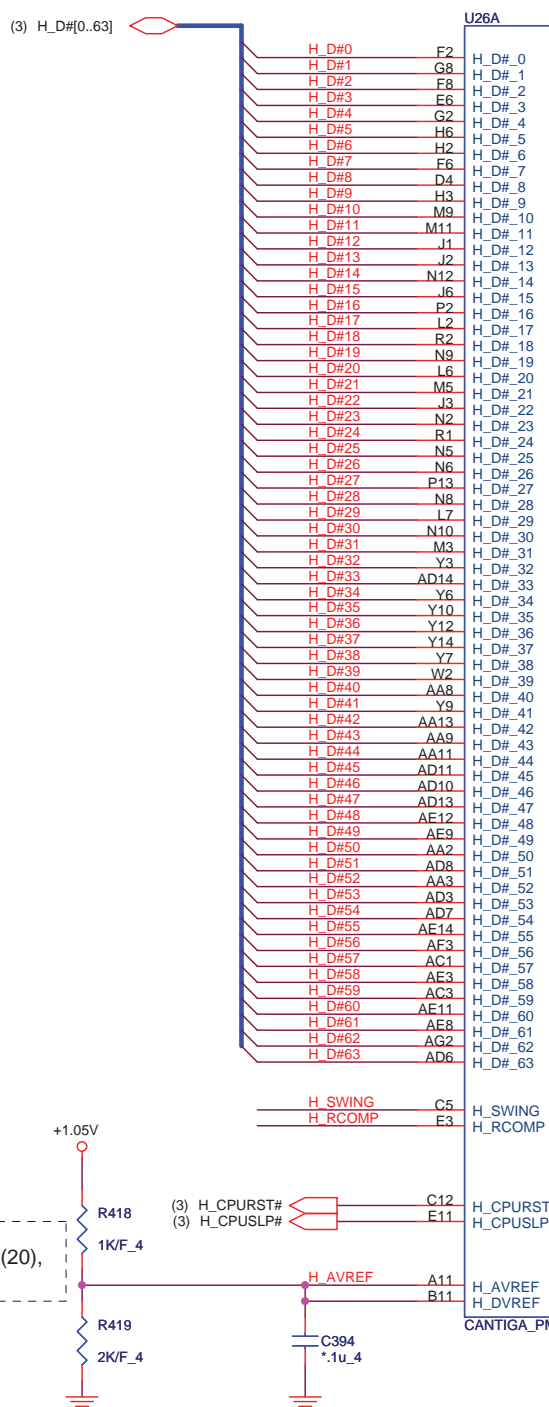
	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



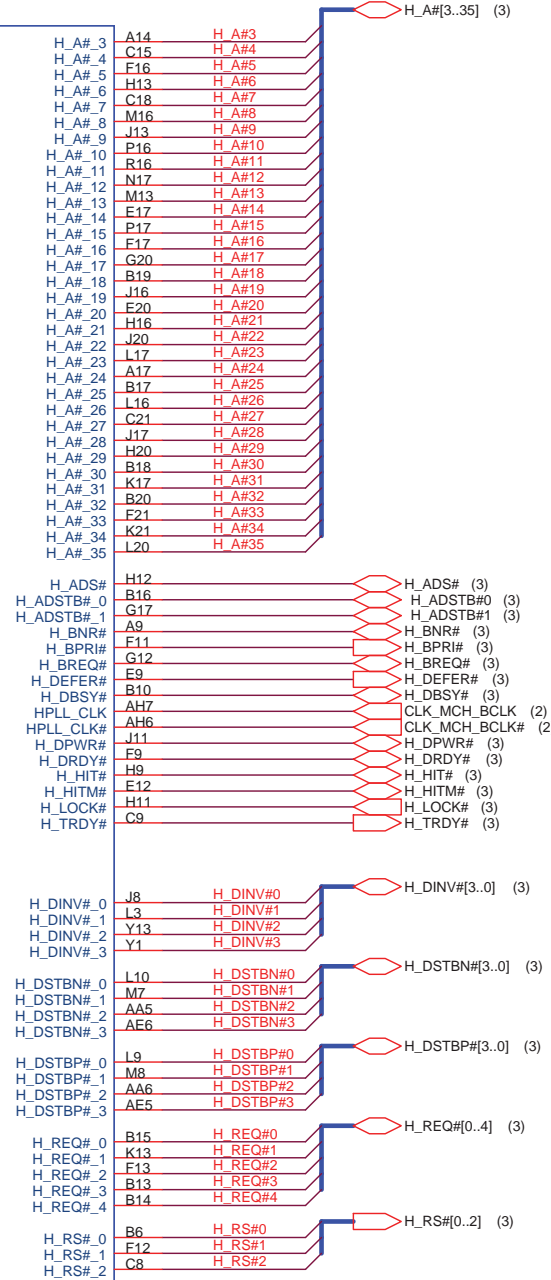
0.3125*VCCP
WIDE(10):SPACING(20),
L<0.5"



Layout Note:
WIDE(10):SPACING(20),
L<0.5"




HOST



GMCH (CANTIGA)

<http://laptop-motherboard-schematic.blogspot.com/>



Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
		3B

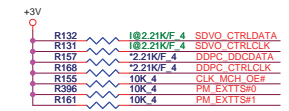
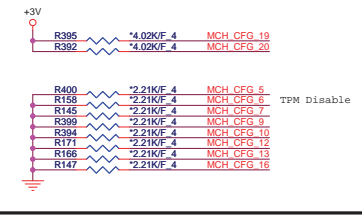
GMCH HOST

Date: Friday, June 27, 2008 Sheet 5 of 39

Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) or PCIe is operational (Default) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

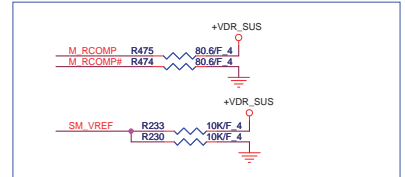
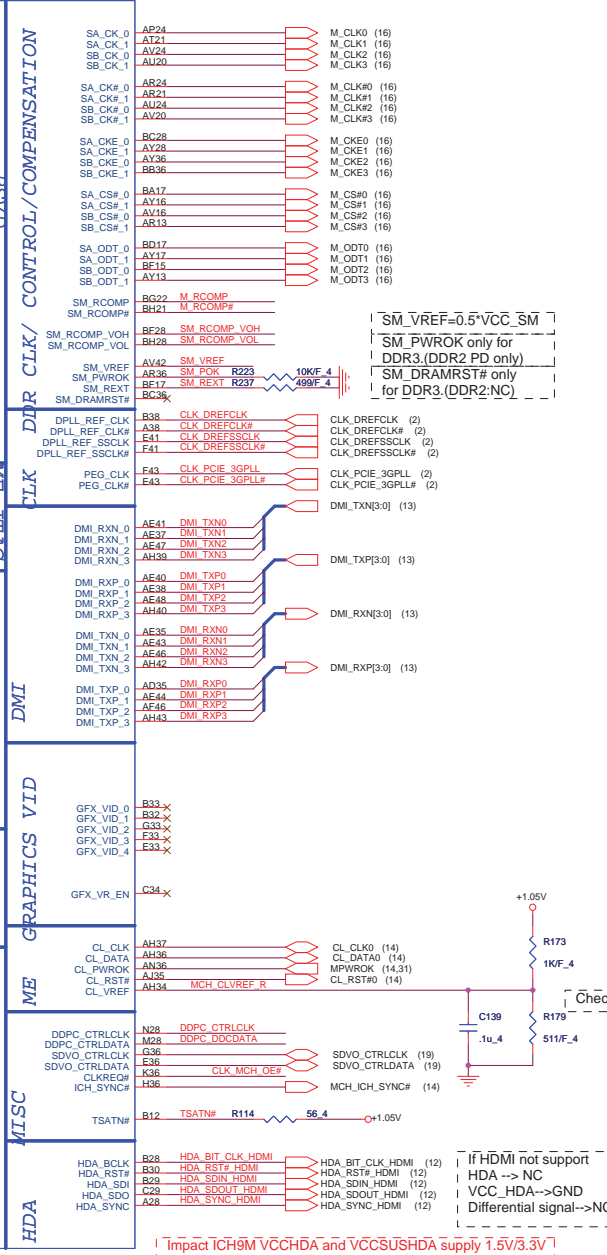
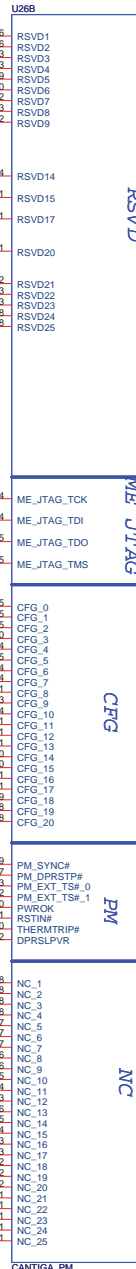
Strap pin



<http://laptop-motherboard-schematic.blogspot.com/>

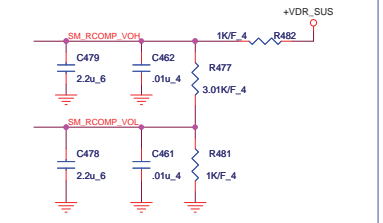
NB Thermal trip pin
No use Thermal trip NB side can NC, (NB has ODT)

PM DPRSTP#
The daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.

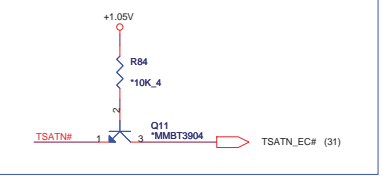


SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K.But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



Check list note : CL_VREF=0.35V

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.
VCC_HDA-->GND
Differential signal-->NC

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V
NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

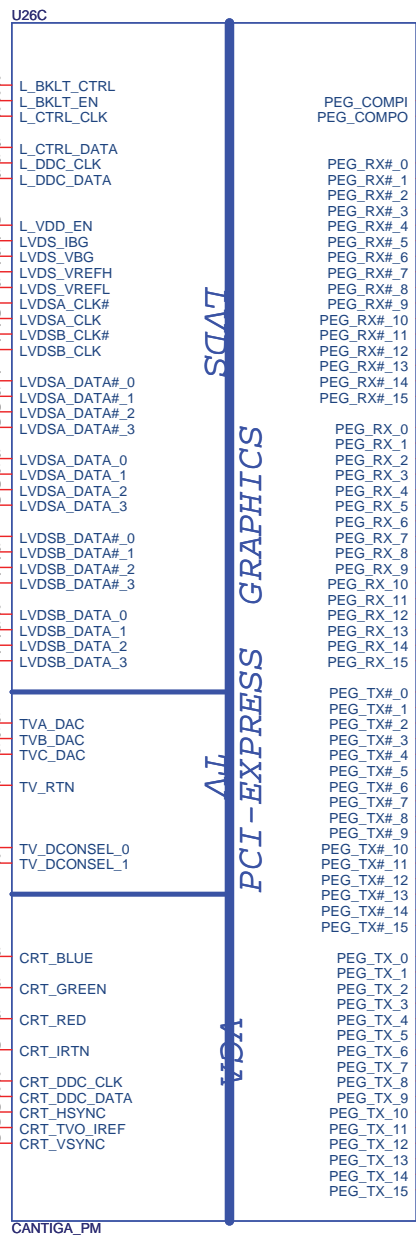
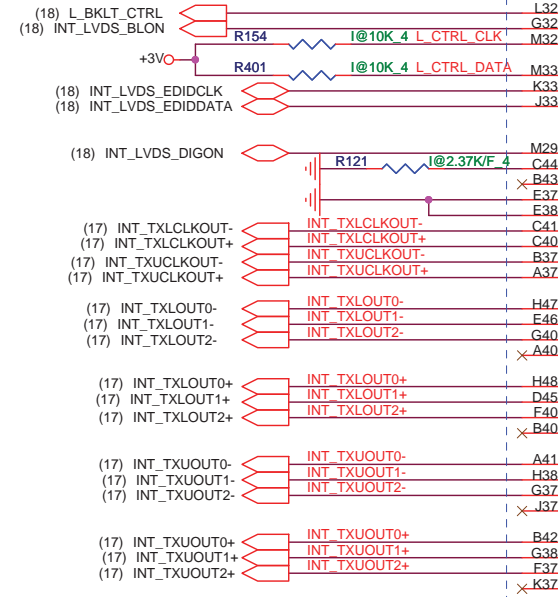
Quanta Computer Inc.
PROJECT : ZK2
GMCH DMI

Size	Document Number	Rev
		8B

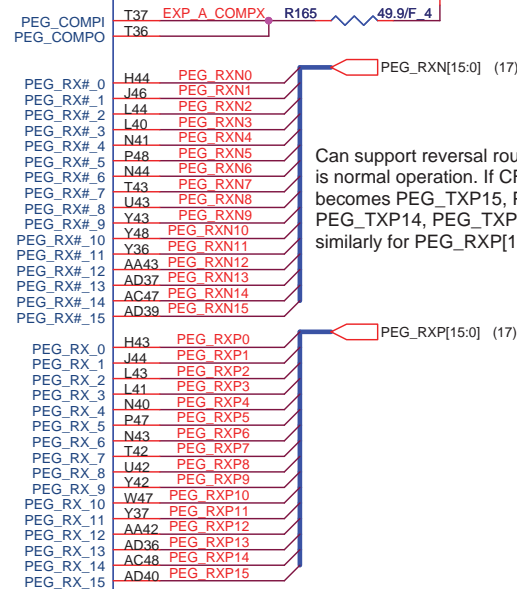
Date: Friday, June 27, 2008 Sheet 6 of 39

IV@
EV@
SP@

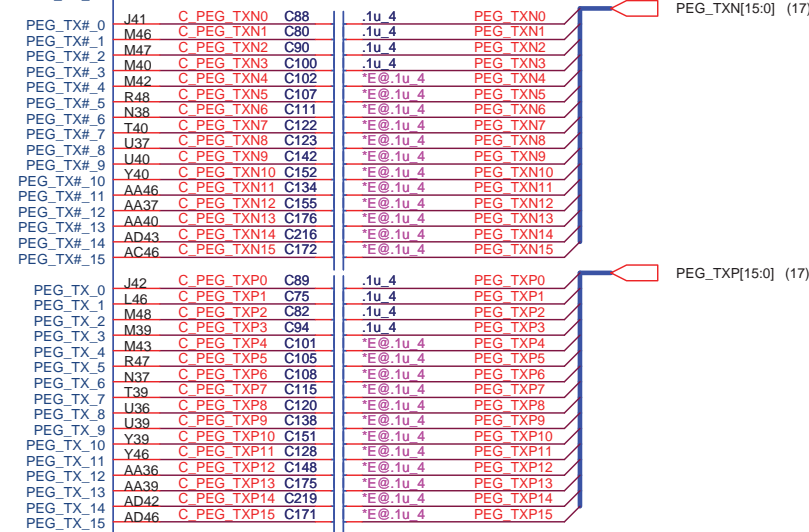
IV&EV Dis/Enable setting
If LVDS no use, all signal can NC



L<0.5", If PCIE not support still connect to +VCC_PEG



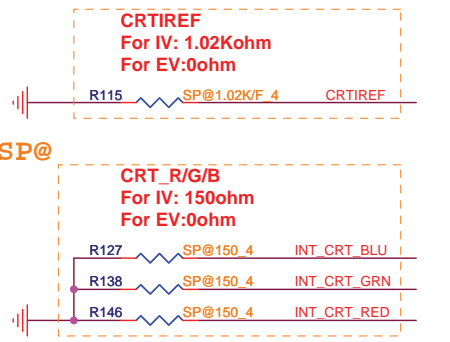
Can support reversal routing. If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]



IV&EV Dis/Enable setting
 <5/31>Montevina_Schematics_Checklist_Rev0_8
 a) For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC. What is correct.
 b) For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC these signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

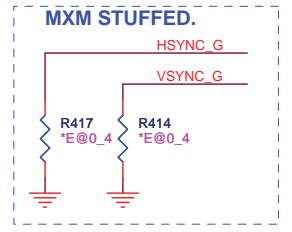
<check list>
 For EV@
 CRT R/G/B 0ohm to GND
 CRTIREF 0ohm to GND

<check list>
 For IV@
 CRT R/G/B 150ohm to GND
 CRTIREF 1.02kOhm to GND

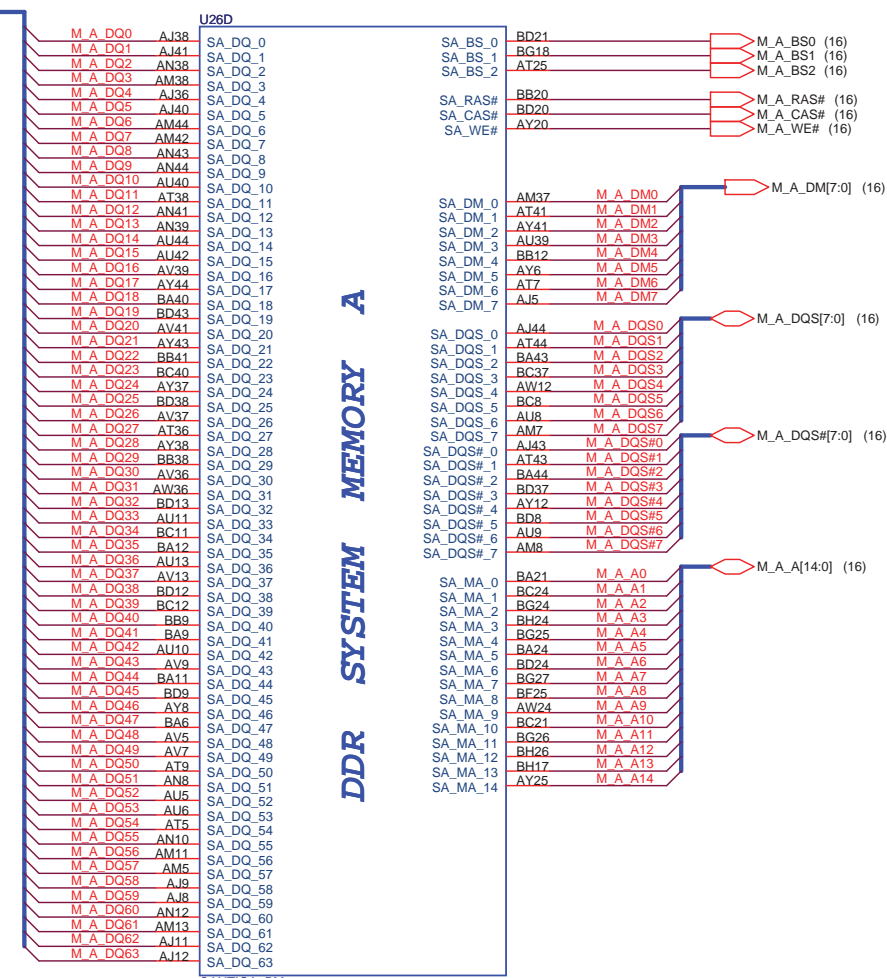


HSYNC/VSYNC serial R place close to NB

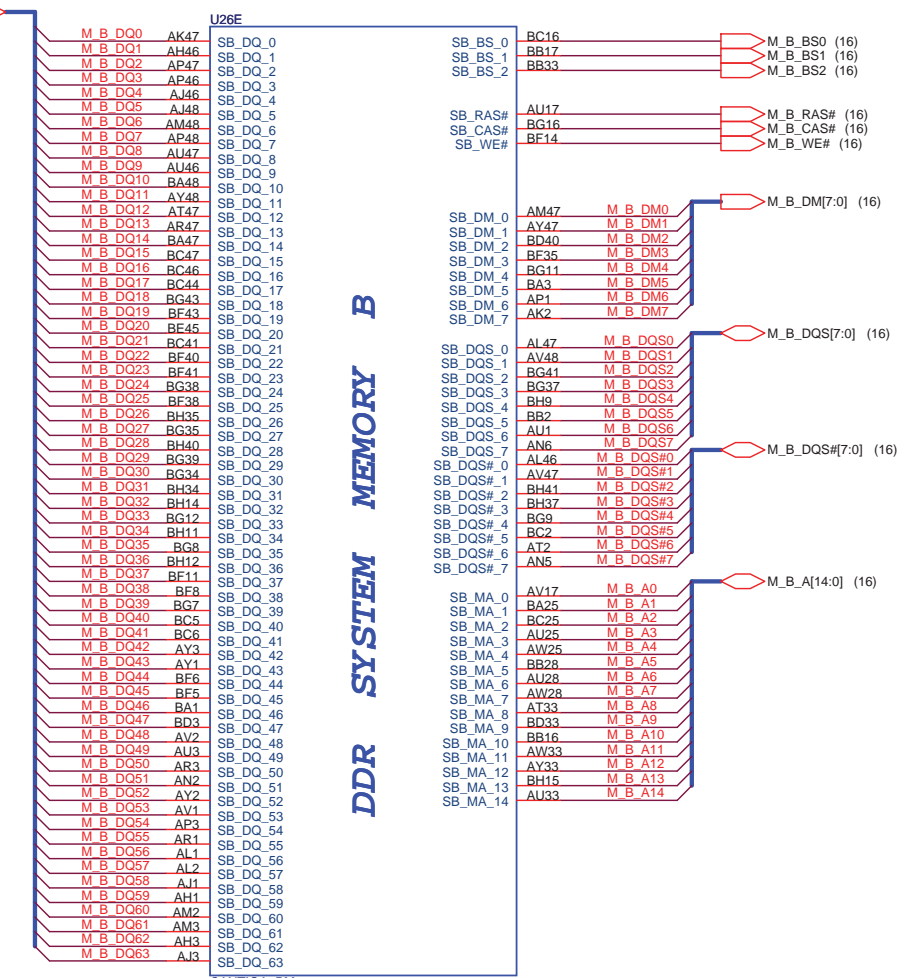
CRTIREF pull down for IV cantiga 1.02k ohm/F



(16) M_A_DQ[63:0]



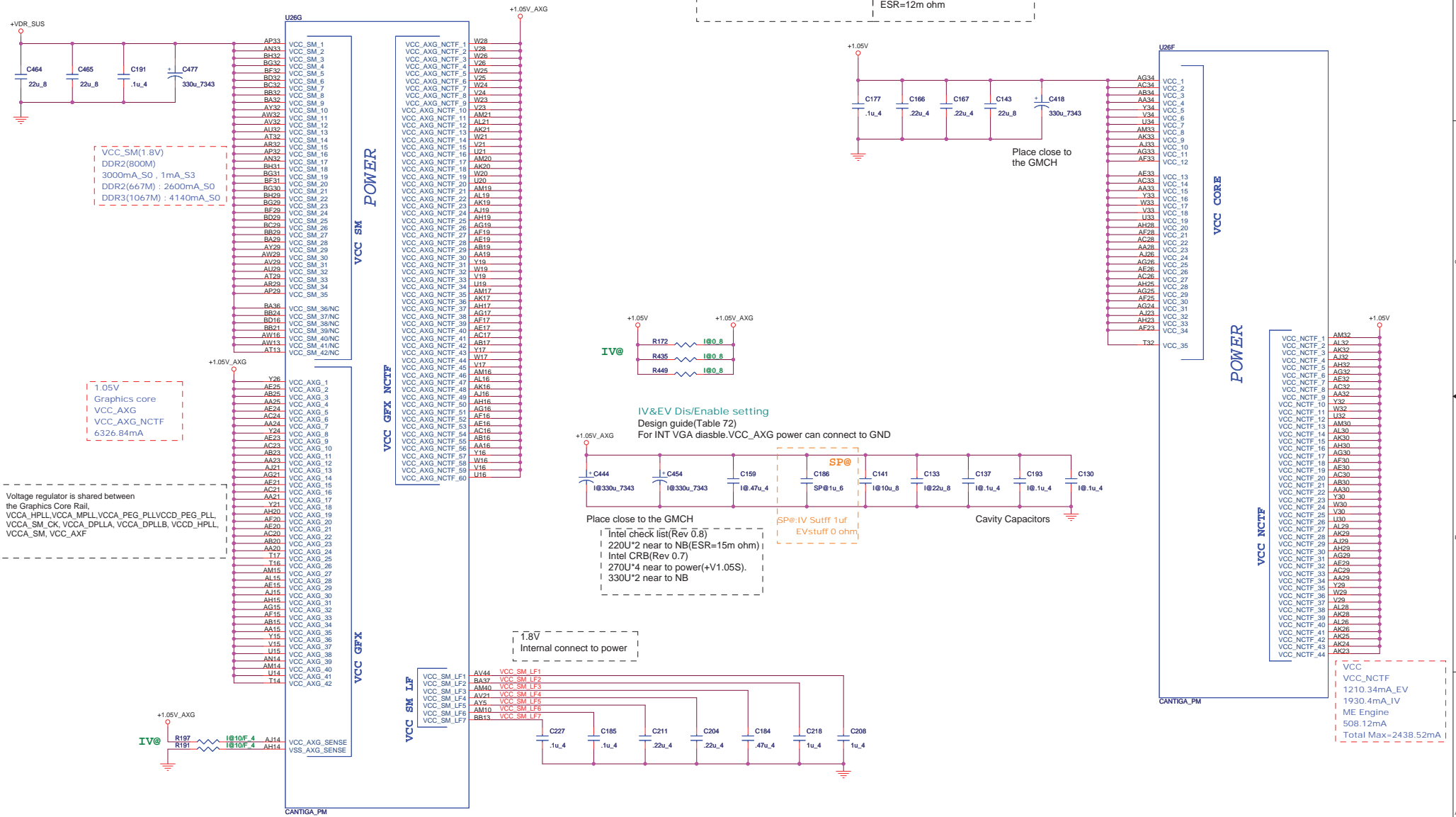
(16) M_B_DQ[63:0]



Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10
GM TDP 10.5-12W
GS TDP 7-8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm



Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL, VCCA_MPLL, VCCA_PEG, PLLVCCD_PEG_PLL, VCCA_SM, CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

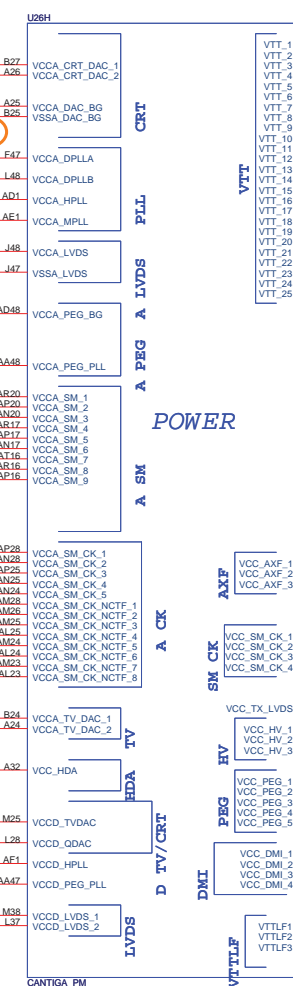
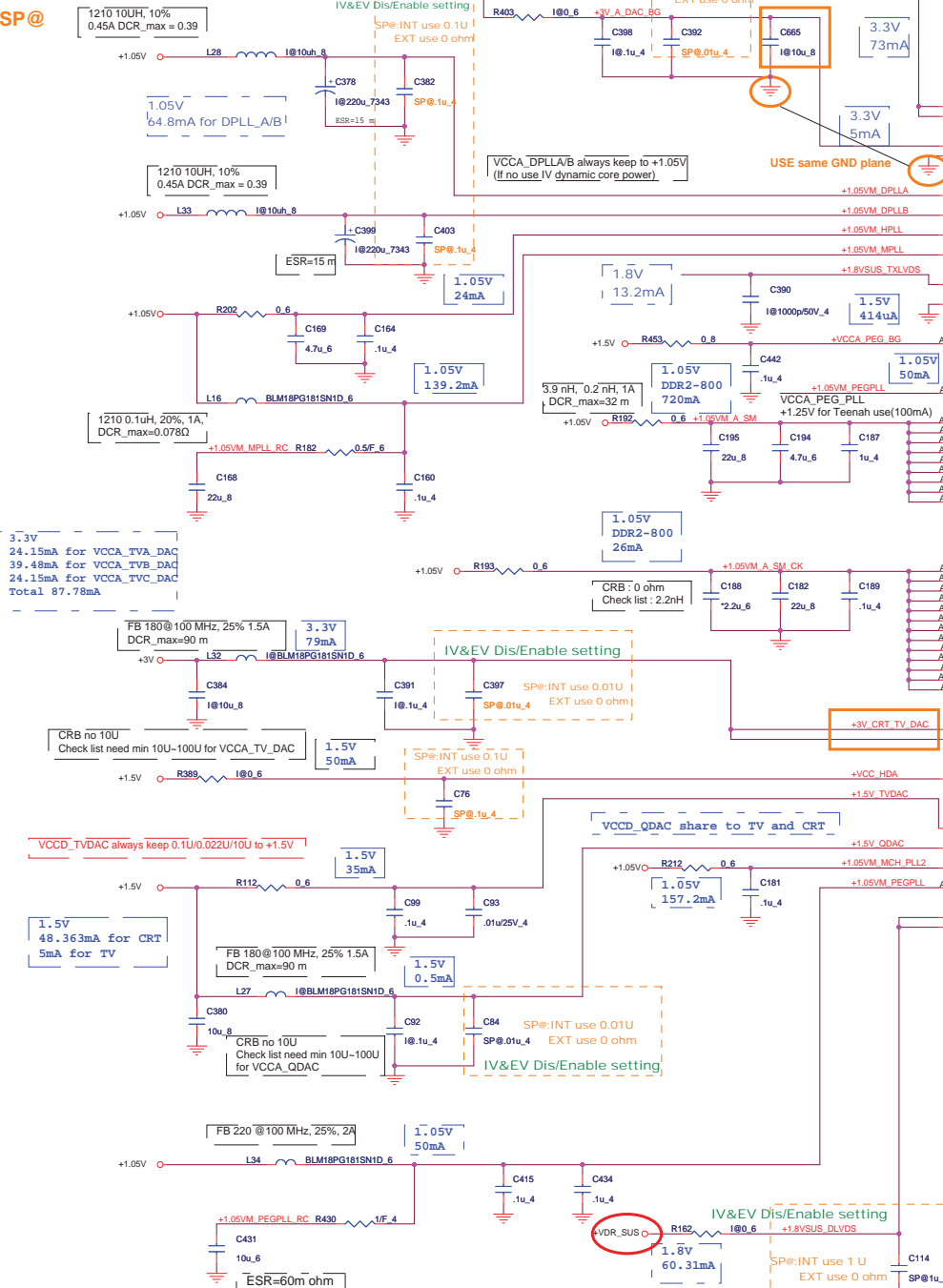
1. Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially
2. VCC_AGX_SENSE PU to +V_GFX_CORE_INT with 10ohm and VSS_AGX_SENSE PD with 10ohm for Intel suggest

Quanta Computer Inc.
PROJECT : ZK2
GMCH VCC,NCTF

Size	Document Number	Rev
		38
Date: Friday, June 27, 2008	Sheet 8 of 39	

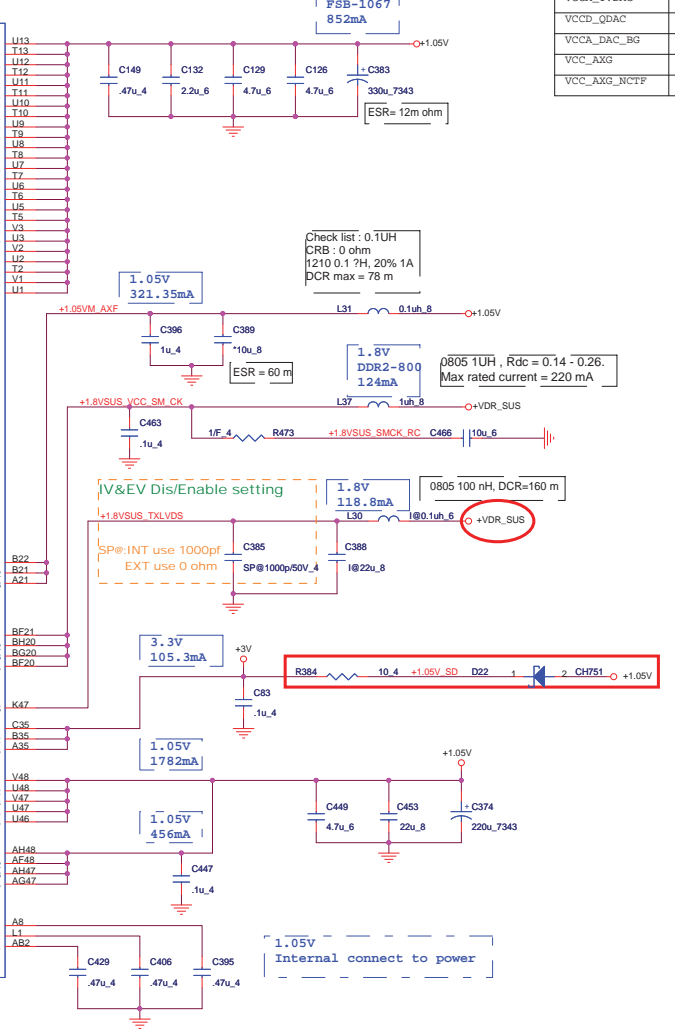
VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTIF	GND

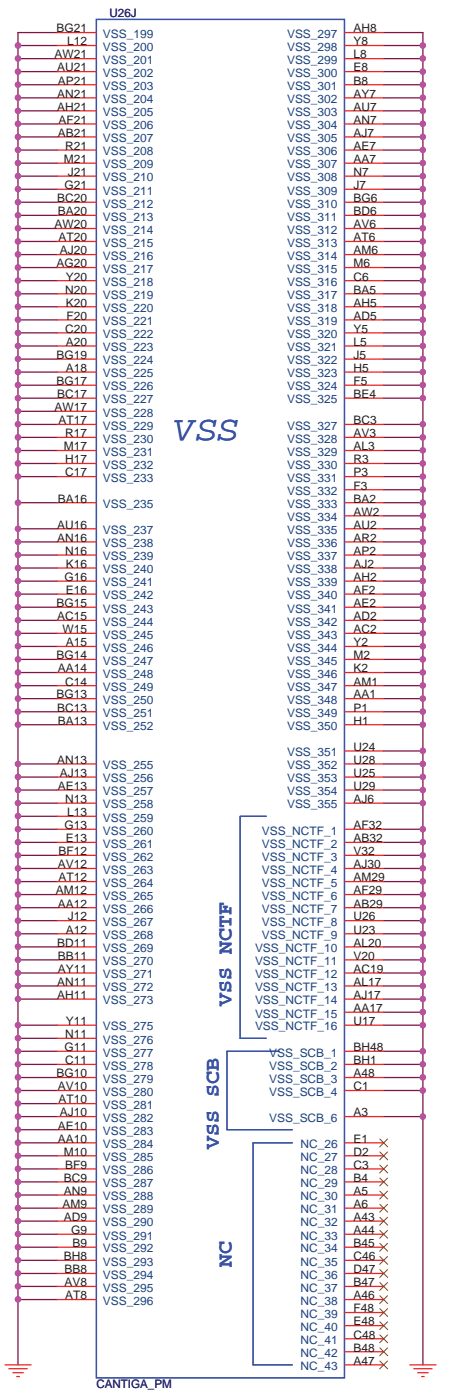
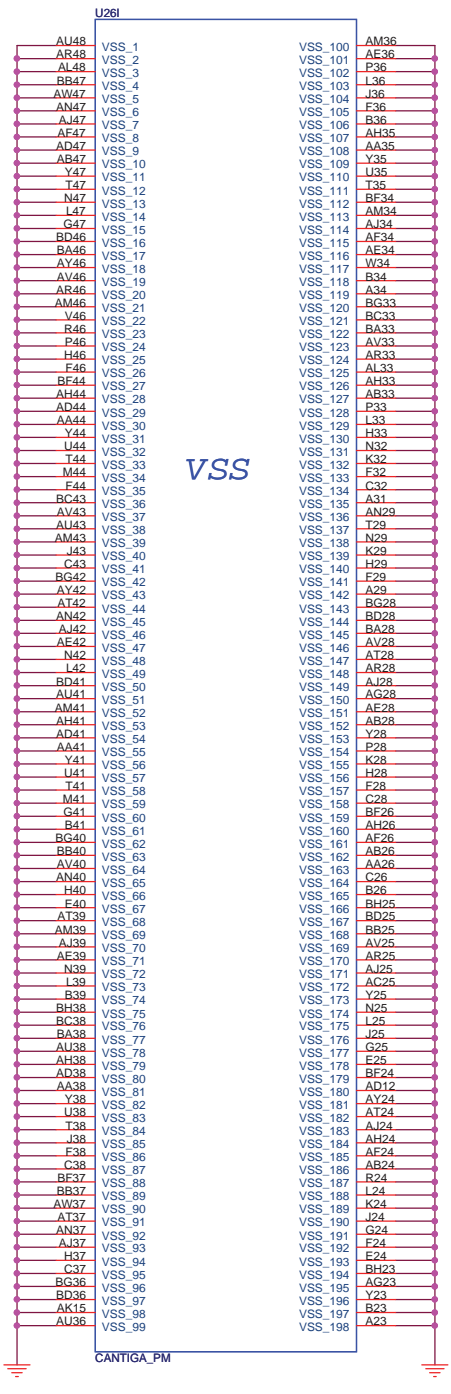
IV@
EV@
SP@

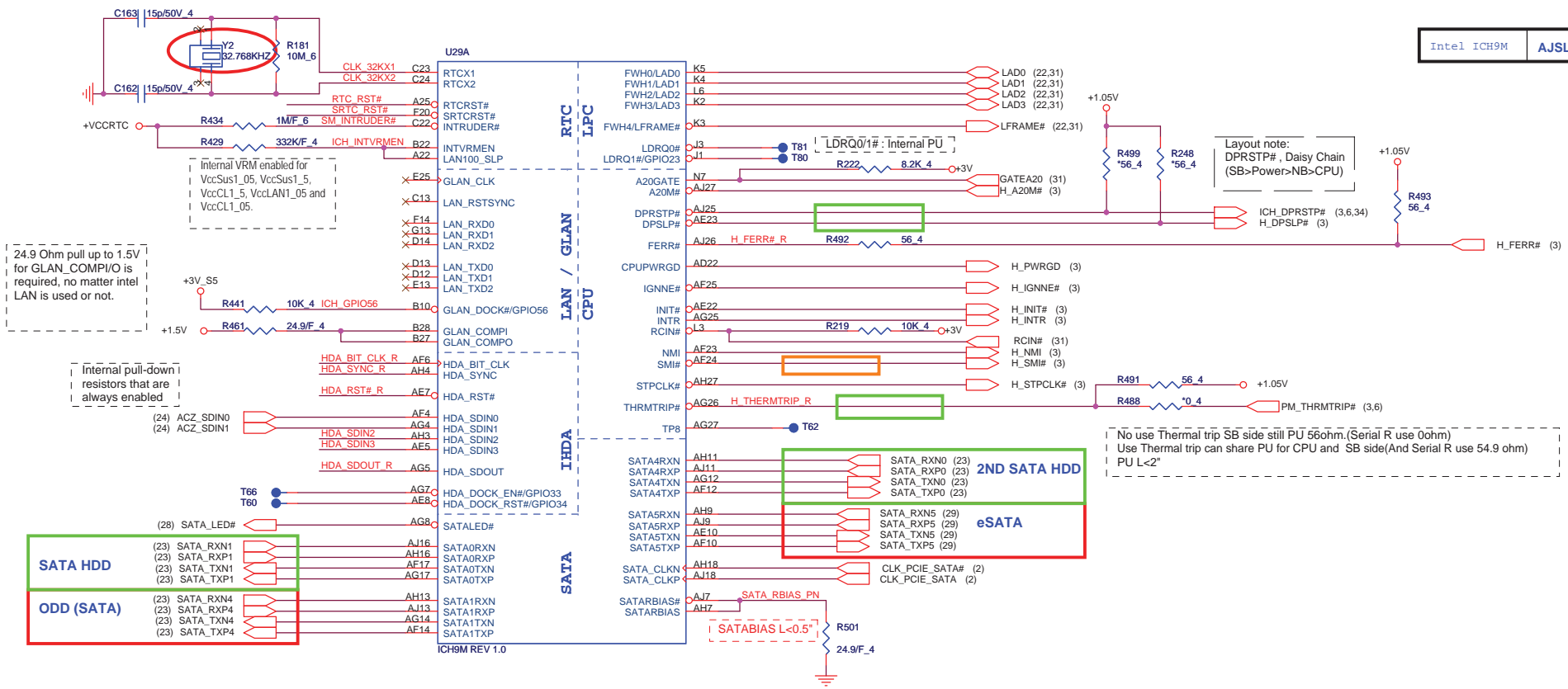


POWER

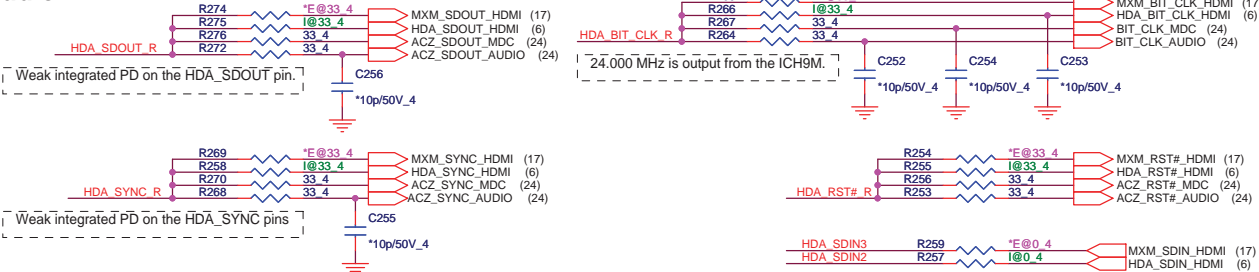
Power Net Name	Cantiga (V)
VCC_AXG_#	1.05V
VCC_AXG_NCTIF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PL	1.05V
VCC_AXF_#	1.05V
VCCD_HPPLL	1.05V
VCCD_PEG_PL	1.05V



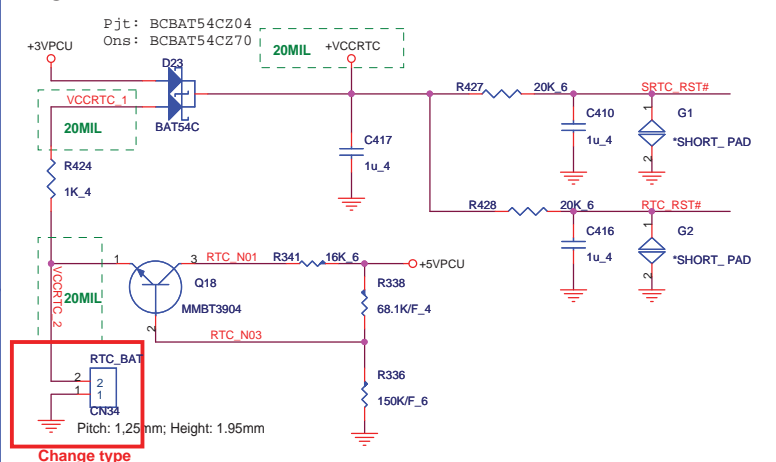




HD Audio



RTC



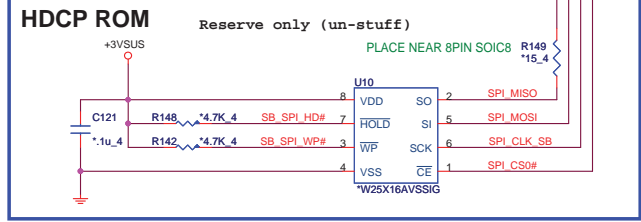
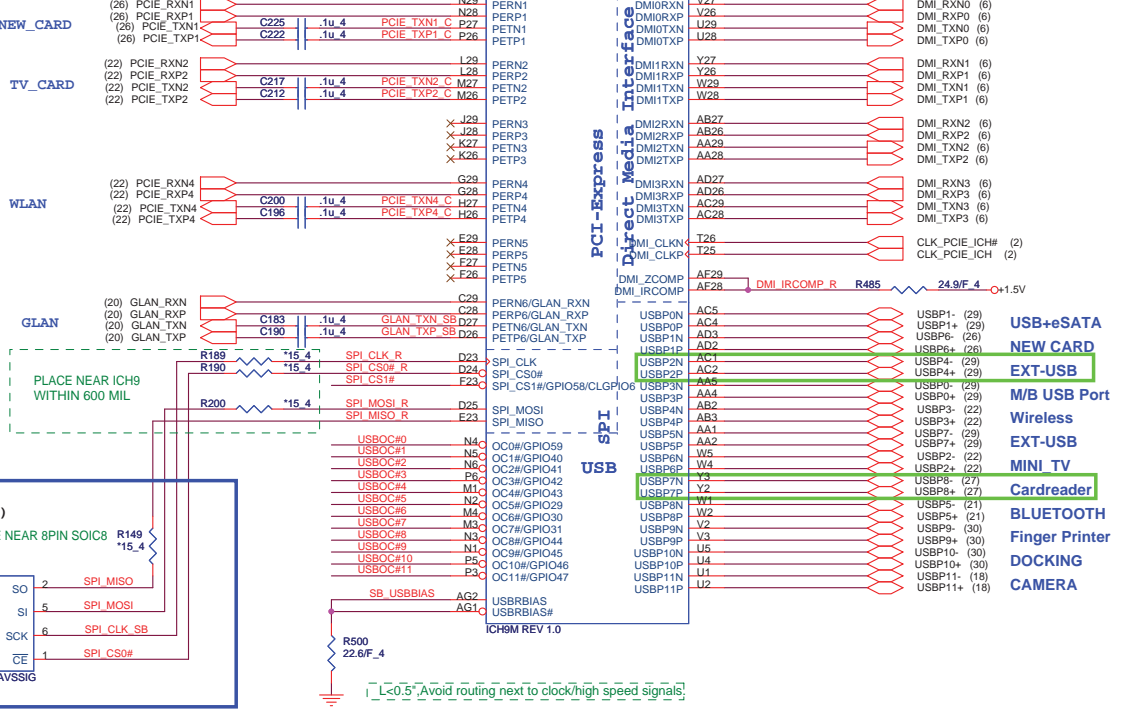
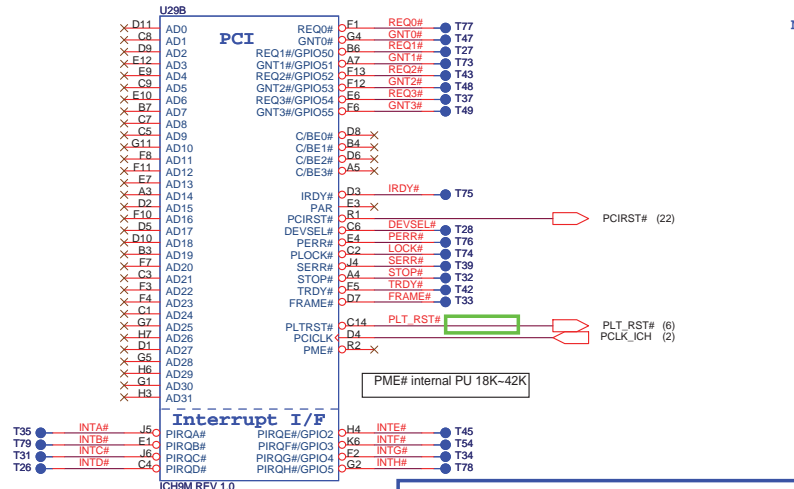
South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD	
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.	
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUR	Description
			0	0	RSVD
			0	1	Enter XOR Chain
HDA_SDOUR	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	1	0	Normal operation(Default)
			1	1	Set PCIe port config bit 1

Quanta Computer Inc.
PROJECT : ZK2

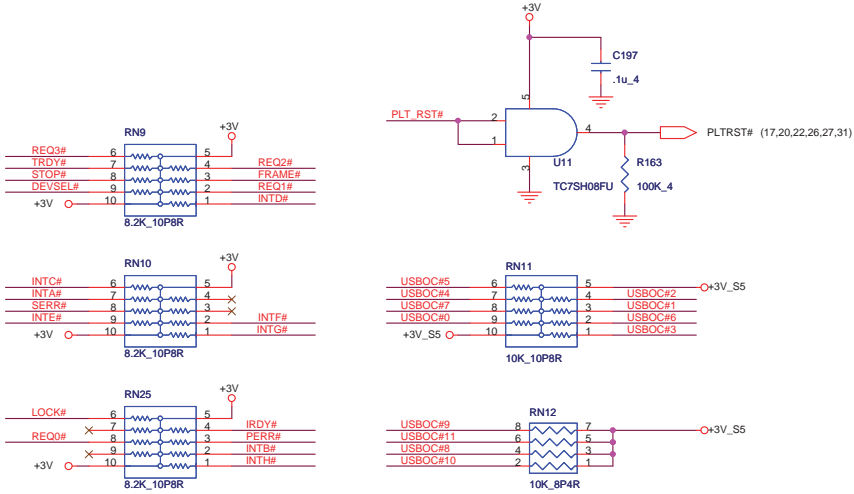
Size Document Number ICH9M HOST Rev 3B

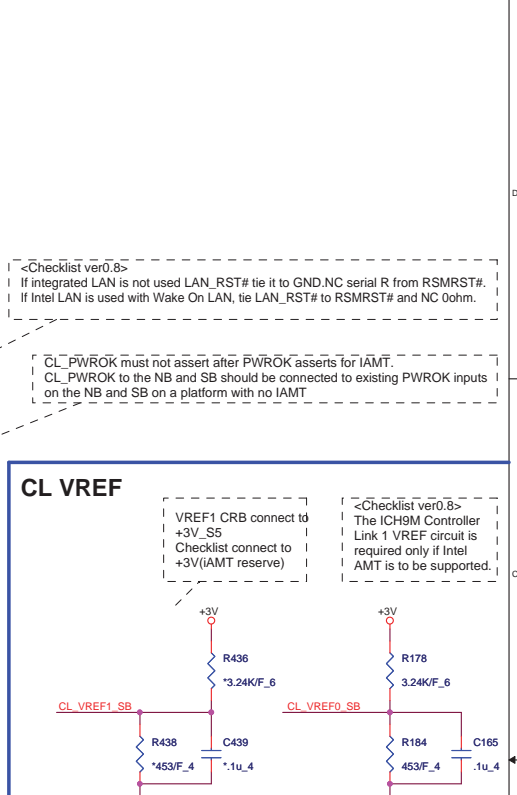
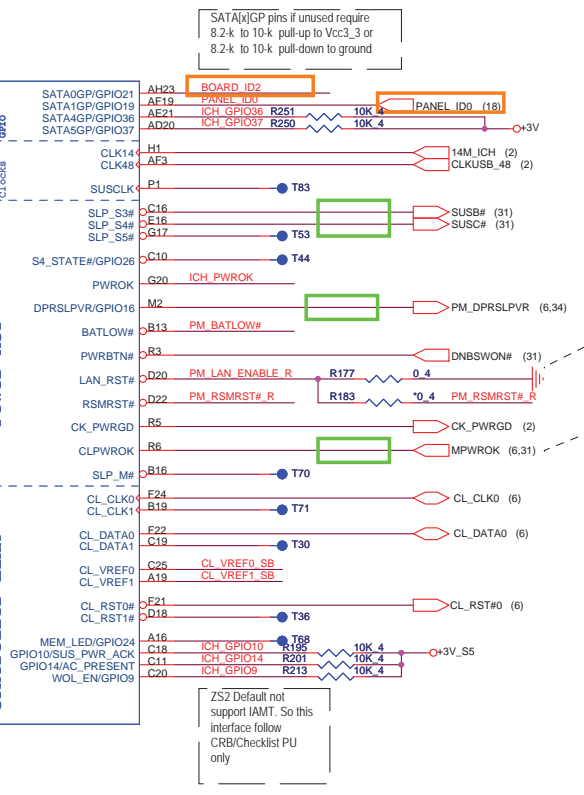
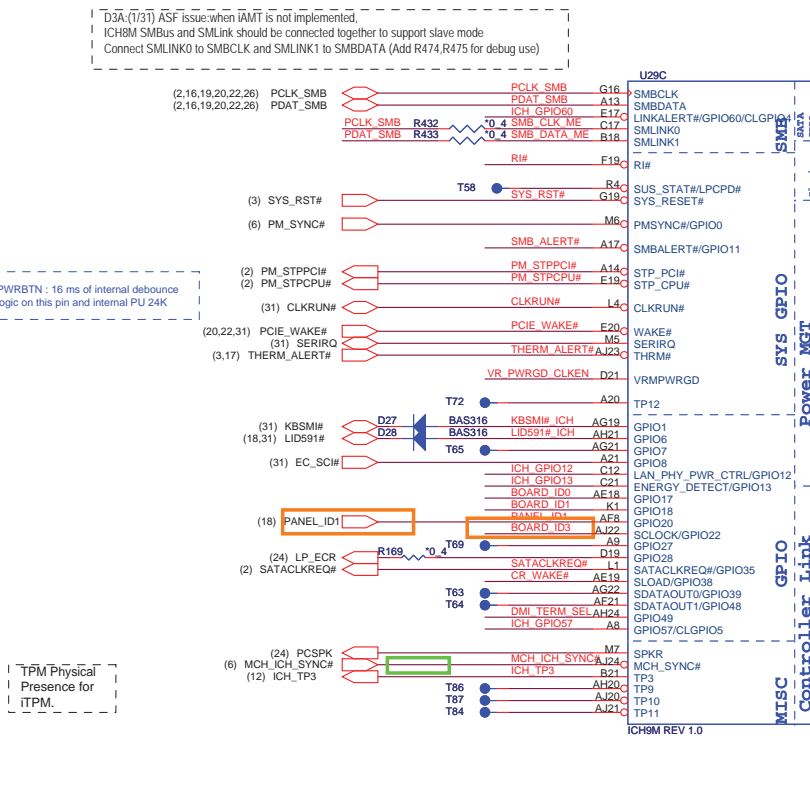
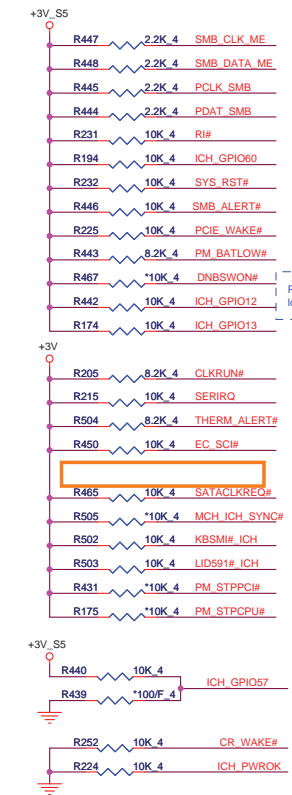
Date: Wednesday, July 09, 2008 Sheet 12 of 39



South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default										
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R204 *1K 4									
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R199 *10K 4 +3V_S5									
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>0</td> <td>1</td> <td>SPI</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI	GNT0# R221 *1K 4			
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI											
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC(Default)</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	1	0	PCI	1	1	LPC(Default)	SPI_CS1# R216 *1K 4
PCI_GNT#0	SPI_CS#1	Boot Location											
1	0	PCI											
1	1	LPC(Default)											





Panel ID (UMA only)

Close to LCD connector (CN3)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

ICH PWROK

DELAY_VR_PWRGOOD need PU 2K to +3V.
ZS2 PU at power side

Resume RST

ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teناه(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R236 *1K 4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R507 *1K 4

CLK Enable

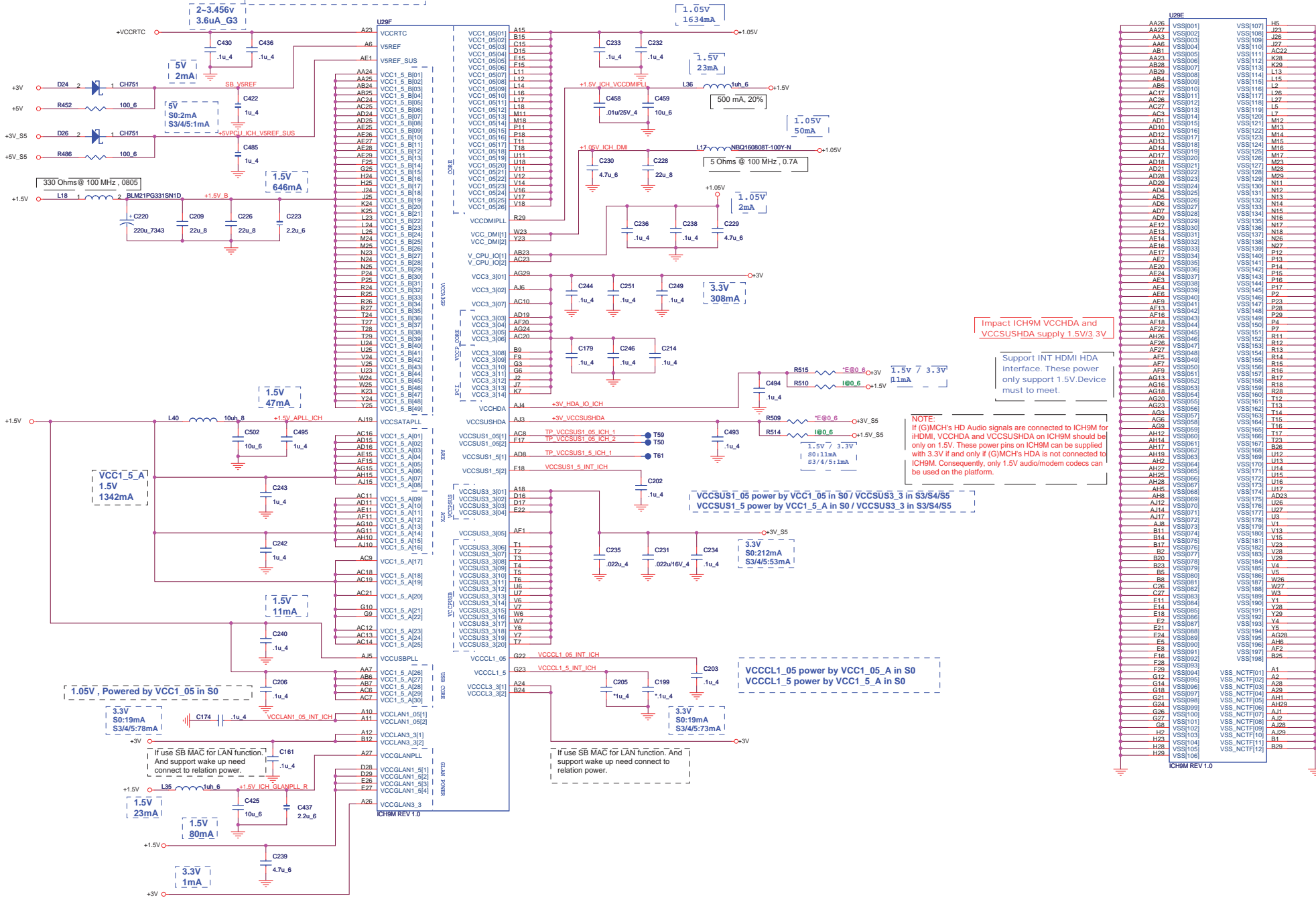
(34) VR_PWRGD_CK410#

Quanta Computer Inc.
PROJECT : ZK2

Size: Document Number: ICH9M GPIO Rev: 3B
Date: Friday, June 27, 2008 Sheet: 14 of 39

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION:
CHANGE TO 100OHM & 1UF



Impact ICH9M VCCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA Interface. These power only support 1.5V Device must to meet.

NOTE: If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

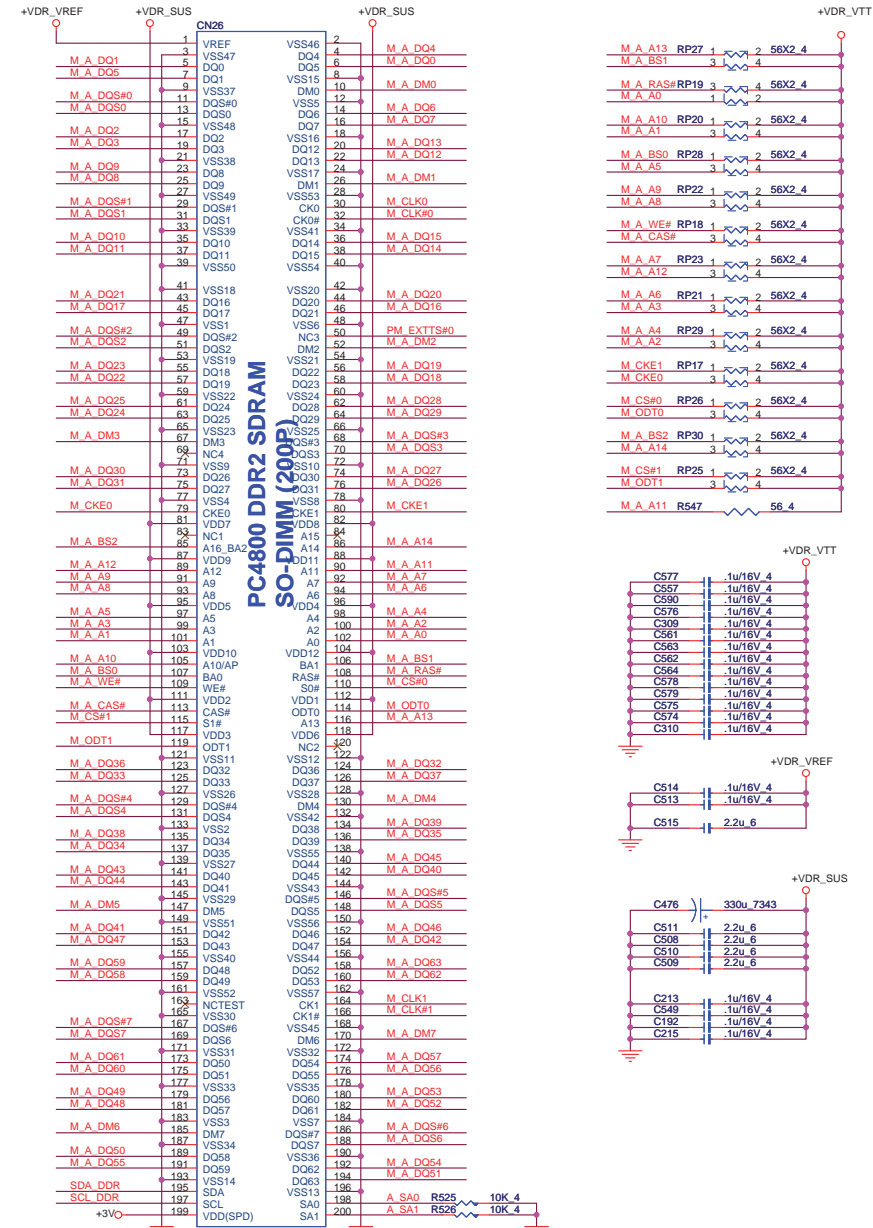
VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

If use SB MAC for LAN function, And support wake up need connect to relation power.

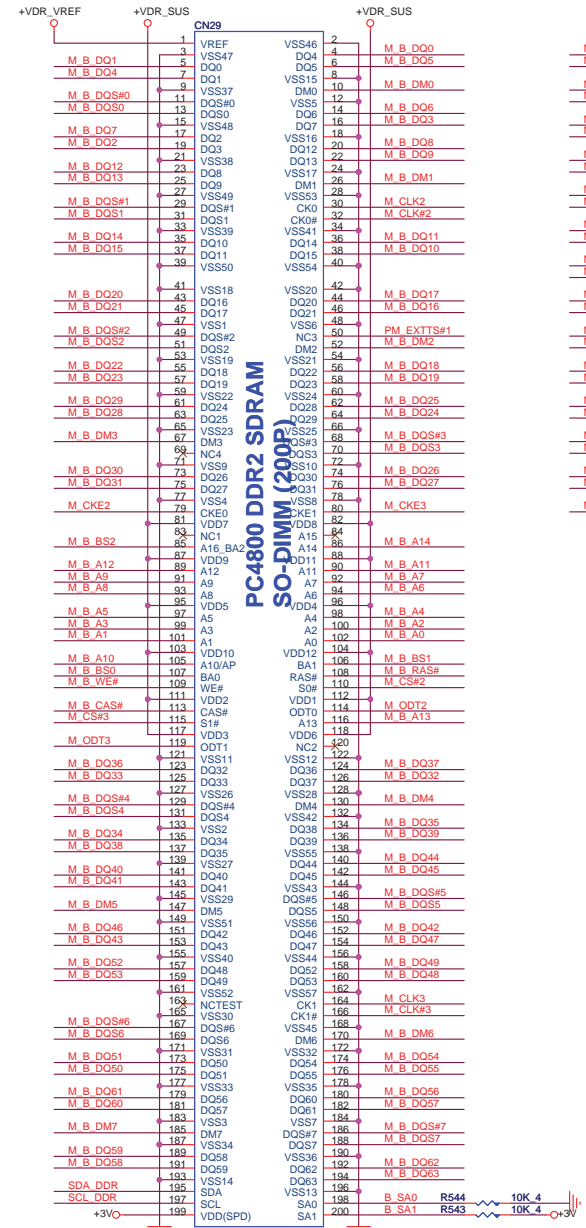
U29E	U29E	U29E
AA26	VSS001	VSS107
AA27	VSS002	VSS108
AA3	VSS003	VSS109
AA6	VSS004	VSS110
D15	VSS005	VSS111
AA23	VSS006	VSS112
AB23	VSS007	VSS113
AB24	VSS008	VSS114
AB25	VSS009	VSS115
AB4	VSS010	VSS116
AB5	VSS011	VSS117
AC17	VSS012	VSS118
AC26	VSS013	VSS119
AC27	VSS014	VSS120
AD1	VSS015	VSS121
AD10	VSS016	VSS122
AD11	VSS017	VSS123
AD12	VSS018	VSS124
AD13	VSS019	VSS125
AD14	VSS020	VSS126
AD17	VSS021	VSS127
AD21	VSS022	VSS128
AD28	VSS023	VSS129
AD29	VSS024	VSS130
AD3	VSS025	VSS131
AD5	VSS026	VSS132
AD6	VSS027	VSS133
AD7	VSS028	VSS134
AD8	VSS029	VSS135
AE12	VSS030	VSS136
AE13	VSS031	VSS137
AE14	VSS032	VSS138
AE16	VSS033	VSS139
AE17	VSS034	VSS140
AE20	VSS035	VSS141
AE24	VSS036	VSS142
AE3	VSS037	VSS143
AE4	VSS038	VSS144
AE6	VSS039	VSS145
AE8	VSS040	VSS146
AE9	VSS041	VSS147
AE10	VSS042	VSS148
AE11	VSS043	VSS149
AE12	VSS044	VSS150
AE13	VSS045	VSS151
AE14	VSS046	VSS152
AE15	VSS047	VSS153
AE16	VSS048	VSS154
AE17	VSS049	VSS155
AE7	VSS050	VSS156
AG3	VSS051	VSS157
AG13	VSS052	VSS158
AG16	VSS053	VSS159
AG18	VSS054	VSS160
AG20	VSS055	VSS161
AG23	VSS056	VSS162
AG24	VSS057	VSS163
AG6	VSS058	VSS164
AG9	VSS059	VSS165
AH12	VSS060	VSS166
AH14	VSS061	VSS167
AH17	VSS062	VSS168
AH19	VSS063	VSS169
AH2	VSS064	VSS170
AH22	VSS065	VSS171
AH23	VSS066	VSS172
AH28	VSS067	VSS173
AH5	VSS068	VSS174
AH6	VSS069	VSS175
AH7	VSS070	VSS176
AH11	VSS071	VSS177
AH14	VSS072	VSS178
AH17	VSS073	VSS179
AH1	VSS074	VSS180
B11	VSS075	VSS181
B12	VSS076	VSS182
B2	VSS077	VSS183
B20	VSS078	VSS184
B23	VSS079	VSS185
B5	VSS080	VSS186
B6	VSS081	VSS187
C26	VSS082	VSS188
C27	VSS083	VSS189
E11	VSS084	VSS190
E12	VSS085	VSS191
E18	VSS086	VSS192
E2	VSS087	VSS193
E24	VSS088	VSS194
E28	VSS089	VSS195
E5	VSS090	VSS196
E8	VSS091	VSS197
F16	VSS092	VSS198
F28	VSS093	VSS199
G12	VSS_NCT00	A1
G13	VSS_NCT01	A2
G14	VSS_NCT02	A3
G16	VSS_NCT03	A4
G18	VSS_NCT04	A5
G21	VSS_NCT05	A6
G22	VSS_NCT06	A7
G24	VSS_NCT07	A8
G26	VSS_NCT08	A9
G8	VSS_NCT09	A10
H2	VSS_NCT10	A11
H23	VSS_NCT11	B1
H28	VSS_NCT12	B2
H29	VSS_NCT13	B3

DDR2 Module



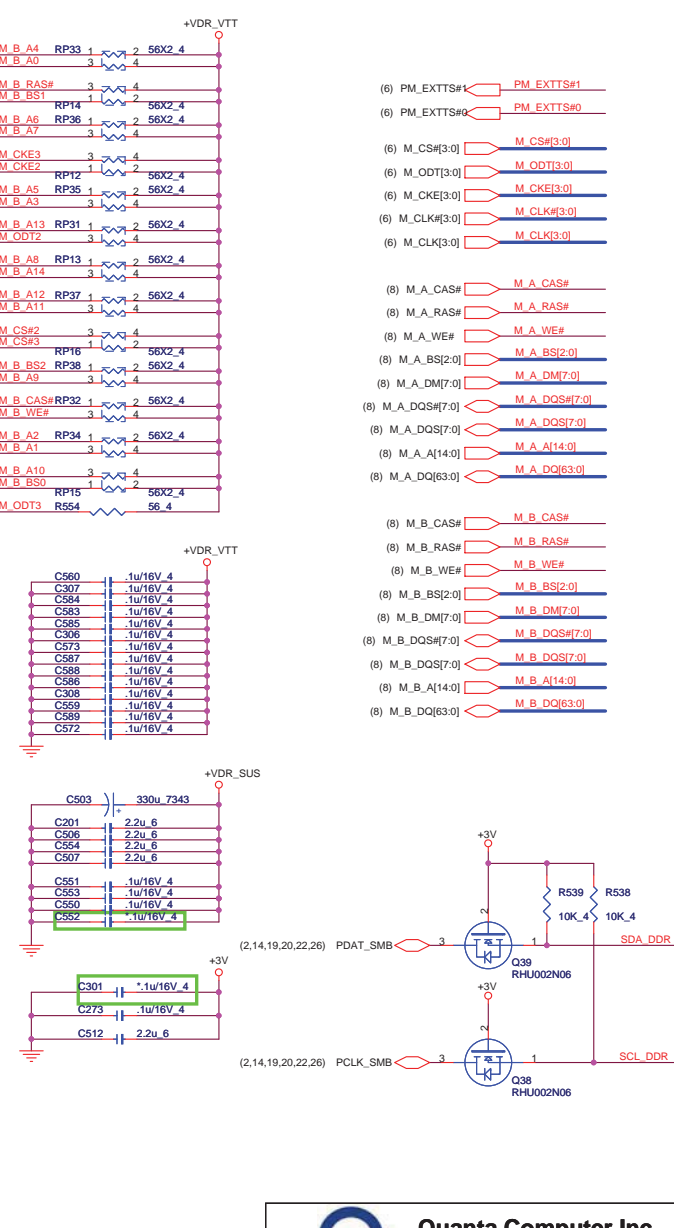
DDR2_DIMM_H9.2_Stand
IN2-Layer
CLOCK 0,1

Smbus address A0
NOTE: Place one cap close to every 2 pull-up resistors terminated to +SMDDR_VTERM



DDR2_DIMM_H5.2_Stand
IN1-Layer
CLOCK 2,3

Smbus address A2



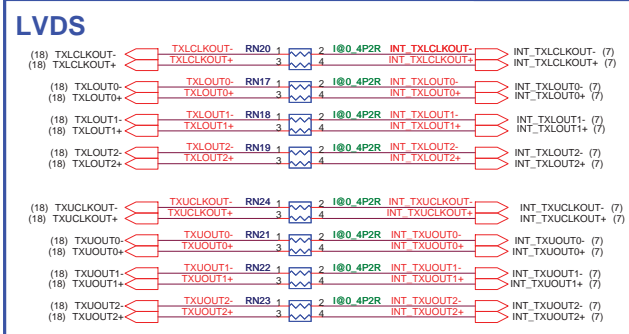
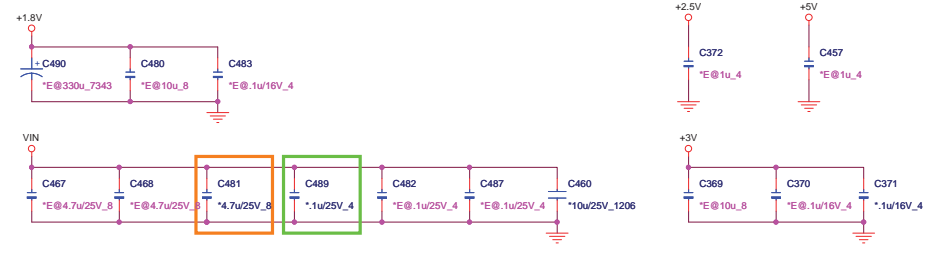
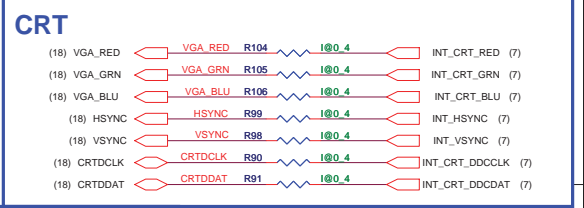
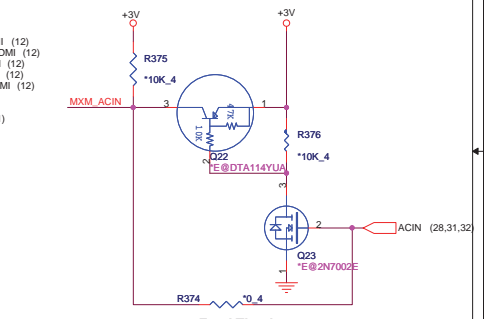
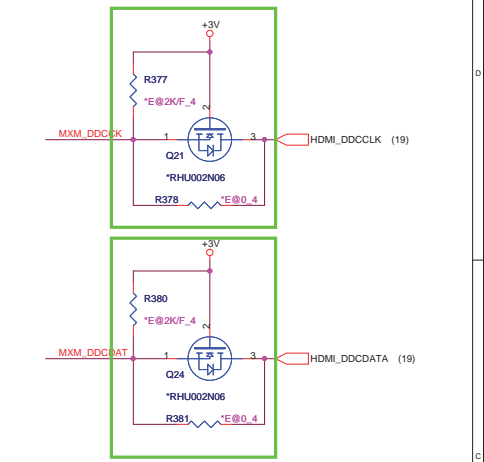
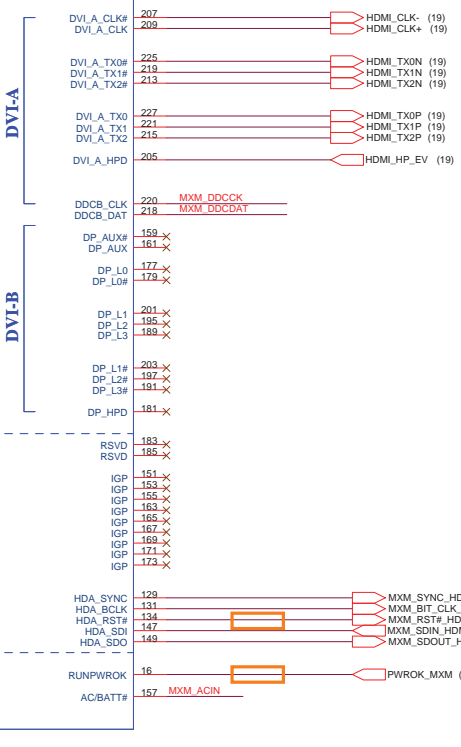
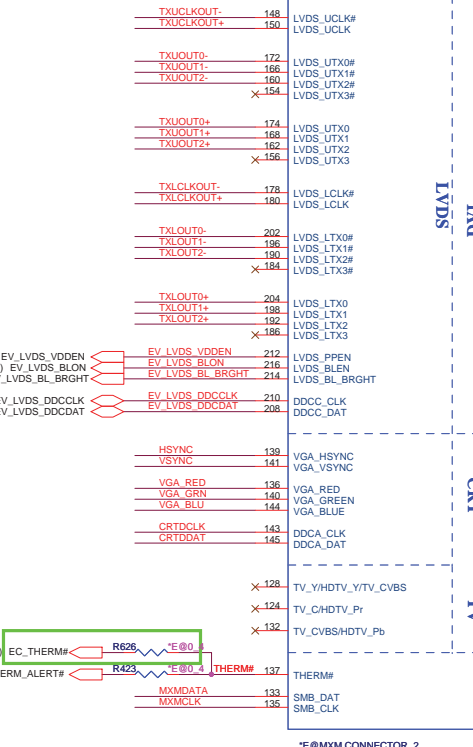
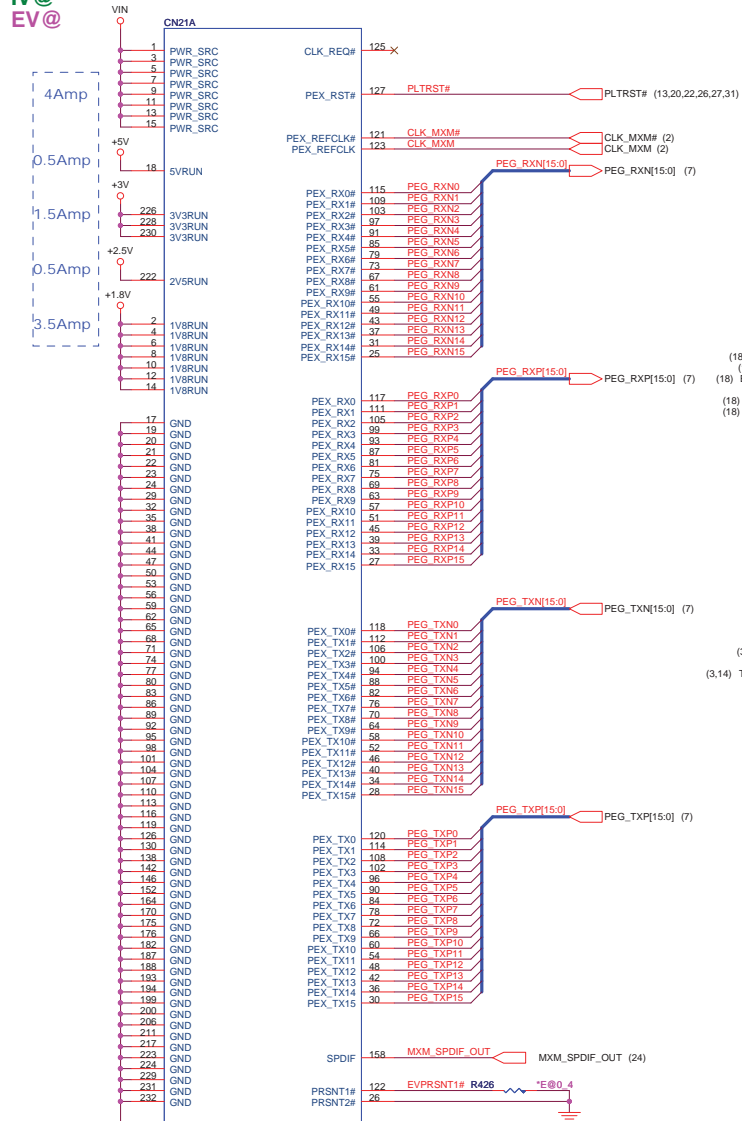
SDA_DDR
SCL_DDR

Quanta Computer Inc.
PROJECT : ZK2
DDRII SO-DIMM

Size	Document Number	Rev
Date: Friday, June 27, 2008	Sheet	16 of 39

MXM Module

IV@
EV@



Quanta Computer Inc.

PROJECT : ZK2

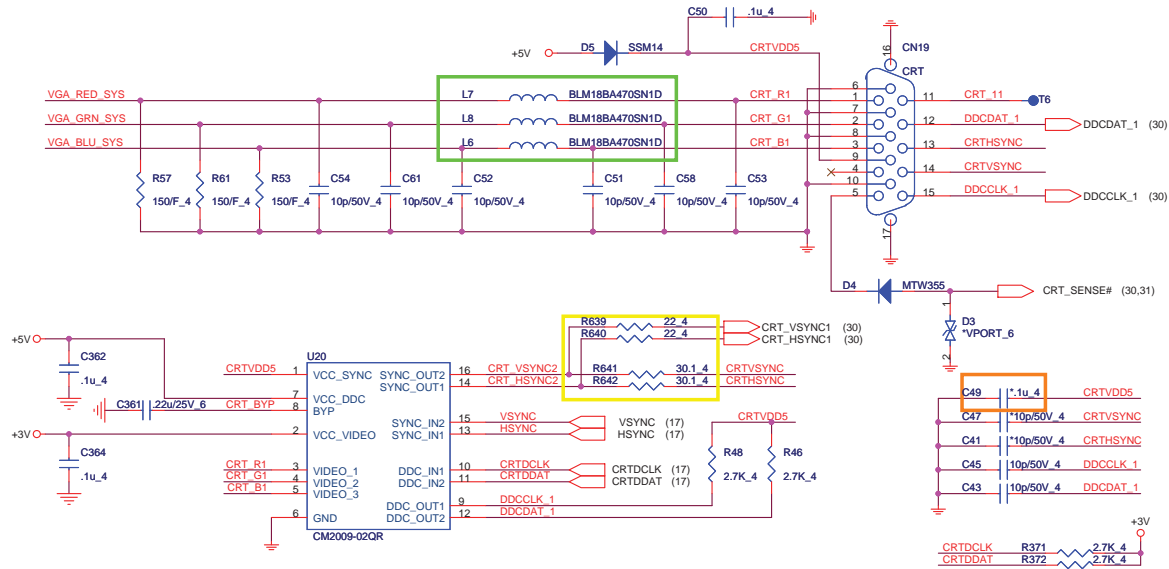
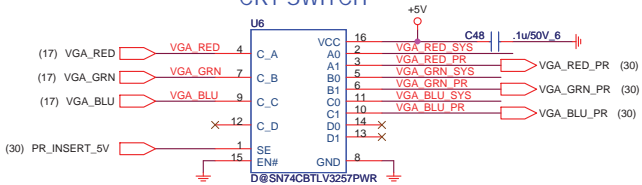
Size Document Number **MXM** Rev 3B

Date: Friday, June 27, 2008 Sheet 17 of 39

CRT

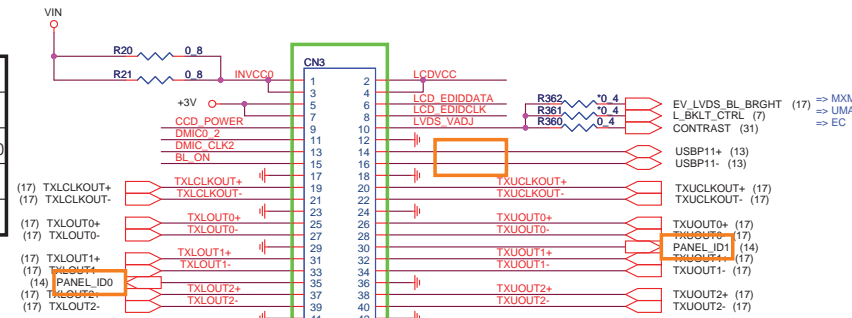
IV@
EV@

CRT SWITCH

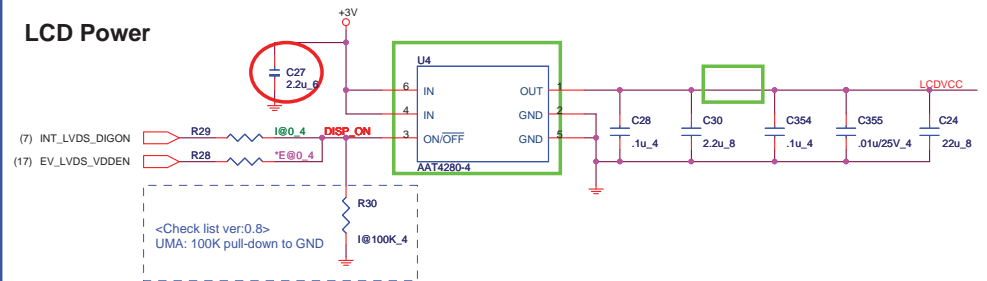


LVDS

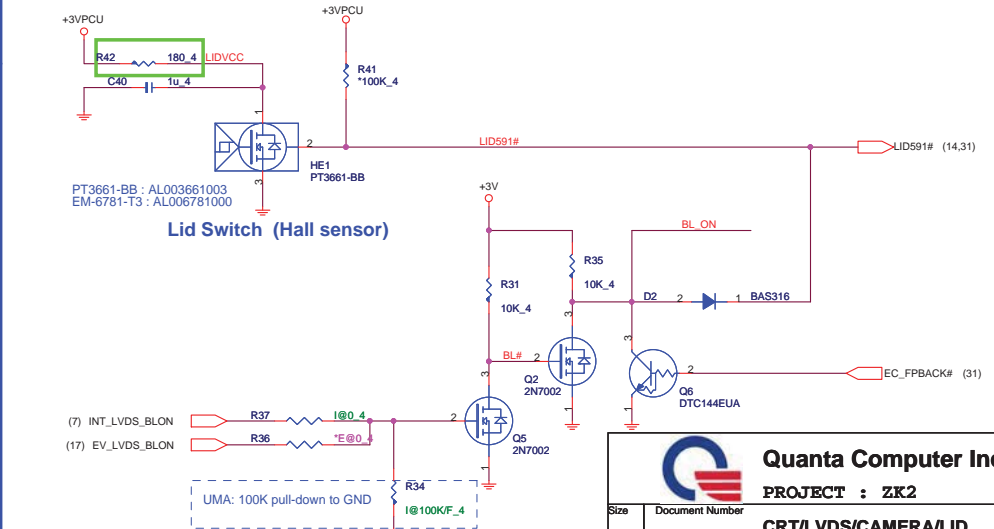
P_ID1	P_ID0	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved



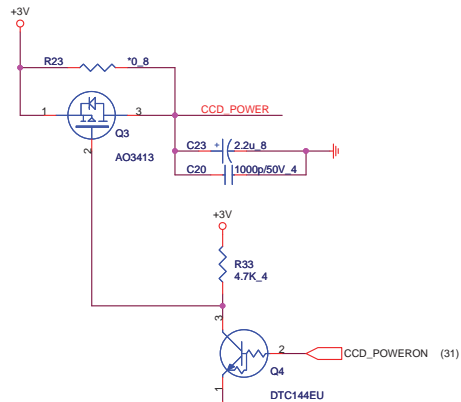
LCD Power



Backlight Control & Lid



CCD

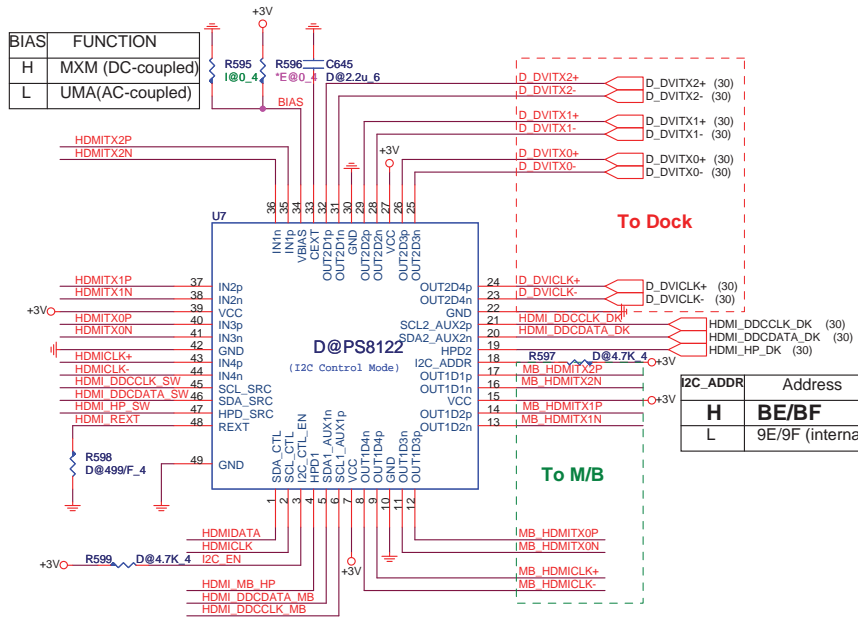


Quanta Computer Inc.
PROJECT : ZK2
CRT/LVDS/CAMERA/LID
Rev 38

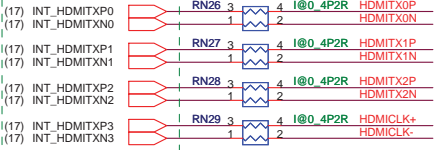
HDMI Switch

IV@
EV@
SP@

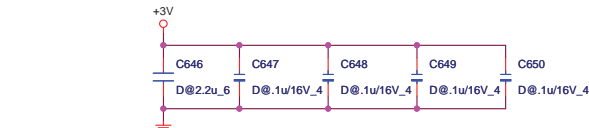
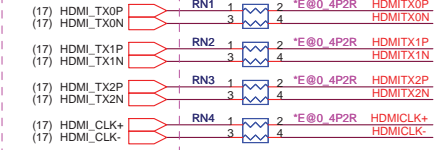
BIAS	FUNCTION
H	MXM (DC-coupled)
L	UMA(AC-coupled)



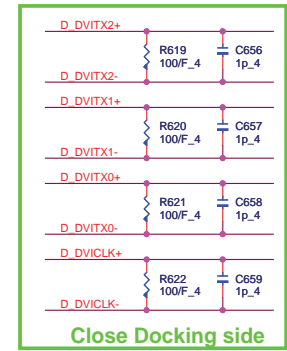
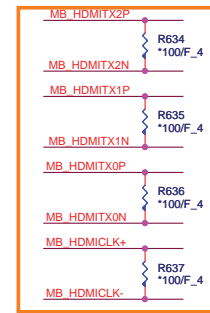
From GMCH



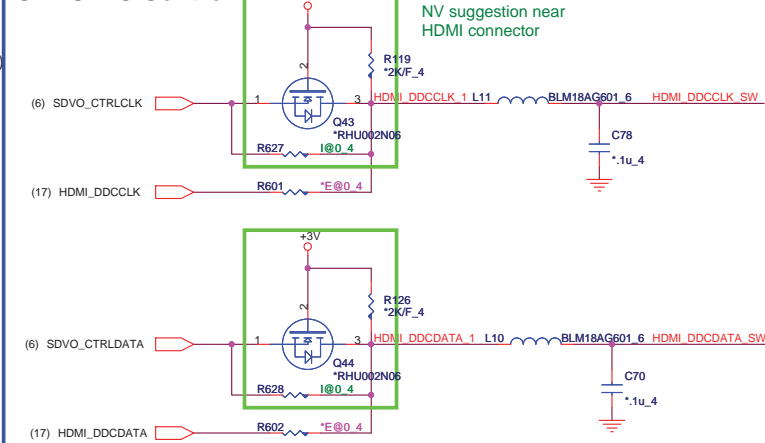
From MXM



EMI reserve

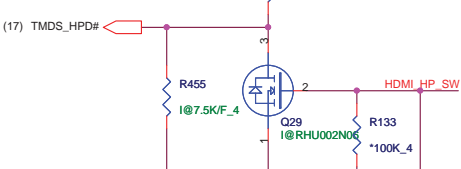


SDVO I2C Control



HP-detect

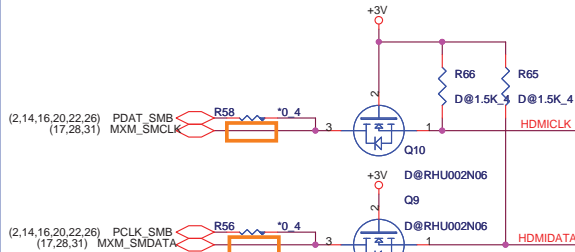
To GMCH



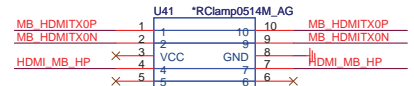
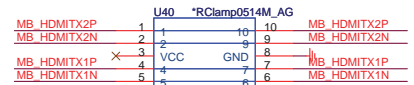
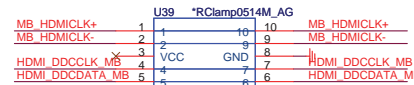
To MXM



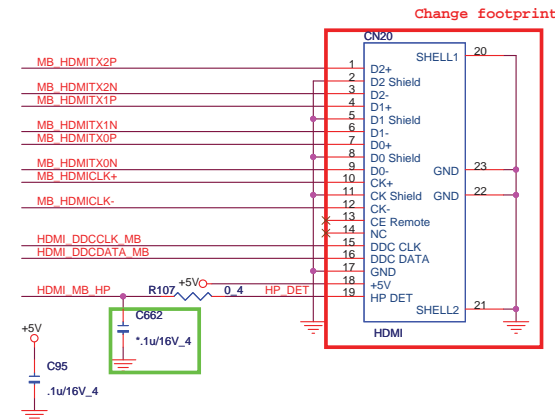
SMBUS



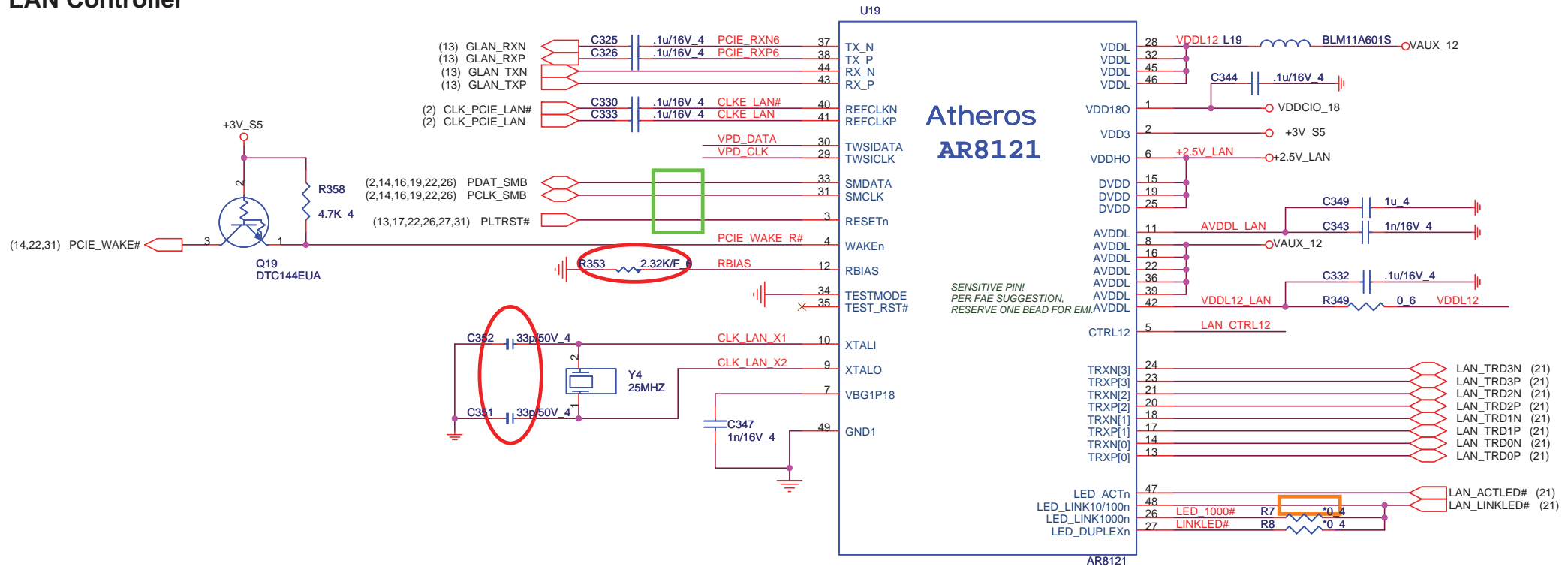
ESD Protect



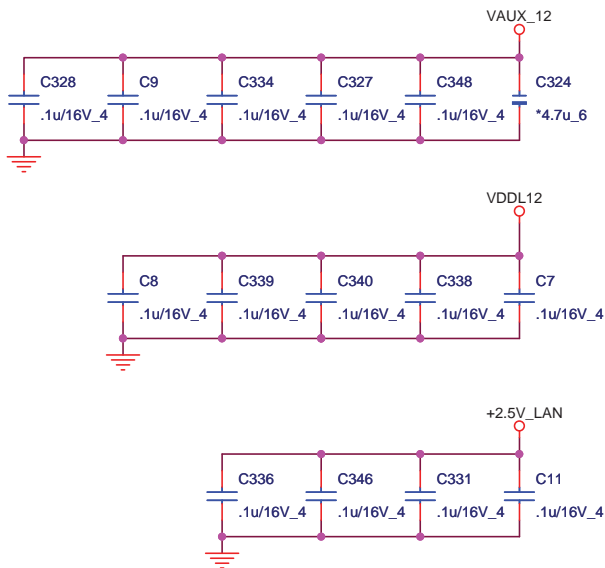
HDMI connector



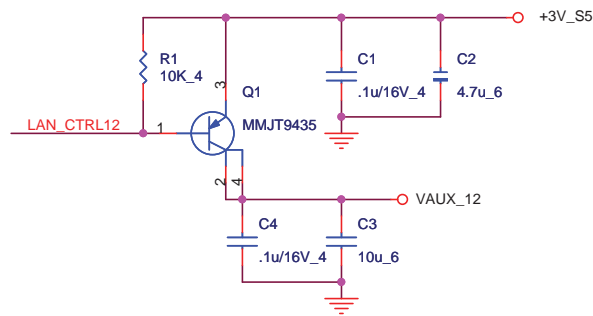
LAN Controller



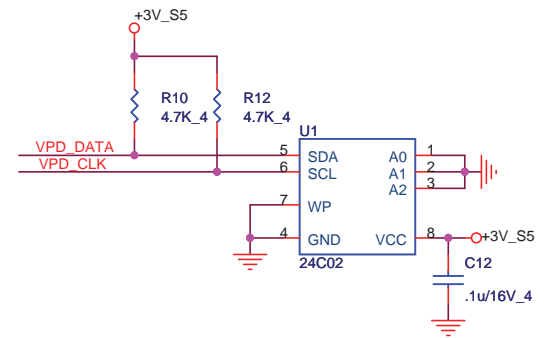
Decoupling CAP



Regulator(1.2V)



EEPROM

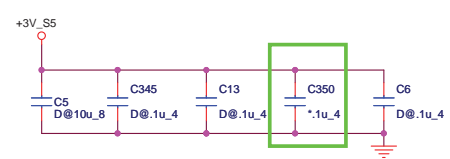
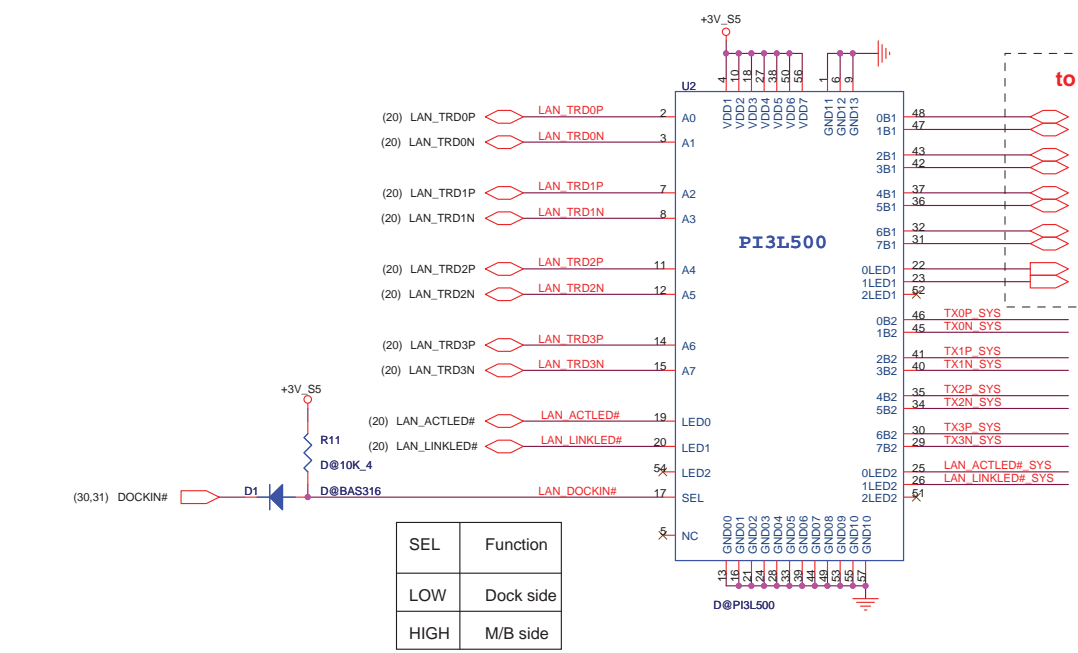


Quanta Computer Inc.

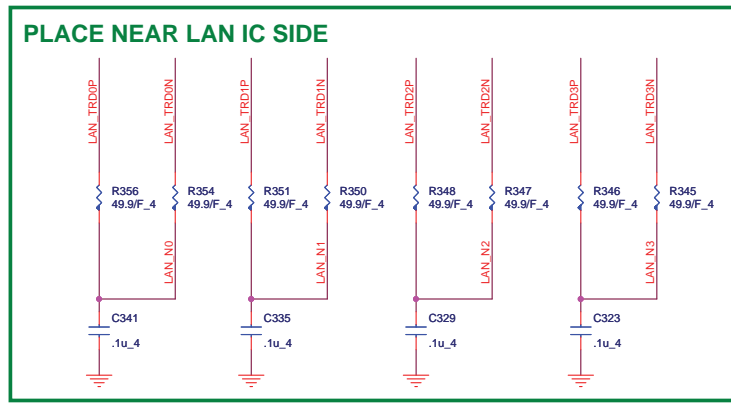
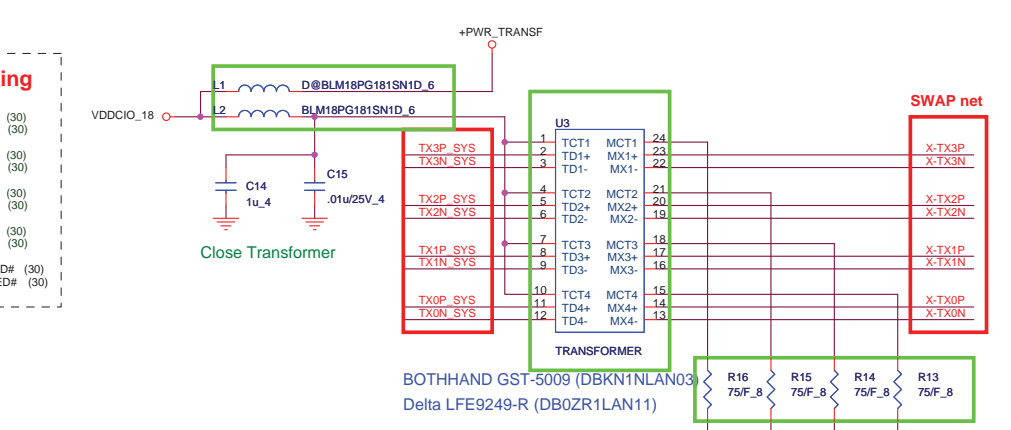
PROJECT : ZK2

Size	Document Number	Rev
	AR8121 LAN	3B
Date:	Friday, June 27, 2008	Sheet 20 of 39

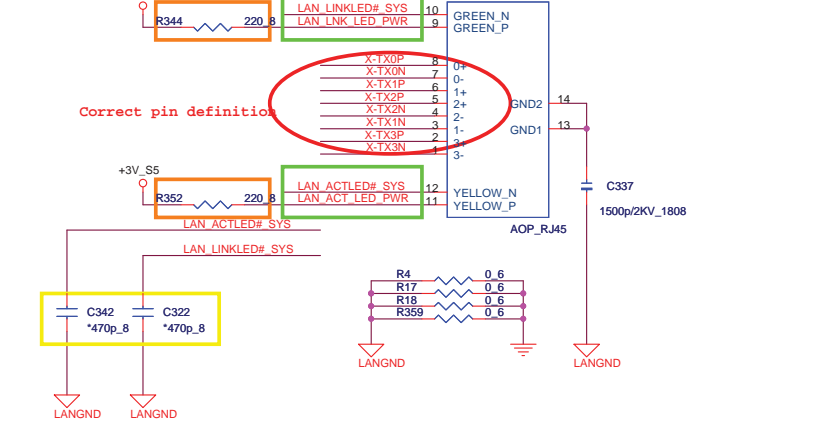
LAN SWITCH



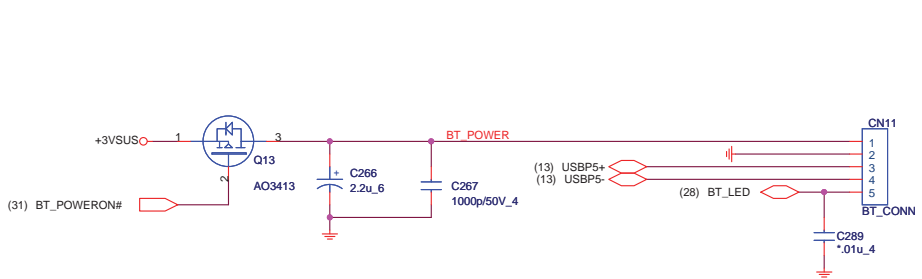
TRANSFORMER



RJ45

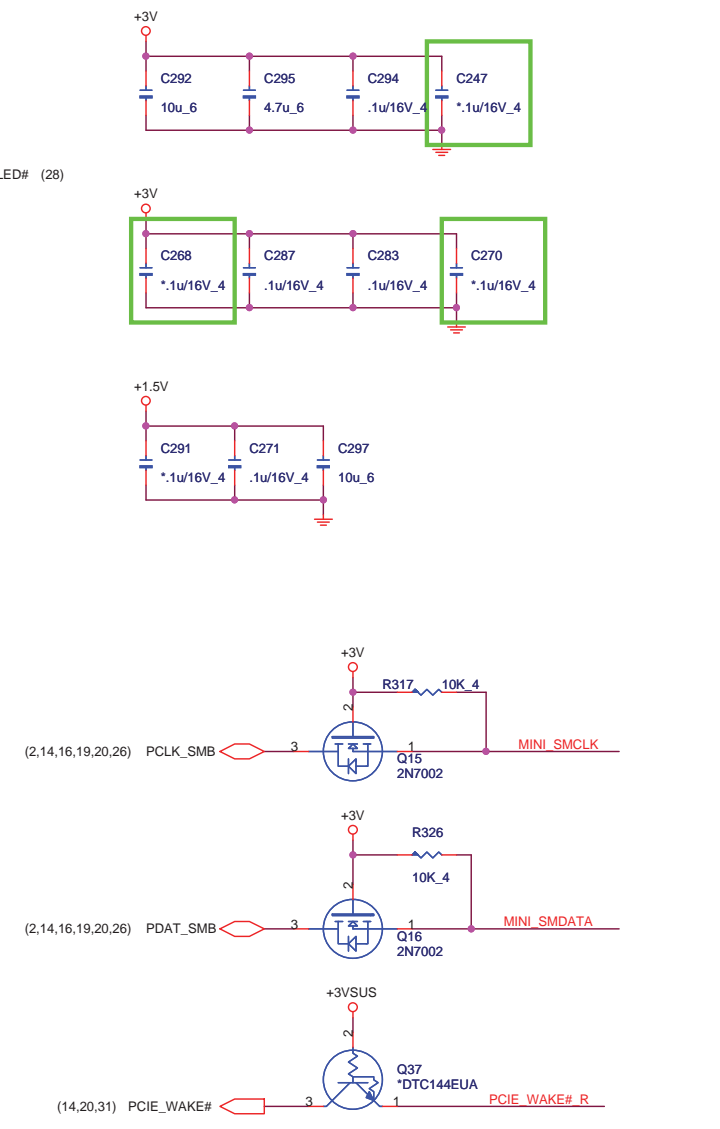
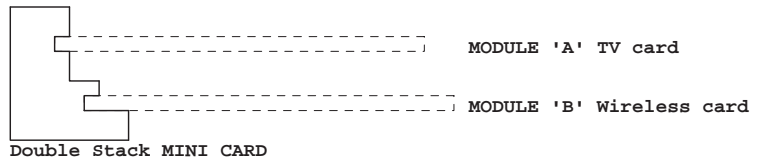
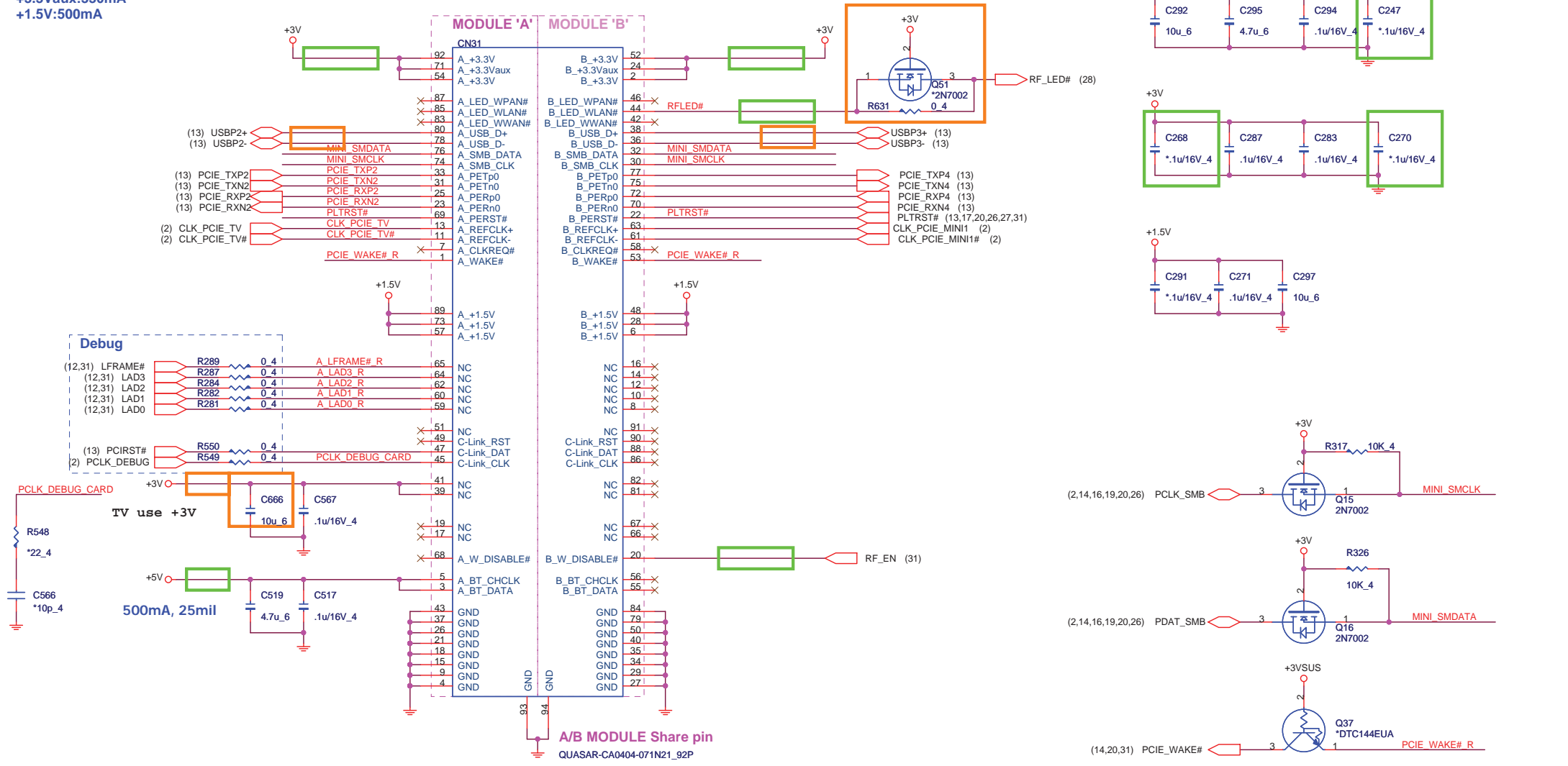


BLUETOOTH CONNECTOR



MINI-CARD

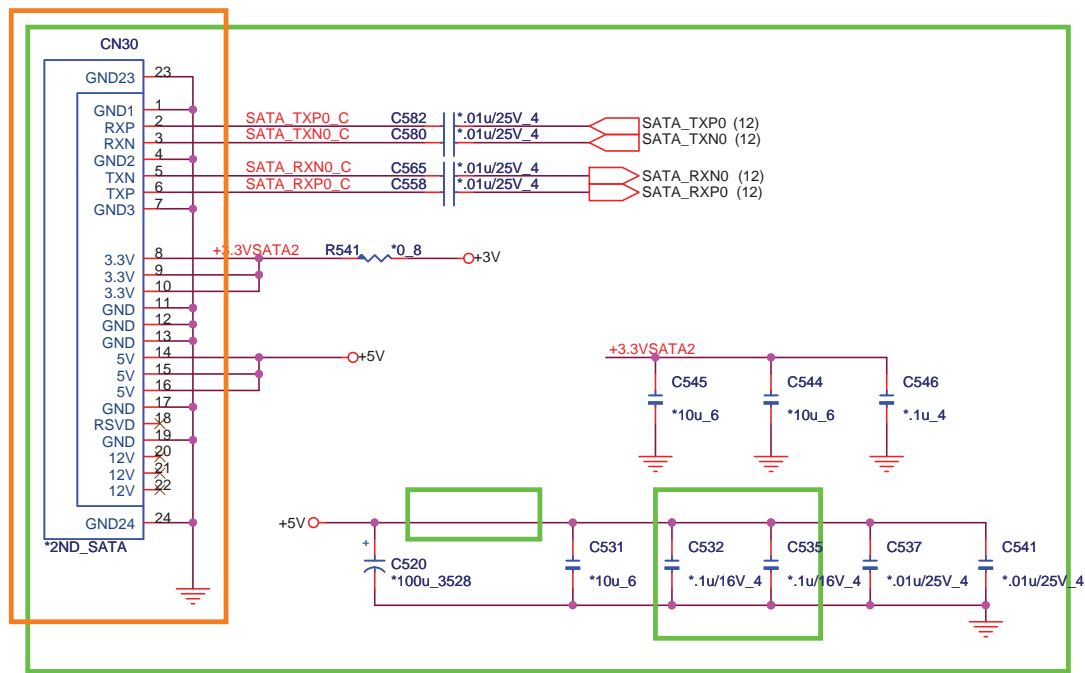
+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA



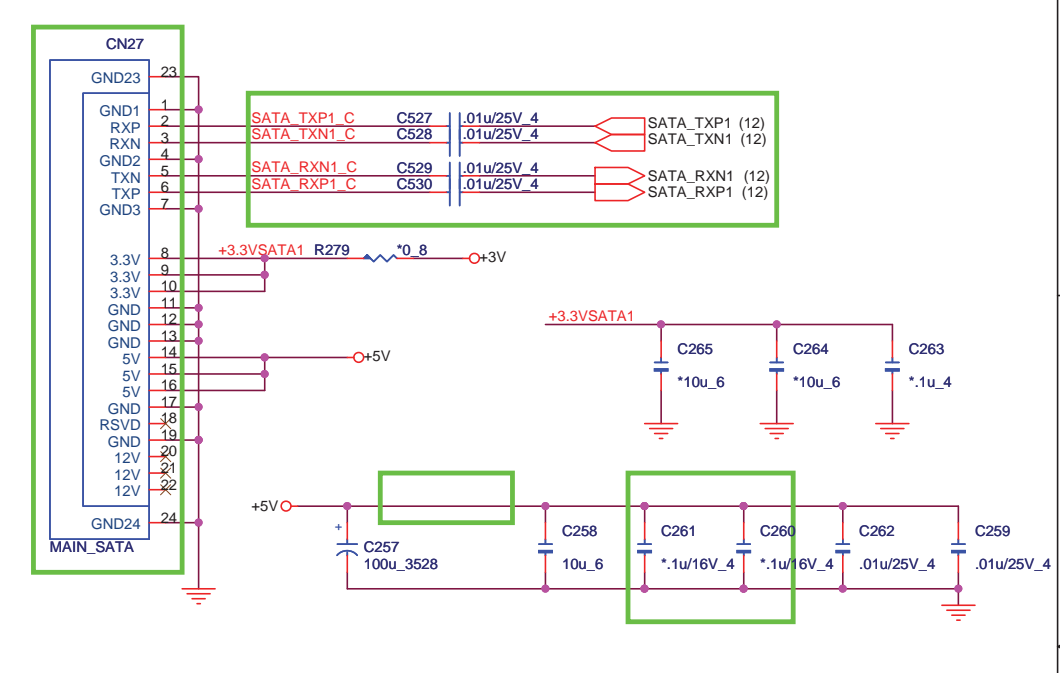
Quanta Computer Inc.
 PROJECT : ZK2

Size	Document Number	Rev
	MINI PCI-E card/TV	3B
Date:	Friday, June 27, 2008	Sheet 22 of 39

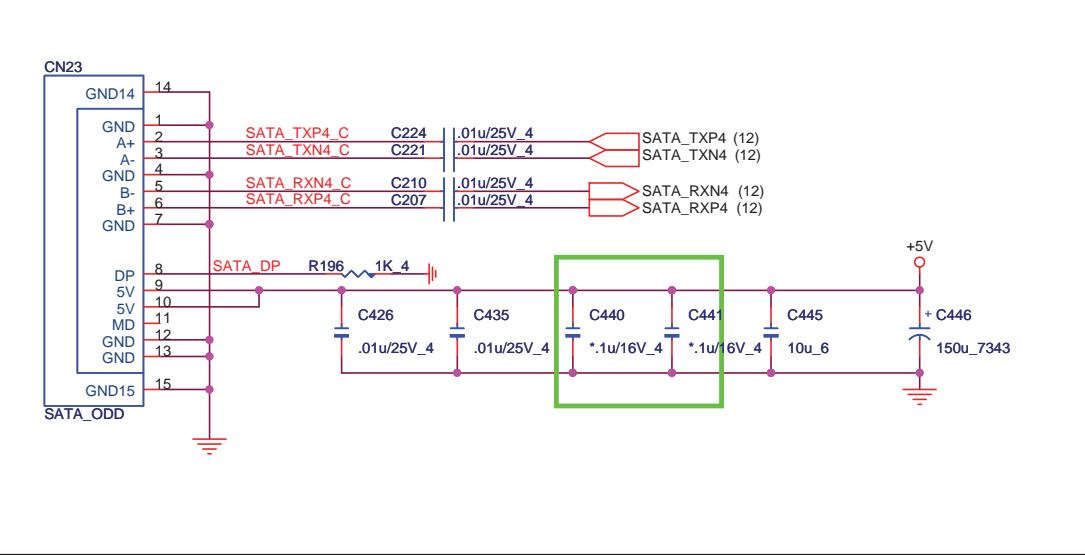
2nd SATA HDD (edge of board)



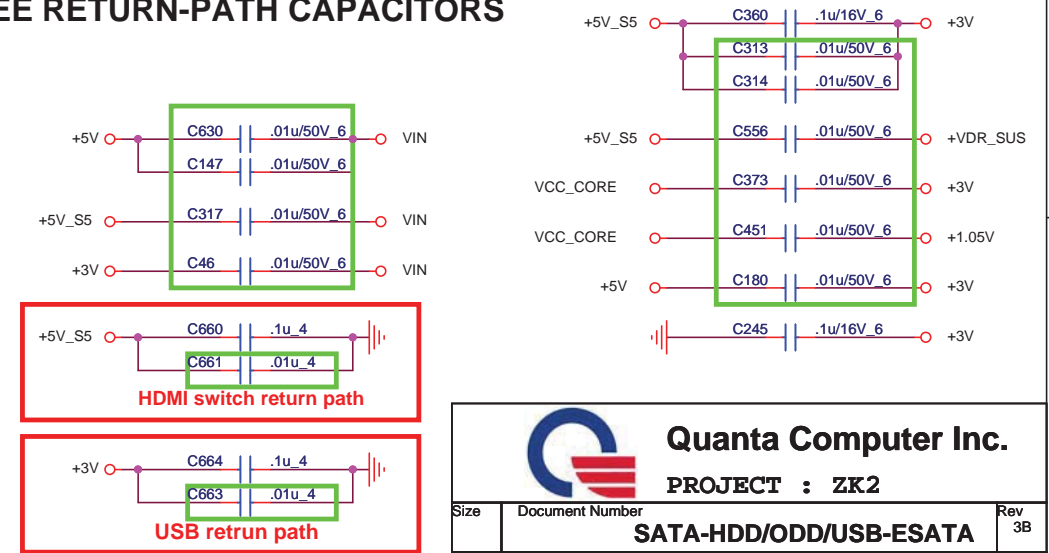
MAIN SATA HDD



ODD (SATA)



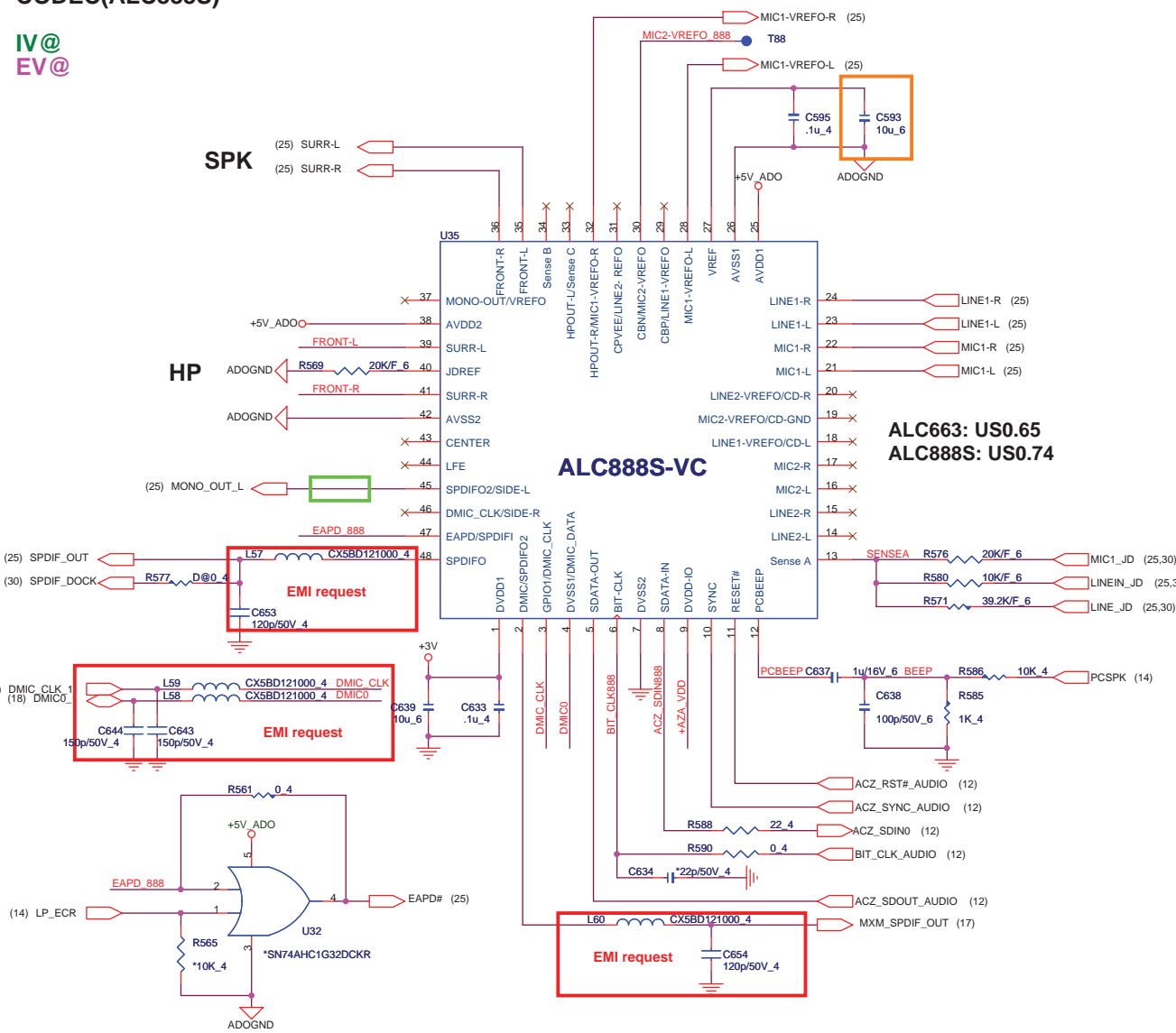
EE RETURN-PATH CAPACITORS



Quanta Computer Inc.
PROJECT : ZK2

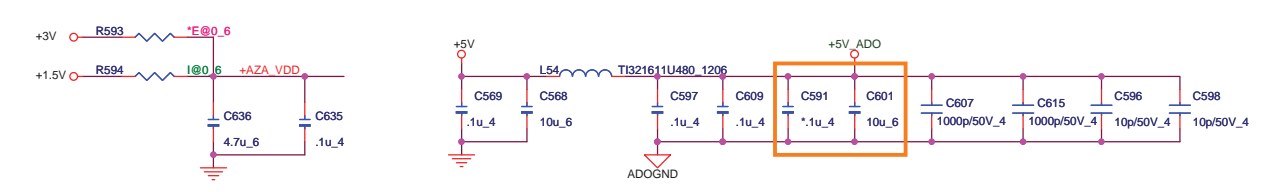
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
Date:	Friday, June 27, 2008	Sheet 23 of 39

CODEC(ALC888S)



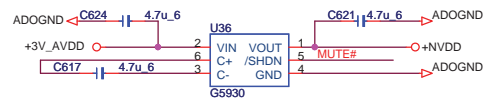
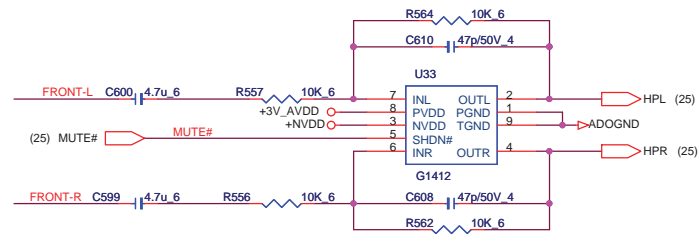
ALC663: US0.65
ALC888S: US0.74

Codec Power

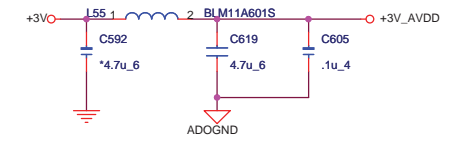


CODEC & MDC

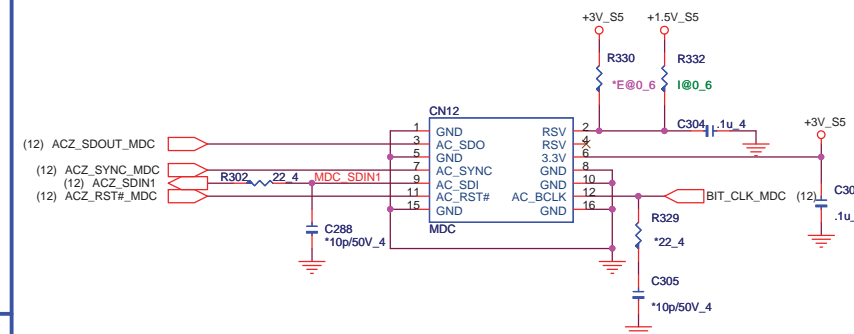
LINE-Out Amplifier



LINE-Out Amplifier Power



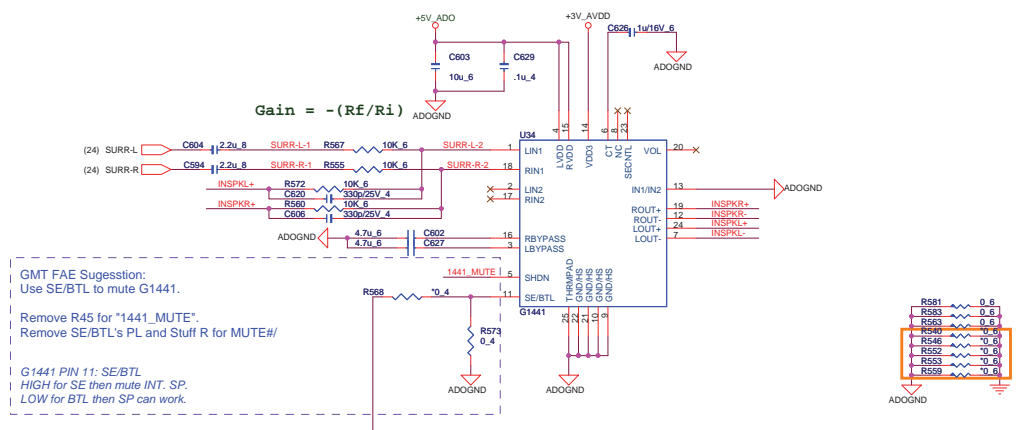
MDC



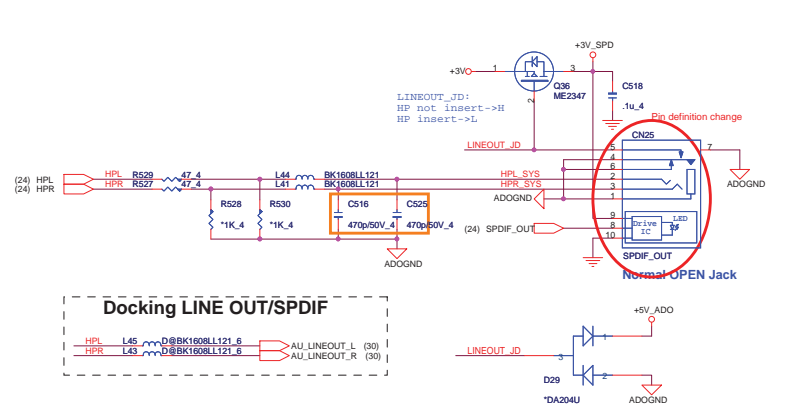
Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
REALTEK ALC663&888/MDC		3B
Date:	Friday, June 27, 2008	Sheet 24 of 39

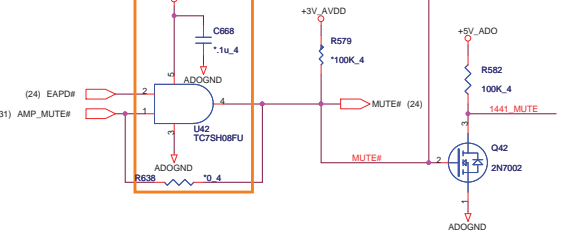
SPEAKER AMP.



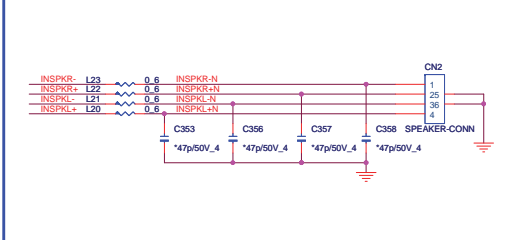
LINE-OUT/SPDIF0



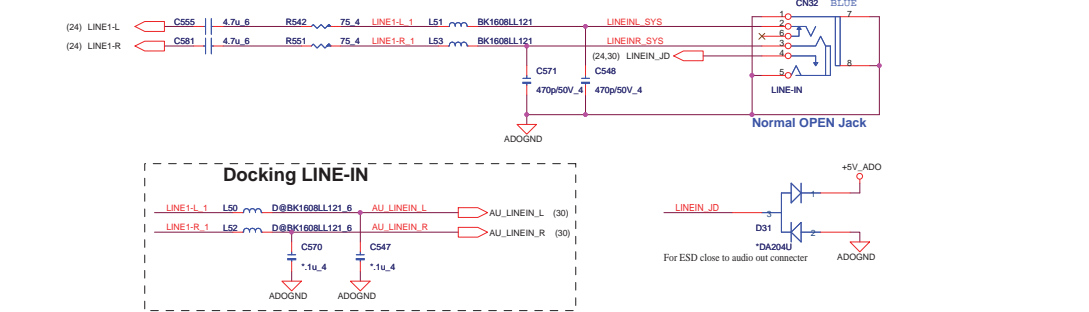
MUTE



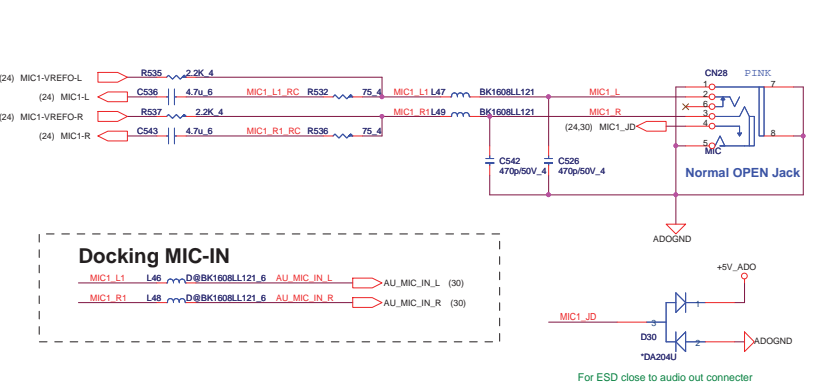
SPEAKER



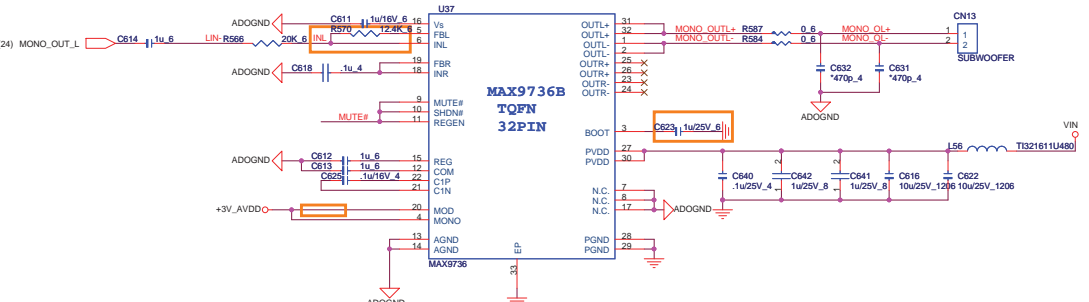
LINE IN




MIC



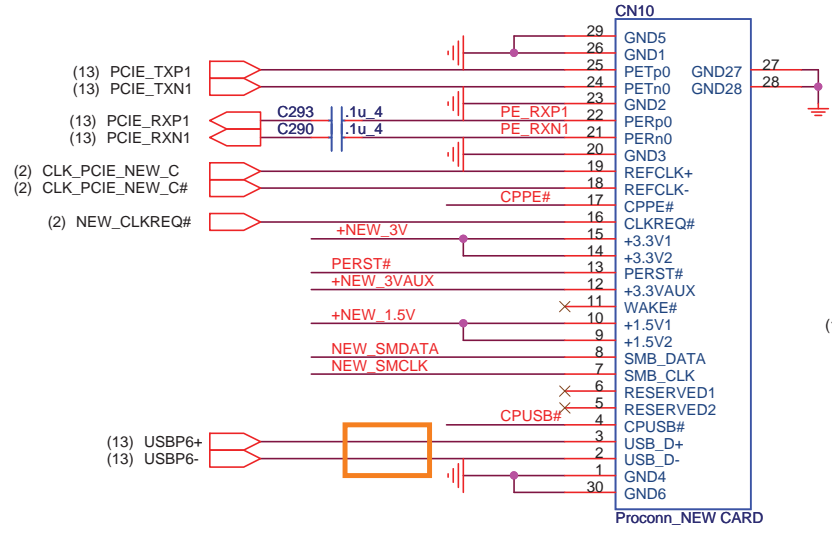
SUBWOOFER



AMP & PHONE JACK & SUBWOOFER

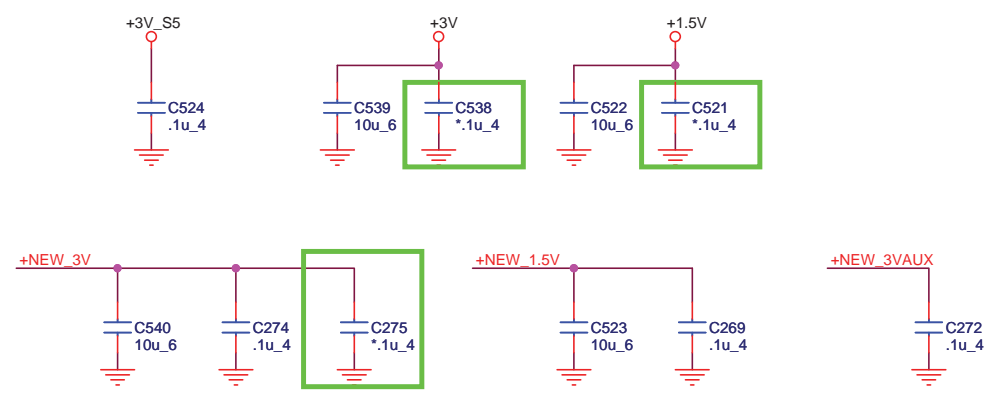
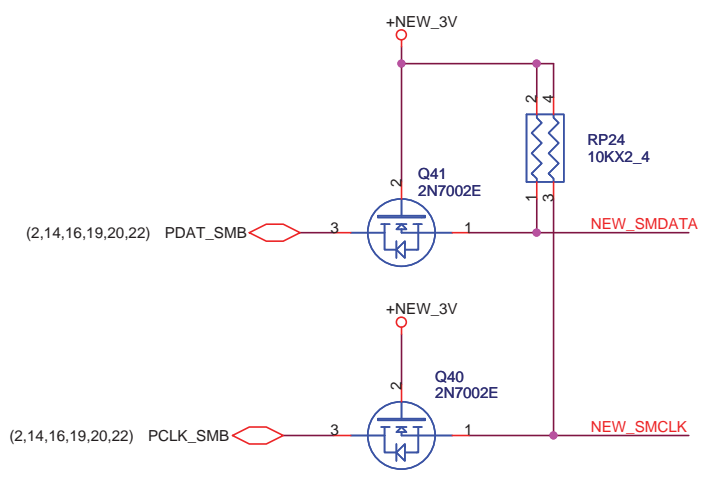
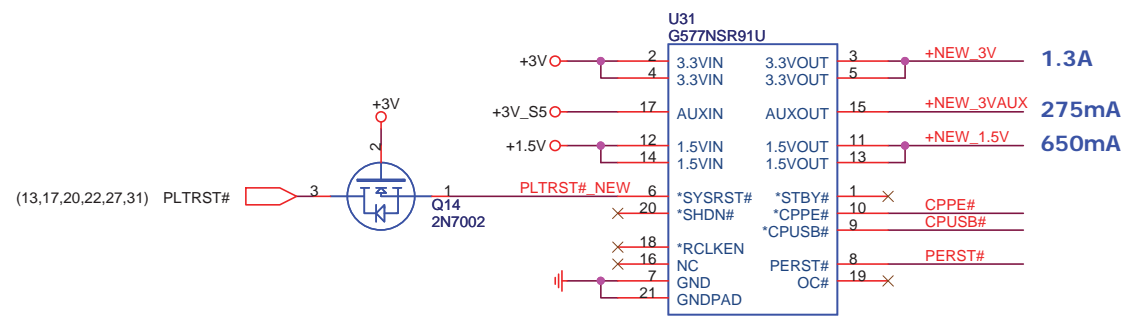

Quanta Computer Inc.
PROJECT : ZK2
 Size Document Number **AMP /AUDIO JACK CONN** Rev 38
 Date: Friday, June 27, 2008 Sheet 25 of 39

NEW CARD



NEW CARD'S POWER SWITCH

TI: AL002231000
GMT: AL000577002

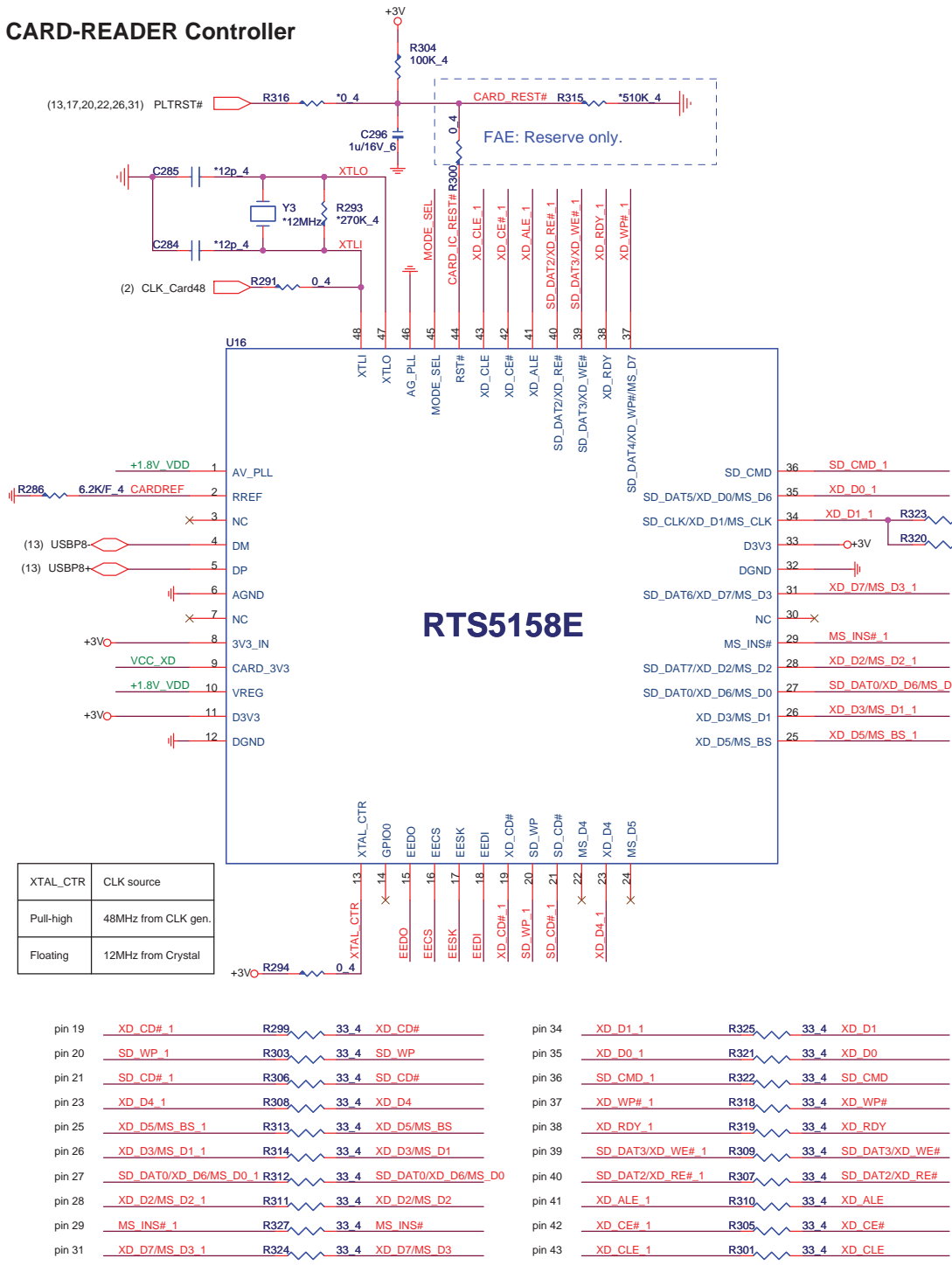


Quanta Computer Inc.
PROJECT : ZK2

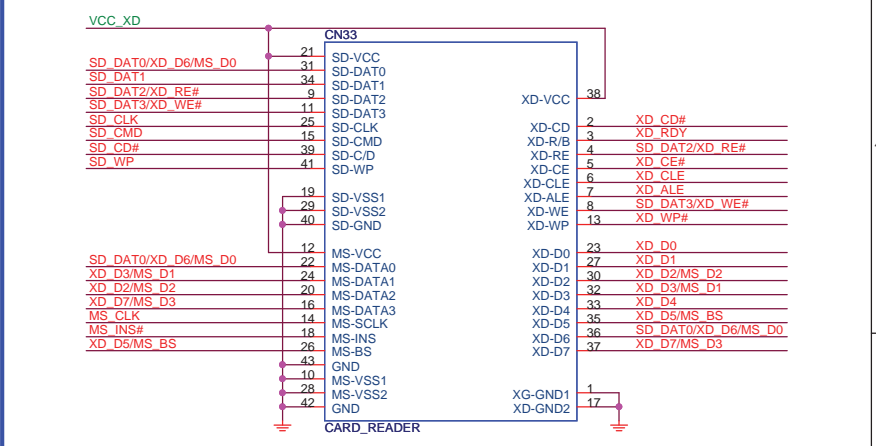
Size	Document Number	Rev
		3B

Date: Friday, June 27, 2008 Sheet 26 of 39

CARD-READER Controller

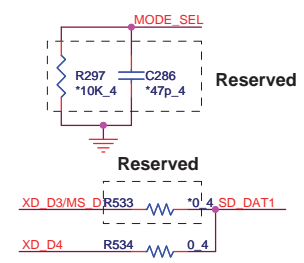


4 IN 1 CARD READER

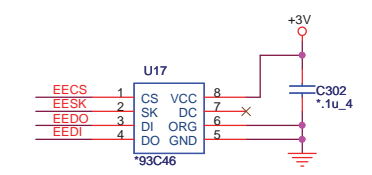


Model Select

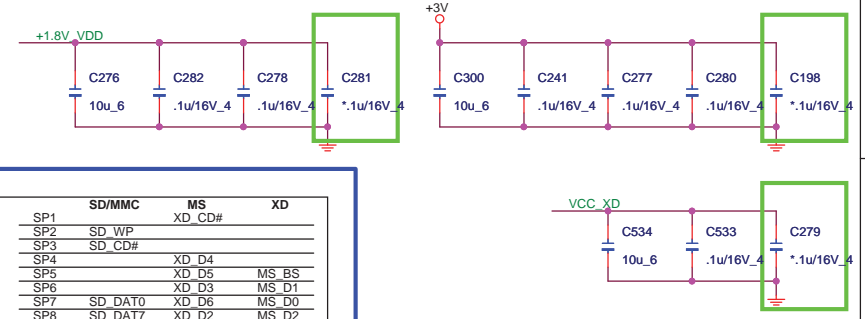
R6256/C860=NC/NC (R6258:ON)=> SD_D1 from pin23
 R6256/C860=10K/47pF(R6257:ON)=>SD_D1 from pin26



EEPROM(Reserved)



Decoupling CAP

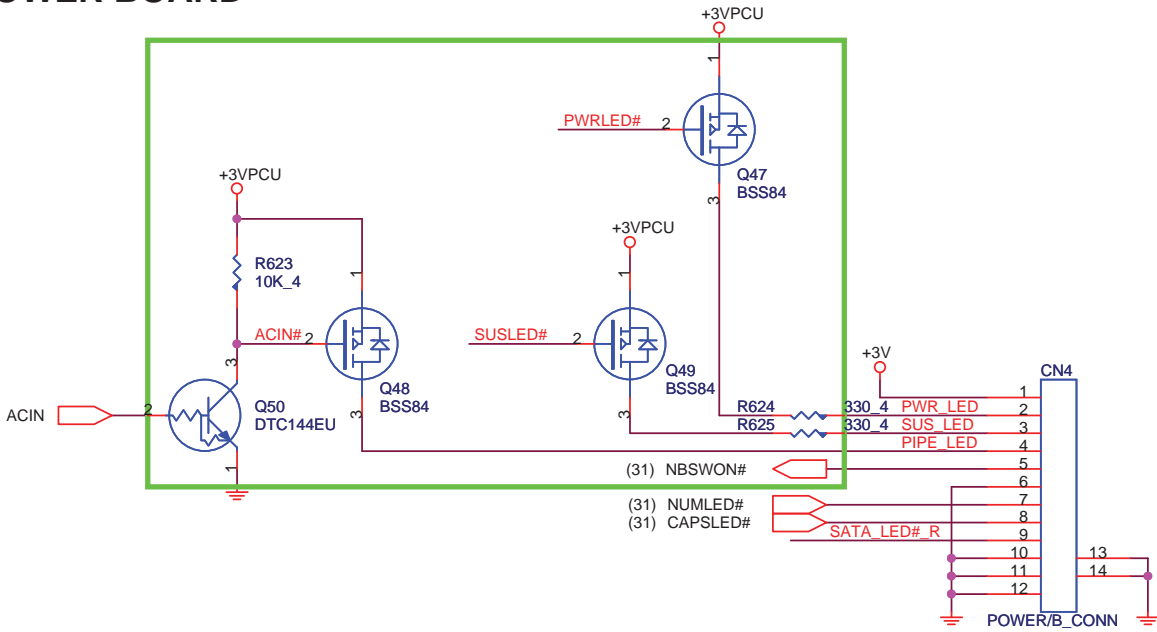


SP	SD/MMC	MS	XD
SP1		XD_CD#	
SP2	SD_WP		
SP3	SD_CD#		
SP4		XD_D4	
SP5		XD_D5	MS_BS
SP6		XD_D3	MS_D1
SP7	SD_DAT0	XD_D6	MS_D0
SP8	SD_DAT7	XD_D2	MS_D2
SP9			MS_INS#
SP10	SD_DAT6	XD_D7	MS_D3
SP11		XD_D1	
SP12	SD_DAT5	XD_D0	MS_D6
SP13	SD_DAT4	XD_WP#	MS_D7
SP14		XD_RDY	
SP15	SD_DAT3	XD_WE#	
SP16	SD_DAT2	XD_RE#	
SP17		XD_ALE	
SP18		XD_CE#	
SP19		XD_CLE	
		MS_D4	
		MS_D5	

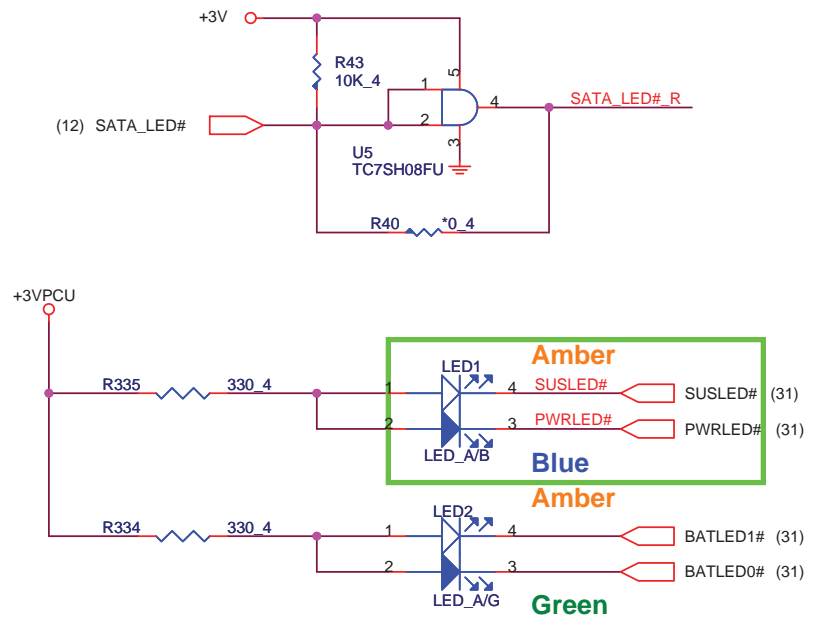
Quanta Computer Inc.
PROJECT : ZK2
CARD READER RTS5158E

Size: Document Number: Rev: 3B

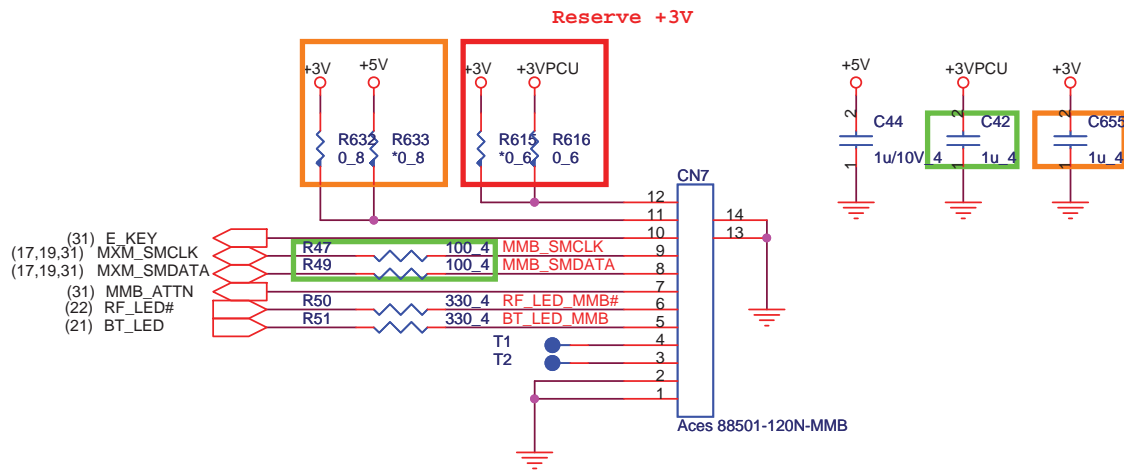
POWER BOARD



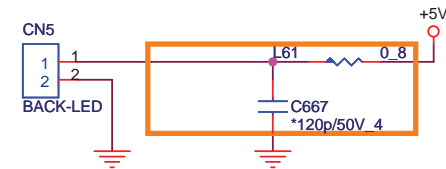
LED




MMB

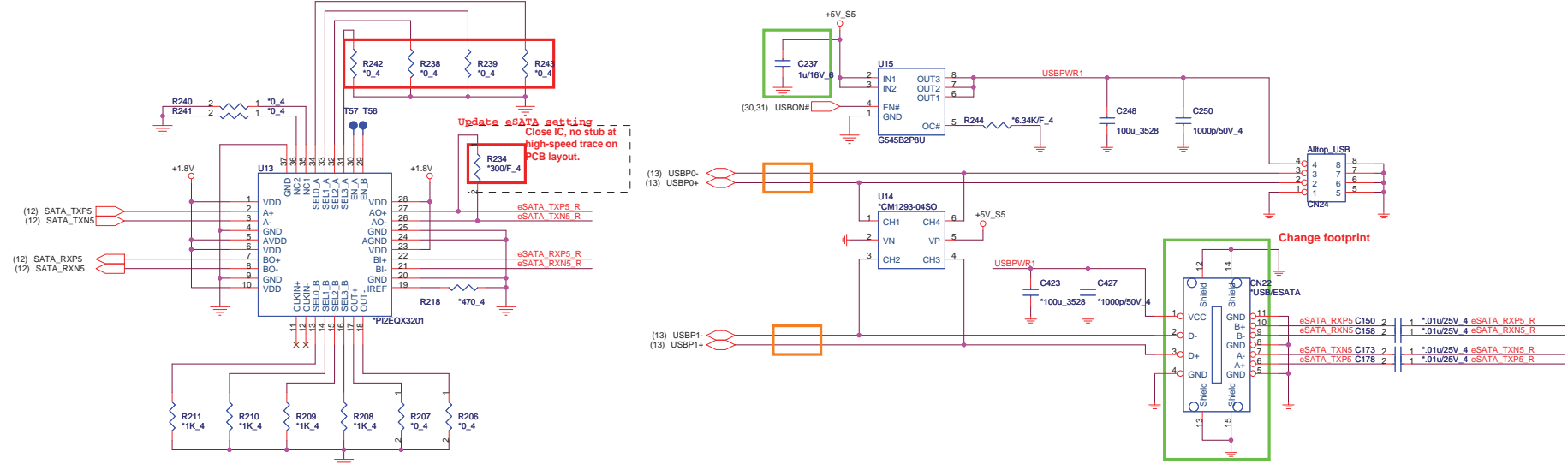


Backlight Logo LED



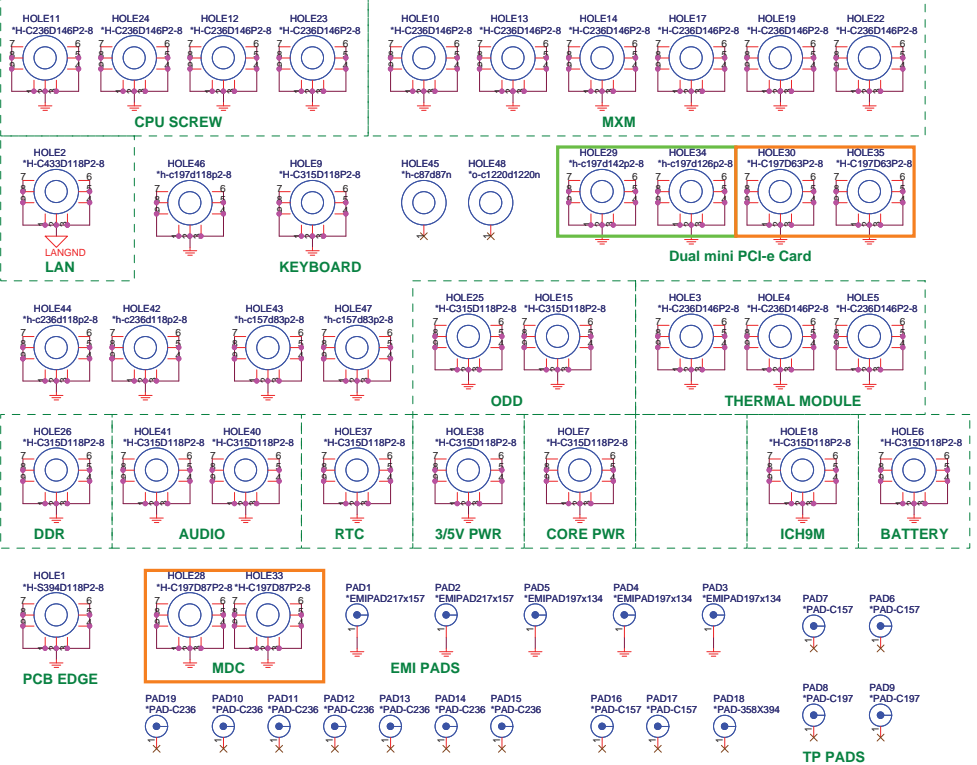

Quanta Computer Inc.
PROJECT : ZK2
 Size Document Number **POWER/MMB/LAUNCH/LED** Rev 3B
 Date: Friday, June 27, 2008 Sheet 28 of 39

USB & eSATA

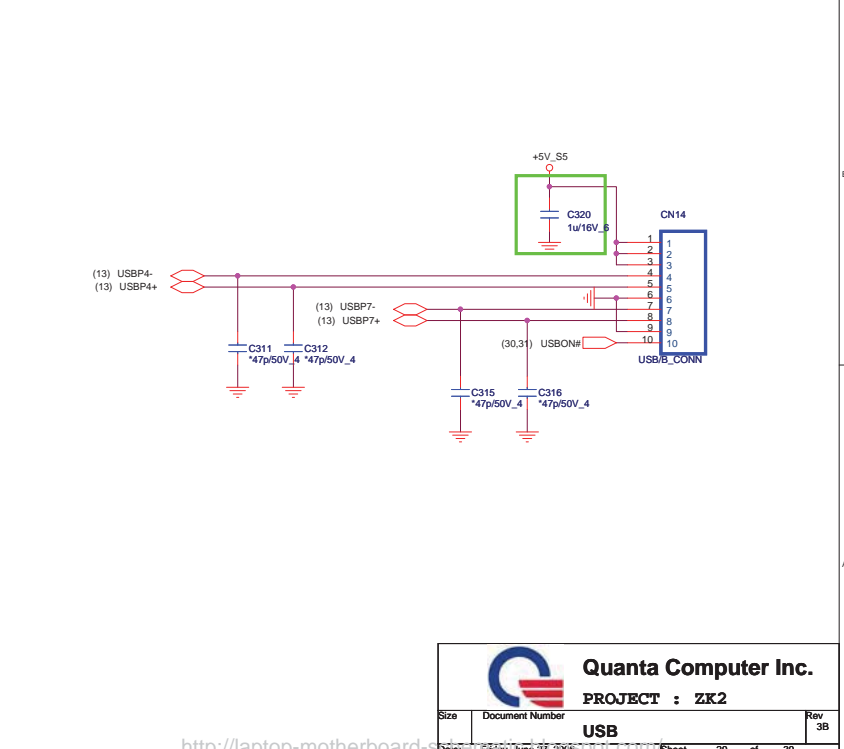



SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

HOLES



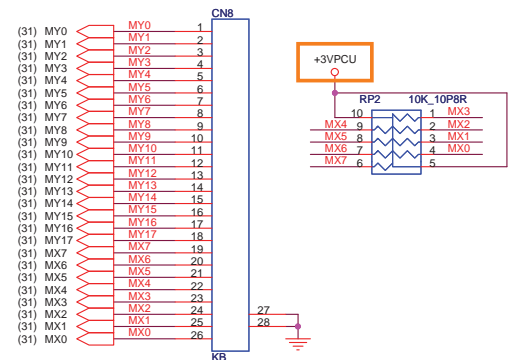
USB/B



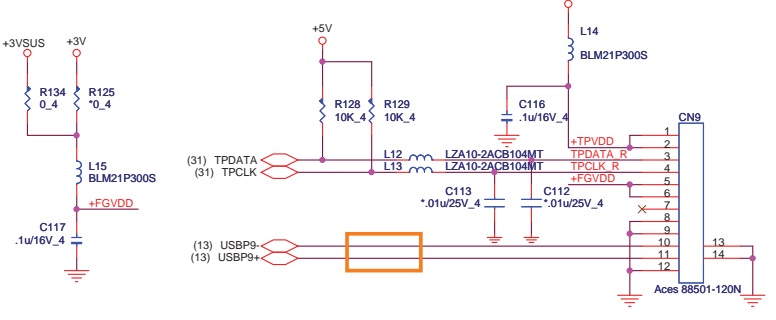

Quanta Computer Inc.
PROJECT : ZK2
USB

Size	Document Number	Rev
		3B

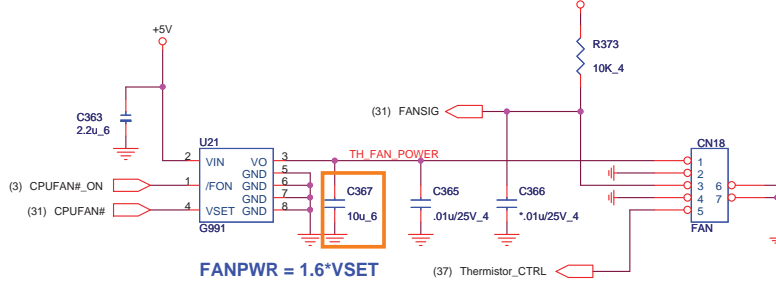
INT K/B



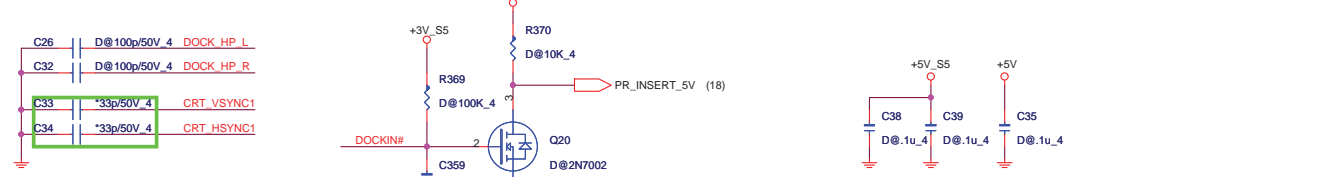
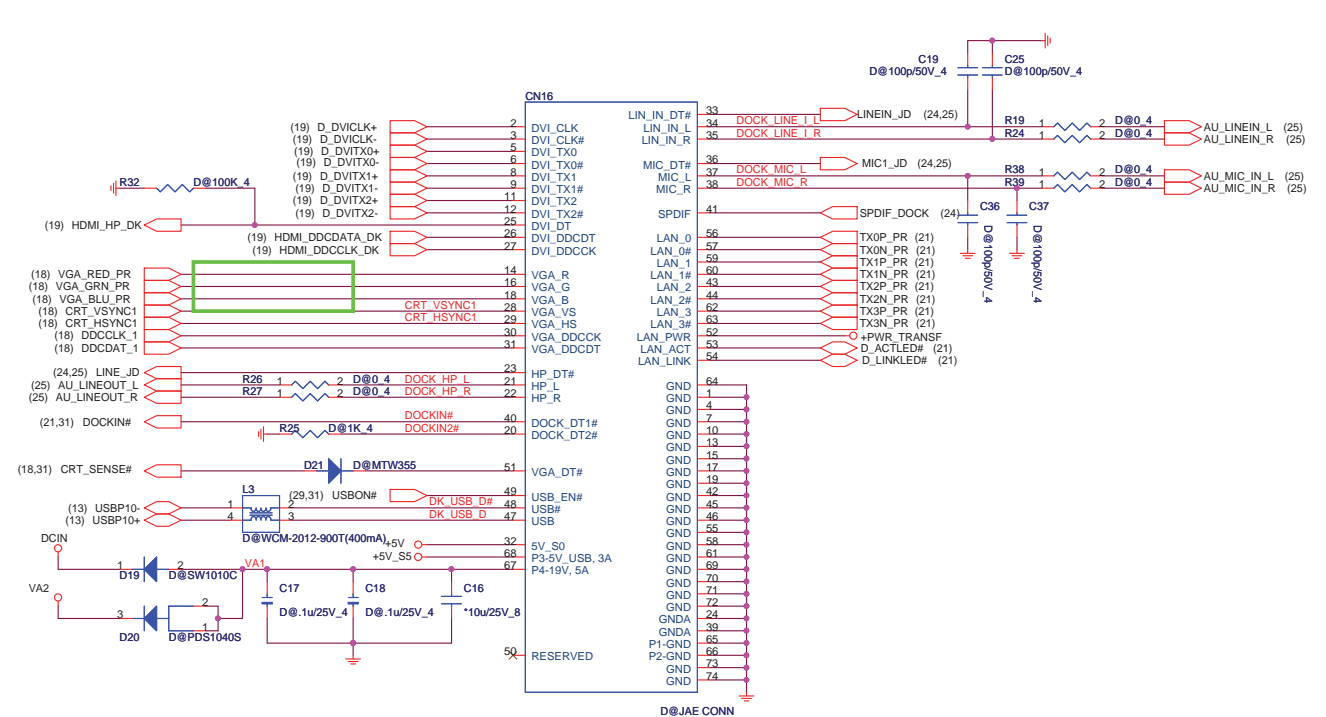
TOUCHPAD & Finger-Printer CONN.



CPU FAN

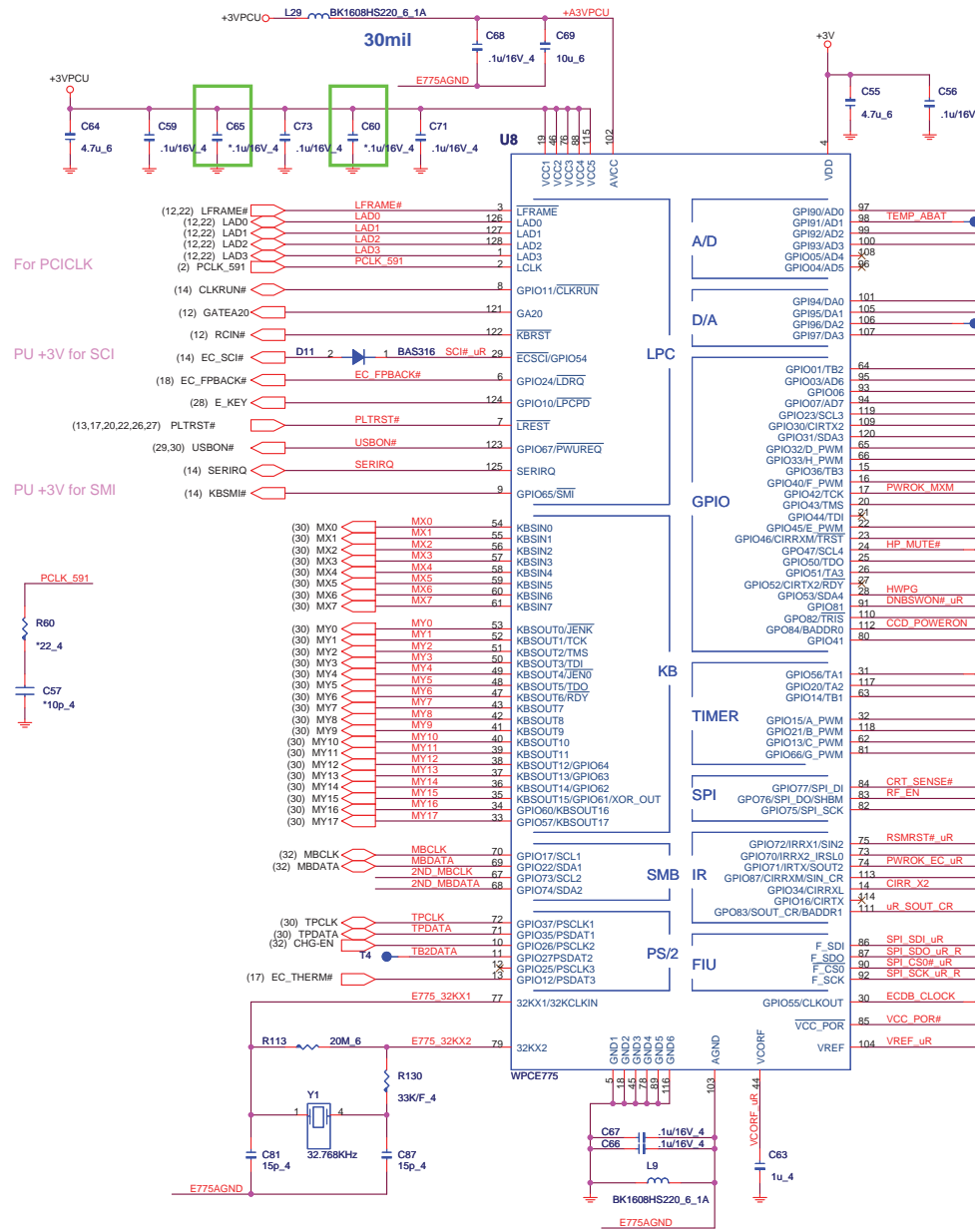


CABLE DOCK



Quanta Computer Inc.
PROJECT : ZK2

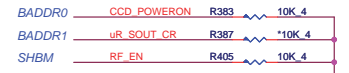
Size	Document Number	Rev
	KB/FAN/TP+FP/DOCK	3B
Date:	Wednesday, July 09, 2008	Sheet 30 of 39



I/O ADDRESS SETTING

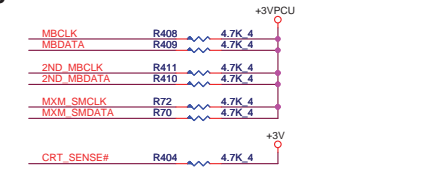
I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

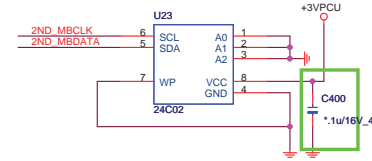


1/13 Confirm by vendor mail :
Disabled (*1) if using FWH device on LPC.
Enabled (0') if using SPI flash for both system BIOS and EC firmware

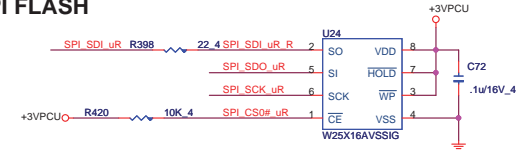
SM BUS PU



ACER ID

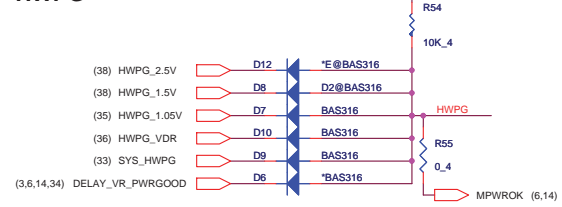


SPI FLASH

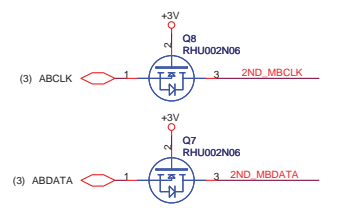


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

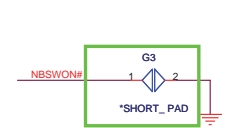
HWPG



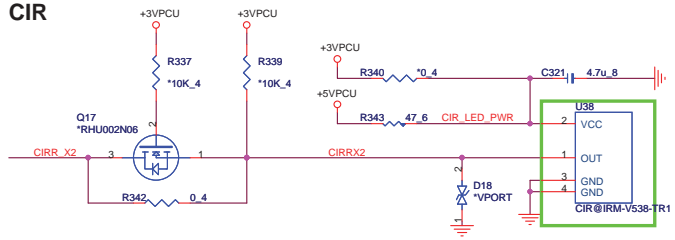
SMBus



POWER-ON PAD



CIR



INTERNAL KEYBOARD STRIP SET



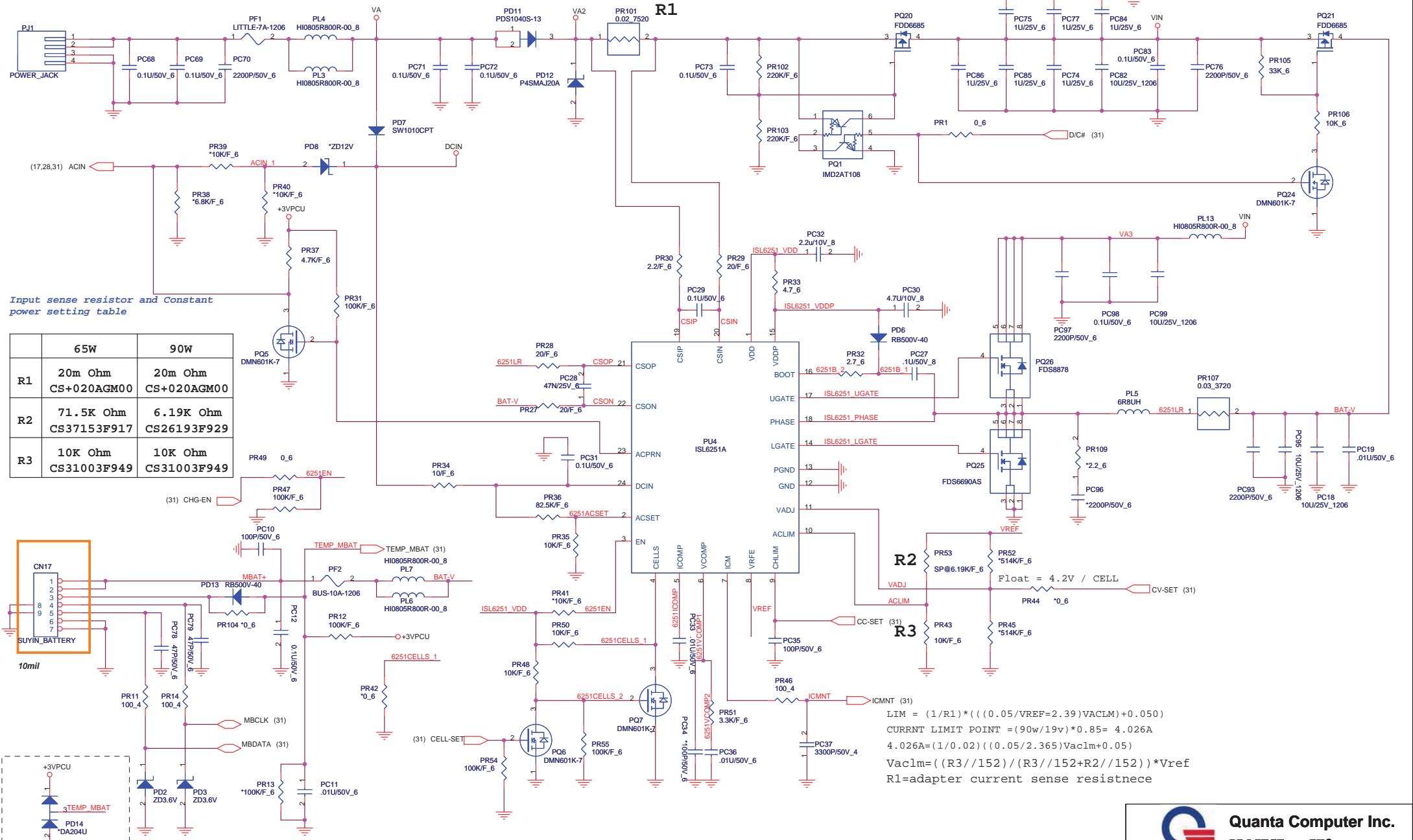
Quanta Computer Inc.

PROJECT : ZK2

WPCE775C_ODG & FLASH

Size Document Number Rev 3B

Date: Friday, June 27, 2008 Sheet 31 of 39



Input sense resistor and Constant power setting table

	65W	90W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

$$LIM = (1/R1) * (((0.05/VREF=2.39) \text{Vaclm}) + 0.050)$$

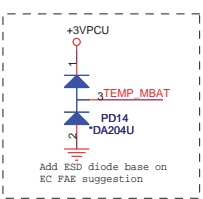
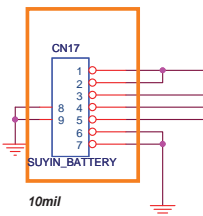
$$CURRNT \text{ LIMIT POINT} = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * ((0.05/2.365) \text{Vaclm} + 0.05)$$

$$\text{Vaclm} = ((R3//152) / (R3//152 + R2//152)) * Vref$$

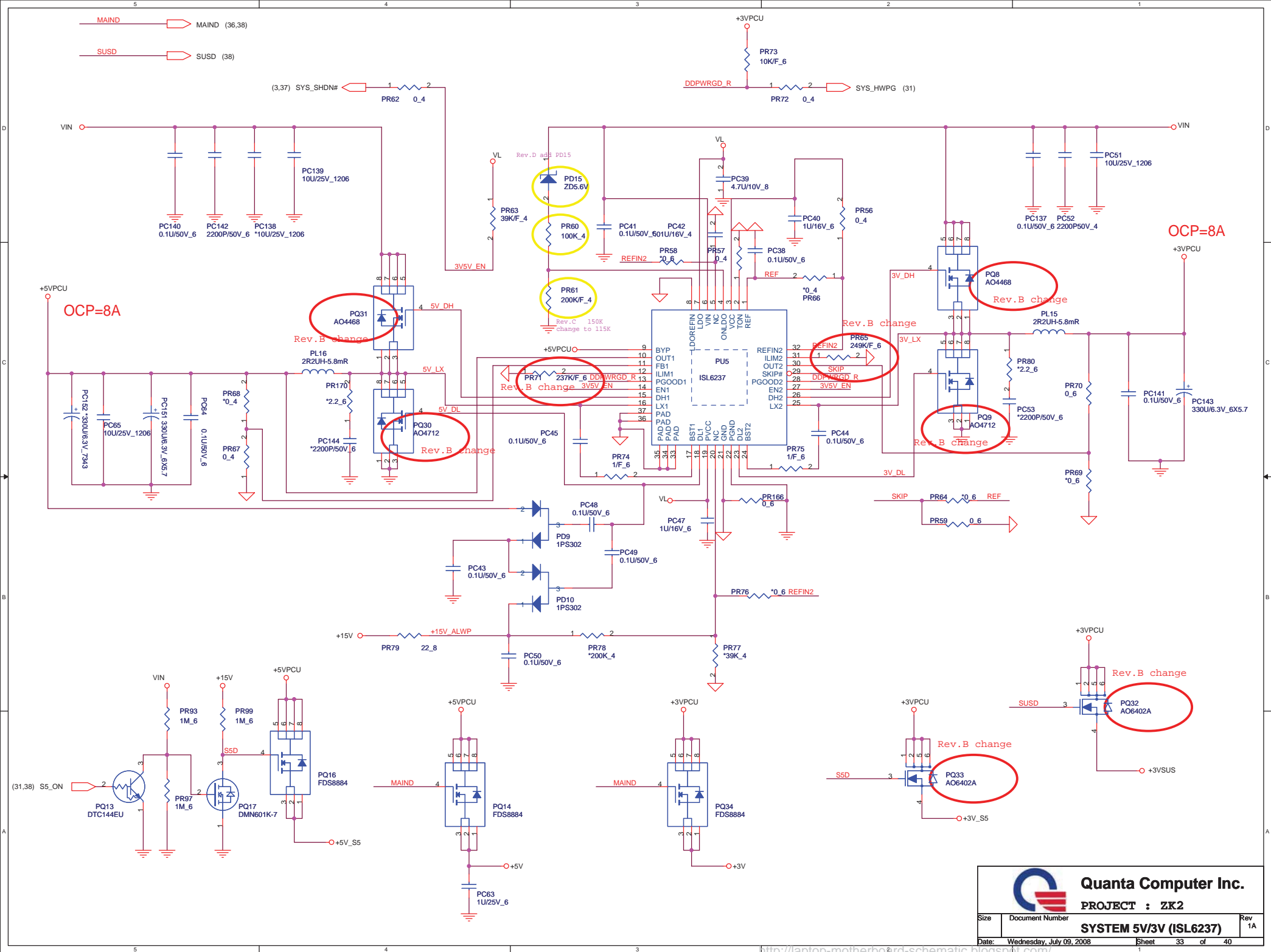
R1=adapter current sense resistnece

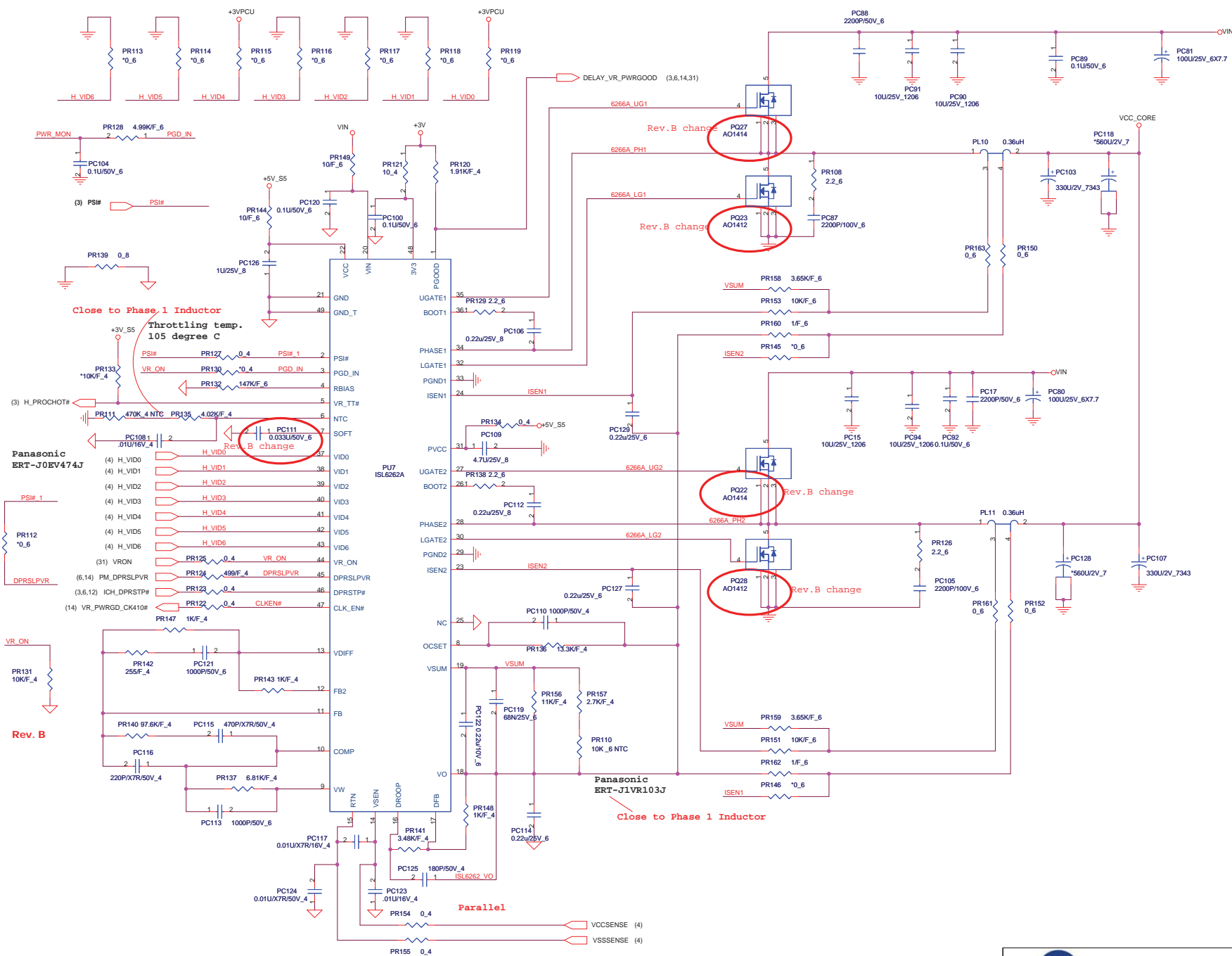
CELL-SET = Hi ----> Cells = VDD ---->4S
 CELL-SET = Low ----> Cells = GND ---->3S

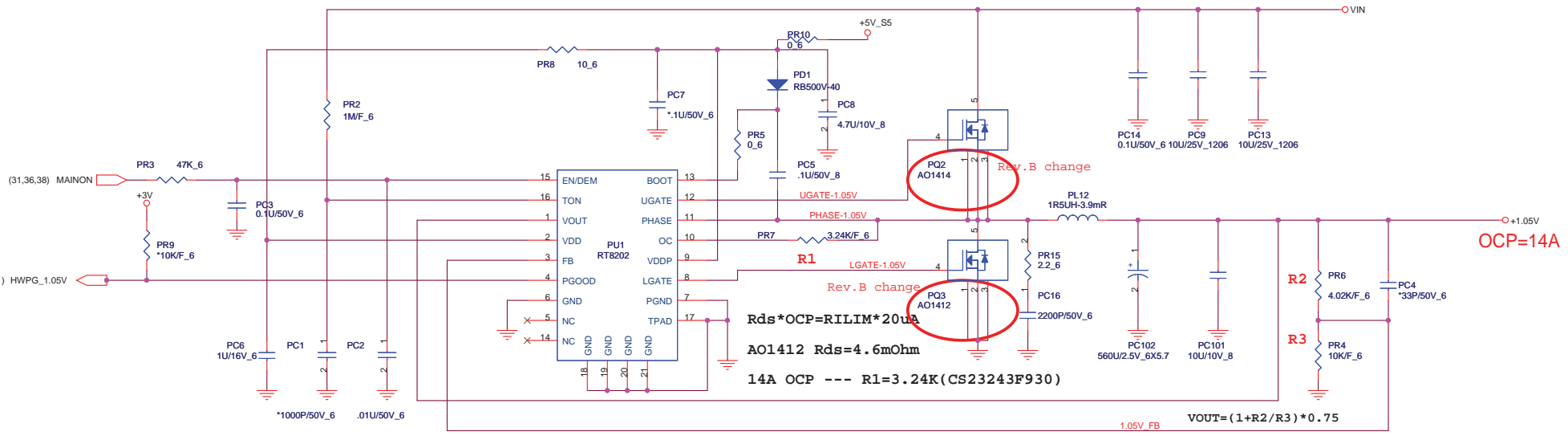


Quanta Computer Inc.
PROJECT : ZK2
CHARGER (ISL6251A)

Size: Document Number: Rev 1A
 Date: Friday, June 27, 2008 Sheet 32 of 40

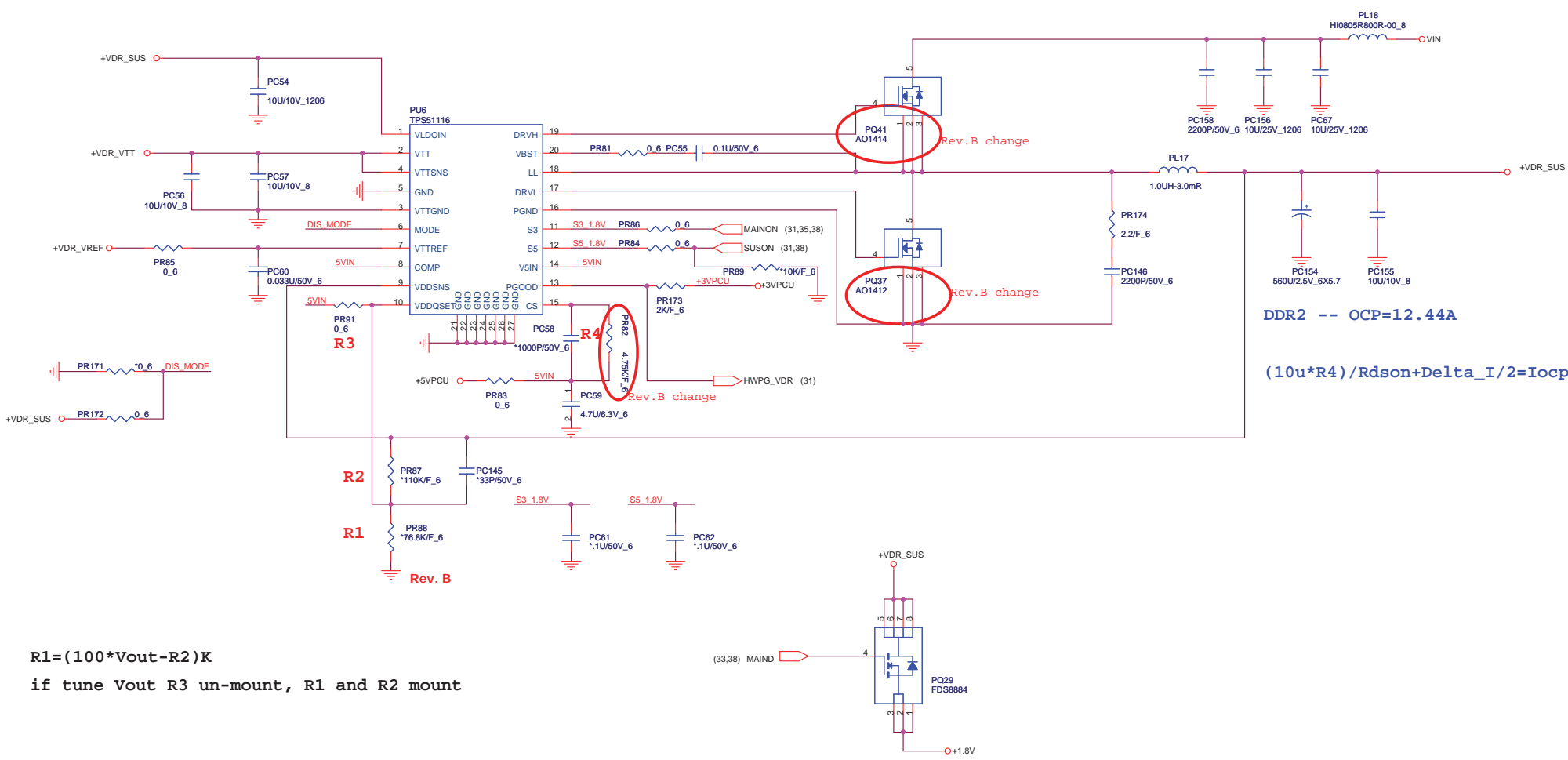






$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$

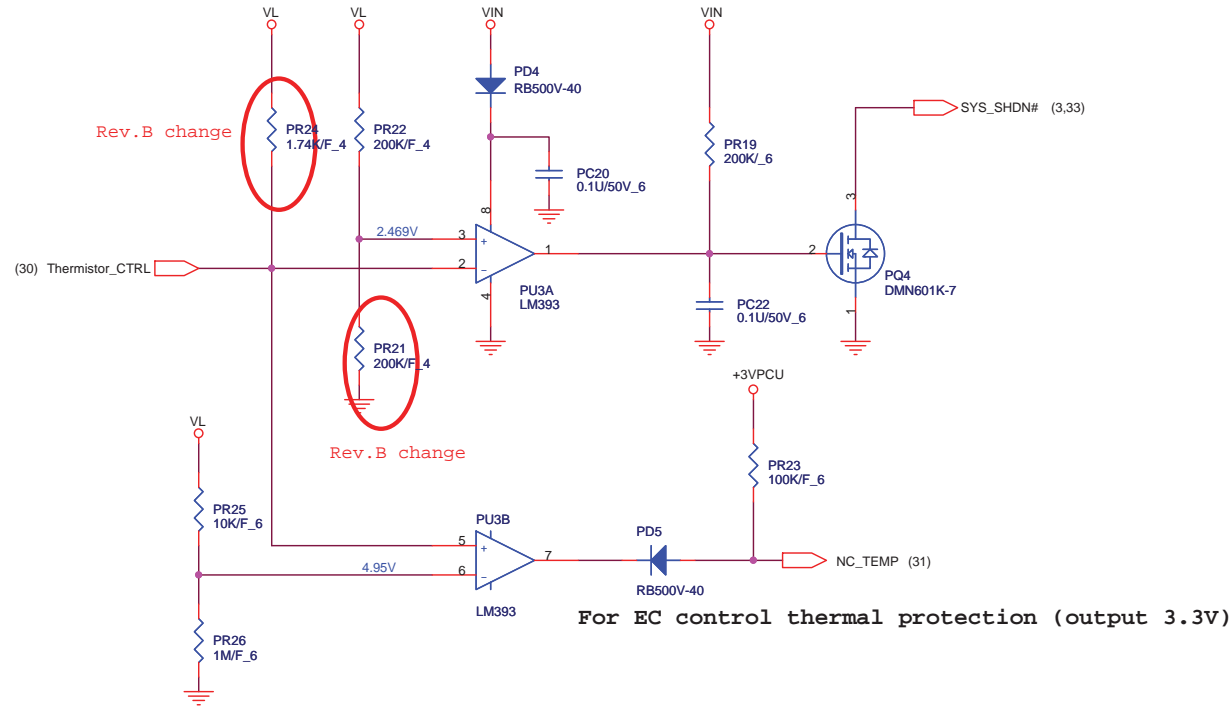
$Frequency = V_{out} / (V_{in} * TON)$




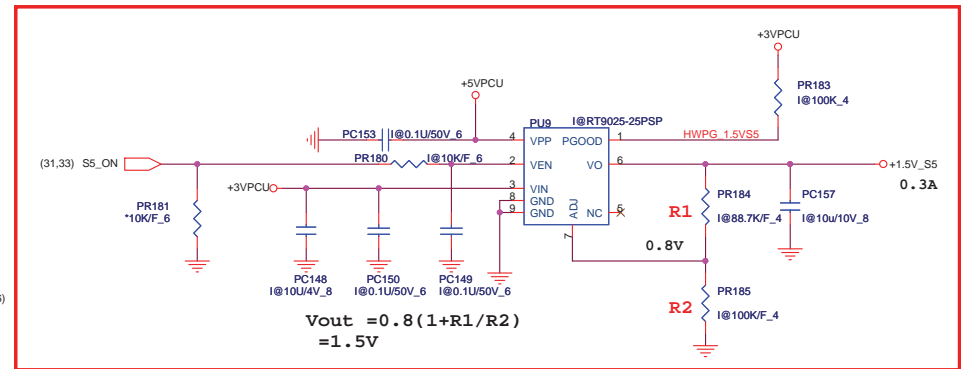
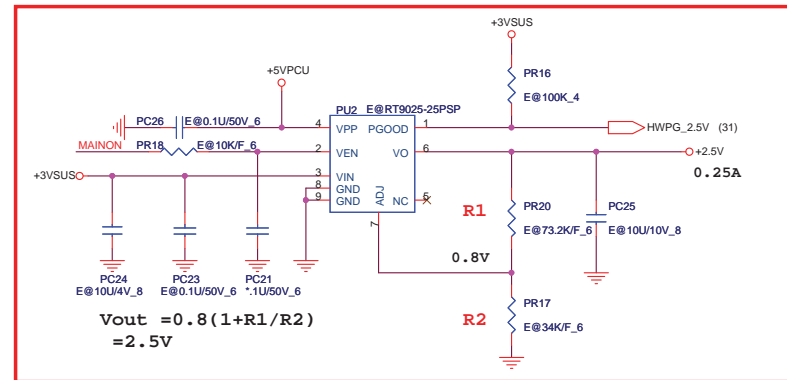
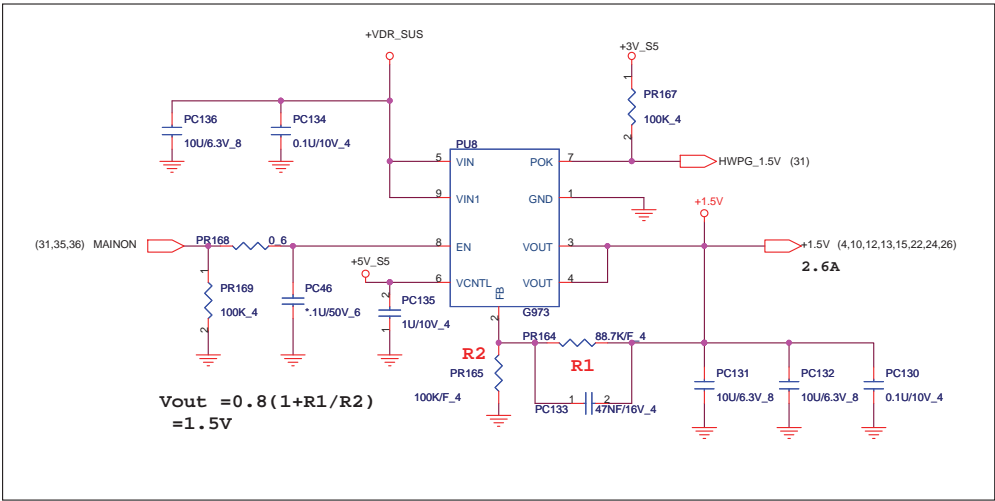
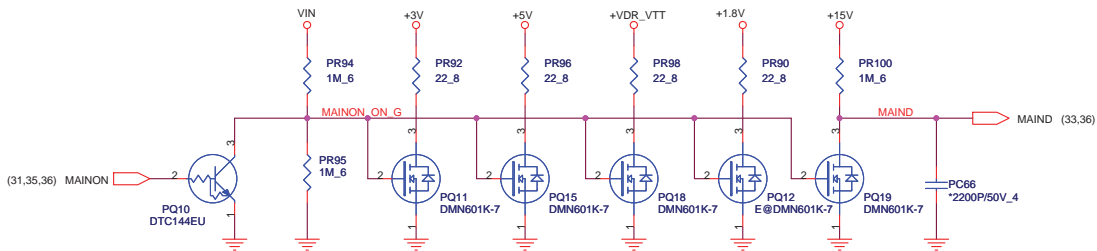
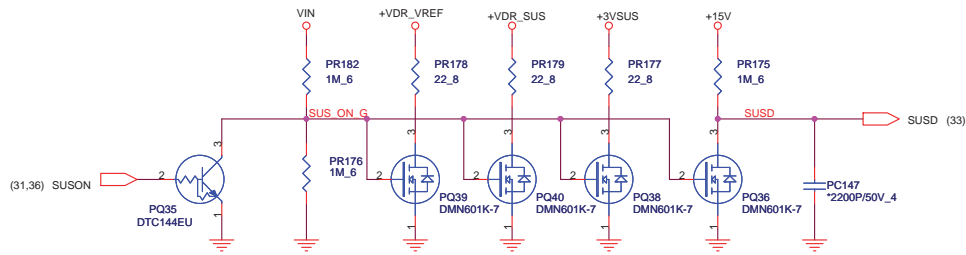
DDR2 -- OCP=12.44A
 $(10\mu * R4) / R_{dson} + \Delta I / 2 = I_{ocp}$

$R1 = (100 * V_{out} - R2)K$
 if tune V_{out} R3 un-mount, R1 and R2 mount


thermal protection



		Quanta Computer Inc.	
		PROJECT : ZK2	
Size	Document Number	Rev 1A	
Thermal protect			
Date:	Friday, June 27, 2008	Sheet	37 of 40



Model	REV	CHANGE LIST	MODEL	ZK2	
				FROM	To
ZK2 MB	1A	FIRST RELEASED: E200803-5424 (PCB: DAQZK2MB6A0)		X	1A
				X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
2A		Power change items		1A	2A
		Page32 : [PRS3] 6.19Kohm(CS26193F929) for MDM(90W ADP)		1A	2A
		71.5Kohm(CS37153F917) for DDM(60W ADP)		1A	2A
		Page33 : 1. Change PQ31/PQ8 from FDS8878(BAM88780020) to A04468(BAM44680003)		1A	2A
		2. Change PQ30/PQ9 from FDS6690A8(BAM66900022) to A04712 (BAM47120000)		1A	2A
		3. Change PQ32/PQ33 from FDC853 (BAM65300003) to A06402A (BAM64020000)		1A	2A
		4. Change PR61 from 150K/F 4(CS41502F818) to 150K/F 4(CS41502B10)		1A	2A
		5. Change PR71 from 178K/F 6 (CS41783F918) to 237K/F 6 (CS42373F911)		1A	2A
		6. Change PR65 from 196K/F 6 (CS41963F916) to 249K/F 6 (CS42493F914)		1A	2A
		Page34 : 1. Change PQ27/PQ22 from TPC8023-H(BAM80230000) to A01414 (BAM14140001)		1A	2A
	2. Change PQ28/PQ23 from TPC8019-H (BAM80190000) to A01412 (BAM14120000)		1A	2A	
	3. Change PQ11 from 0.0220/50V 6 (CH3226K1901) to 0.0330/50V 6 (CH3336J1900)		1A	2A	
	Page35 : 1. Change PQ2 from TPC8023-H (BAM80230000) to A01414 (BAM14140001)		1A	2A	
	2. Change PQ3 from TPC8019-H (BAM80190000) to A01412 (BAM14120000)		1A	2A	
	Page36 : 1. Change PQ41 from TPC8023-H (BAM80230000) to A01414 (BAM14140001)		1A	2A	
	2. Change PQ37 from TPC8019-H (BAM80190000) to A01412 (BAM14120000)		1A	2A	
	3. Change PR81 from 62K/F 6 (CS42623F914) to 4.75K/F 6 (CS42753F919)		1A	2A	
	Page37 : 1. Change PR21 from 196K/F 4 (CS41962F801) to 200K/F 4 (CS42002F812)		1A	2A	
	2. Change PR24 from 1.43K/F 4 (CS21432F800) to 1.74K/F 4 (CS21742F800)		2A	3A	
3A		Page2 : no mount 0.1uF (C475/C492/C471)		2A	3A
		Page3 : no mount 0.1uF (C515)		2A	3A
		Page4 : remove 0 ohm (R486/R390/R402/R159), and connect them directly		2A	3A
		Page12 : 1. remove 0 ohm (R498/R249/R487), and connect them directly		2A	3A
		Swap Main HDD to port-0, and 2nd HDD to port-4		2A	3A
		Page13 : remove 0 ohm (R198), and connect them directly		2A	3A
		Swap USB port2 to external USB, and port-7 to Cardreader		2A	3A
		Page14 : remove 0 ohm (R186/R185/R466/R235/R506), and connect them directly.		2A	3A
		no mount 0.1uF (C170/C448)		2A	3A
		Page16 : no mount 0.1uF (C301/C552)		2A	3A
	Page17 : reserve 0 ohm (R626) from MDM to EC (EC_THERM#)		2A	3A	
	no mount 0.1uF (C489)		2A	3A	
	Page18 : Change L67/7/8 to BLM18BA4708N1D		2A	3A	
	Change U4 to AL004280001 (AM04280-4) part		2A	3A	
	Remove 0 ohm (R22), and connect directly		2A	3A	
	Change CN3 to DFWF40MR000 for SMT request		2A	3A	
	Change R42 from 330 ohm to 180 ohm (CS11802B15)		2A	3A	
	Page19 : Use 100 ohm (R619/R620/R621/R622) and 10uF (C656/C657/C658/C659) for HDMI EMI request		2A	3A	
	Reserve C662/Q43/Q44/R119/R126, and bypass 0ohm (R627/R628)		2A	3A	
	Page20 : remove 0ohm (R5/R9/R357) and connect directly		2A	3A	
	Page21 : Change L17/2 (BAM180G1810N1D) to increase current rating		2A	3A	
	Change transformer to GST-5009		2A	3A	
	Change R13-R16 from 75ohm 0402 to 0805 size		2A	3A	
	no mount 0.1uF (C250)		2A	3A	
	Page22 : Swap LAN LED color connect (green: linking/orange/active)		2A	3A	
	Remove R296/R292/R328/R42/R298 and connect directly		2A	3A	
	no mount 0.1uF (C247/C270/C268)		2A	3A	
	Page23 : Change main (CN27) and 2nd (CN30) HDD footprint for M/E request		2A	3A	
	no mount 0.1uF (C532/C535/C260/C261/C440/C441)		2A	3A	
	Page24 : Change 0.1uF to 0.01uF (C630/C547/C317/C46/C661/C663/C314/C314/C556/C373/C451/C180)		2A	3A	
	Page25 : remove 0ohm (R74), and connect directly		2A	3A	
	Page26 : remove 0ohm (R74), and connect directly		2A	3A	
	Page27 : no mount 0.1uF (C281/C198/C279)		2A	3A	
	Page28 : Add AC-IN LED-on function (C48/Q50)		2A	3A	
	Add PWMLD/SUSLED function on Power/B (Q47/Q49/R624/R625)		2A	3A	
	Change R47/R49 from 0ohm to 100ohm for synaptic MMB		2A	3A	
	Page29 : Change L27, C520 from (AM04280-4) to (AM04280-4) per design team suggestion		2A	3A	
	Change e-SATA connector (CN22)		2A	3A	
	Update incorrect hole29/hoes4 footprint		2A	3A	
	Page30 : no mount 33pF (C33/C34)		2A	3A	
	Remove L24/L25/L26 and connect directly		2A	3A	
	no mount 0.1uF (C60/C65/C400)		2A	3A	
	Page31 : Change SW1 to short-pad (G3) for easy power-on		2A	3A	
	Change U38 to everlight part (IRM-V538-TR1)		2A	3A	
3B		Page5 : update NB p/n to AJSLB940T04 (GM45), AJSLB970T06 (PM45)		3A	3B
		Page6 : remove 0 ohm (R167), and connect them directly		3A	3B
		Page10 : Add 10uF capacitor (C549/C393) for CRT flicker issue		3A	3B
		Page12 : remove 0 ohm (R247), and connect them directly		3A	3B
		update SB p/n to AJSLB900T03		3A	3B
		Page14 : Add panel_ID0 (GPIO19)/1 (GPIO20) on SB, and pull-up 10Kohm (R629/R630) to +3V near LCD connector (CN3)		3A	3B
		Change Board_ID2 to GPIO21, and Board_ID3 to GPIO22		3A	3B
		Remove R516		3A	3B
		Page17 : no mount 4.7uF capacitor (C481)		3A	3B
		remove 0 ohm (R176/R472), and connect directly		3A	3B
	delete no-dock CRT resistor, no mount 0.1uF (C49)		3A	3B	
	remove 0 ohm (R617/R18), and connect directly for USB		3A	3B	
	Page19 : Add panel_ID0 (CN335) and panel_ID1 (CN330)		3A	3B	
	reserve 100 ohm (R634/R635/R636/R637)		3A	3B	
	Remove 0 ohm (R59/R64) and connect directly		3A	3B	
	Page20 : remove 0ohm (R355), and connect directly		3A	3B	
	Page21 : delete no-dock LAN resistor		3A	3B	
	Change R344/R352 to 220 0805 size for RMA request		3A	3B	
	Page22 : Remove RP11/RP10/R545 and connect directly		3A	3B	
	Reserve Q51 and bypass 0ohm (R631)		3A	3B	
	Page23 : Add 10uF (C666) for TV		3A	3B	
	Page24 : Update new footprint (CN30) library issue		3A	3B	
	no mount 0.1uF (C591) and add 10uF (C593)		3A	3B	
	Change C601 from 4.7uF to 10uF		3A	3B	
	Page25 : Change MUTEH function circuit to AND gate (U42), and reserve bypass 0ohm (R638)		3A	3B	
	remove 0 ohm bridge resistor (R540/R545/R552/R553/R559) to reduce noise		3A	3B	
	Change R570 from 20Kohm to 12.4Kohm for subwoofer gain issue		3A	3B	
	remove 0ohm (R575) and connect directly		3A	3B	
	Change C623 from AD080 to GND		3A	3B	
	Page26 : Change C646 (C627) from 7uF to 100uF directly		3A	3B	
	Page28 : Reserve C646 (C627) for MDM and Reserve +5V (R633)		3A	3B	
	Use +3V power (R632) for MDM and Reserve +5V (R633)		3A	3B	
	Add 1uF (C655) for +3V power		3A	3B	
	Page29 : Remove R45 and connect directly, reserve L61/C667 for EMI request		3A	3B	
	Remove 0ohm (R609/R610/R611/R612) and connect directly		3A	3B	
	Increase 0.1mm width for Hole28/33/30/35		3A	3B	
	Page30 : Change RP2 from +3VUS to +3VPCU for EC engineer suggestion		3A	3B	
	Remove 0ohm (RP7) and connect directly		3A	3B	
	Change 2.2uF to 10uF (C367)		3A	3B	
			3A	3B	
			3A	3B	

 Quanta Computer Inc. PROJECT : ZK2	DOC NO.	PROJECT MODEL :	ZK2	APPROVED BY :		DATE :	2008/06/27
	Change list	PART NUMBER :		DRAWING BY :		REVISION :	3B