

Compal Confidential

NAVD0 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII + NV OPTIMUS

2010-02-09

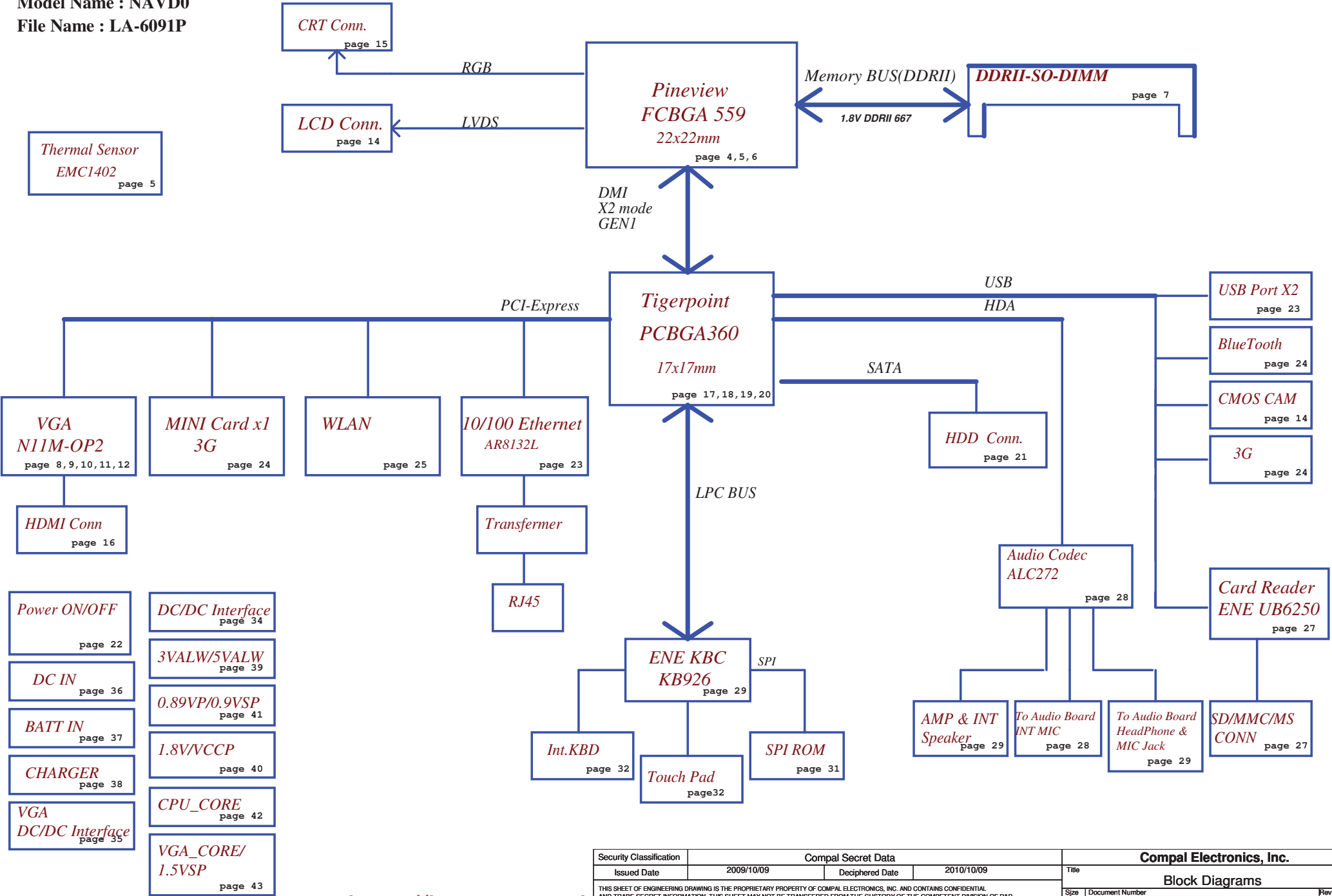
REV: 1.0

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				Date	Wednesday, March 03, 2010
				Sheet	1 of 46
				Rev	1.0
				Document Number	NAVD0 LA-6091P

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Model Name : NAVD0
File Name : LA-6091P

Clock Generator
CK505
page 13



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				Block Diagrams	
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				Date	Sheet
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89VS	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SIGNAL						
		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clck
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 31)

ID	BRD ID	Rb	Vab			
			Vab-Min	Vab-Typ	Vab-Max	
VCC		3.3V				
Ra		100K				
NAVD0	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAVE0	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

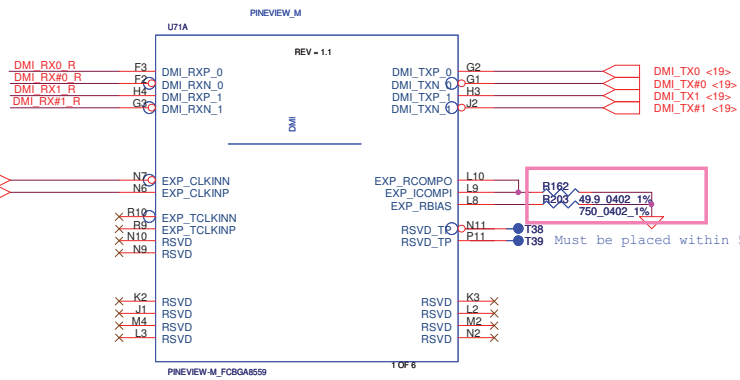
EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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				Notes List
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- <7> DDR_A_DQS[0..7]
- <7> DDR_A_D[0..63]
- <7> DDR_A_DM[0..7]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_MA[0..14]

- DDR_A_MA0 AH19
- DDR_A_MA1 AJ18
- DDR_A_MA2 AK18
- DDR_A_MA3 AK18
- DDR_A_MA4 AJ14
- DDR_A_MA5 AH14
- DDR_A_MA6 AK14
- DDR_A_MA7 AK12
- DDR_A_MA8 AH13
- DDR_A_MA9 AK12
- DDR_A_MA10 AK20
- DDR_A_MA11 AH12
- DDR_A_MA12 AJ11
- DDR_A_MA13 AJ24
- DDR_A_MA14 AJ10

- DDR_A_DQS_0 AD3
- DDR_A_DQS#0 AD2
- DDR_A_DM0 AD4
- DDR_A_DQ_0 AC4
- DDR_A_DO_1 AC1
- DDR_A_DQ_2 AC2
- DDR_A_DQ_3 AC2
- DDR_A_DQ_4 AB2
- DDR_A_DQ_5 AB3
- DDR_A_DQ_6 AE2
- DDR_A_DQ_7 AE3
- DDR_A_DQS_1 AB8
- DDR_A_DQS#1 AD7
- DDR_A_DM1 AA9
- DDR_A_DQ_8 AB6
- DDR_A_DQ_9 AB7
- DDR_A_DQ_10 AE5
- DDR_A_DQ_11 AA5
- DDR_A_DQ_12 AB5
- DDR_A_DQ_13 AB9
- DDR_A_DQ_15 AD6
- DDR_A_DQS_2 AD8
- DDR_A_DQS#2 AD10
- DDR_A_DM2 AE8
- DDR_A_DQ_16 AG8
- DDR_A_DQ_17 AG7
- DDR_A_DQ_18 AE9
- DDR_A_DQ_19 AG11
- DDR_A_DQ_20 AF7
- DDR_A_DQ_21 AF8
- DDR_A_DQ_22 AD11
- DDR_A_DQ_23 AE10
- DDR_A_DQS_3 AK5
- DDR_A_DQS#3 AK3
- DDR_A_DM3 AJ3
- DDR_A_DQ_24 AH1
- DDR_A_DQ_25 AJ2
- DDR_A_DQ_26 AK7
- DDR_A_DQ_27 AJ6
- DDR_A_DQ_28 AF3
- DDR_A_DQ_29 AH2
- DDR_A_DQ_30 AL5
- DDR_A_DQ_31 AJ6
- DDR_A_DQ_32 AG22
- DDR_A_DQ_33 AG21
- DDR_A_DQ_34 AE19
- DDR_A_DQ_35 AD22
- DDR_A_DQ_36 AG17
- DDR_A_DQ_37 AE19
- DDR_A_DQ_38 AD21
- DDR_A_DQ_39 AE26
- DDR_A_DQS_5 AE6
- DDR_A_DQS#5 AG27
- DDR_A_DM5 AJ27
- DDR_A_DQ_40 AE24
- DDR_A_DQ_41 AG25
- DDR_A_DQ_42 AD25
- DDR_A_DQ_43 AD24
- DDR_A_DQ_44 AC22
- DDR_A_DQ_45 AD27
- DDR_A_DQ_46 AE27
- DDR_A_DQ_47 AE27
- DDR_A_DQS_6 AE30
- DDR_A_DQS#6 AF29
- DDR_A_DM6 AF30
- DDR_A_DQ_48 AC31
- DDR_A_DQ_49 AG30
- DDR_A_DQ_50 AD30
- DDR_A_DQ_51 AD29
- DDR_A_DQ_52 AJ30
- DDR_A_DQ_53 AJ29
- DDR_A_DQ_54 AE29
- DDR_A_DQ_55 AD28
- DDR_A_DQS_7 AB27
- DDR_A_DQS#7 AA27
- DDR_A_DM7 AB26
- DDR_A_DQ_56 AA24
- DDR_A_DQ_57 AB25
- DDR_A_DQ_58 W24
- DDR_A_DQ_59 W22
- DDR_A_DQ_60 AB24
- DDR_A_DQ_61 AB23
- DDR_A_DQ_62 AA23
- DDR_A_DQ_63 W27

- <7> DDR_A_WE#
- <7> DDR_A_CAS#
- <7> DDR_A_RAS#
- <7> DDR_A_BS0
- <7> DDR_A_BS1
- <7> DDR_A_BS2

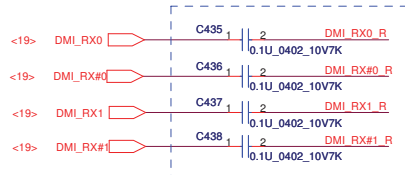
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- <7> DDR_CS#1
- <7> DDR_CKE0
- <7> DDR_CKE1

- <7> M_ODT0
- <7> M_ODT1

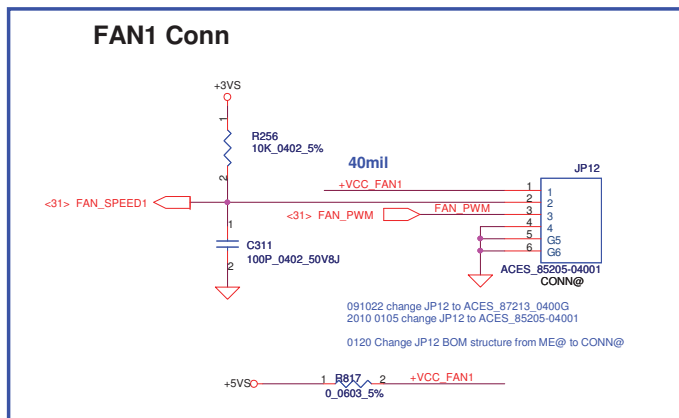
- <7> M_CLK_DDR0
- <7> M_CLK_DDR#0
- <7> M_CLK_DDR1
- <7> M_CLK_DDR#1

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- DDR_A_CAS# AJ22
- DDR_A_RAS# AK21
- DDR_A_BS_0 AJ20
- DDR_A_BS_1 AH20
- DDR_A_BS_2 AK11
- DDR_A_CS#_0 AH22
- DDR_A_CS#_1 AK25
- DDR_A_CS#_2 AJ25
- DDR_A_CS#_3 AK25
- DDR_A_CKE_0 AH10
- DDR_A_CKE_1 AH9
- DDR_A_CKE_2 AK10
- DDR_A_CKE_3 AJ8
- M_ODT0 AK24
- M_ODT1 AK24
- M_ODT1 AK27
- M_CLK_DDR0 AC15
- M_CLK_DDR#0 AE15
- M_CLK_DDR1 AD13
- M_CLK_DDR#1 AC13
- DDR_A_CK_0 AD15
- DDR_A_CK_1 AF13
- DDR_A_CK_2 AG13
- DDR_A_CK_3 AD15
- DDR_A_CK_3# AD15
- DDR_A_CK_4 AF13
- DDR_A_CK_4# AG13

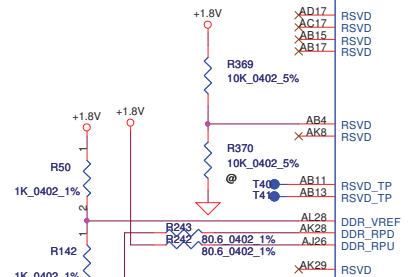
091105 change CPU Part Number to SA00003M870



Close to CPU

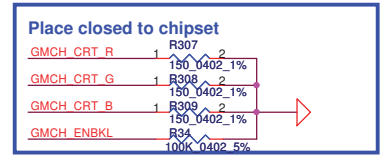
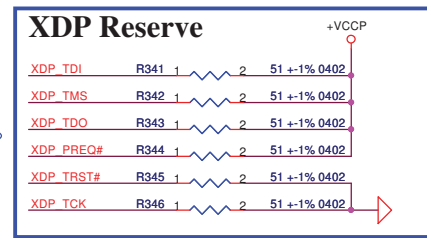
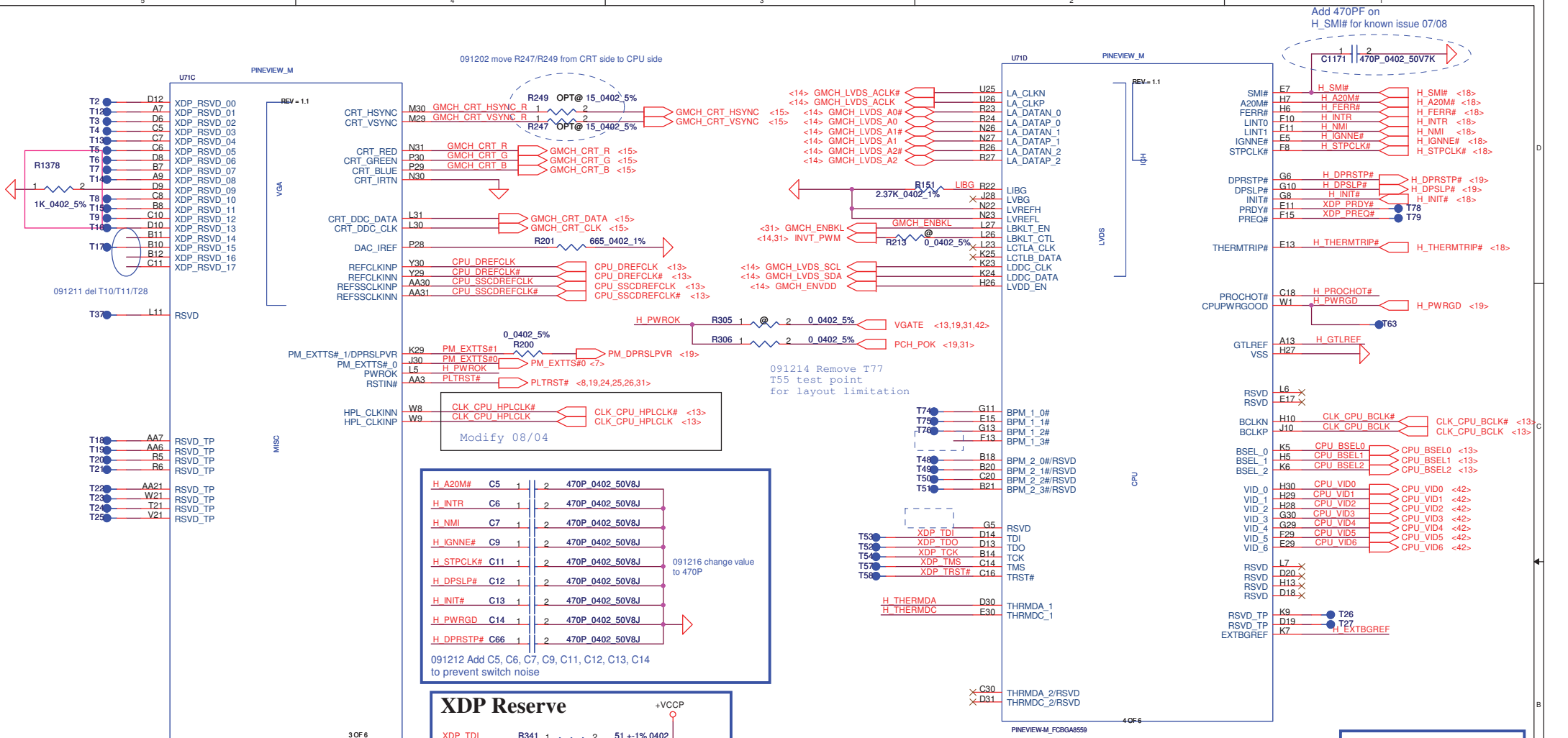


091022 change JP12 to ACES_87213_0400G
2010 0105 change JP12 to ACES_85205-04001
0120 Change JP12 BOM structure from ME@ to CONN@

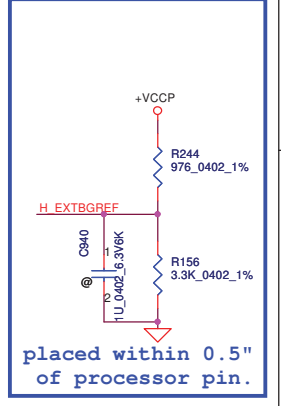
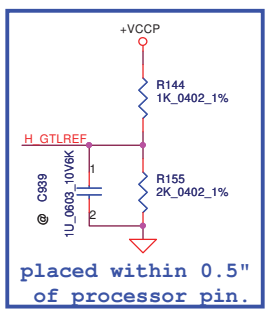
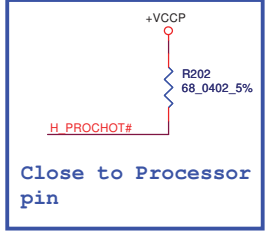
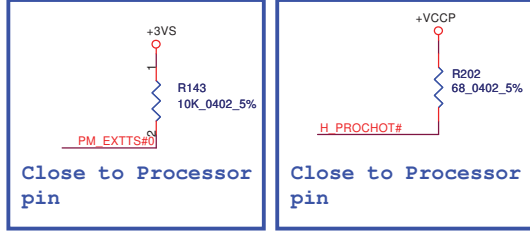
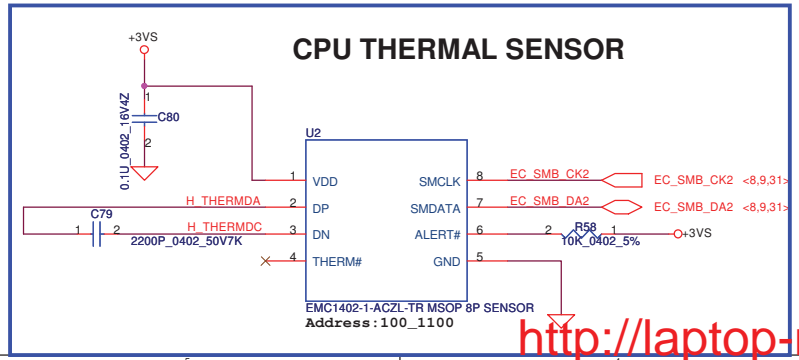


091105 change CPU Part Number to SA00003M870

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				Pineview(1/3)	
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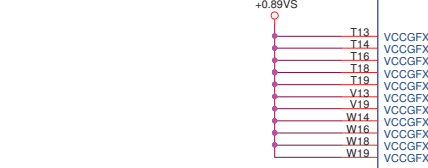
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



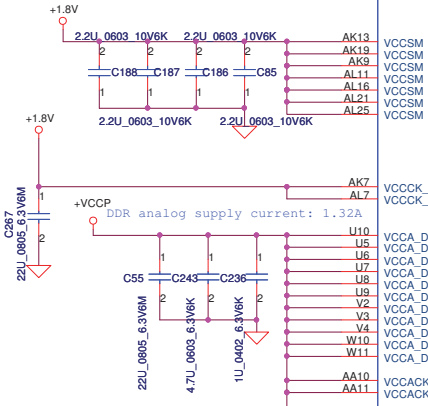
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Title Pineview(2/3)			
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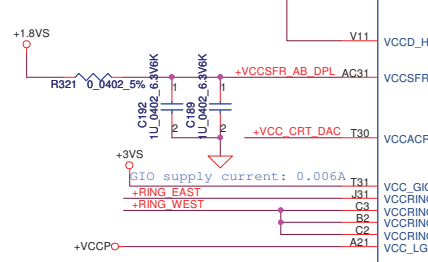
GFX supply current: 1.38A
Sustained GFX supply current: 1.05A



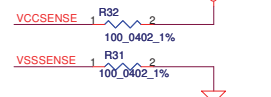
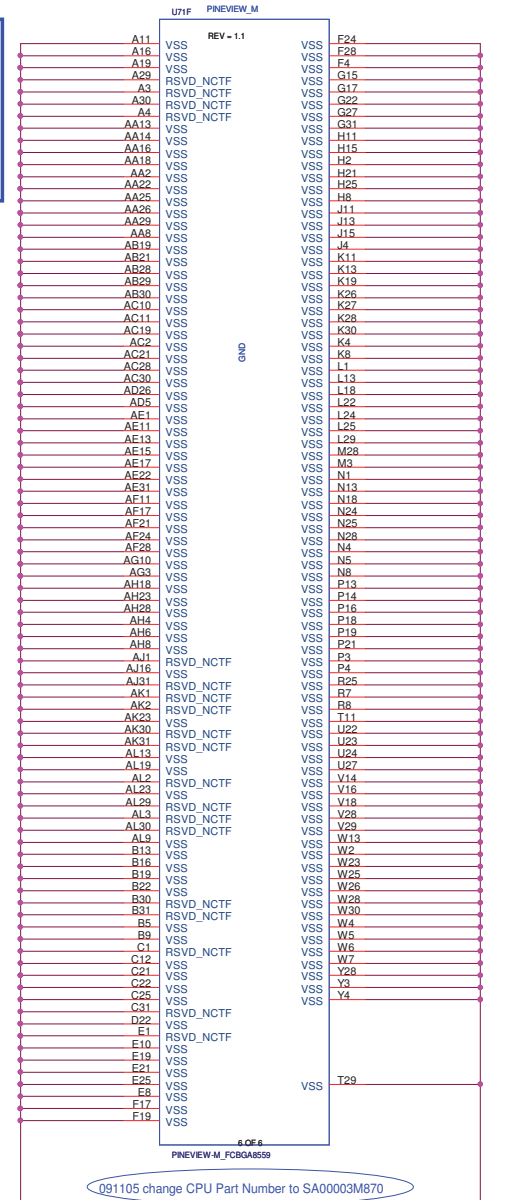
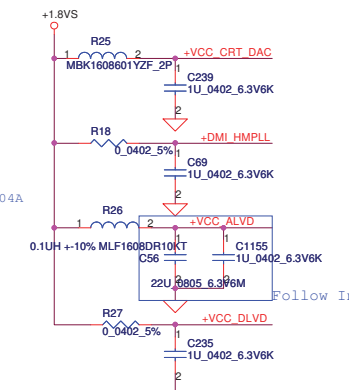
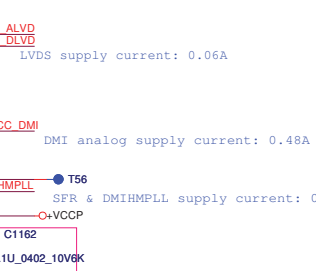
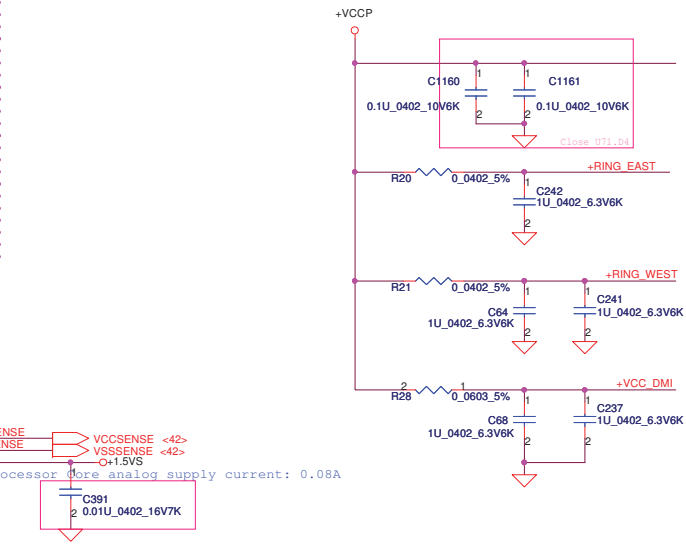
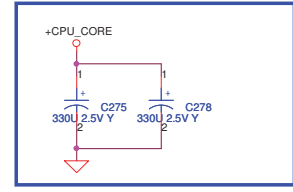
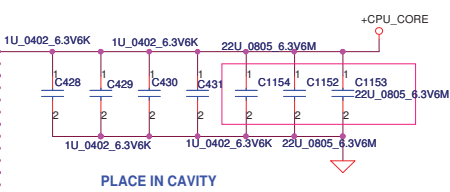
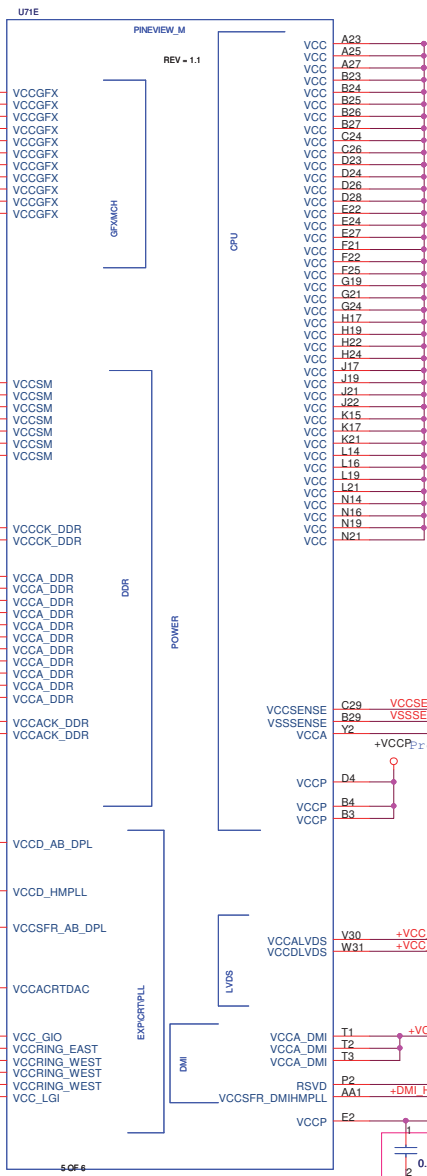
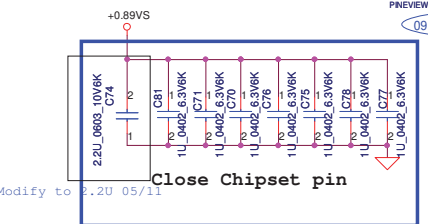
DDR supply current 2.27A



Display PLL SFR and CRT DAC supply current: 0.154A



DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A



Q91105 change CPU Part Number to SA00003M870

Follow Intel check list change to 22uF 06/06

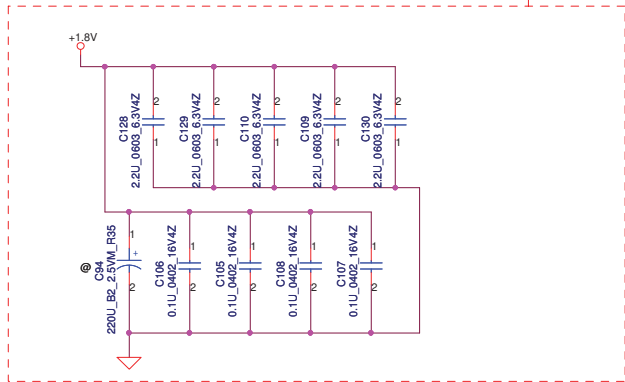
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Compal Electronics, Inc.			
Title Pineview(3/3)			
Size Custom	Document Number NAVDO LA-6091P	Rev 1.0	
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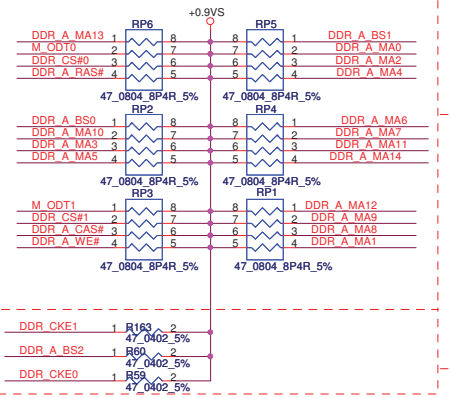
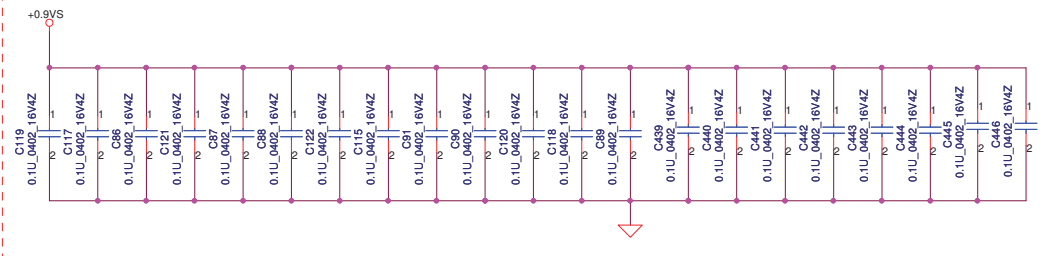
<http://laptop-motherboard-schematic.blogspot.com/>

- <-> DDR_A_DOS#[0..7]
- <-> DDR_A_D[0..63]
- <-> DDR_A_DM[0..7]
- <-> DDR_A_DOS[0..7]
- <-> DDR_A_MA[0..14]

Layout Note:
Place near JDIM1



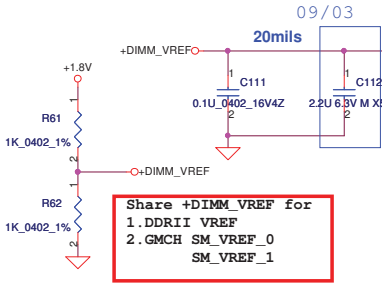
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place this resistor closely DIMMA, all trace length < 750 mil

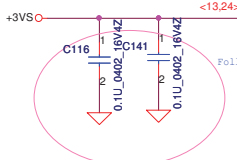
091204 swap nets for layout

Layout Note:
Place this resistor closely DIMMA, all trace length Max=1.3"

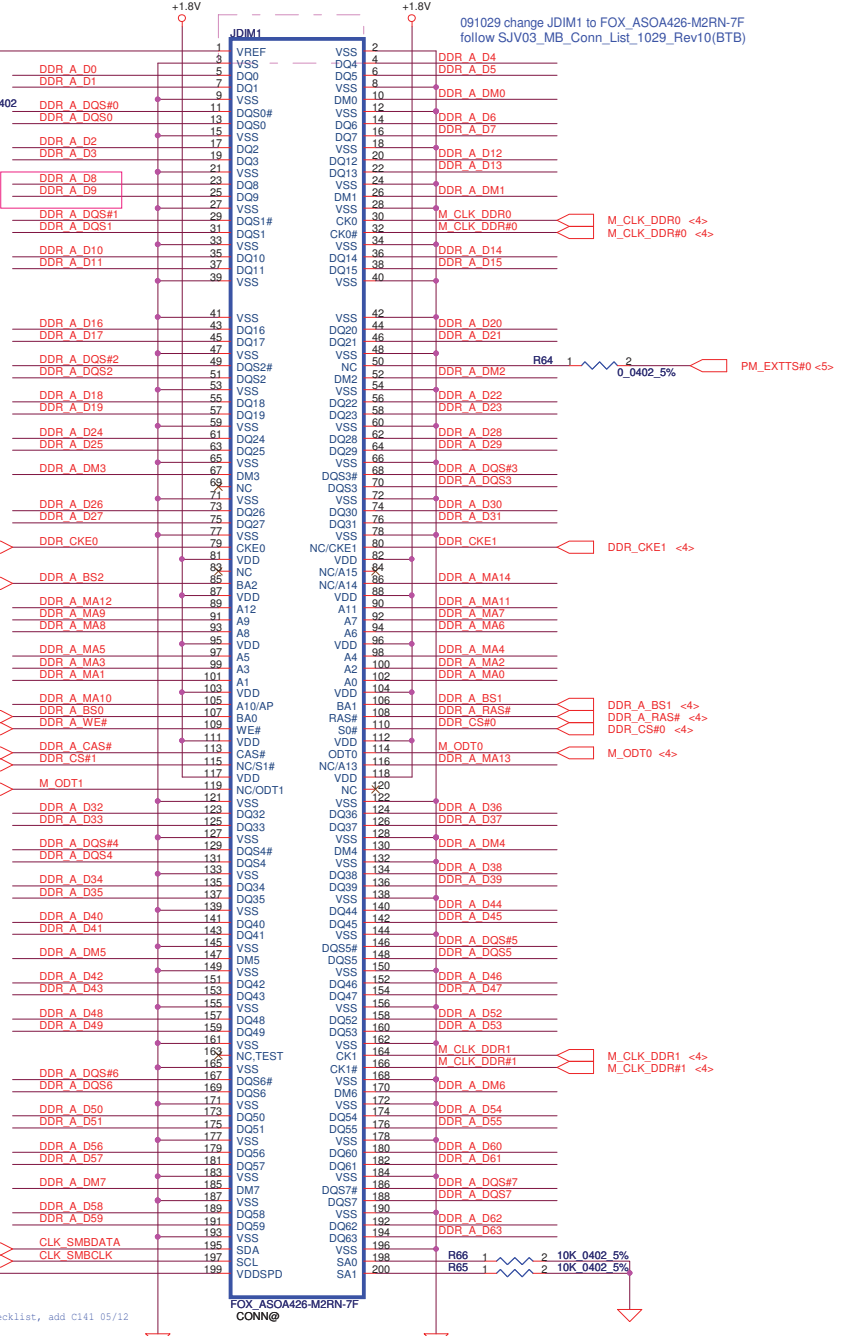


Share +DIMM_VREF for
1. DDR I VREF
2. GMCH SM_VREF_0
SM_VREF_1

- <-> DDR_CKE0
- <-> DDR_A_BS2
- <-> DDR_A_BS0
- <-> DDR_A_WE#
- <-> DDR_A_CAS#
- <-> DDR_CS#1
- <-> M_ODT1



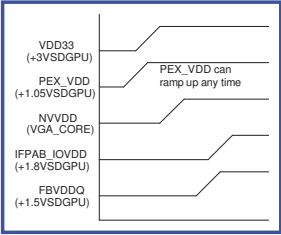
<13.24> CLK_SMBDATA
<13.24> CLK_SMBCLK



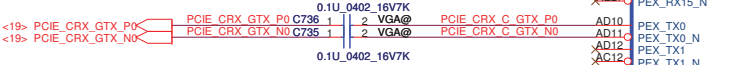
DIMMA

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Issued Date	2009/10/09	Deciphered Date	2010/10/09	DDR II-SODIMMA	
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<small>FOX_AS0A426-M2RN-7F CONN@</small>				Document Number	NAVDO LA-6091P
<small>Follow Intel Layout checklist, add C141 05/12</small>				Date	Wednesday, March 03, 2010
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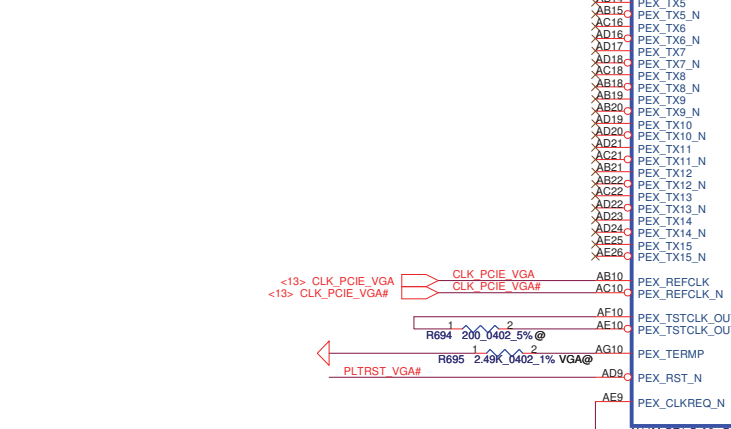
DIS ONLY



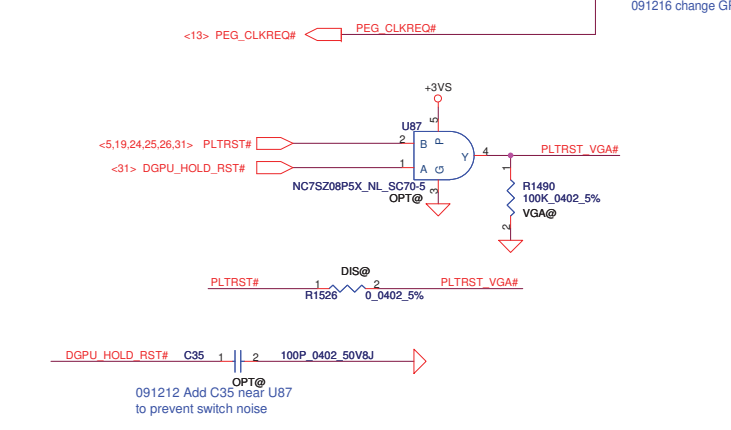
DIS@



PCIEXPRESS

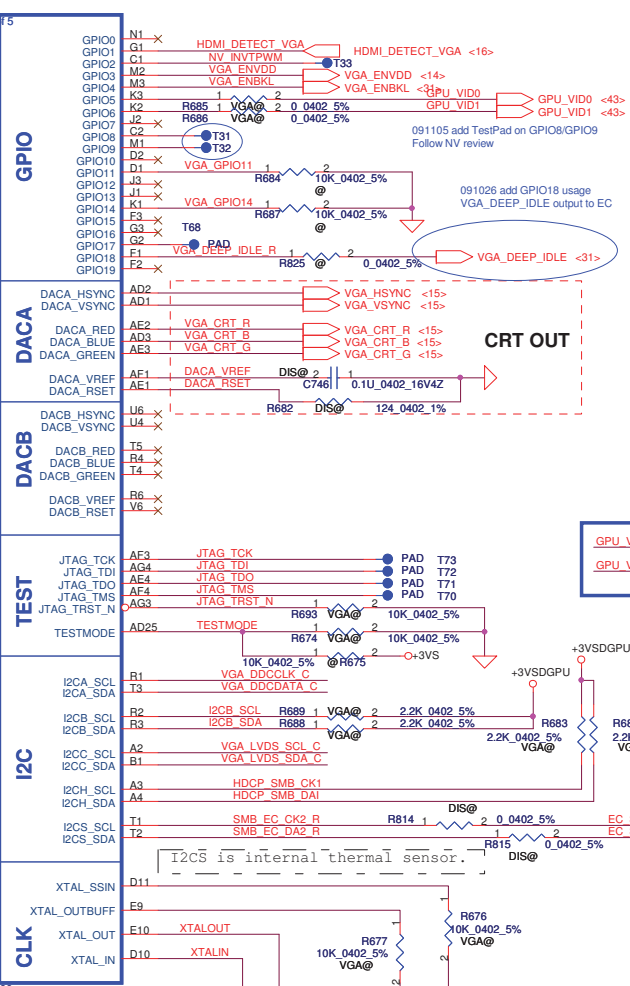


CLK



Part 1 of 5

AE10	PEX_RX0
AE12	PEX_RX0_N
AG12	PEX_RX1
AE13	PEX_RX1_N
AE14	PEX_RX2
AE13	PEX_RX2_N
AE15	PEX_RX3
AE15	PEX_RX3_N
AG15	PEX_RX4
AG16	PEX_RX4_N
AE18	PEX_RX5
AE16	PEX_RX5_N
AE18	PEX_RX6
AE18	PEX_RX6_N
AG18	PEX_RX7
AE19	PEX_RX7_N
AE19	PEX_RX8
AE21	PEX_RX8_N
AE21	PEX_RX9
AE21	PEX_RX9_N
AG21	PEX_RX10
AG22	PEX_RX10_N
AE22	PEX_RX11
AE22	PEX_RX11_N
AG22	PEX_RX12
AG24	PEX_RX12_N
AG24	PEX_RX13
AG24	PEX_RX13_N
AG25	PEX_RX14
AG25	PEX_RX14_N
AG26	PEX_RX15
AG26	PEX_RX15_N
AD10	PEX_TX0
AD11	PEX_TX0_N
AD12	PEX_TX1
AD12	PEX_TX1_N
AB11	PEX_TX2
AB12	PEX_TX2_N
AD13	PEX_TX3
AD13	PEX_TX3_N
AD14	PEX_TX4
AD14	PEX_TX4_N
AD15	PEX_TX5
AD15	PEX_TX5_N
AC18	PEX_TX6
AD16	PEX_TX6_N
AD17	PEX_TX7
AD18	PEX_TX7_N
AD18	PEX_TX8
AD18	PEX_TX8_N
AB19	PEX_TX9
AD19	PEX_TX9_N
AD19	PEX_TX10
AD20	PEX_TX10_N
AD21	PEX_TX11
AD21	PEX_TX11_N
AB22	PEX_TX12
AD22	PEX_TX12_N
AD22	PEX_TX13
AD23	PEX_TX13_N
AD24	PEX_TX14
AD24	PEX_TX14_N
AE25	PEX_TX15
AE26	PEX_TX15_N
AB10	PEX_REFCLK
AC10	PEX_REFCLK_N
AF10	PEX_TSTCLK_OUT
AE10	PEX_TSTCLK_OUT_N
AG10	PEX_TEMP
AD9	PEX_RST_N
AE9	PEX_CLKREQ_N

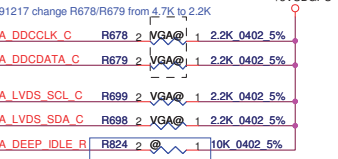
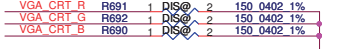


Device ID	Device ID
N10M-GS (40nm)	0x0A74
N11M-GE1/LP1 (40nm)	0x0A7D

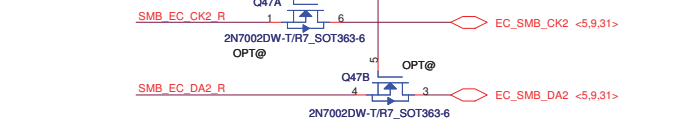
GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.0V	P0

Ball Name	GB1-N11x Normal Function	Function Description
GPIO0	General Purpose	
GPIO1	HPD-C	Hot Plug detect for IFP link C
GPIO2	LCD0_BL_PWM	Panel Backlight Brightness (PWM capable)
GPIO3	LCD0_VDD	Panel power enable
GPIO4	LCD0_BL_EN	Panel Backlight on/off (PWM Capable)
GPIO5	GPU_VID0	GPU_VID0
GPIO6	GPU_VID1	GPU_VID1
GPIO7	GPU_VID2	GPU_VID2
GPIO8	OVERT	Thermal Catastrophic Overtemp
GPIO9	ALERT	Thermal Alert

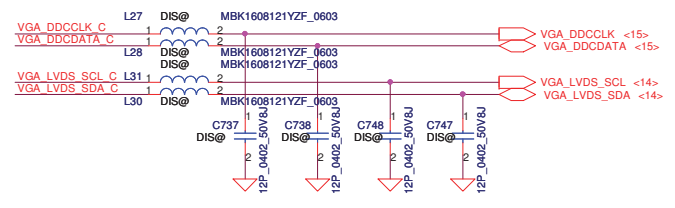
Ball Name	GB1-N11x Normal Function	Function Description
GPIO10	MEM_VREF	Memory VREF switch
GPIO11	SLI_SYNC	SLI raster sync
GPIO12	PWR_LEVEL	AC power detect input
GPIO13	MEM_VID	MEM_VID or Power supply Control
GPIO14	PWR_CTRL1	
GPIO15	HPD-E	Power supply control
GPIO16	FAN_PWM	Hot plug detect for IFP link E
GPIO17	Reserved	Programmable Fan control
GPIO18	Reserved	
GPIO19	HPD-D	Hot plug detect for IFP link D



091022 follow NV OPTIMUS D.G.



100112 change Q47 P/N from SB00000AR00 to SB00000DH00

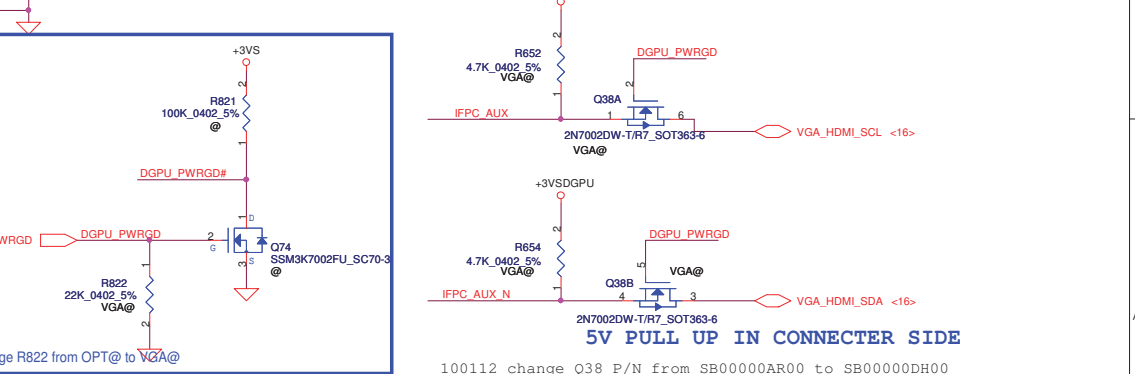
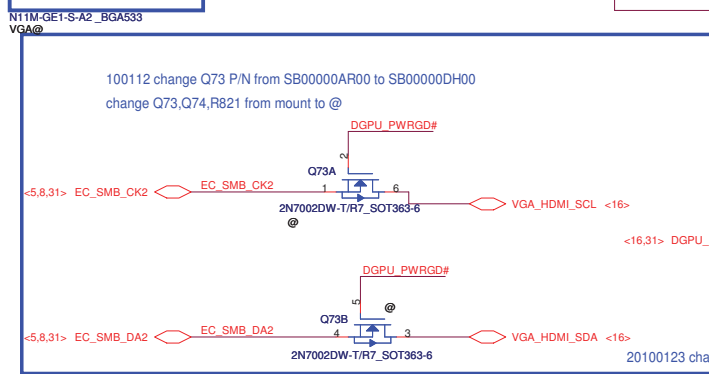
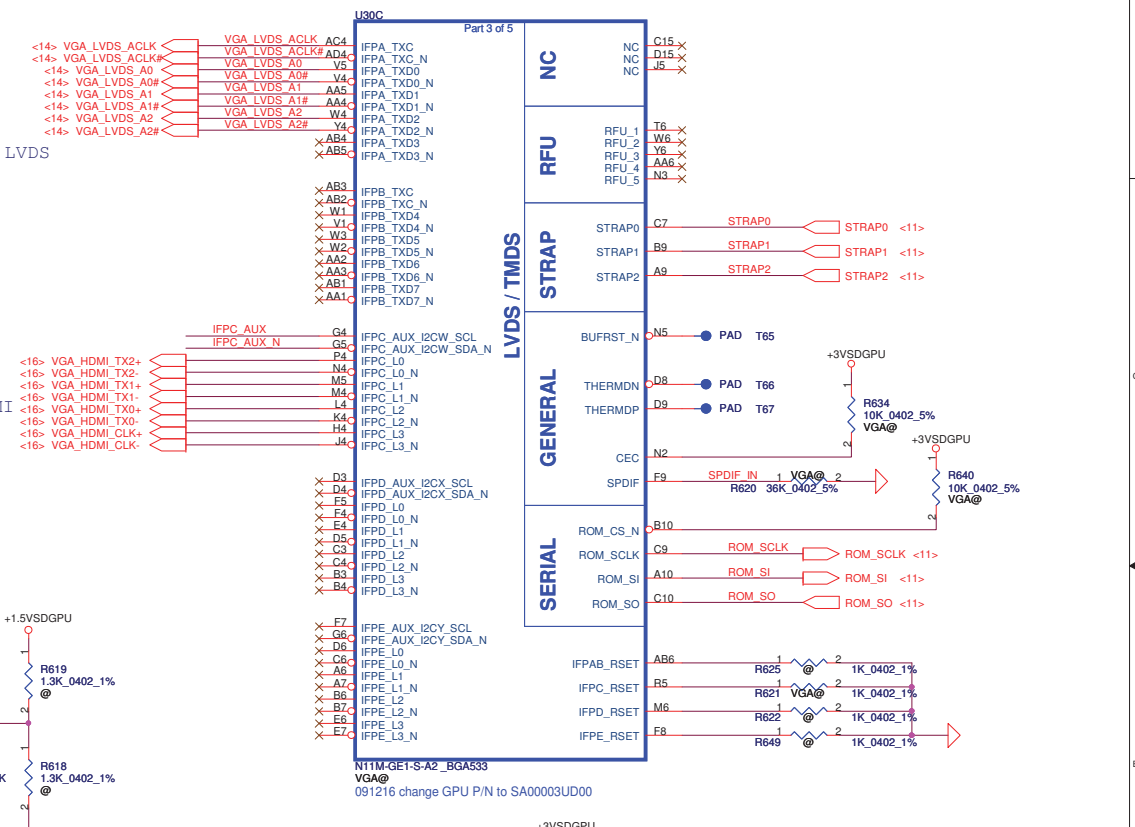
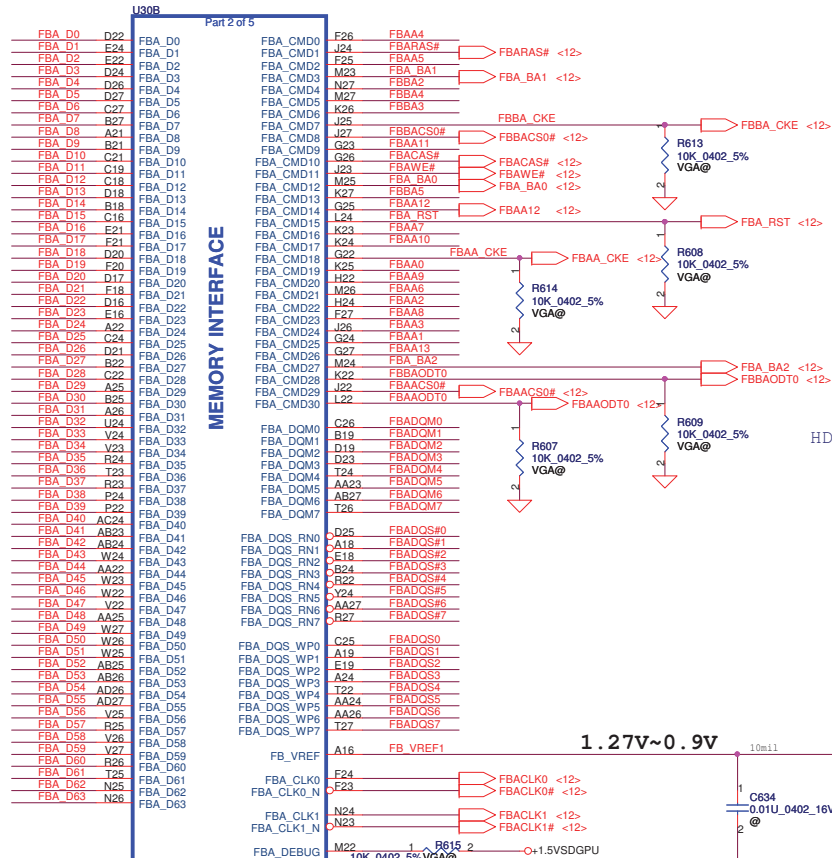
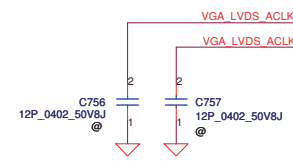


Security Classification	Compal Secret Data
Issued Date	2009/10/09
	Deciphered Date
	2010/10/09

Compal Electronics, Inc.		
Title	Document Number	Rev
N11M-OP2 PCIE,GPIO,CLK		1.0

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Date	Wednesday, March 03, 2010	Sheet	8	of	46
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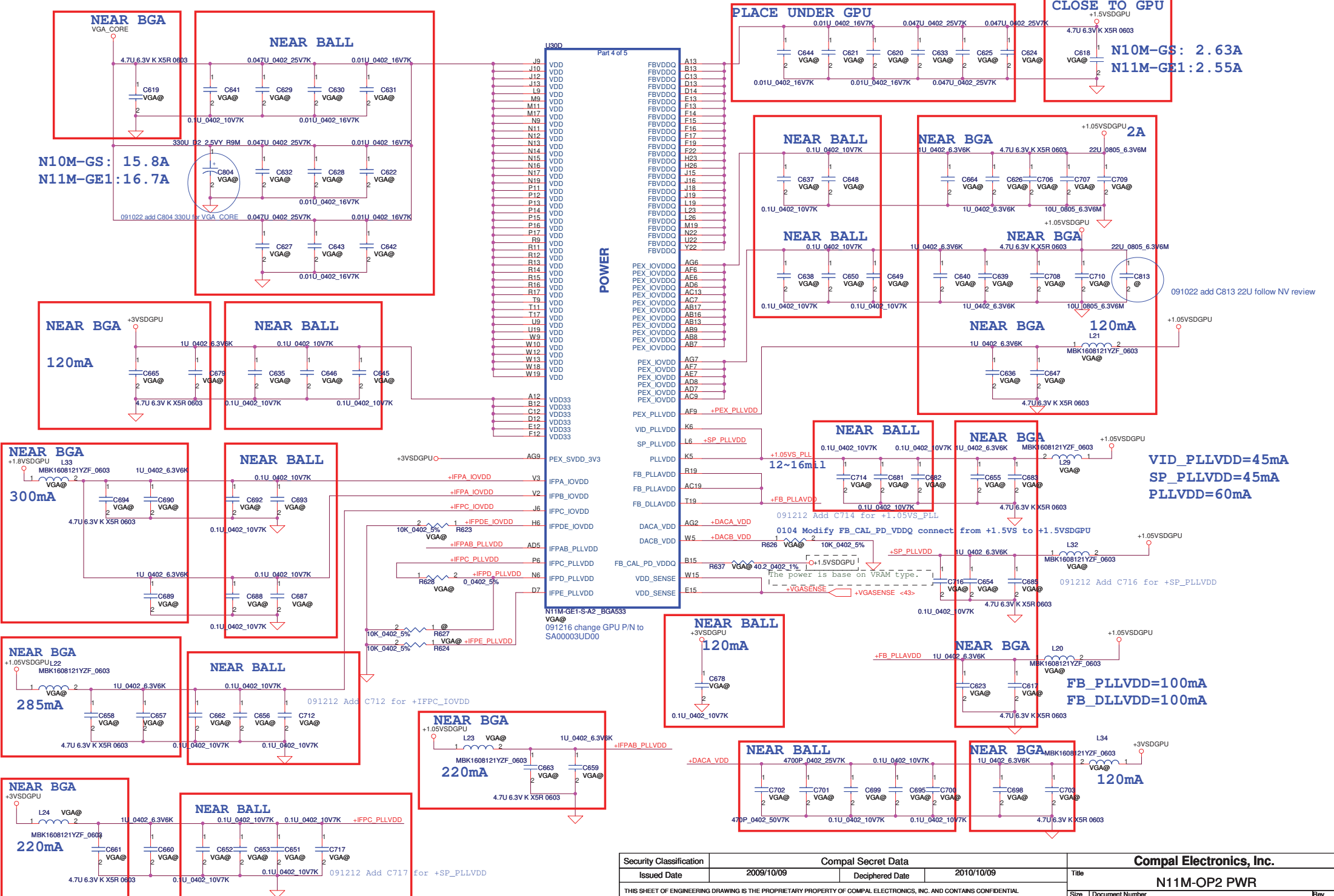


091022 add for OPTIMUS

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		2010/10/09

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Compal Electronics, Inc.		
Title		
N11M-OP2 LVDS,Memory Bus		
Size	Document Number	Rev
B		1.0
Date:	Wednesday, March 03, 2010	Sheet 9 of 46



N10M-GS: 15.8A
N11M-GE1: 16.7A

N10M-GS: 2.63A
N11M-GE1: 2.55A

VID_PLLVDD=45mA
SP_PLLVDD=45mA
PLLVDD=60mA

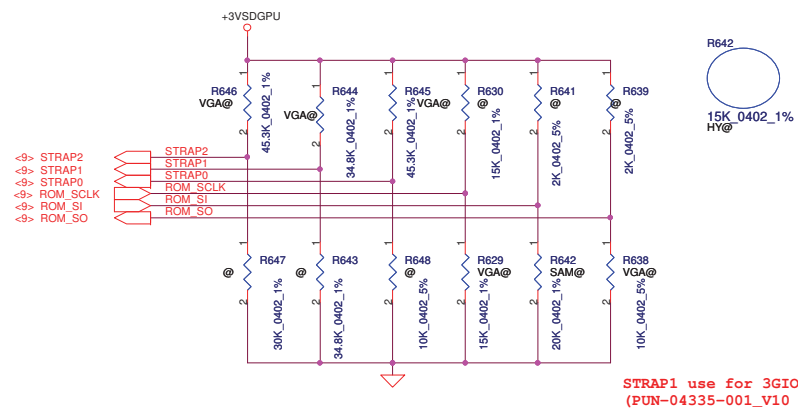
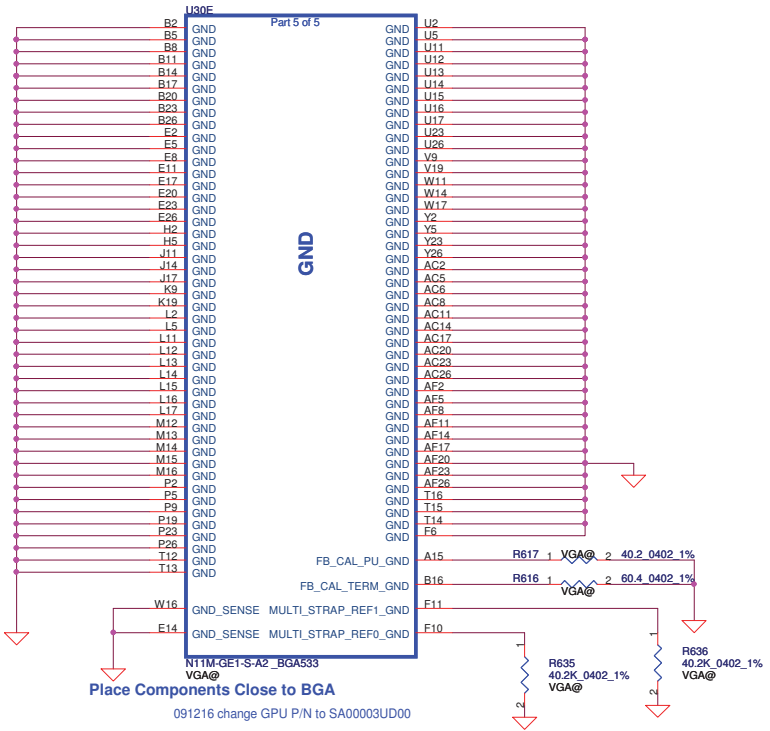
FB_PLLVDD=100mA
FB_DLLVDD=100mA

120mA

120mA

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title	N11M-OP2 PWR
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				Customer	NAVDO LA-6091P
				Rev	1.0

A total of 8 signals are required for GBI strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default) K4W1G1646E-HC12 64Mx16	PD 10K	PD 15K	PD 20K	PU 45K	PU 35K	PU 45K
	Hynix 800MHz H5TQ1G63BFR-12C 64Mx16	PD 10K	PD 15K	PD 15K	PU 45K	PU 35K	PU 45K
				X76			

Resistor Values	Pull-up to VDD	Pull-down to GND
5Kohm	1000	0000
10Kohm	1001	0001
15Kohm	1010	0010
20Kohm	1011	0011
25Kohm	1100	0100
30Kohm	1101	0101
35Kohm	1110	0110
45Kohm	1111	0111

SUB_VENDOR		XCLK_417	
0 *	No VBIOS ROM (Default)	0 *	277MHz (Default)
1	BIOS ROM is present	1	Reserved
Panel USER Straps		SMBUS_ALT_ADDR	
User [3:0]		0 *	0x9E (Default)
EDID used *	Customer defined	1	0x9C (Multi-GPU usage)
FB_0_BAR_SIZE		VGA_DEVICE	
0 *	256MB (Default)	0	3D Device
1	Reserved	1 *	VGA Device (Default)
PEX_PLL_EN_TERM		3GIO_PADCFG	
0 *	Disable (Default)	3GIO_PADCFG [3:0]	
1	Enable	0110 *	Notebook Default
SLOT_CLOCK_CFG			
0 *	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		

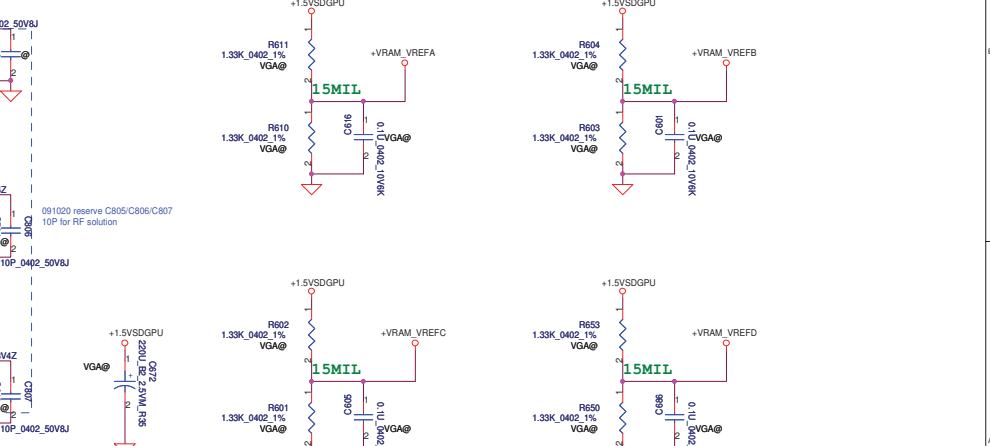
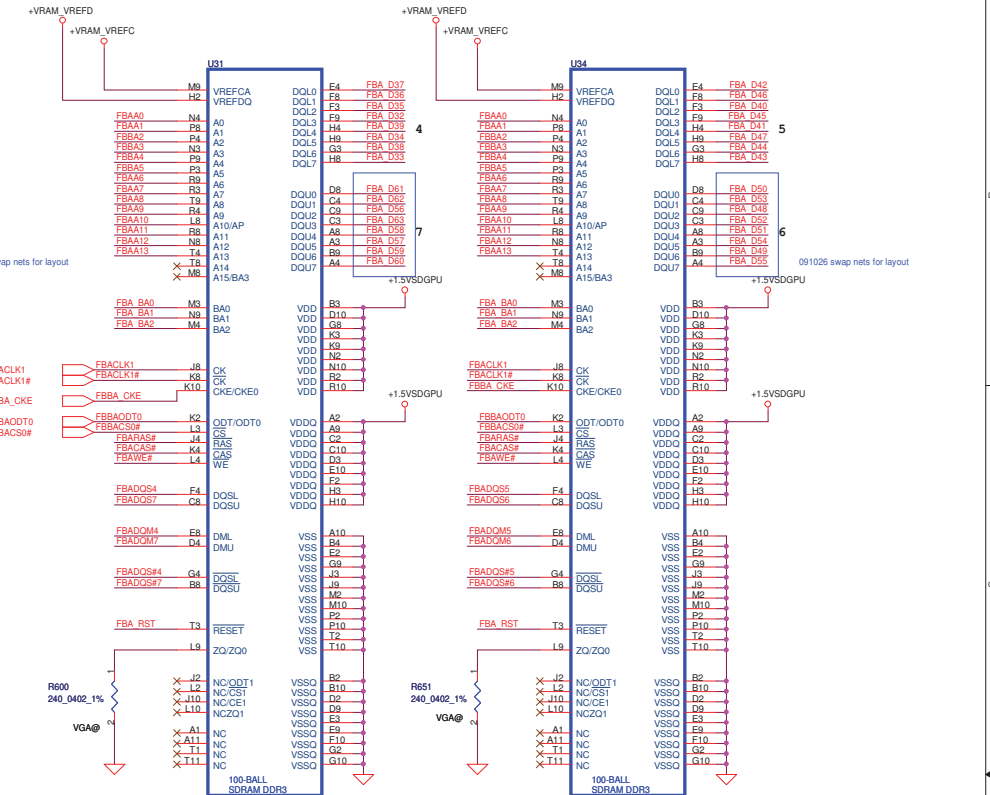
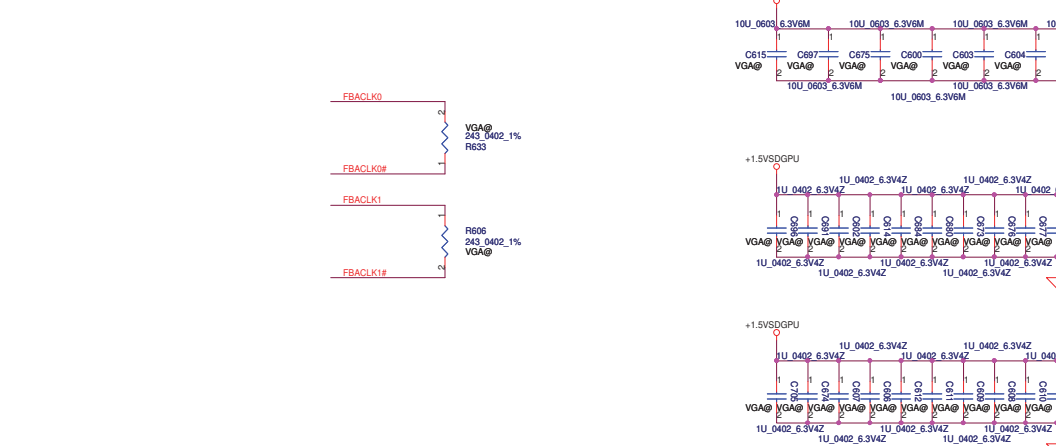
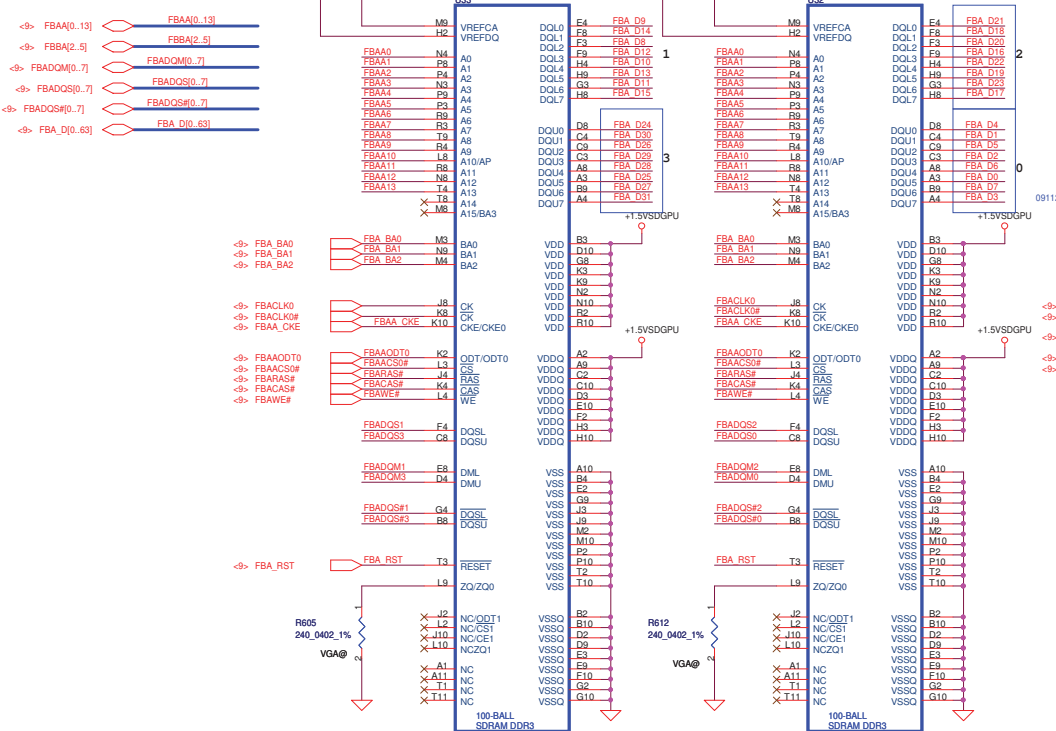
Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

<http://laptop-motherboard-schematic.blogspot.com/>

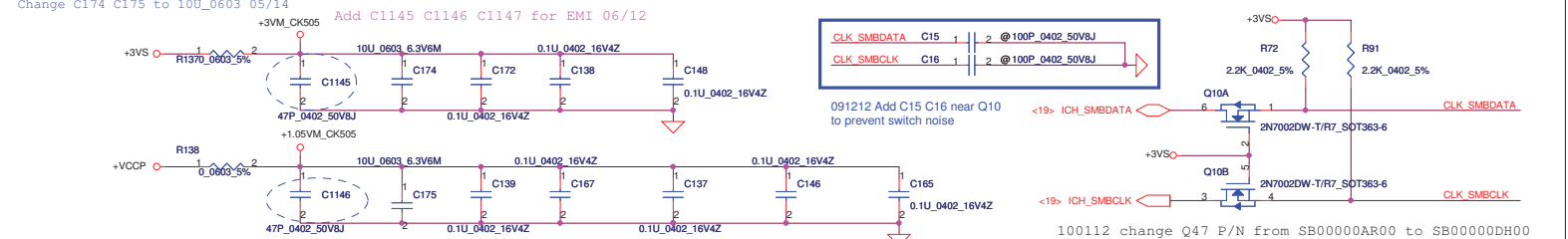
N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



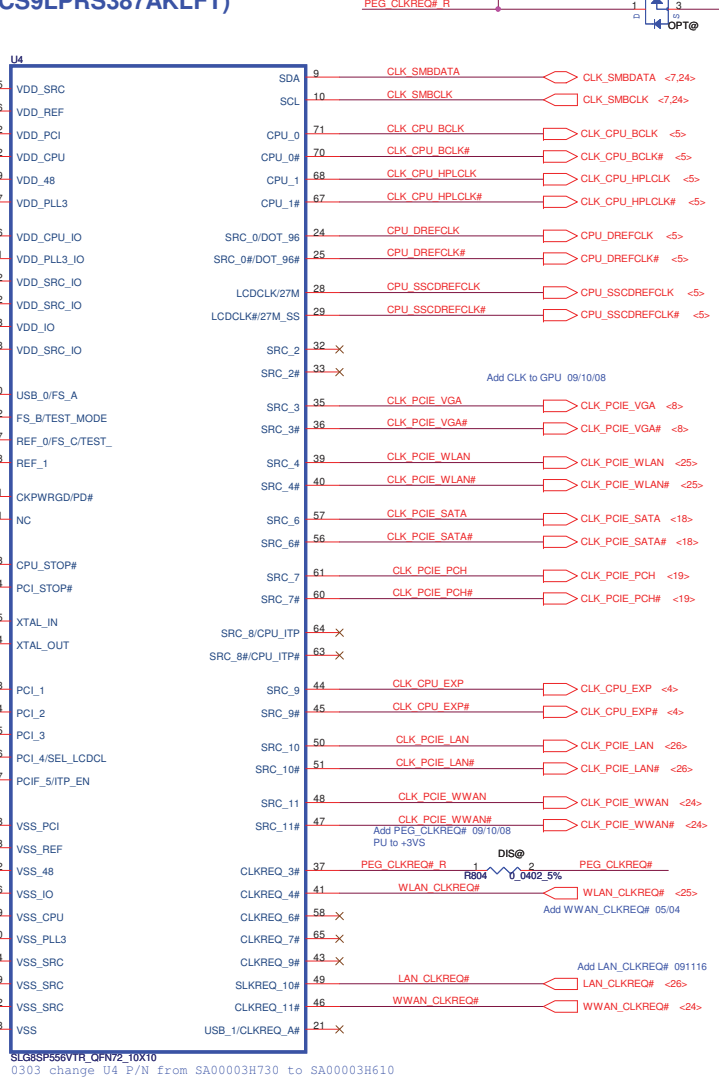
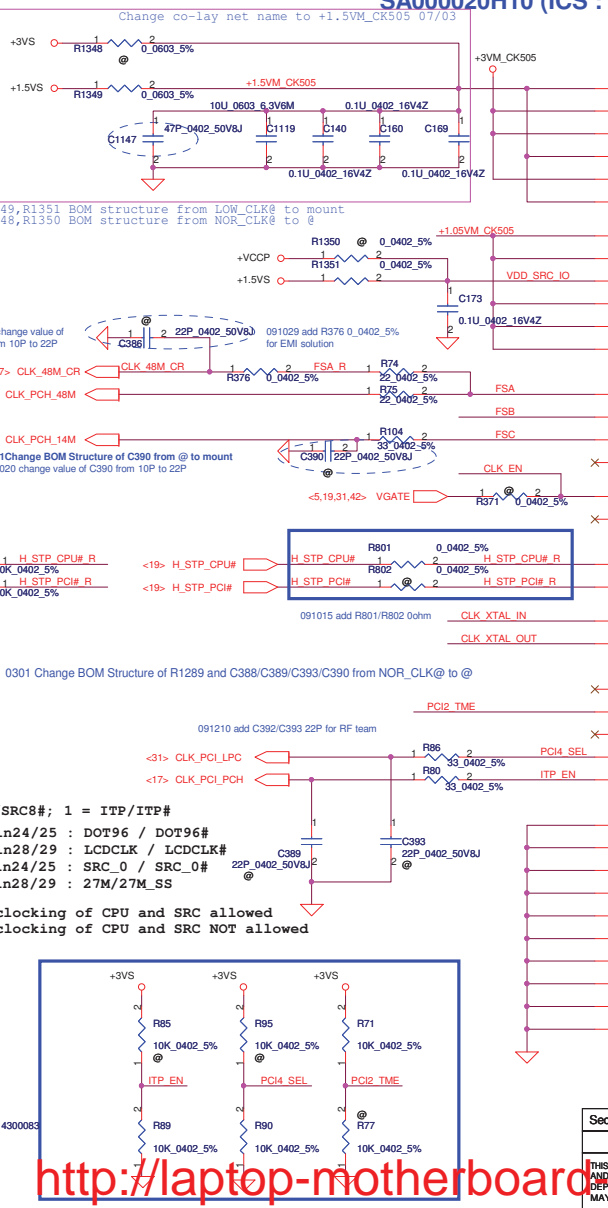
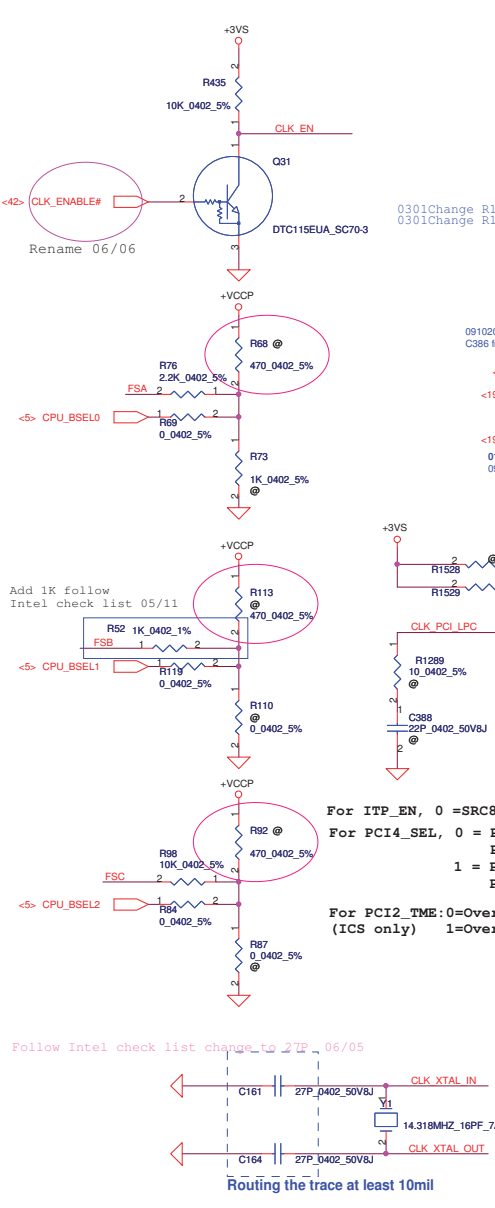
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Size C	Document Number	NAVD0 LA-6091P		Rev 1.0
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<http://laptop-motherboard.com/>

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

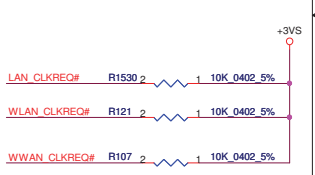


SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)



SRC PORT LIST

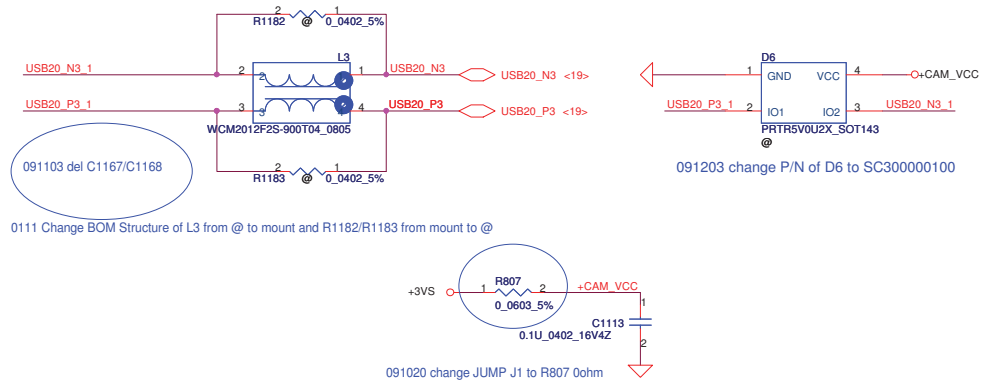
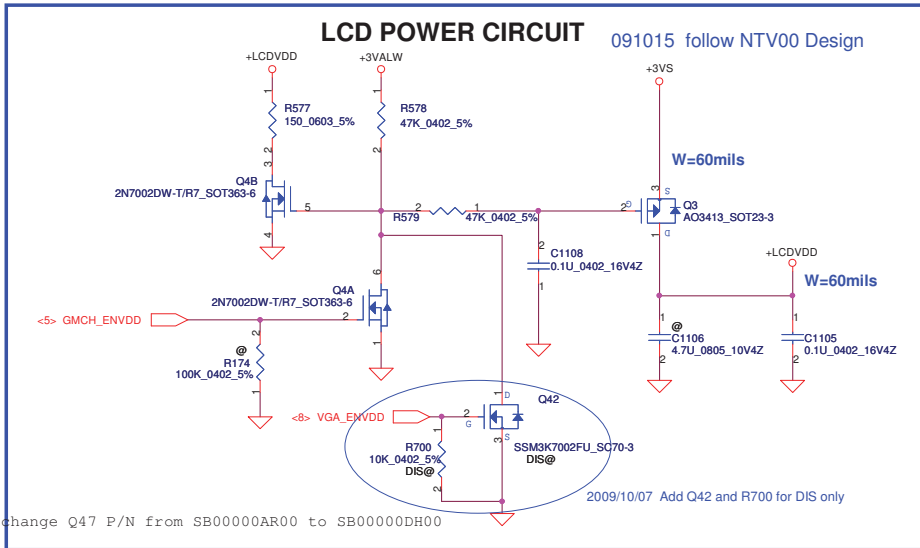
PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	PCIE_VGA
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN



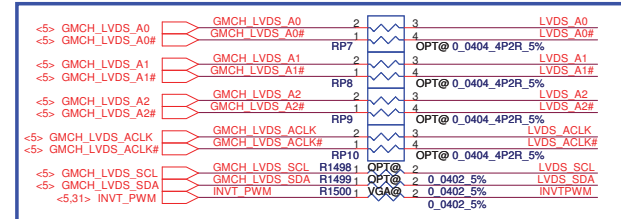
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_VGA
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	PCIE_WWAN
REQ_A#	

<http://laptop-motherboard.com/news/2010/03/03/>

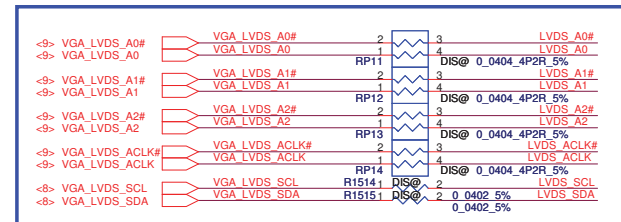


OPTIMUS

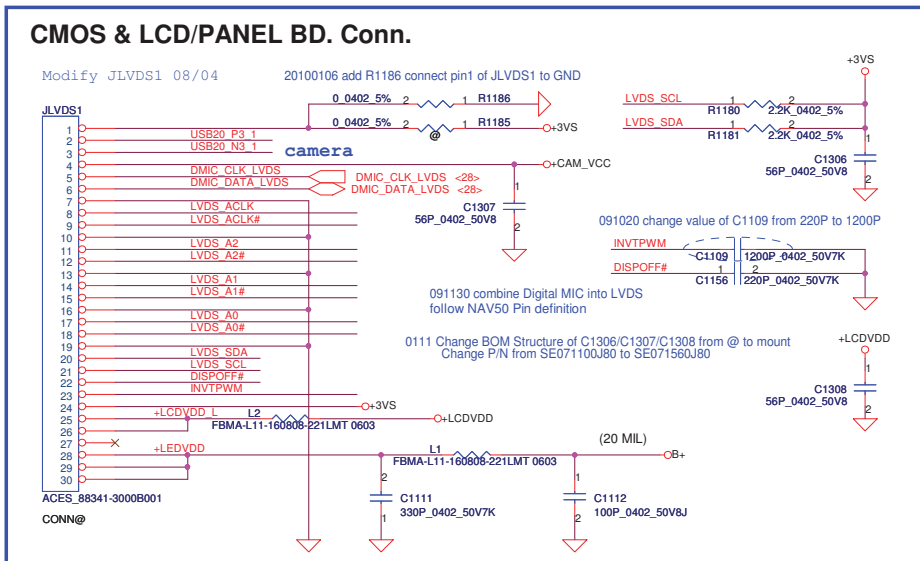


091202 swap A0/A0#,A1/A1#,A2/A2#,ACLK/ACLK# nets on RP7/RP8/RP9/RP10
091209 change BOM Structure of R1500 from OPT@ to VGA@

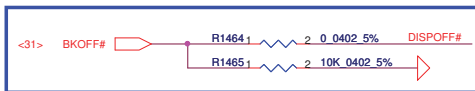
DIS ONLY



091202 swap A0/A0#,A1/A1#,A2/A2#,ACLK/ACLK# nets on RP11/RP12/RP13/RP14



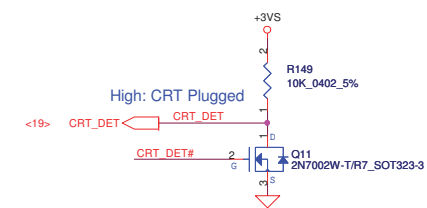
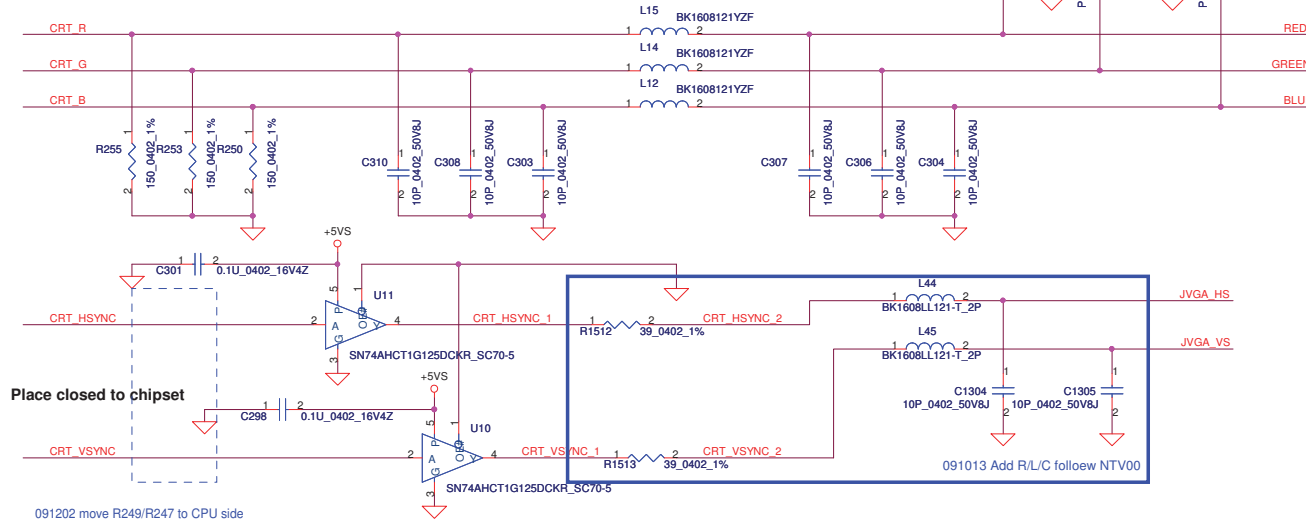
LED PANEL Conn.



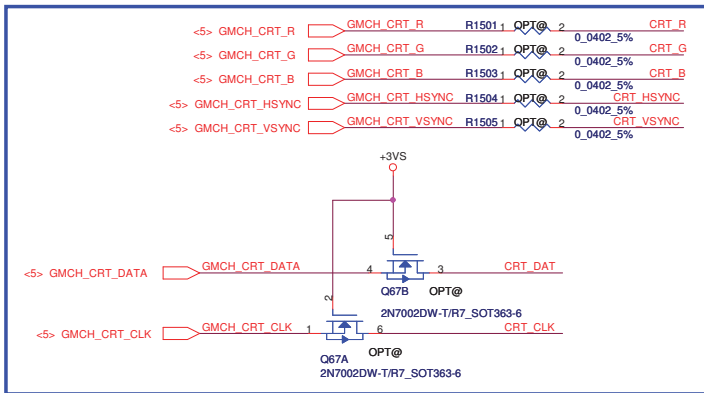
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				Custom	NAVDO LA-6091P	1.0
				Date:	Wednesday, March 03, 2010	Sheet 14 of 46

CRT PORT

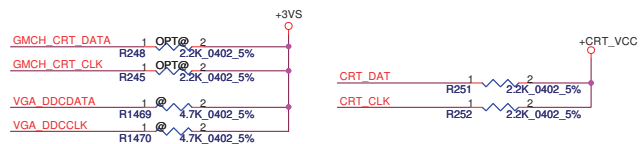
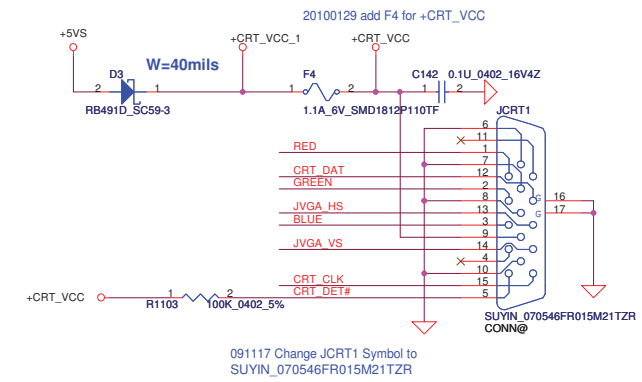
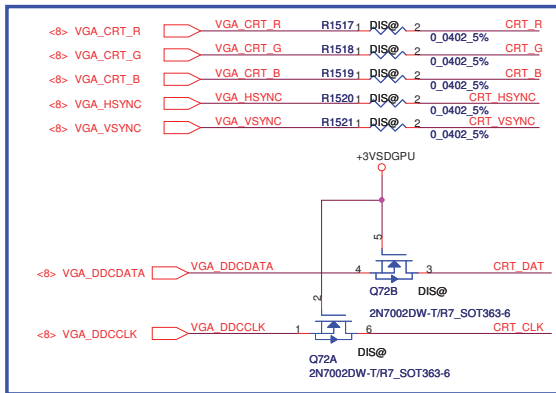
Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615
0120 Change L12,L14,L15 P/N from SM01000AL00 to SM010032020



OPTIMUS

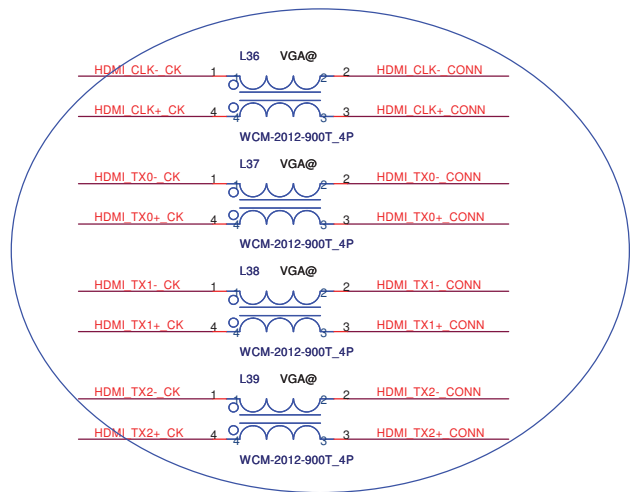


DIS ONLY

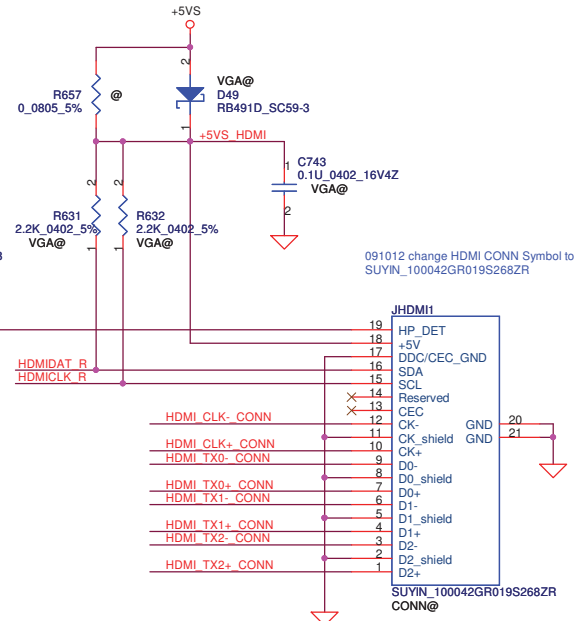
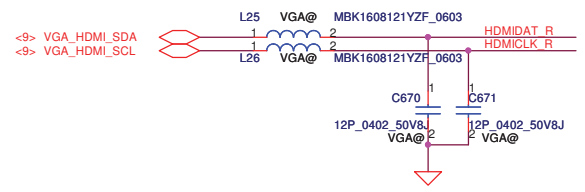
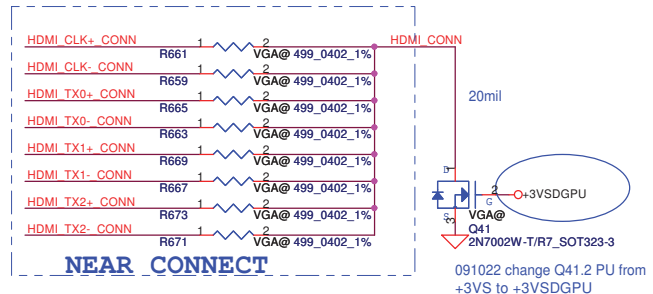
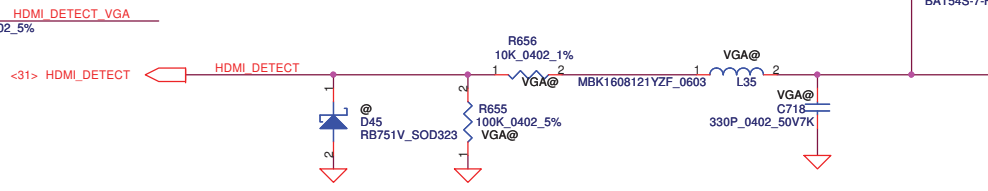
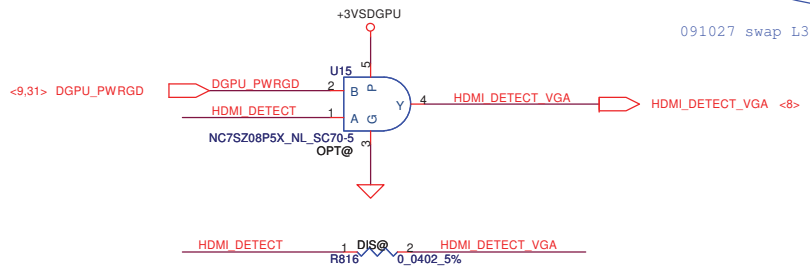


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				CRT PORT	
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				Custom	NAVD0 LA-6091P
				Date	Wednesday, March 03, 2010
				ISheet	15 of 46
				Rev	1.0

<9> VGA_HDMI_CLK+	C669	1	2	VGA@ 0.1U_0402_16V7K	HDMI_CLK+_CK	R660	1	2	0_0402_5%	HDMI_CLK+_CONN
<9> VGA_HDMI_CLK-	C668	1	2	VGA@ 0.1U_0402_16V7K	HDMI_CLK-_CK	R658	1	2	0_0402_5%	HDMI_CLK-_CONN
<9> VGA_HDMI_TX0+	C667	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX0+_CK	R664	1	2	0_0402_5%	HDMI_TX0+_CONN
<9> VGA_HDMI_TX0-	C666	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX0-_CK	R662	1	2	0_0402_5%	HDMI_TX0-_CONN
<9> VGA_HDMI_TX1+	C715	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX1+_CK	R668	1	2	0_0402_5%	HDMI_TX1+_CONN
<9> VGA_HDMI_TX1-	C713	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX1-_CK	R666	1	2	0_0402_5%	HDMI_TX1-_CONN
<9> VGA_HDMI_TX2+	C730	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX2+_CK	R672	1	2	0_0402_5%	HDMI_TX2+_CONN
<9> VGA_HDMI_TX2-	C711	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX2-_CK	R670	1	2	0_0402_5%	HDMI_TX2-_CONN

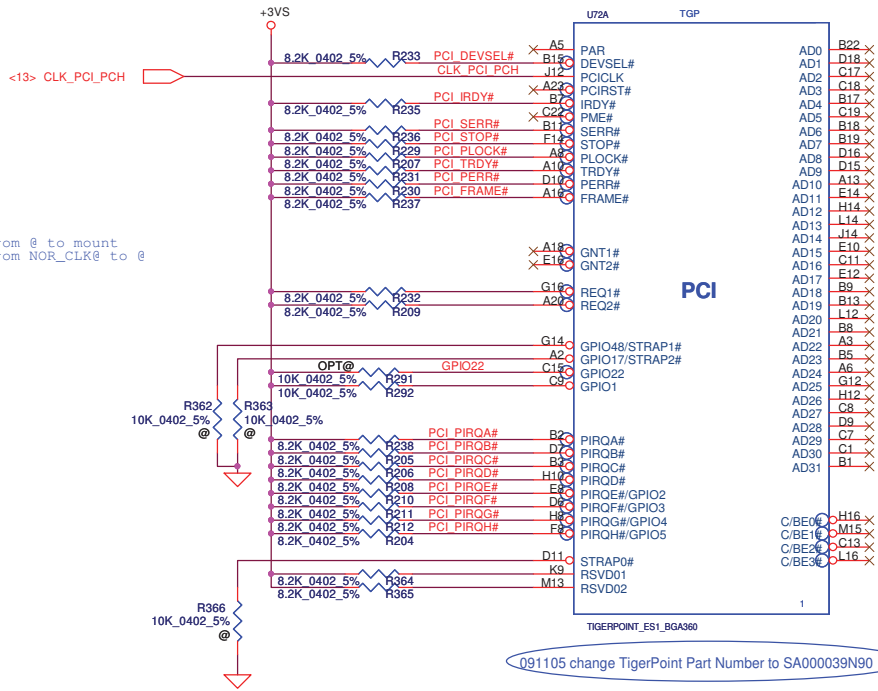
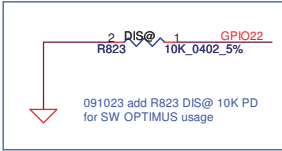
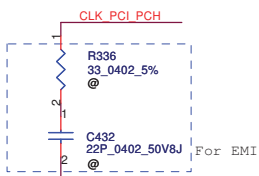


091027 swap L36/L37/L38/L39 nets for layout



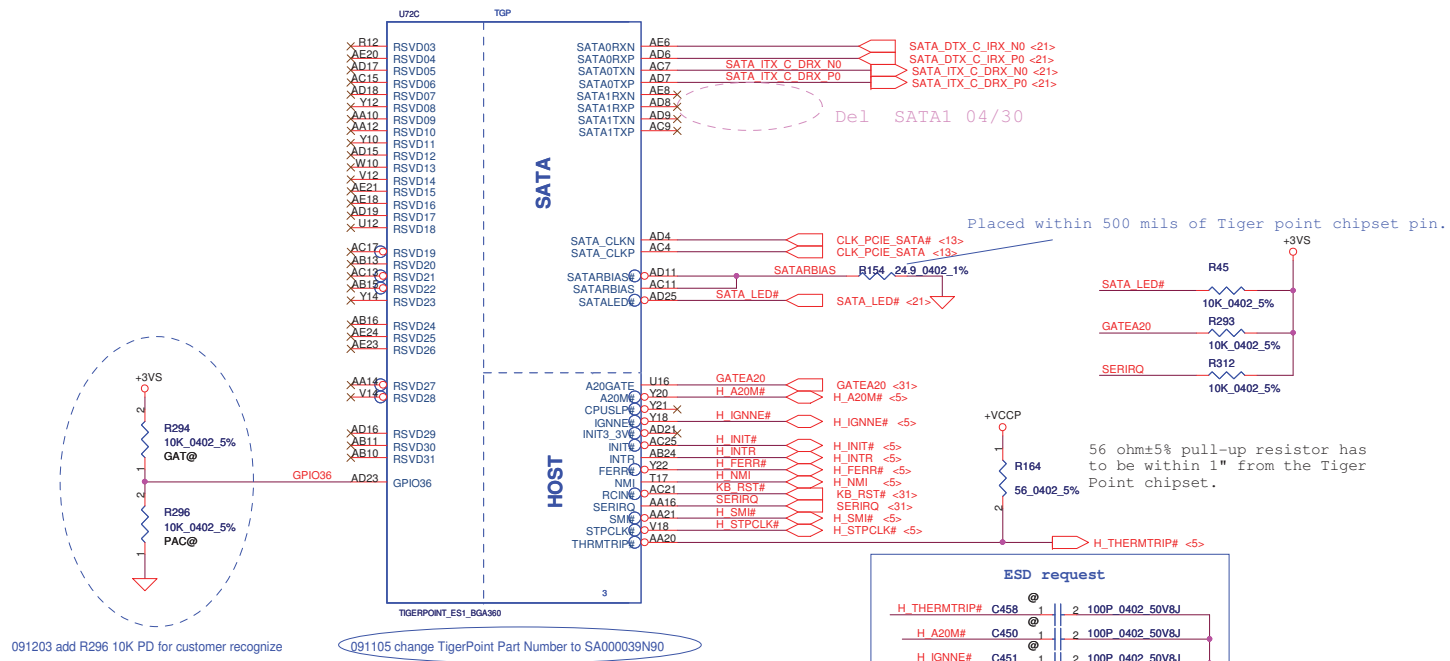
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title
				HDMI CONN
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Size	Document Number	Date		Rev
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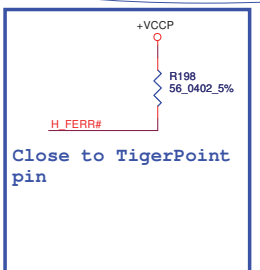
STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title Tigerpoint(1/4)	
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				Sheet	17 of 46
				Rev	1.0



091203 add R296 10K PD for customer recognize

091105 change TigerPoint Part Number to SA000039N90



ESD request

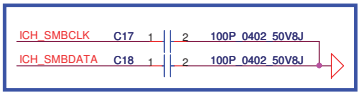
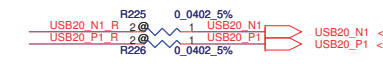
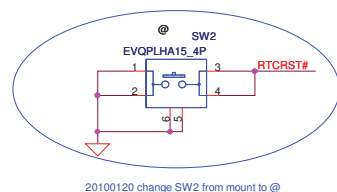
H_THERMTRIP#	C458	1	2	100P_0402_50V8J
H_A20M#	C450	1	2	100P_0402_50V8J
H_IGNNE#	C451	1	2	100P_0402_50V8J
H_INIT#	C452	1	2	100P_0402_50V8J
H_INTR#	C453	1	2	100P_0402_50V8J
H_FERR#	C454	1	2	470P_0402_50V8J
H_NMI#	C455	1	2	100P_0402_50V8J
H_SMI#	C456	1	2	100P_0402_50V8J
H_STPCLK#	C457	1	2	100P_0402_50V8J

091216 change value of C454 to 470P

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title Tigerpoint(2/4)		
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				Date	Wednesday, March 03, 2010	Sheet 18 of 46

PCIe Port List	
1	LAN
2	WLAN
3	WWAN
4	

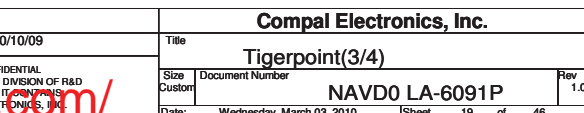
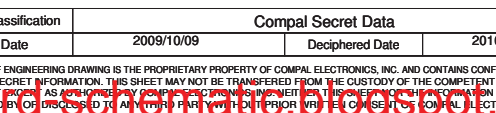
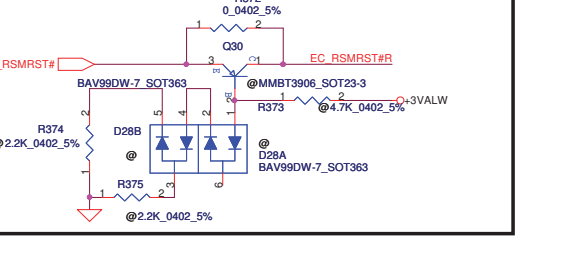
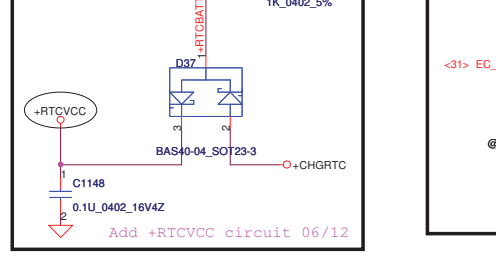
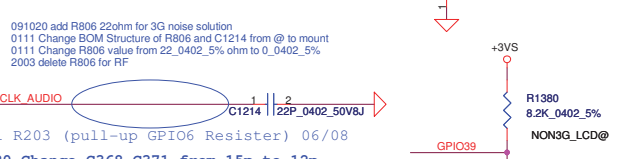
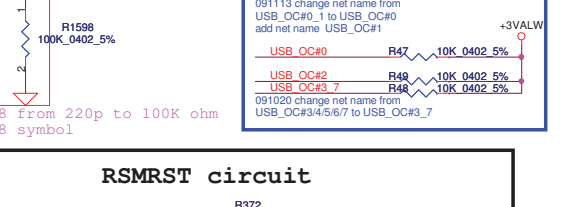
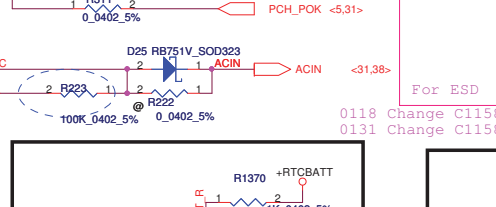
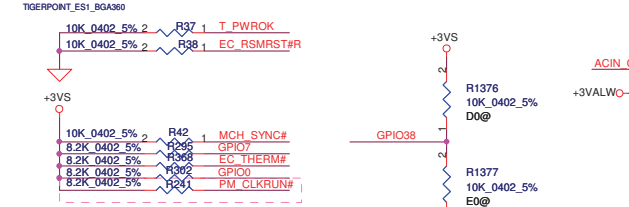
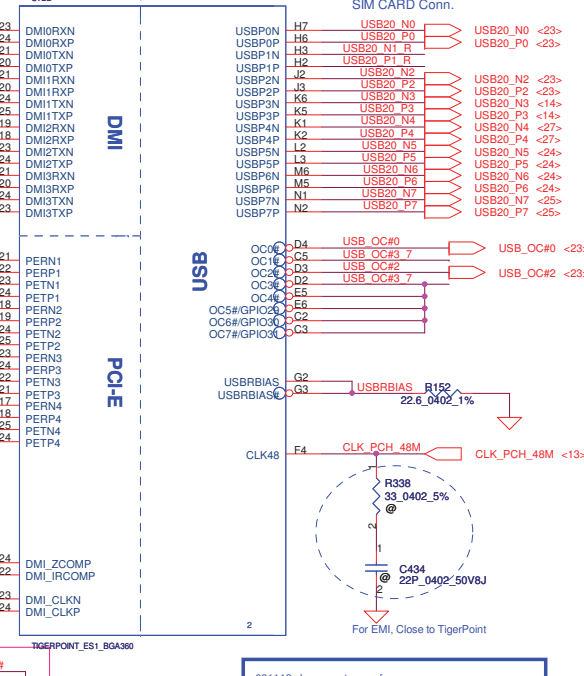
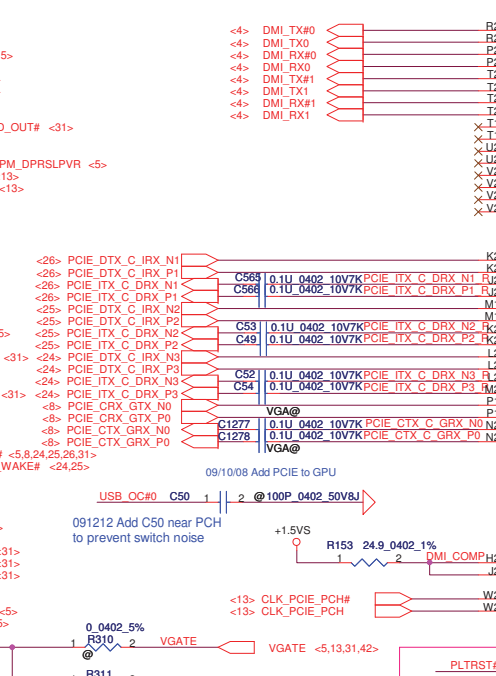
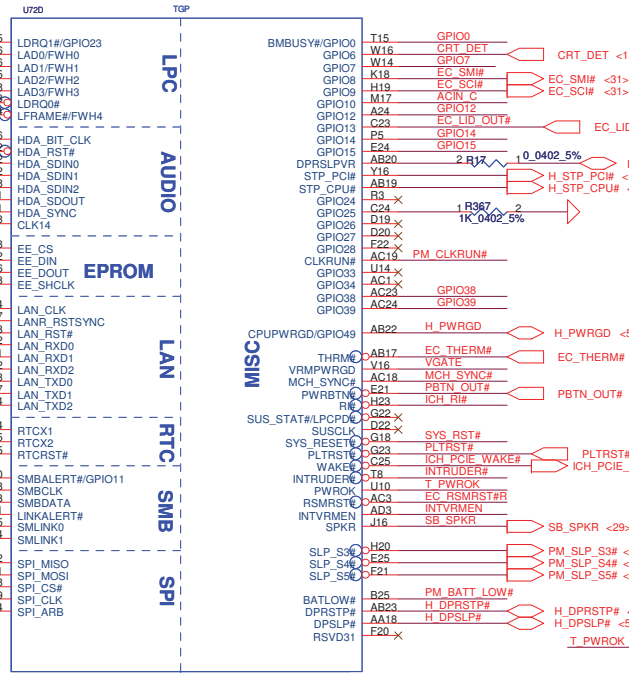
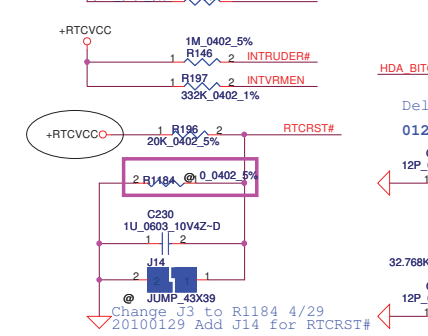
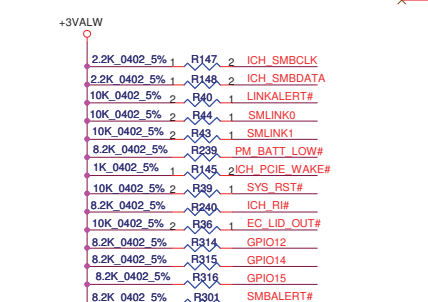
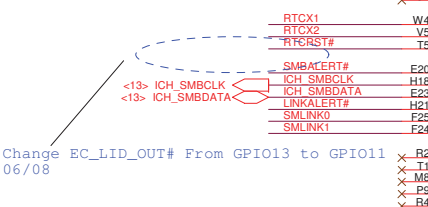
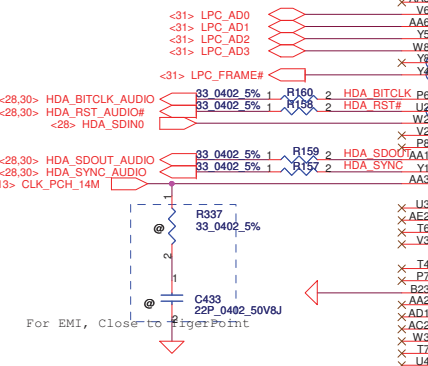
USB Port List	
0	USB Left1
1	
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



091105 change TigerPoint Part Number to SA000039N90

091105 change TigerPoint Part Number to SA000039N90

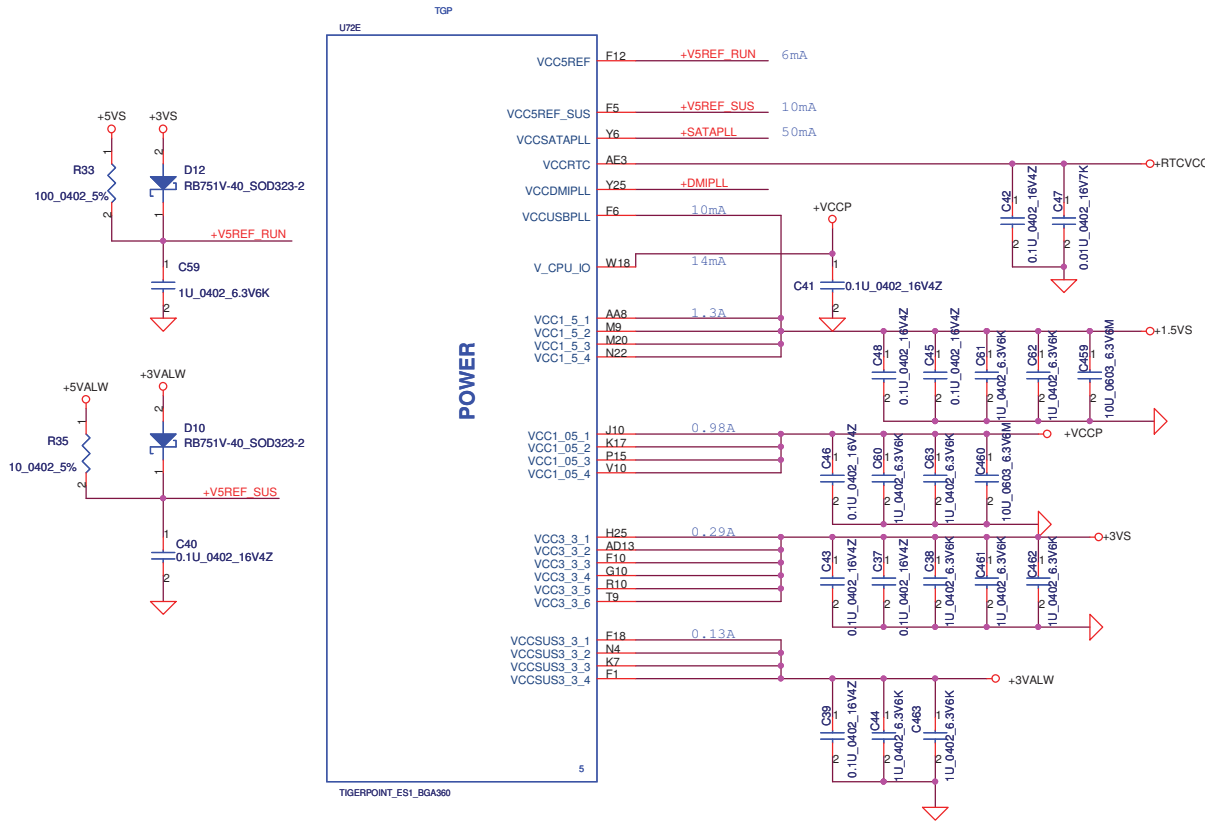
091212 Add C30 near PCH to prevent switch noise



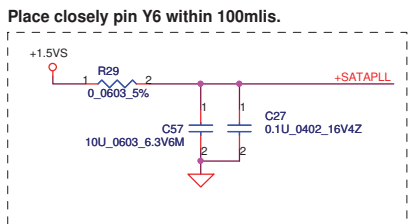
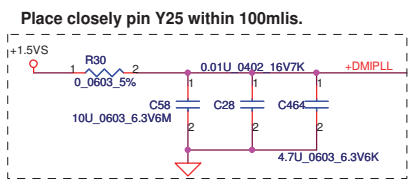
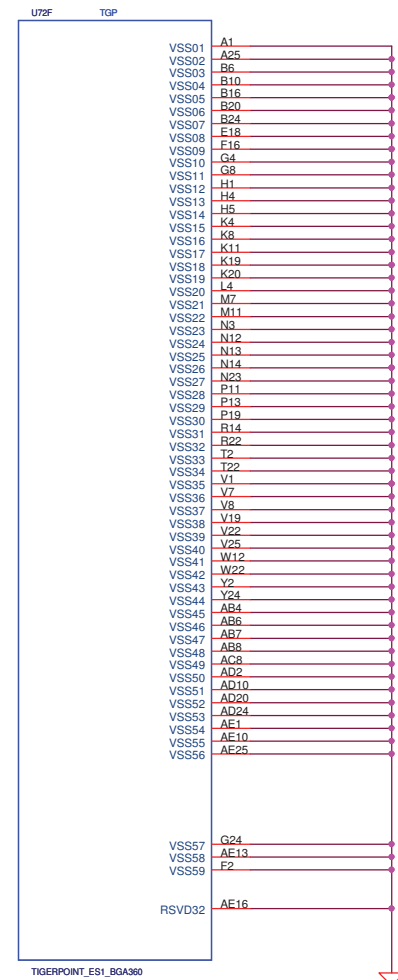
Security Classification	2009/10/09	Compal Secret Data	2010/10/09	Title
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Compal Electronics, Inc.
				Tigerpoint(3/4)
				NAVD0 LA-6091P
				Rev 1.0
				Date: Wednesday, March 03, 2010 Sheet 19 of 46

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091105 change TigerPoint Part Number to SA000039N90

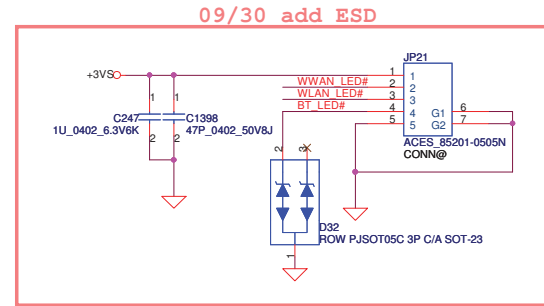
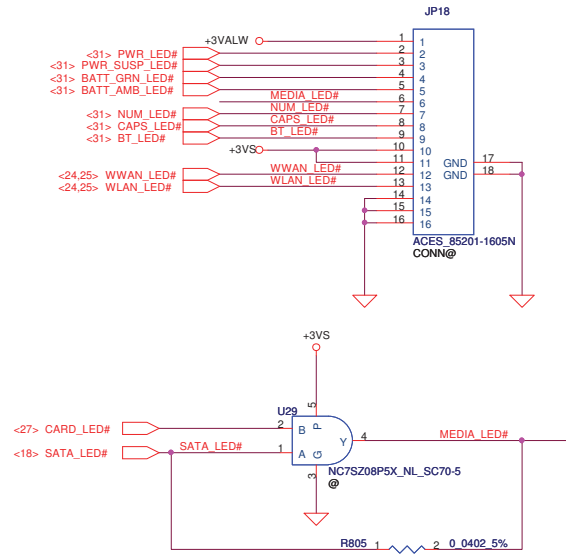


091105 change TigerPoint Part Number to SA000039N90



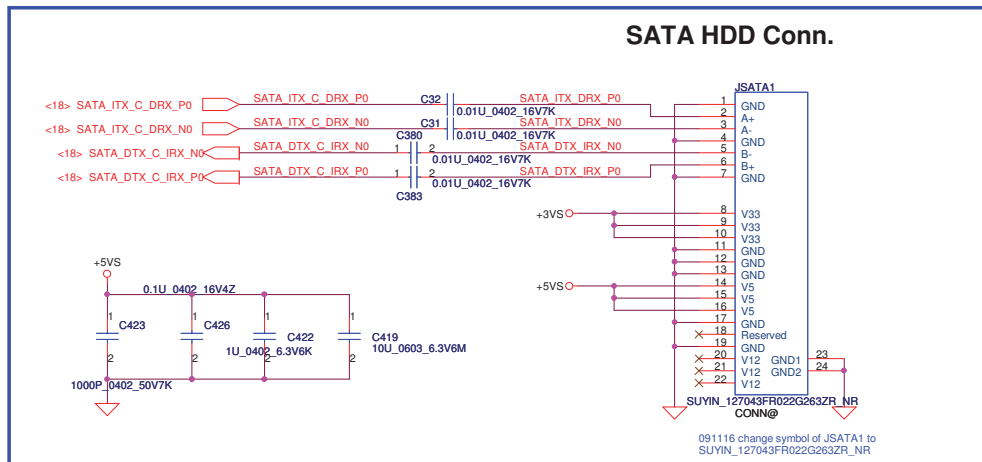
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size Custom	Document Number	NAVDO LA-6091P		Rev	1.0
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LED PCB CONN



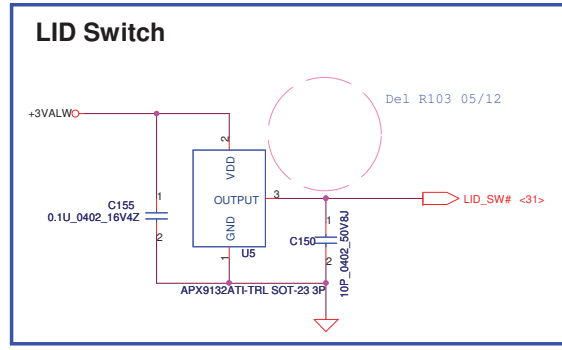
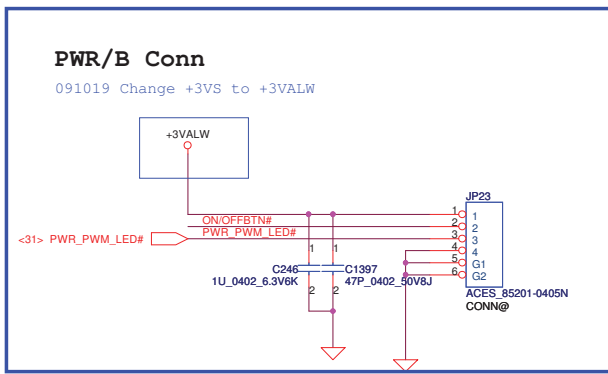
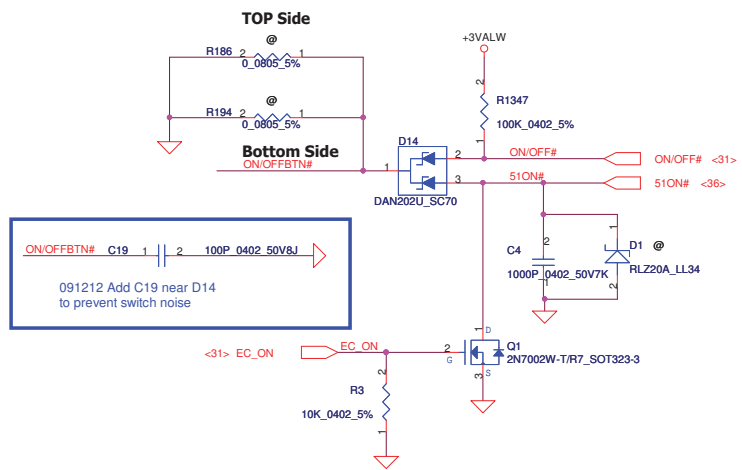
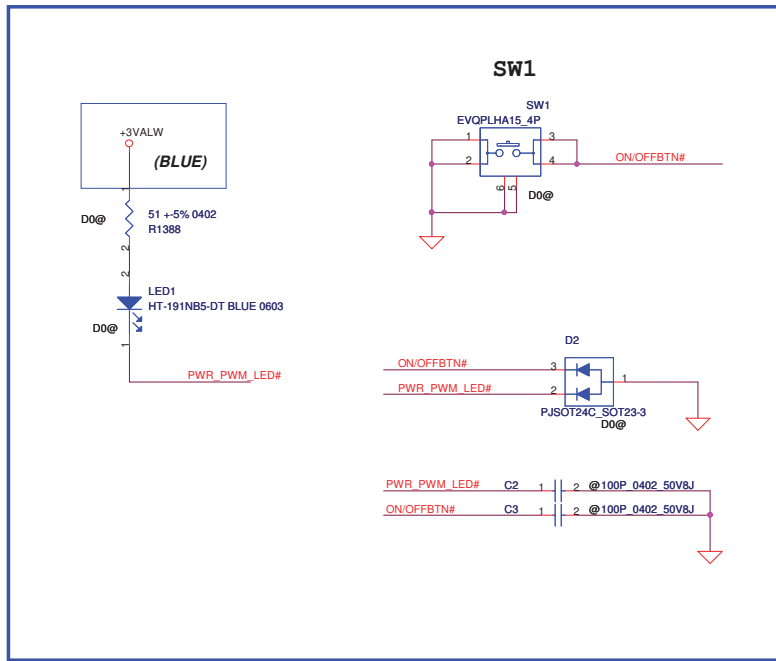
0108 Add C247,C1398 on pin1 of JP21 (RF)

SATA HDD Conn.



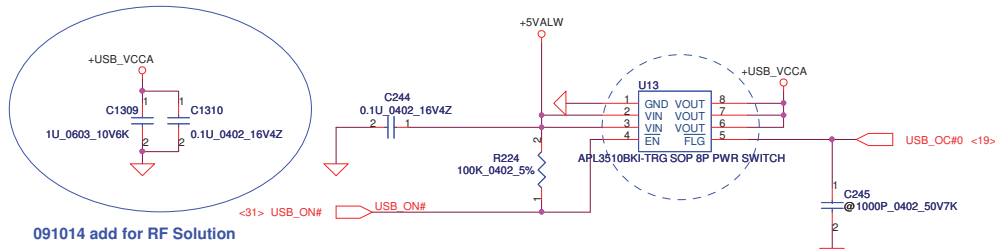
091116 change symbol of JSATA1 to SUYIN_127043FR022G263ZR_NR CONN@

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title		
				LED/HDD/Function Board CONN.		
Size	Document Number	Date		Wednesday, March 03, 2010	Sheet	21 of 46
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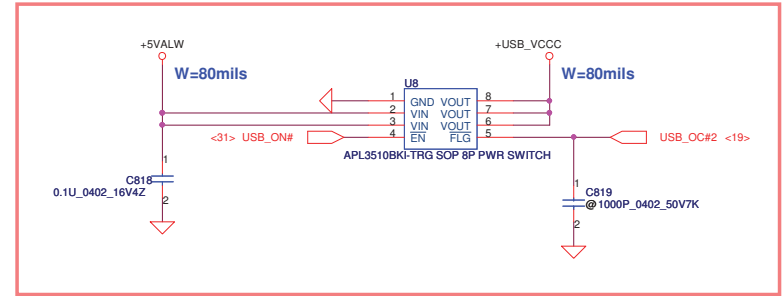


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title	
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Size	B	Document Number	NAV00 LA-6091P	Rev	1.0
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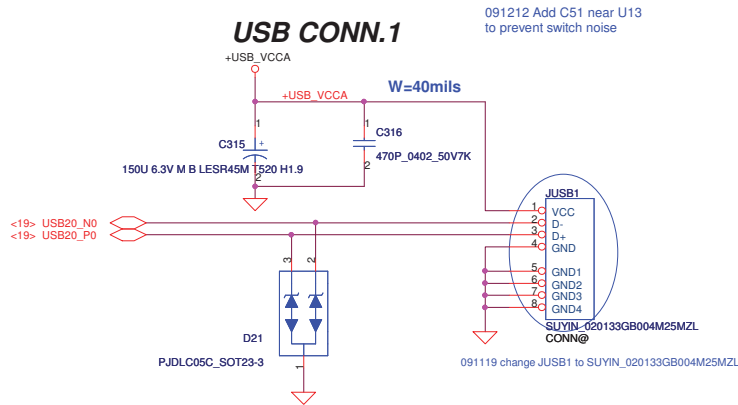
5/5 Add U2 circuit



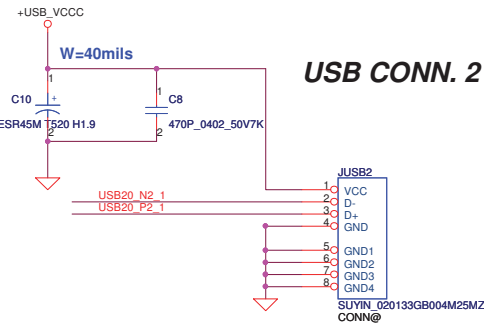
091014 add for RF Solution



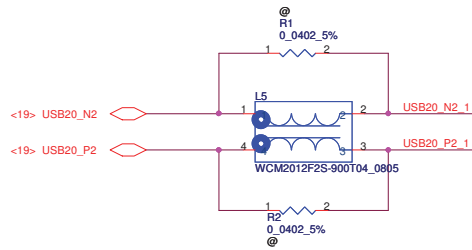
USB CONN. 1



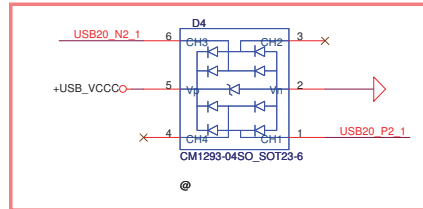
091212 Add C51 near U13 to prevent switch noise



USB CONN. 2



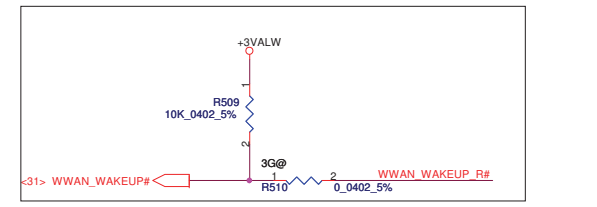
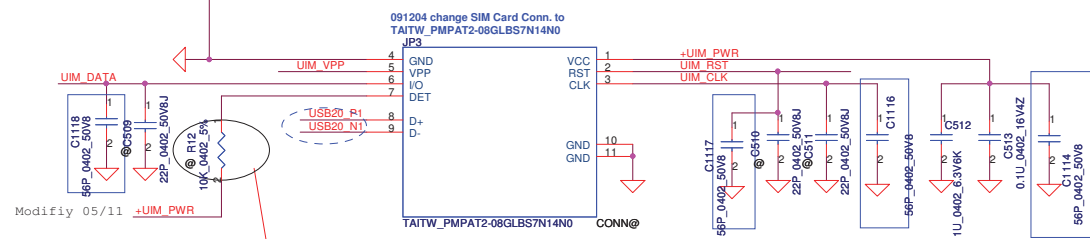
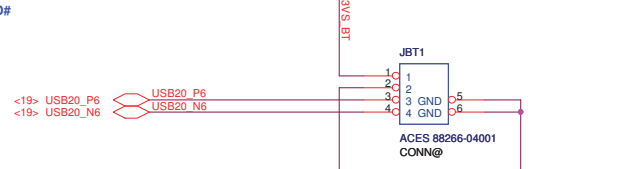
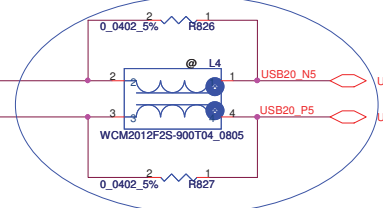
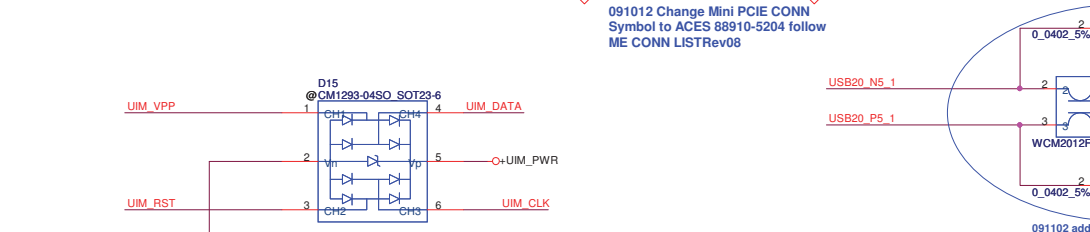
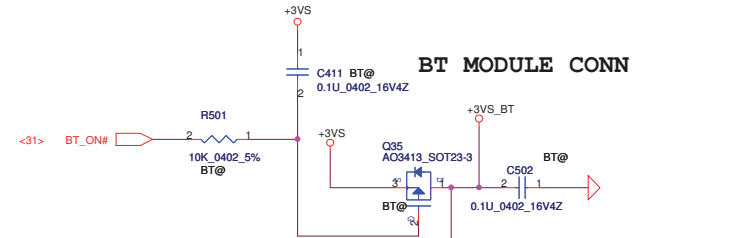
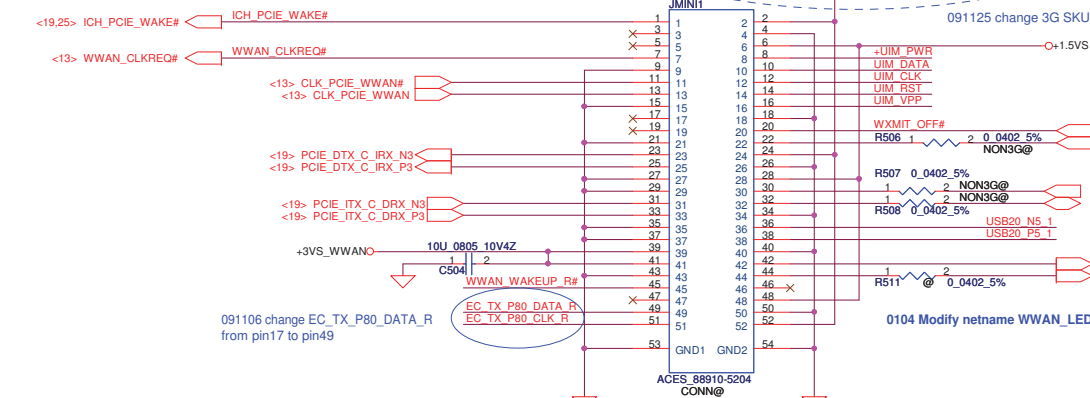
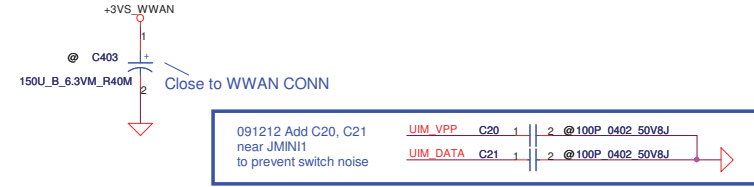
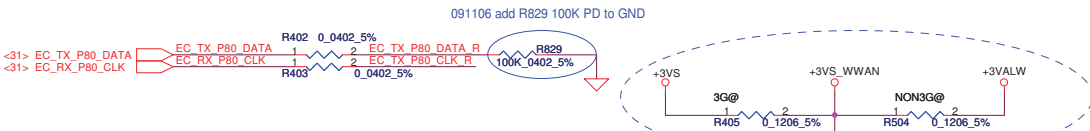
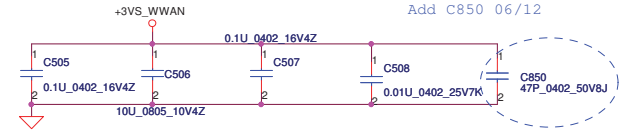
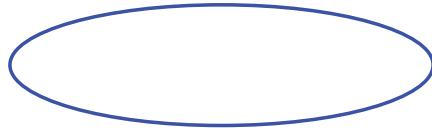
5/12 Revised net name



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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				USB PORT		
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Mini-Express Card for WWAN

091019 Remove C1163/C1164/C1165/C1166



Reserve for SIM card does not meet rise time and pull-up is needed.

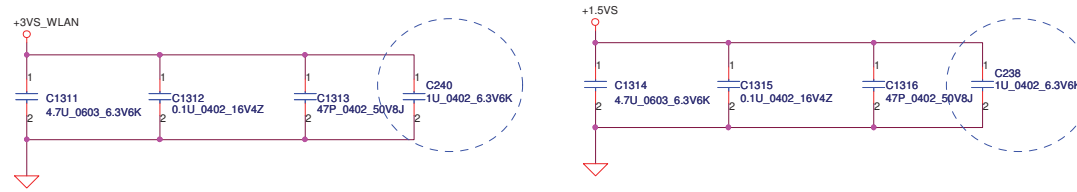
091204 add USB20_P1/N1 for SIM Card Conn.

091204 add USB20_P1/N1 for SIM Card Conn.

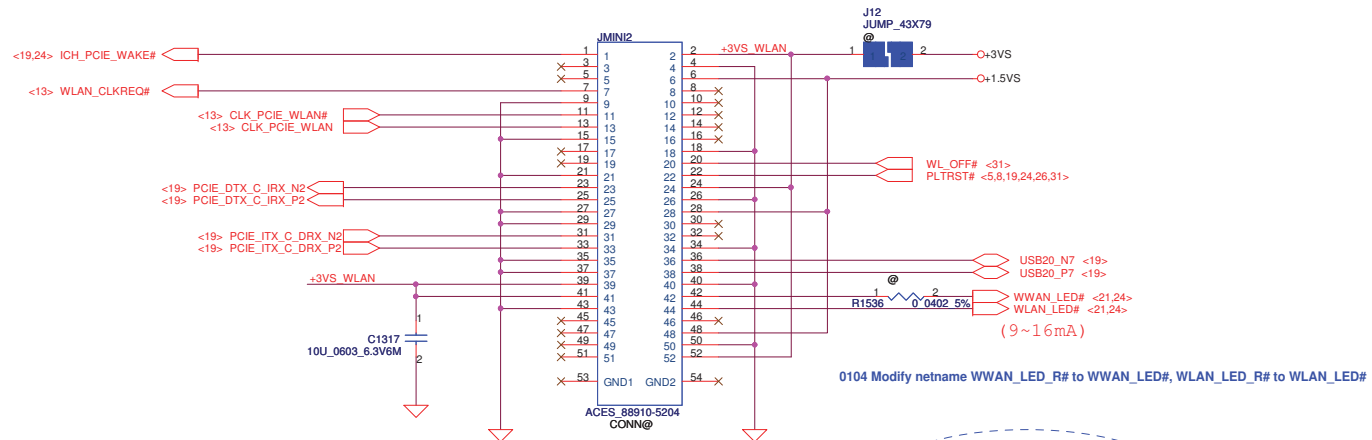
Add C1114 C1116 C1117 C1118 05/11
Change C512 to 1U_0402 05/14

Security Classification		Compal Secret Data		Title	
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Mini-Card/BT CONN	
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Mini-Express Card for WLAN



091127 reserve C240/C238 for RF team
 0111 Change BOM Structure of C238/C240 from @ to mount



0104 Modify netname WWAN_LED_R# to WWAN_LED#, WLAN_LED_R# to WLAN_LED#

091116 Change JMINI2
 Symbol to ACES 88910-5204 follow
 ME CONN LIST 1116 Rev01



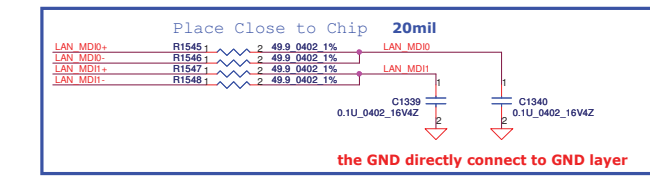
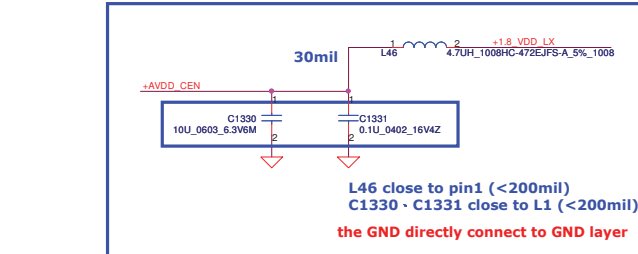
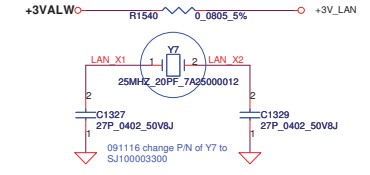
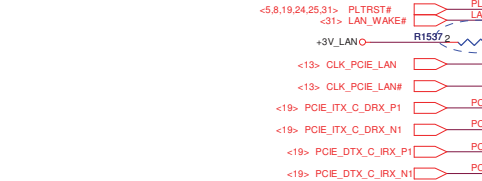
091125 reserve 0ohm for WIMAX

- 5/12 Update WLAN connector(the same as KAV60)
- 6/1 Revised 37、39、41、42、43 to NC
- 6/12 Update connector to DC040006S00
- 6/26 Update JMINI1 footprint
- 7/01 update pin 23,25,31,33

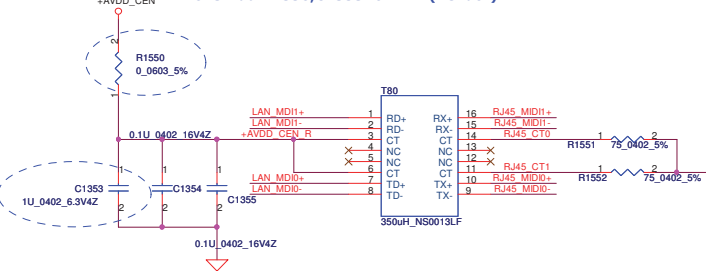
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title WLAN		
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				Date:	Wednesday, March 03, 2010	Sheet 25 of 46

1013 pull up R1537 (Vendor)

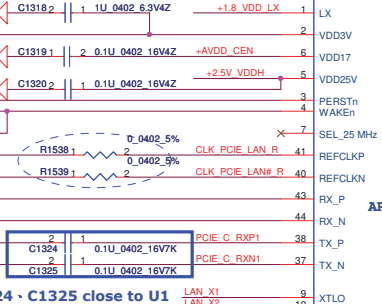
1013 Add R1538,R1539 for reserve 0.1u cap (Vendor)



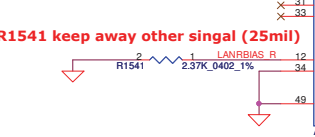
1013 Add R1550,C1353 for EMI (Vendor)



C1319 close to pin6
 C1318 close to pin2
 C1320 close to pin5

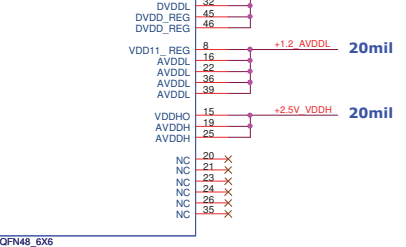


C1324 - C1325 close to U1



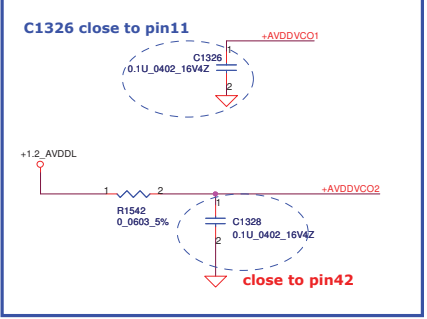
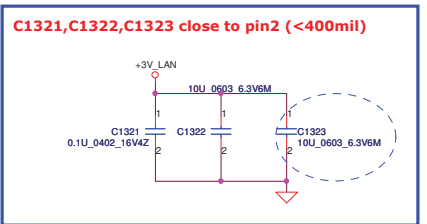
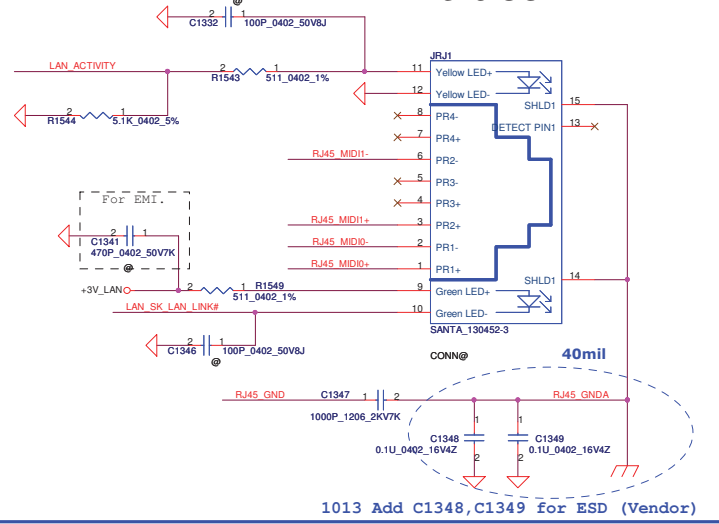
Atheros

AR8132 10/100 LAN

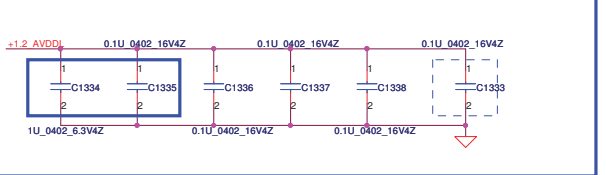


close to JRJ1

RJ45 CONN



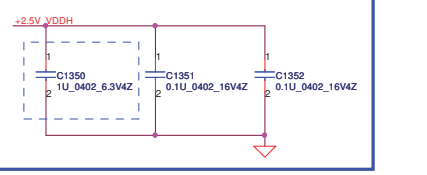
C1334,C1335 close to pin8
 C1336 close to pin16
 C1337,C1338 close to pin22 .36



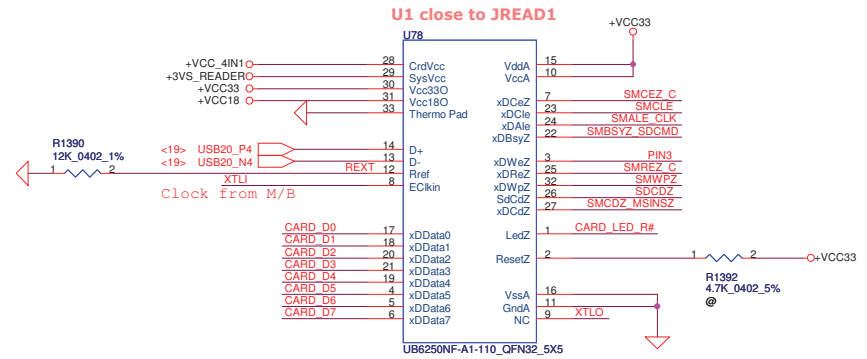
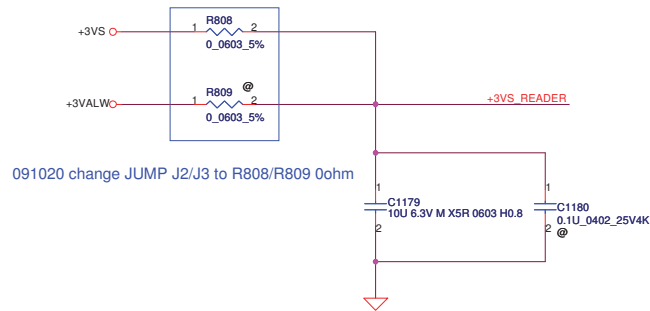
C1343 close to pin28
 C1344 close to pin32
 C1345 close to pin45
 C1342 close to pin46



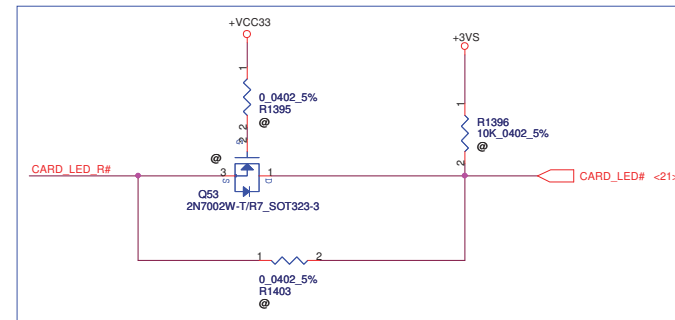
C1350 close to pin15
 C1351 close to pin19
 C1352 close to pin25



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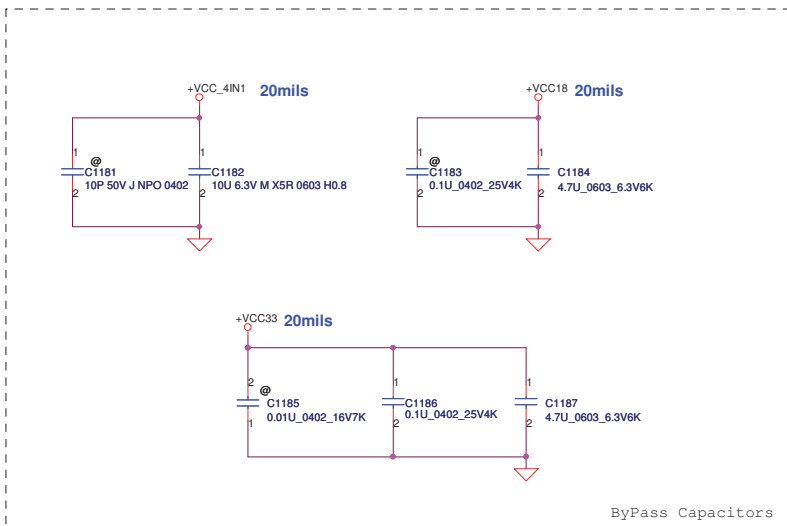
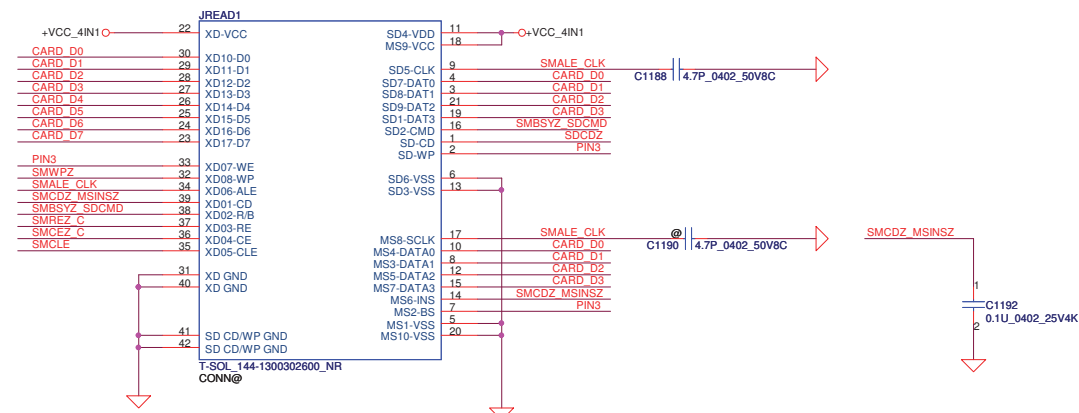


If use external crystal (Y6),
U78 will change UB6252

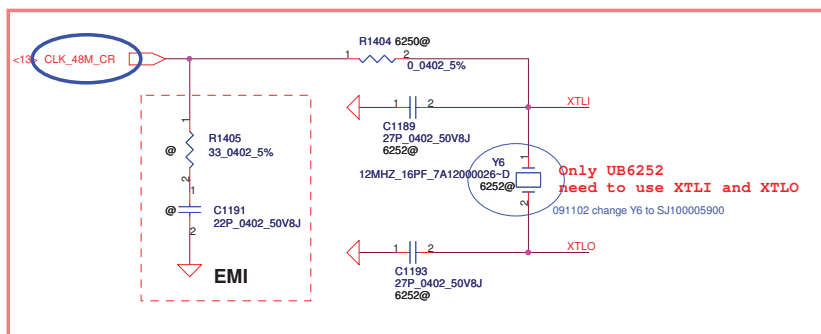


091203 change BOM structure of
Q53/R1395/R1396 from mount to @

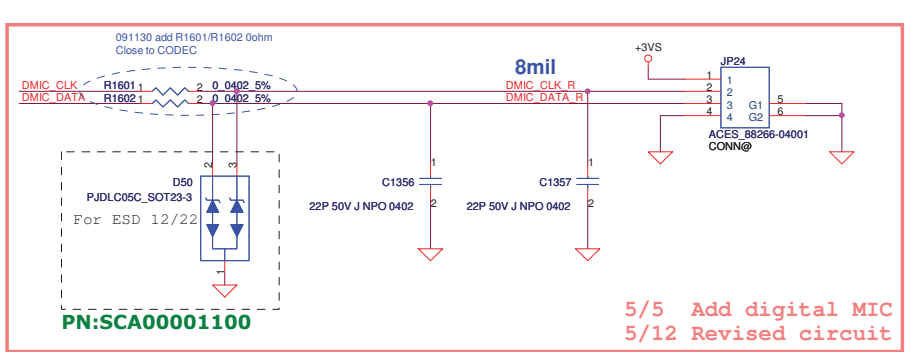
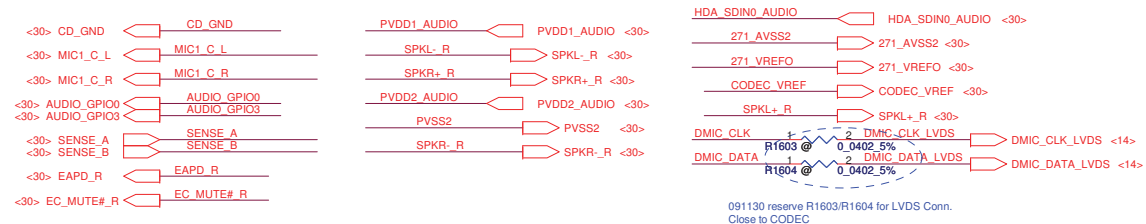
Card Reader Connector



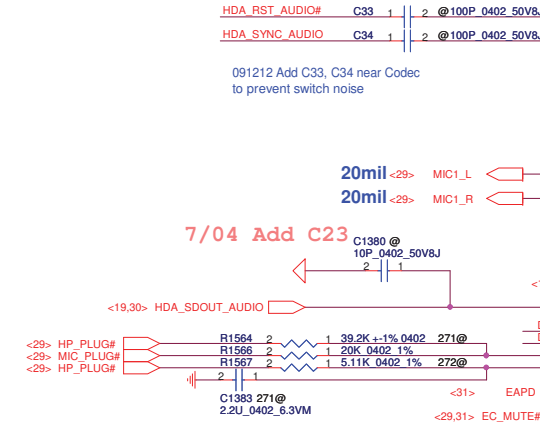
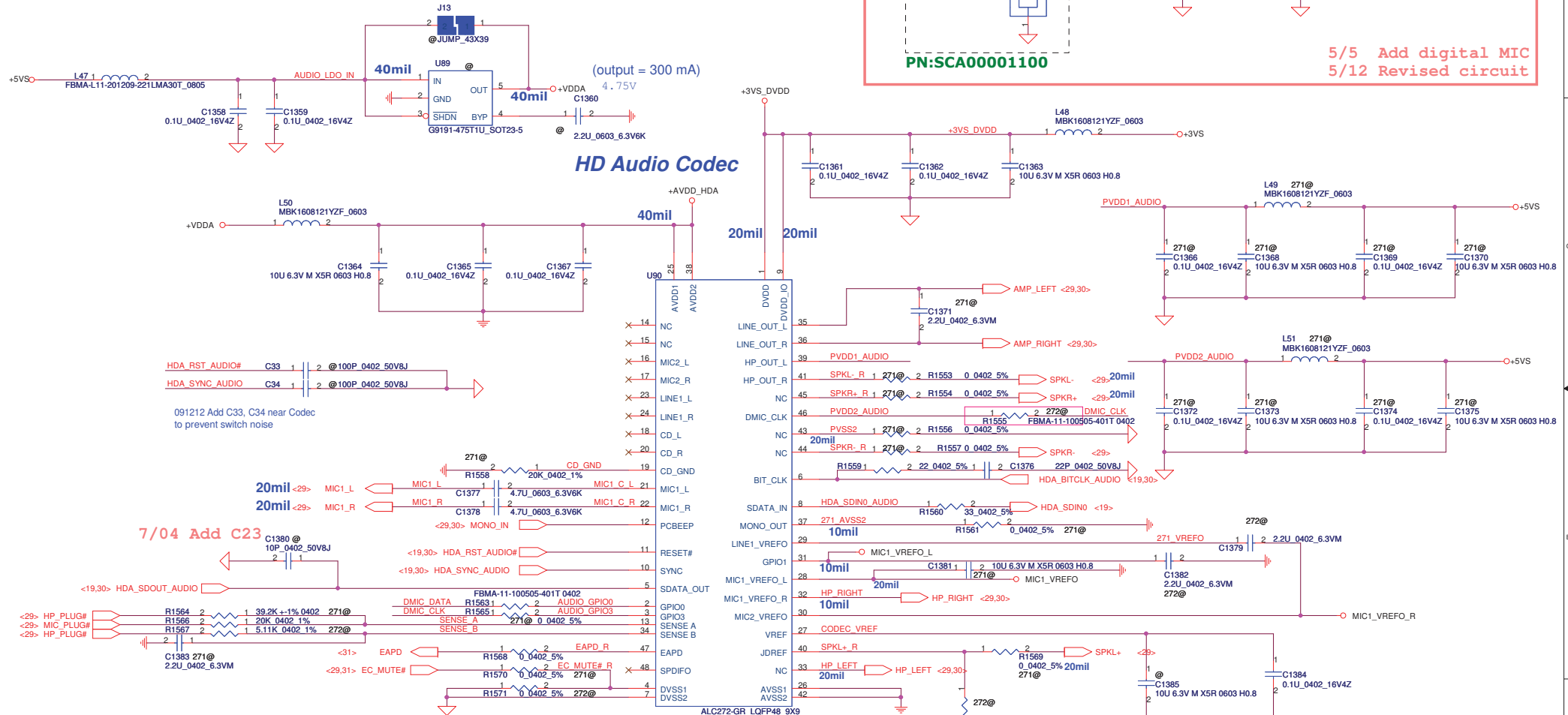
ByPass Capacitors



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				CARD READER		
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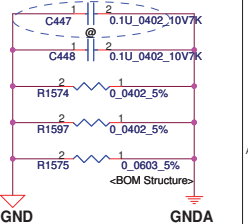
5/5 Add digital MIC
5/12 Revised circuit



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

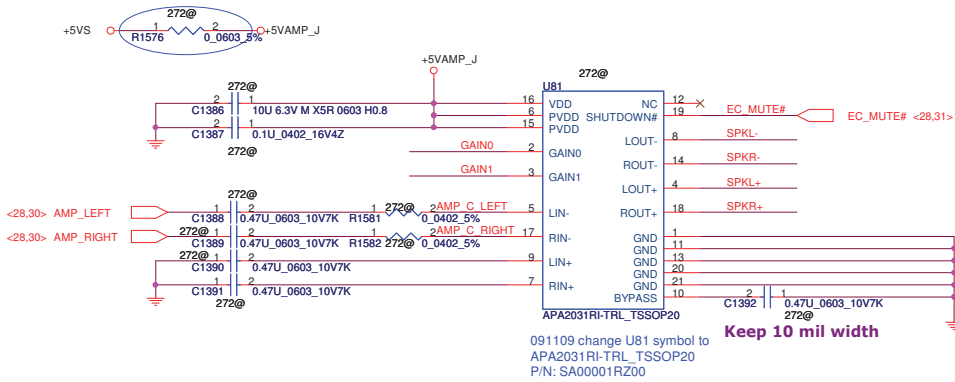
Change to SA00002CI20 ALC272-VA2-GR

091127 reserve C447 0.1U for EMI request
20100125 change R1573 P/N from SD028000080 to SE102104K00,
value from 0.0402_5% to 0.1U_0402_10V7K
20100131 change R1573 symbol to C448

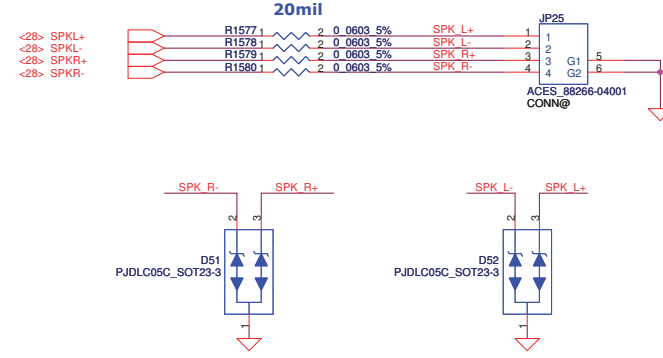


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Size	Document Number	Date		Rev	
C-start	NAV00 LA-6091P	Wednesday, March 03, 2010		1 Sheet 28 of 46	

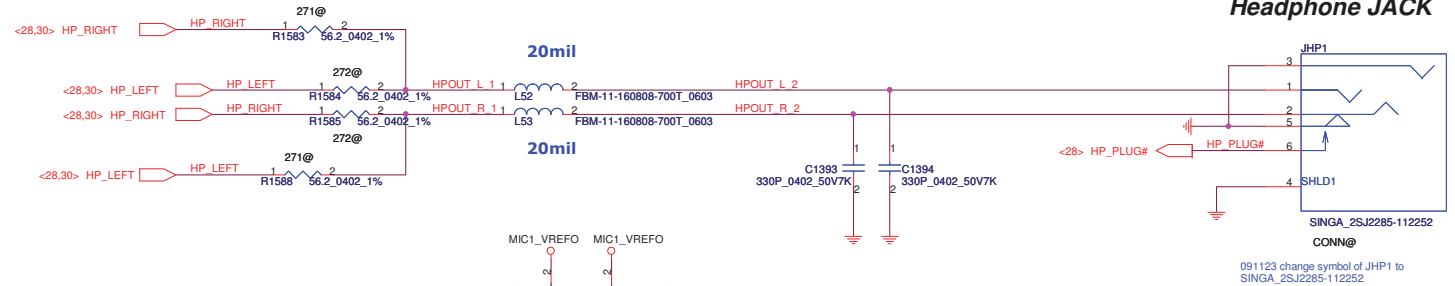
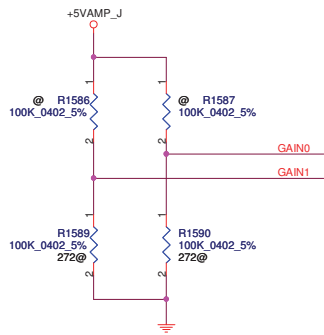
091020 change JUMP J5 to R1576 0ohm



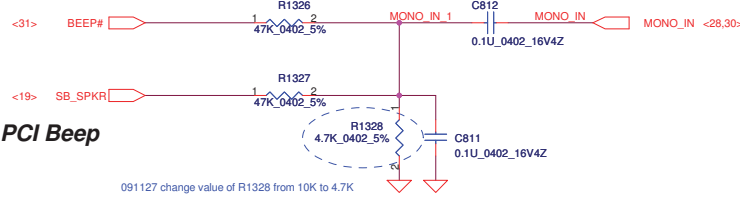
Int. Speaker Conn.



20081029 Update to 6dB

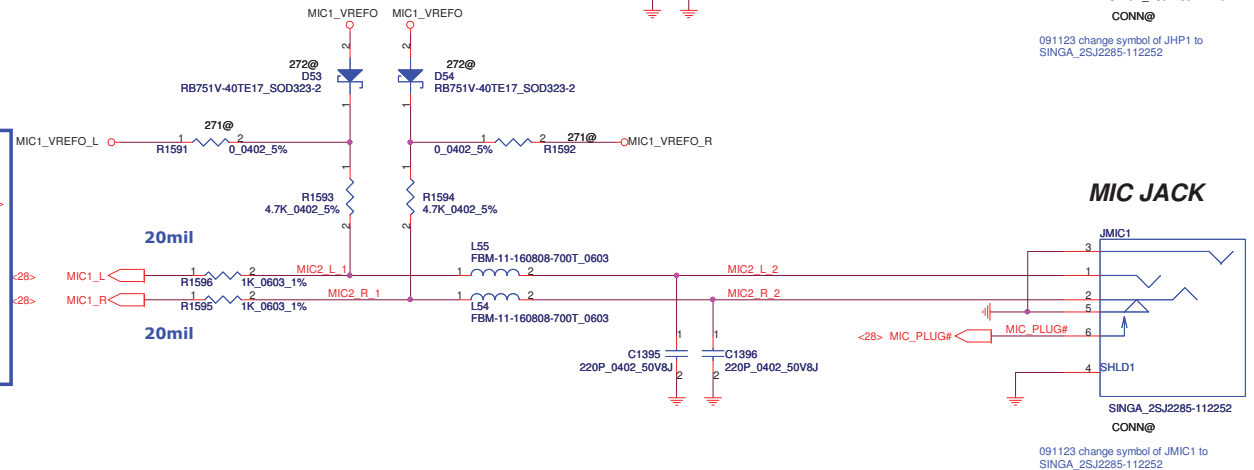


EC Beep



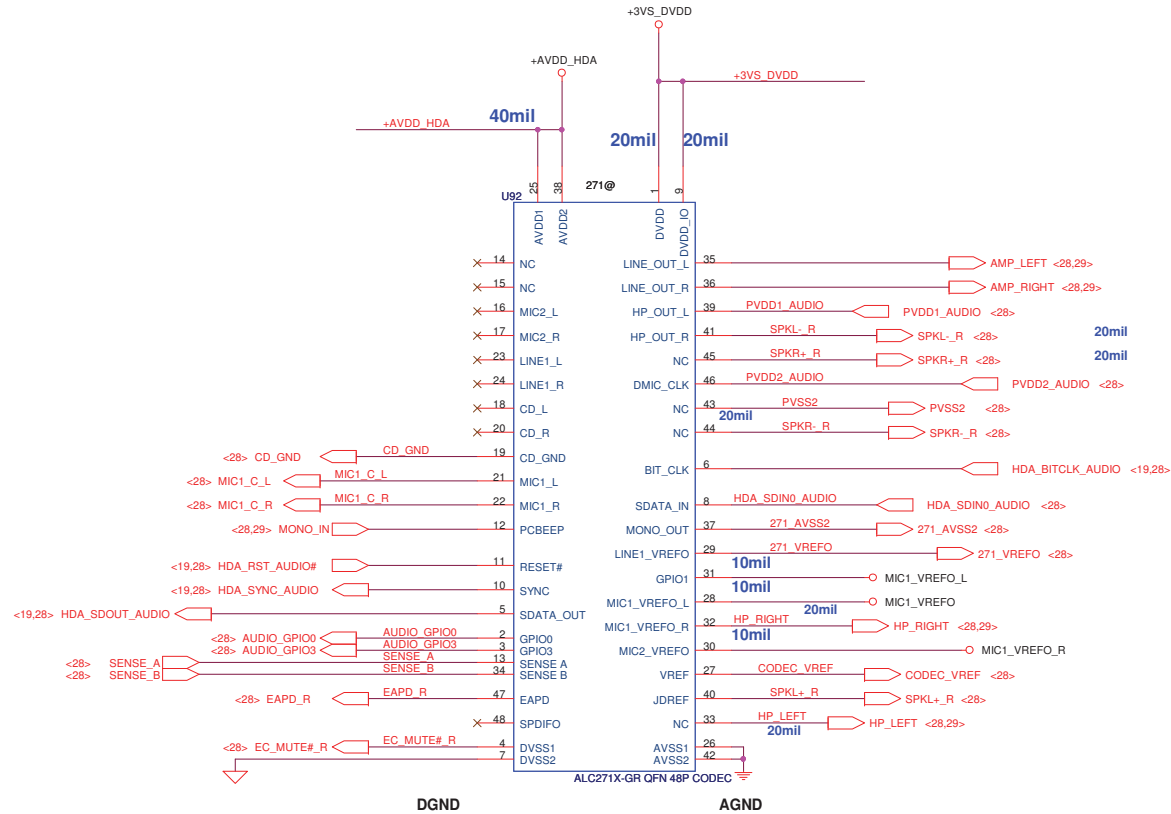
PCI Beep

091020 follow NTV00 Design



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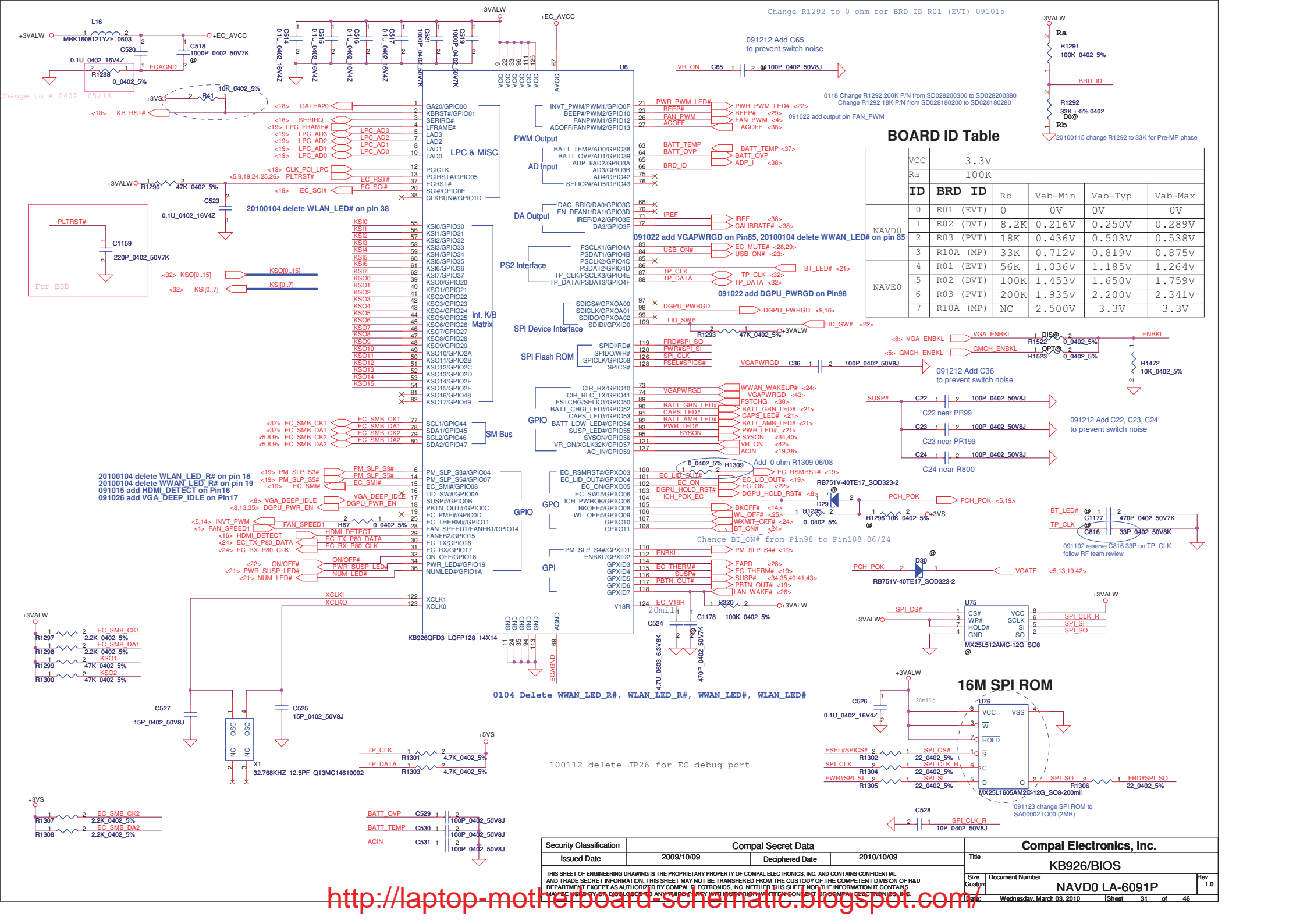
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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				AUDIO CODEC ALC271		
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				Custom	NAV00 LA-6091P	1.0
				Date:	Wednesday, March 03, 2010	Sheet 30 of 46

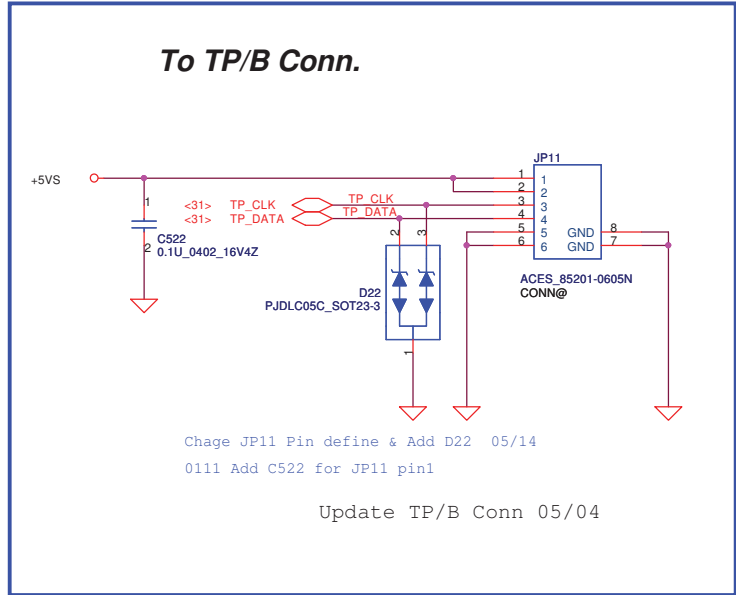
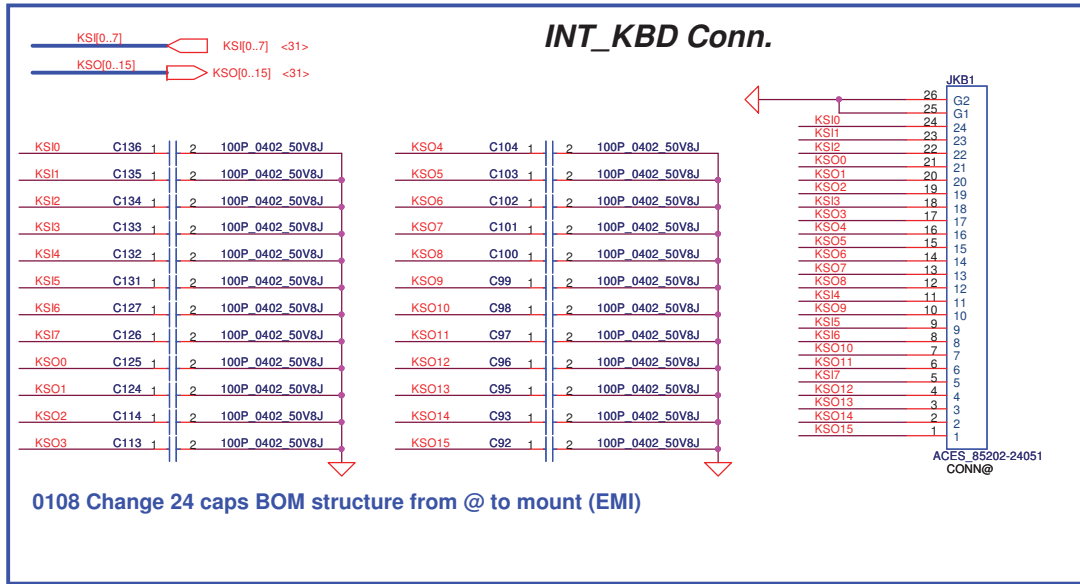
<http://laptop-motherboard-schematic.blogspot.com/>



BOARD ID Table

VCC		3.3V				
Ra		100K				
ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max	
0	R01 (EVT)	0	0V	0V	0V	
1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V	
2	R03 (PVT)	18K	0.436V	0.503V	0.538V	
3	R10A (MP)	33K	0.712V	0.819V	0.875V	
4	R01 (EVT)	56K	1.036V	1.185V	1.264V	
5	R02 (DVT)	100K	1.453V	1.650V	1.759V	
6	R03 (PVT)	200K	1.935V	2.200V	2.341V	
7	R10A (MP)	NC	2.500V	3.3V	3.3V	

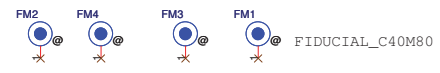
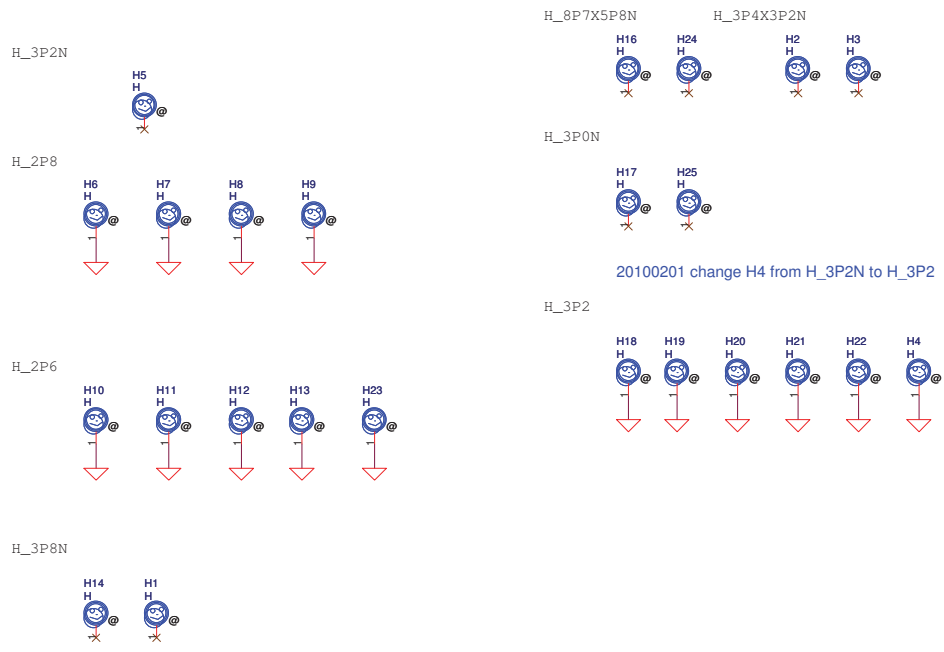
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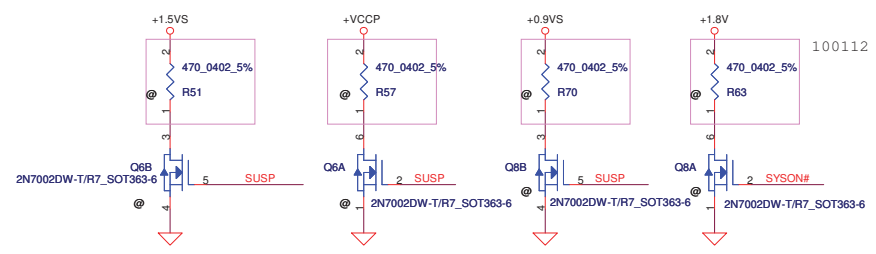
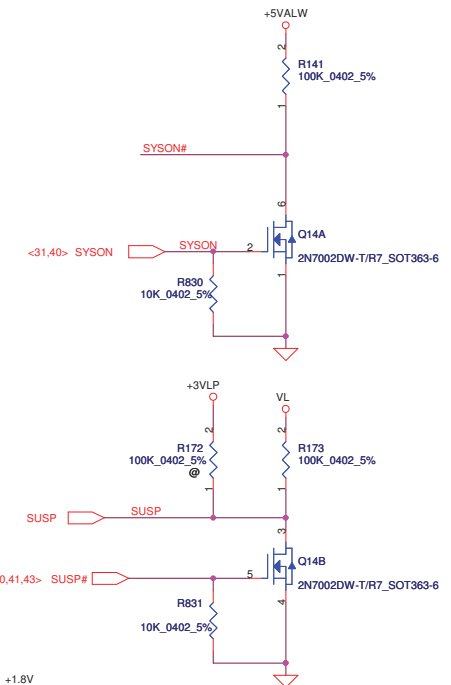
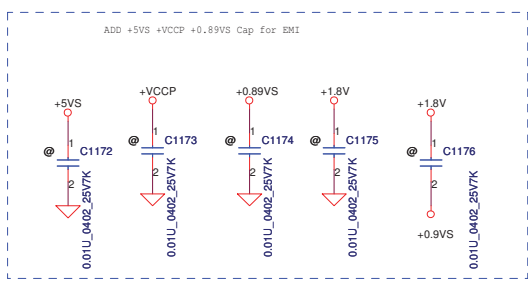
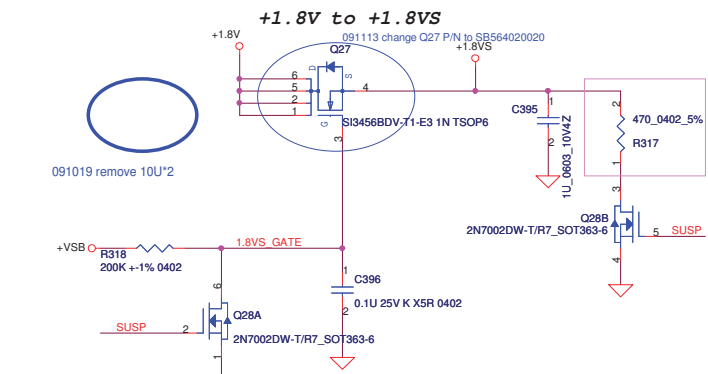
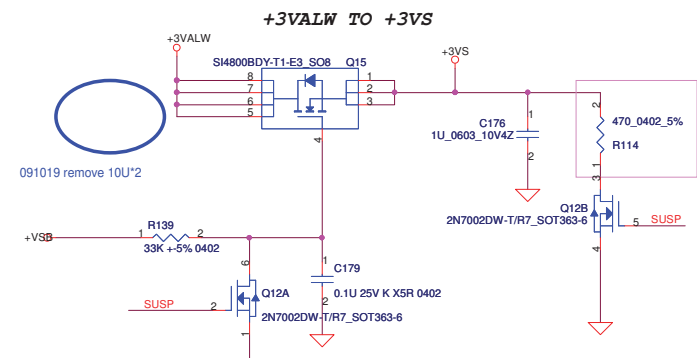
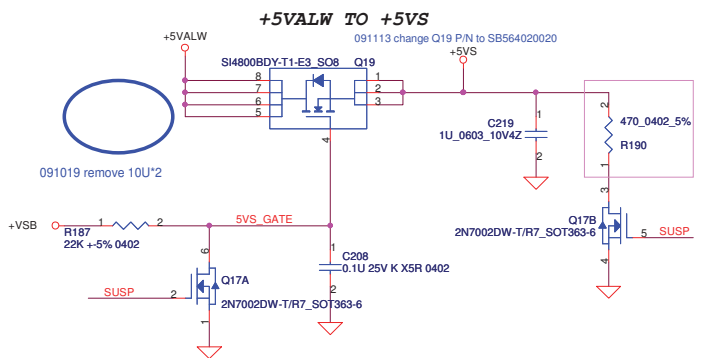
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091028 Modify Hole location by 1127_NAVD0_NEW_MB_ASSY_FOR_2865_v11



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				Date:	Wednesday, March 03, 2010	Sheet 33 of 46

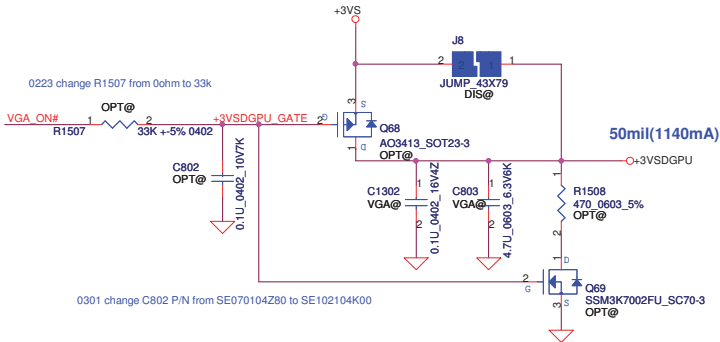


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				DC INTERFACE		
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				B	NAVDO LA-6091P	1.0
				Date:	Wednesday, March 03, 2010	ISheet 34 of 46

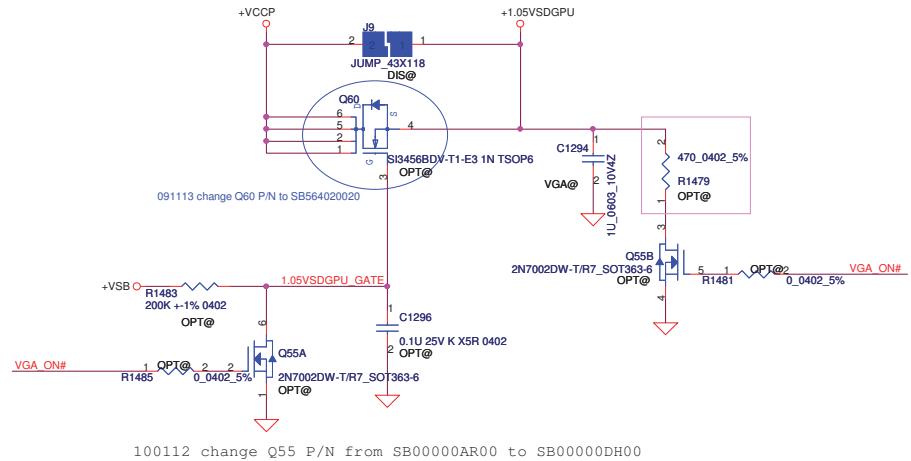
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+3VS to +3VSDGPU Transfer

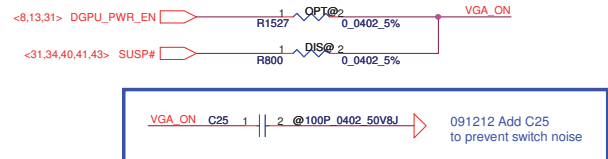
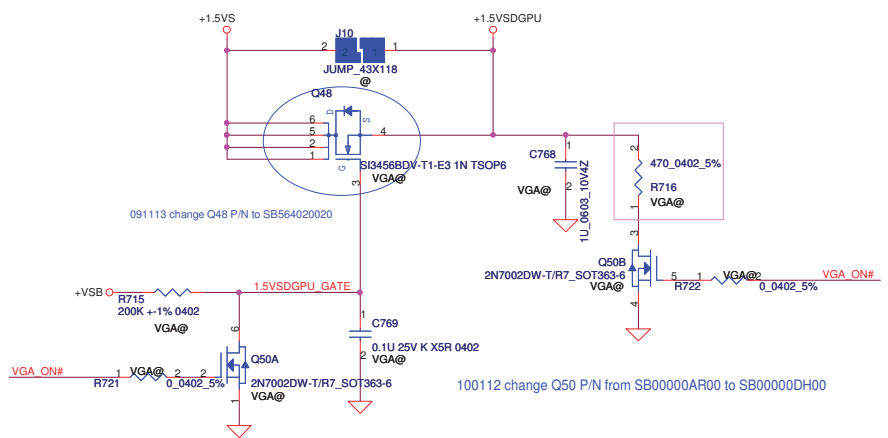
0111 Change BOM Structure of C1302/C803/C1303/C801/C1294 from OPT@ to VGA@



+VCCP to +1.05VSDGPU Transfer

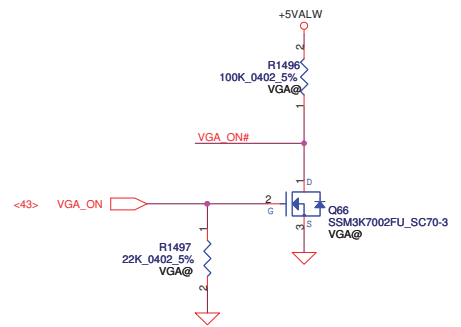
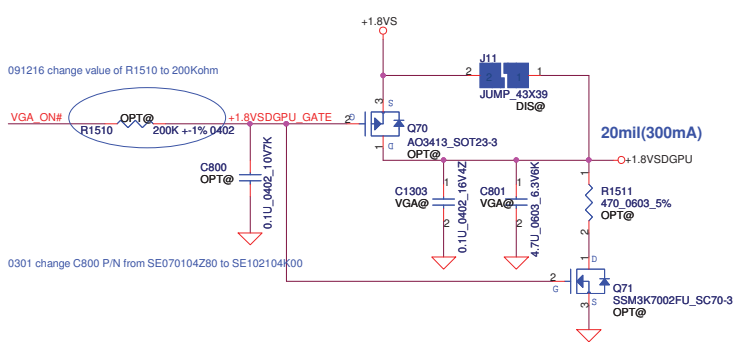


+1.5VS to +1.5VSDGPU Transfer

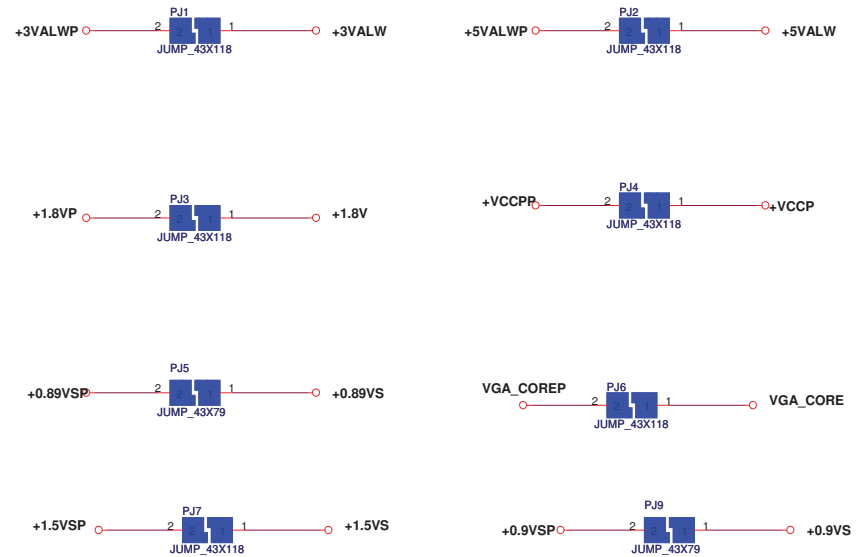
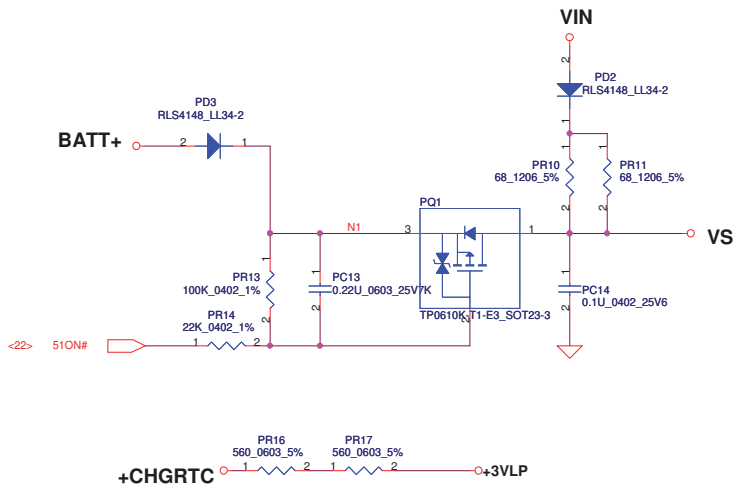
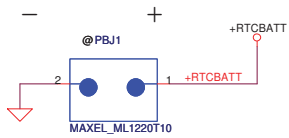
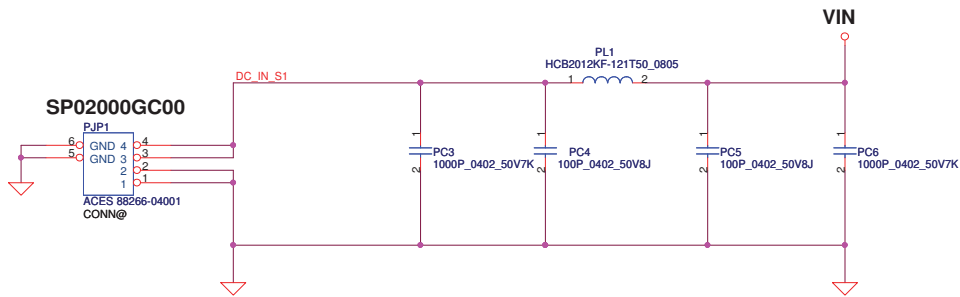


VGA_ON C25 1 2 @100P 0402 50V8J 091212 Add C25 to prevent switch noise

+1.8VS to +1.8VSDGPU Transfer

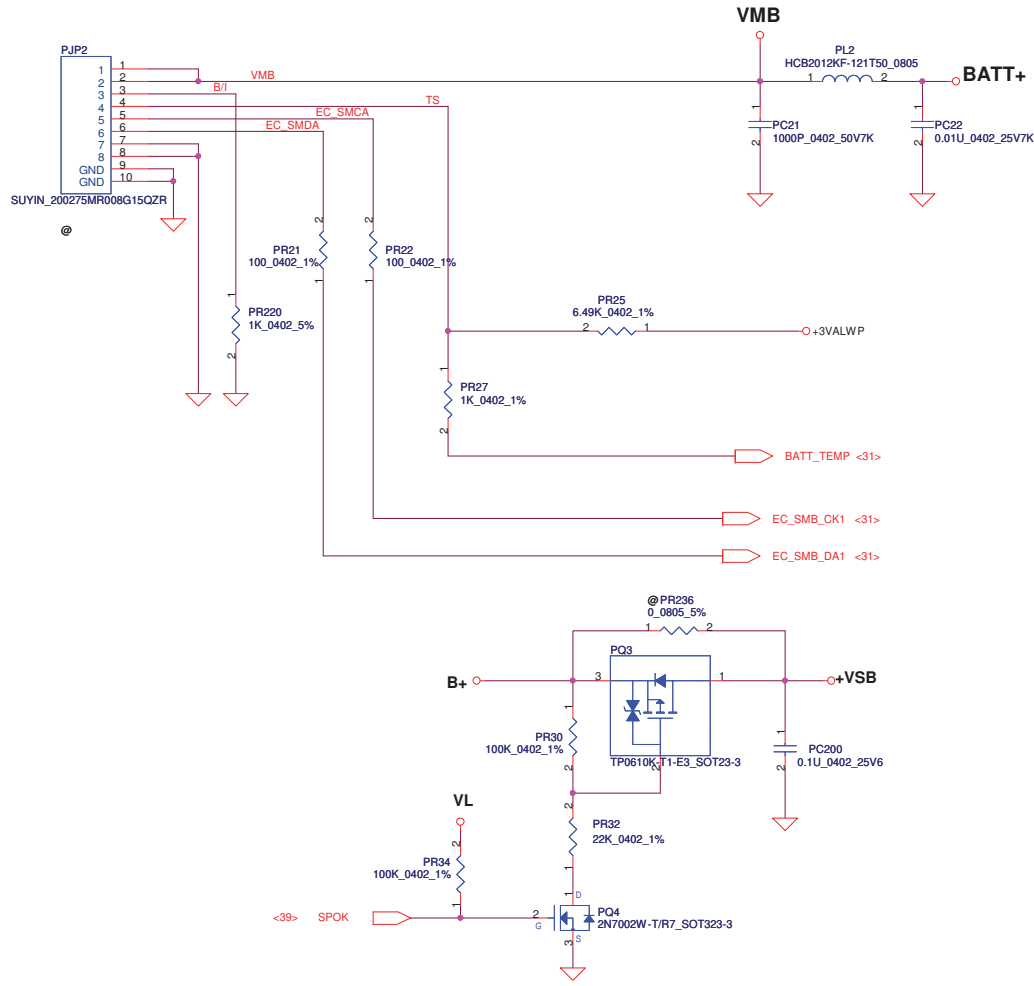


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				VGA DC INTERFACE				
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		Custom		NAVD0 LA-6091P		1.0		
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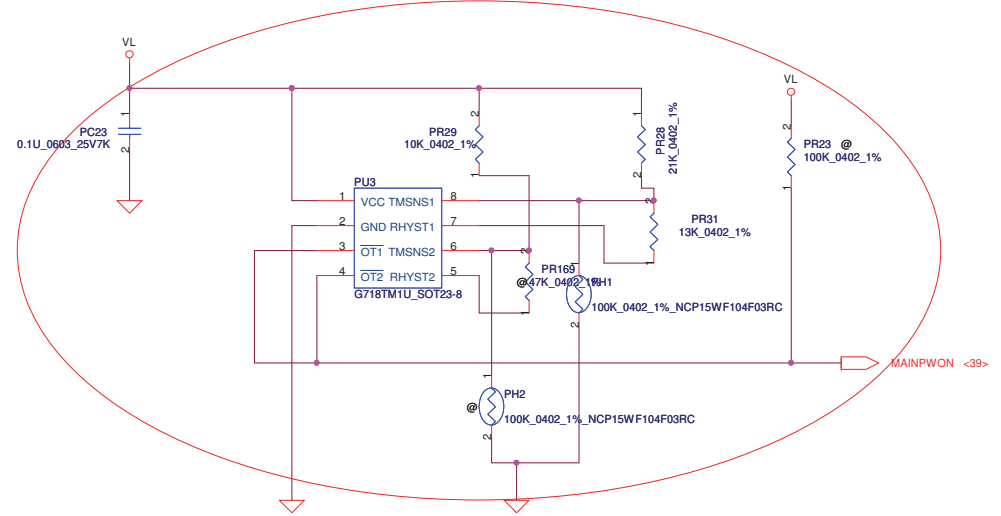


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Size	Document Number	NAVD0 LA-6091P		Rev	1.0
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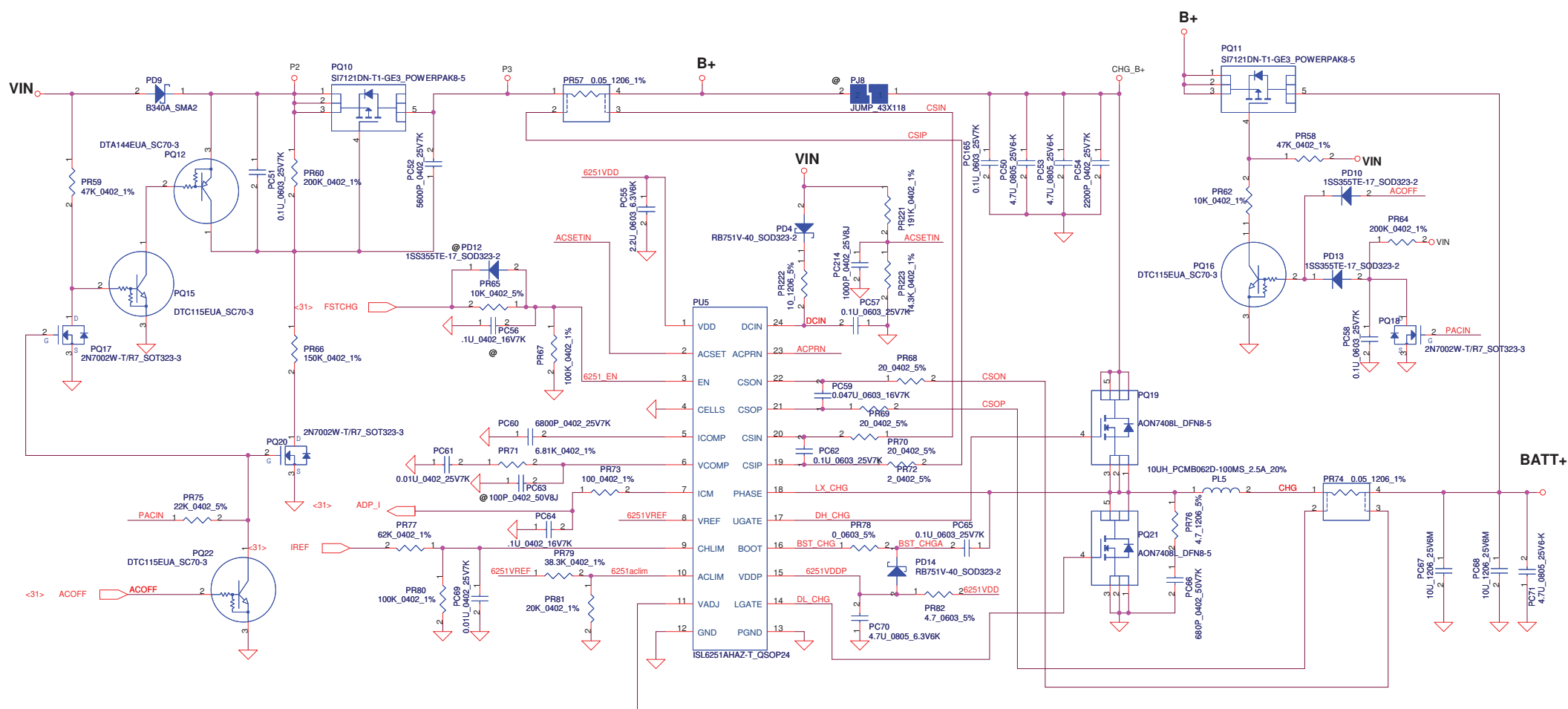


PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 70 degree C



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<http://laptop-motherboards.com/>



I_{ada}=0~1.58A(30W) CP = 85%*I_{ada} ; CP = 1.343A

CP mode
 $V_{acLim}=2.39 * (4.99K / (20K+4.99K)) = 1.876V$
 $I_{input} = (1/0.05) * ((0.05 * V_{acLim}) / 2.39 + 0.05) = 1.343A$

CC=0.3~1.76A
 $I_{REF}=1.62 * I_{charge}$
 $I_{REF}=0.486V \sim 2.85V$
 $3.24V \Rightarrow 2A$

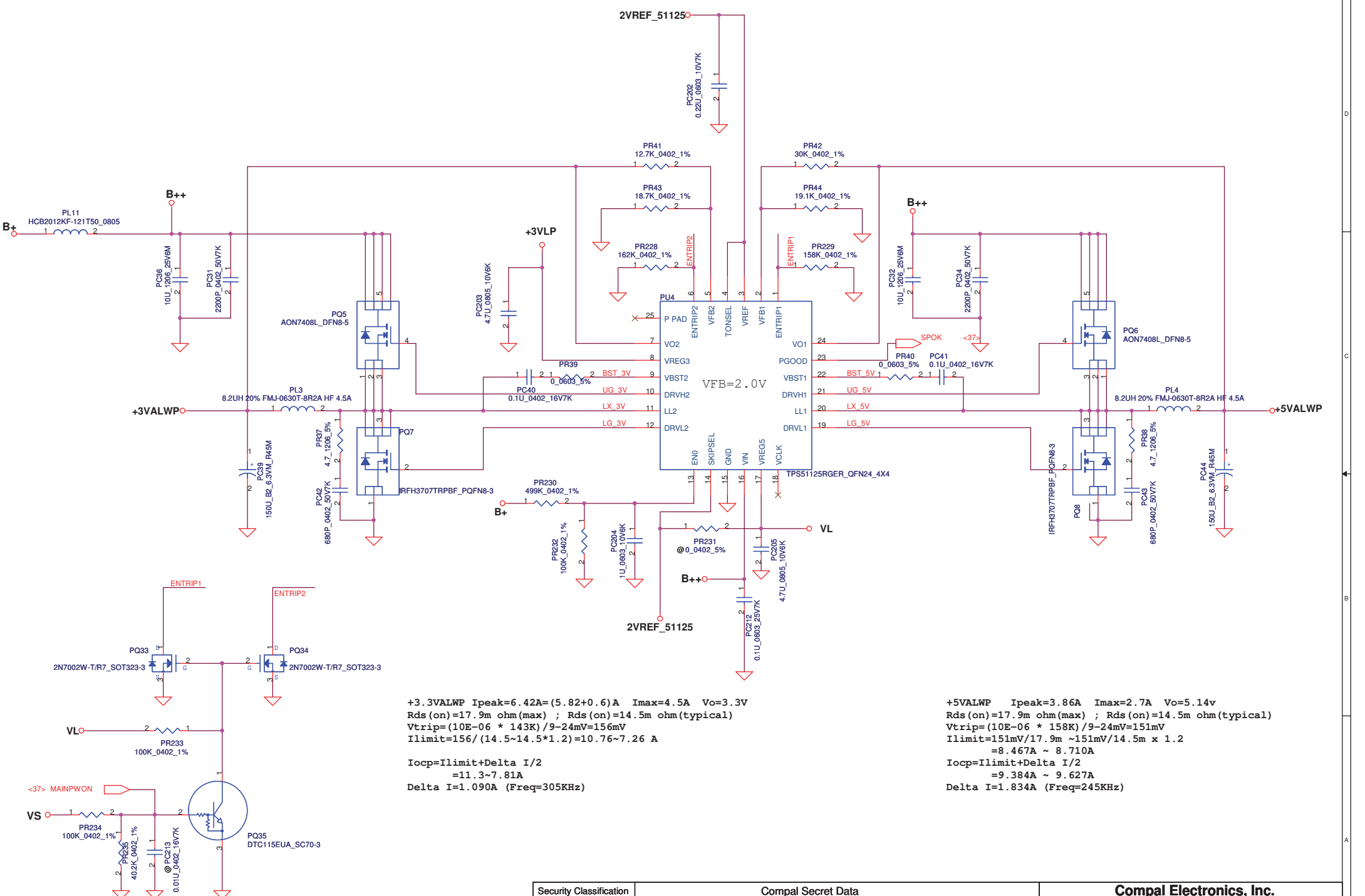
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ → VREF → 4.41V
 VADJ → Ground → 3.99V
 $V_{cell} = (0.175 * VADJ + 3.99)$

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Title: CHARGER			
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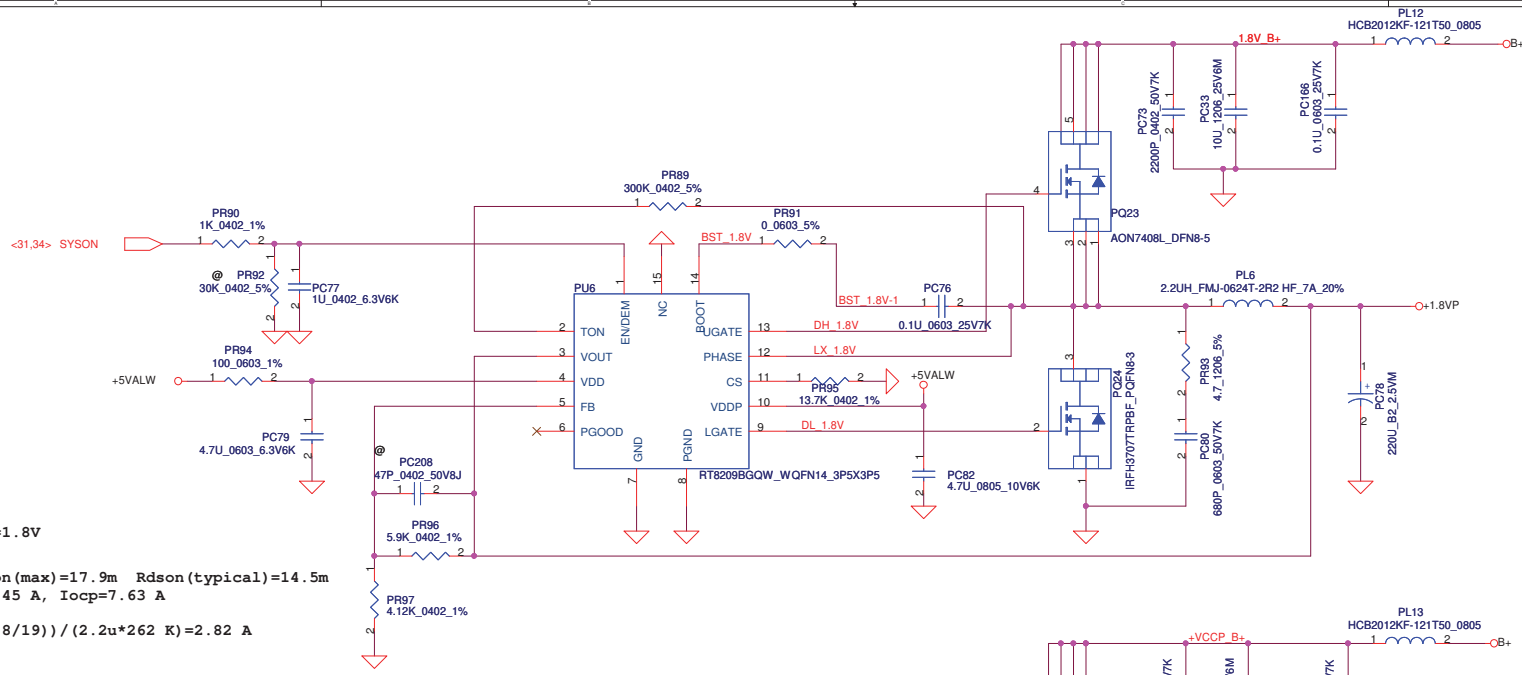


+3.3VALWP Ipeak=6.42A=(5.82+0.6)A Imax=4.5A Vo=3.3V
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
 Vtrip=(10E-06 * 143K)/9-24mV=156mV
 Ilimit=156/(14.5~14.5*1.2)=10.76~7.26 A

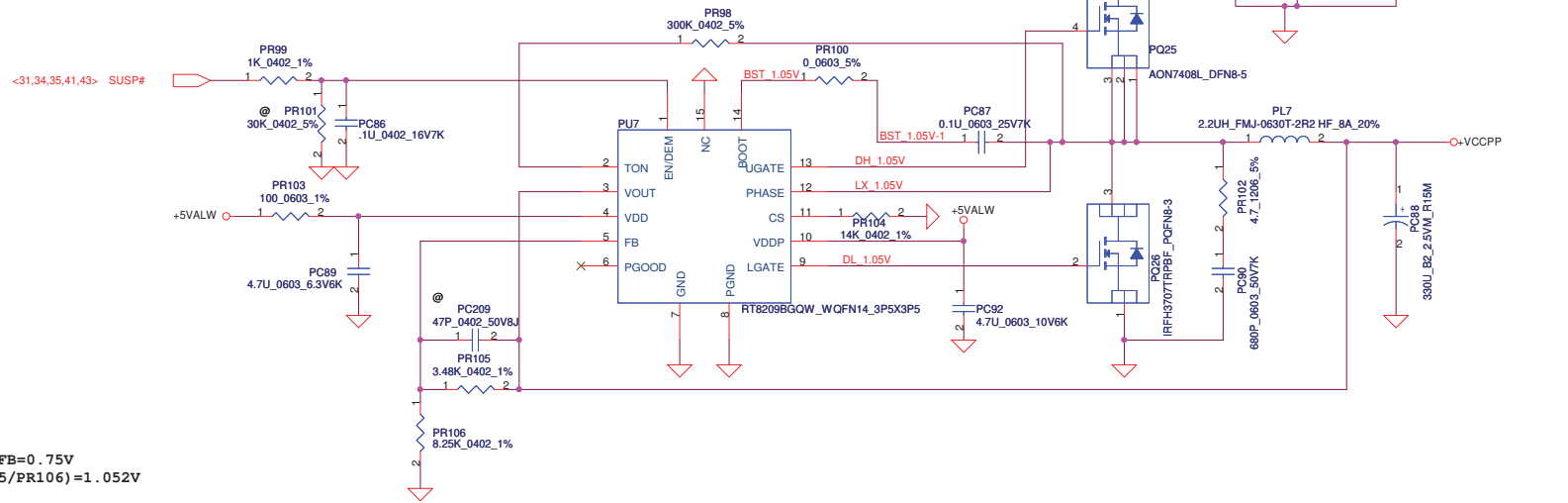
 Iocp=Ilimit+Delta I/2
 =11.3~7.81A
 Delta I=1.090A (Freq=305KHz)

+5VALWP Ipeak=3.86A Imax=2.7A Vo=5.14v
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
 Vtrip=(10E-06 * 158K)/9-24mV=151mV
 Ilimit=151mV/17.9m ~151mV/14.5m x 1.2
 =8.467A ~ 8.710A
 Iocp=Ilimit+Delta I/2
 =9.384A ~ 9.627A
 Delta I=1.834A (Freq=245KHz)

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				3V/5V	
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$<Vo=1.8V>$ $VFB=0.75V$
 $Vo=VFB*(1+PR96/PR97)=1.8V$
 $Fsw=262\text{ KHz}$
 $Cout\ ESR=15m\ \text{ohm}\ R_{dson}(max)=17.9m\ R_{dson}(typical)=14.5m$
 $I_{peak}=6.36\ \text{A},\ I_{max}=4.45\ \text{A},\ I_{ocp}=7.63\ \text{A}$
 $\Delta I = ((19-1.8)*(1.8/19))/(2.2u*262\ \text{K})=2.82\ \text{A}$
 $\Rightarrow 1/2\Delta I=1.41\ \text{A}$
 $V_{trip}=137mV$
 $I_{ocp}=V_{trip}/(R_{dson})+1.41$
 $=95.3/(17.9\sim 21.48)+1.41=9.07\sim 7.79$



$<Vo=1.052V>$ $VFB=0.75V$
 $Vo=VFB*(1+PR105/PR106)=1.052V$
 $Fsw=262\text{ KHz}$
 $Cout\ ESR=15m\ \text{ohm}\ R_{dson}(max)=17.9m\ R_{dson}(typical)=14.5m$
 $I_{peak}=6.1\ \text{A},\ I_{max}=4.27\ \text{A},\ I_{ocp}=7.32\ \text{A}$
 $\Delta I = ((19-1.05)*(1.05/19))/(2.2u*262\ \text{K})=1.72\ \text{A}$
 $\Rightarrow 1/2\Delta I=0.86\ \text{A}$
 $V_{trip}=14K*10uA=0.140\ \text{V}$
 $I_{ocp}=V_{trip}/(R_{dson})+0.86$
 $=113/(17.9\sim 21.48)+0.86=8.68\sim 7.37\ \text{A}$

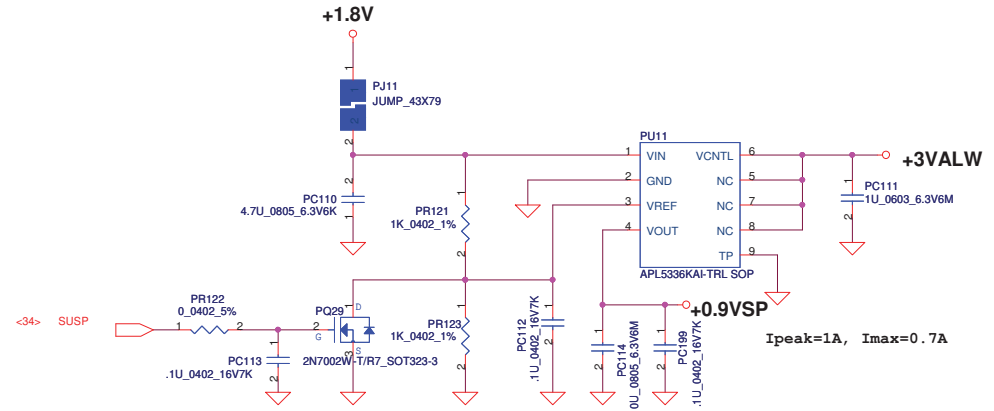
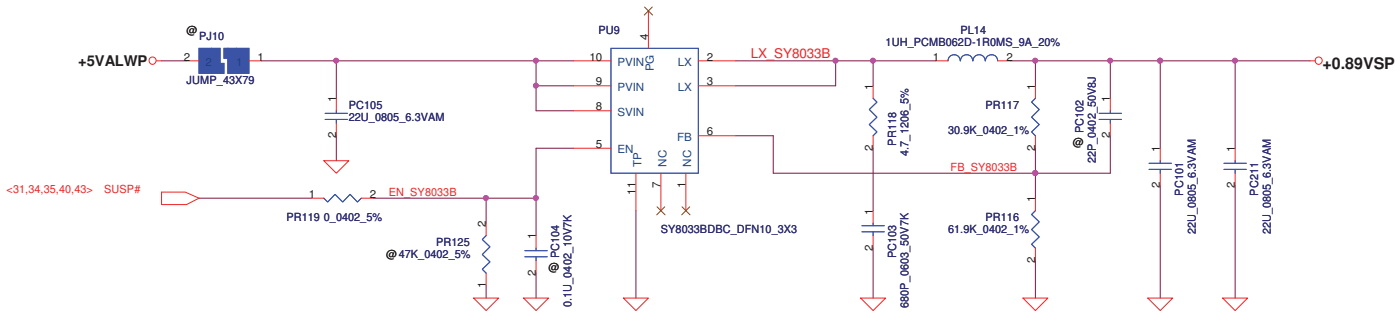
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Compal Electronics, Inc.			
Title VCCPP/1.8VP			
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<http://laptop-motherboard.com/>

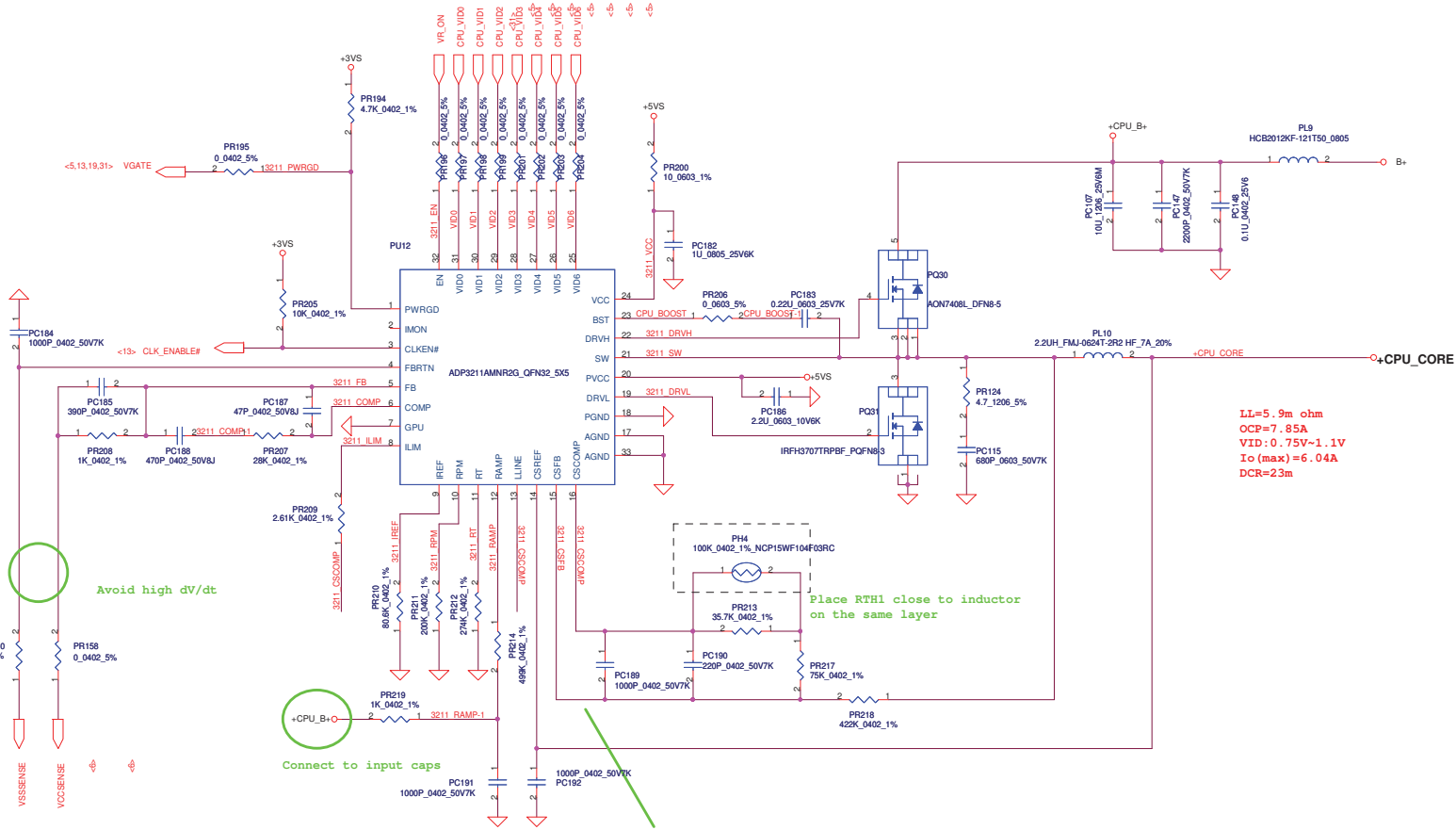
<Vo=0.89V> VFB=0.6V
 Vo=VFB*(1+PR117/PR116)=0.6*(1+30.1K/61.9K)=0.8917V

Ipeak=2.64A



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LL=5.9m ohm
 OCP=7.85A
 VID: 0.75V-1.1V
 Io(max)=6.04A
 DCR=23m

Avoid high dV/dt

Connect to input caps

Place RTH close to inductor on the same layer

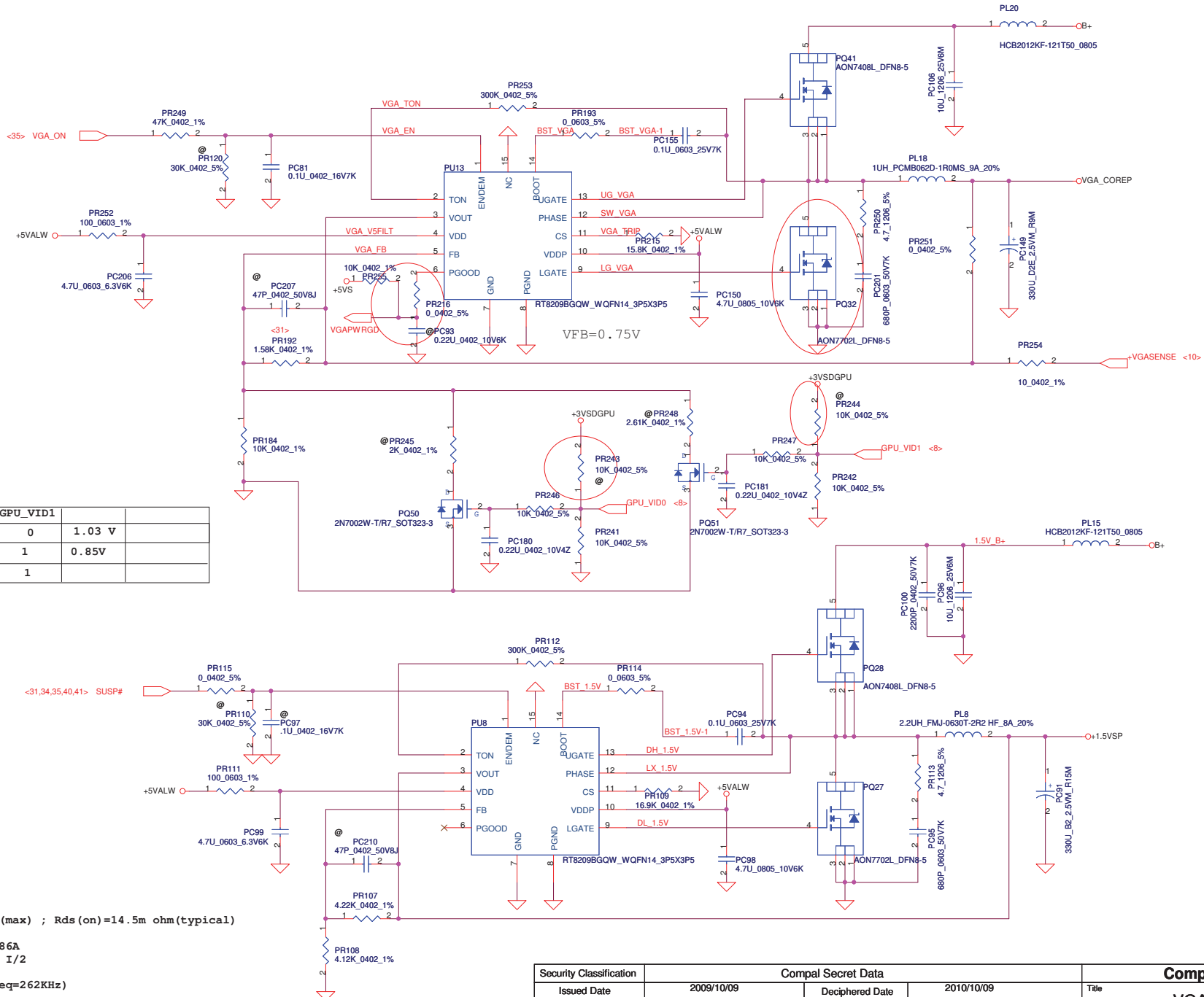
Shortest the net trace

<http://laptop-motherboard.com/>

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Ipeak=11.6 A
 Imax=8.15 A

delta I=3.27A 1/2 delta I=1.636 A
 Iocp=RTEIP*ITRIP/RDS(ON)+I/2 I=14~11.98 A
 Rds(on)=11~14m



GPU_VID0	GPU_VID1		
0	0	1.03 V	
0	1	0.85V	
1	1		

Vo=1.518V
 Fsw=262 KHz

Ipeak=8.62 A
 Imax=6.034 A
 Iocp=10.35 A

Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)

Ilimit=9.44A ~ 7.86A
 Iocp=Ilimit+Delta I/2
 =12~10.5A
 Delta I=5.27A (Freq=262KHz)

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<http://laptop-motherboards.com/>

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For save layout space and shortage	A		change PC50 PC53 to 0805 4.7u		
2		For VGA_core 51117 power good delay	A		Reserve PR216 PC93		
3		Save layout space	A		Delet PC35 PC36, change PC29 PC32 to 1206 10uF		
4		For cost down	A		change 0.89V from MP2121 to SY8033		
5		For cost down	A		delet Vin detector,battery OVP circuit		
6		For cost down	A		change 3V/5v from ISL6237 to TPS51125		
7		For Design change	A		change PR116 to 61.9K PR117 to 30.1K PL14 to 1uH		
8		For cost down	A		change 1.5V PL8 to 3mm height		
9		For cost down	A		change VCCP PL7 to 3mm height		
10		For Design change	A		change PQ31 to IRFH3707		
11		For Design change	A		change PQ23 PQ25 PQ28 PQ30 TO AON7408		
12		change 1.5V enable RC ,for HW request	A		change PR115 to 0 ohm ,unpop PR101		
13		change VCCP enable RC ,for HW request	A		change PR99 to 1k ohm ,pc86 to 0.1u,unpop PR110		
14		change VGACORE enable RC ,for HW request	A		change PR249 to 47k ohm ,pc81 to 0.1u,unpop PR120		
15		For charger ripple			Add PC71 4.7u 0805 25V		
16		For charger ripple			change PL5 to 10uF		
17		Buyer suggest			change PQ36 from 2N7002 TO SSM3K7002FU		
18		Fix VGA_VID at 0.85V			delete PR248 PR245 ,change PR192 to 1.58K		
19		OTP INPUT PULL HIGH resister			Add PR29		
20		change OTP set			change PR31 to 13K		
21		1.8V enable cap			Add PC77 1u 6.3v X5R		
22		51125 VL cap size up to 1206			change PC205 to 1206 size		
23		Buyer suggest			change PC96 PC106 PC107 from X6S to X5R		

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				PIR-PWR-1	
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http://laptop_motherboard_schema.blogspot.com/

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2009.6.30	EVT
2						2009.6.30	EVT
3						2009.7.2	EVT
4						2009.8.4	EVT
5						2009.8.12	EVT
6						2009.8.12	EVT
7						2009.8.12	EVT
8						2009.8.12	EVT
9						2009.8.24	EVT
10						2009.8.24	EVT
11						2009.8.24	EVT
12						2009.8.24	EVT
13						2009.8.24	EVT
14						2009.8.24	EVT
15						2009.8.27	EVT
16						2009.9.4	DVT
17						2009.9.10	DVT
18						2009.9.30	PVT
19							
20							
21							
22							
23							

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<http://laptop-motherboard-schematic.blogspot.com/>

<2009/4/28>
 Update new power schematic,
 release first version NAV50 schematic

<2009/04/29>
 . Add R1182 R1183 L3 on page 9
 . Change J3 to R1184 on page 13

<2009/04/30>
 . Change JDIM1 to SP07F001720 on page 7
 . Del SATA1 Port on page 12
 . Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
 . Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
 . Add CRT_DET# on page 10
 . Add CRT_DET# circuit on page 13
 . Add 3 LEDs on page 16
 . Add BT/BTN Board CONN. on page 16
 . Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
 . Add INVT_PWM on Page 5
 . Del R323 on page 5
 . C74 change to 2.2U_0603 on page 6
 . C267 change to 22U on page 6
 . C391 change to 0.1U on page 6
 . Del C67 C35 C33 C36 on page 6
 . Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
 . Follow Intel checklist, add R52 on FSB on page 8
 . Add D5 D7 D8 on page 4
 . Add R174 on page 9
 . Add PCI_RST# on page 11
 . Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
 . Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
 . Modify SRC CLK PORT LIST on page 8
 . Del CLKREQ_LAN# on page 8
 . Change PCIE Port list on page 13
 . Change USB Port list on page 13
 . Add W/L 3G SW on page 16
 . Del R103 on page 18

<2009/05/13>
 . Change JMINI1 to PCIE Port 3 on page 15

<2009/05/14>
 . Page8 Change C174 C175 to 10U_0603

<2009/05/14>
 . Update New Power schematic
 . Del R376 R377 on page 8
 . Del D5 D7 D8 on page 4
 . Change JLVDS1 to SP010006810 on page 9
 . Add D6 for EMI on page 9
 . Change C1106 to C_0603 type on page 9
 . Change USB_OC# on page 13
 . Add USB Port2 on page 20
 . Change JP11 Pin define & Add D22 on page 19
 . Change C512 to 1u_0402 on page 15
 . Add U29 (MEDIA_LED#) on page 16

<2009/05/19>
 .Update new clock GEN co-lay schematic on page 8

<2009/06/05>
 .Update new clock GEN co-lay schematic on page 8
 .Follow Intel check list change C161 C165 to 27P on page 8
 .Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
 .Update New Power schematic 06/06 version
 Page 13- a.Del R203 (pull-up GPIO6 Resistor)
 b.Change R1184 NU
 Page 17- a. Add VGATE
 b. Del R1294
 c. Change D30 NU
 d. Change R1295 to 0 ohm
 e. Add R1309 0 ohm on EC_RSMRST#
 f. Pull-up LAN_WAKE# +3VALW
 g. ICH_POK change to PCH_POK
 h. Pull-up KB_RST# to +3VS
 Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
 b. Add @ on U10 U11 C301 C298
 c. Del C302 C300 R1281 R1287

<2009/06/10>
 . Page 7- Add C116 @
 . Page 22- Modify USB_OC#1_2 to USB_OC#2
 . Page 17- Modify PLTRST# to PCI_RST#
 . Page 17- Add @ on R1311

<2009/06/12>
 . Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
 . Page8 Add C1145 C1146 C1147
 . Page10 Move CRT_DET# from Page13 to Page10
 . Page13 Add +RTCVCC circuit

<2009/06/15>
 . Update New Power schematic (change PBJ1 to PJP3)
 . Page 10 modify C310 C308 C303 C306 C304 Bom Structure
 . Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
 . Page7 Modify DDR Command Control Pin pull-high Resister location
 . Page9 Change R577 to 0402 type

<2009/06/17>
 . Update New Power schematic 06/17
 . Page9 modify LVDS Conn. Pin define
 . Page9 Del C1110
 . Page4 Add EMI solution D38 D39 D40

<2009/06/18>
 . Update New Power schematic 06/18
 . Page8 modify U4 Pin define and Q31
 . Page13 Add R1376, R1377
 . Page15 Modify C403
 . Page23 Modify H11

<2009/06/19>
 . Page4 Add new signal CPU_ITP , CPU_ITP#
 . Page5 ADD R1378
 . Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
 . Page7 DDR_A_D8與DDR_A_D9互換
 . Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
 . Page8 DEL C390
 . Page9 ADD C1156
 . Page11 DEL R1322, R1154
 . Page13 DEL U77, ADD C1158
 . Page17 ADD C1159

<2009/06/22>
 . Page22 change IO Conn. pin34 from 48M to USB_ON#
 . Page10 change JCR11 P/N to SP010906182

<2009/06/23>
 . Page15 Add C1163 C1164 C1165 C1166
 . Page18 change PWR/B Conn. P/N to SP01000H300
 . Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
 . Page8 Change C1350 C1351 to 0402 type
 . Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
 . Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B

<2009/06/29>
 . Page16 Change JP24 to ACES_88266_05001
 . Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
 . Page18 Change PWR_LED# to PWR_PWM_LED#
 . Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
 . Update New Power schematic 07/02
 . Page9 Add C1167 C1168 for RF request.
 . Page13 Change R223 to 100K
 . Page16 change JP24 to ACES_85201-0505N
 . Page17 Del R1387 R1388 on EC Pin97
 . Page17 Add New Board ID to separate NAV50 NAV60
 . Page17 Change 展頻IC to SA00003J400 (New)
 . Page18 Add D41 for ESD

<2009/07/03>
 . Page18 Add D41.2 to PWR_PWM_LED#
 . Page8 Change co-lay net name to +1.5VM_CK505
 . Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
 . Page18 Add pwr switch for NAV50

<2009/07/08>
 . Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
 . Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
 . Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
 . Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
 . Page18 Del D41

<2009/09/03>
 . Page7 Change C112 to 0402 type
 . Page8 Add T6 on CLK_48M_CR
 . Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
 . Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
 . Page21 Del H12

<2009/09/08>
 Update Power schematic 0904
 . Page18 Change R1388 to 100 ohm 0402
 . Page18 Change LED1 to SC591NB5A00

<2009/09/10>
 Update Power schematic 0910
 . Page22 unmount Q6 Q8

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