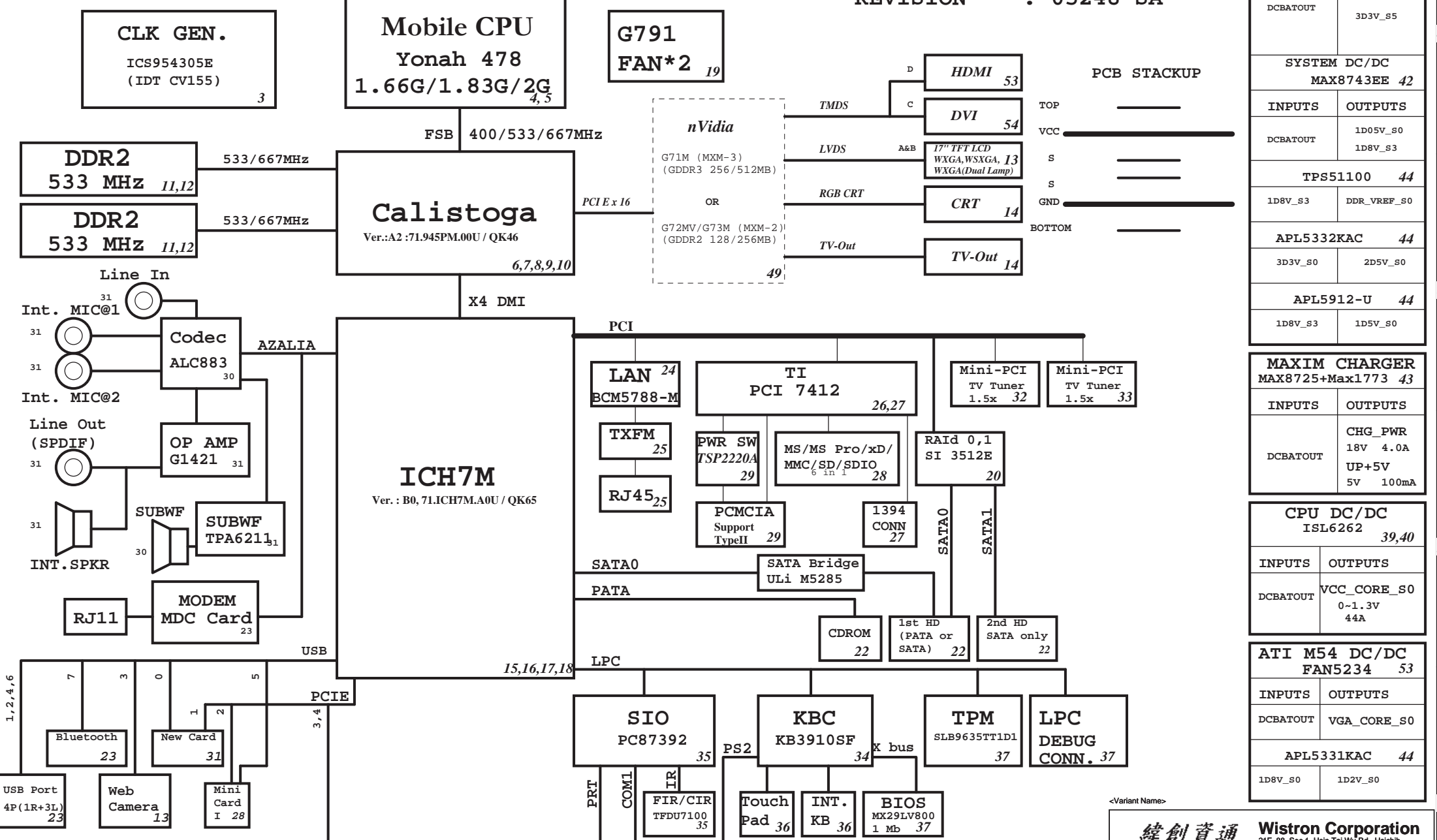


Kirkini Block Diagram

(Discrete)

Project code: 91.4G801.001
 PCB P/N :
 REVISION : 05248-SA



G791 FAN*2 19

nVidia
 G71M (MXM-3) (GDDR3 256/512MB)
 OR
 G72MV/G73M (MXM-2) (GDDR2 128/256MB)

HDMI 53
DVI 54
17" TFT LCD WXGA, WSXGA, 13 WXGA (Dual Lamp)
CRT 14
TV-Out 14

PCB STACKUP
 TOP
 VCC
 S
 S
 GND
 BOTTOM

SYSTEM DC/DC TPS51120 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC MAX8743EE 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100 44	
1D8V_S3	DDR_VREF_S0
APL5332KAC 44	
3D3V_S0	2D5V_S0
APL5912-U 44	
1D8V_S3	1D5V_S0

MAXIM CHARGER MAX8725+Max1773 43	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 39,40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 44A

ATI M54 DC/DC FAN5234 53	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0
APL5331KAC 44	
1D8V_S0	1D2V_S0

Easy Port 4 (124 PIN)
 AC IN RJ45-11 SERIAL PORT CRT PRINTER PS2 MIC LINE IN LINE TV DVI PCIE*2 SMBUS
 38, 39

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Title: **BLOCK DIAGRAM**

Size A3 Document Number: **Kirkini** Rev: **SA**

Date: Monday, February 20, 2006 Sheet 1 of 56

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

page 3

PCI Routing

DEVICE	IDSEL	INT -> PIRQ	REQ/GNT
MiniPCI Slot 1 & Slot 2	AD21	A/C-E B/D-E	REQ1# / GNT1#
Cardbus Controller TI7412	AD22	A-G B-B C-F D-G	REQ0# / GNT0#
RAID	AD20	A-A	REQ3# / GNT3#
LAN	AD23	A-H	REQ2# / GNT2#

History

Calistoga Strapping Signals and Configuration

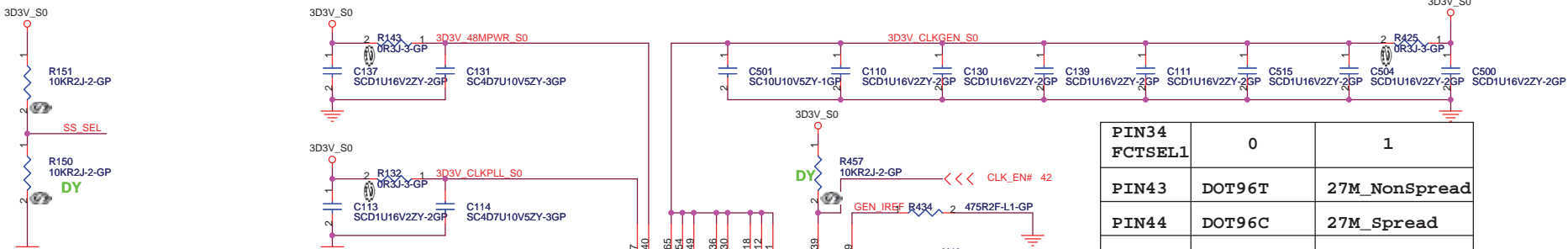
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

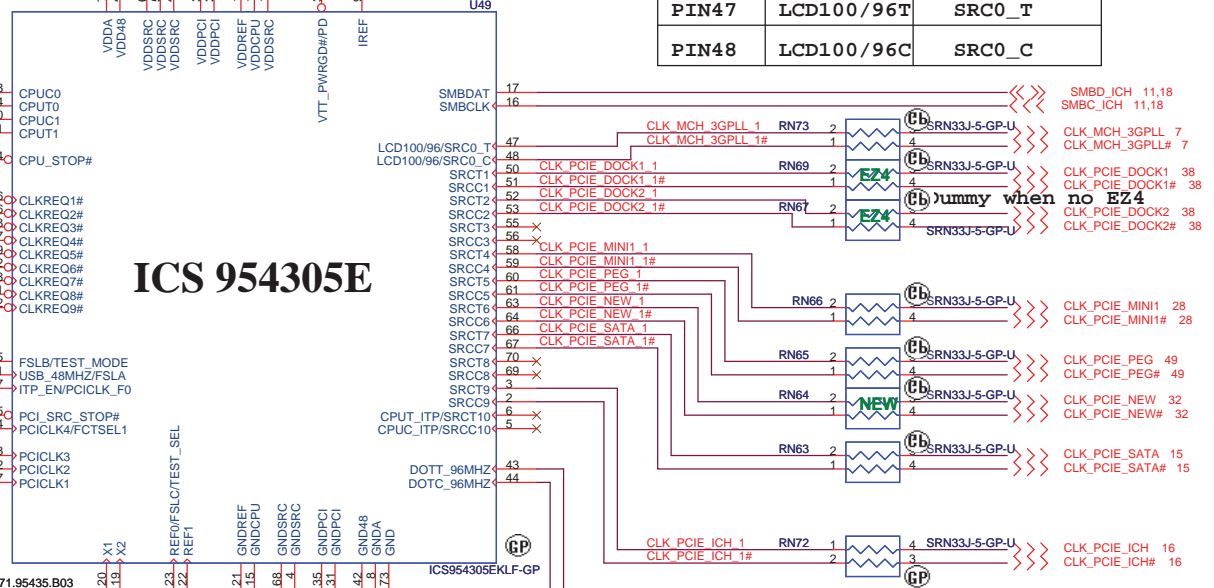
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Reference			
Size A3	Document Number	Kirkini	Rev SA
Date: Monday, February 20, 2006	Sheet 2	of	56

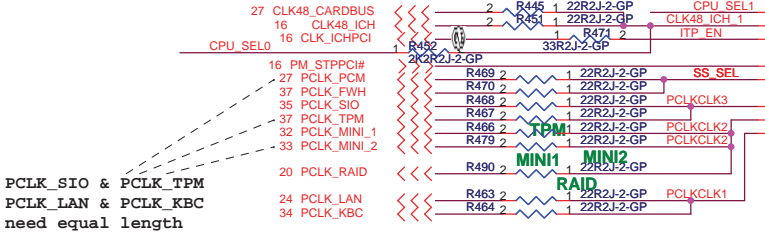


PIN#	FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread	
PIN44	DOT96C	27M_Spread	
PIN47	LCD100/96T	SRC0_T	
PIN48	LCD100/96C	SRC0_C	

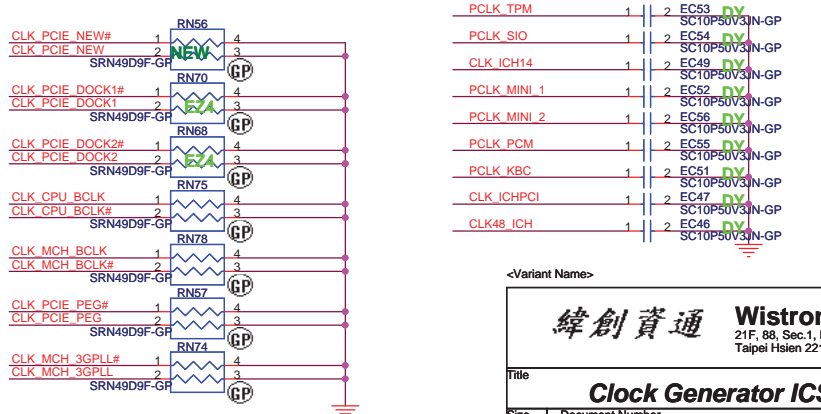
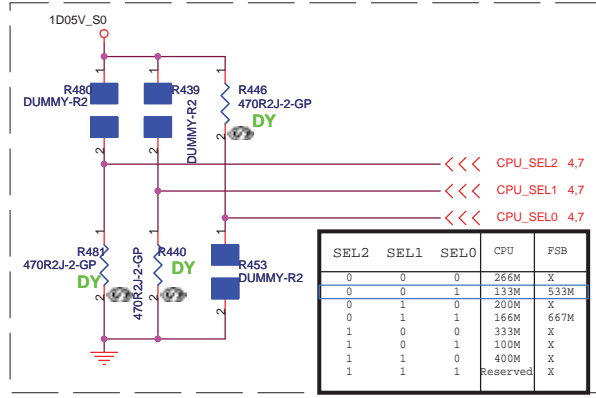
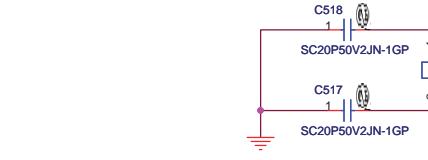
ICS 954305E




Smbus Table:
 Byte12 bit 0-7 & Byte13 bit7.
 "0": not controlled, "1": controlled.



PCLK_SIO & PCLK_TPM
 PCLK_LAN & PCLK_KBC
 need equal length

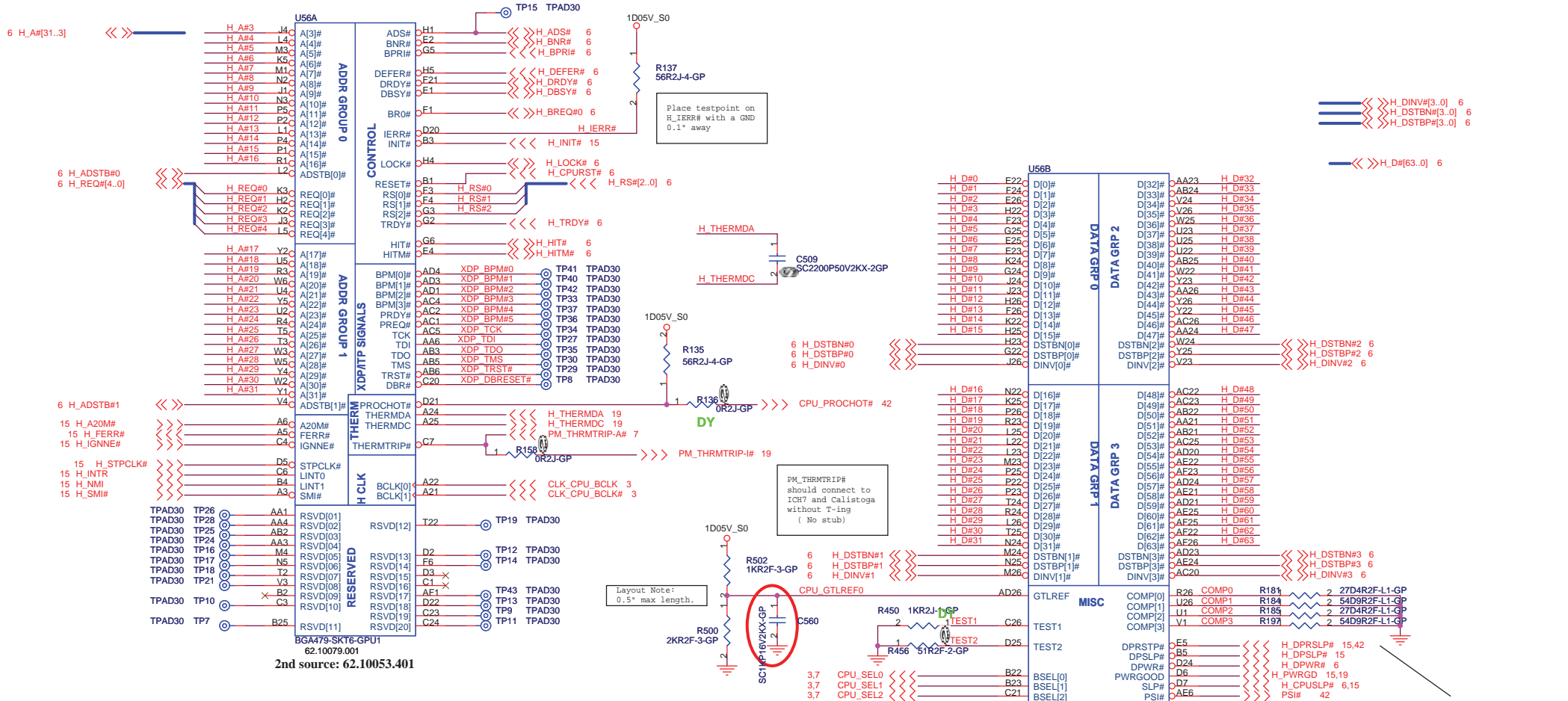


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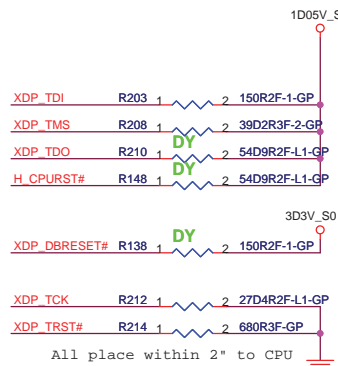


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Clock Generator ICS954305D			
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2nd source: 62.10053.401



All place within 2" to CPU

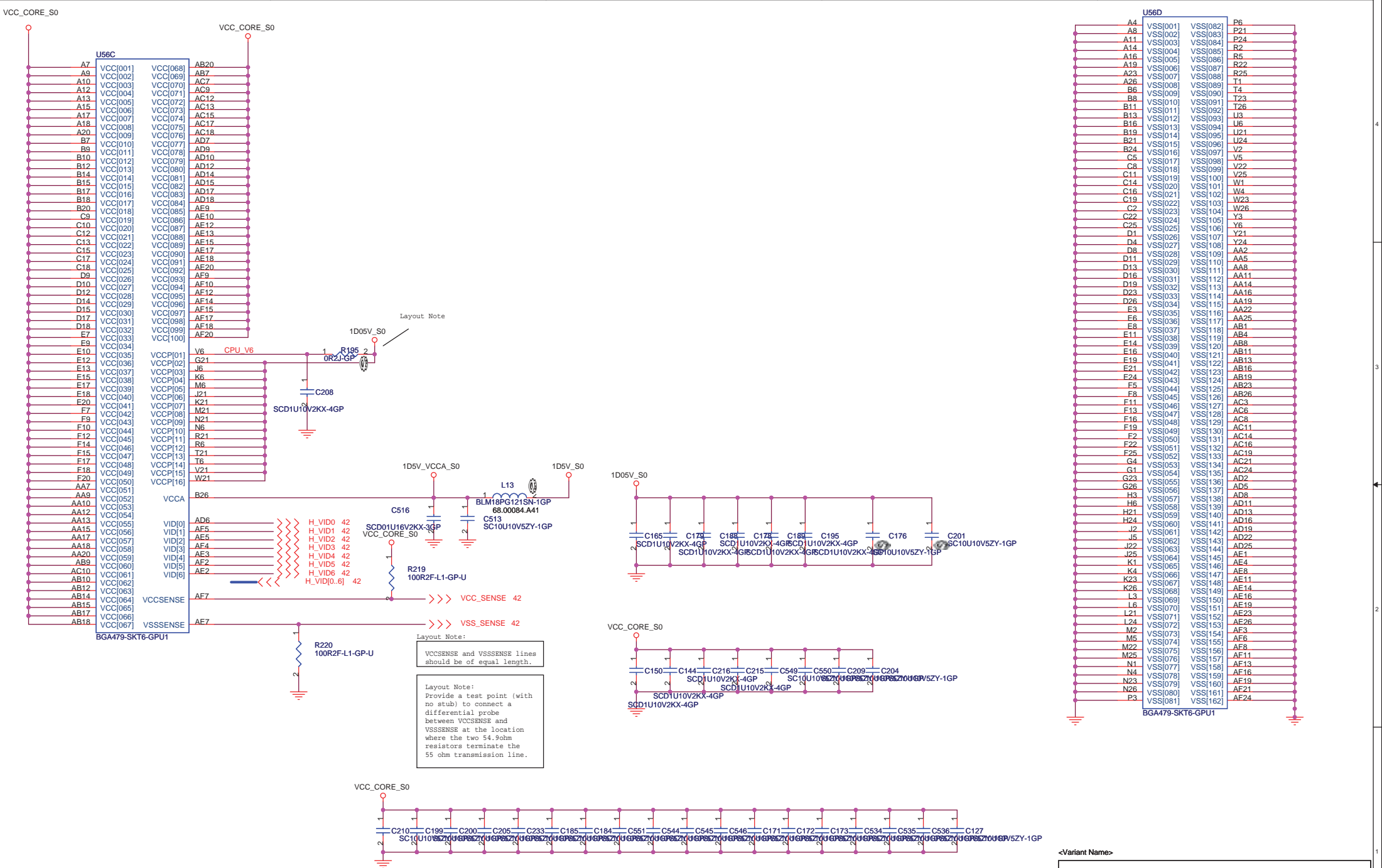
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

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Title: **CPU (1 of 2)**

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Date: Monday, February 20, 2006 Sheet 4 of 56



Layout Note:
 VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
 Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

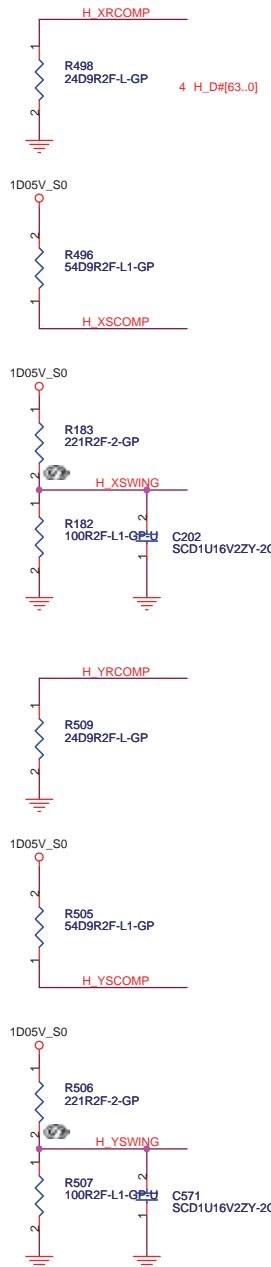
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Title: **CPU (2 of 2)**

Size A3 Document Number **Kirkini** Rev **SA**

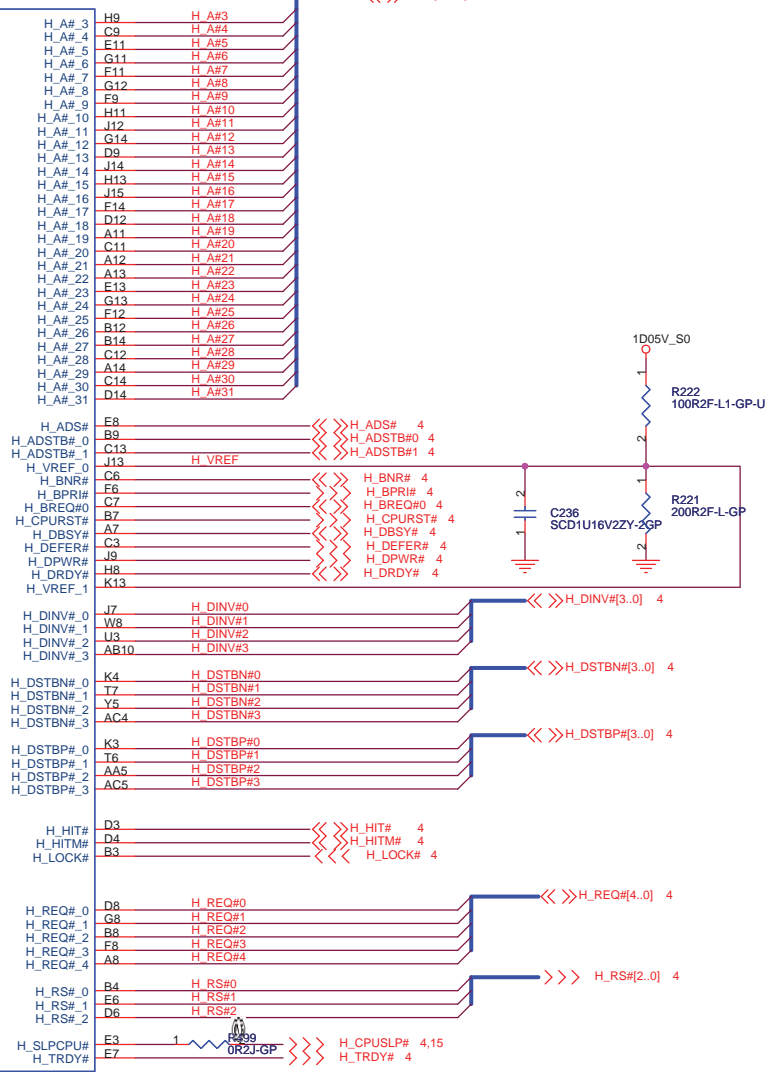
Date: Monday, February 20, 2006 Sheet 5 of 56



Place them near to the chip (< 0.5")

U58A		CALISTOGA	
H_D#0	F1	H_D#0	F1
H_D#1	J1	H_D#1	J1
H_D#2	H1	H_D#2	H1
H_D#3	J6	H_D#3	J6
H_D#4	H3	H_D#4	H3
H_D#5	K2	H_D#5	K2
H_D#6	G1	H_D#6	G1
H_D#7	G2	H_D#7	G2
H_D#8	K9	H_D#8	K9
H_D#9	K1	H_D#9	K1
H_D#10	K7	H_D#10	K7
H_D#11	J8	H_D#11	J8
H_D#12	H4	H_D#12	H4
H_D#13	J3	H_D#13	J3
H_D#14	K11	H_D#14	K11
H_D#15	G4	H_D#15	G4
H_D#16	T10	H_D#16	T10
H_D#17	W11	H_D#17	W11
H_D#18	T3	H_D#18	T3
H_D#19	U7	H_D#19	U7
H_D#20	U9	H_D#20	U9
H_D#21	U11	H_D#21	U11
H_D#22	T11	H_D#22	T11
H_D#23	W9	H_D#23	W9
H_D#24	T1	H_D#24	T1
H_D#25	T8	H_D#25	T8
H_D#26	T4	H_D#26	T4
H_D#27	W7	H_D#27	W7
H_D#28	U5	H_D#28	U5
H_D#29	T9	H_D#29	T9
H_D#30	W6	H_D#30	W6
H_D#31	T5	H_D#31	T5
H_D#32	AB7	H_D#32	AB7
H_D#33	AA9	H_D#33	AA9
H_D#34	W4	H_D#34	W4
H_D#35	W3	H_D#35	W3
H_D#36	Y3	H_D#36	Y3
H_D#37	Y7	H_D#37	Y7
H_D#38	W5	H_D#38	W5
H_D#39	Y10	H_D#39	Y10
H_D#40	AB8	H_D#40	AB8
H_D#41	W2	H_D#41	W2
H_D#42	AA4	H_D#42	AA4
H_D#43	AA7	H_D#43	AA7
H_D#44	AA2	H_D#44	AA2
H_D#45	AA6	H_D#45	AA6
H_D#46	AA10	H_D#46	AA10
H_D#47	Y8	H_D#47	Y8
H_D#48	AA1	H_D#48	AA1
H_D#49	AB4	H_D#49	AB4
H_D#50	AC9	H_D#50	AC9
H_D#51	AB11	H_D#51	AB11
H_D#52	AC11	H_D#52	AC11
H_D#53	AB3	H_D#53	AB3
H_D#54	AC2	H_D#54	AC2
H_D#55	AD1	H_D#55	AD1
H_D#56	AD9	H_D#56	AD9
H_D#57	AC1	H_D#57	AC1
H_D#58	AD7	H_D#58	AD7
H_D#59	AC6	H_D#59	AC6
H_D#60	AB5	H_D#60	AB5
H_D#61	AD10	H_D#61	AD10
H_D#62	AD4	H_D#62	AD4
H_D#63	AC8	H_D#63	AC8
H_XRCOMP	E1	H_XRCOMP	E1
H_XSCOMP	E2	H_XSCOMP	E2
H_XSWING	E4	H_XSWING	E4
H_YRCOMP	Y1	H_YRCOMP	Y1
H_YSCOMP	U11	H_YSCOMP	U11
H_YSWING	W1	H_YSWING	W1
3 CLK_MCH_BCLK	AG2	H_CLKIN	AG2
3 CLK_MCH_BCLK#	AG1	H_CLKIN#	AG1

HOST



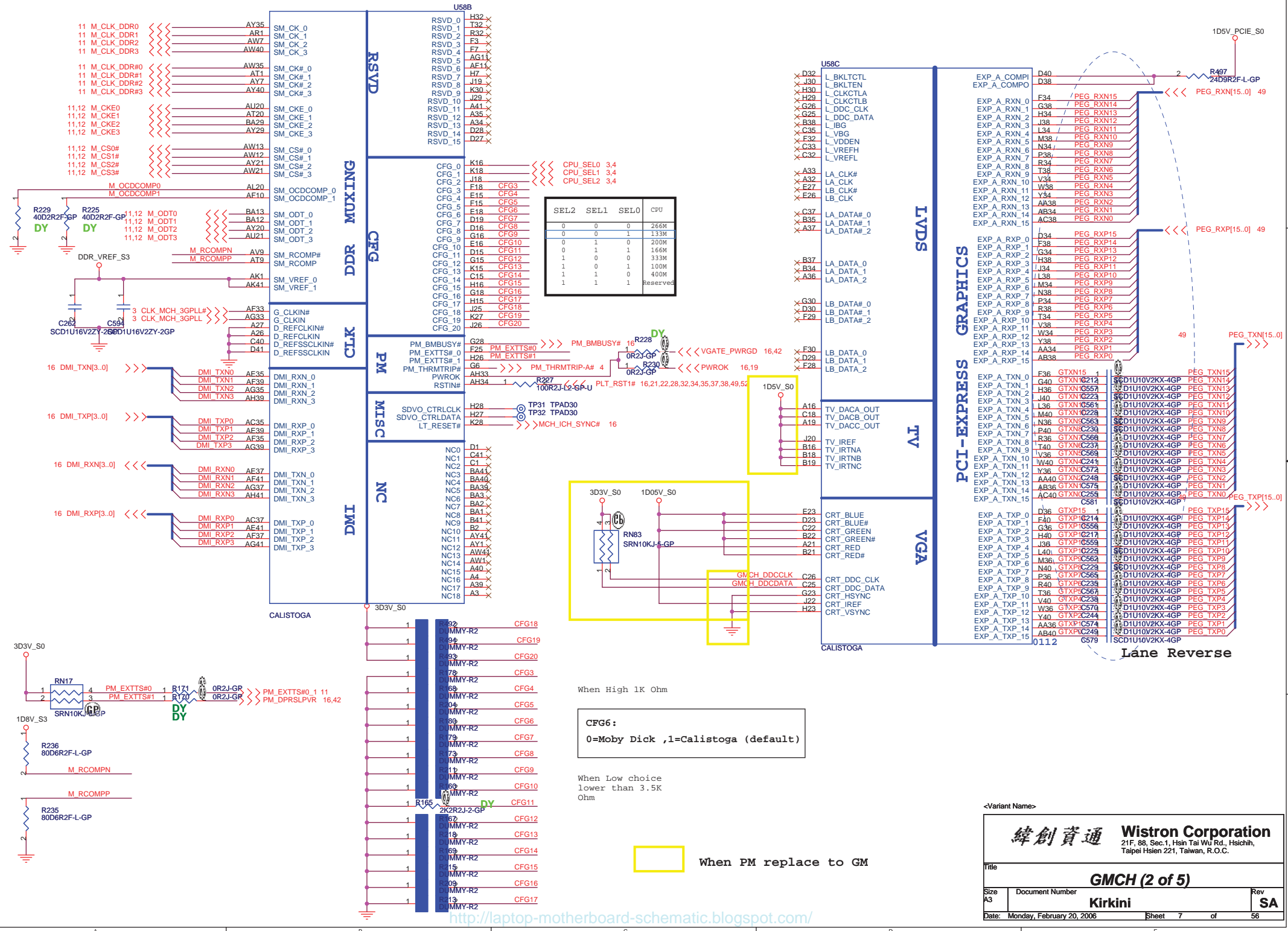
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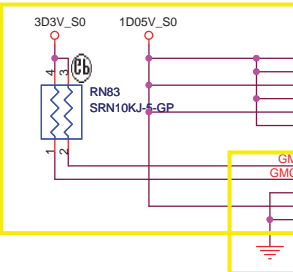
Title: **GMCH (1 of 5)**

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SEL2	SEL1	SEL0	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



When High 1K Ohm

CFG6:
0=Moby Dick ,1=Calistoga (default)

When Low choice lower than 3.5K Ohm

When PM replace to GM

Lane Reverse

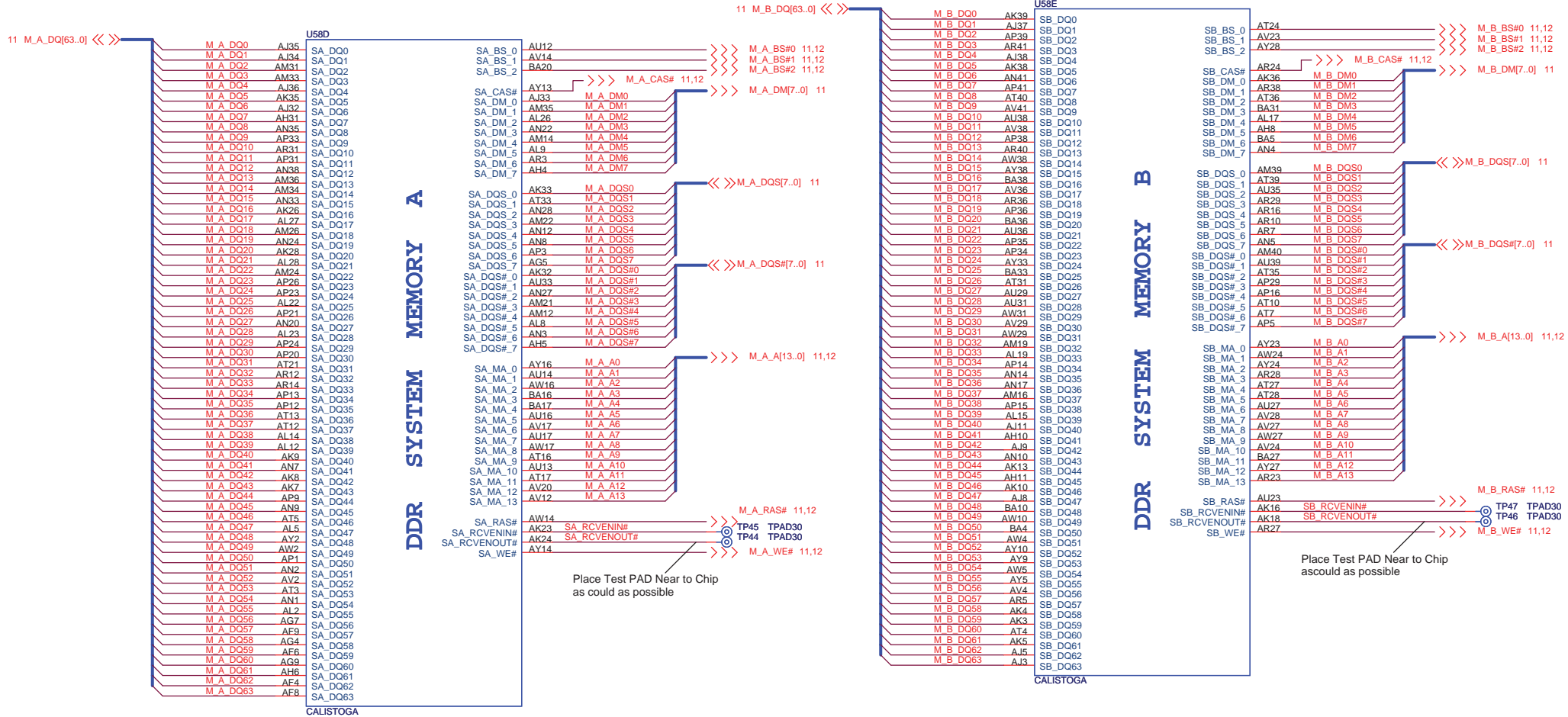
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Title: **GMCH (2 of 5)**

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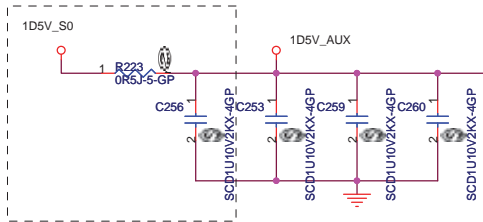
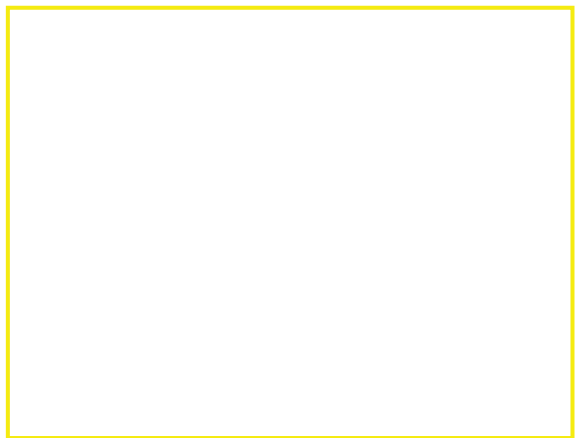
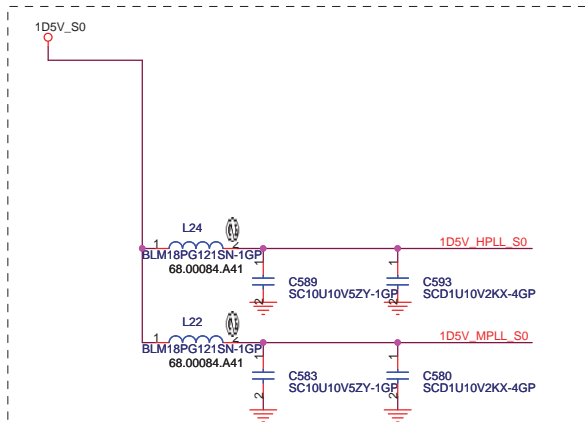
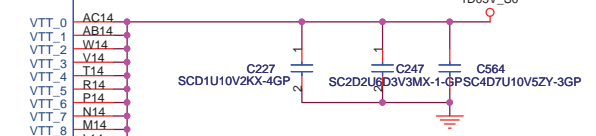
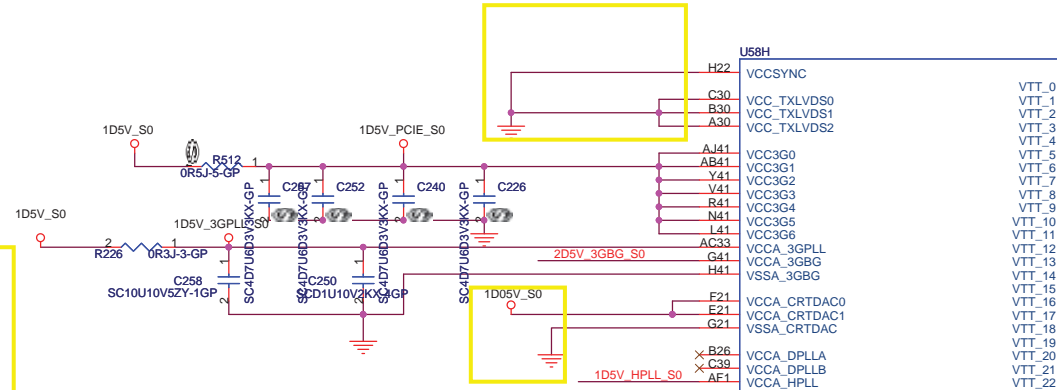
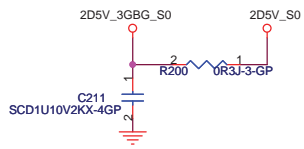
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Title: **GMCH (3 of 5)**

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- U58H**
- H22 VCCSYNCR
 - C30 VCC_TXLVD50
 - B30 VCC_TXLVD51
 - A30 VCC_TXLVD52
 - A41 VCC3G0
 - AB41 VCC3G1
 - Y41 VCC3G2
 - V41 VCC3G3
 - R41 VCC3G4
 - M41 VCC3G5
 - L41 VCC3G6
 - AC33 VCCA_3GPLL
 - G41 VCCA_3GBG
 - H41 VSSA_3GBG
 - E21 VCCA_CRTDAC0
 - E21 VCCA_CRTDAC1
 - G21 VSSA_CRTDAC
 - B26 VCCA_DPLLA
 - C39 VCCA_DPLLB
 - AF1 VCCA_HPLL
 - A38 VCCA_LVDS
 - B39 VSSA_LVDS
 - AF2 VCCA_MPLL
 - H20 VCCA_TVBG
 - G20 VSSA_TVBG
 - E19 VCCA_TVDACA0
 - E19 VCCA_TVDACA1
 - C20 VCCA_TVDACB0
 - D20 VCCA_TVDACB1
 - E20 VCCA_TVDACC0
 - F20 VCCA_TVDACC1
 - AH1 VCCD_HMPLL0
 - AH2 VCCD_HMPLL1
 - A28 VCCD_LVDS0
 - B28 VCCD_LVDS1
 - C28 VCCD_LVDS2
 - D21 VCCD_TVDAC
 - A23 VCC_HV0
 - B23 VCC_HV1
 - B25 VCC_HV2
 - H19 VCCD_QTVDAC
 - AK31 VCCAUX0
 - AF31 VCCAUX1
 - AE31 VCCAUX2
 - AC31 VCCAUX3
 - AL30 VCCAUX4
 - AK30 VCCAUX5
 - AJ30 VCCAUX6
 - AH30 VCCAUX7
 - AG30 VCCAUX8
 - AF30 VCCAUX9
 - AE30 VCCAUX10
 - AD30 VCCAUX11
 - AC30 VCCAUX12
 - AC29 VCCAUX13
 - AF29 VCCAUX14
 - AD29 VCCAUX15
 - AC29 VCCAUX16
 - AG28 VCCAUX17
 - AG28 VCCAUX18
 - AE28 VCCAUX19
 - AE28 VCCAUX20
 - AH22 VCCAUX21
 - AJ21 VCCAUX22
 - AH21 VCCAUX23
 - AJ20 VCCAUX24
 - AH19 VCCAUX25
 - P19 VCCAUX26
 - P16 VCCAUX27
 - AH15 VCCAUX28
 - AH15 VCCAUX29
 - P15 VCCAUX30
 - AH14 VCCAUX31
 - AC14 VCCAUX32
 - AE14 VCCAUX33
 - Y14 VCCAUX34
 - Y14 VCCAUX35
 - AE13 VCCAUX36
 - AE13 VCCAUX37
 - AE12 VCCAUX38
 - AE12 VCCAUX39
 - AD12 VCCAUX40

- VTT_0 AC14
- VTT_1 AB14
- VTT_2 W14
- VTT_3 Y14
- VTT_4 T14
- VTT_5 R14
- VTT_6 P14
- VTT_7 N14
- VTT_8 M14
- VTT_9 L14
- VTT_10 AD13
- VTT_11 AC13
- VTT_12 AB13
- VTT_13 AA13
- VTT_14 Y13
- VTT_15 W13
- VTT_16 V13
- VTT_17 T13
- VTT_18 R13
- VTT_19 P13
- VTT_20 N13
- VTT_21 M13
- VTT_22 L13
- VTT_23 AB12
- VTT_24 AA12
- VTT_25 Y12
- VTT_26 W12
- VTT_27 V12
- VTT_28 U12
- VTT_29 T12
- VTT_30 P12
- VTT_31 N12
- VTT_32 M12
- VTT_33 L12
- VTT_34 R11
- VTT_35 P11
- VTT_36 N11
- VTT_37 M11
- VTT_38 R10
- VTT_39 P10
- VTT_40 N10
- VTT_41 M10
- VTT_42 P9
- VTT_43 N9
- VTT_44 M9
- VTT_45 R8
- VTT_46 P8
- VTT_47 N8
- VTT_48 M8
- VTT_49 P7
- VTT_50 N7
- VTT_51 M7
- VTT_52 R6
- VTT_53 P6
- VTT_54 M6
- VTT_55 A6
- VTT_56 R5
- VTT_57 P5
- VTT_58 N5
- VTT_59 M5
- VTT_60 P4
- VTT_61 N4
- VTT_62 M4
- VTT_63 R3
- VTT_64 P3
- VTT_65 N3
- VTT_66 M3
- VTT_67 R2
- VTT_68 P2
- VTT_69 M2
- VTT_70 D2
- VTT_71 AB1
- VTT_72 AB1
- VTT_73 P1
- VTT_74 N1
- VTT_75 M1
- VTT_76 M1



POWER

CALISTOGA

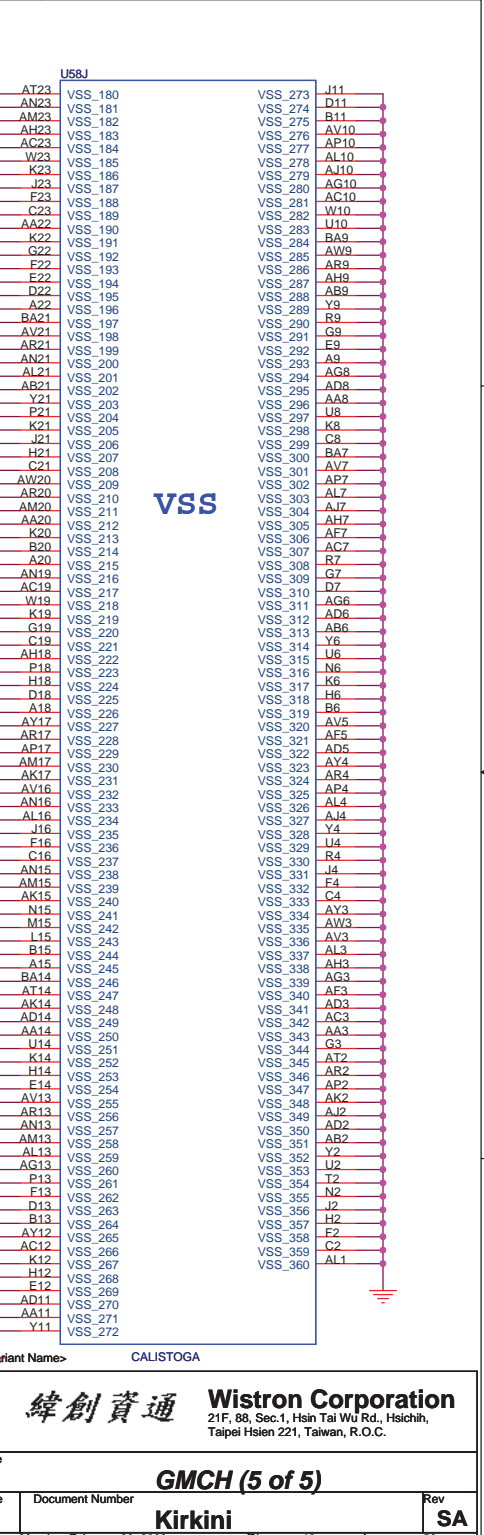
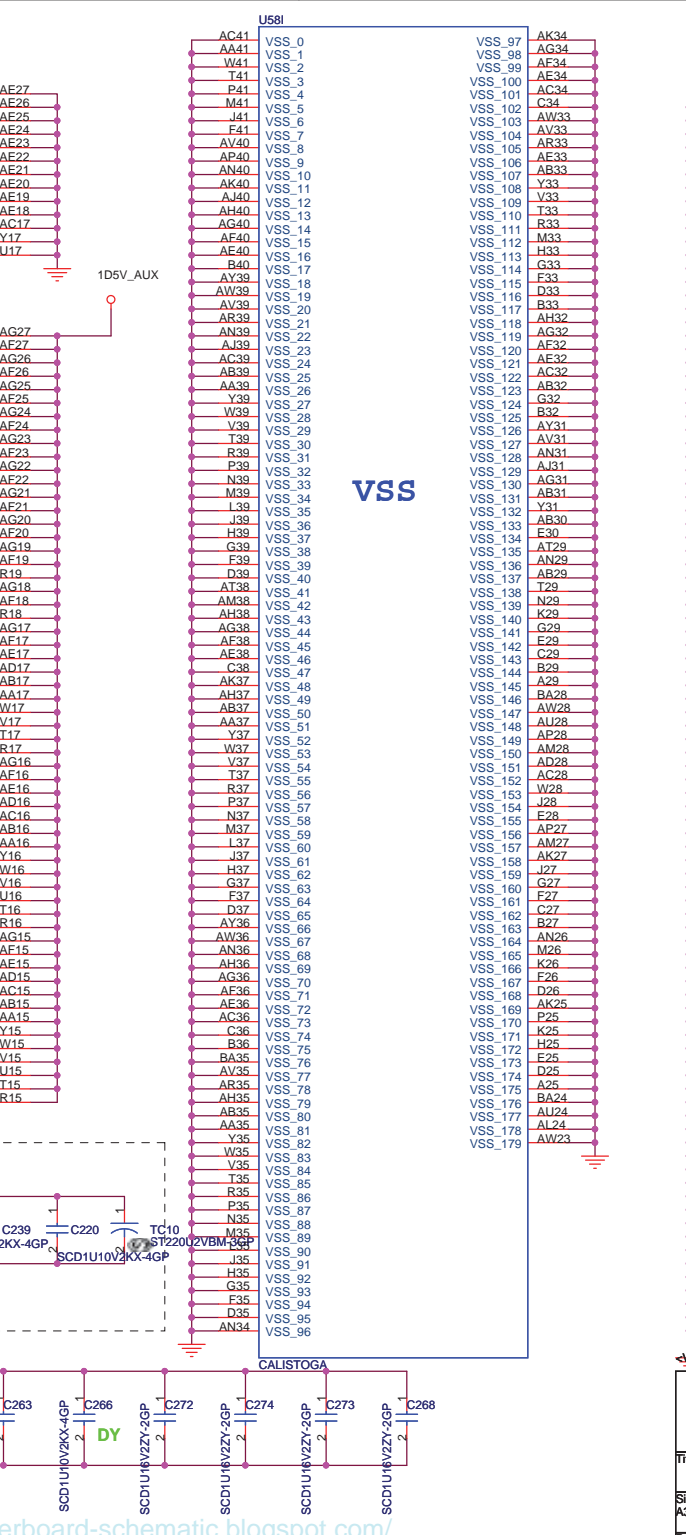
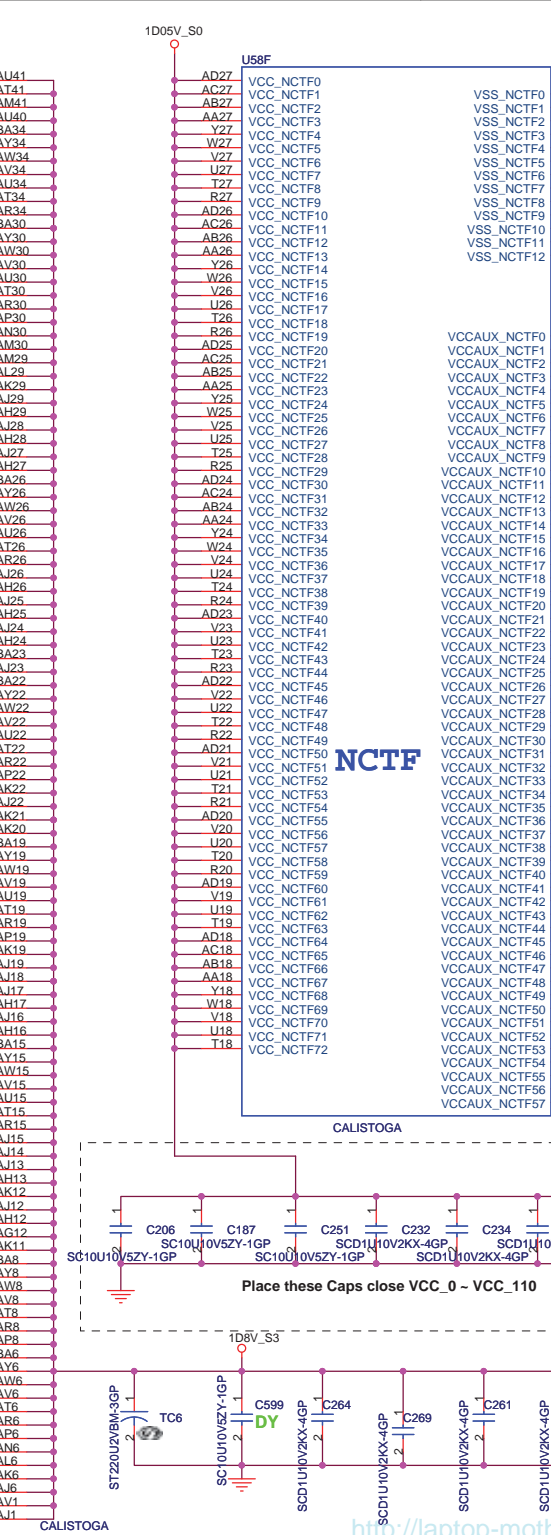
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Title: **GMCH (4 of 5)**

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1D05V_S0	AA33	VCC_0	
	W33	VCC_1	
	F33	VCC_2	
	N33	VCC_3	
	L33	VCC_4	
	J33	VCC_5	
	AA32	VCC_6	VCC_SM_0
	Y32	VCC_7	VCC_SM_1
	W32	VCC_8	VCC_SM_2
	P32	VCC_9	VCC_SM_3
	N32	VCC_10	VCC_SM_4
	M32	VCC_11	VCC_SM_5
	L32	VCC_12	VCC_SM_6
	J32	VCC_13	VCC_SM_7
	AA31	VCC_14	VCC_SM_8
	W31	VCC_15	VCC_SM_9
	V31	VCC_16	VCC_SM_10
	T31	VCC_17	VCC_SM_11
	R31	VCC_18	VCC_SM_12
	P31	VCC_19	VCC_SM_13
	N31	VCC_20	VCC_SM_14
	M31	VCC_21	VCC_SM_15
	W30	VCC_22	VCC_SM_16
	V30	VCC_23	VCC_SM_17
	T30	VCC_24	VCC_SM_18
	R30	VCC_25	VCC_SM_19
	P30	VCC_26	VCC_SM_20
	N30	VCC_27	VCC_SM_21
	M30	VCC_28	VCC_SM_22
	L30	VCC_29	VCC_SM_23
	AA29	VCC_30	VCC_SM_24
	Y29	VCC_31	VCC_SM_25
	W29	VCC_32	VCC_SM_26
	V29	VCC_33	VCC_SM_27
	U29	VCC_34	VCC_SM_28
	R29	VCC_35	VCC_SM_29
	P29	VCC_36	VCC_SM_30
	M29	VCC_37	VCC_SM_31
	L29	VCC_38	VCC_SM_32
	AA28	VCC_39	VCC_SM_33
	Y28	VCC_40	VCC_SM_34
	W28	VCC_41	VCC_SM_35
	V28	VCC_42	VCC_SM_36
	U28	VCC_43	VCC_SM_37
	T28	VCC_44	VCC_SM_38
	R28	VCC_45	VCC_SM_39
	P28	VCC_46	VCC_SM_40
	N28	VCC_47	VCC_SM_41
	M28	VCC_48	VCC_SM_42
	L28	VCC_49	VCC_SM_43
	P27	VCC_50	VCC_SM_44
	N27	VCC_51	VCC_SM_45
	M27	VCC_52	VCC_SM_46
	L27	VCC_53	VCC_SM_47
	P26	VCC_54	VCC_SM_48
	N26	VCC_55	VCC_SM_49
	L26	VCC_56	VCC_SM_50
	N25	VCC_57	VCC_SM_51
	M25	VCC_58	VCC_SM_52
	L25	VCC_59	VCC_SM_53
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	N24	VCC_61	VCC_SM_55
	M24	VCC_62	VCC_SM_56
	AA23	VCC_63	VCC_SM_57
	Y23	VCC_64	VCC_SM_58
	P23	VCC_65	VCC_SM_59
	N23	VCC_66	VCC_SM_60
	M23	VCC_67	VCC_SM_61
	L23	VCC_68	VCC_SM_62
	AC22	VCC_69	VCC_SM_63
	AB22	VCC_70	VCC_SM_64
	Y22	VCC_71	VCC_SM_65
	W22	VCC_72	VCC_SM_66
	P22	VCC_73	VCC_SM_67
	N22	VCC_74	VCC_SM_68
	M22	VCC_75	VCC_SM_69
	L22	VCC_76	VCC_SM_70
	AC21	VCC_77	VCC_SM_71
	AA21	VCC_78	VCC_SM_72
	W21	VCC_79	VCC_SM_73
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	L21	VCC_82	VCC_SM_76
	AC20	VCC_83	VCC_SM_77
	AB20	VCC_84	VCC_SM_78
	Y20	VCC_85	VCC_SM_79
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	V20	VCC_87	VCC_SM_81
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	T20	VCC_89	VCC_SM_83
	R20	VCC_90	VCC_SM_84
	P20	VCC_91	VCC_SM_85
	N20	VCC_92	VCC_SM_86
	M20	VCC_93	VCC_SM_87
	L20	VCC_94	VCC_SM_88
	AB19	VCC_95	VCC_SM_89
	AA19	VCC_96	VCC_SM_90
	Y19	VCC_97	VCC_SM_91
	N19	VCC_98	VCC_SM_92
	M19	VCC_99	VCC_SM_93
	L19	VCC_100	VCC_SM_94
	N18	VCC_101	VCC_SM_95
	M18	VCC_102	VCC_SM_96
	L18	VCC_103	VCC_SM_97
	P17	VCC_104	VCC_SM_98
	N17	VCC_105	VCC_SM_99
	M17	VCC_106	VCC_SM_100
	L16	VCC_107	VCC_SM_101
		VCC_108	VCC_SM_102
		VCC_109	VCC_SM_103
		VCC_110	VCC_SM_104
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			VCC_SM_109
			VCC_SM_110



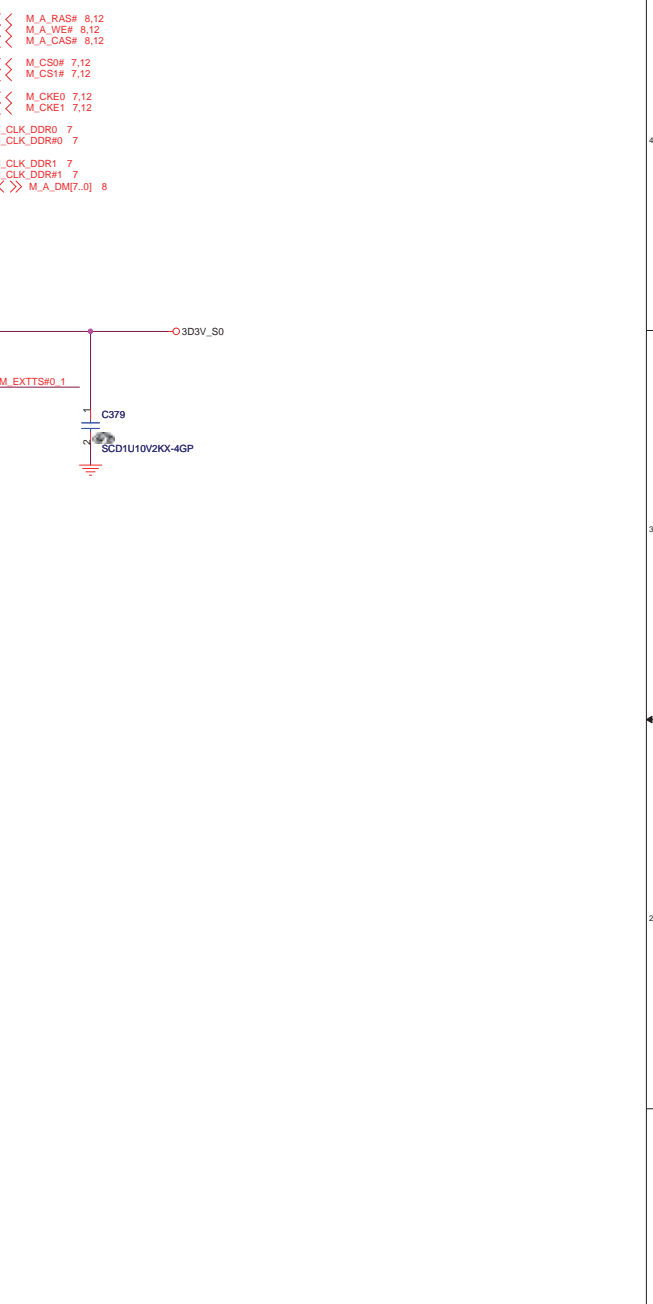
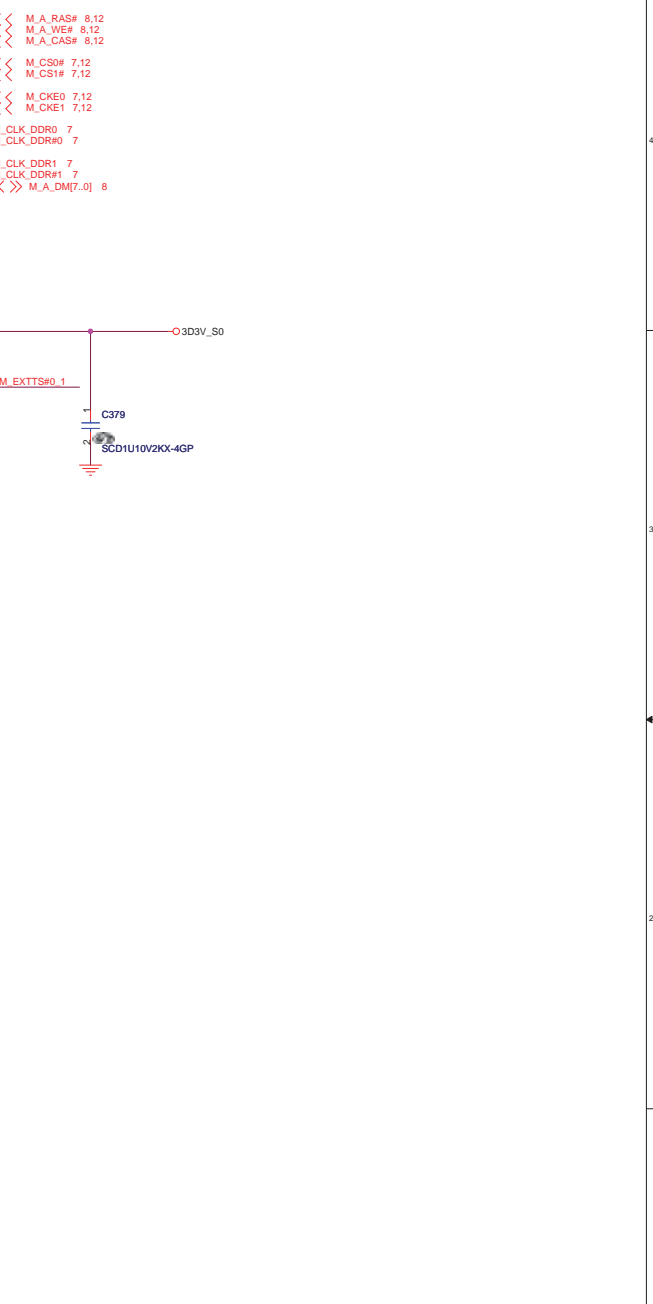
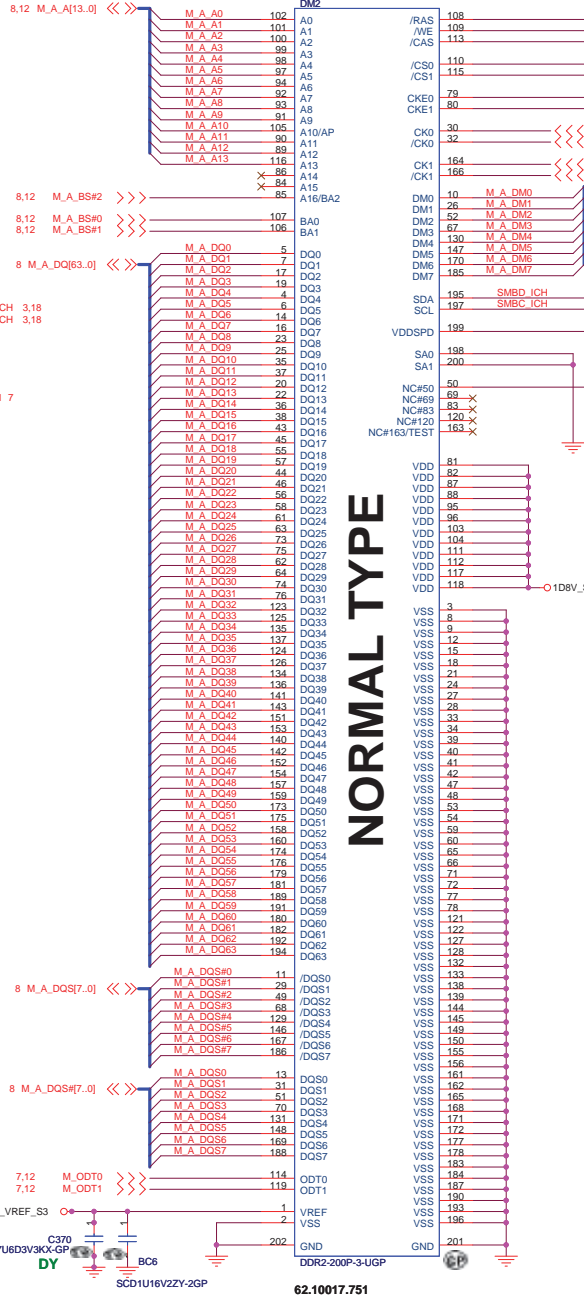
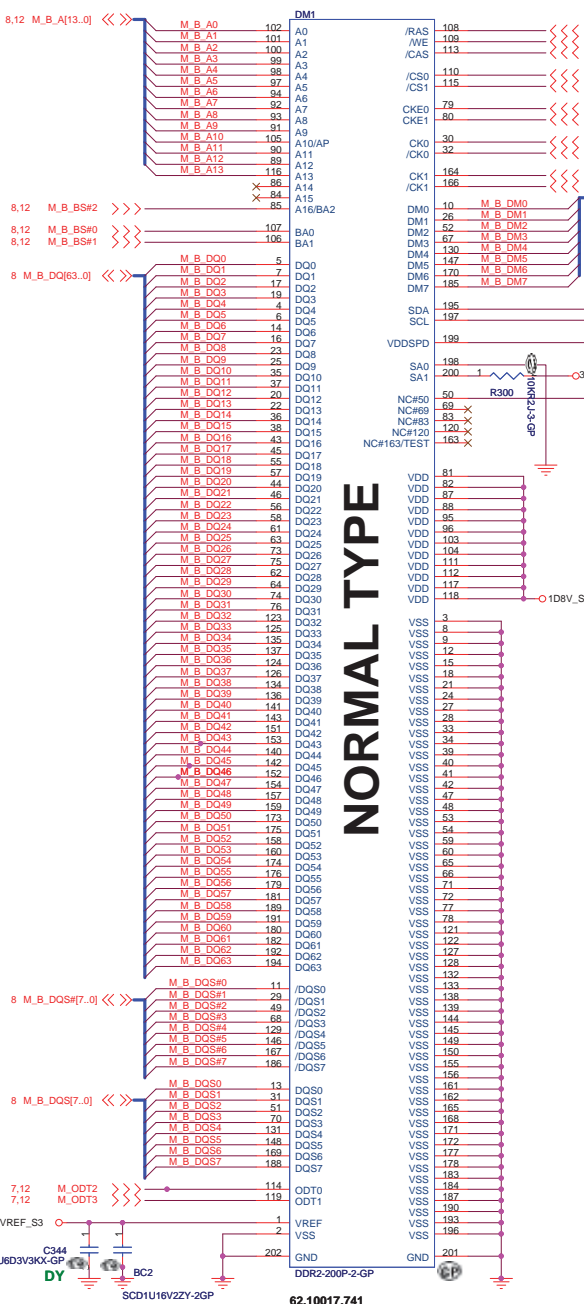
Variant Name: CALISTOGA

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Title: **GMCH (5 of 5)**

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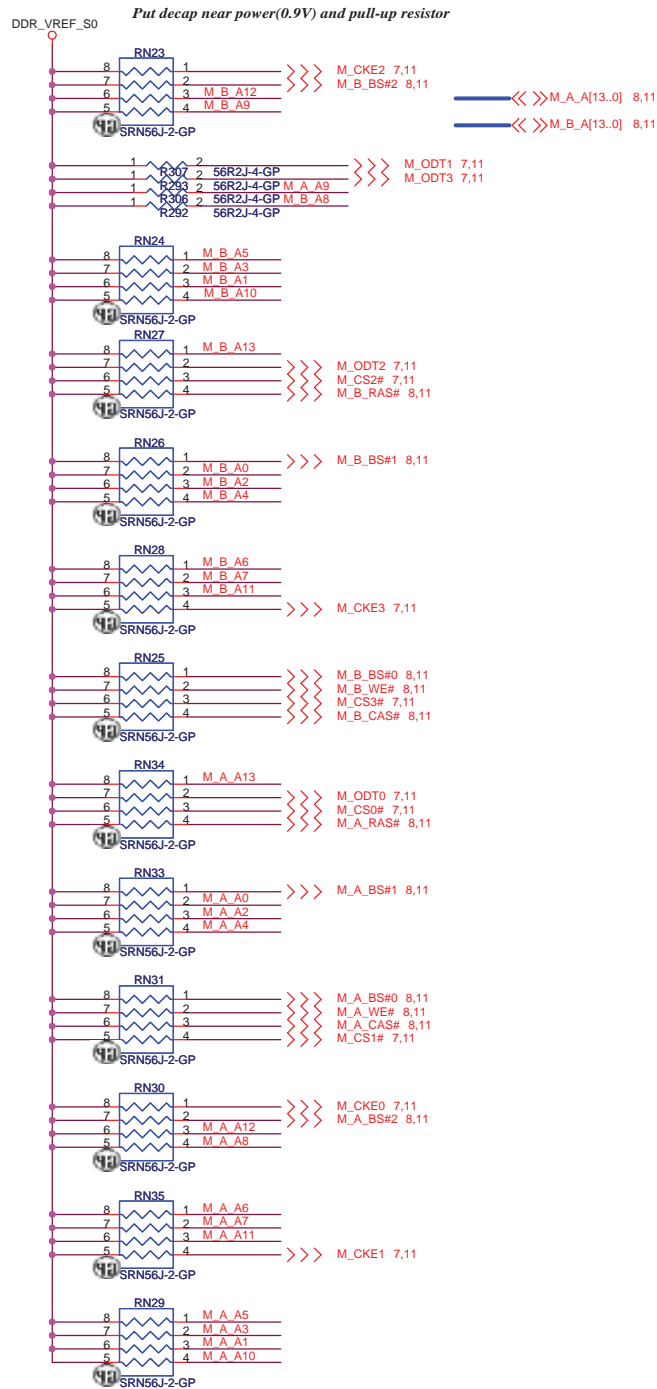
DDR Socket

Kirkini

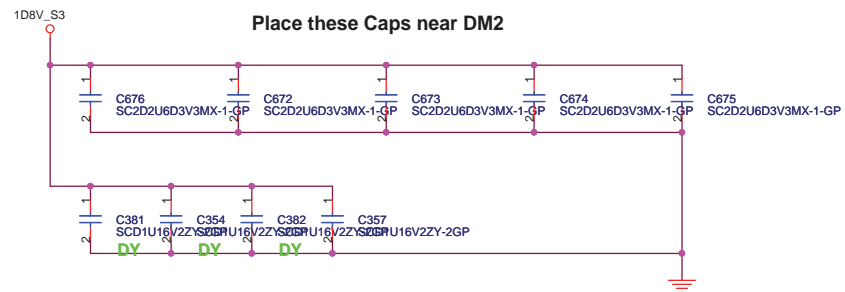
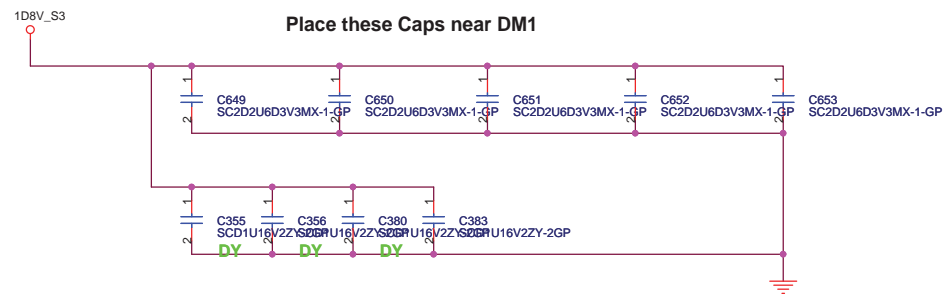
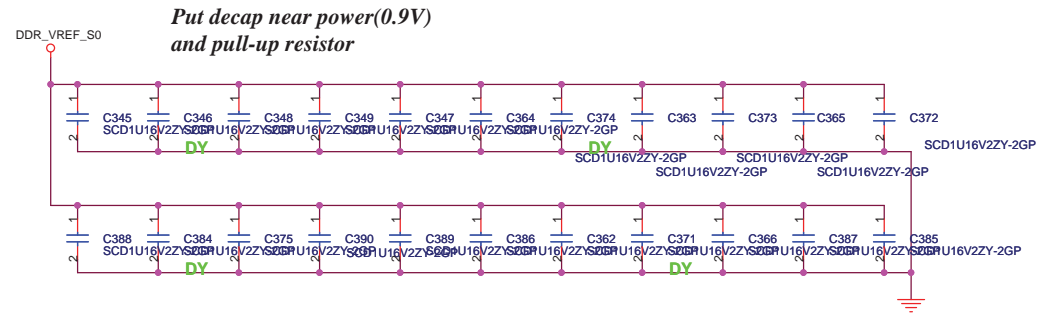
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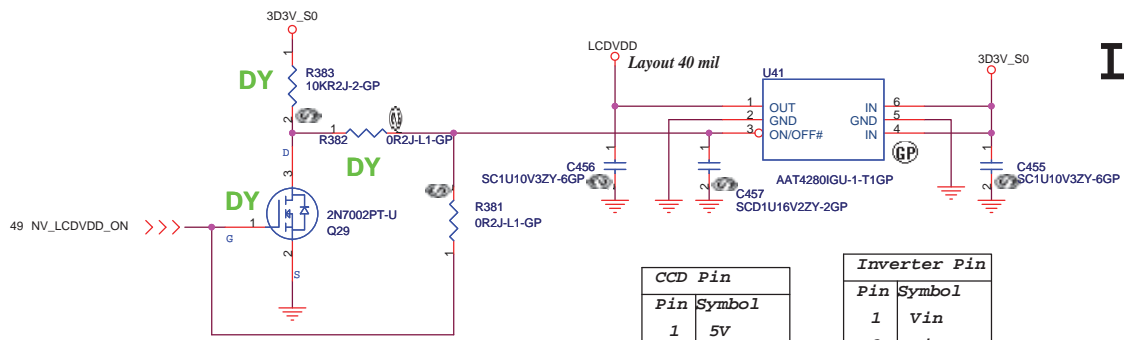
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PARALLEL TERMINATION



Decoupling Capacitor

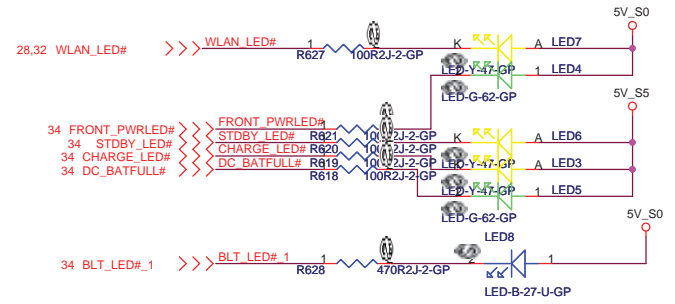
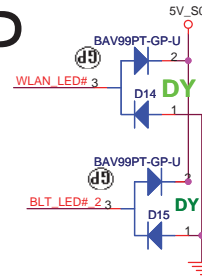




CCD Pin		Inverter Pin	
Pin	Symbol	Pin	Symbol
1	5V	1	Vin
2	USB-	2	Vin
3	USB+	3	PWM
4	GND	4	BLON
5	GND	5	GND
6	GND	6	GND

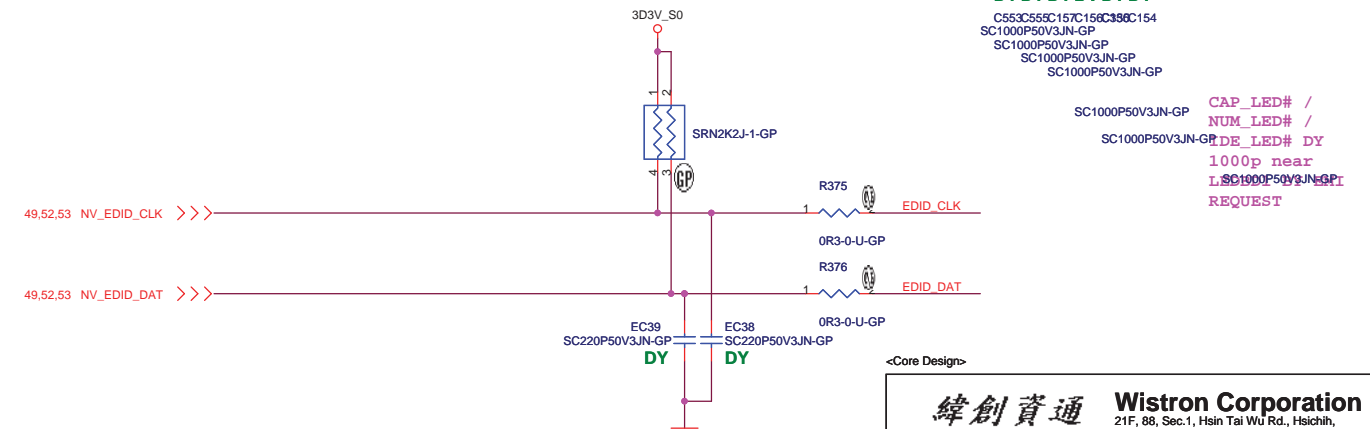
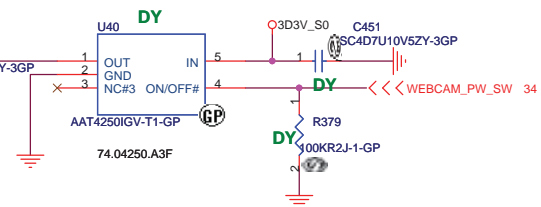
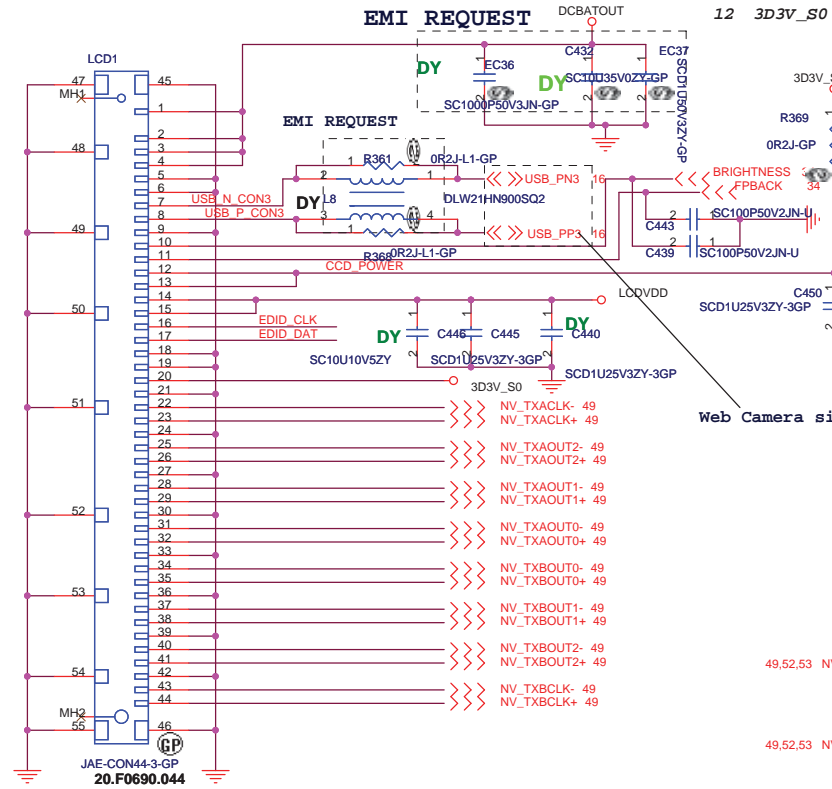
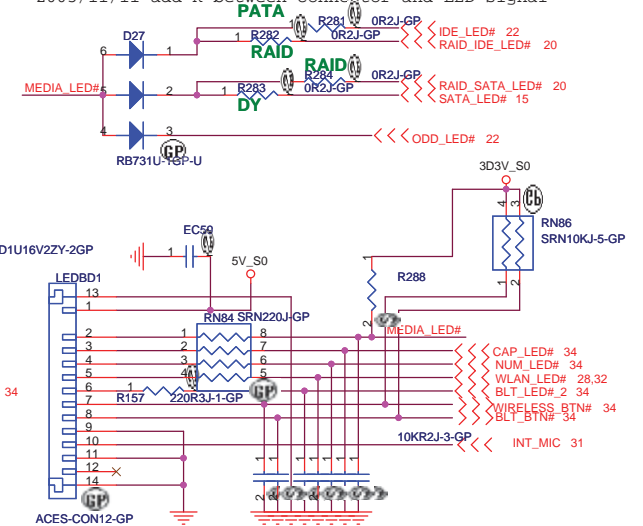
LCD/INVERTER CONN

LED



LED BD CONN

2005/11/11 add R between connector and LED signal



<Core Design>

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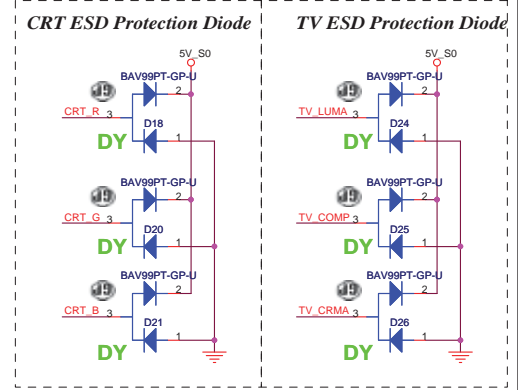
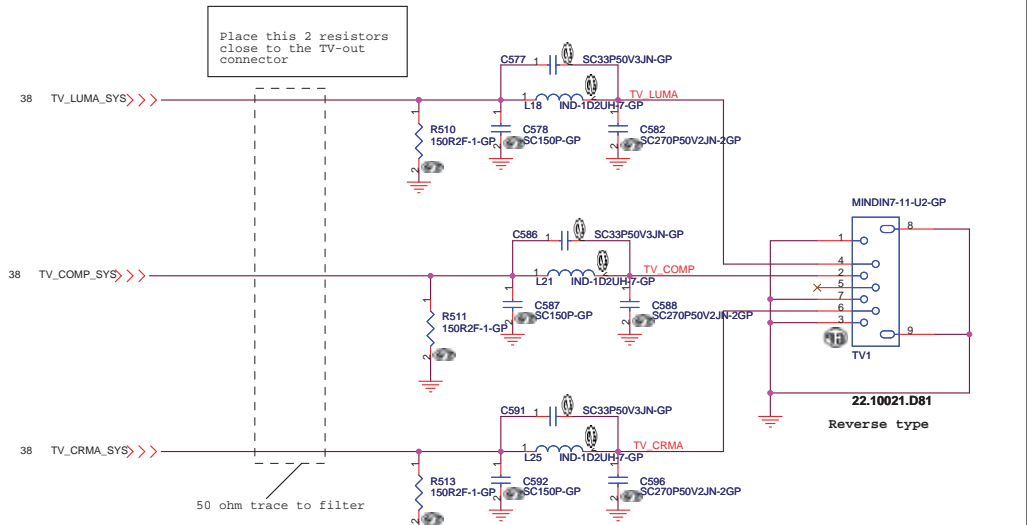
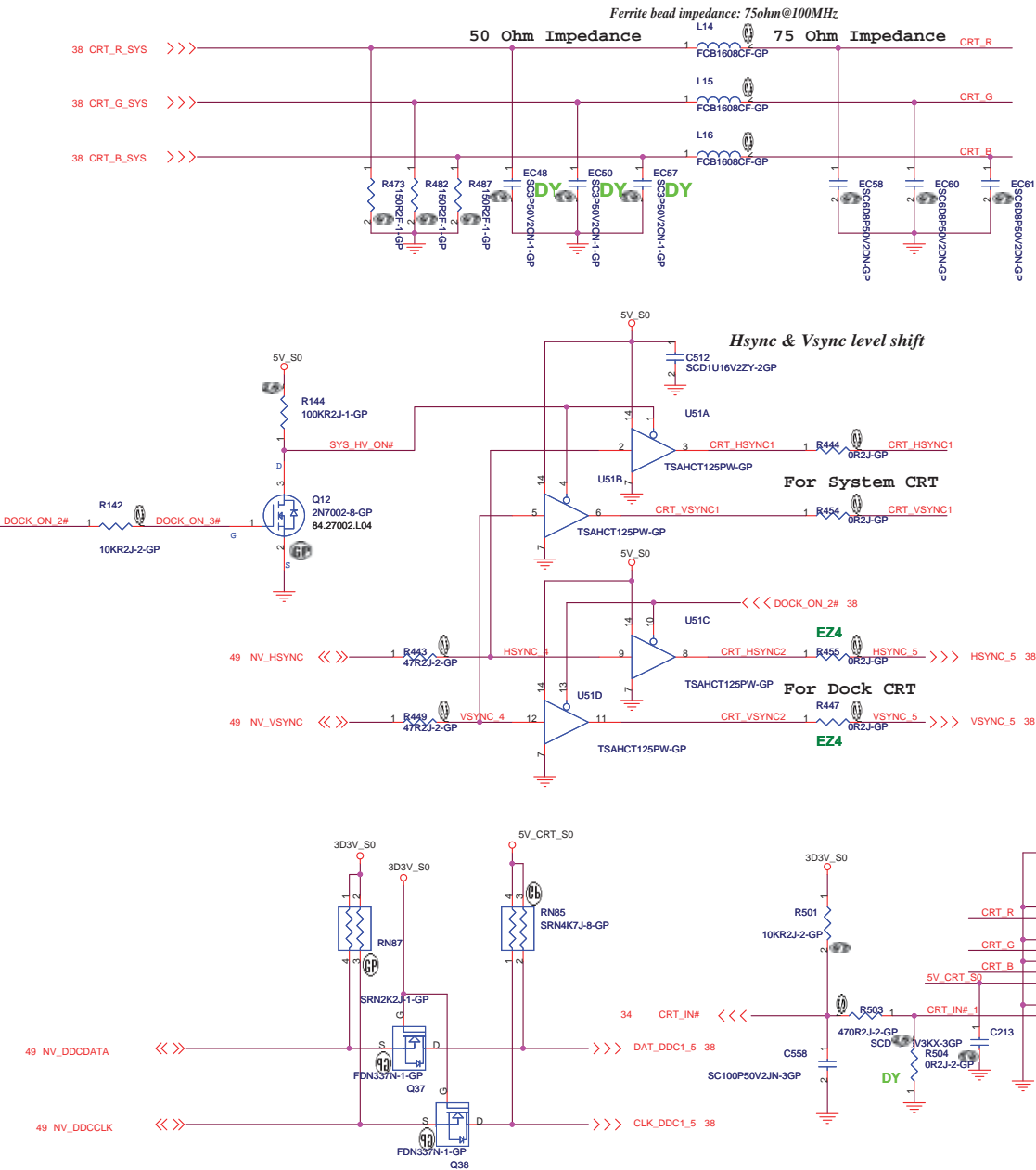
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LCD CONN & LED

Size A3 Document Number
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CRT CONNECTOR

TV CONNECTOR

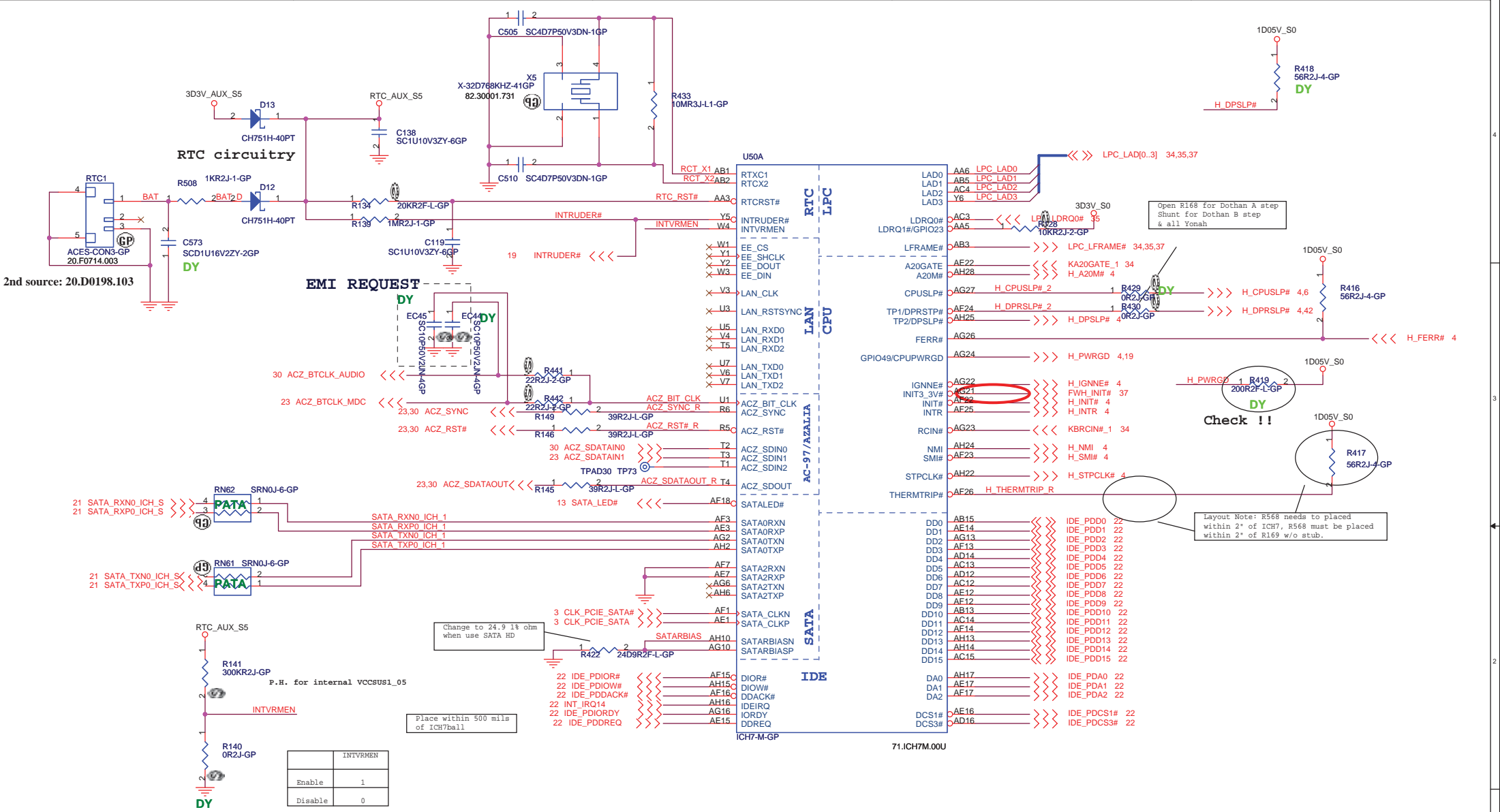


<Core Design>

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Title: **CRT/TV Connector**

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2nd source: 20.D0198.103

Open R168 for Dothan A step
Shunt for Dothan B step
& all Yonah

Check !!

Layout Note: R568 needs to be placed
within 2" of ICH7, R568 must be placed
within 2" of R169 w/o stub.

Placement Note:
Distance between the ICH-7 M and cap on the "P" signal
should be identical distance between the ICH-7 M and cap
on the "N" signal for same pair.

	INTVRMEN
Enable	1
Disable	0

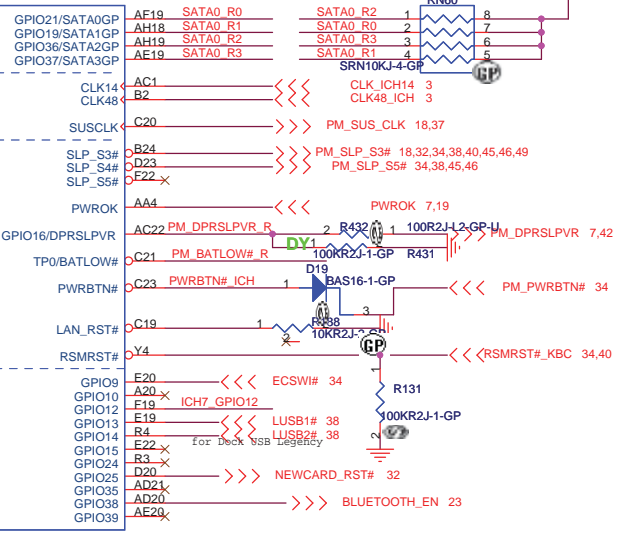
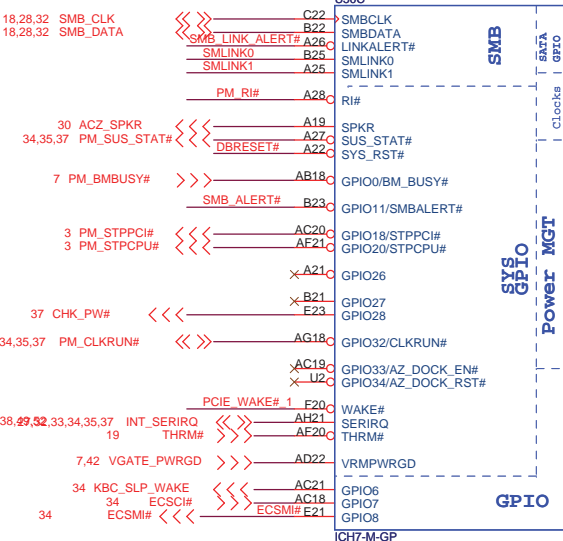
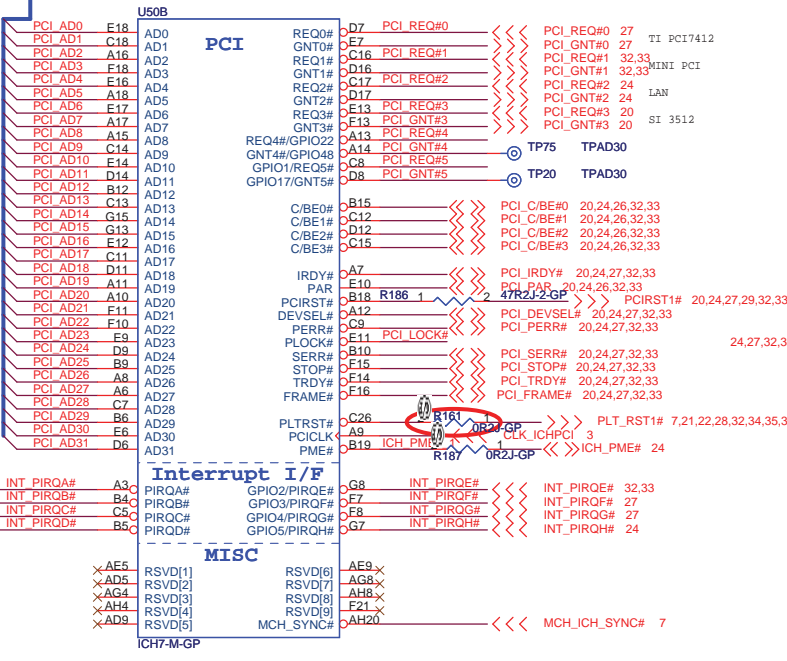
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Taipei Hsien 221, Taiwan, R.O.C.

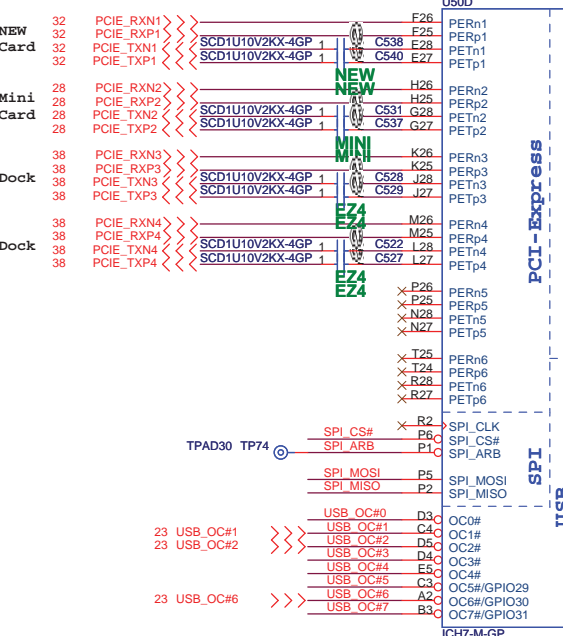
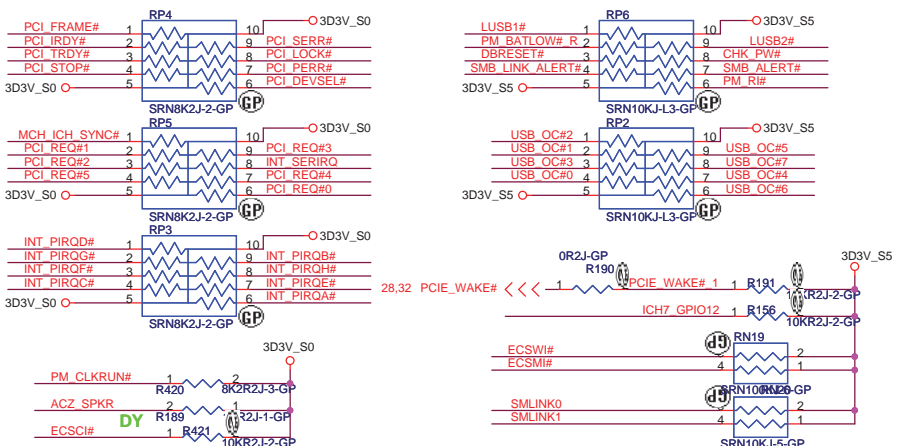
Title: **ICH7-M (1 of 4)**

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ICH7 Pullups



USB	
Pair	Device
0	NEW CARD
1	USB2.0
2	USB2.0
3	CCD
4	USB2.0
5	MINI CARD
6	USB2.0
7	BLUETOOTH

Default:H

GNT#5#	GNT#4#
LPC	H
PCI	H
SPI	L
	H

Boot from various source

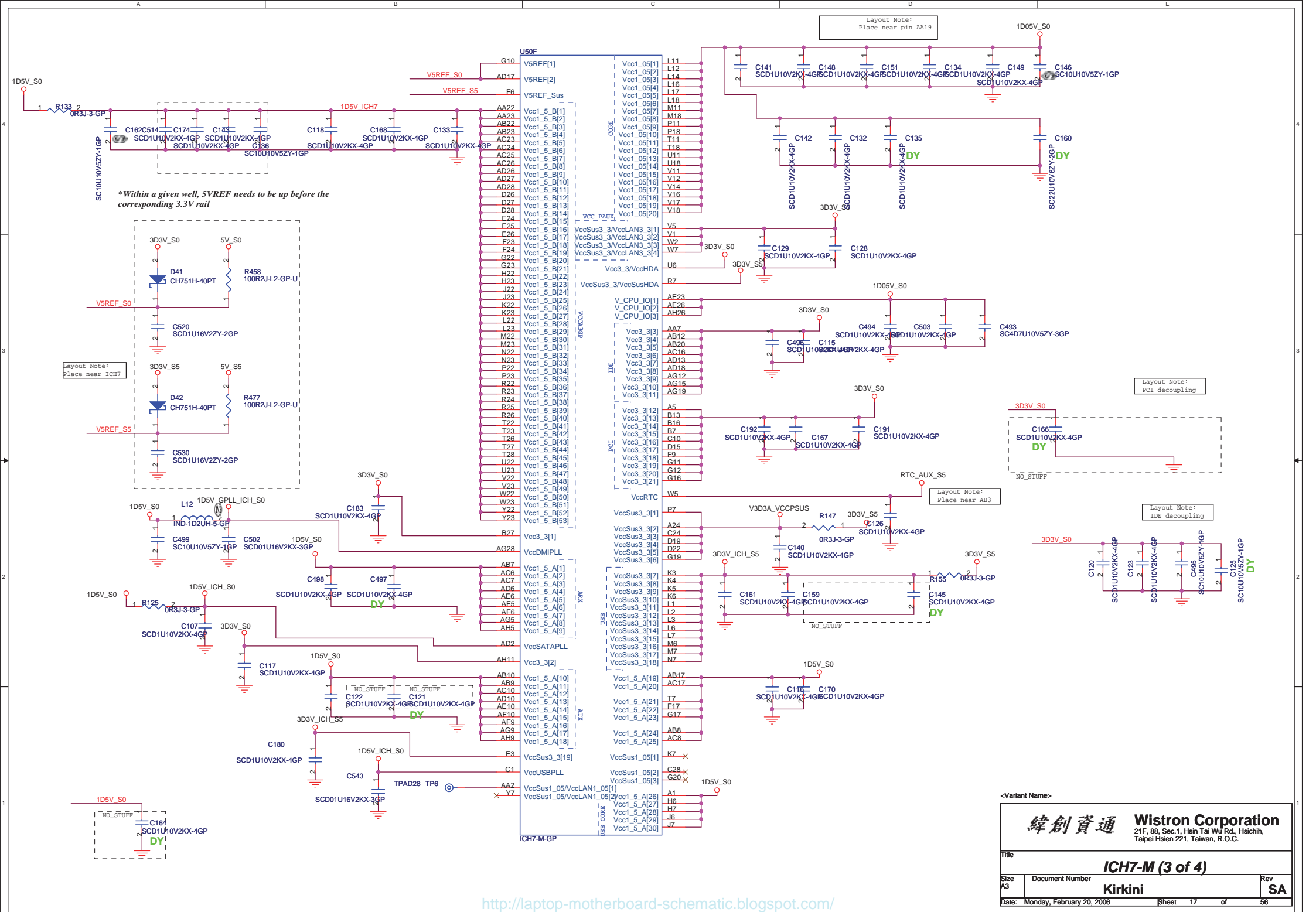
Layout Note:
PCIe AC coupling caps need to be within 250 mils of the driver.

Layout Note:
Place within 500 mils of ICH

<Variant Name>

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*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note: Place near pin AA19

Layout Note: Place near ICH7

Layout Note: PCI decoupling

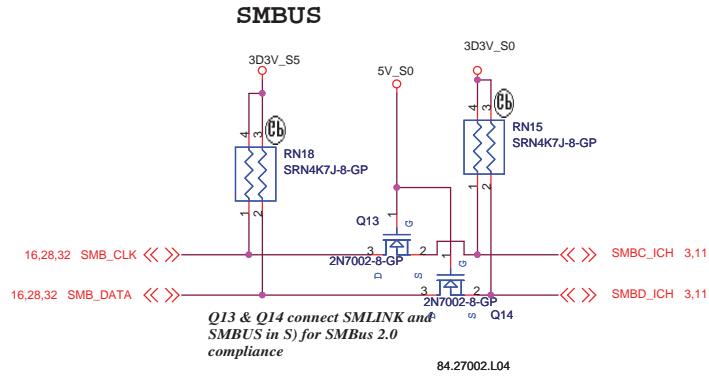
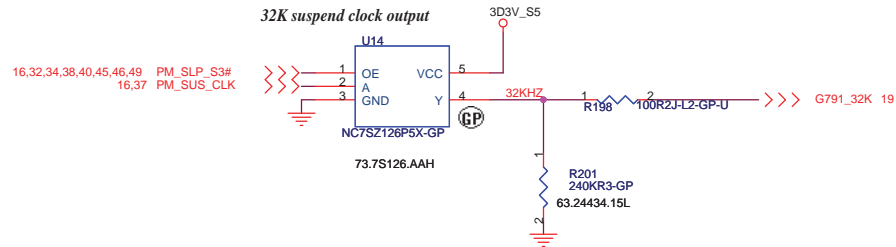
Layout Note: Place near AB3

Layout Note: IDE decoupling

<Variant Name>

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Title			ICH7-M (3 of 4)		
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A3		Kirkini			SA
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U50E		
A4	VSS[1]	P28
A23	VSS[2]	R1
B1	VSS[3]	R11
B8	VSS[4]	R12
B11	VSS[5]	R13
B14	VSS[6]	R14
B17	VSS[7]	R15
B20	VSS[8]	R16
B28	VSS[9]	R17
B28	VSS[10]	R18
C2	VSS[11]	T6
C6	VSS[12]	T12
C27	VSS[13]	T13
D10	VSS[14]	T14
D13	VSS[15]	T15
D18	VSS[16]	T16
D21	VSS[17]	T17
D24	VSS[18]	U4
E1	VSS[19]	U12
E2	VSS[20]	U13
E4	VSS[21]	U14
E8	VSS[22]	U15
E15	VSS[23]	U16
F3	VSS[24]	U17
F4	VSS[25]	U24
F5	VSS[26]	U25
F12	VSS[27]	U26
F27	VSS[28]	V2
F28	VSS[29]	V13
G1	VSS[30]	V15
G2	VSS[31]	V24
G5	VSS[32]	V27
G6	VSS[33]	V28
G9	VSS[34]	W6
G14	VSS[35]	W24
G18	VSS[36]	W25
G21	VSS[37]	W26
G24	VSS[38]	Y3
G25	VSS[39]	Y24
G26	VSS[40]	Y27
H3	VSS[41]	AA1
H4	VSS[42]	AA24
H5	VSS[43]	AA25
H24	VSS[44]	AA26
H27	VSS[45]	AB4
H28	VSS[46]	AB6
J1	VSS[47]	AB11
J2	VSS[48]	AB14
J4	VSS[49]	AB16
J25	VSS[50]	AB19
J26	VSS[51]	AB21
K24	VSS[52]	AB24
K27	VSS[53]	AB27
K28	VSS[54]	AB28
L13	VSS[55]	AC2
L15	VSS[56]	AC5
L24	VSS[57]	AC9
L25	VSS[58]	AC11
L26	VSS[59]	AD1
M3	VSS[60]	AD3
M4	VSS[61]	AD4
M5	VSS[62]	AD7
M12	VSS[63]	AD8
M13	VSS[64]	AD11
M14	VSS[65]	AD15
M15	VSS[66]	AD19
M16	VSS[67]	AD23
M17	VSS[68]	AE2
M24	VSS[69]	AE4
M27	VSS[70]	AE8
M28	VSS[71]	AE11
N1	VSS[72]	AE18
N2	VSS[73]	AE21
N5	VSS[74]	AE24
N6	VSS[75]	AE25
N11	VSS[76]	AF2
N12	VSS[77]	AF4
N13	VSS[78]	AF8
N14	VSS[79]	AF11
N15	VSS[80]	AG1
N16	VSS[81]	AG3
N17	VSS[82]	AG7
N18	VSS[83]	AG11
N24	VSS[84]	AG17
N25	VSS[85]	AG20
N28	VSS[86]	AG25
P3	VSS[87]	AH1
P4	VSS[88]	AH3
P12	VSS[89]	AH7
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P14	VSS[91]	AH23
P15	VSS[92]	AH27
P16	VSS[93]	AH28
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P28	VSS[97]	AH42
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P28	VSS[99]	AH52
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P28	VSS[174]	AH427
P28	VSS[175]	AH432
P28	VSS[176]	AH437
P28	VSS[177]	AH442
P28	VSS[178]	AH447
P28	VSS[179]	AH452
P28	VSS[180]	AH457
P28	VSS[181]	AH462
P28	VSS[182]	AH467
P28	VSS[183]	AH472
P28	VSS[184]	AH477
P28	VSS[185]	AH482
P28	VSS[186]	AH487
P28	VSS[187]	AH492
P28	VSS[188]	AH497
P28	VSS[189]	AH502
P28	VSS[190]	AH507
P28	VSS[191]	AH512
P28	VSS[192]	AH517
P28	VSS[193]	AH522
P28	VSS[194]	AH527

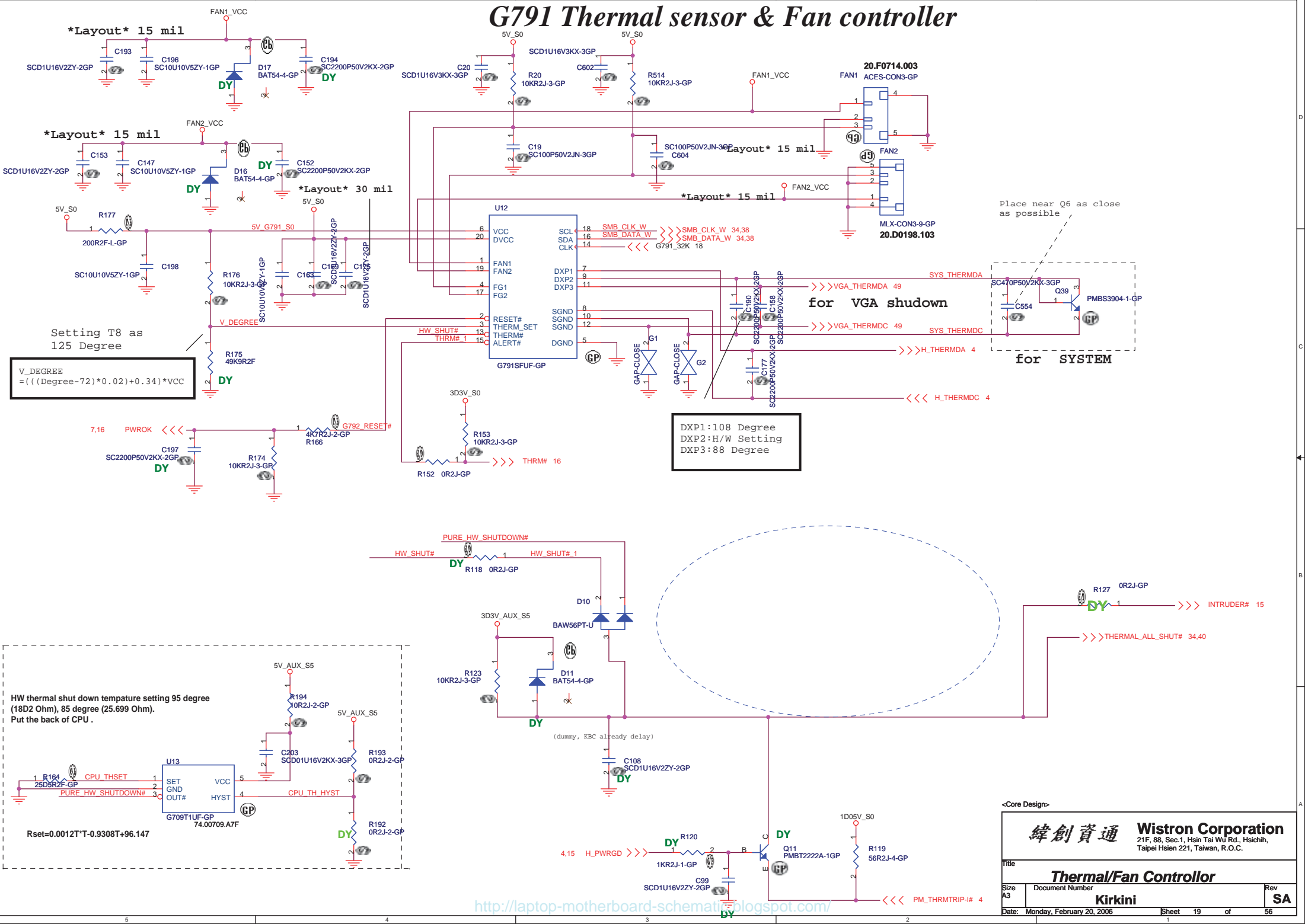
<Variant Name> ICH7-M-GP

緯創資通 Wistron Corporation
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Title: **ICH7-M (4 of 4)**

Size A3	Document Number	Rev SA
Date: Monday, February 20, 2006		Sheet 18 of 56

G791 Thermal sensor & Fan controller



Setting T8 as 125 Degree

$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

HW thermal shut down temperature setting 95 degree (18D2 Ohm), 85 degree (25.699 Ohm). Put the back of CPU.

Rset=0.0012T-0.9308T+96.147

Place near Q6 as close as possible

for VGA shudown

for SYSTEM

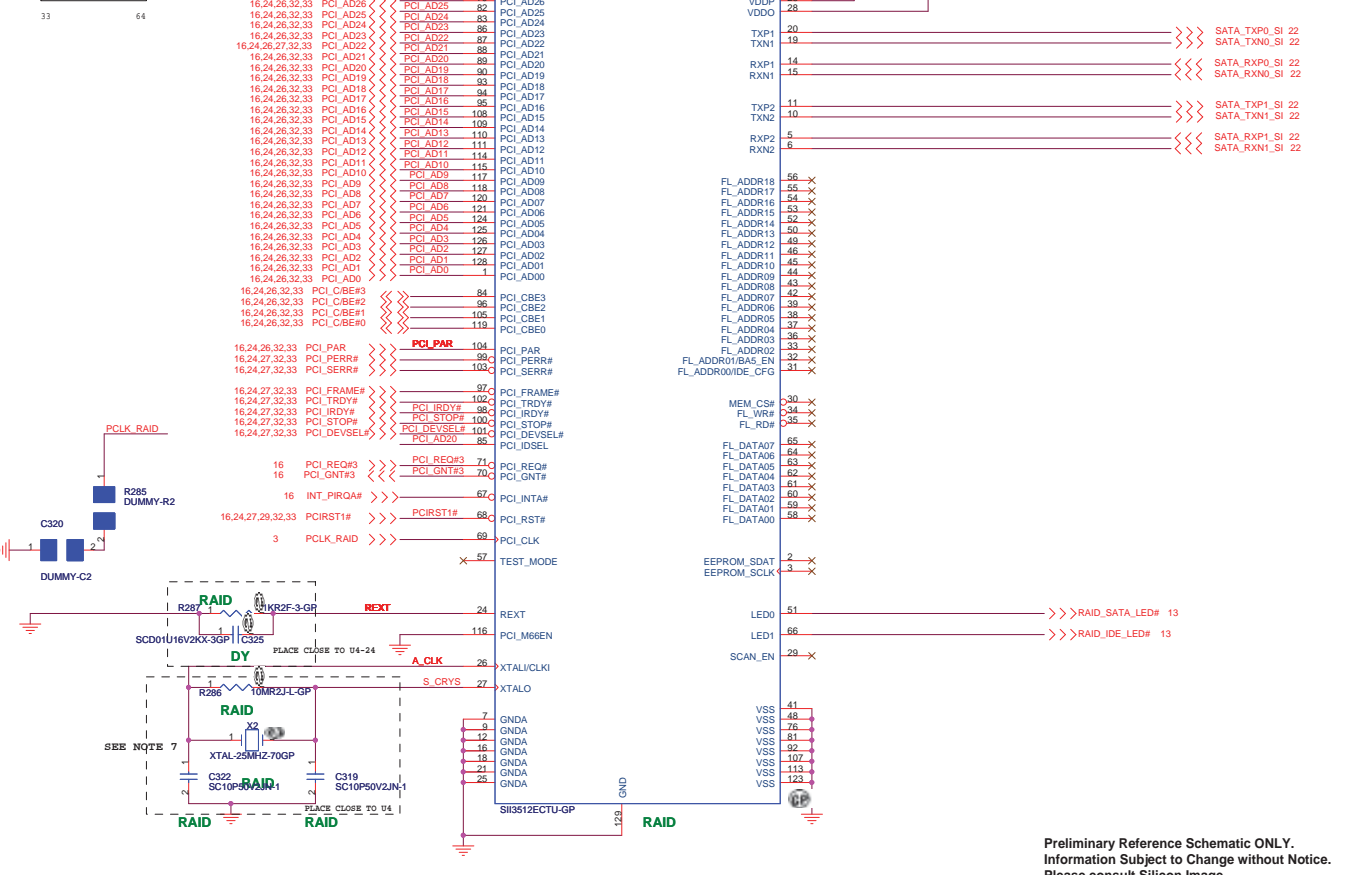
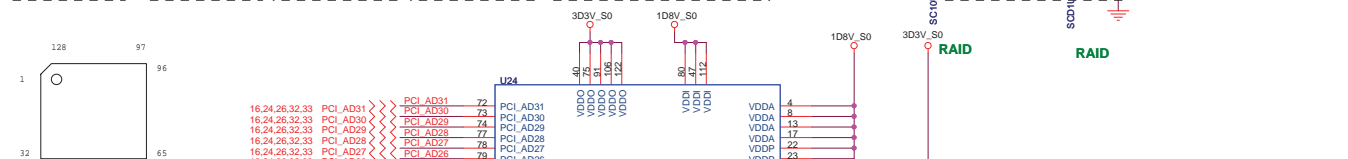
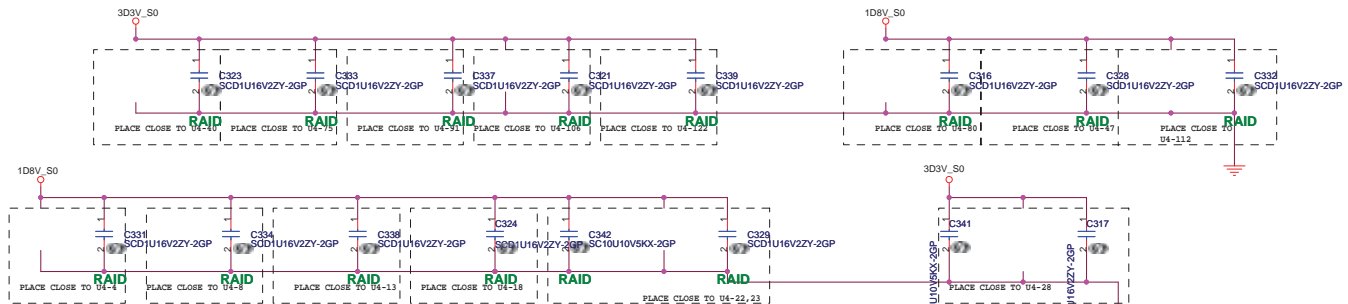
<Core Design>

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Title: **Thermal/Fan Controller**

Size A3	Document Number	Rev
	Kirkini	SA

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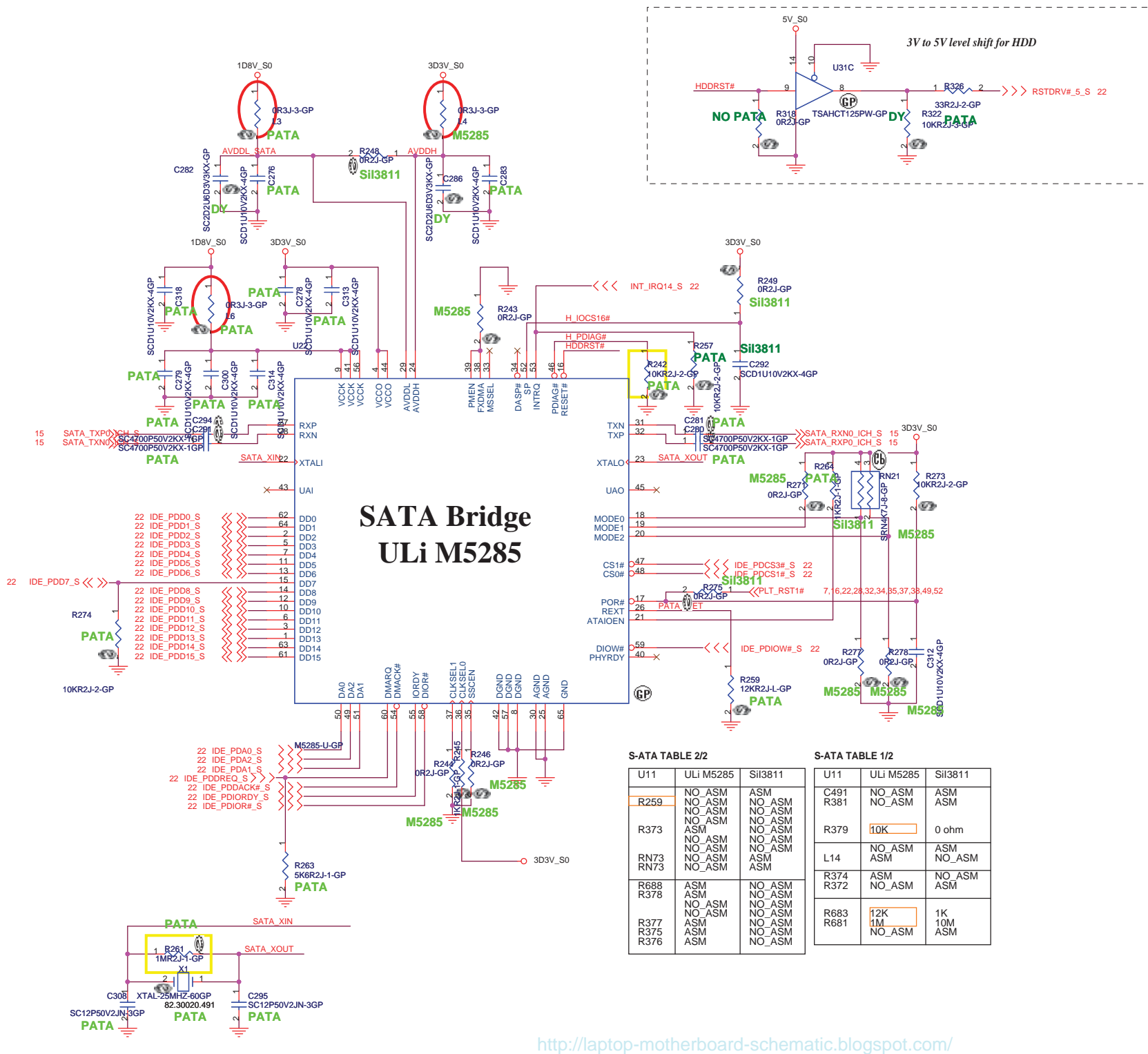
<Core Design>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **RAID SII3512**

Size	Document Number	Rev
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Date:	Monday, February 20, 2006	Sheet 20 of 56

Preliminary Reference Schematic ONLY.
 Information Subject to Change without Notice.
 Please consult Silicon Image.



SATA Bridge ULi M5285

S-ATA TABLE 2/2

U11	ULi M5285	Sii3811
R259	NO_ASM	ASM
R373	NO_ASM	NO_ASM
RN73	NO_ASM	NO_ASM
R688	ASM	NO_ASM
R378	NO_ASM	NO_ASM
R377	ASM	NO_ASM
R375	ASM	NO_ASM
R376	ASM	NO_ASM

S-ATA TABLE 1/2

U11	ULi M5285	Sii3811
C491	NO_ASM	ASM
R381	NO_ASM	ASM
R379	10K	0 ohm
L14	NO_ASM	ASM
R374	ASM	NO_ASM
R372	NO_ASM	ASM
R683	12K	1K
R681	1M	10M
	NO_ASM	ASM

<Variant Name>

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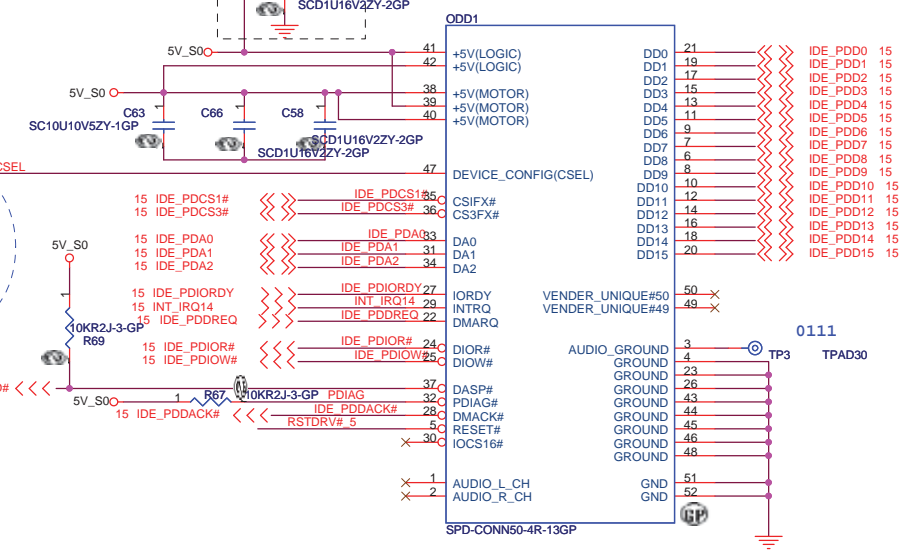
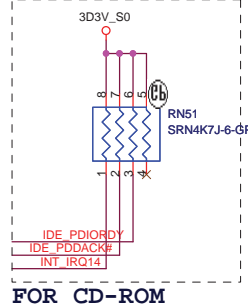
Title: **SATA Bridge**

Size A3 Document Number: **Kirkini** Rev: **SA**

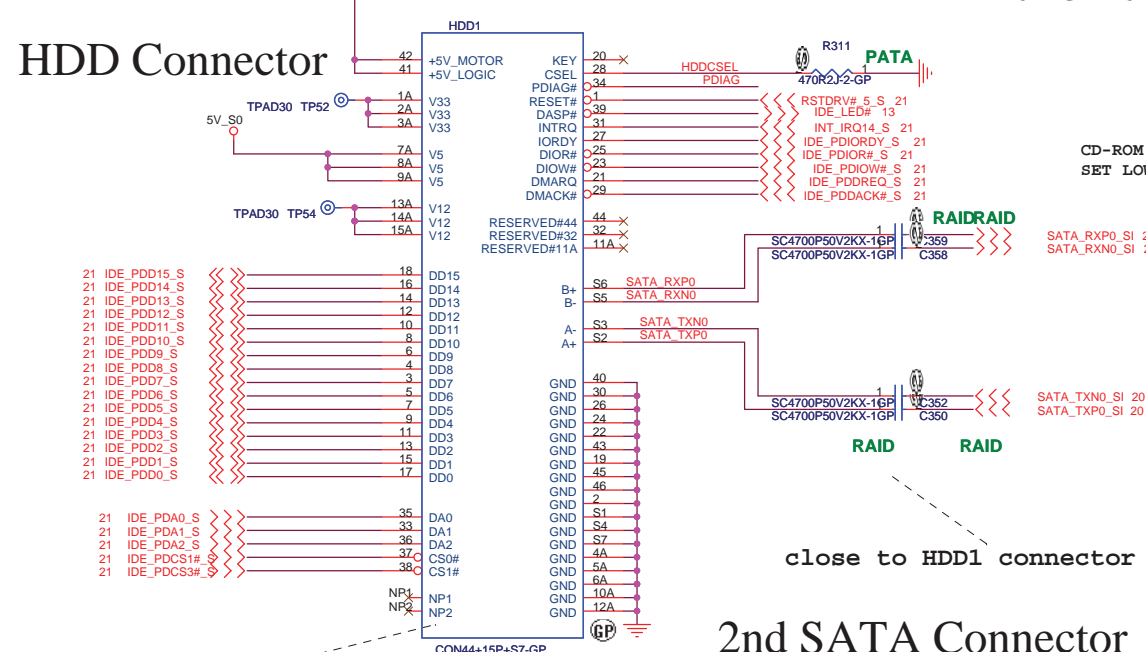
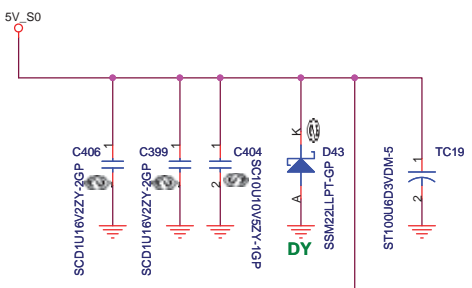
Date: Monday, February 20, 2006 Sheet 21 of 56

CD-ROM Connector

EMI REQUEST

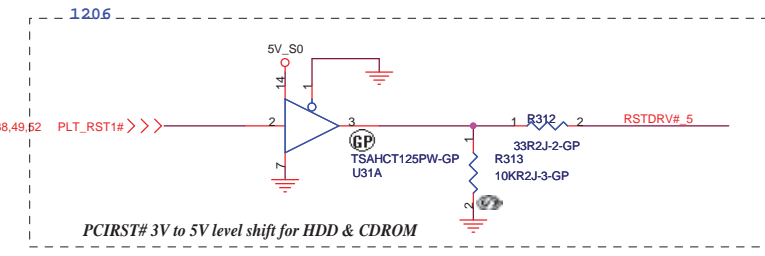
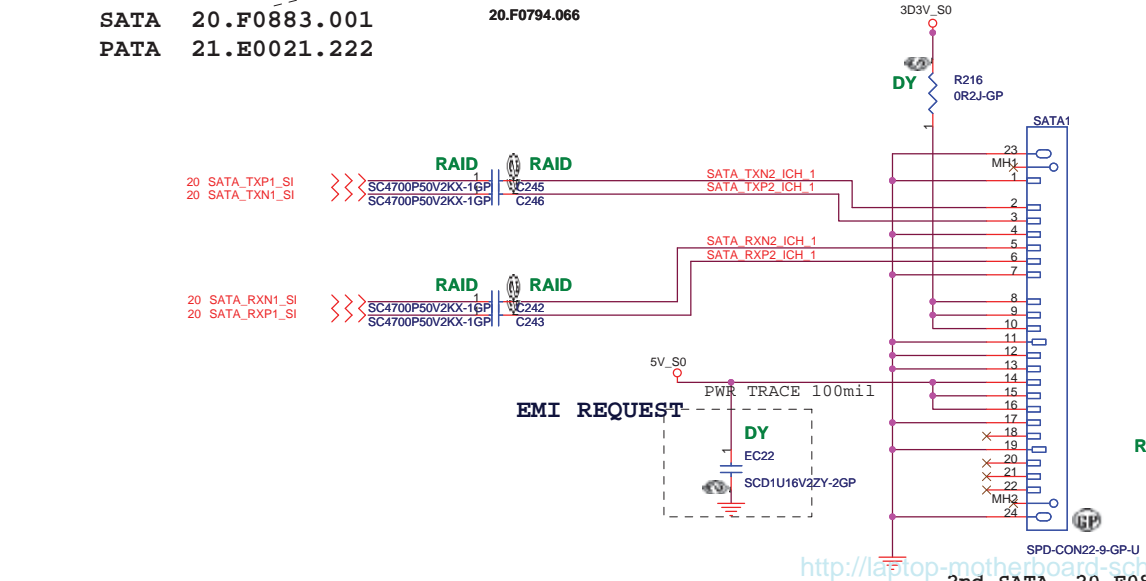


HDD Connector

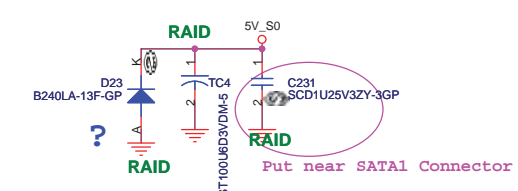


SATA 20.F0883.001
 PATA 21.E0021.222

2nd SATA Connector



For HDD & SATA both



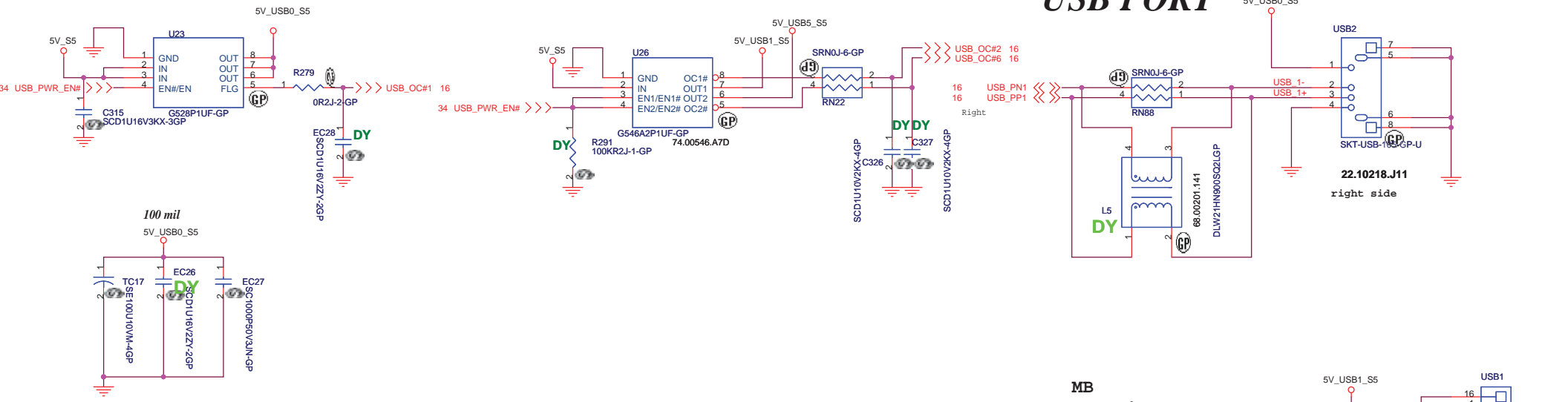
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD and CDROM**

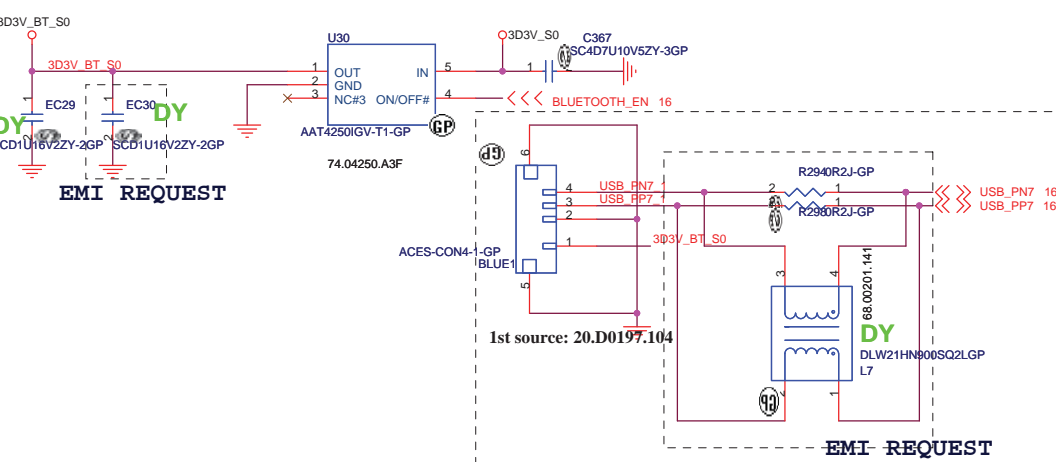
Size A3 Document Number **Kirkini** Rev **SA**

Date: Monday, February 20, 2006 Sheet 22 of 56

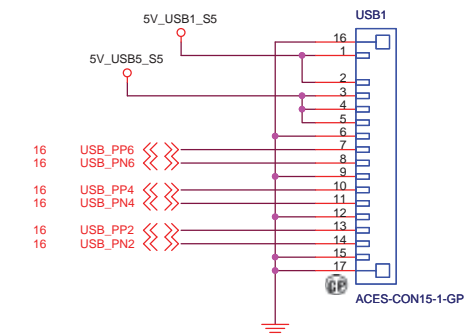
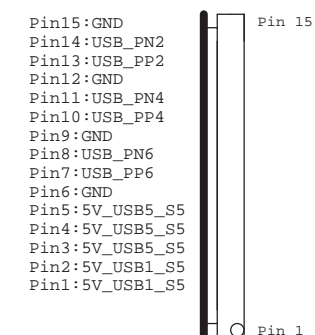
USB PORT



BLUETOOTH MODULE

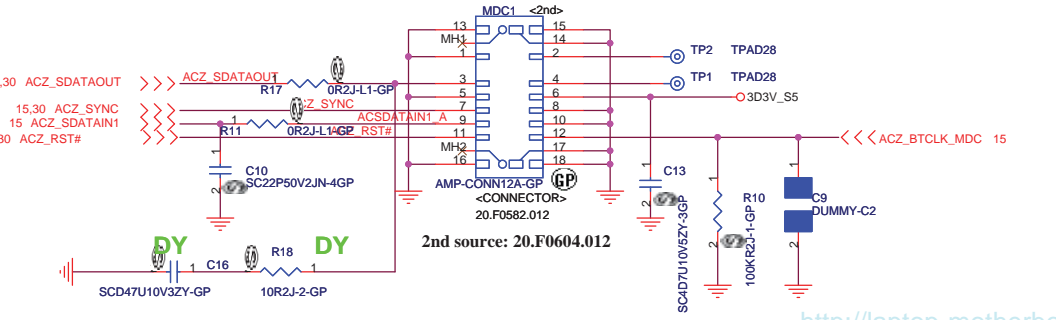


MB Top view



MDC 1.5 CONNECTOR

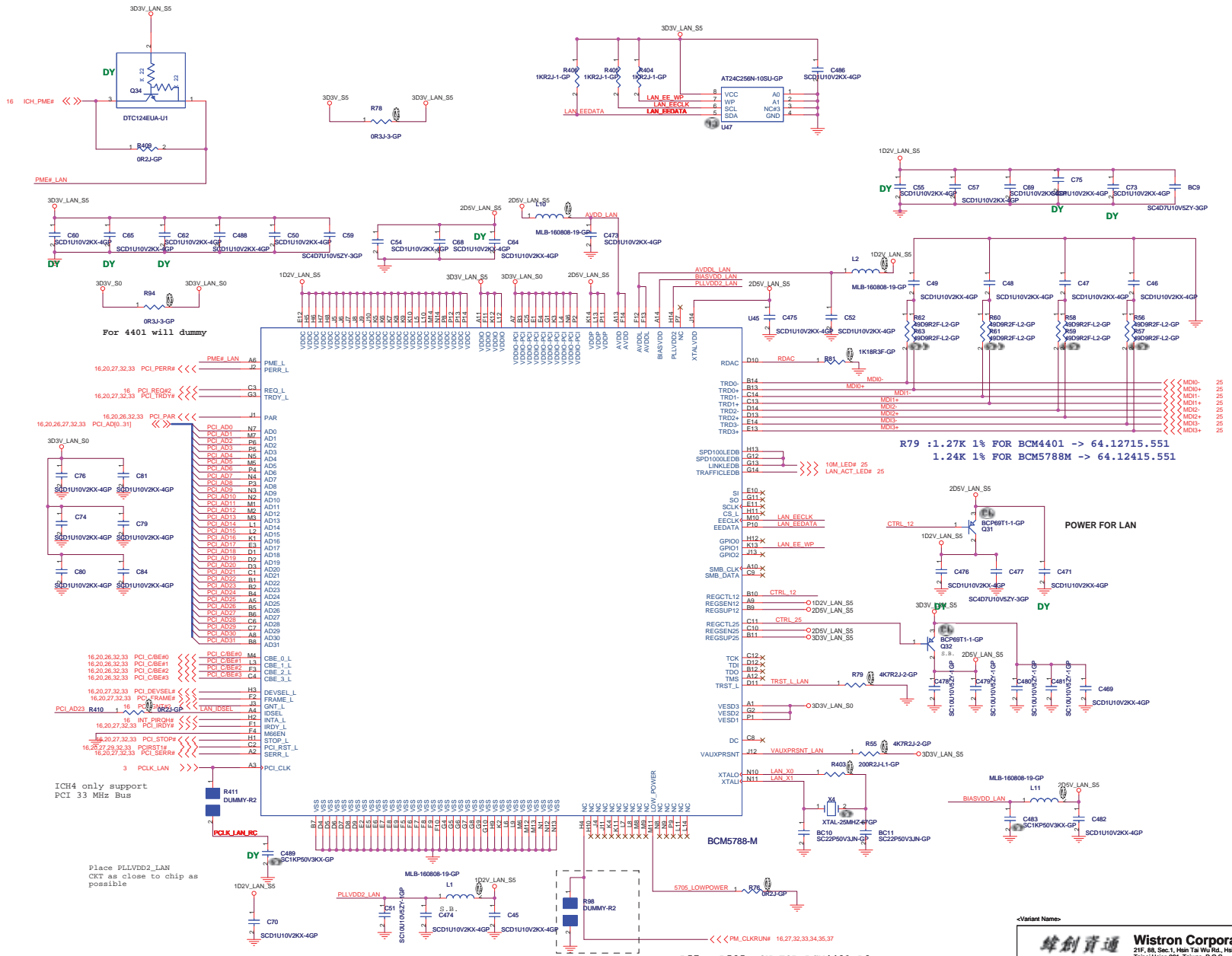
CHANGE TO AZ



<Core Design>

緯創資通 Wistron Corporation
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Title USB / MDC / BLUETOOTH		
Size A3	Document Number Kirkini	Rev SA
Date: Monday, February 20, 2006	Sheet 23	of 56

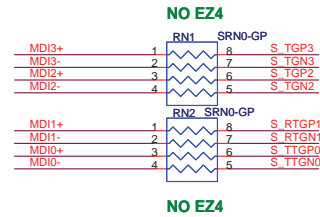


Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

LAN BC5788M

File: **Kirkini** Rev: **SA**

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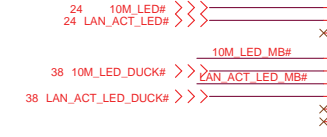
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

Green LED: Speed 100: ON / Speed 10: OFF
 Yellow LED: Link: ON, TX/RX:
 Flash(10Hz).

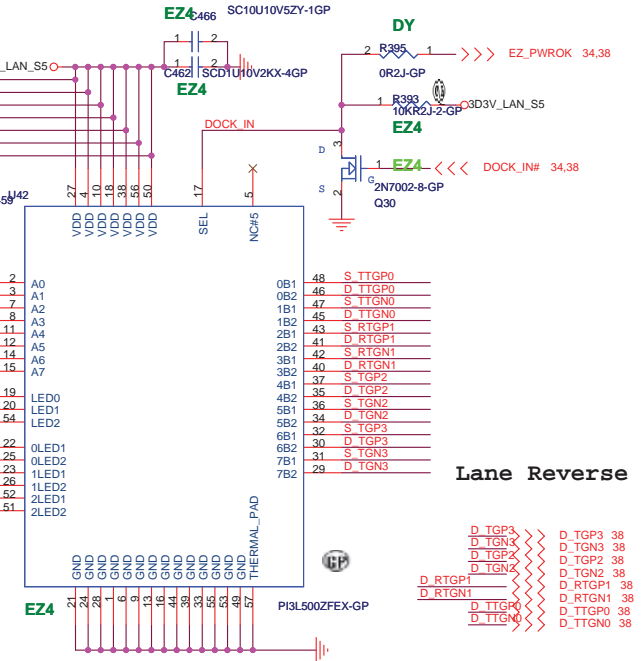
RJ11 signal must leave the other signal
 or power plane 100mil.

DOC_TIP, DOC_RING, TIP_RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

Lane Reverse



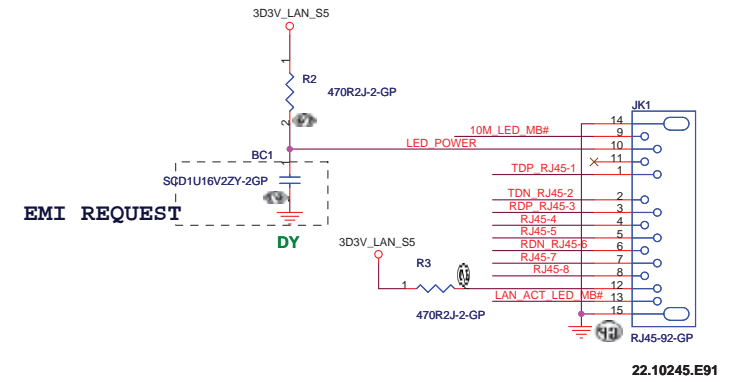
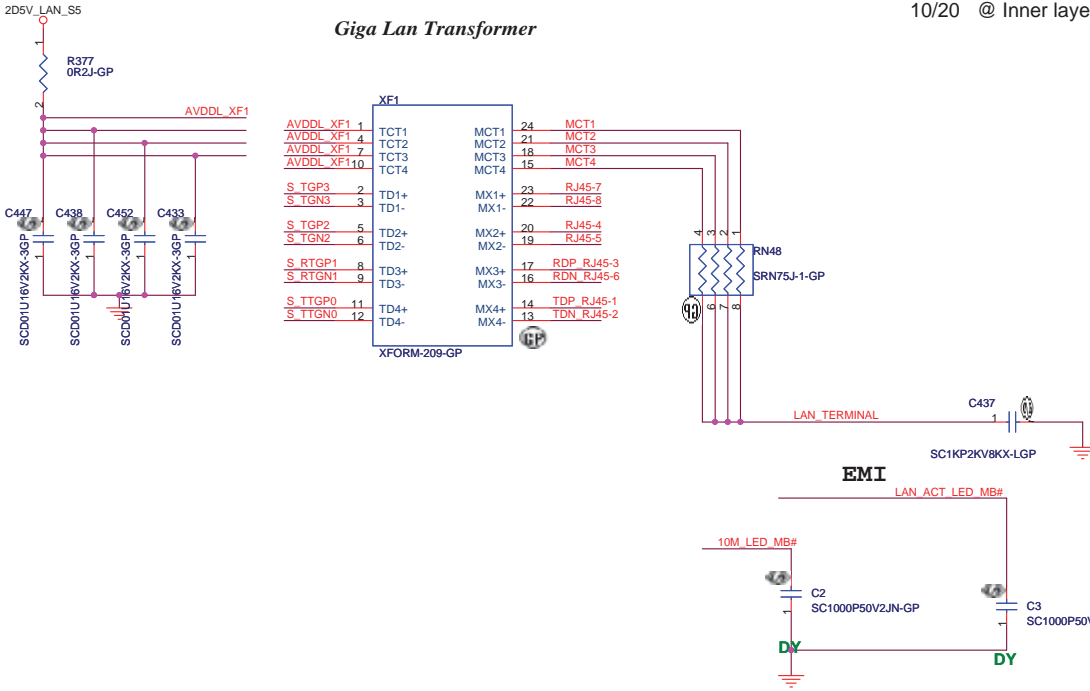
Function	SEL
An to nB1(MB)	L
An to nB2(DUCK)	H



Lane Reverse



RJ45 Connector



Link: Green -10M / 100M / 1Gbps/802.11b
 Activity: Yellow

<Variant Name>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

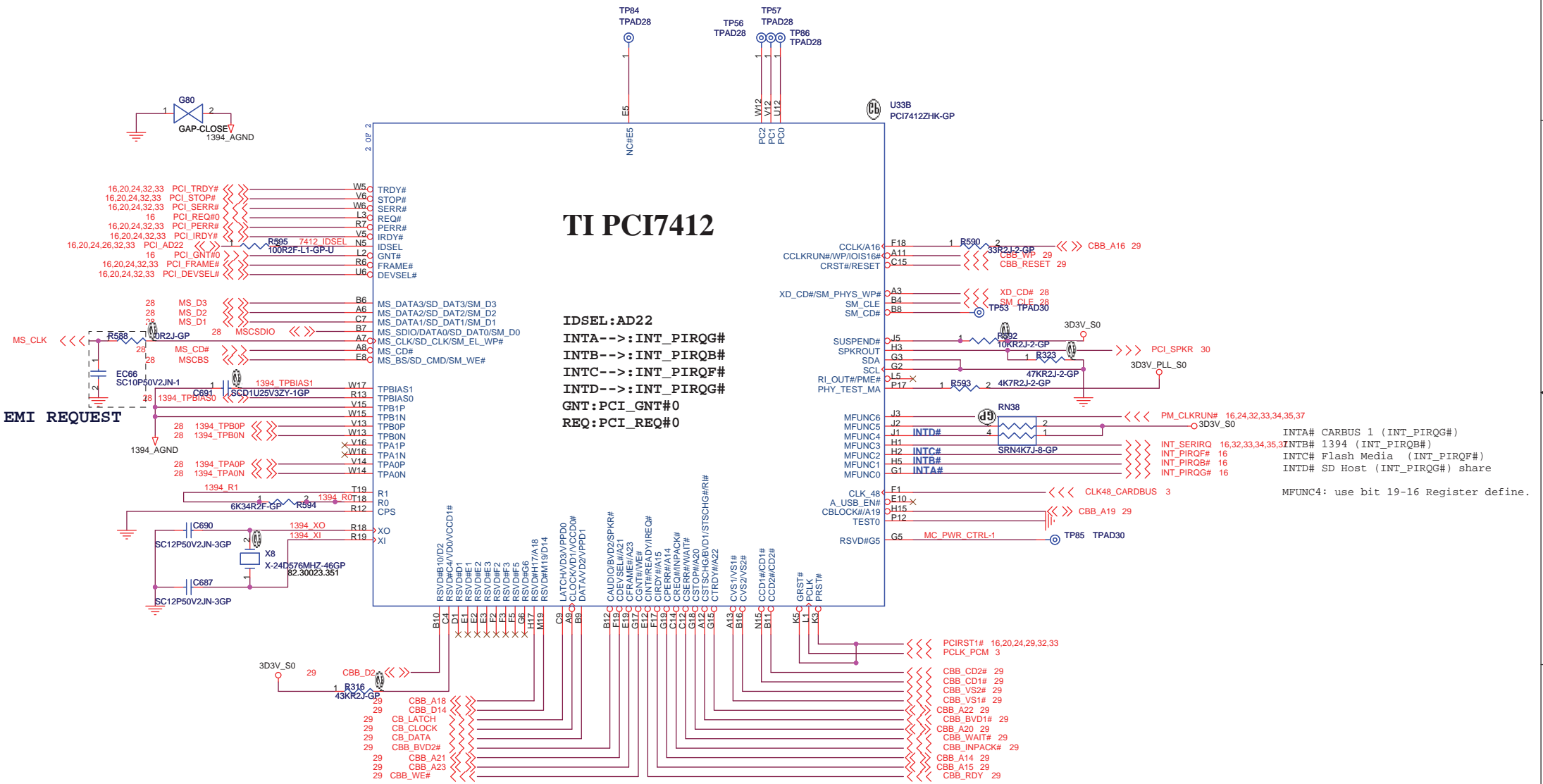
Size	Document Number	Rev
Custom	Kirkini	SA
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- PCI_AD0
- PCI_AD1
- PCI_AD2
- PCI_AD3
- PCI_AD4
- PCI_AD5
- PCI_AD6
- PCI_AD7
- PCI_AD8
- PCI_AD9
- PCI_AD10
- PCI_AD11
- PCI_AD12
- PCI_AD13
- PCI_AD14
- PCI_AD15
- PCI_AD16
- PCI_AD17
- PCI_AD18
- PCI_AD19
- PCI_AD20
- PCI_AD21
- PCI_AD22
- PCI_AD23
- PCI_AD24
- PCI_AD25
- PCI_AD26
- PCI_AD27
- PCI_AD28
- PCI_AD29
- PCI_AD30
- PCI_AD31



MC_PWR_CTRL1_0





TI PCI7412

IDSEL: AD22
INTA-->: INT_PIRQ#
INTB-->: INT_PIRQ#
INTC-->: INT_PIRQ#
INTD-->: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

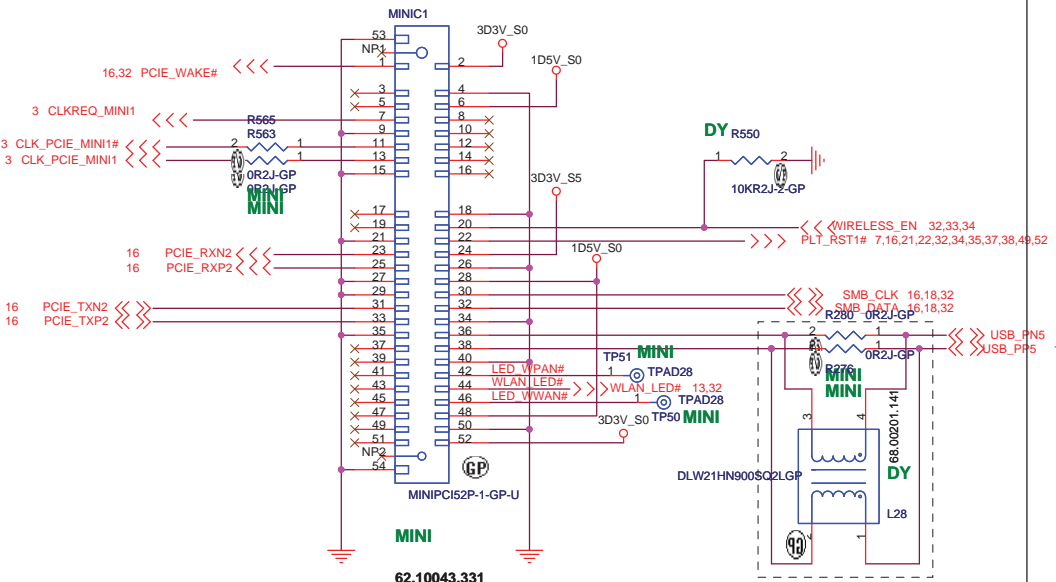
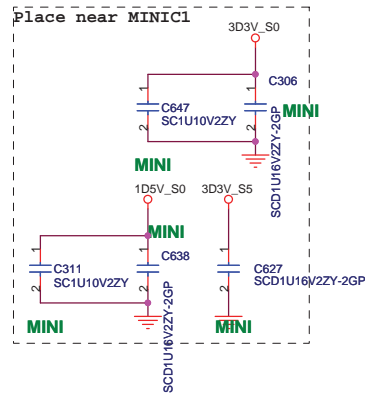
EMI REQUEST

INTA# CARBUS 1 (INT_PIRQ#)
 INTB# 1394 (INT_PIRQ#)
 INTC# Flash Media (INT_PIRQ#)
 INTD# SD Host (INT_PIRQ#) share
 MFUNC4: use bit 19-16 Register define.

<Variant Name>

緯創資通		Wistron Corporation	
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TI PCI7412 (2 of 2)			
Title	Document Number	Rev	
	Kirkini	SA	
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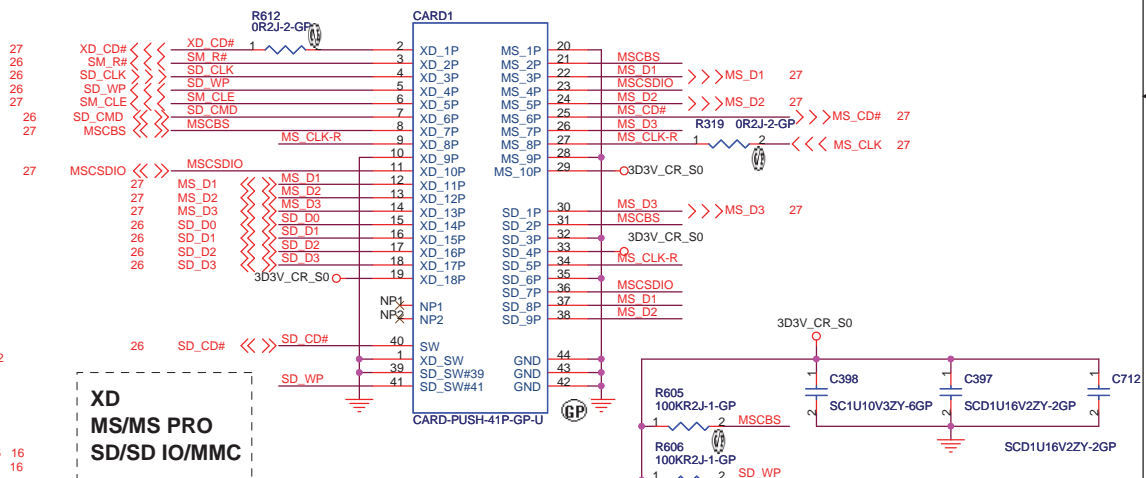
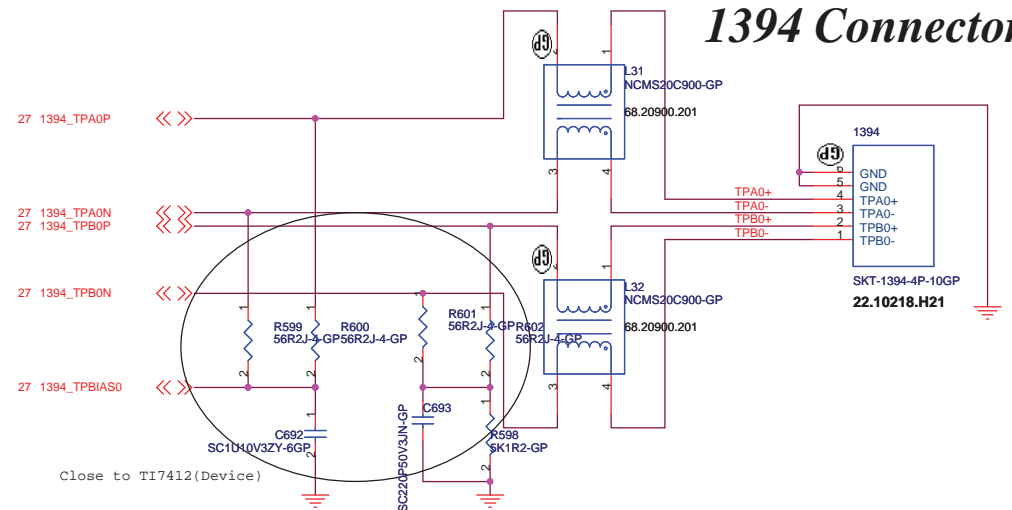
Mini Card Connector



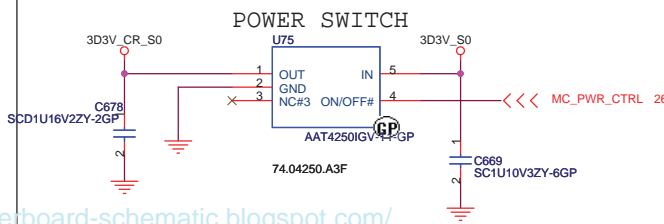
EMI REQUEST

62.10043.331

1394 Connector



Bottom VIEW



<Variant Name>

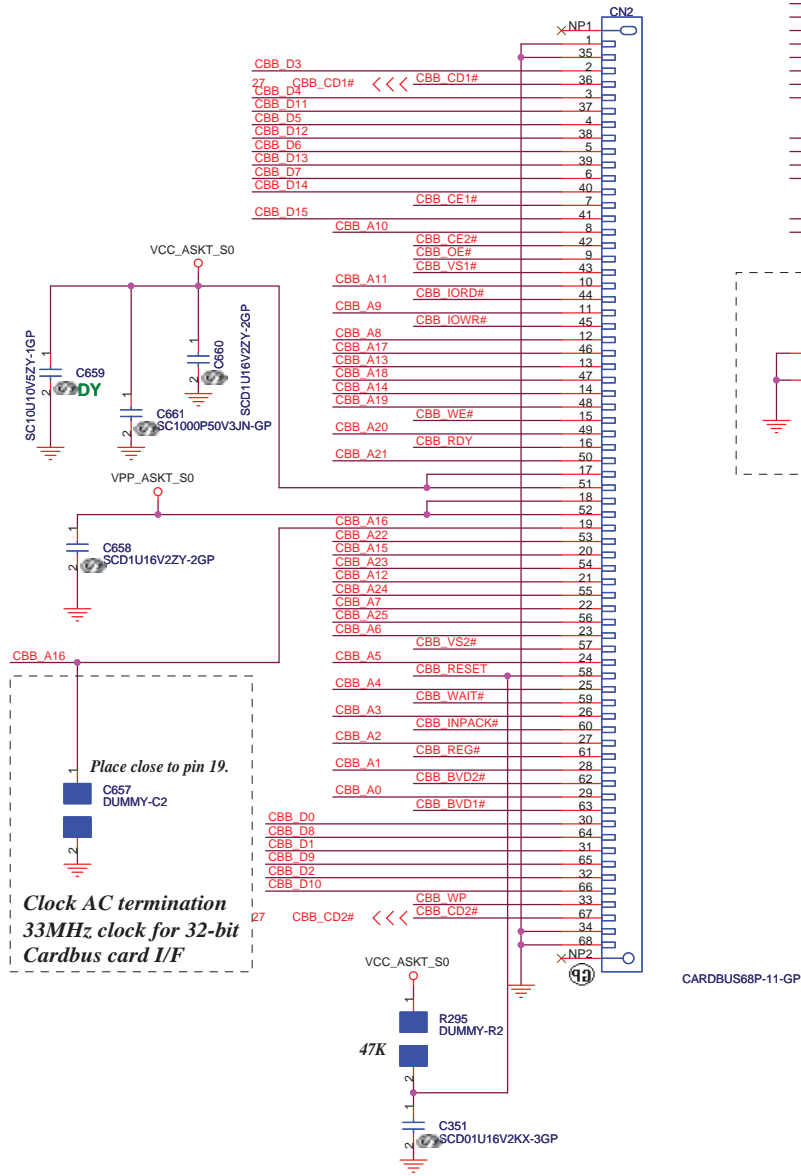
緯創資通 Wistron Corporation
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Title: **MINI CARD / 1394/6 in 1 card**

Size A3 Document Number: **Kirkini** Rev: **SA**

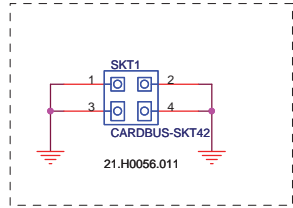
Date: Monday, February 20, 2006 Sheet 28 of 56

PCMCIA Socket

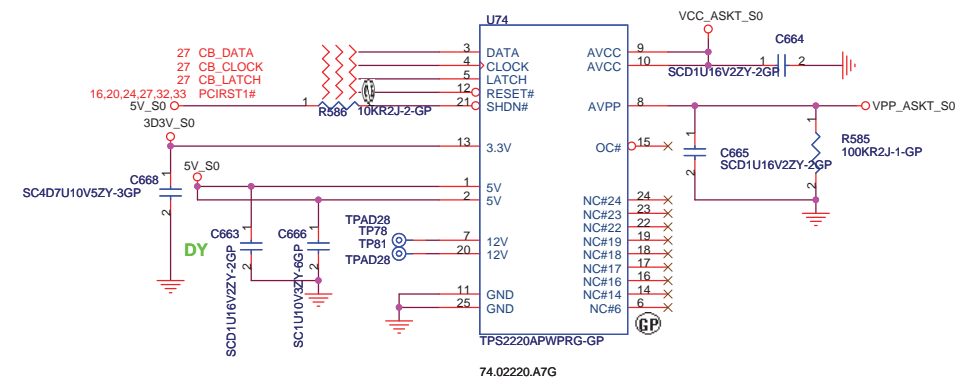


Cardbus I/F

- CBB_D[0..15] 26,27
 CBB_A[0..25] 26,27
- CBB_IORD# 26
 CBB_IOWR# 26
 CBB_OE# 26
 CBB_WE# 27
 CBB_REG# 26
 CBB_RDY 27
 CBB_WP 27
 CBB_RESET 27
 CBB_WAIT# 27
 CBB_INPACK# 27
- CBB_CE1# 26
 CBB_CE2# 26
 CBB_BVD1# 27
 CBB_BVD2# 27
- CBB_VS1# 27
 CBB_VS2# 27



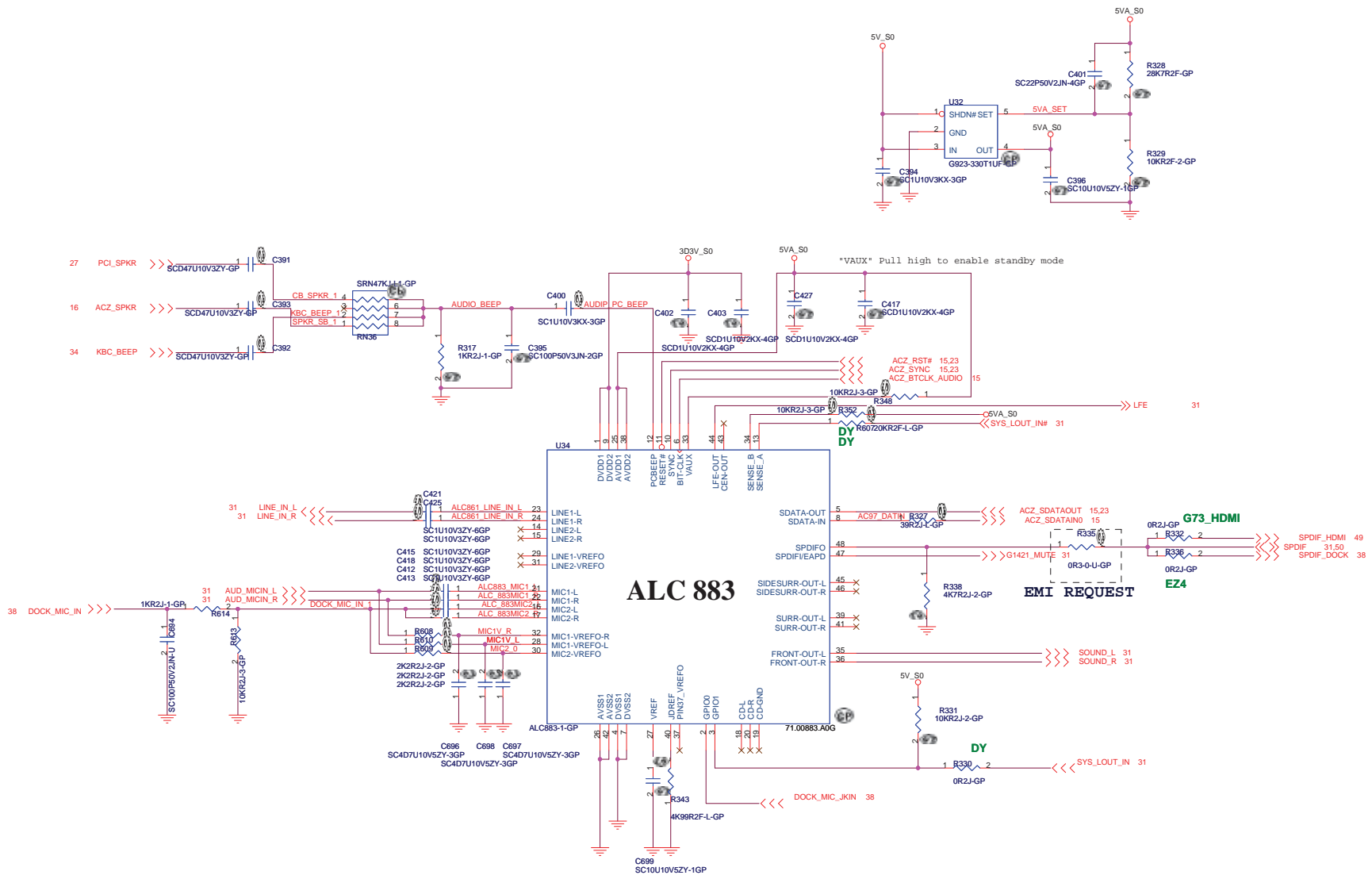
Power switch

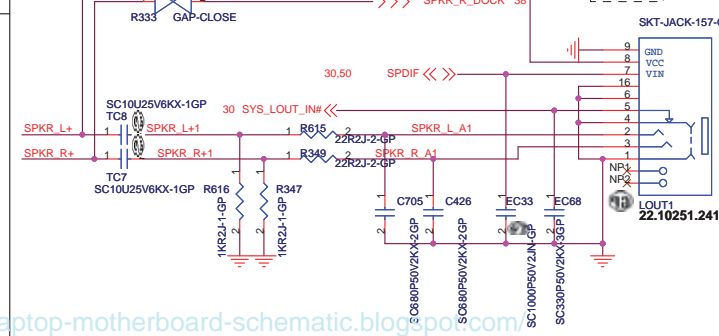
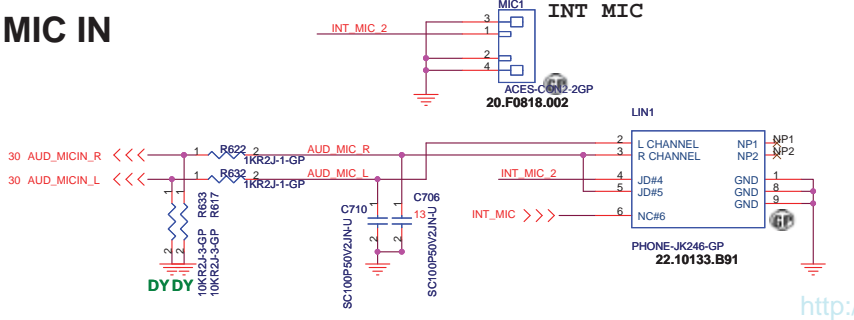
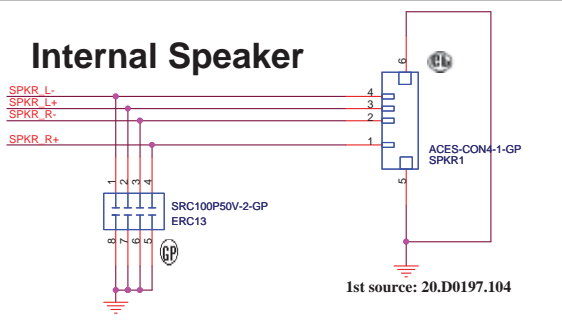
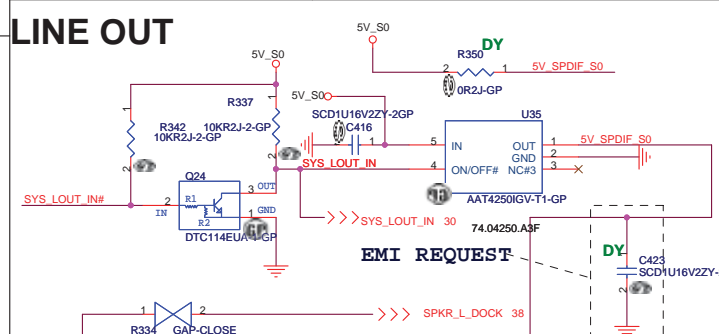
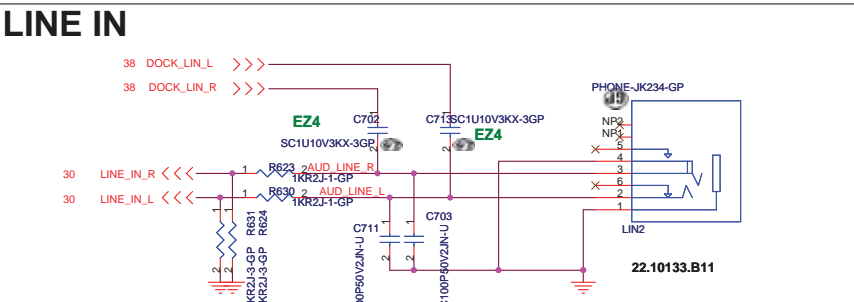
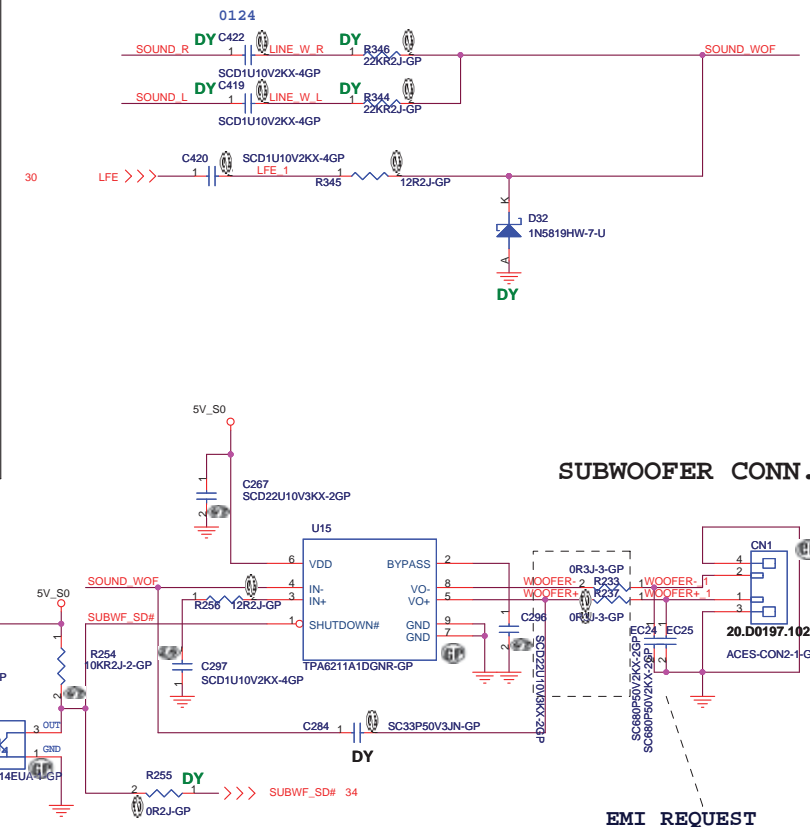
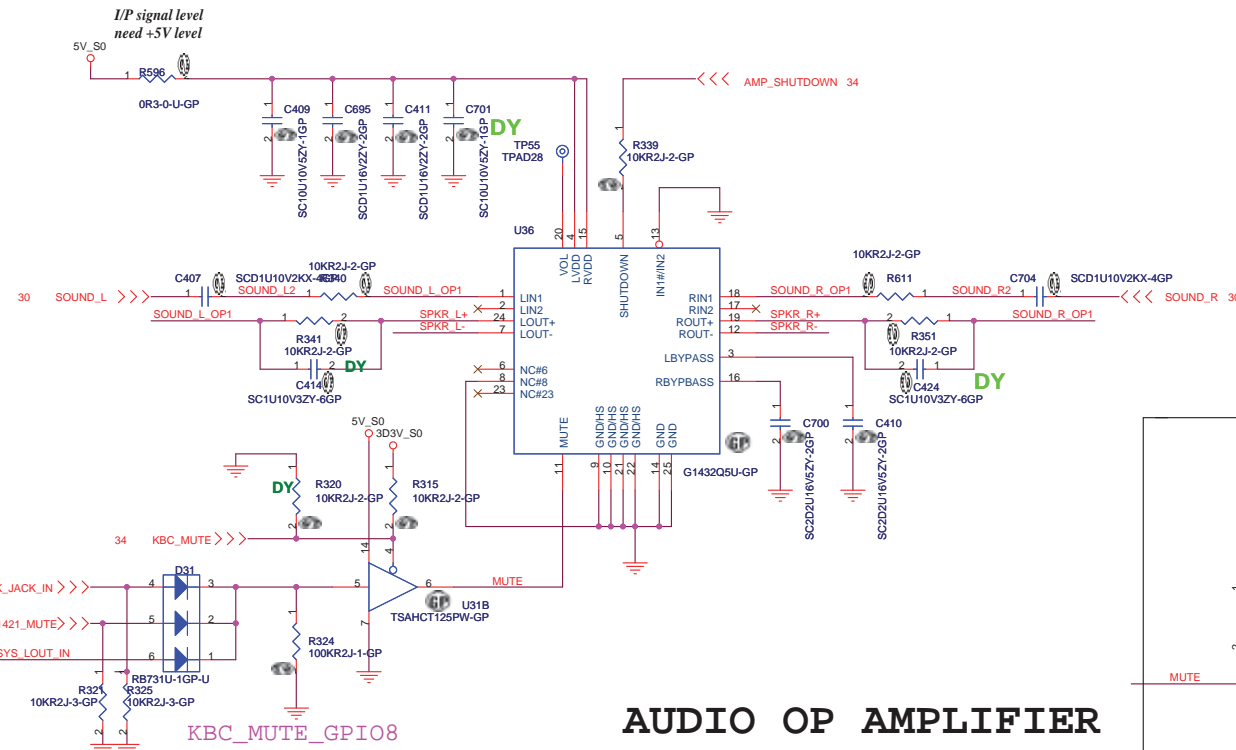


CARDBUS68P-11-GP

<Variant Name>

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PCMCIA/WEB Camera	
Title	
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Kirkini	SA





SPDIF FUNCTION

VCC	VIN	LED
0	>2	ON
5	2	MORE ON
5	0	OFF

<Core Design>

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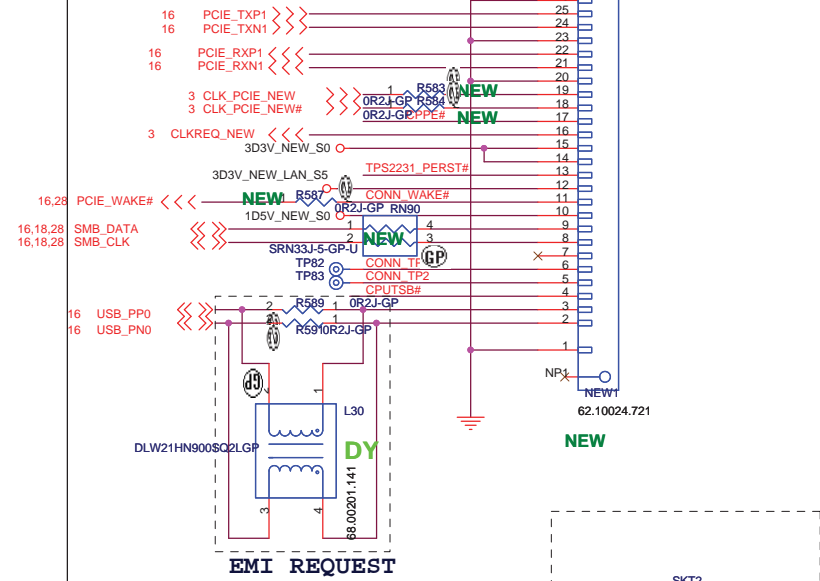
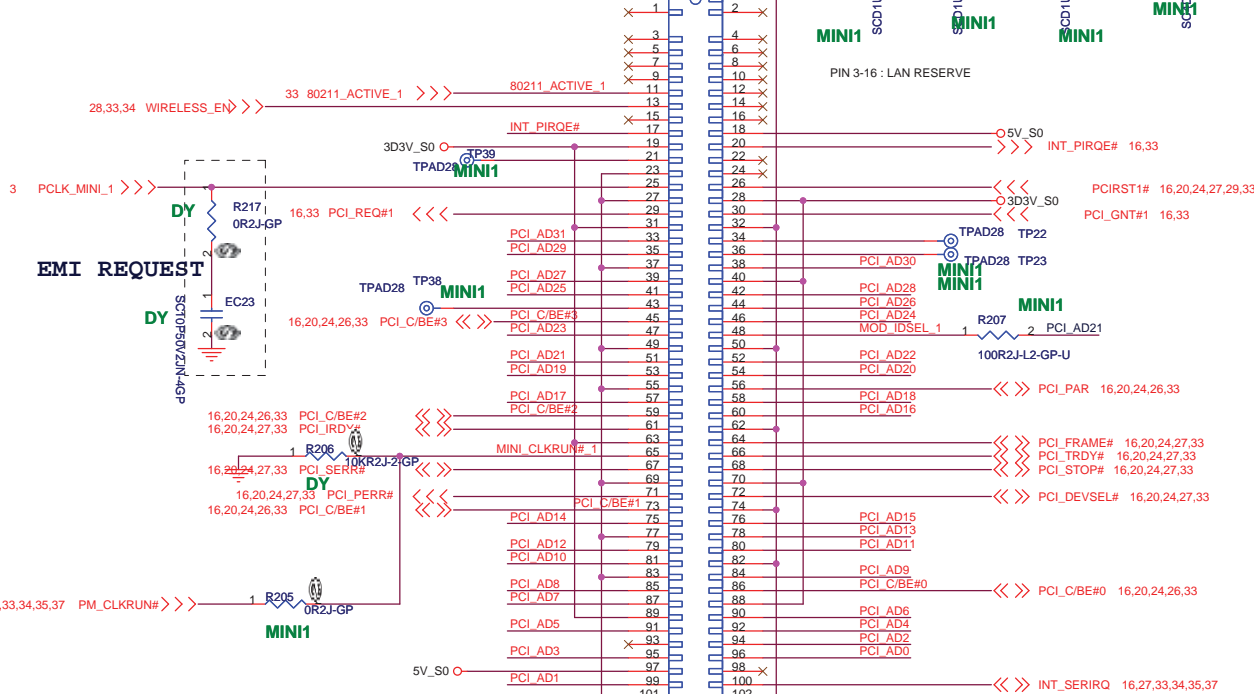
Kirkini

AUDIO AMP AND JACK

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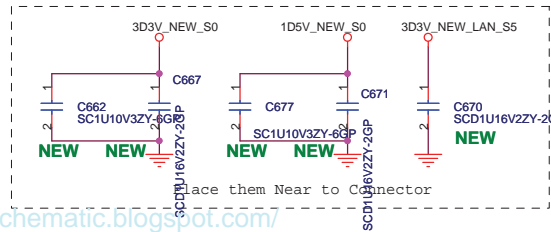
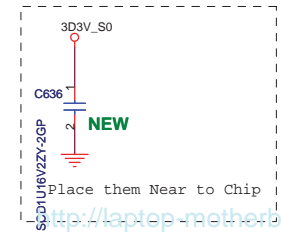
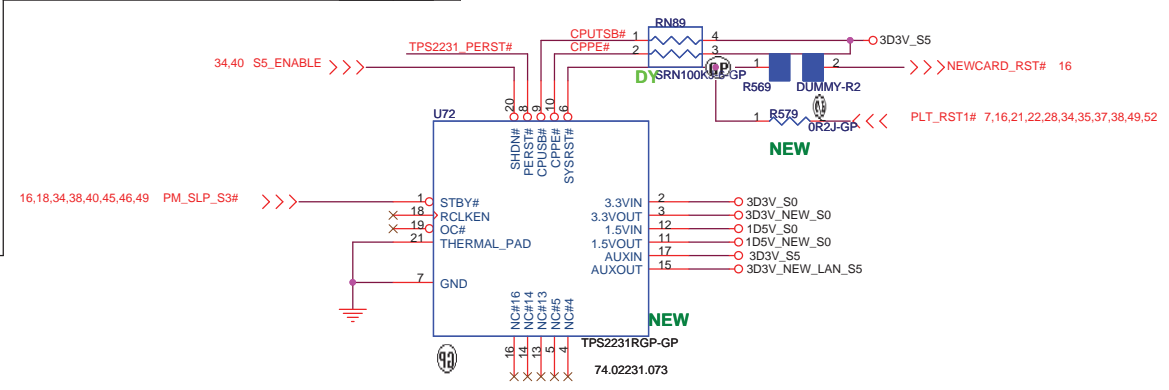
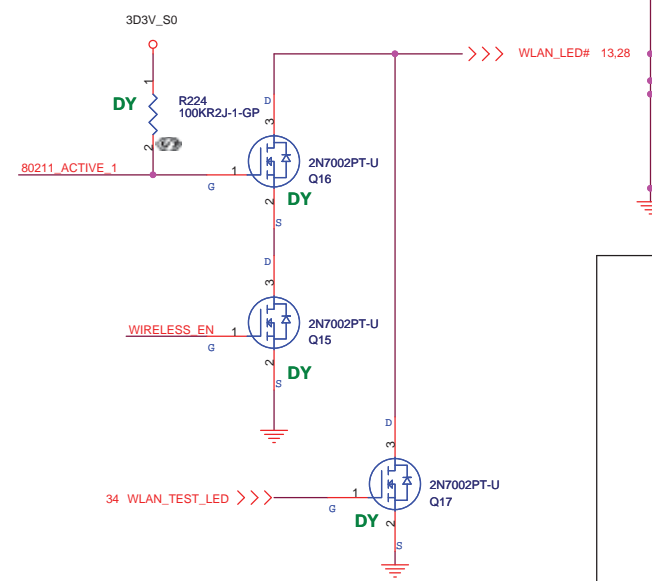
16,20,24,26,27,33 PCI_AD[0..31]

IDSEL:AD21
INTA-->:INT_PIRQ#
GNT:PCI_GNT1#
REQ:PCI_REQ1#



NEWCARD Connector

Reserve the symbol for bottom side connector



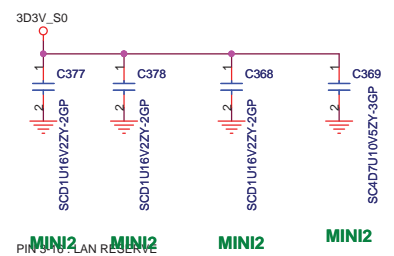
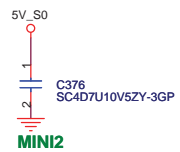
緯創資通 Wistron Corporation
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Title: **MINI-PC-11/NEW Card**

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16,20,24,26,27,32 PCI_AD[0..31] <<<

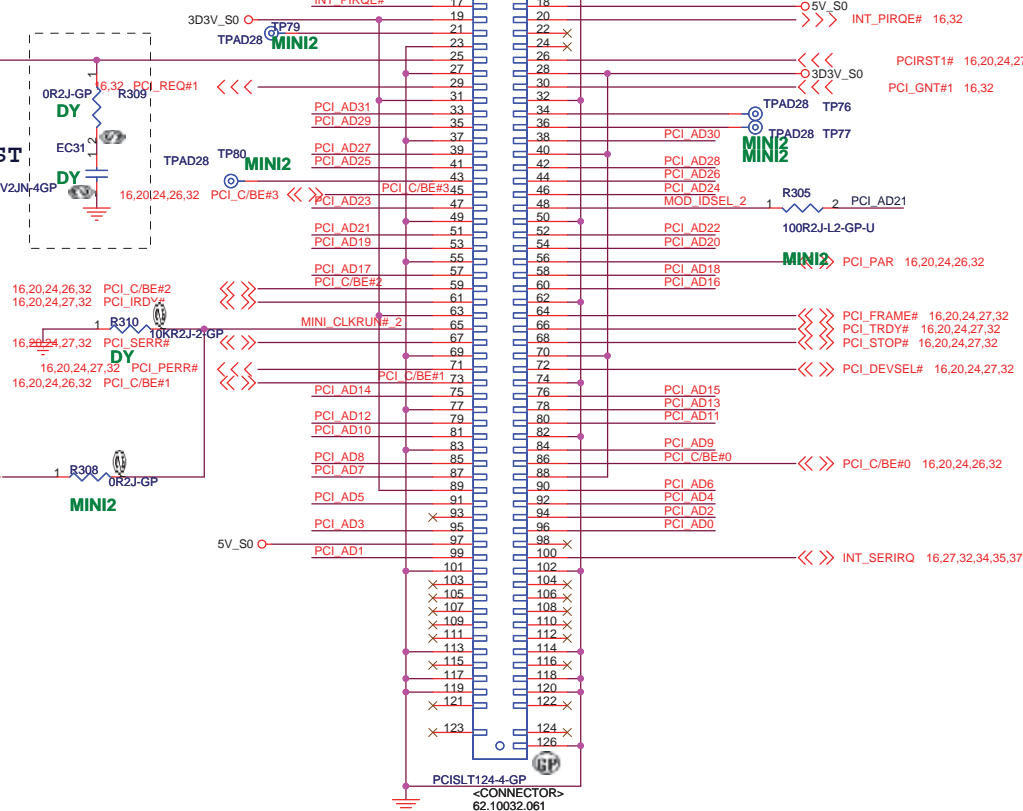
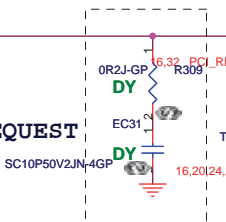
IDSEL:AD17
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 GNT:PCI_GNT4#
 REQ:PCI_REQ4#



28,32,34 WIRELESS_EN# >>> 32 80211_ACTIVE_1 >>> 80211_ACTIVE_1

3 PCLK_MINI_2 >>>

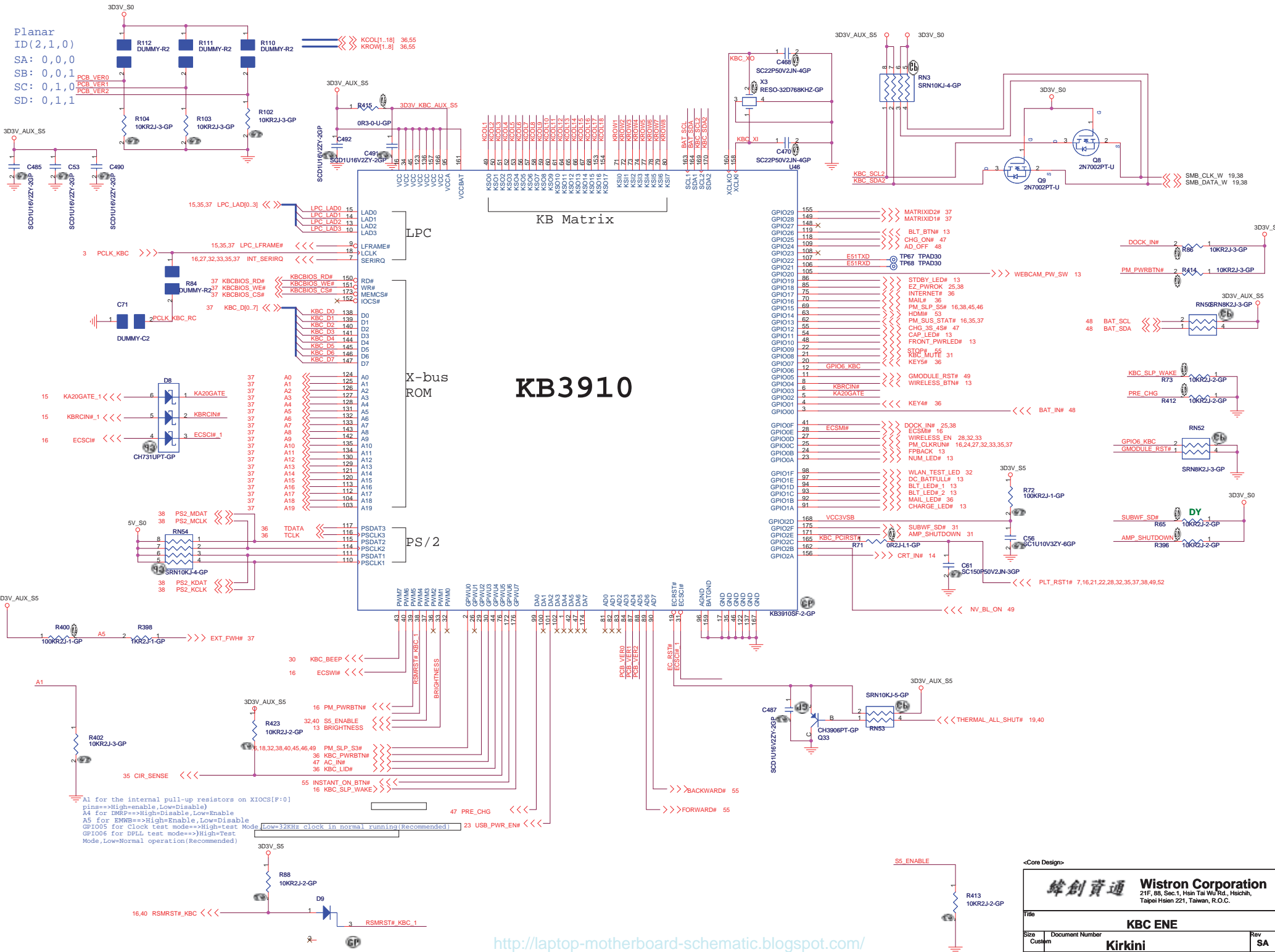
EMI REQUEST



2nd source: 62.10043.151
 MINI2

<Variant Name>

Title MINI-PCI-2		
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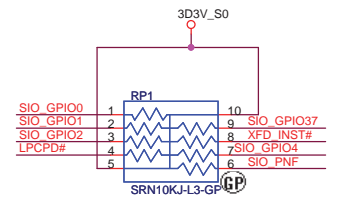
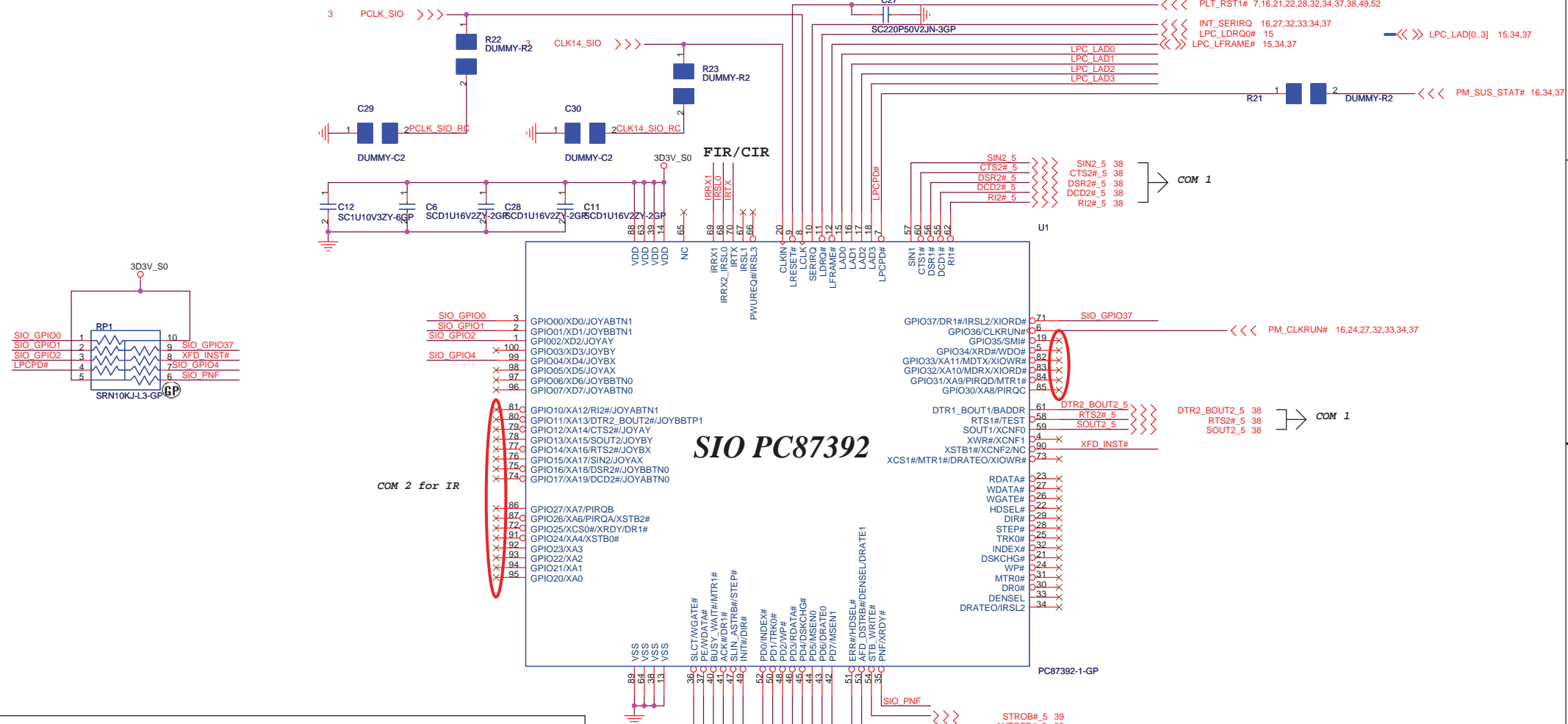


<http://laptop-motherboard-schematic.blogspot.com/>

Wistron Corporation
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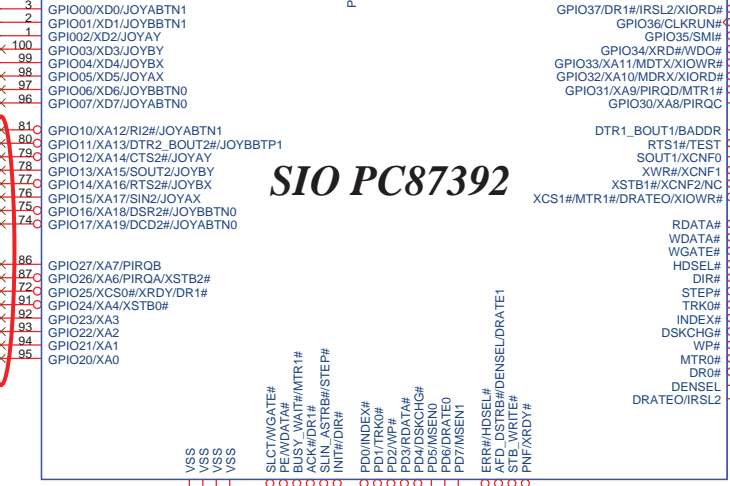
KBC ENE

Size: Custom Document Number: Kirkini Rev: SA
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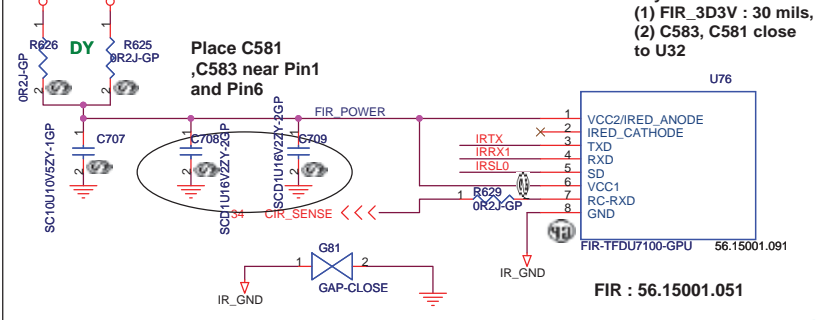


COM 2 for IR

SIO PC87392



VISHAY FIR/CIR Module



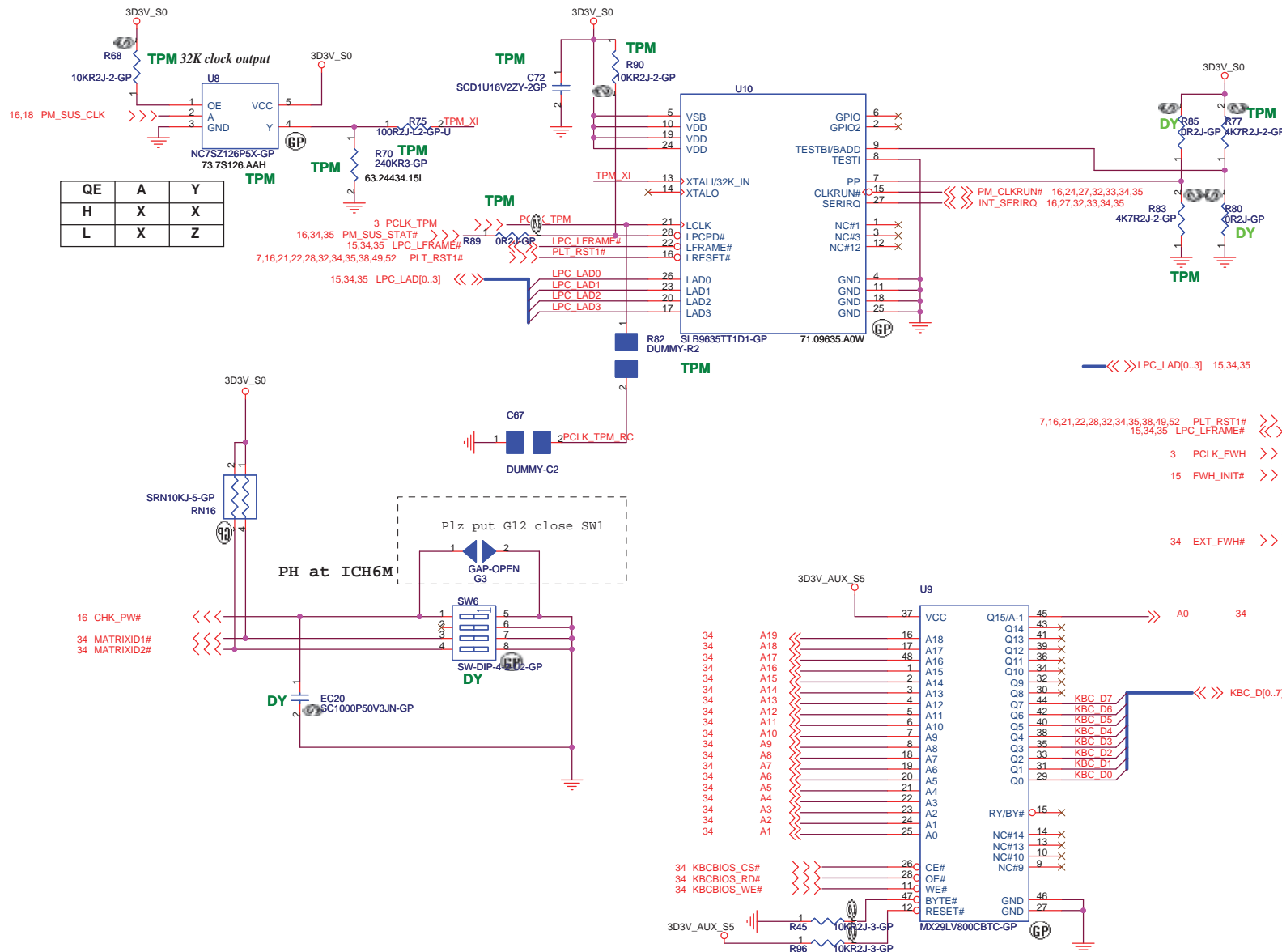
<http://laptop-motherboard-schematic.blogspot.com/>

緯創資通 Wistron Corporation
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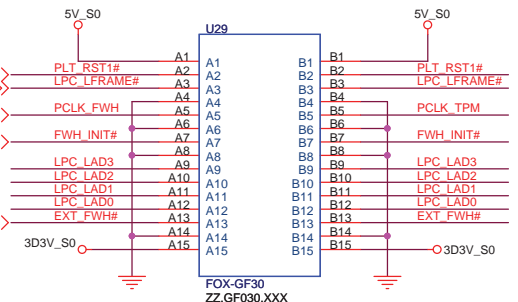
Title: **SIO 87392 / FIR / CIR**

Size A3 Document Number: **Kirkini** Rev: **SA**

Date: Monday, February 20, 2006 Sheet 35 of 56



GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46

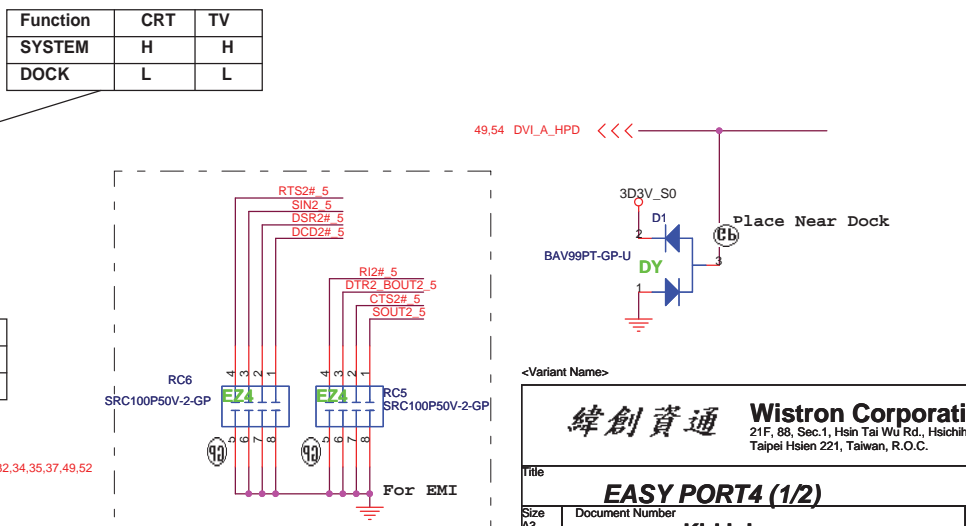
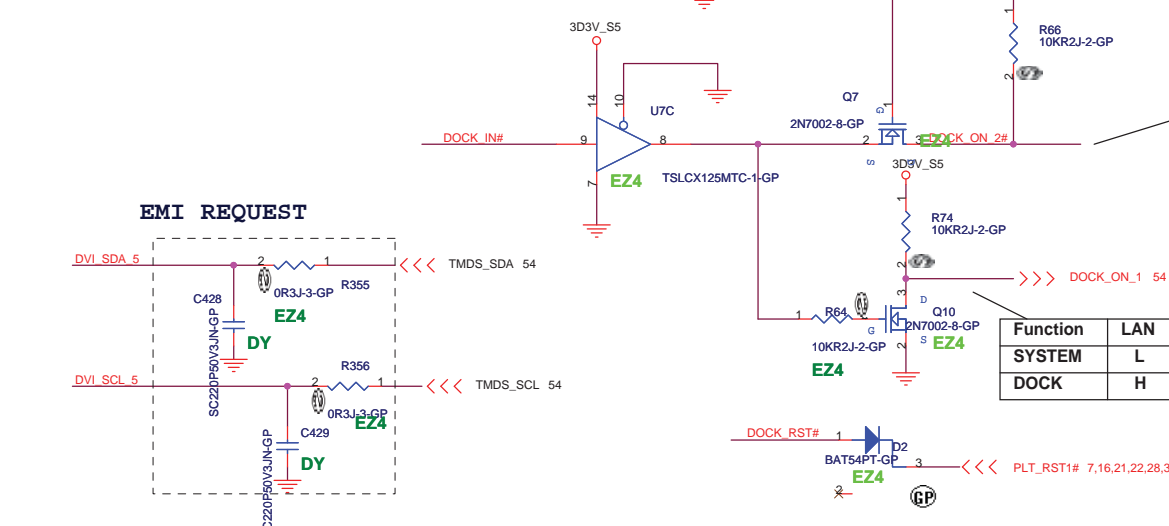
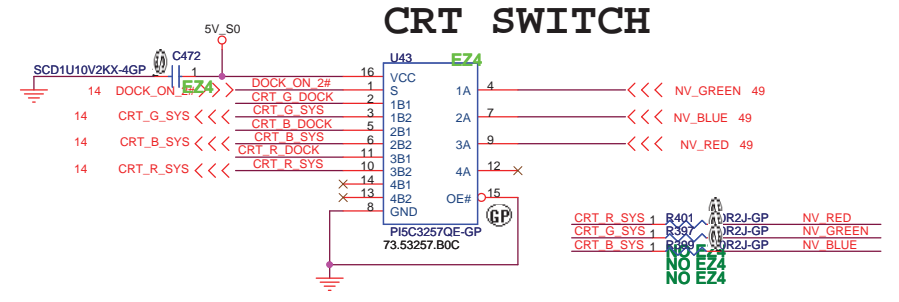
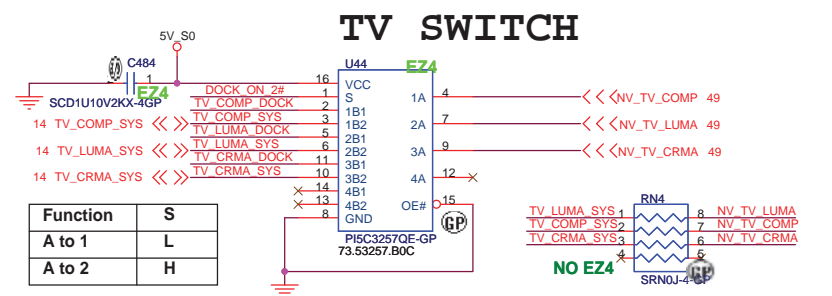
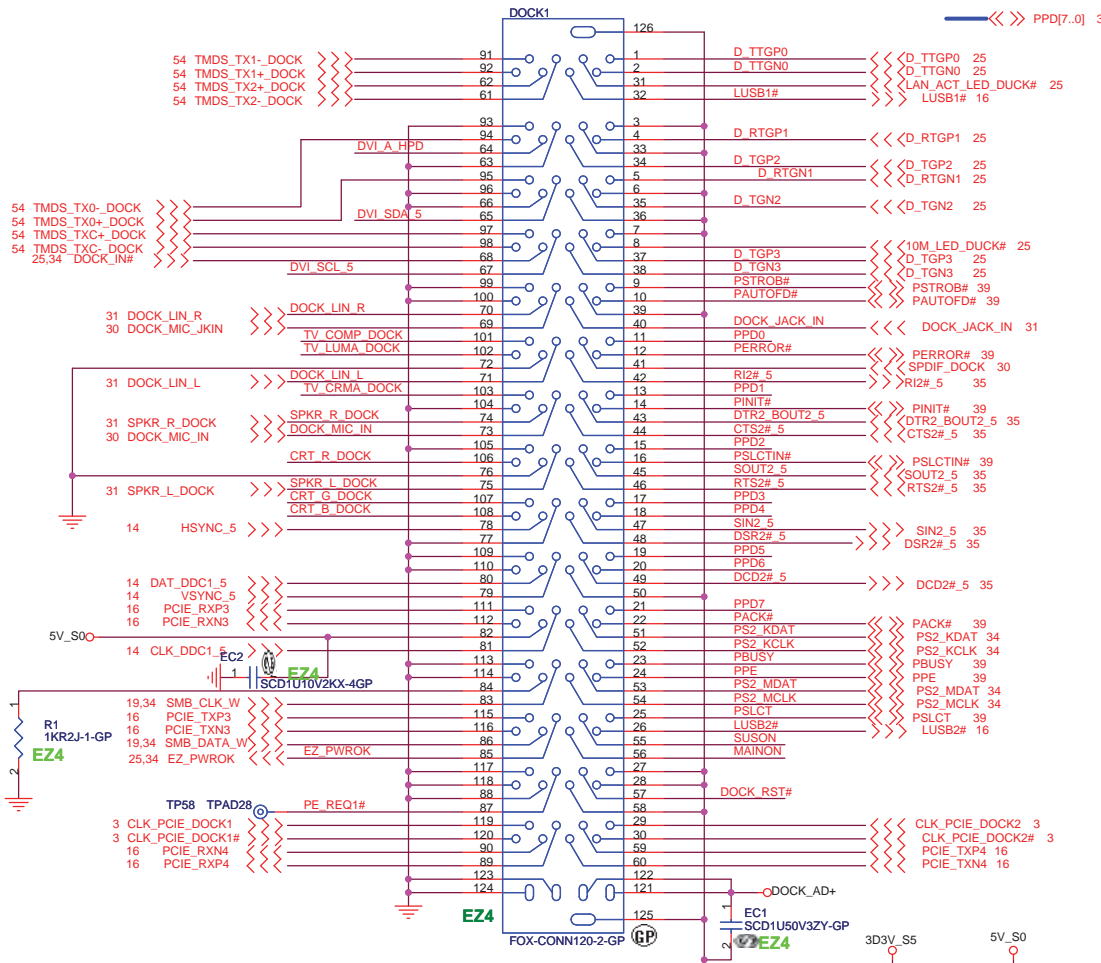
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **TPM & BIOS**

Size A3 Document Number: **Kirkini** Rev: **SA**

Date: Monday, February 20, 2006 Sheet 37 of 56



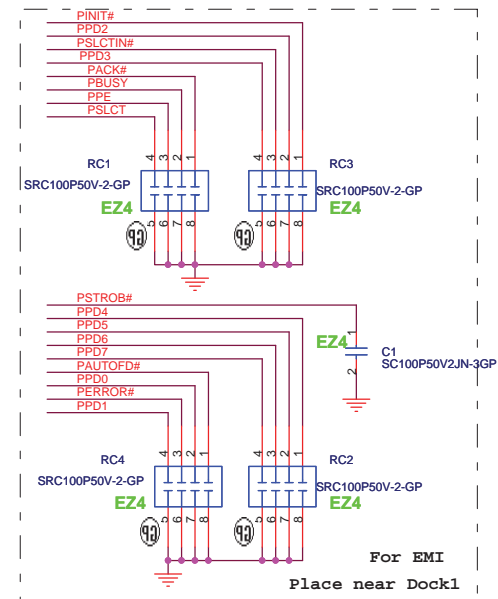
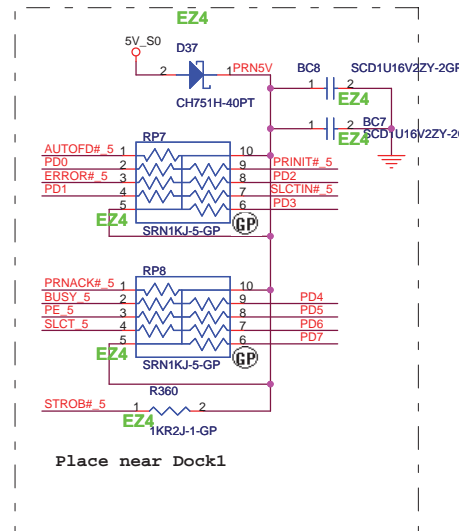
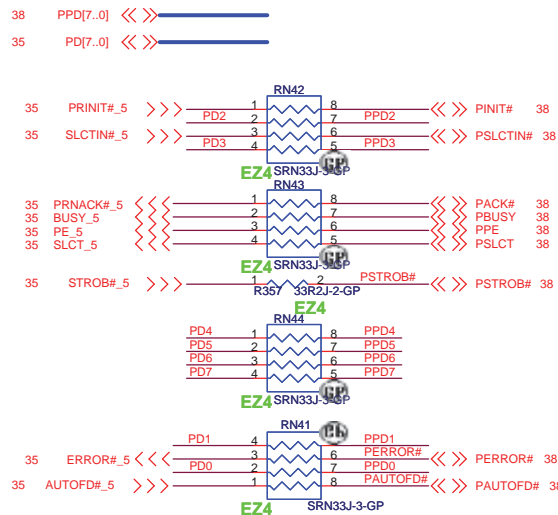
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EASY PORT4 (1/2)**

Size A3 Document Number: **Kirkini** Rev: **SA**

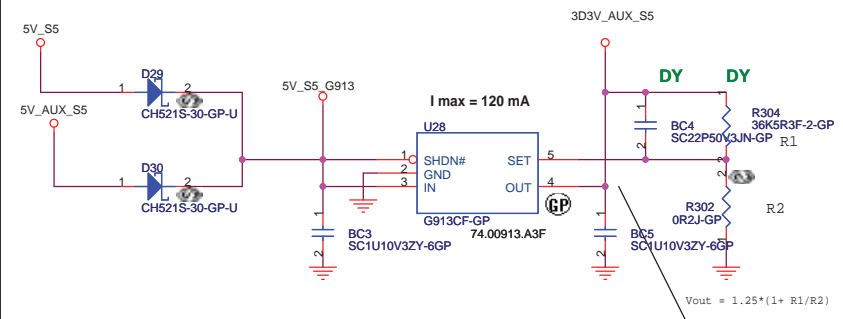
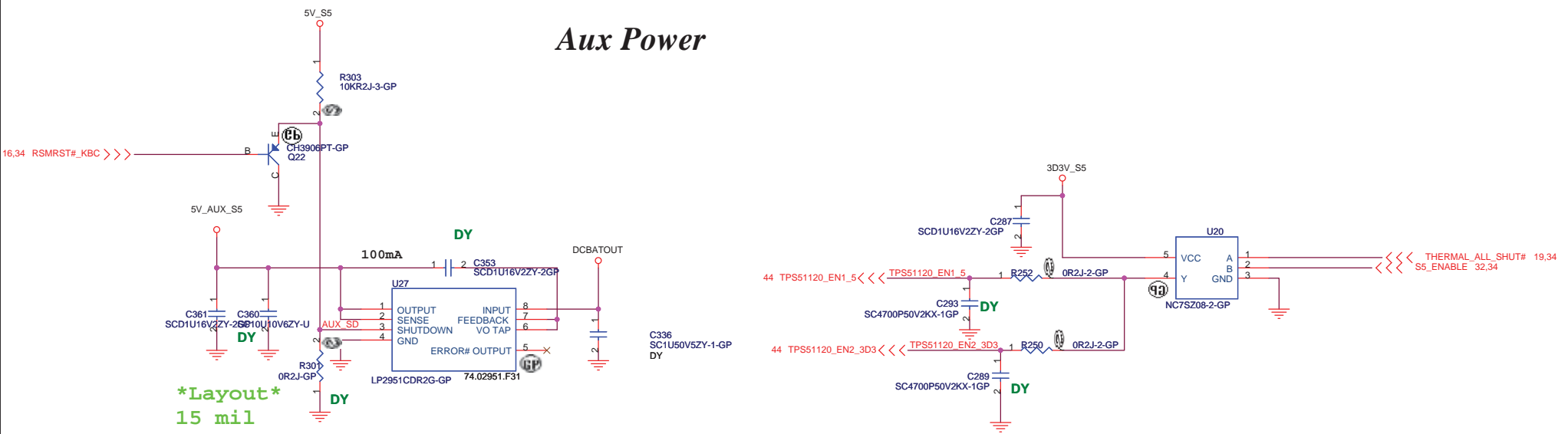
Date: Monday, February 20, 2006 Sheet 38 of 56

PRINT PORT

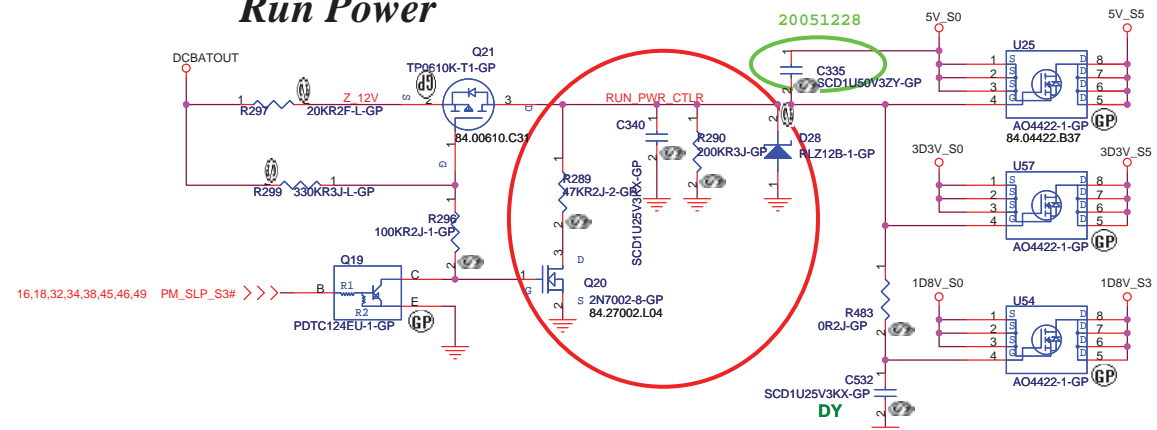


<Variant Name>

Aux Power



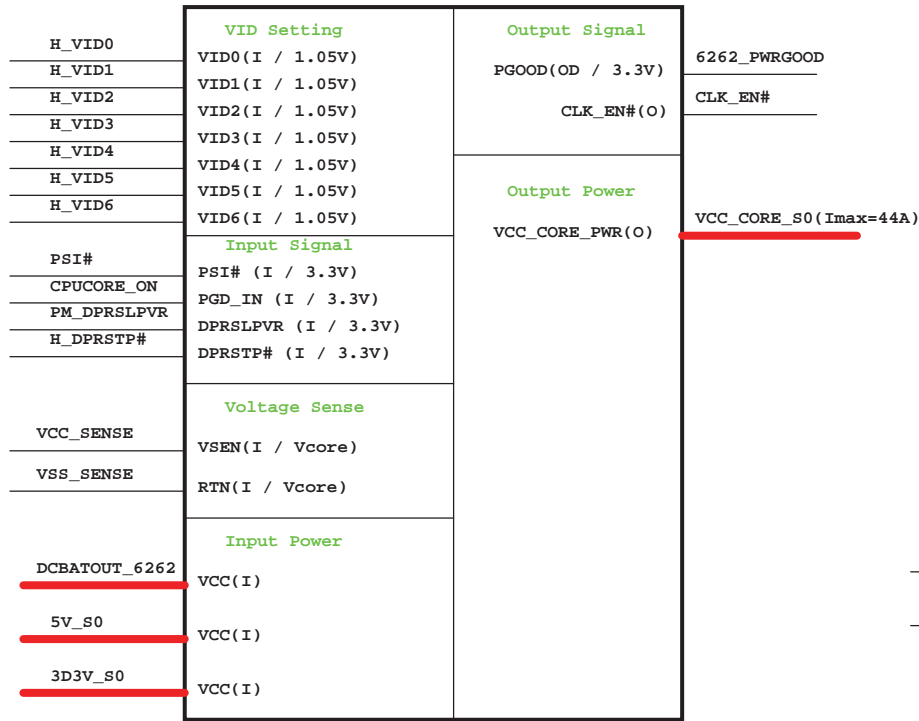
Run Power



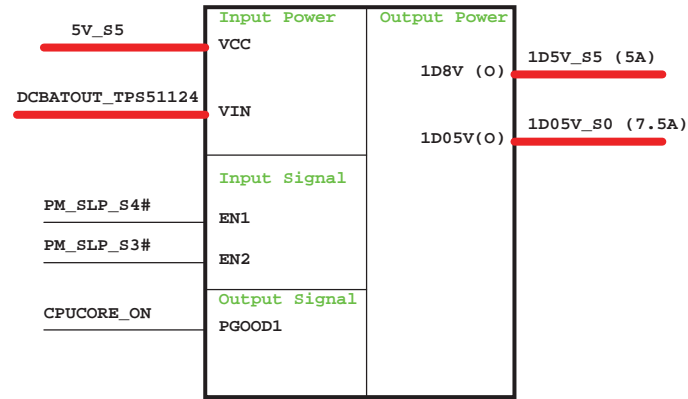
<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
TITLE		
RUN and AUX POWER		
Size A3	Document Number Kirkini	Rev SA
Date: Monday, February 20, 2006	Sheet 40	of 56

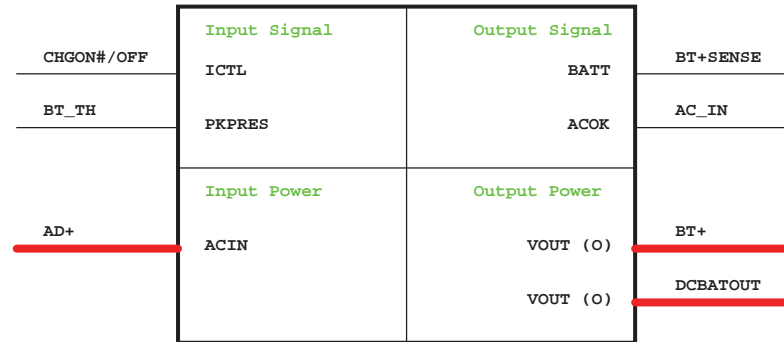
CPU_CORE
Intersil ISL6262



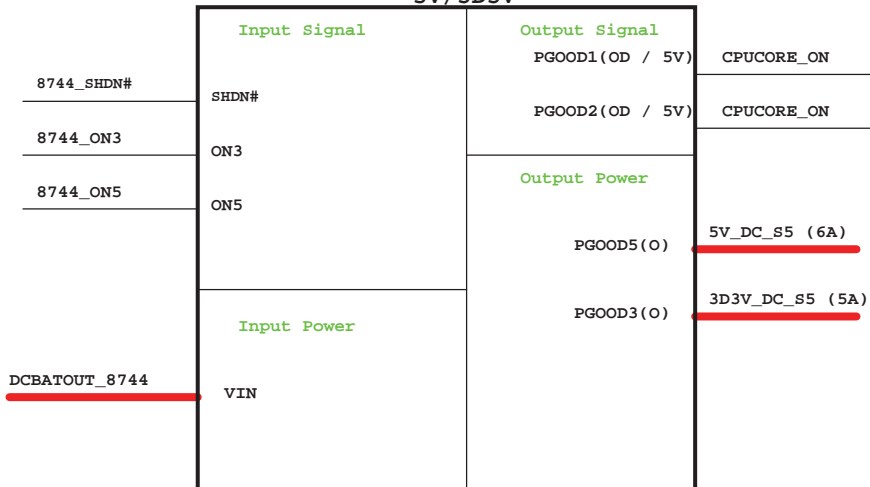
TI TPS51124
1D5V/1D05V



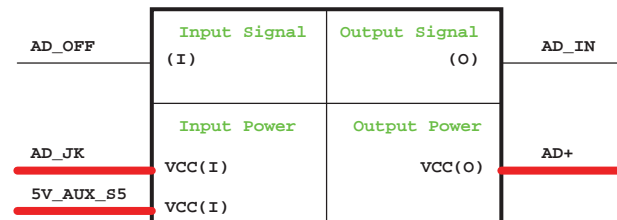
Charger ISL6255



MAX8744
5V/3D3V



Adapter

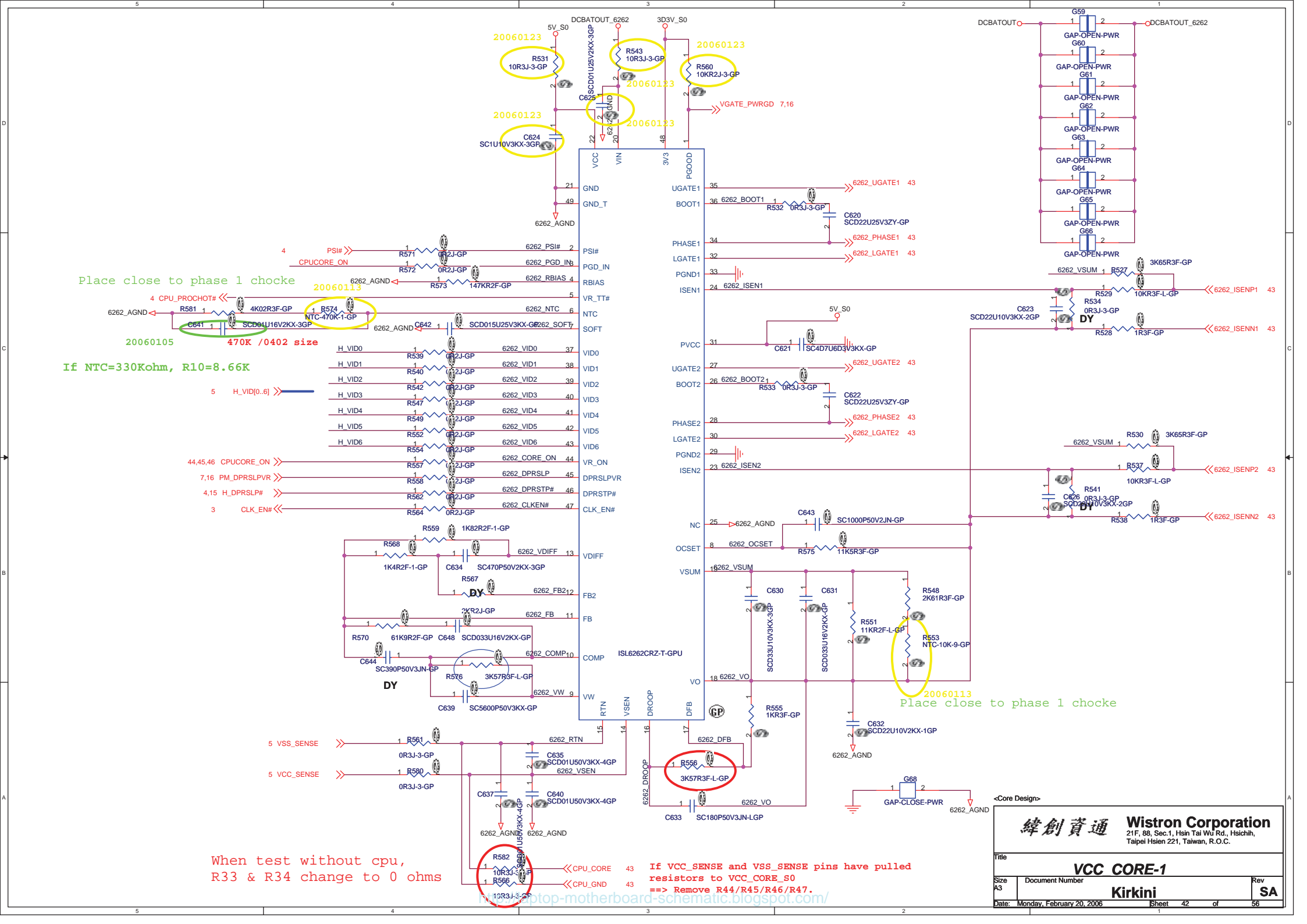


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size: A3	Document Number: Kirkini	Rev: SA
Date: Monday, February 20, 2006	Sheet: 41 of 56	



Place close to phase 1 choke

IF NTC=330Kohm, R10=8.66K

Place close to phase 1 choke

When test without cpu, R33 & R34 change to 0 ohms

If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0 ==> Remove R44/R45/R46/R47.

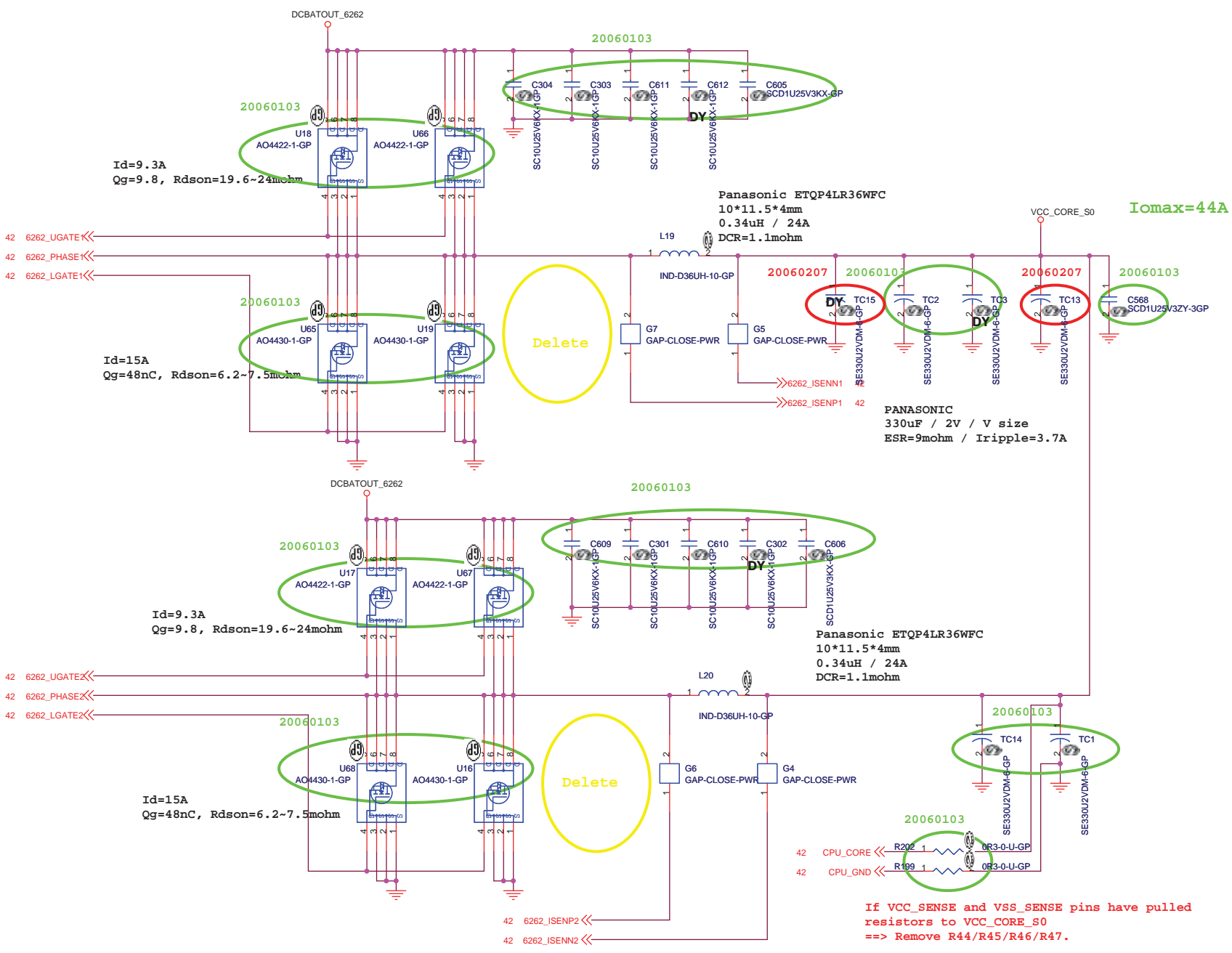
- 4 CPU_PROCHOT# <<<
- 4 CPUCORE_ON <<<
- 5 H_VID[0..6] <<<
- 44,45,46 CPUCORE_ON <<<
- 7,16 PM DPRSLPVR <<<
- 4,15 H DPRSLP# <<<
- 3 CLK_EN# <<<

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VCC CORE-1**

Size A3 Document Number **Kirkini** Rev SA

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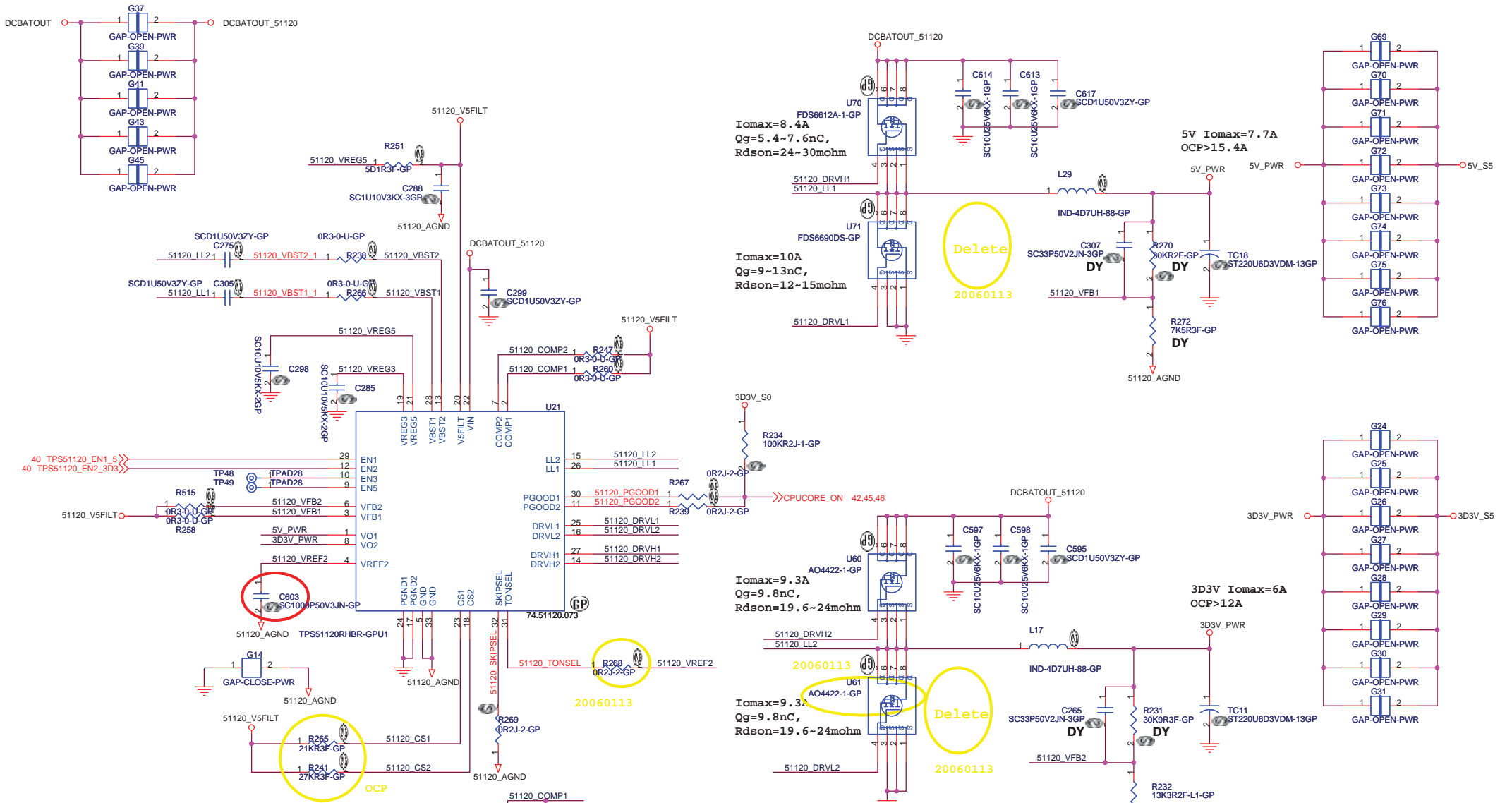
Delete

Delete

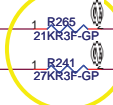
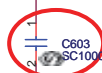
If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: VCC CORE 2		
Size: A3	Document Number:	Rev: SA
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40 TPS51120_EN1_5
40 TPS51120_EN2_3D3



20060113

20060113

20060113

$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	Fixed Output 3.3V
VFB2	N/A	not use	ADJ.	Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

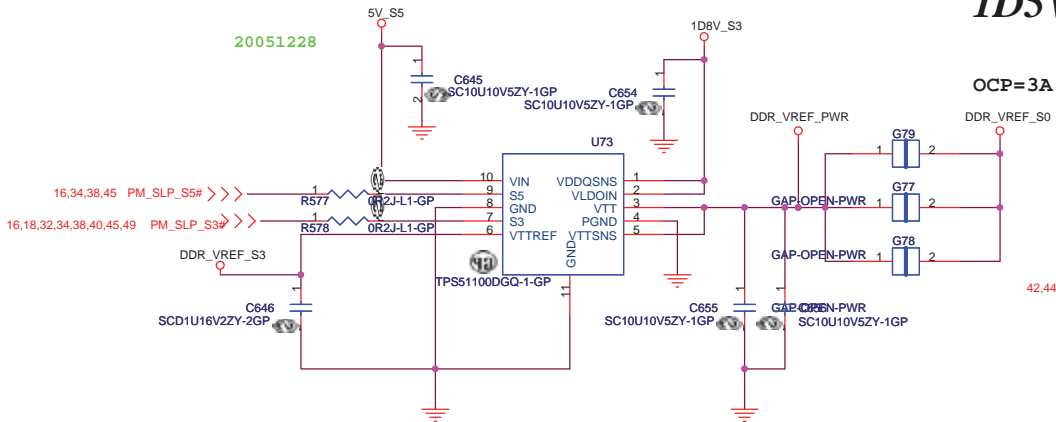
Title: **TPS51120 5V/3D3V**

Size A3 Document Number: **Kirkini** Rev: **SA**

Date: Monday, February 20, 2006 Sheet 44 of 56

0D9V

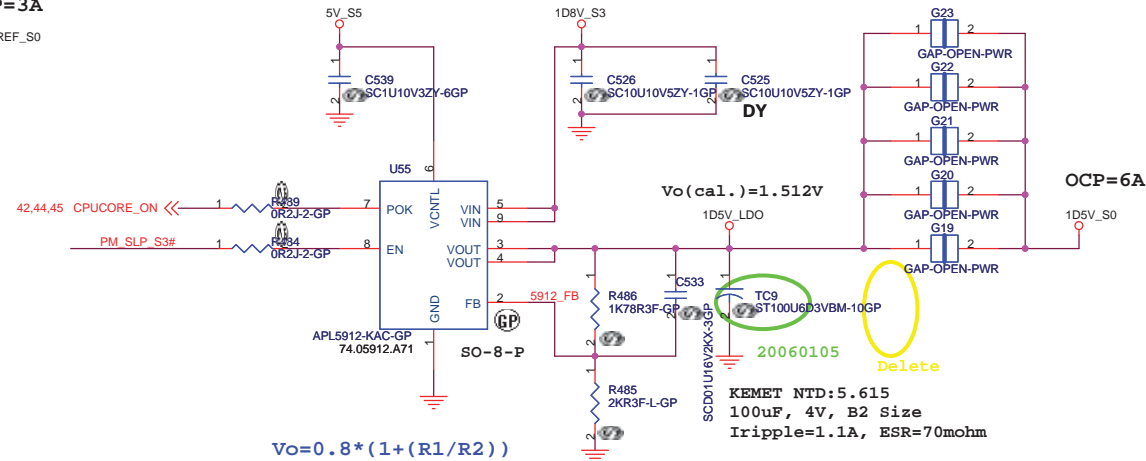
0D9V_S3
Iomax=1.5A



1D5V

OCP=3A

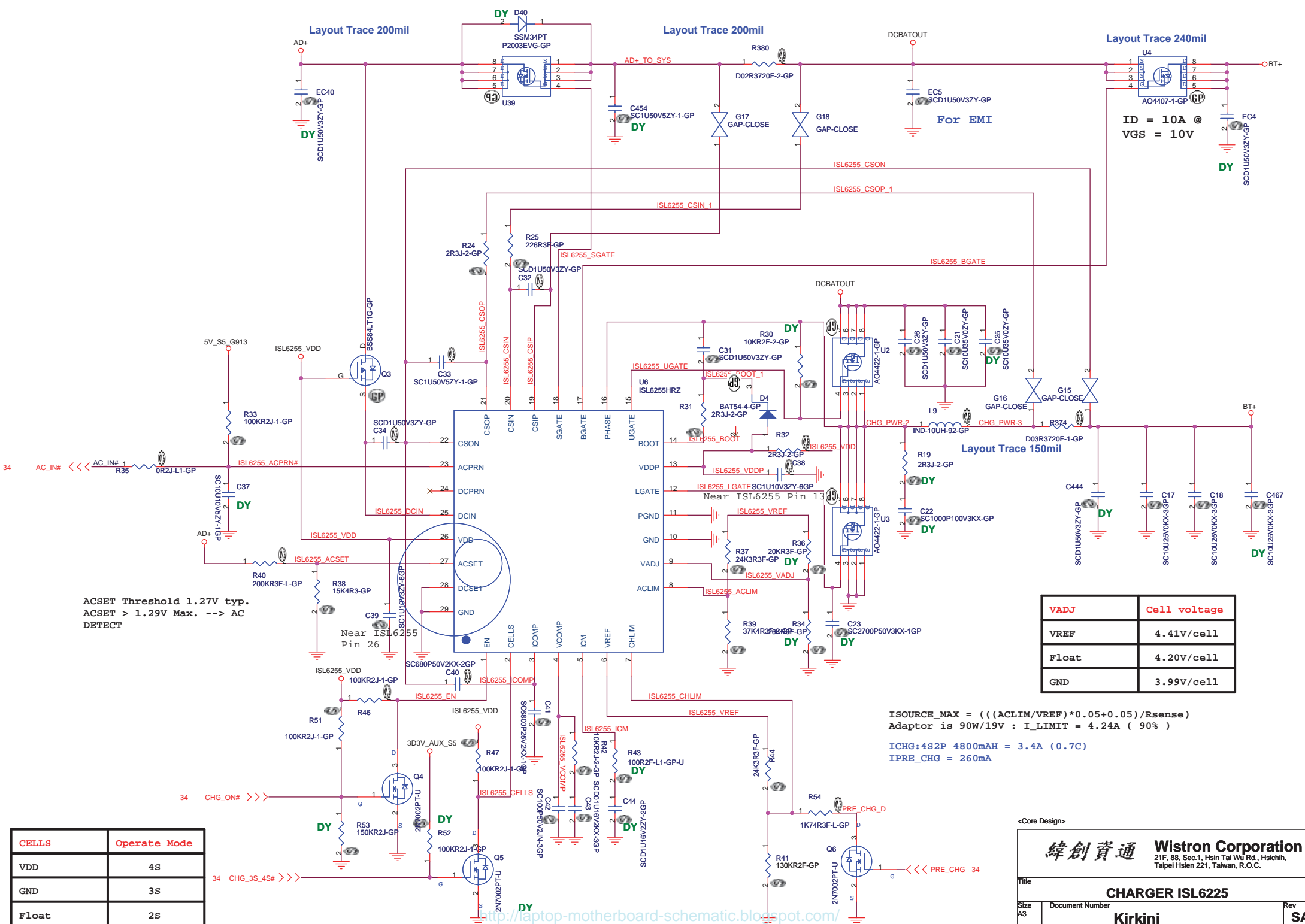
1D5V_S0
Iomax=4.0A



$$V_o = 0.8 * (1 + (R1/R2))$$

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title 1.5V_APL5912 / 0.9V_TPS51100		
Size A3	Document Number Kirkini	Rev SA
Date: Monday, February 20, 2006	Sheet 46 of	56



ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. --> AC
 DETECT

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
 Adaptor is 90W/19V : I_LIMIT = 4.24A (90%)
 ICHG:4S2P 480mAH = 3.4A (0.7C)
 IPRE_CHG = 260mA

<Core Design>

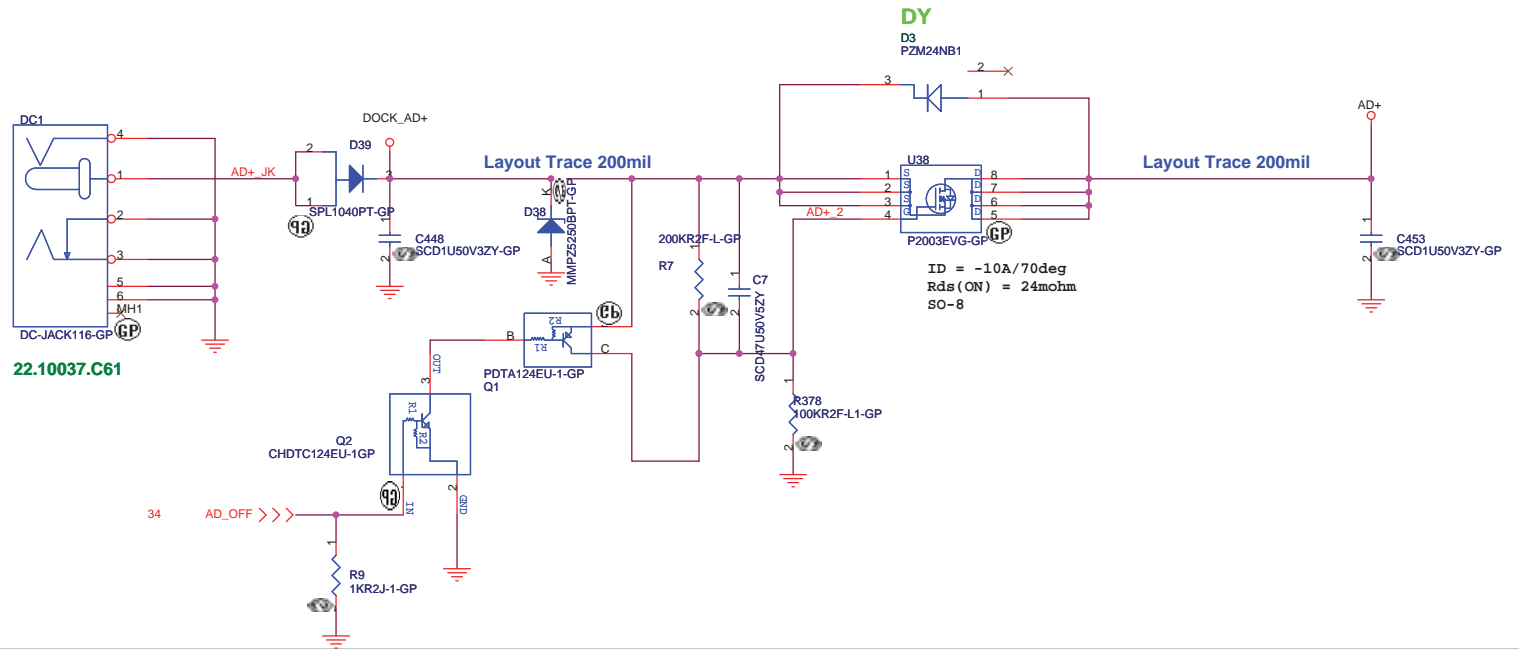
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER ISL6225**

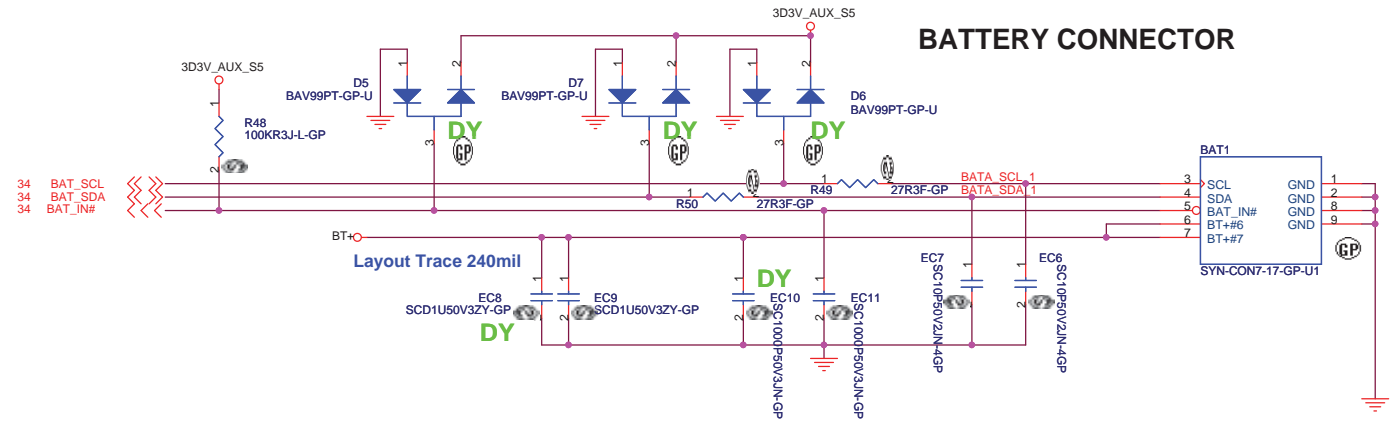
Size A3	Document Number	Rev SA
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Date: Monday, February 20, 2006 Sheet 47 of 56

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



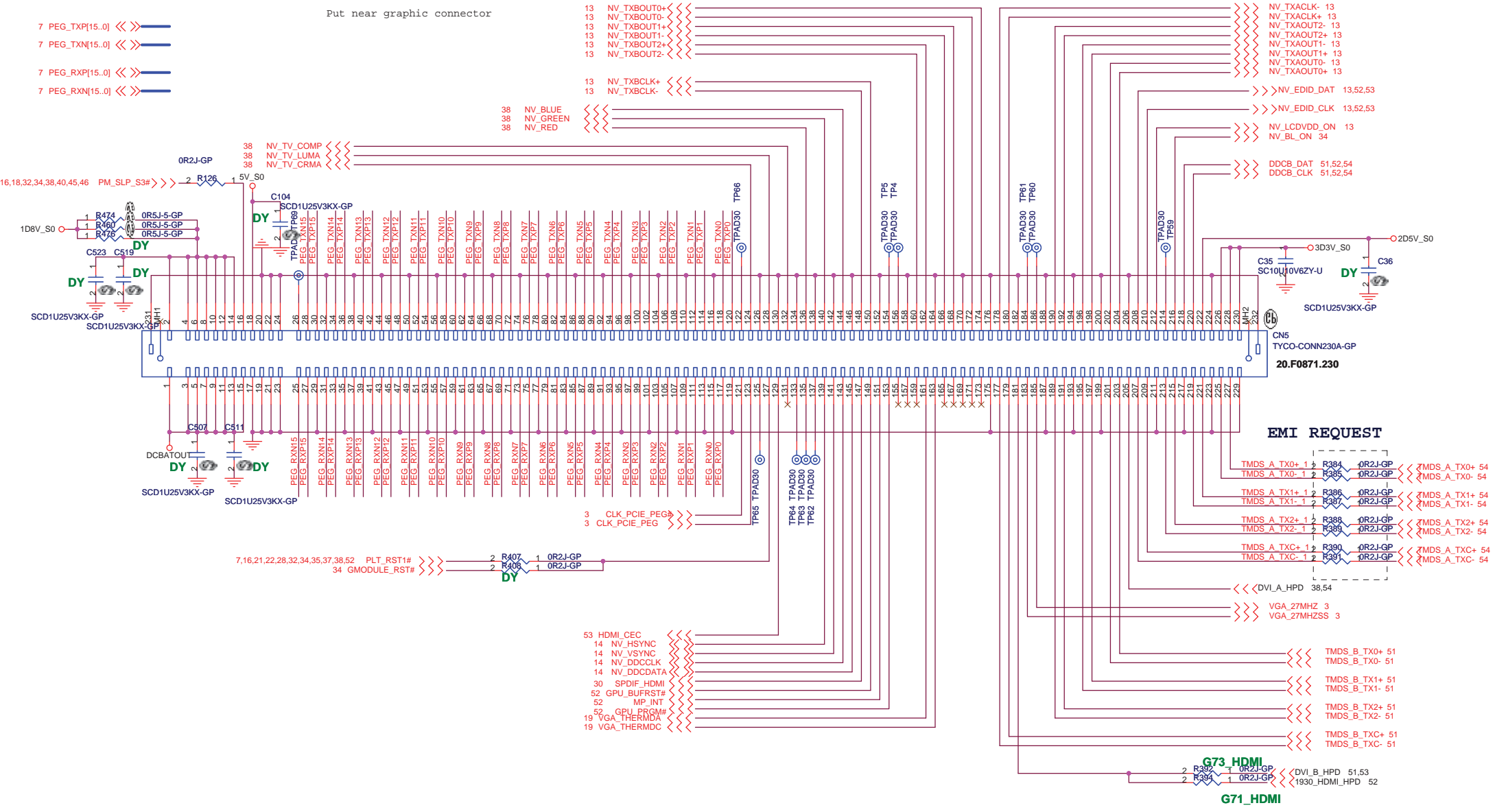
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size: A3	Document Number: Kirkini	Rev: SA
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NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS



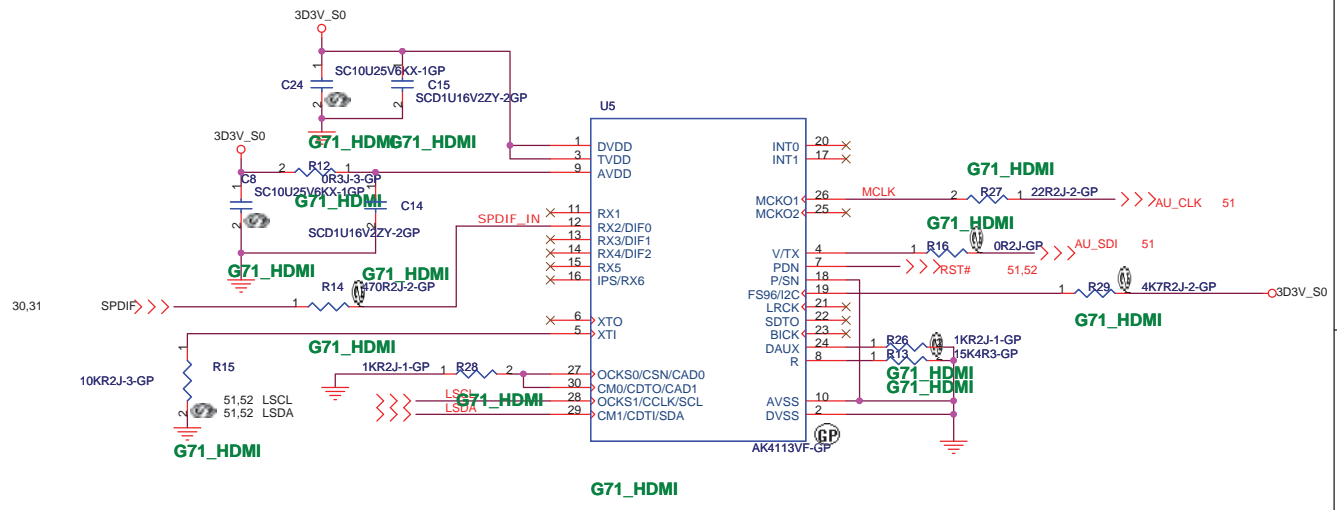
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

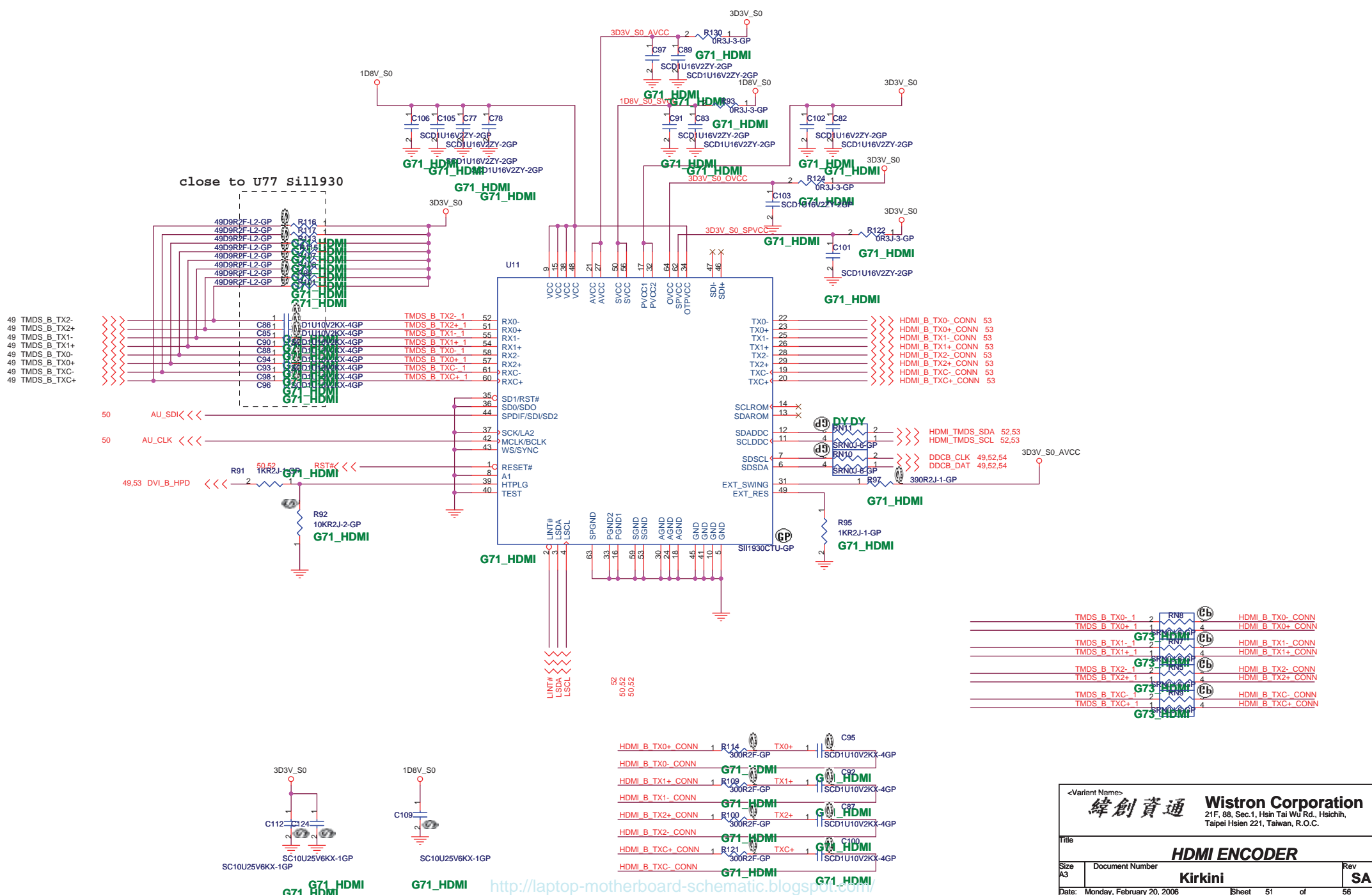
Title _____

KBC ENE

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Kirkini		
Date: Monday, February 20, 2006	Sheet 49 of	56



<Variant Names> 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
HDMI AUDIO CODEC		
Title Size A3 Date: Monday, February 20, 2006	Document Number Kirkini Sheet 50 of 56	Rev SA



close to U77 Sill1930

- 49 TMDS_B_TX2-
- 49 TMDS_B_TX2+
- 49 TMDS_B_TX1-
- 49 TMDS_B_TX1+
- 49 TMDS_B_TX0-
- 49 TMDS_B_TX0+
- 49 TMDS_B_TXC-
- 49 TMDS_B_TXC+

- C86 1 SCD1U10V2KX-4GP
- C85 1 SCD1U10V2KX-4GP
- C90 1 SCD1U10V2KX-4GP
- C88 1 SCD1U10V2KX-4GP
- C94 1 SCD1U10V2KX-4GP
- C93 1 SCD1U10V2KX-4GP
- C98 1 SCD1U10V2KX-4GP
- C96 1 SCD1U10V2KX-4GP

- TMDS B TX2- 1 52
- TMDS B TX2+ 1 51
- TMDS B TX1- 1 55
- TMDS B TX1+ 1 54
- TMDS B TX0- 1 58
- TMDS B TX0+ 1 57
- TMDS B TXC- 1 61
- TMDS B TXC+ 1 60

- 9 VCC
- 15 VCC
- 38 VCC
- 48 VCC
- 21 AVCC
- 27 AVCC
- 50 SVCC
- 56 SVCC
- 32 PVCC1
- 64 OVCC
- 62 SPVCC
- 38 OTPVCC
- 47 SDI+
- 46 SDI+

- 22 TX0-
- 23 TX0+
- 25 TX1-
- 26 TX1+
- 28 TX2-
- 29 TX2+
- 19 TXC-
- 20 TXC+

- HDMI_B_TX0- CONN 53
- HDMI_B_TX0+ CONN 53
- HDMI_B_TX1- CONN 53
- HDMI_B_TX1+ CONN 53
- HDMI_B_TX2- CONN 53
- HDMI_B_TX2+ CONN 53
- HDMI_B_TXC- CONN 53
- HDMI_B_TXC+ CONN 53

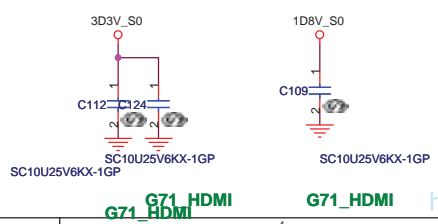
G71_HDMI

G71_HDMI

G71_HDMI

- TMDS B TX0- 1 2 HDMI B TX0- CONN
- TMDS B TX0+ 1 4 HDMI B TX0+ CONN
- TMDS B TX1- 1 2 HDMI B TX1- CONN
- TMDS B TX1+ 1 4 HDMI B TX1+ CONN
- TMDS B TX2- 1 2 HDMI B TX2- CONN
- TMDS B TX2+ 1 4 HDMI B TX2+ CONN
- TMDS B TXC- 1 2 HDMI B TXC- CONN
- TMDS B TXC+ 1 4 HDMI B TXC+ CONN

- HDMI_B_TX0+ CONN 1 R114 TX0+ 1 SCD1U10V2KX-4GP
- HDMI_B_TX0- CONN 1 G71_HDMI TX0+ 1 G71_HDMI
- HDMI_B_TX1+ CONN 1 R109 TX1+ 1 SCD1U10V2KX-4GP
- HDMI_B_TX1- CONN 1 G71_HDMI TX1+ 1 G71_HDMI
- HDMI_B_TX2+ CONN 1 R100 TX2+ 1 SCD1U10V2KX-4GP
- HDMI_B_TX2- CONN 1 G71_HDMI TX2+ 1 G71_HDMI
- HDMI_B_TXC+ CONN 1 R121 TXC+ 1 SCD1U10V2KX-4GP
- HDMI_B_TXC- CONN 1 G71_HDMI TXC+ 1 G71_HDMI

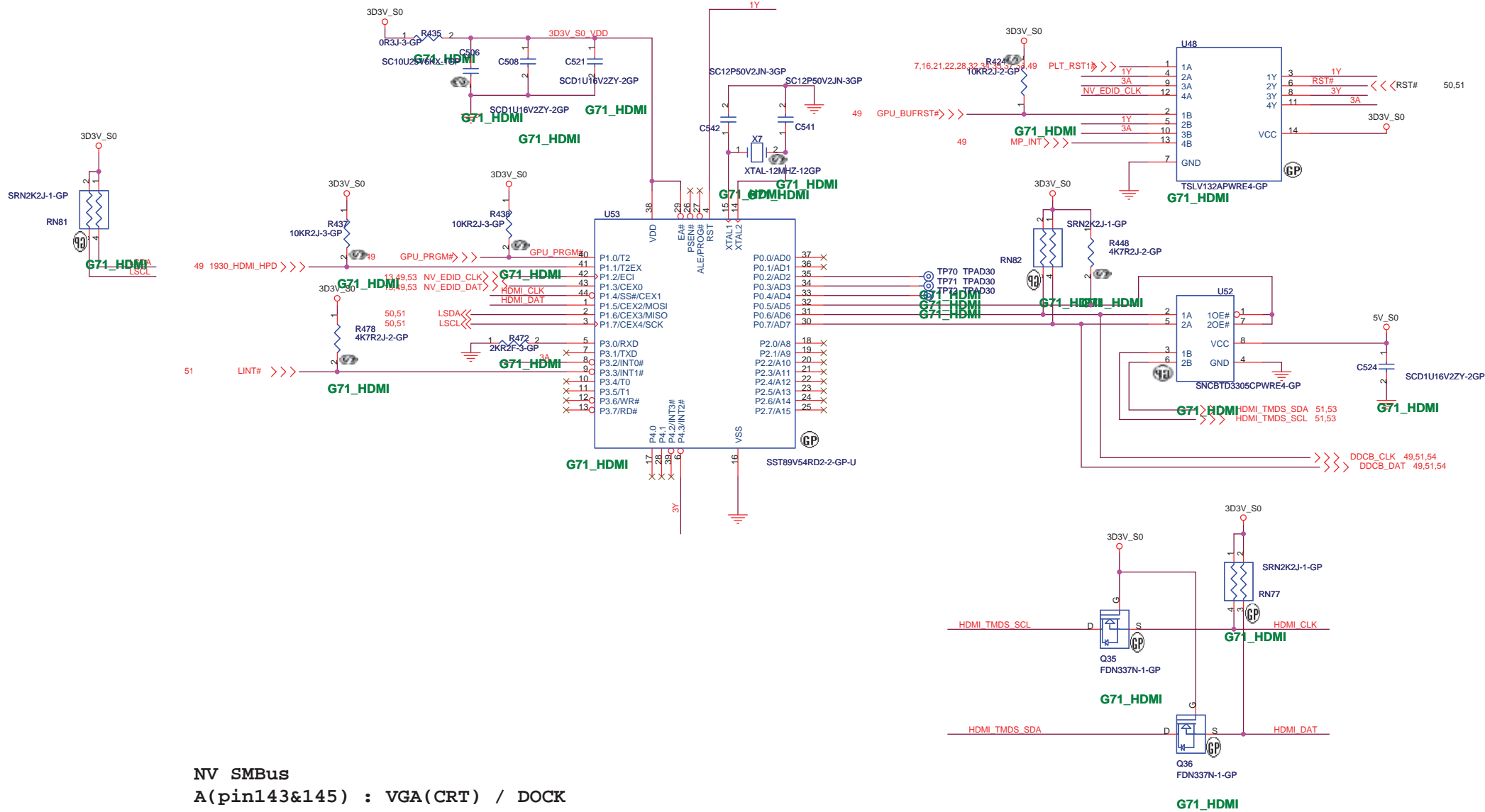


<Variant Names>
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **HDMI ENCODER**

Size A3 Document Number **Kirkini** Rev **SA**

Date: Monday, February 20, 2006 Sheet 51 of 56

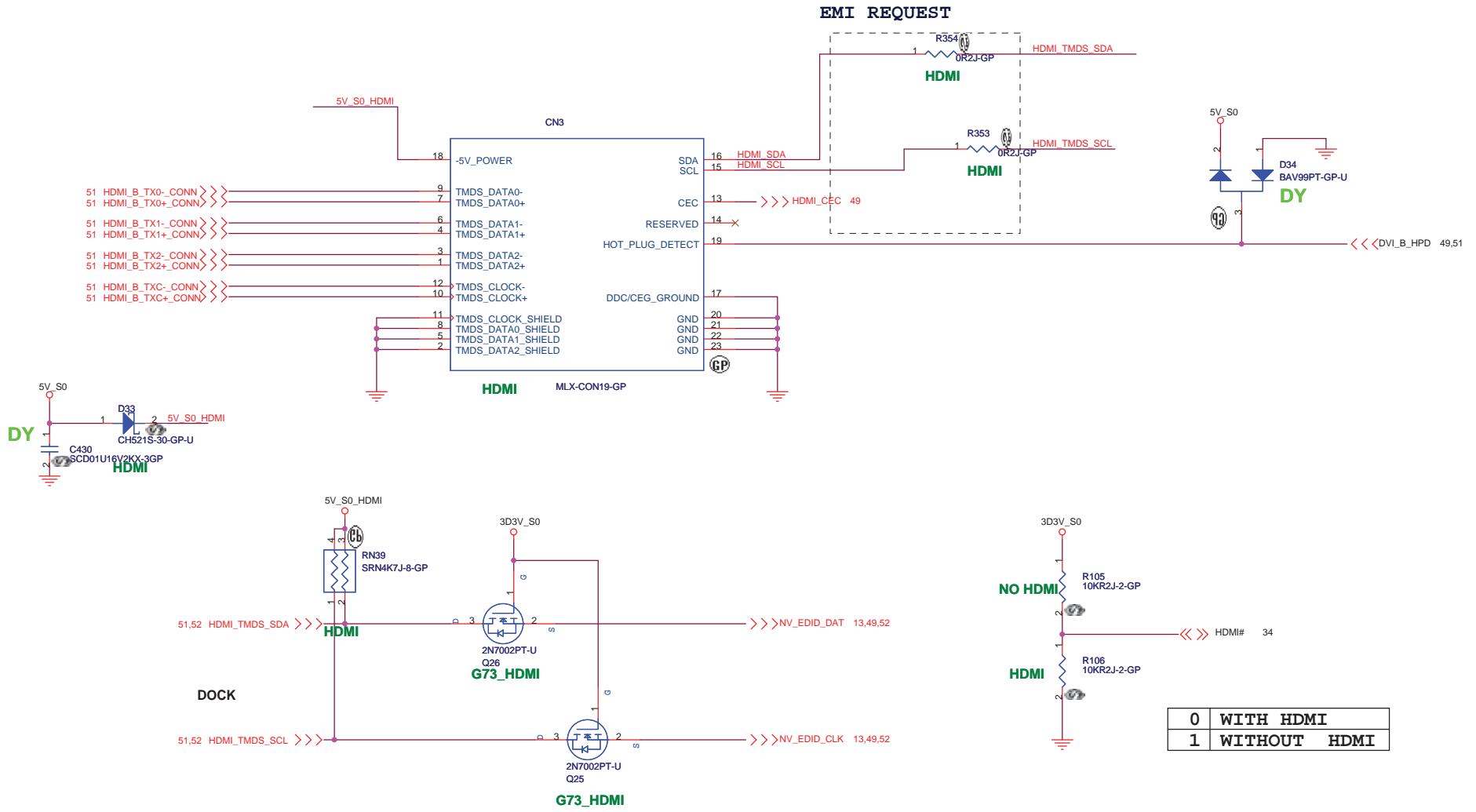


NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS

<Variant Names>
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MICRO CONTROLLER**

Size A3	Document Number	Rev SA
Date: Monday, February 20, 2006	Kirkini	Sheet 52 of 56

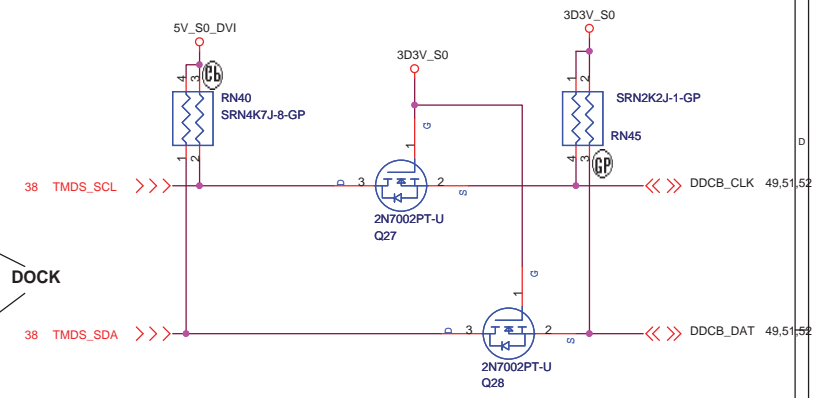
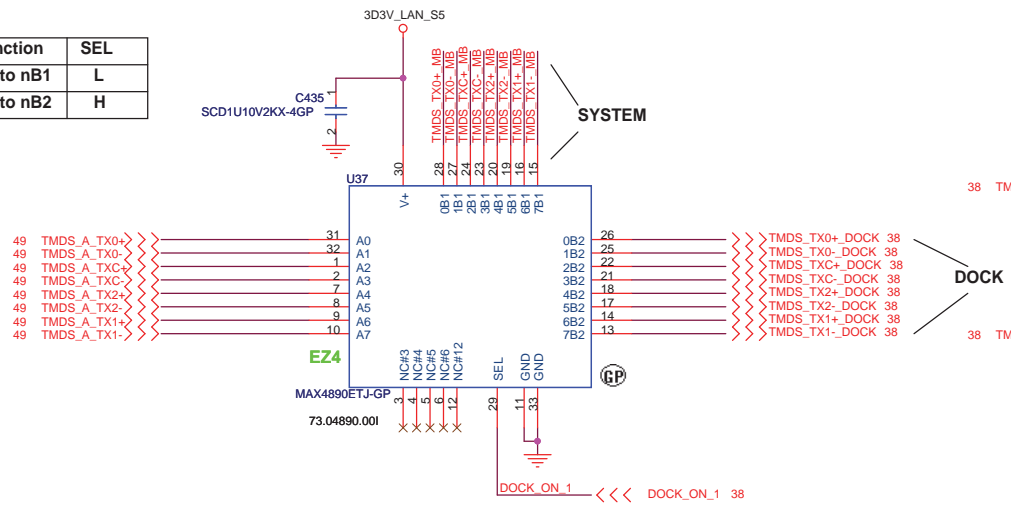
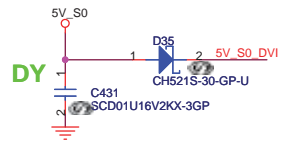


0	WITH HDMI
1	WITHOUT HDMI

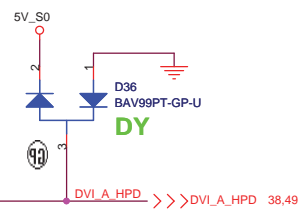
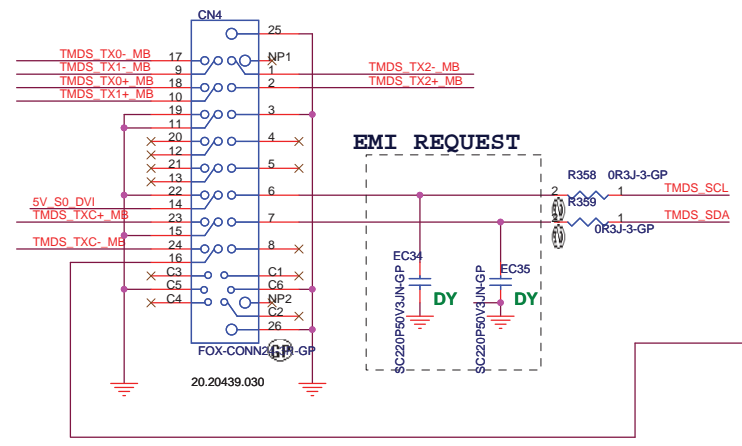
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
HDMI CONNECTOR		
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Function	SEL
An to nB1	L
An to nB2	H



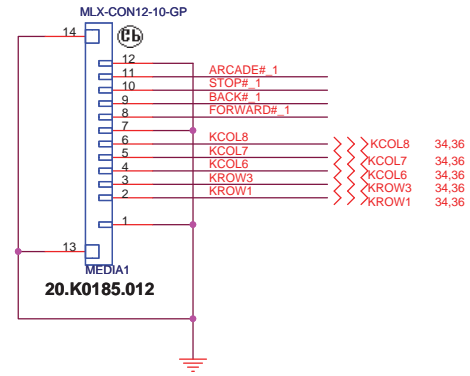
TMDS A TX0+	1	R362	2	OR2J-L1-GP	TMDS TX0+ MB
TMDS A TX0-	1	R366	2	OR2J-L1-GP	TMDS TX0- MB
TMDS A TXC+	1	R372	2	OR2J-L1-GP	TMDS TXC+ MB
TMDS A TXC-	1	R376	2	OR2J-L1-GP	TMDS TXC- MB
TMDS A TX2+	1	R382	2	OR2J-L1-GP	TMDS TX2+ MB
TMDS A TX2-	1	R386	2	OR2J-L1-GP	TMDS TX2- MB
TMDS A TX1+	1	R392	2	OR2J-L1-GP	TMDS TX1+ MB
TMDS A TX1-	1	R396	2	OR2J-L1-GP	TMDS TX1- MB



<Variant Name>


Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

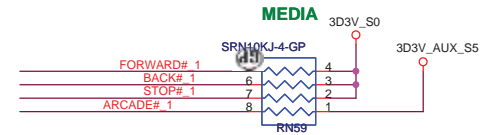
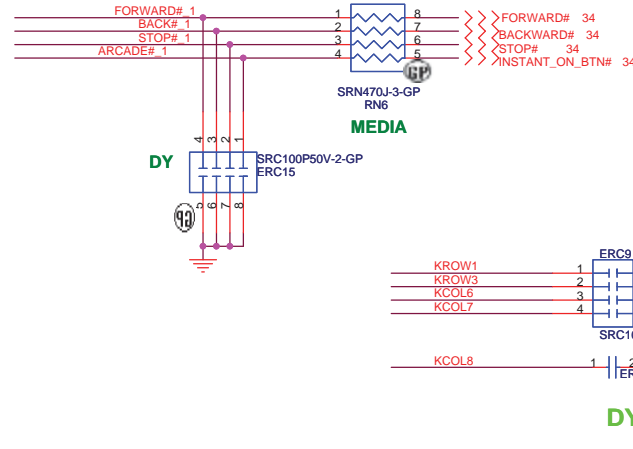
Title			Rev
DVI CONNECTOR			
Size	Document Number	SA	
A3	Kirkini		
Date:	Monday, February 20, 2006	Sheet	54 of 56



- Pin12:GND
- Pin11:ARCADE#_1
- Pin10:STOP#_1
- Pin9:BACK#_1
- Pin8:FORWARD#_1
- Pin7:GND
- Pin6:KCOL8
- Pin5:KCOL7
- Pin4:KCOL6
- Pin3:KROW3
- Pin2:KROW1
- Pin1:GND



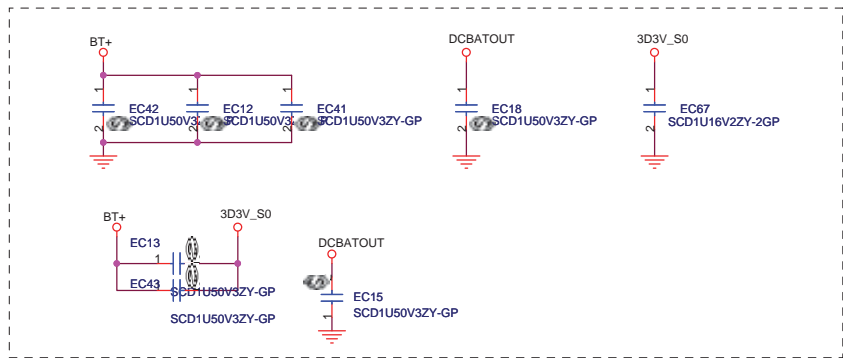
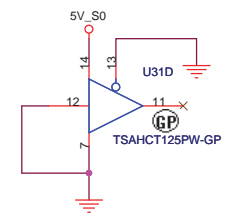
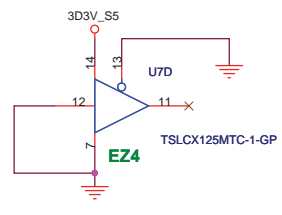
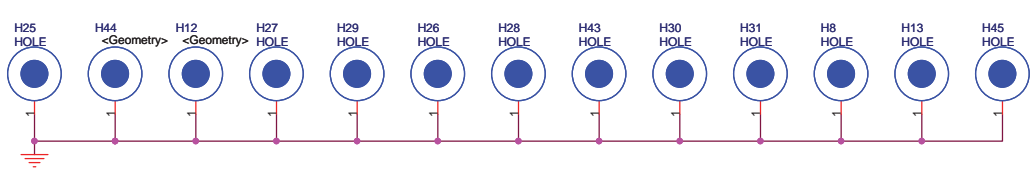
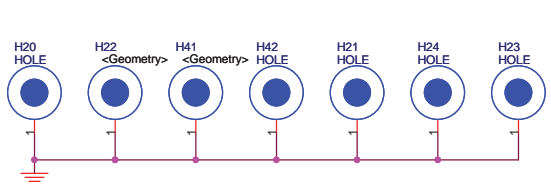
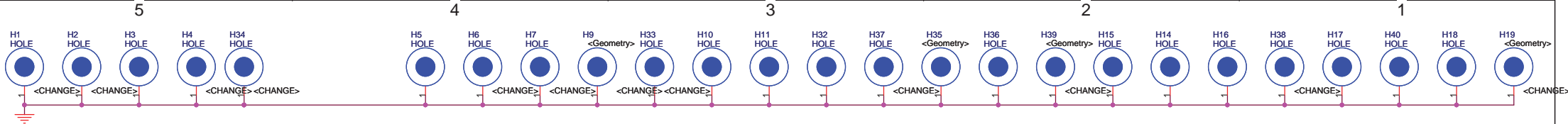
MB
Top view



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