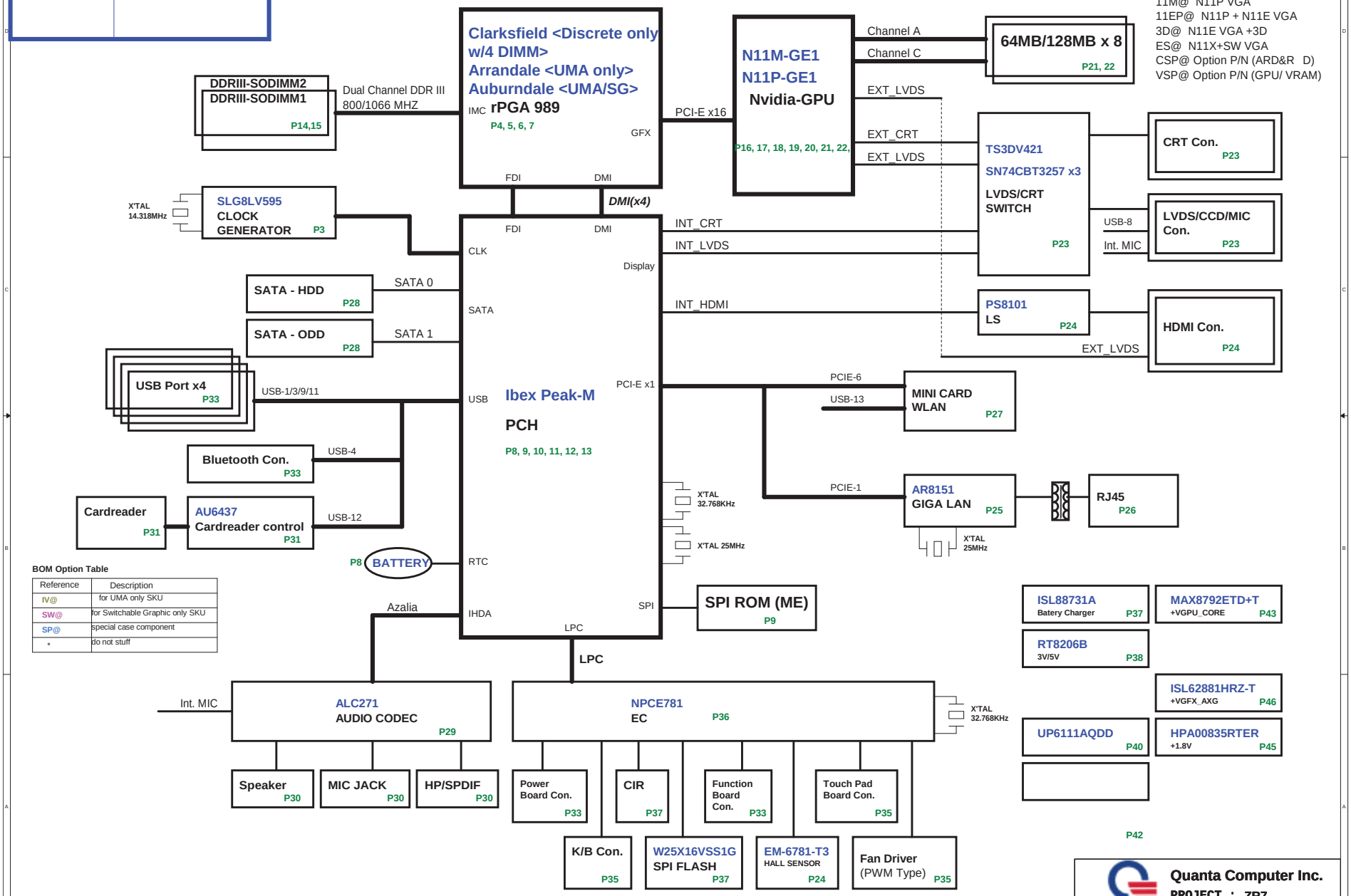
VER : 1A

BOM P/N	Description

ZR7 SYSTEM BLOCK DIAGRAM

BOM MARK

IV@ INT VGA
EV@ DISCRETE
SW@ SW VGA
11P@ N11P VGA
11M@ N11P VGA
11EP@ N11P + N11E VGA
3D@ N11E VGA +3D
ES@ N11X+SW VGA
CSP@ Option P/N (ARD&R D)
VSP@ Option P/N (GPU/ VRAM)



BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU
SP@	special case component
*	do not stuff

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Size	Document Number	Rev
	Block Diagram	3B

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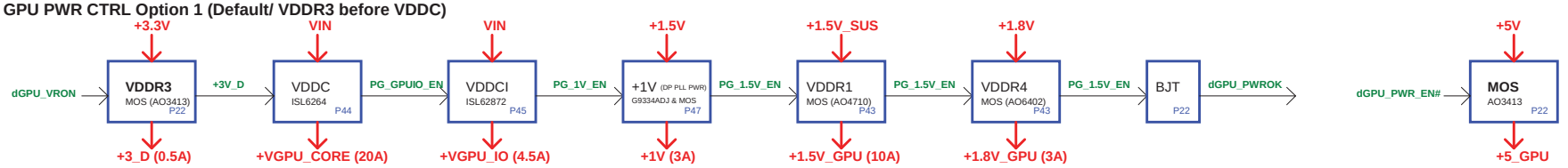
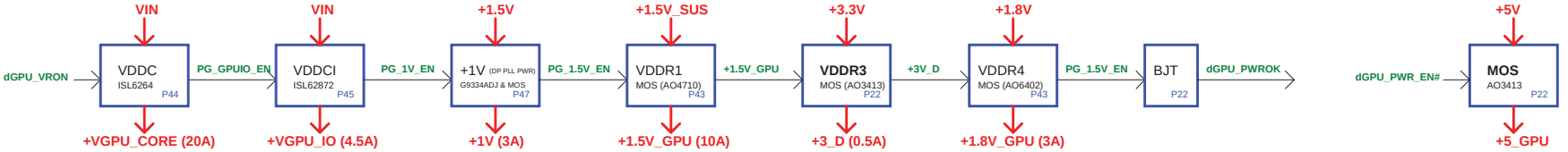
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



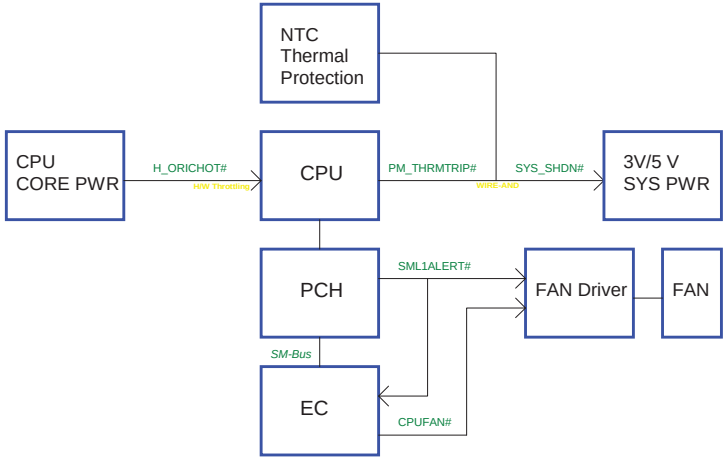
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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PROJECT : ZR7

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	3B

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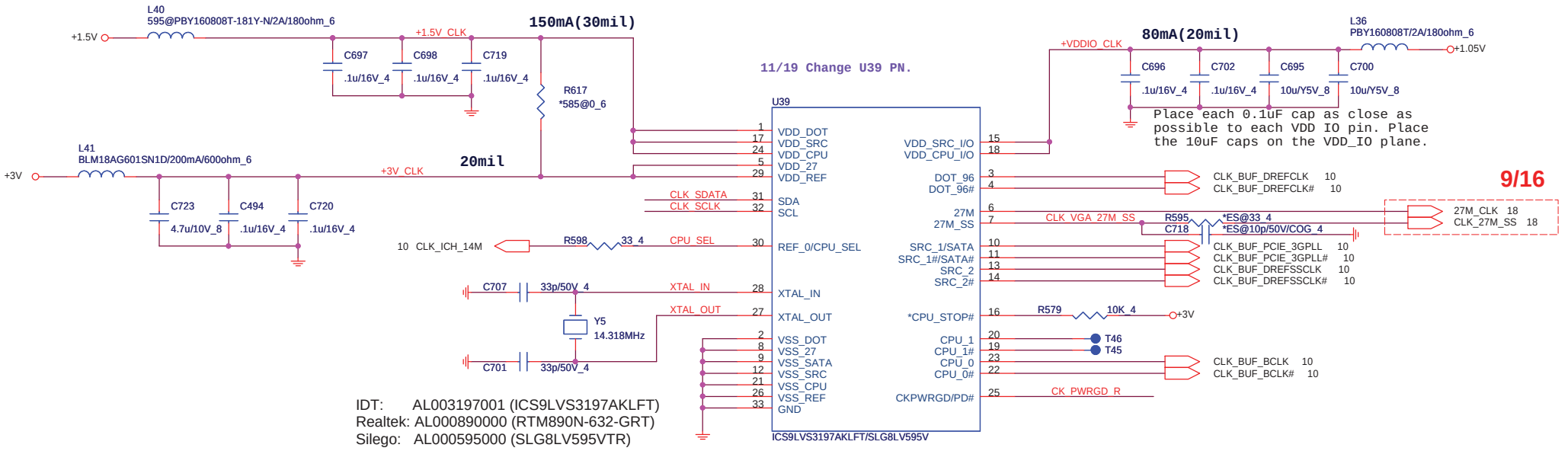
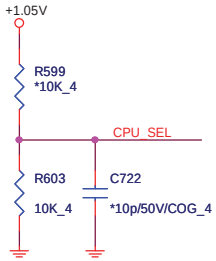
CLK GEN.



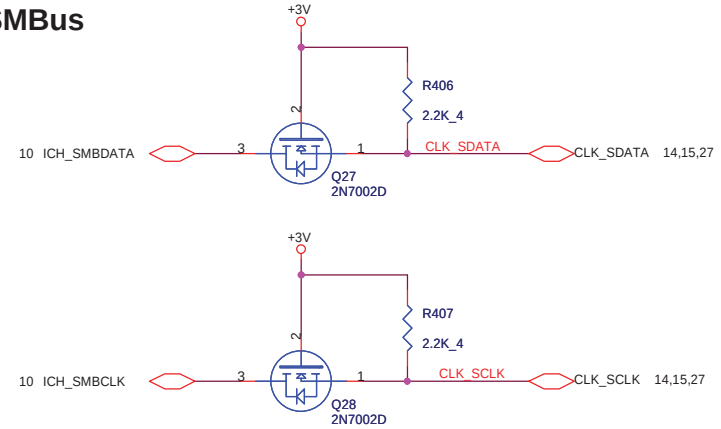
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

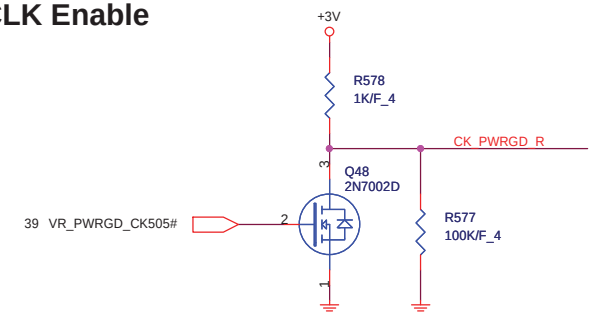


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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PROJECT : ZR7

Size	Document Number	Rev
	Clock Generator	3B
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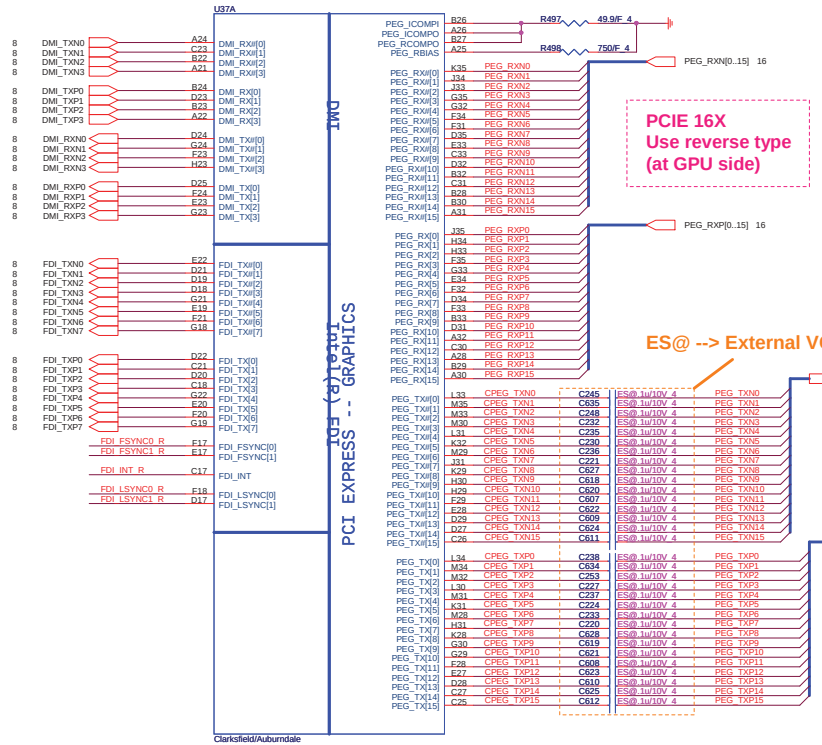
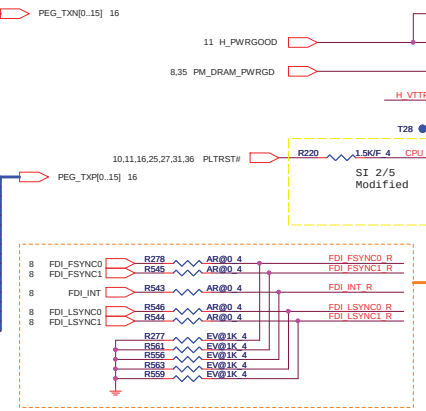
AR@ --> ARD CPU
CF@ --> CFD CPU
ES@ --> External VGA SKU

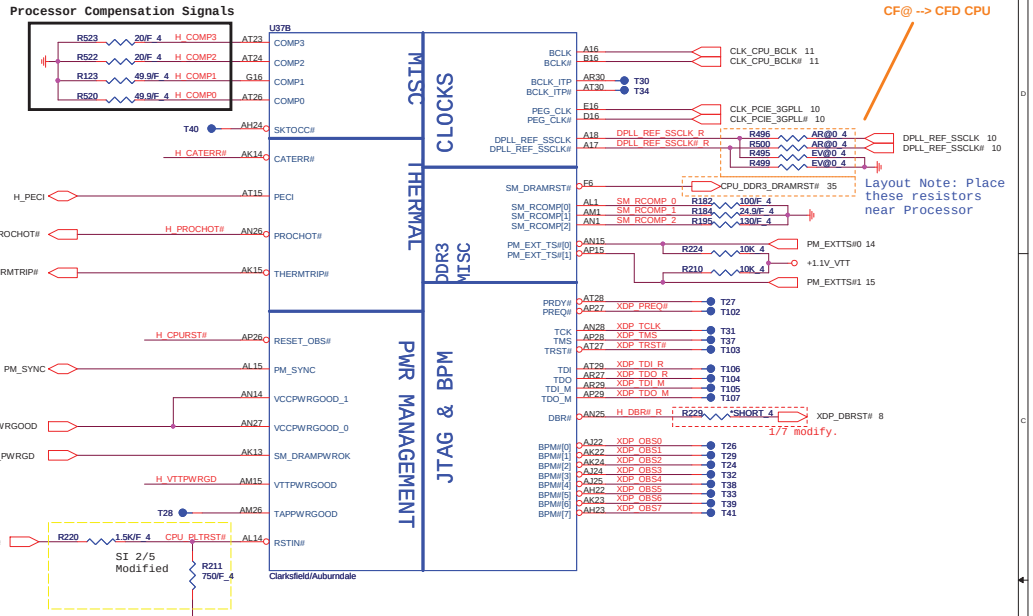
ARRANDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



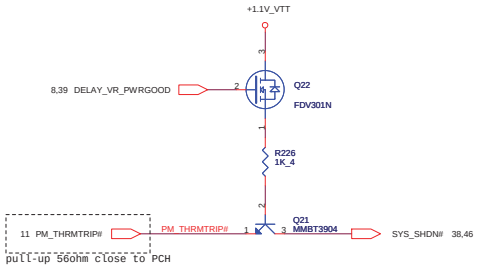
PCIE 16X
Use reverse type
(at GPU side)



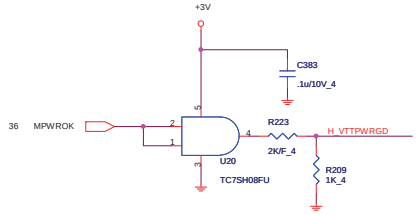
ARRANDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



Thermaltrip protect

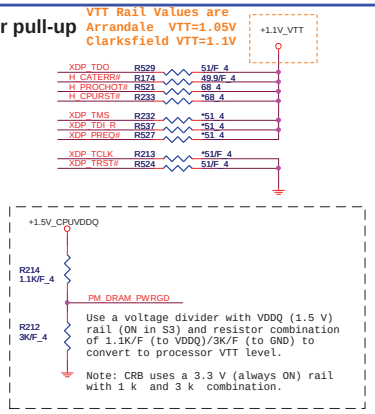


VTT PWR_Good



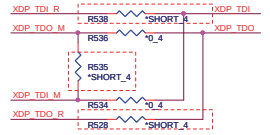
Processor pull-up

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V



JTAG MAPPING

2/4 modify.



Scan Chain (Default)	STUFF -> R535, R538, R528 NO STUFF -> R536, R534
CPU Only	STUFF -> R538, R536 NO STUFF -> R535, R534, R528
GMCH Only	STUFF -> R534, R528 NO STUFF -> R535, R536, R538

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	ARRANDALE/CLARKSFIELD 1/4	3B

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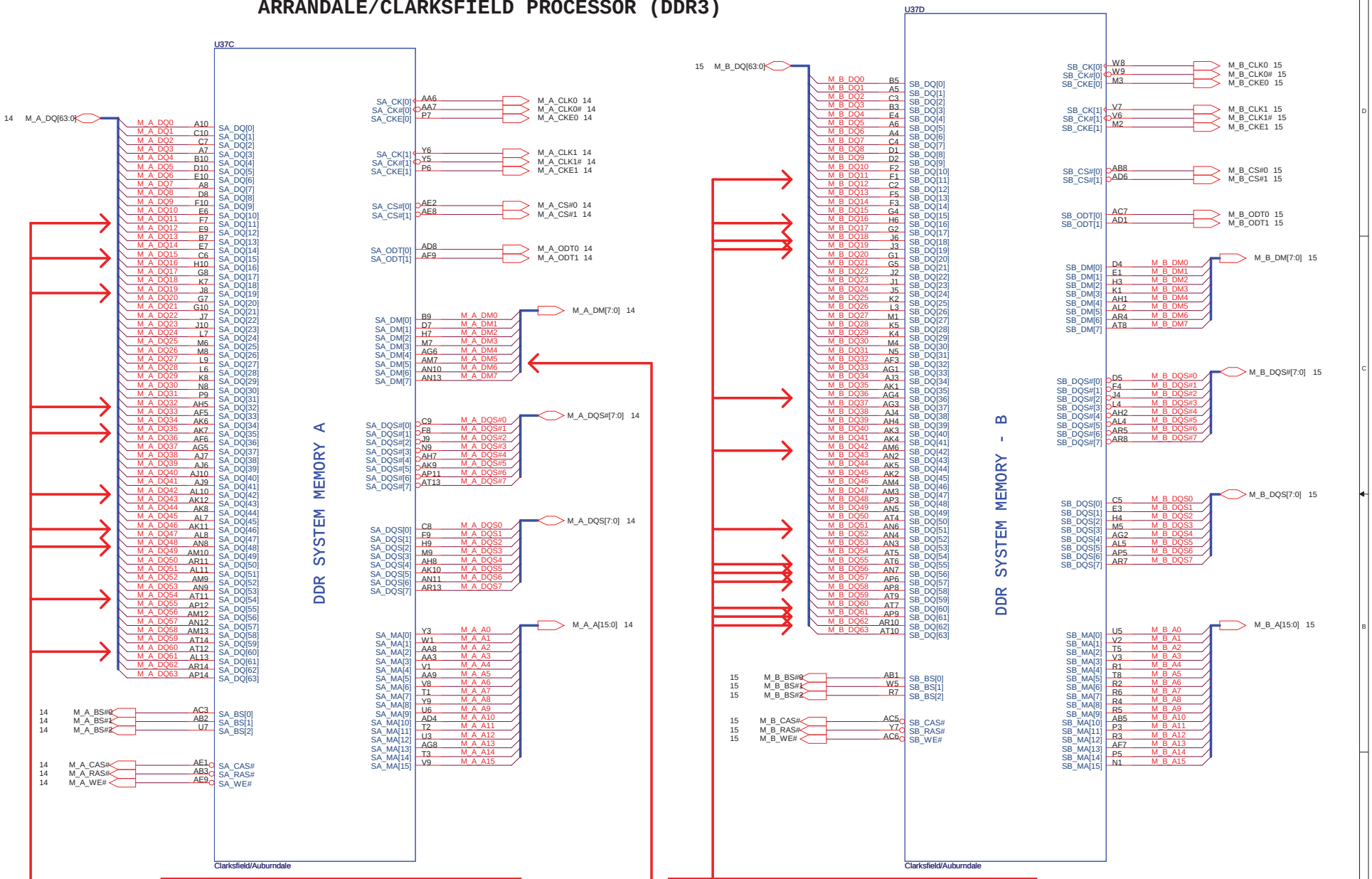
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



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Size	Document Number		Rev
	ARRANDALE/CLARKSFIELD 2/4		3B
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AR@ --> ARD CPU
CF@ --> CFD CPU

ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

ARRANDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

ARD:48A
CFD:52A

+VCC_CORE

U37F

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V

+1.1V_VTT 18A

1.1V RAIL POWER

CPU CORE SUPPLY

1/7 modify.
(15mils)

POWER

CPU VIDS

SENSE LINES

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

Clarksfield/Auburndale

AR@ --> ARD CPU
CF@ --> CFD CPU

22A

+VGFX_AXG

U37G

Add it for discrete only

GRAPHICS POWER

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

ARD:3A
CFD:6A

CF@ --> CFD CPU

+1.5V_CPUVDDQ

FDI

PEG & DMI

1.1V

1.8V

0.6A

+1.8V

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V

Clarksfield/Auburndale

Note:
For Validating IMVP VR R6451 should be STUFF
and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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PROJECT : ZR7

Size	Document Number	Rev
	ARRANDALE/CLARKSFIELD 3/4 (PWR)	3B

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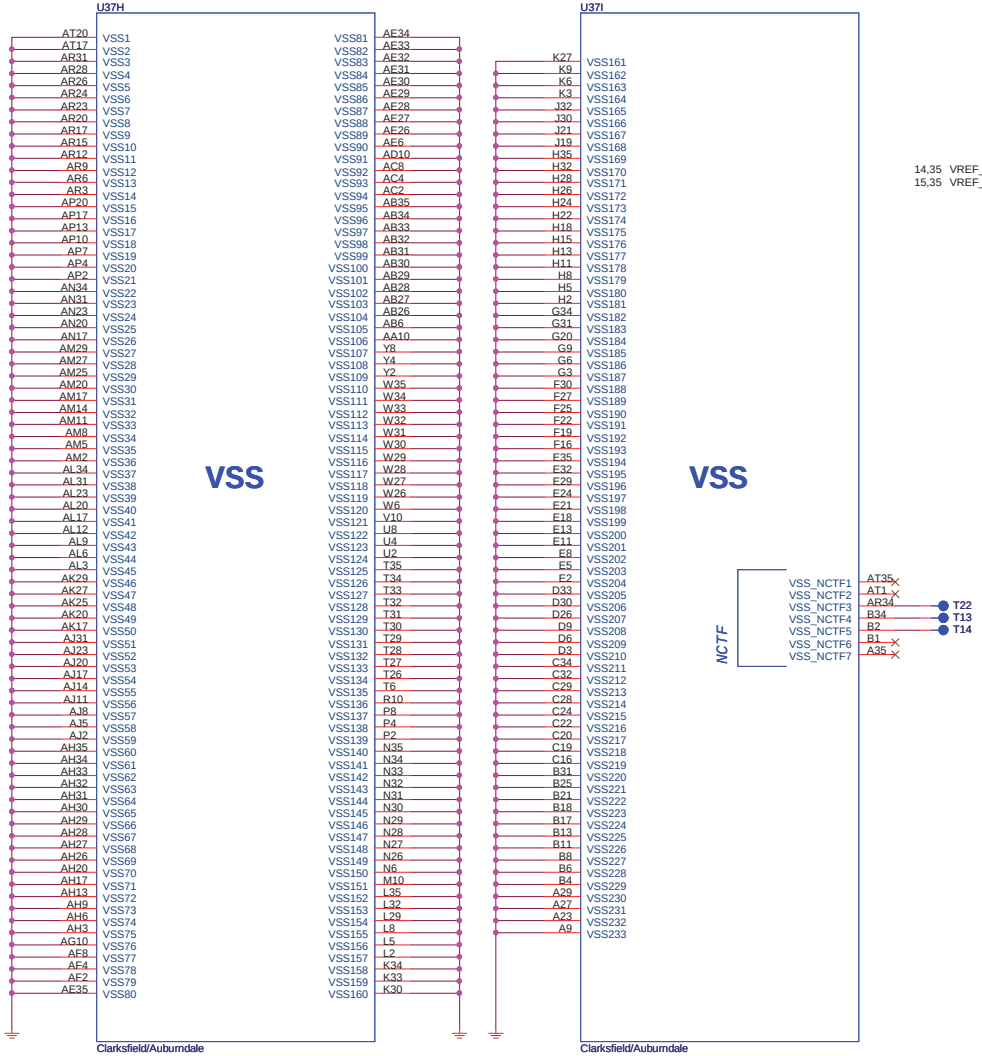
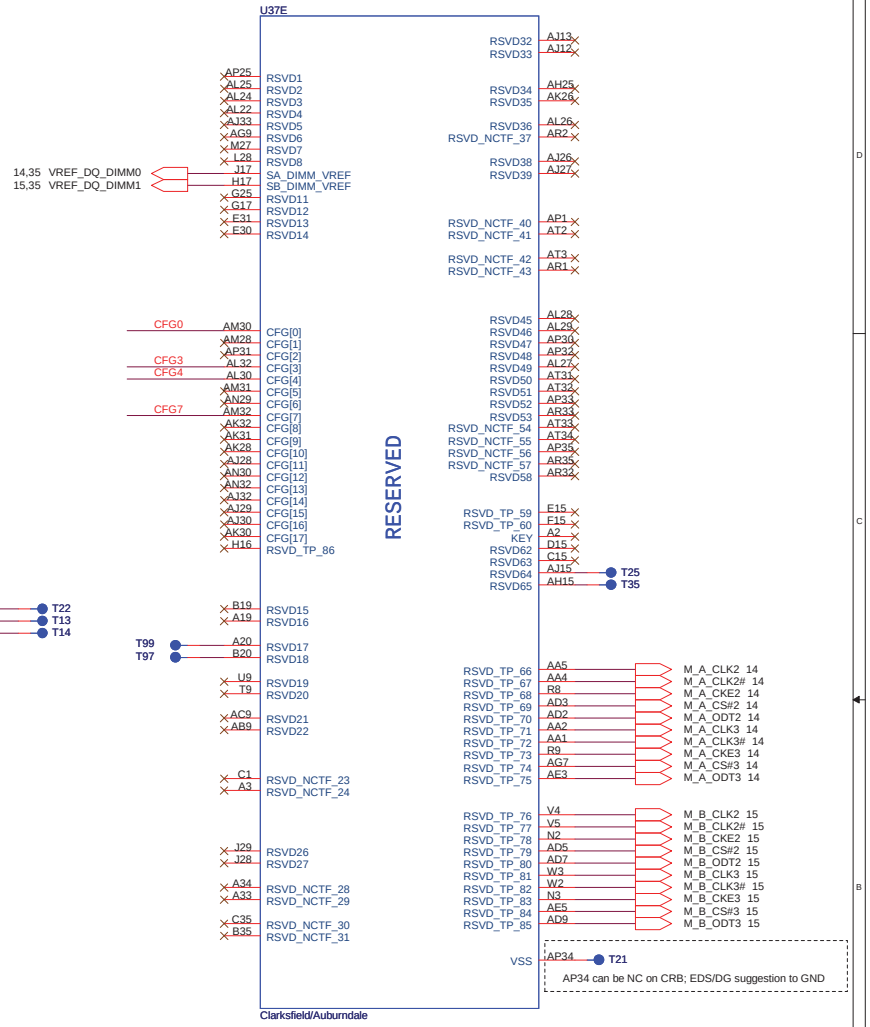
ARRANDALE/CLARKSFIELD PROCESSOR (GND)



ARRANDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

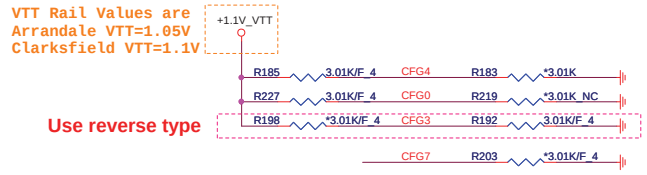


Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications.
Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA
components. This pull down resistor should be removed when this issue is fixed.

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V



Use reverse type

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PROJECT : ZR7

Size	Document Number	Rev
	ARRANDALE/CLARKSFIELD 4/4	3B

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AR@ --> ARD CPU
CF@ --> CFD CPU
IV@ --> iGPU only

IBEX PEAK-M (DMI,FDI,GPIO)

AR@ --> ARD CPU
CF@ --> CFD CPU

Arrandale only

U40C

DMI

FDI

System Power Management

10/20 Modify Unstuff

ibexPeak-M_R1P0

IBEX PEAK-M (LVDS,DDI)

AR@ --> ARD CPU

U40D

LVDS

Digital Display Interface

CRT

IV@ --> iGPU only

AR@ --> ARD CPU

R place close to PCH

ibexPeak-M_R1P0

PCH Pull-high/low

AR@ --> ARD CPU

System PWR_OK

DELAY_VR_PWRGOOD need PU 2K to +3V.
PU at power side

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PROJECT : ZR7	
Size	Document Number: IBEX PEAK-M 1/6
Rev	3B
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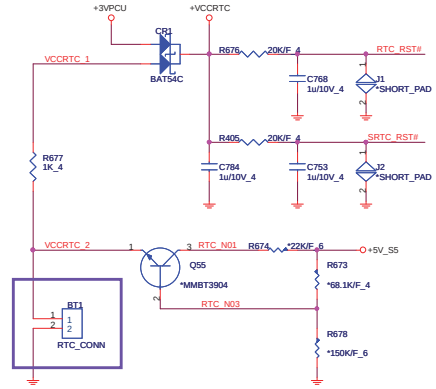
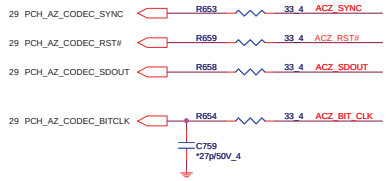
RTC Circuitry



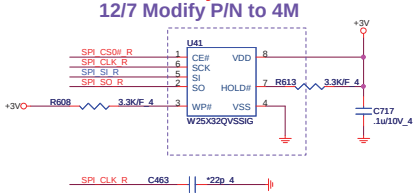
1/7 Change P/N by ME.

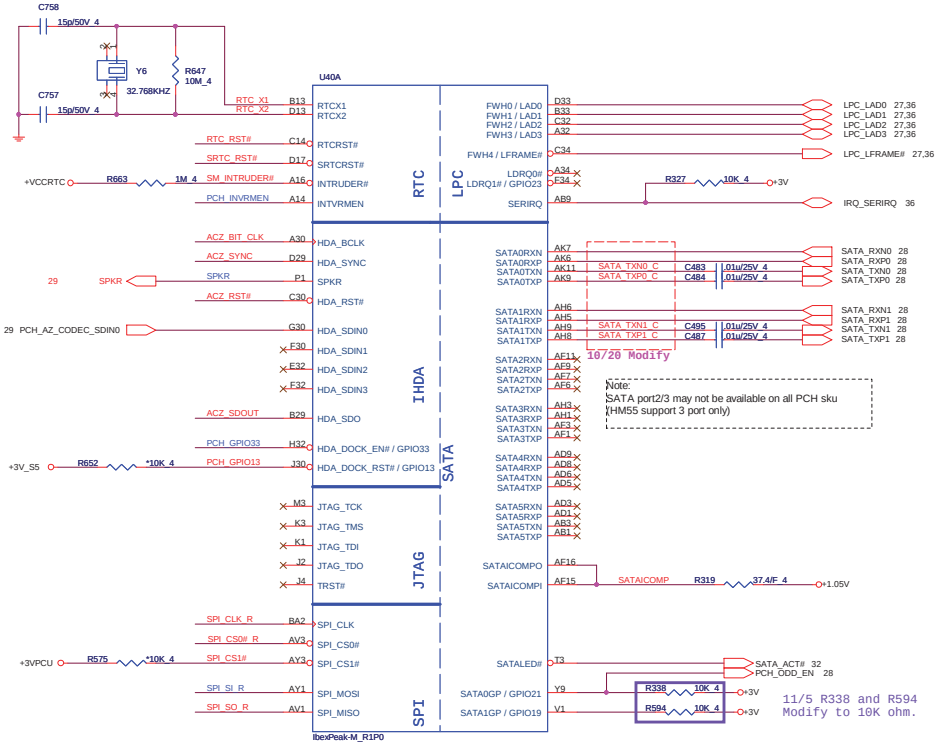
HDA Bus



PCH SPI

10/29 Modify P/N to 2M
12/7 Modify P/N to 4M



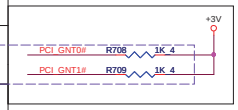


PCH Strap Pin Configuration Table-1

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R685 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R618 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R611 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R370 *1K/F_4 R382 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCI_GNT0# R360 *1K_4 10 PCI_GNT1# R363 *1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10,23 PWM_SELECT# R364 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCI_GNT3# R628 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R296 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R295 *1K/F_4 +1.8V

12/1 Add by SPI ROM



GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 R380 10K_4 +3V_S5 R371 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# R341 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R324 *10K_4

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	IBEX PEAK-M 2/6	3B

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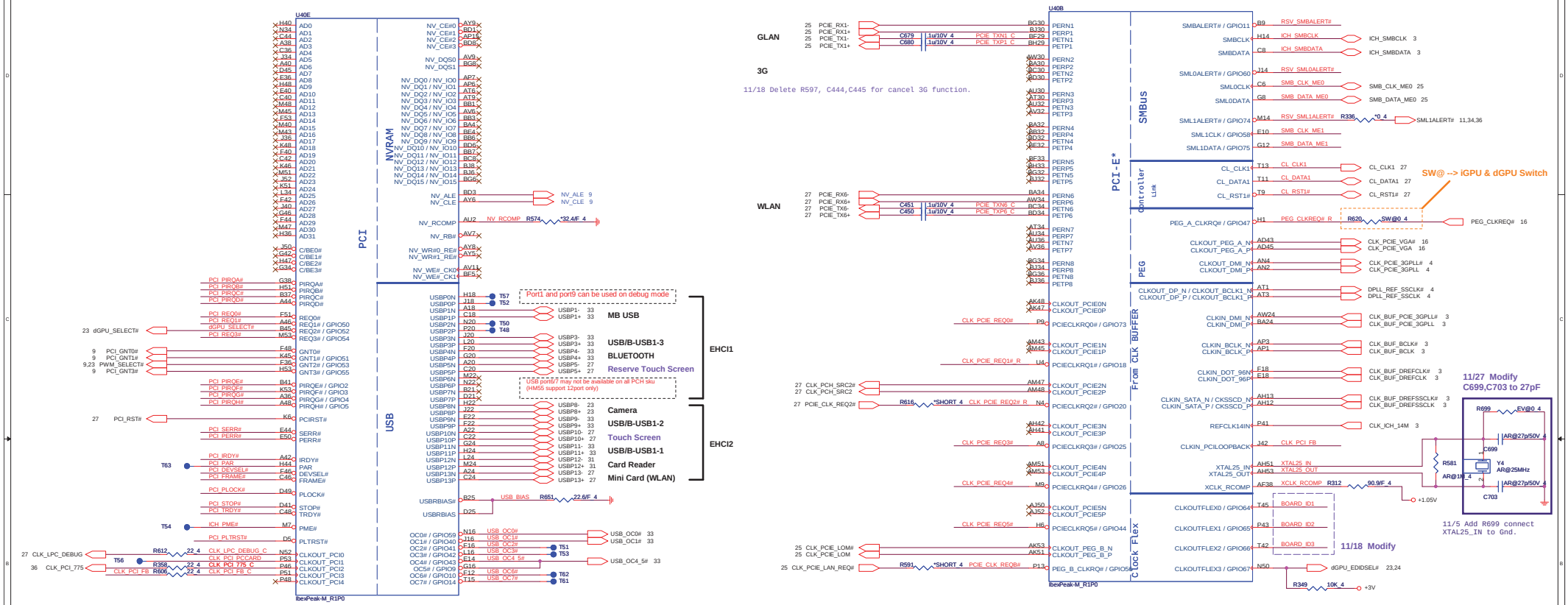
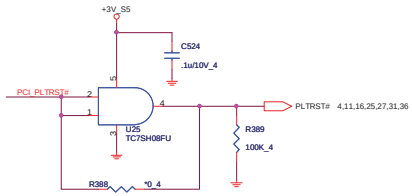
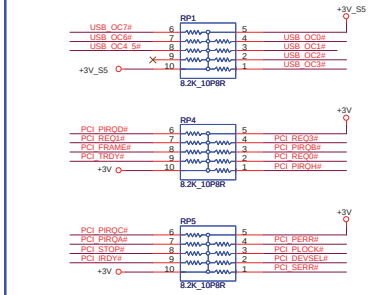
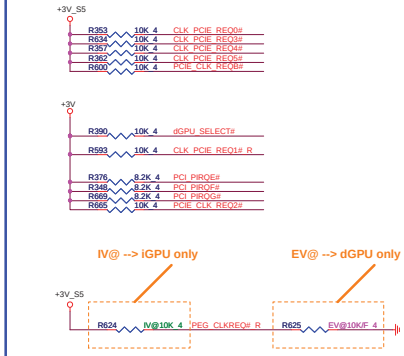
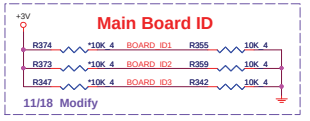
IV@ --> iGPU only
EV@ --> dGPU only
SW@ --> iGPU & dGPU Switch

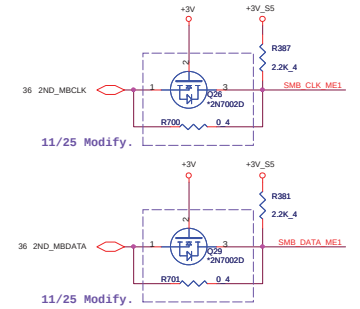










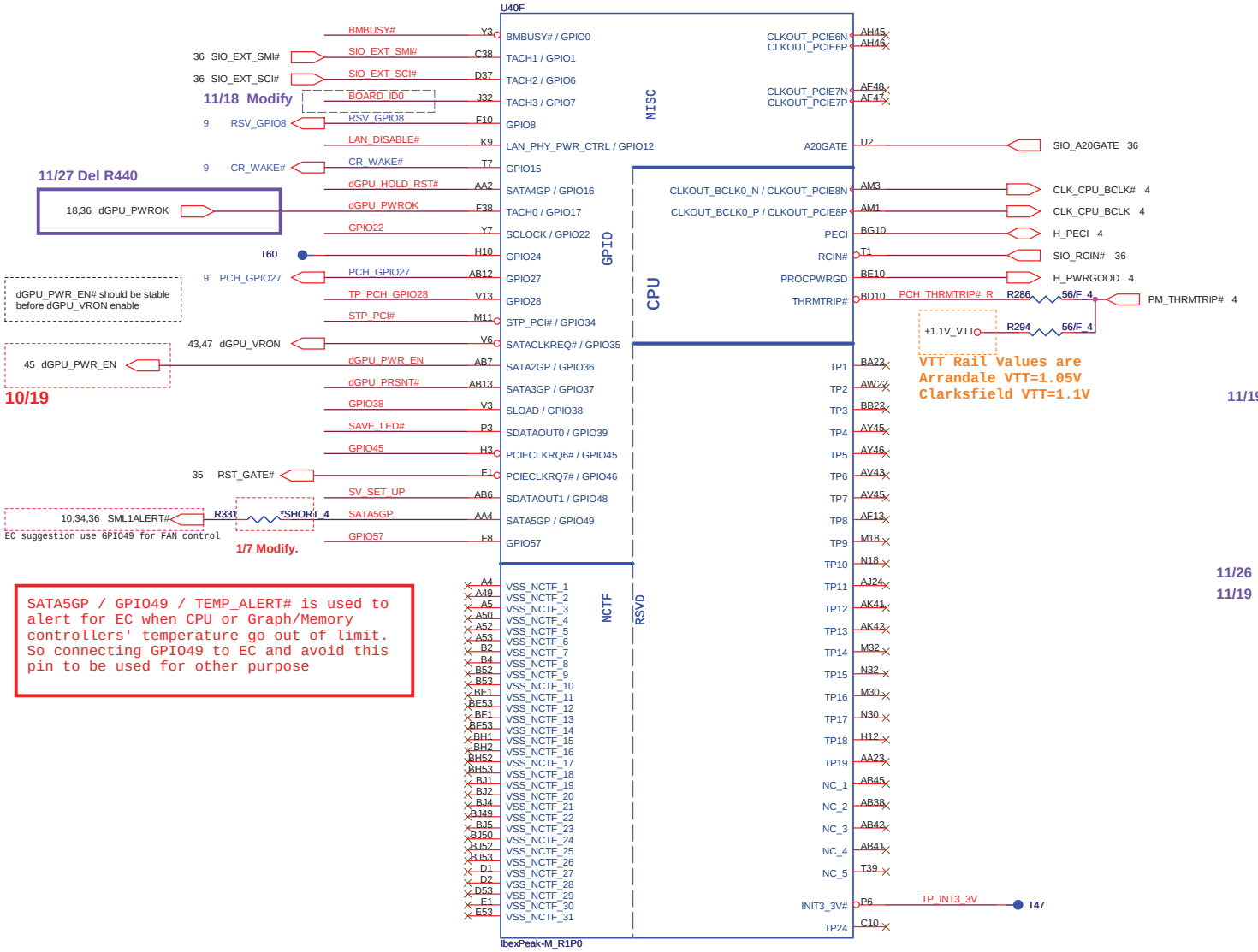


Quanta Computer Inc.
PROJECT : ZR7

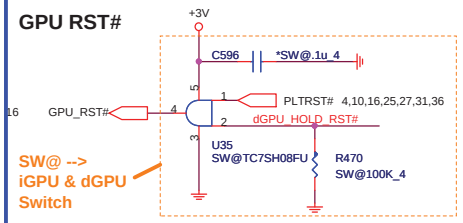
Size	Document Number	Rev
	IBEX PEAK-M 3/6	3B
Date: Monday, February 22, 2010	Sheet 10 of 49	

IV@ --> iGPU only
EV@ --> dGPU only
SW@ --> iGPU & dGPU Switch
ES@ --> External VGA SKU

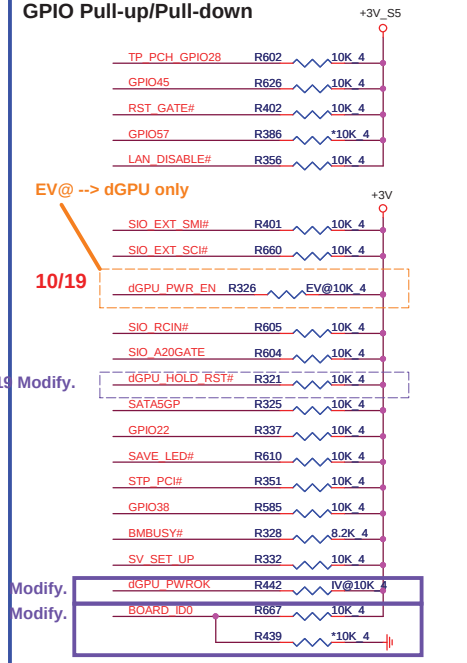
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#

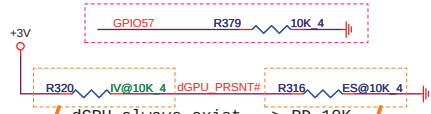


GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1



Integrated Clock Chip Enable	
RSV_GPIO8	High = Disable Low = Enable

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PROJECT : ZR7

Size	Document Number	Rev
	IBEX PEAK-M 4/6	3B
Date: Monday, February 22, 2010	Sheet 11 of 49	

IBEX PEAK-M (POWER)

AR@ --> ARD CPU
CF@ --> CFD CPU

VCCCORE(+1.05V) = 1.432A(80mils)

40mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VCCADAC= 69mA(15mils)

VCCALVDS= 1mA

VCCTX_LVDS= 59mA(15mils)

VCC3_3 = 357mA(30mils)

VCCVRM= 196mA(15mils)

VCCDMI= 61mA(15mils)

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V

VCCPNAND= 156mA(15mils)

VCCME3_3= 85mA(15mils)

VCCVRM=196mA(15mils)

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]

AR@ --> ARD CPU
CF@ --> CFD CPU

VCCACLK= 52mA(15mils)

VCCLAN = 320mA(30mils)

10/20 Change to 0.1uF

VCCME(+1.05V) = 1.849A(100mils)

68mA(15mils)

69mA(15mils)

VCCIO = 3.062A(150mils)

VCCSUS3_3 = 163mA(20mils)

VCC3_3 = 0.357A(30mils)

V_CPU_IO >1mA(15mils)

VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V

VCCRTC= 2mA(15mils)

VCCIO = 3.208A(150mils)

VCCSUS3_3 = 0.163A(20mils)

V5REF_SUS< 1mA

10/20 Change to 0.1uF

V5REF< 1mA

VCC3_3 = 0.357A(30mils)

31mA(15mils)

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

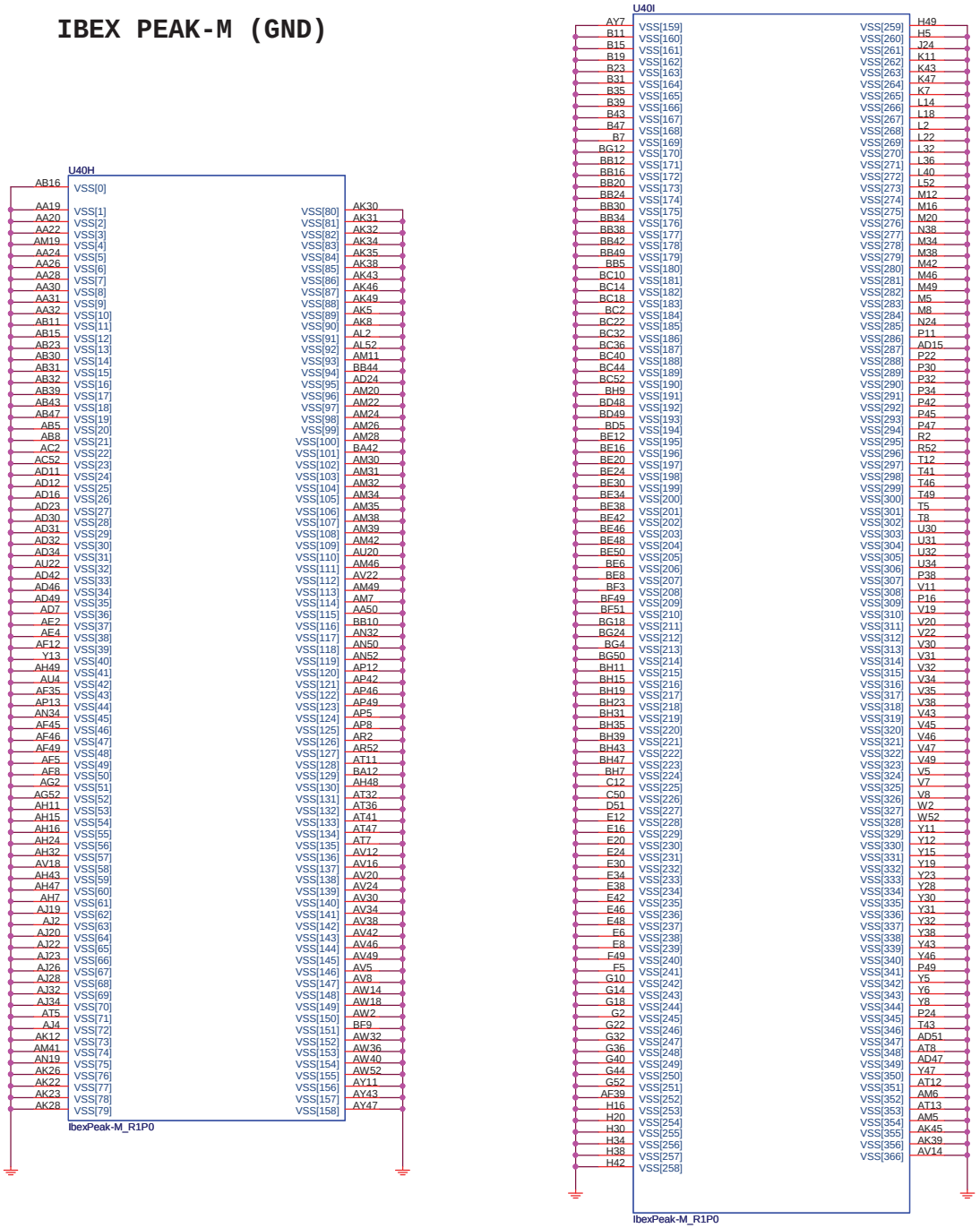
VCCSUSHDA= 8mA(15mils)

10/22 Stuff

Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	IBEX PEAK-M 5/6	3B
Date: Monday, February 22, 2010	Sheet 12 of 49	

IBEX PEAK-M (GND)



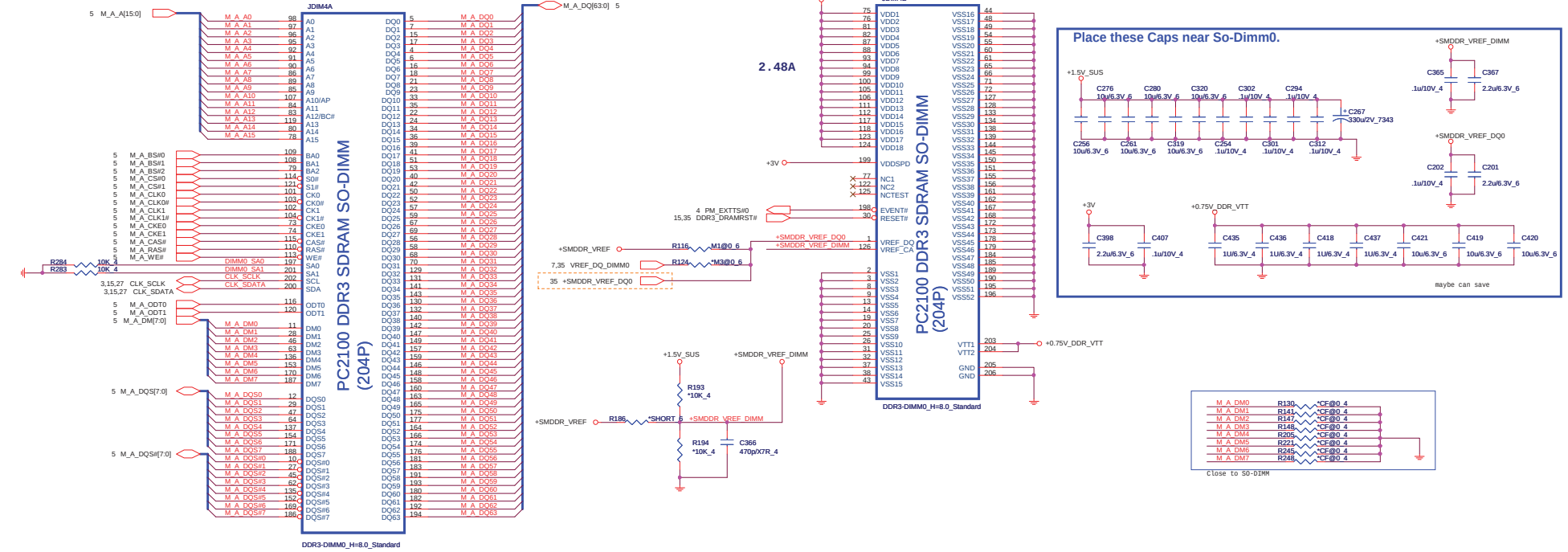
Quanta Computer Inc.

PROJECT : ZR7

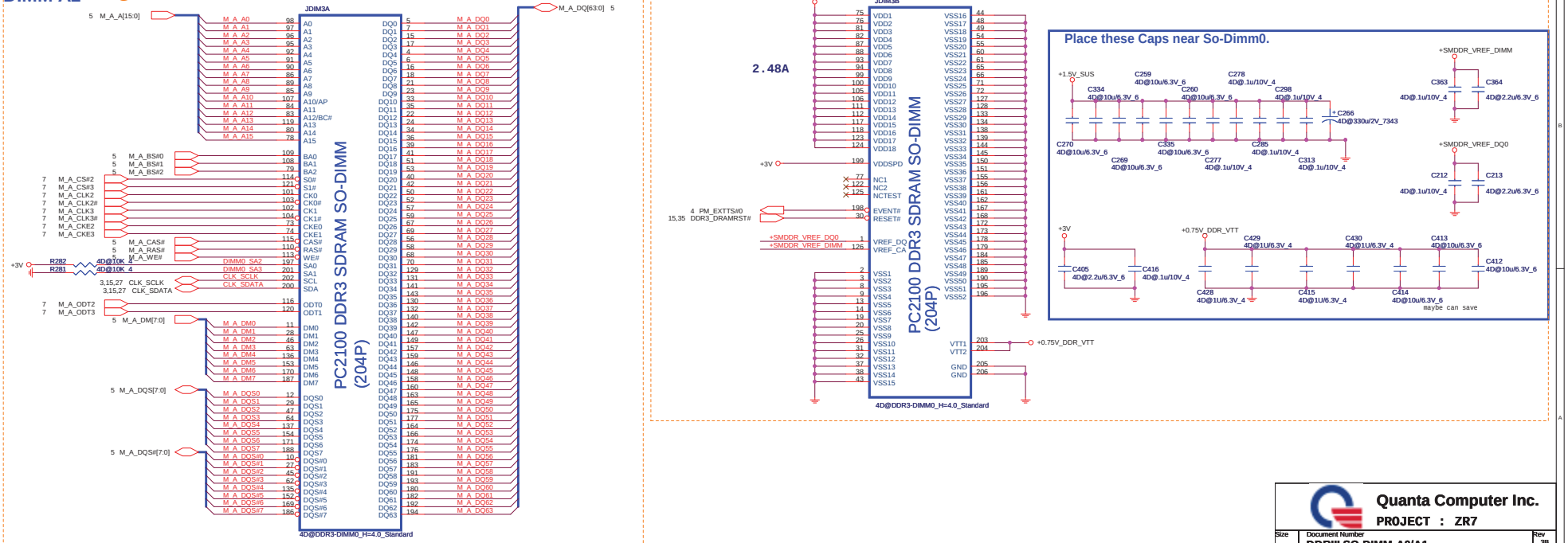
Size	Document Number	Rev
	IBEX PEAK-M 6/6	3B

Date: Monday, February 22, 2010 Sheet 13 of 49

DIMM A0

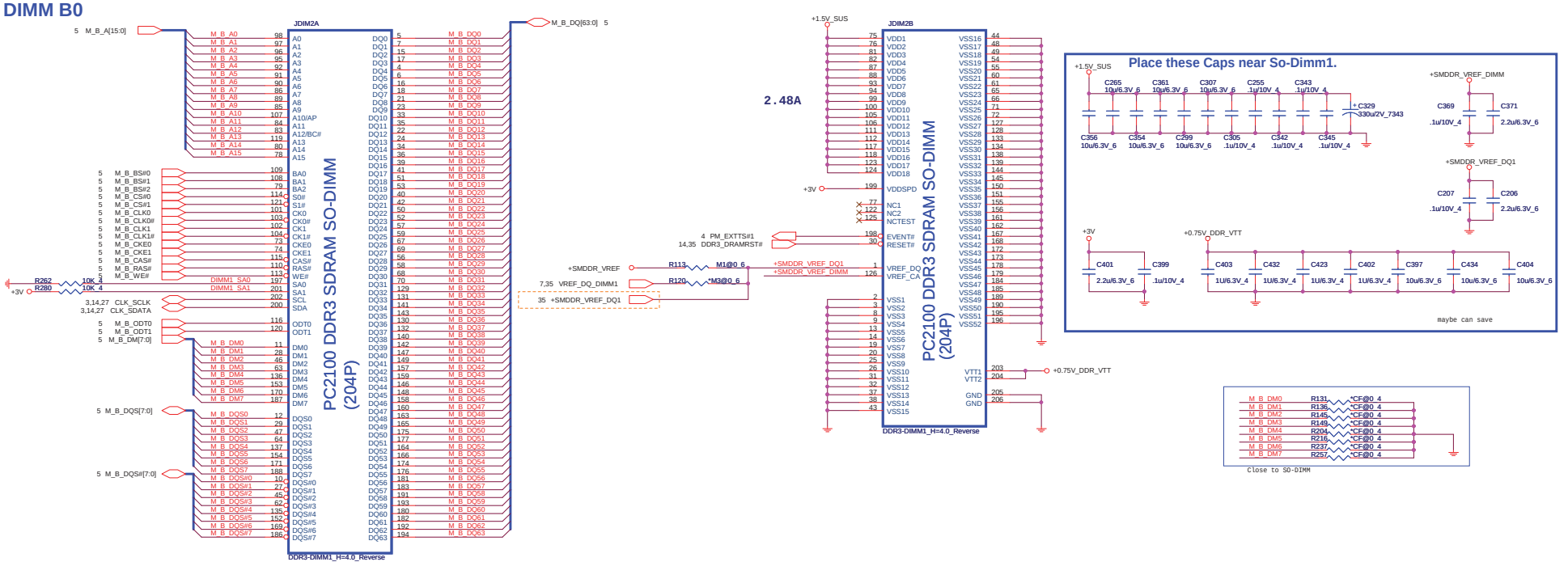


DIMM A1 4D@ --> 4 SO-DIMM

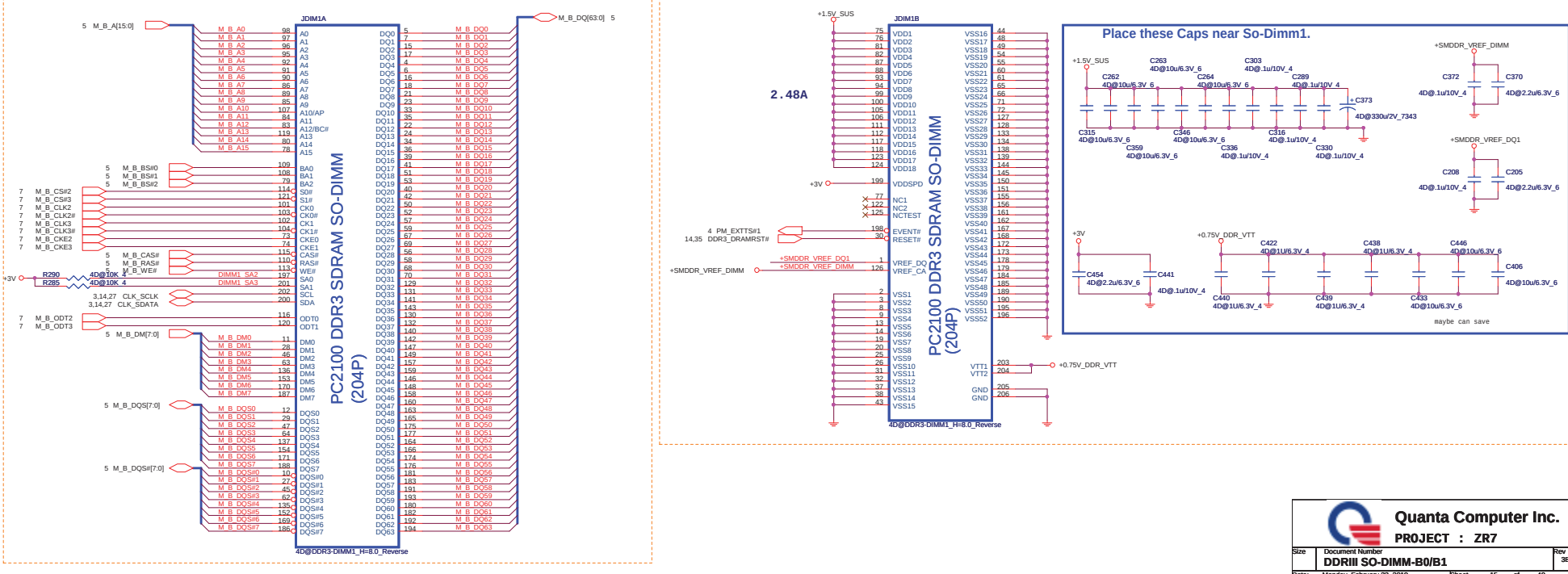


Quanta Computer Inc.			
PROJECT : ZR7			
Size	Document Number		Rev
	DDRIII SO-DIMM-A0/A1		3B
Date: Monday, February 22, 2010	Sheet 14 of 49		

DIMM B0



DIMM B1 4D@ --> 4 SO-DIMM



Quanta Computer Inc.		
PROJECT : ZR7		
Size	Document Number: DDRIII SO-DIMM-B0/B1	Rev: 3B
Date: Monday, February 22, 2010	Sheet 15 of 49	

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

Near BGA

12~16 mils width 110mA

12~16 mils width

10/20 add

10/20 del C3553,C3554

10/20 Modify to 1uF

11/27 Modify to CC0603

11/27 Modify to CC0603

U33A
VSP@N11P-GE-A1/H
COMMON

PCI EXPRESS

EV@ --> dGPU only
SW@ --> iGPU & dGPU Switch
ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)

SW@ --> iGPU & dGPU Switch

EV@ --> dGPU only

R456 un-mount for switchable function

Only for Hybrid

SW@ --> iGPU & dGPU Switch

power up sequence

PXE 1.05VDD

I/O 3.3V

NVCORE

1.5VFBDDQ

NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time

NVVDD

GPIO

tsNVVDD<= 192us

PEX_RST timing

I/O 3.3V

PEX_RST

Trise >= 1uS

Tfail <=500nS

Quanta Computer Inc.

PROJECT : ZR7

Size | Document Number: N11P-GE (PCIE I/F) 1/5 | Rev: 3B

Date: Monday, February 22, 2010 | Sheet 16 of 49

VSP@ --> Operation P/N (VGA) 11EP@ --> N11P/N11E-GE1 Setting

ES@ --> External VGA SKU

U33B

fcbga973-nvidia-n11p-es-a1
COMMON

12/02 modify package for N10

21 VMA_DQ[63..0]
21 VMA_DM[7..0]
21 VMA_WDQS[7..0]
21 VMA_RDQS[7..0]
22 VMC_DQ[63..0]
22 VMC_DM[7..0]
22 VMC_WDQS[7..0]
22 VMC_RDQS[7..0]

U33C

fcbga973-nvidia-n11p-es-a1
COMMON

12/02 modify package for N10

12/02 modify package for N10

12/02 modify package for N10

Un-stuff for N11M
Stuff for N11P ,N11E

11EP@ --> N11P/N11E-GE1 Setting

MEMORY I/F A

MEMORY I/F C

15mils width

For Debug only

15mils width

2/16

All need stuff for N10P

VSP@ N11P/N11E-GE1 Stuff 40.2 ohm
N11M-GE1 Stuff 60.4 ohm

Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE (MEMORY I/F) 2/5	3B

Date: Monday, February 22, 2010 Sheet 17 of 49

ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)

U33D COMMON
fcbga973-nvidia-n11p-es-a1

IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL

LVDS clk spread : Center
+/-0.5% (30~33KHZ)

11/16 Change LVDS to two channel.

TMDS channel two

Display port output

10/20 Del C3647

10/20 Del C3515

10/23 Modify

10/20

GPU all PWROK

10/20 STUFF

PLACE CLOSE TO GPU

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

11/27 Modify C601,C600 to 27pF

10 k pull-down only if no spread chip used.

(1.05V +/- 3%)

Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
N11P-GE (DISPLAY) 3/5
Rev 3B
Date: Monday, February 22, 2010
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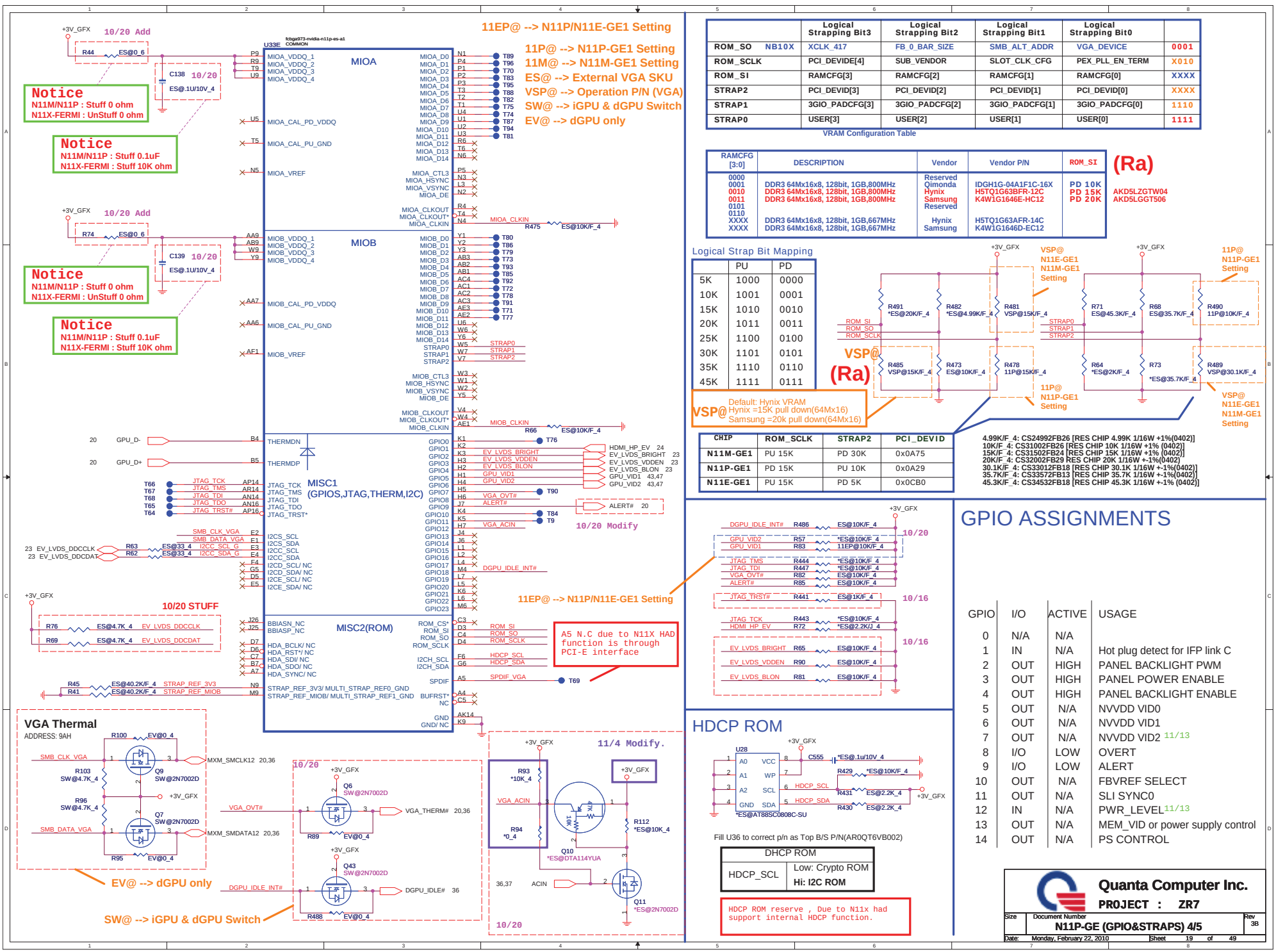


	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

AKD5LZGTW04
AKD5LGGT506

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VSP@ Default: Hynix VRAM
Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PD 15K	PU 10K	0x0A29
N11E-GE1	PU 15K	PD 5K	0x0CB0

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

Size	Document Number	Rev
	N11P-GE (GPIO&STRAPS) 4/5	3B
Date: Monday, February 22, 2010	Sheet 19 of 49	

ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)

U33F

+VGPU_CORE

fcbga973-nvidia-n11p-es-a1
COMMON

+VGPU_CORE

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

U33G

fcbga973-nvidia-n11p-es-a1
COMMON

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

NVVDD Decoupling

+VGPU_CORE

2/16

PLACE UNDER BALLS

C72	ES@.01u/25V_4
C73	ES@.01u/25V_4
C117	ES@.01u/25V_4
C108	ES@.01u/25V_4
C78	ES@.01u/25V_4
C92	ES@.01u/25V_4
C125	ES@0.022U/16V_4
C95	ES@0.022U/16V_4
C115	ES@0.022U/16V_4
C116	ES@0.022U/16V_4
C69	ES@0.047U/25V_4
C94	ES@0.047U/25V_4
C75	ES@0.047U/25V_4
C106	ES@0.22u/6.3V_4
C91	ES@0.22u/6.3V_4
C120	ES@1U/6.3V_4
C113	ES@4.7U/6.3V_6
C81	ES@10U/6.3V_6
C105	ES@10U/6.3V_6

11/27 Modify to CC0603

C151	ES@330u/2V_7343

11/25 Modify.

PLACE NEAR BALLS

Thermal Sensor

+3V_GFX

R427 *ES@10K_4

19,36 MXM_SMCLK12

Q30 *ES@2N7002D

+3V_GFX

*ES@10K_4 R426

19,36 MXM_SMDATA12

Q31 *ES@2N7002D

GPU_SMCLK

GPU_SMDATA

19 ALERT#

19,36 VGA_THERM#

10/20 Modify

U27

SCLK		VCC	1
SDA		DXP	2
ALERT#		DXN	3
OVERT#		GND	5

+3V_GFX

*ES@.1u/10V_4 C553

C554 *ES@2200p/50V_4

GPU_D+ 19

GPU_D- 19

*ES@G780-1P81U(MSOP)

ADDRESS: 9AH

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

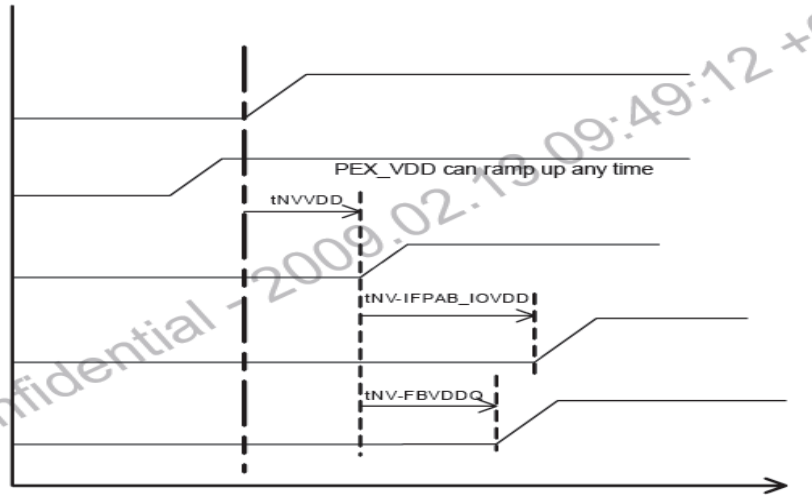
+3V VDD33

+1.05V PEX_VDD

V_CORE NVVDD

+1.8V IFPAB_IOVDD

+1.5V FBVDDQ



Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	3B

Date: Monday, February 22, 2010 Sheet 20 of 49

ES@ --> External VGA SKU

VSP@ --> Operation P/N (VGA-VRAM)

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3

U2 / U30 / U1 / U29 — 96-BALL SDRAM DDR3 — VSP@VRAM_DDR3

Should be 240 Ohms +-1%

R4 ES@243/F_4 (U2) / R423 ES@243/F_4 (U30) / R1 ES@243/F_4 (U1) / R433 ES@243/F_4 (U29)

10/21 Add for NV Request

R3 ES@243/F_4 (VMA_CLKP0 / VMA_CLKN0)

R2 ES@243/F_4 (VMA_CLKP1 / VMA_CLKN1)

R422 ES@1.33K/F_4 (VREFC_VMA1) — R419 ES@1.33K/F_4 — C546 ES@.1u/10V_4

R417 ES@1.33K/F_4 (VREFD_VMA1) — R424 ES@1.33K/F_4 — C533 ES@.1u/10V_4

R420 ES@1.33K/F_4 (VREFC_VMA3) — R421 ES@1.33K/F_4 — C542 ES@.1u/10V_4

R416 ES@1.33K/F_4 (VREFD_VMA3) — R418 ES@1.33K/F_4 — C545 ES@.1u/10V_4

+1.5V_GFX decoupling: C564, C539, C563, C16, C15, C13, C1, C2 (ES@1U/6.3V_4); C14, C6, C537, C538, C557, C559, C7, C560 (ES@1U/6.3V_4); C18, C10, C541, C536 (ES@1U/6.3V_4); C551 *ES@10u/6.3V_6; C20, C556 (ES@.1u/10V_4); C4, C19, C3, C5, C17, C12, C535, C562 (ES@.1u/10V_4); C9, C21, C534, C11, C561, C540 (ES@.1u/10V_4); C544, C552, C543, C558 (ES@.1u/10V_4)

Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE VRAM-1(DDR3 BGA96)	3B

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11EP@ --> N11P/N11E-GE1 Setting

VSP@ --> Operation P/N (VGA-VRAM CH:B N11P/N11E only)

CHANNEL B: 256MB/512MB DDR3

17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]

U34 / U6 / U3 / U32 — VSP@VRAM_DDR3 — 96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R452 11EP@243/F_4 — R50 11EP@243/F_4 — R23 11EP@243/F_4 — R438 11EP@243/F_4

+1.5V_GFX

10/21 Add for NV Request

R451 11EP@243/F_4 (VMC_CLKP0 / VMC_CLKN0)

R446 11EP@1.33K/F_4 (VREFC_VMC1) — R445 11EP@1.33K/F_4 — C590 11EP@.1u/10V_4

R55 11EP@1.33K/F_4 (VREFD_VMC1) — R54 11EP@1.33K/F_4 — C152 11EP@.1u/10V_4

R21 11EP@243/F_4 (VMC_CLKP1 / VMC_CLKN1)

10/21 Add for NV Request

R14 11EP@1.33K/F_4 (VREFC_VMC3) — R15 11EP@1.33K/F_4 — C38 11EP@.1u/10V_4

R437 11EP@1.33K/F_4 (VREFD_VMC3) — R436 11EP@1.33K/F_4 — C571 11EP@.1u/10V_4

+1.5V_GFX decoupling: C49 C65 C55 C579 C580 C581 C567 C569 (11EP@1U/6.3V_4); C128 C25 C584 C578 (11EP@1U/6.3V_4); C592 C29 C114 C159 C121 C593 (*11EP@10u/6.3V_6 / 11EP@.1u/10V_4); C595 C572 C591 C46 C577 C575 C167 C33 (11EP@.1u/10V_4); C585 C70 C570 C41 C568 C594 C171 (11EP@.1u/10V_4); C135 C131 C142 C162 C587 C588 C597 C582 (11EP@1U/6.3V_4)

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PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE VRAM-2(DDR3 BGA96)	3B

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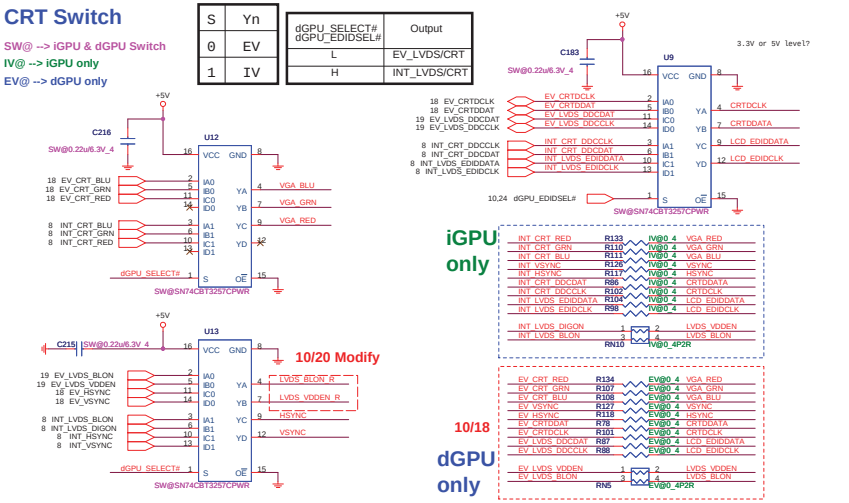
CRT Switch

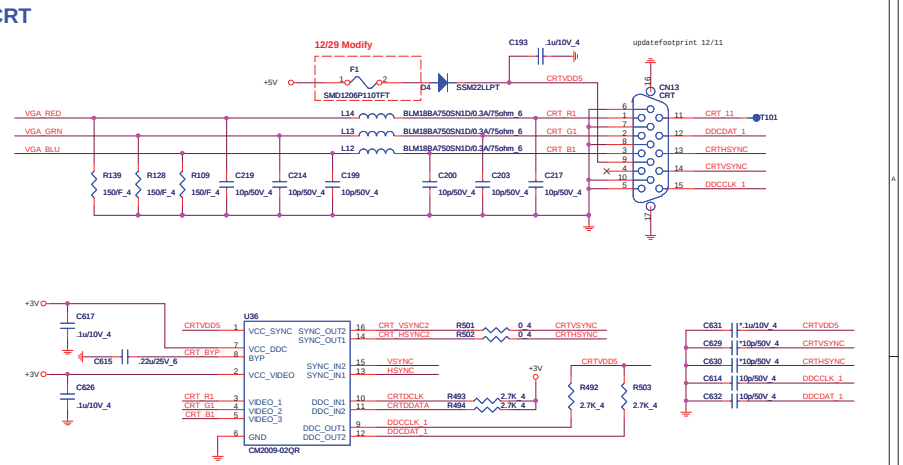
SW@ --> iGPU & dGPU Switch
IV@ --> iGPU only
EV@ --> dGPU only

S	Yn
0	EV
1	IV

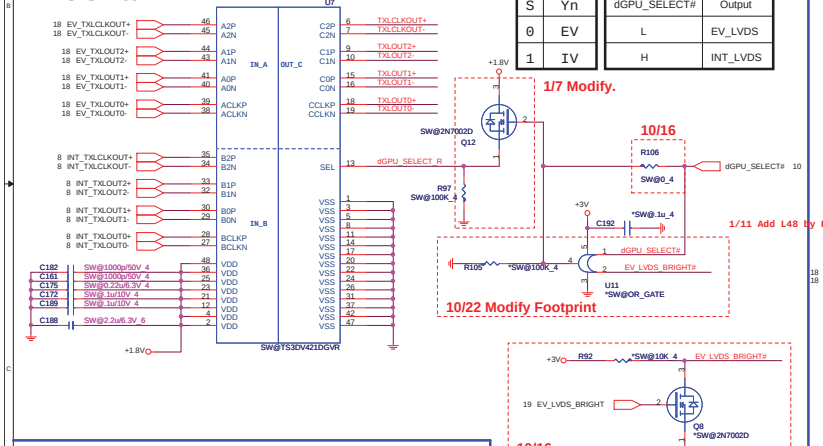
dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT



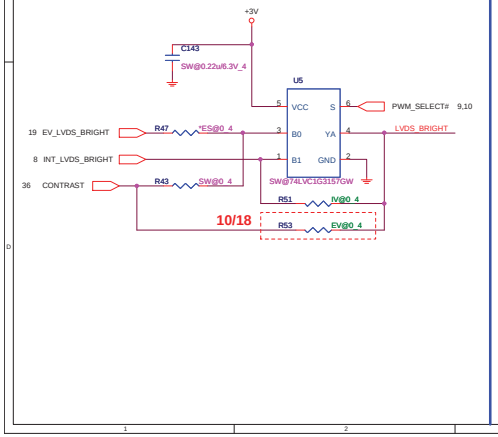
CRT



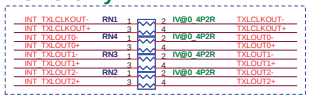
LVDS Switch



Brightness

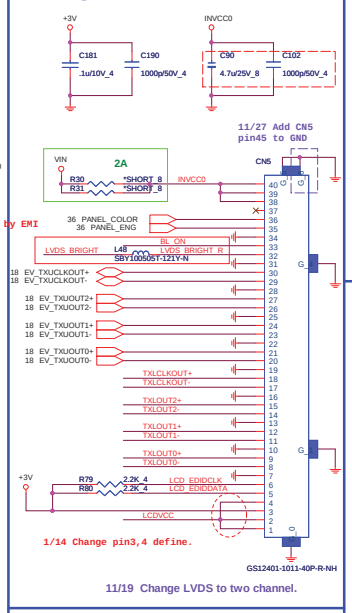


iGPU only

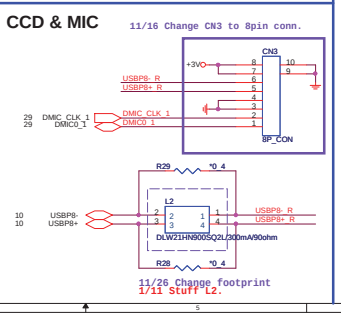


dGPU only

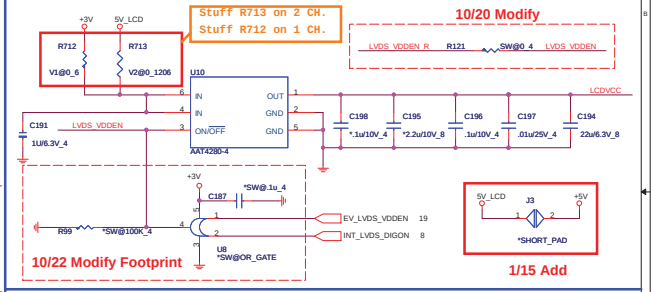
LVDS



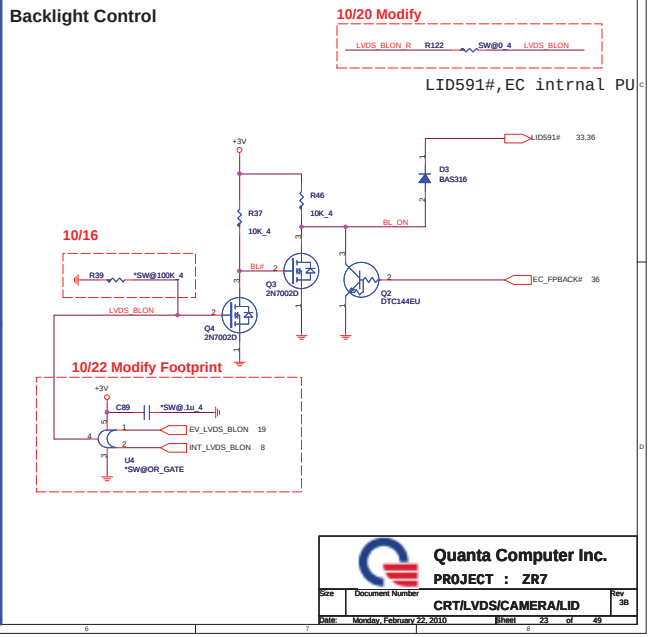
CCD & MIC



LCD_ON (LCD Power)



Backlight Control



Quanta Computer Inc.			
PROJECT : ZR7			
Size	Document Number	CRT/LVDS/CAMERA/LID	Rev 3B
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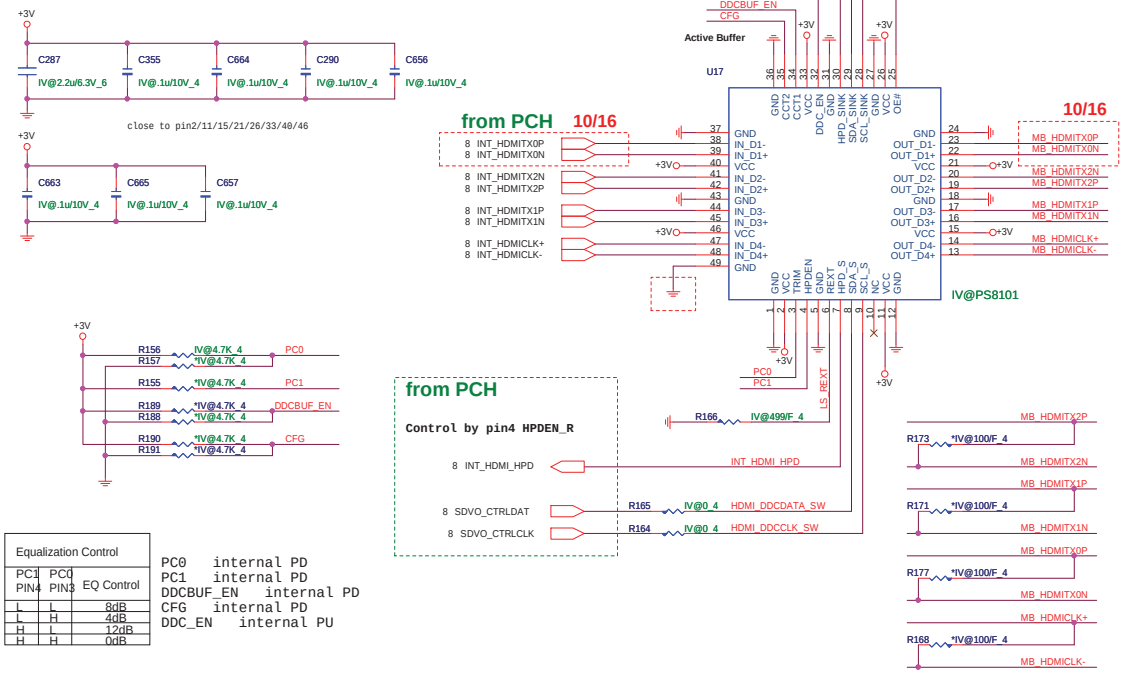
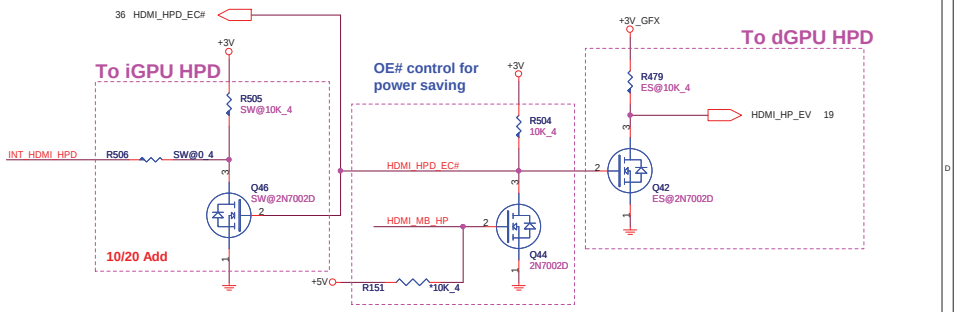
iGPU HDMI LEVEL SHIFTER

IV@ --> iGPU only
EV@ --> dGPU only
ES@ --> External VGA SKU
SW@ --> iGPU & dGPU Switch
CSP@ --> Operation P/N

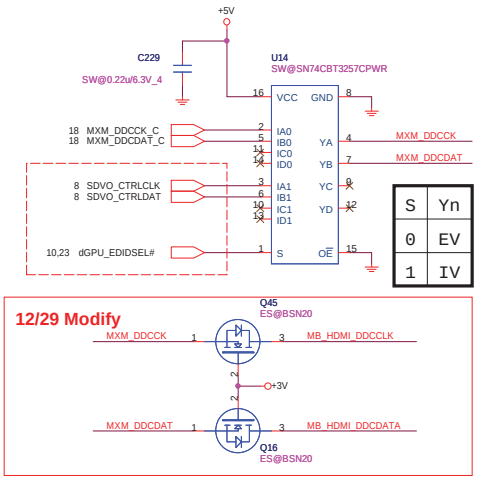


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

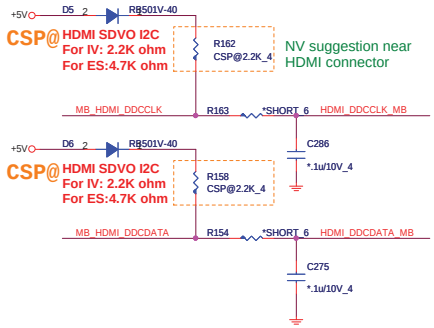
PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU



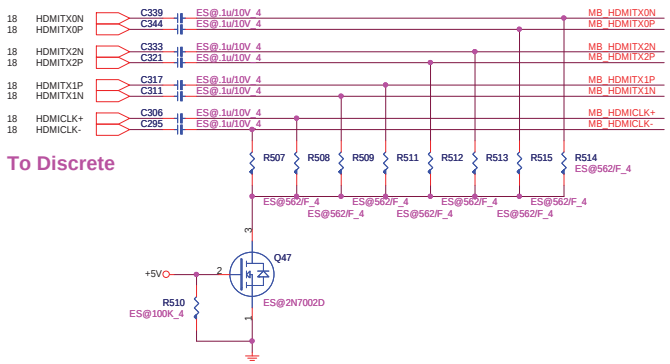
SDVO I2C Control



Bypass(default)
MXM_DDCCK_C R150 EV@0_4 MXM_DDCCK
MXM_DDCDAT_C R146 EV@0_4 MXM_DDCDAT



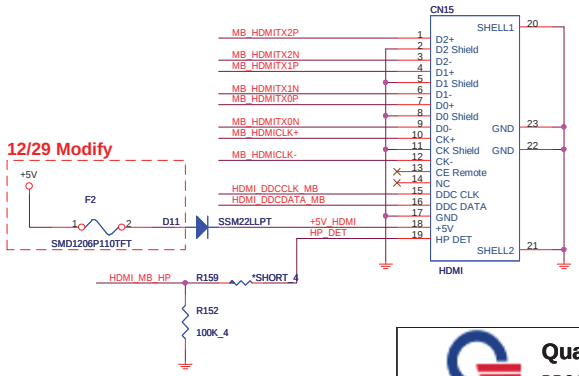
GPU Switchable Graphic HDMI source



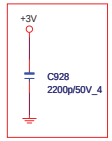
ESD Protect

12/29 Delete U15, U16, U18.

HDMI connector



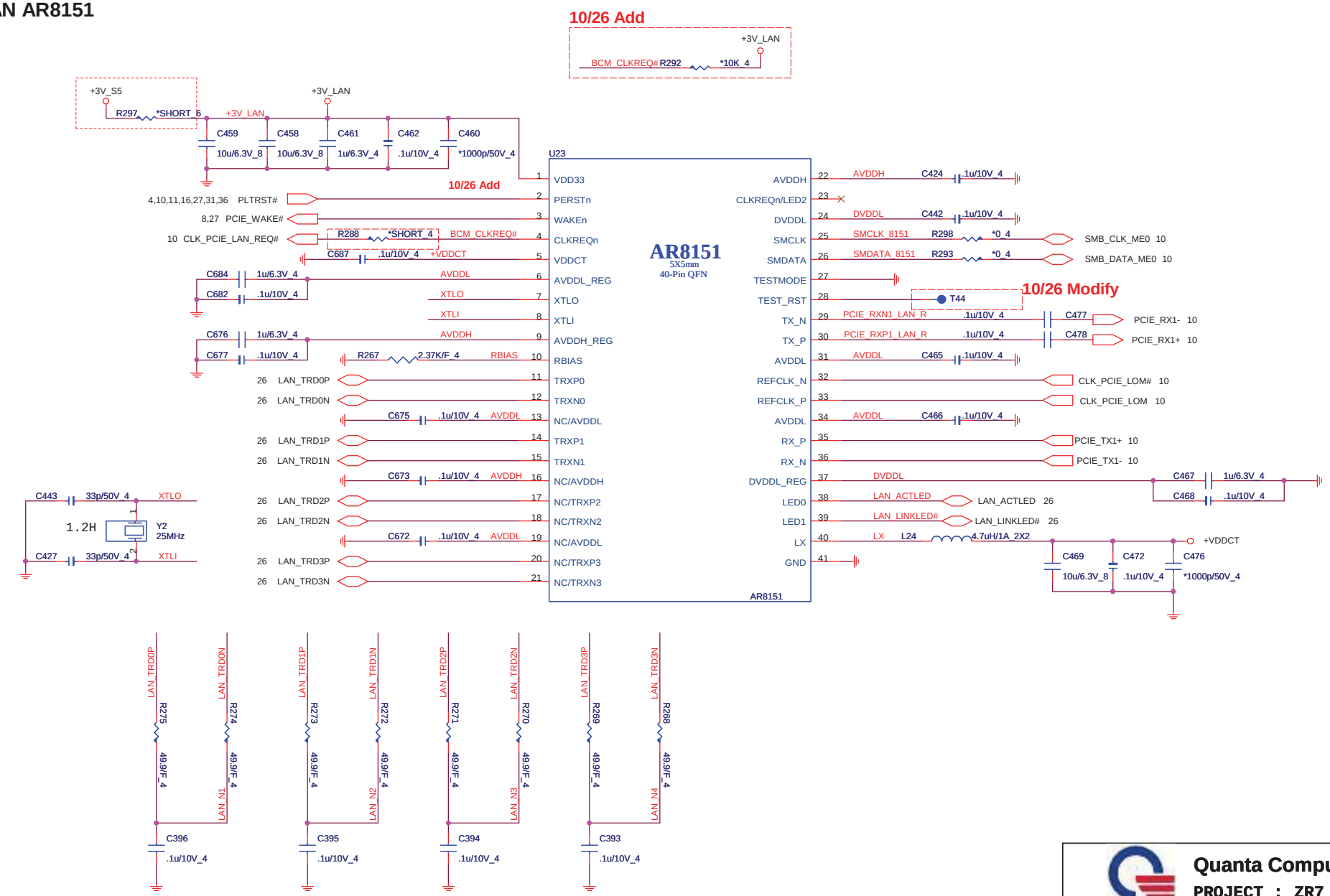
1/11 Add C928 by EMI.



Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	HDMI (PS8101)	3B
Date: Monday, February 22, 2010	Sheet 24 of 49	

Giga-LAN AR8151



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PROJECT : ZR7

Size	Document Number	Rev
	GLAN BCM57780	3B

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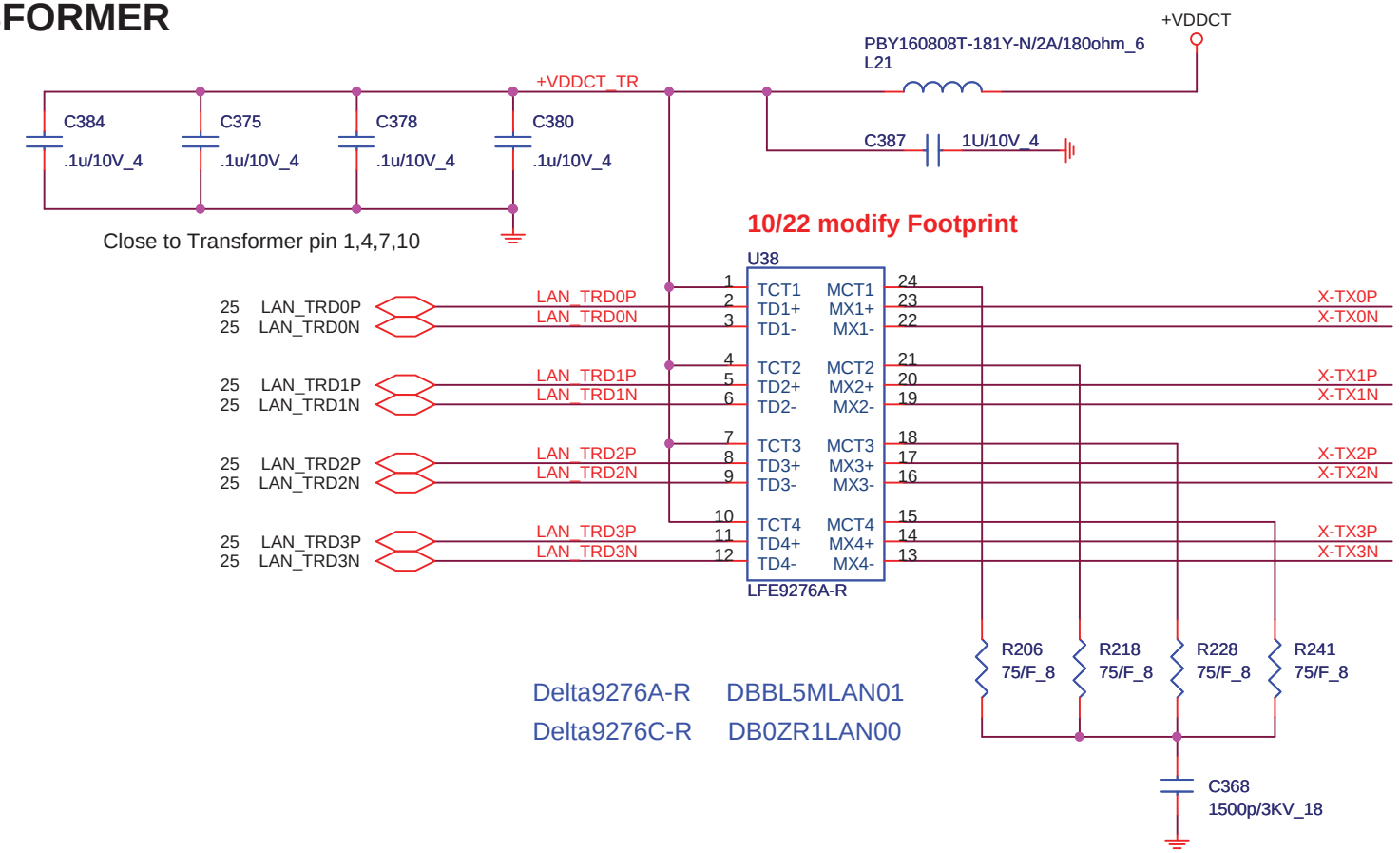
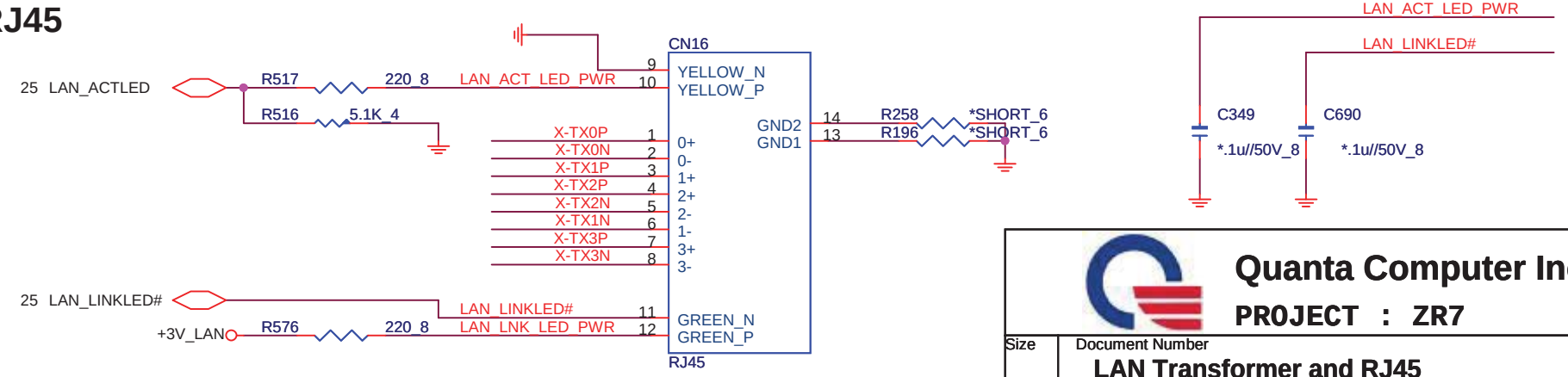
TRANSFORMER



RJ45



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PROJECT : ZR7

Size	Document Number	Rev
	LAN Transformer and RJ45	3B
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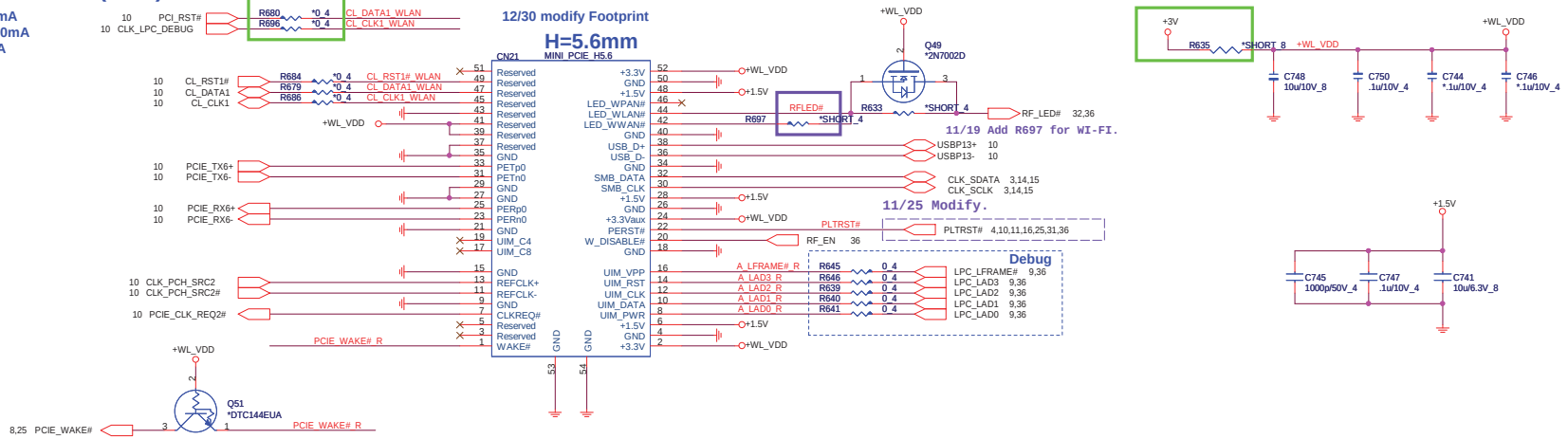
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

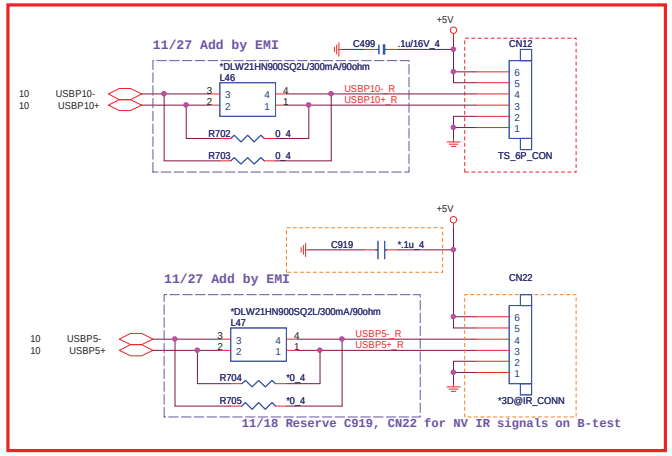
Check LED signal. (active high or low)

12/30 modify Footprint

H=5.6mm



1/8 Change CN12,CN22 6pin conn footprint for Touch Screen.



Quanta Computer Inc.			
PROJECT : ZR7			
Size	Document Number		Rev
	MINI PCI-E card/Touch Screen		3B
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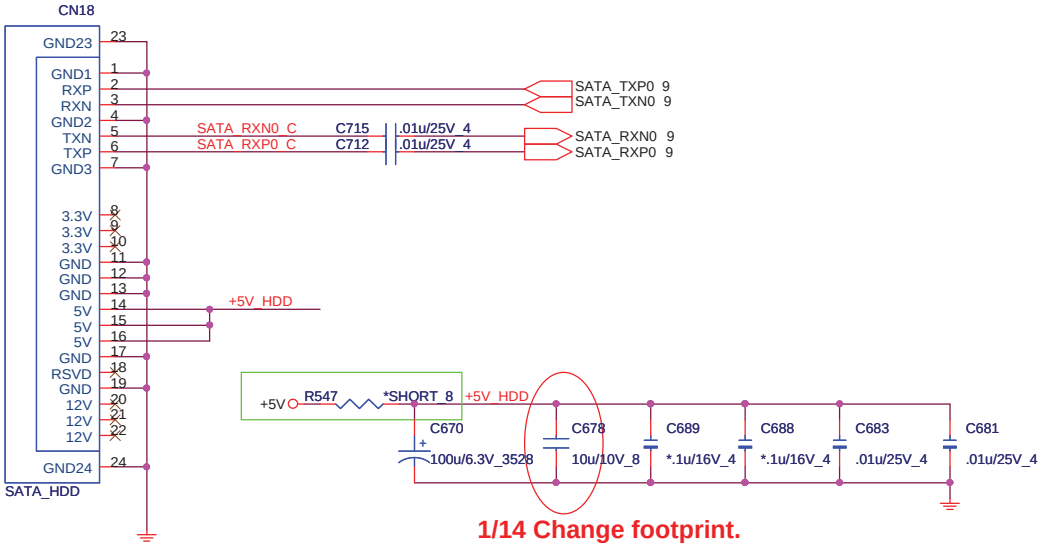
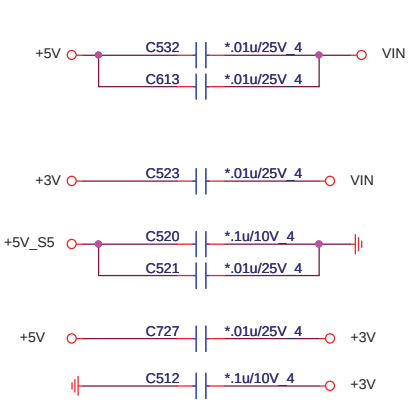
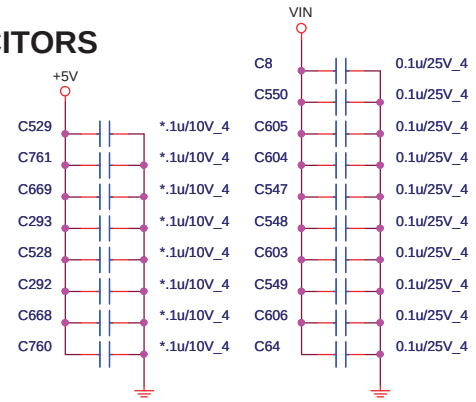
MAIN SATA HDD

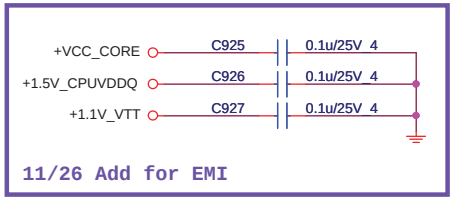


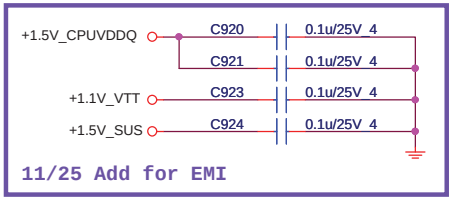
1/14 Change footprint.

EE RETURN-PATH CAPACITORS

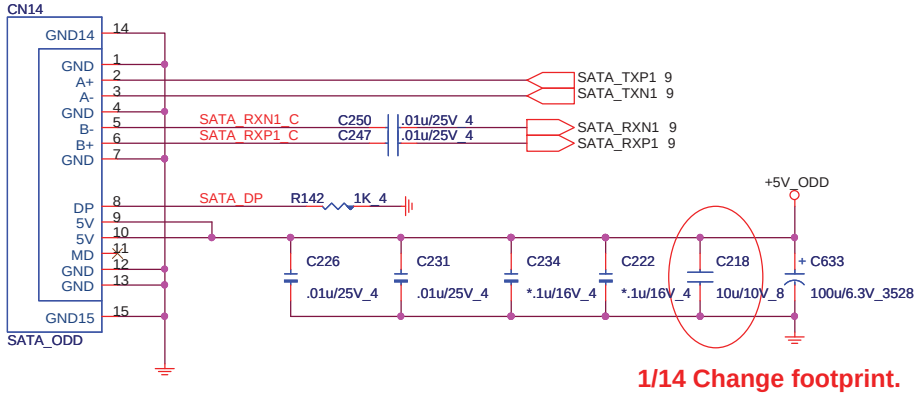






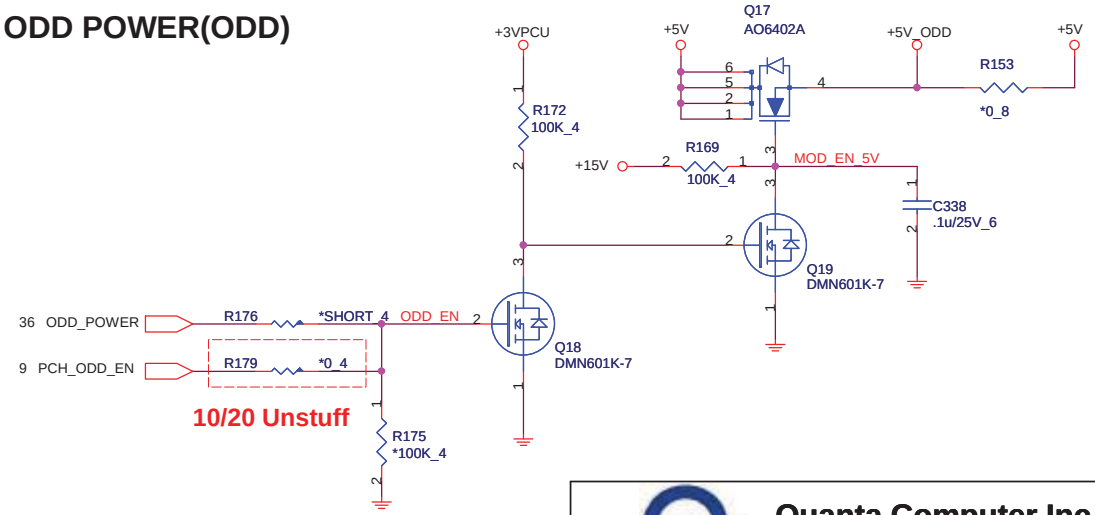


ODD (SATA)



1/14 Change footprint.

ODD POWER(ODD)



Quanta Computer Inc.		
PROJECT : ZR7		
Size	Document Number: SATA-HDD/ODD/USB-ESATA	Rev 3B
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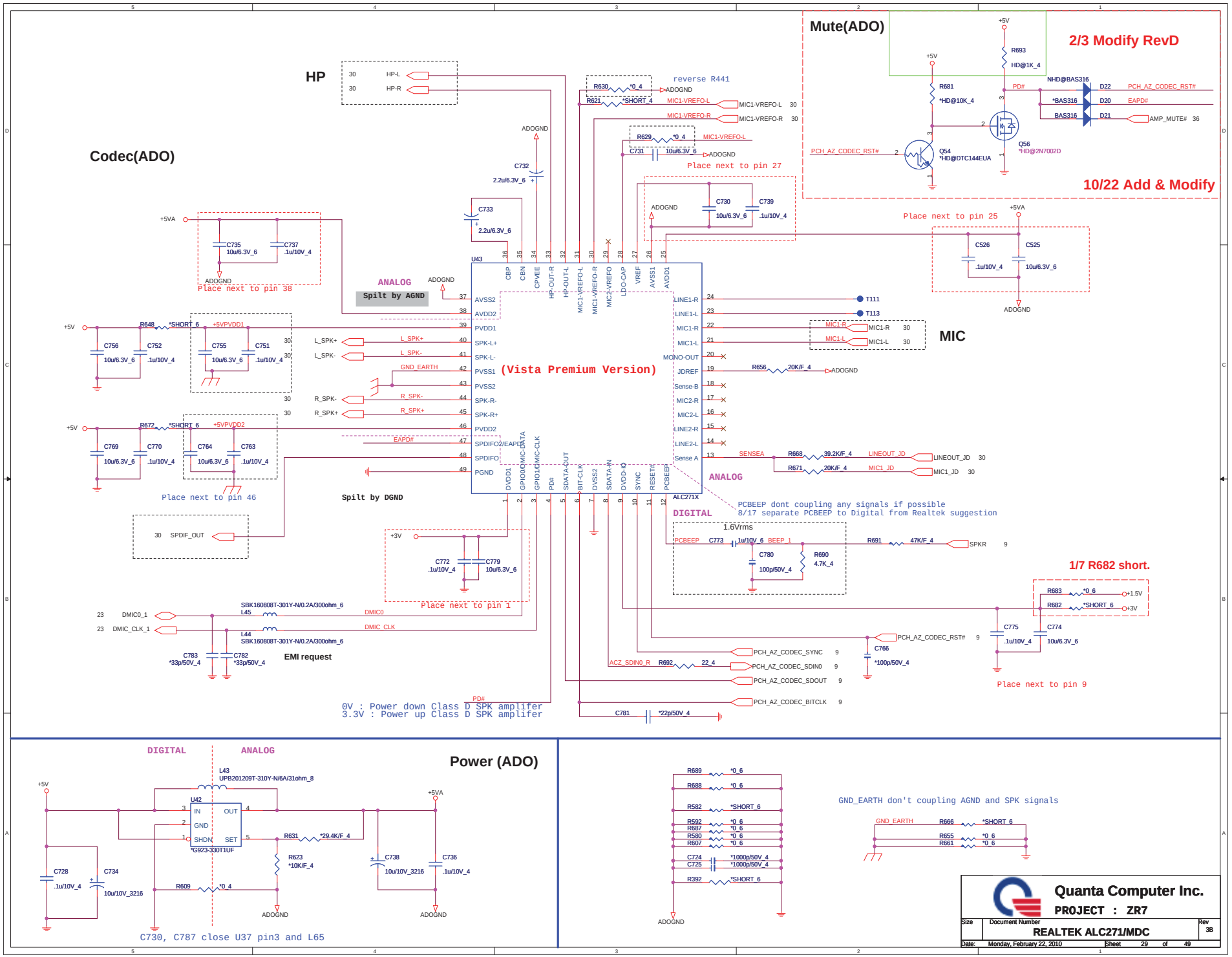
Mute(ADO)
2/3 Modify RevD
10/22 Add & Modify
HP
Codec(ADO)
MIC
Power (ADO)
ANALOG
DIGITAL
Spilt by AGND
Spilt by DGND
(Vista Premium Version)
ALC271X
reverse R441
Place next to pin 27
Place next to pin 25
Place next to pin 38
Place next to pin 46
Place next to pin 1
Place next to pin 9
1/7 R682 short.
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
1.6Vrms
EMI request
0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier
GND_EARTH don't coupling AGND and SPK signals
C730, C787 close U37 pin3 and L65
Quanta Computer Inc.
PROJECT : ZR7
REALTEK ALC271/MDC
Monday, February 22, 2010
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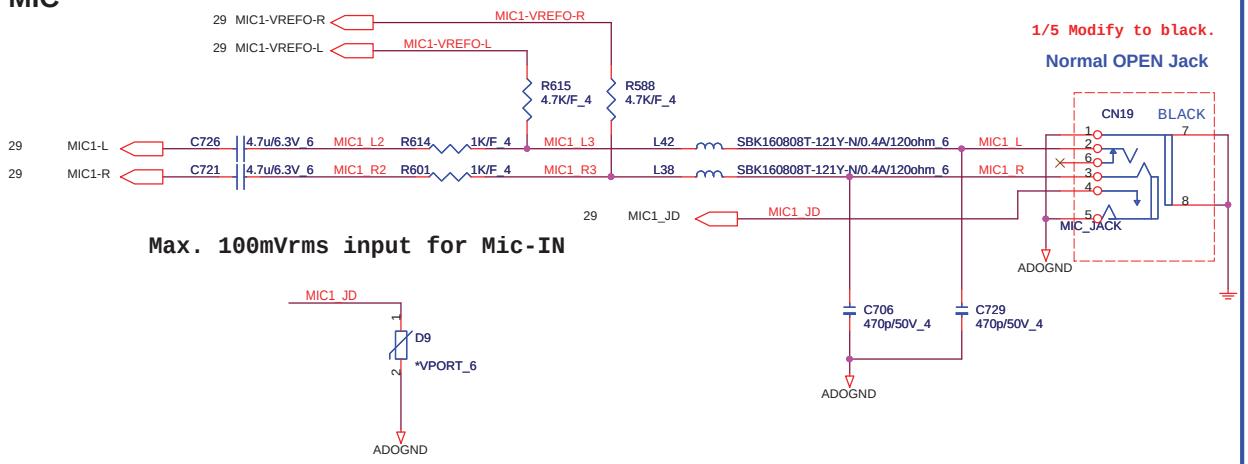
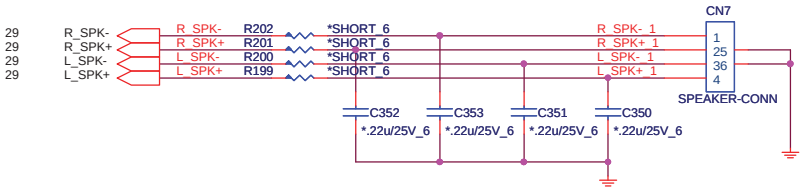
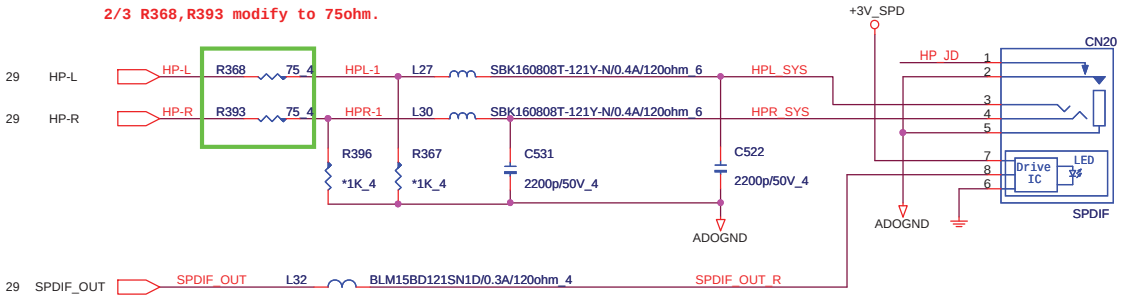
MIC

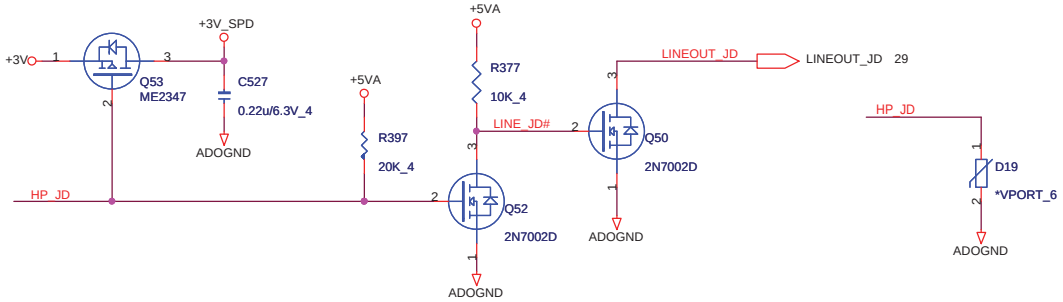


Internal Speaker



HP/SPDIF





Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	3B

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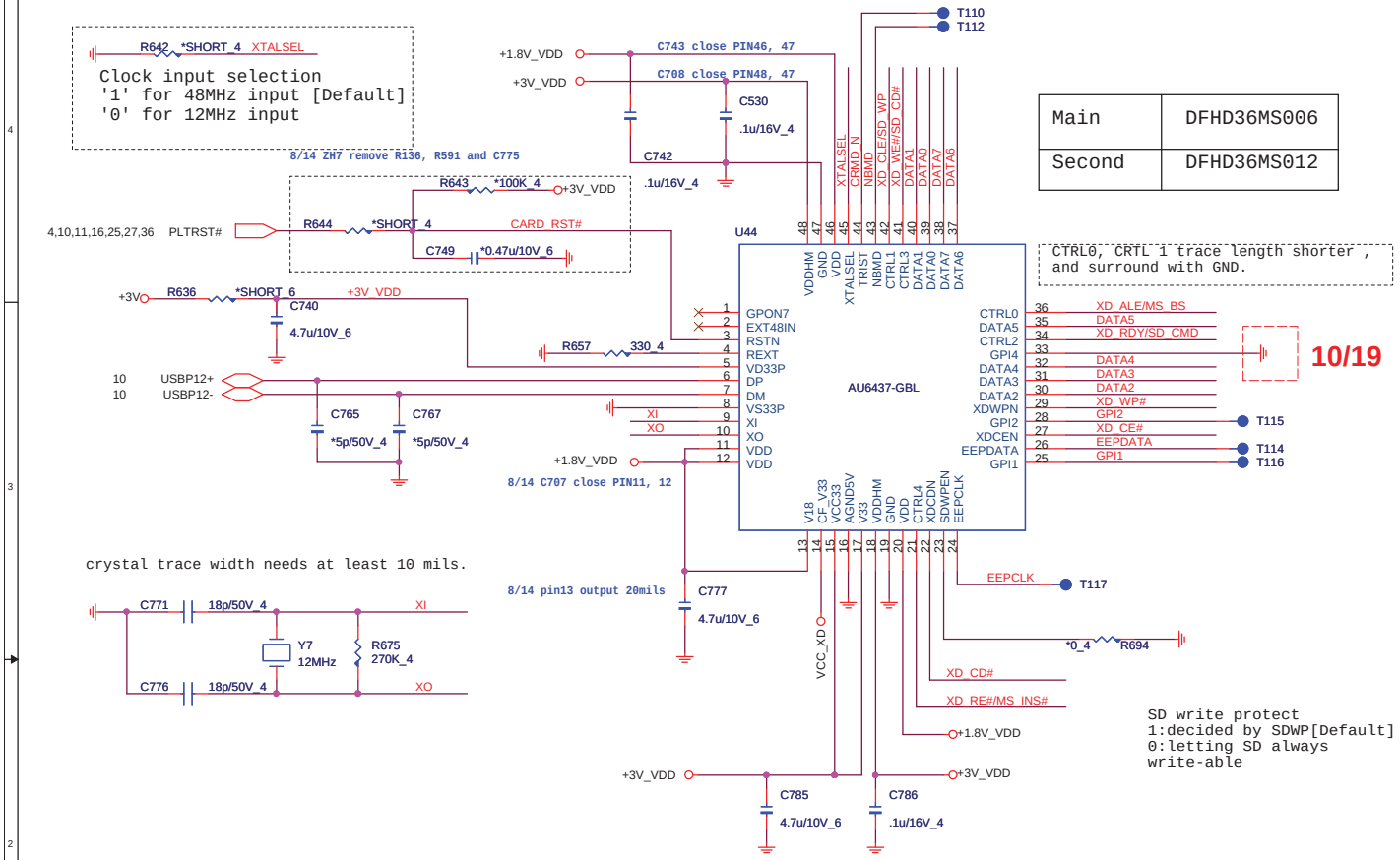
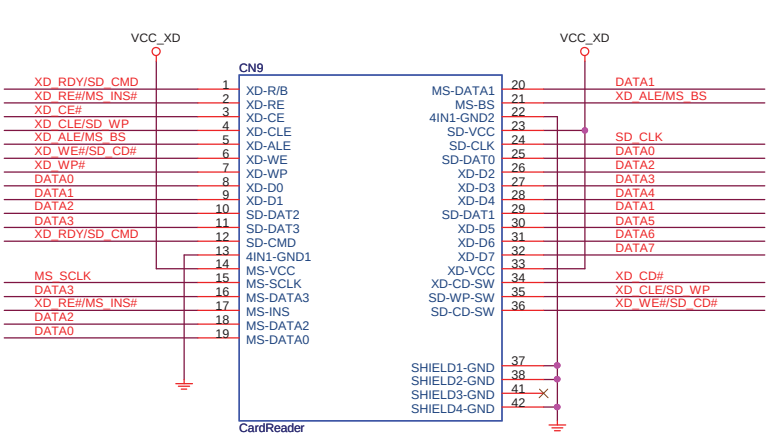
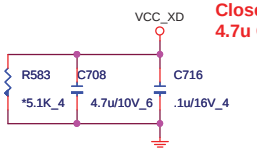
CARD READER Controller



Main	DFHD36MS006
Second	DFHD36MS012

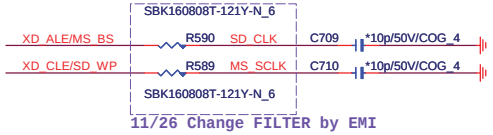
4 IN 1 CARD READER (MMC)





Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

Close to connector



11/26 Change FILTER by EMI

Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	AU6437 CardReader	3B
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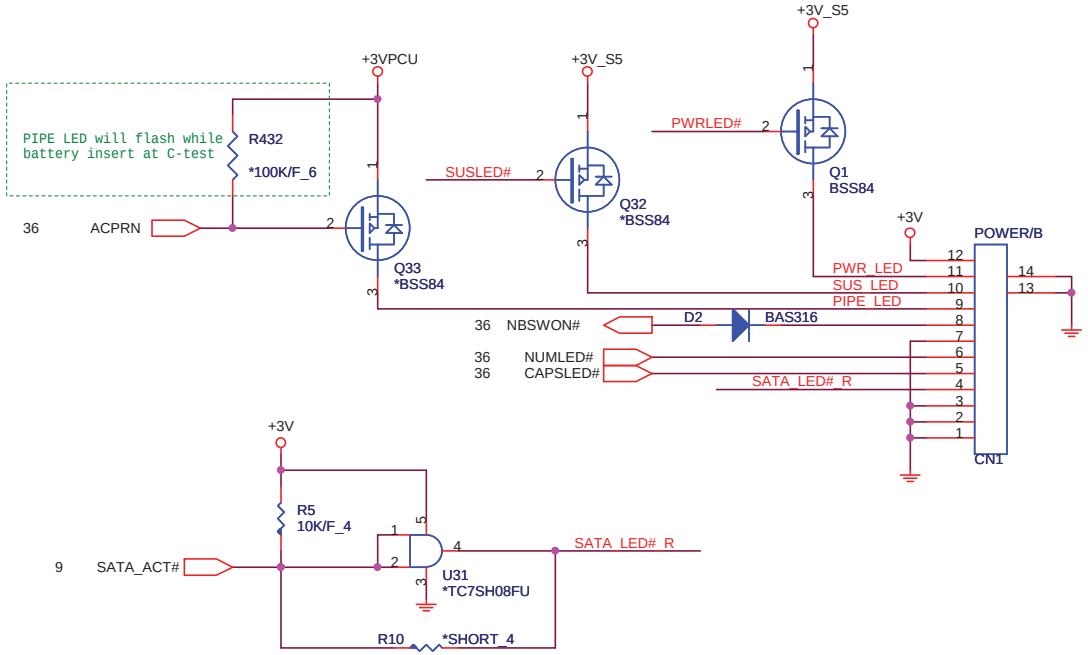
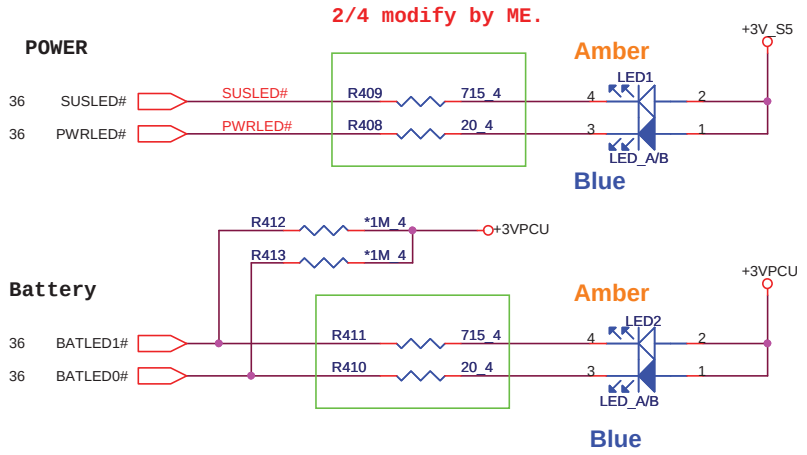
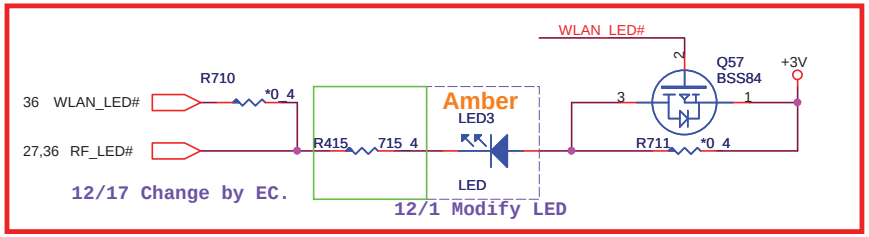
POWER BOARD CONN(UIF)

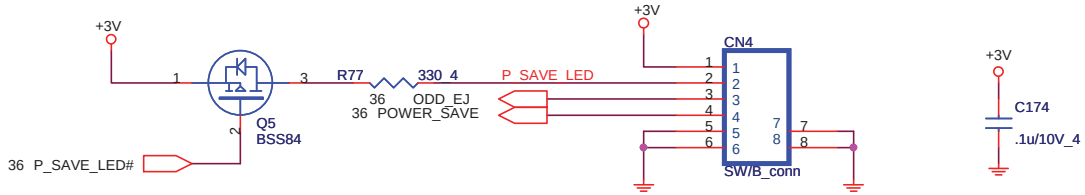


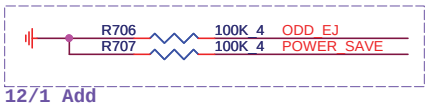
LED





SW /B





Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3B
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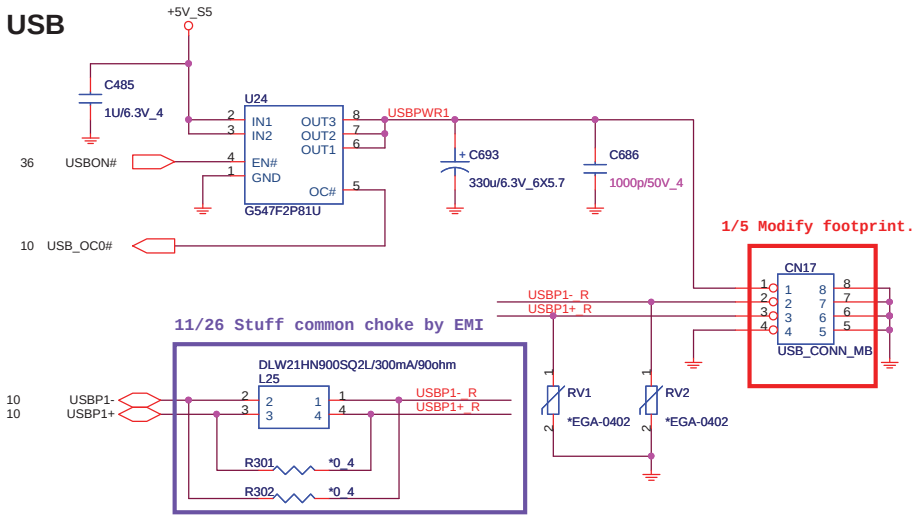
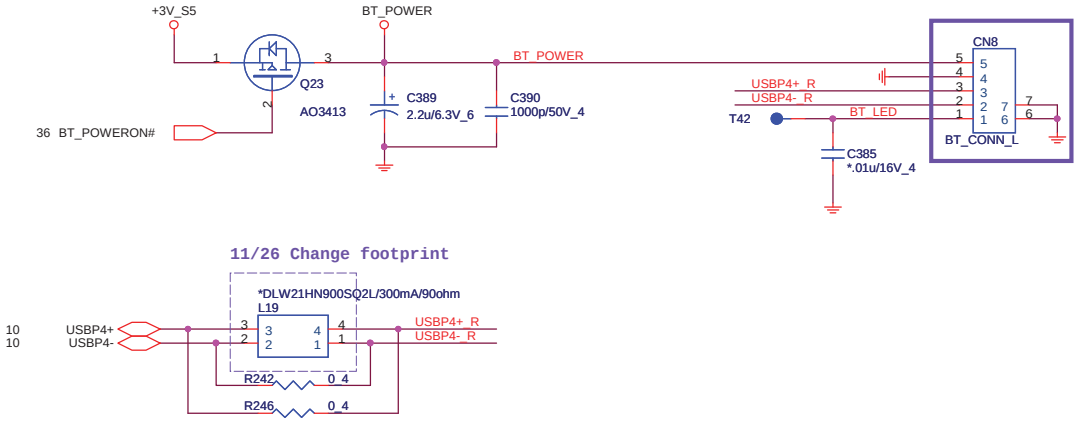
USB

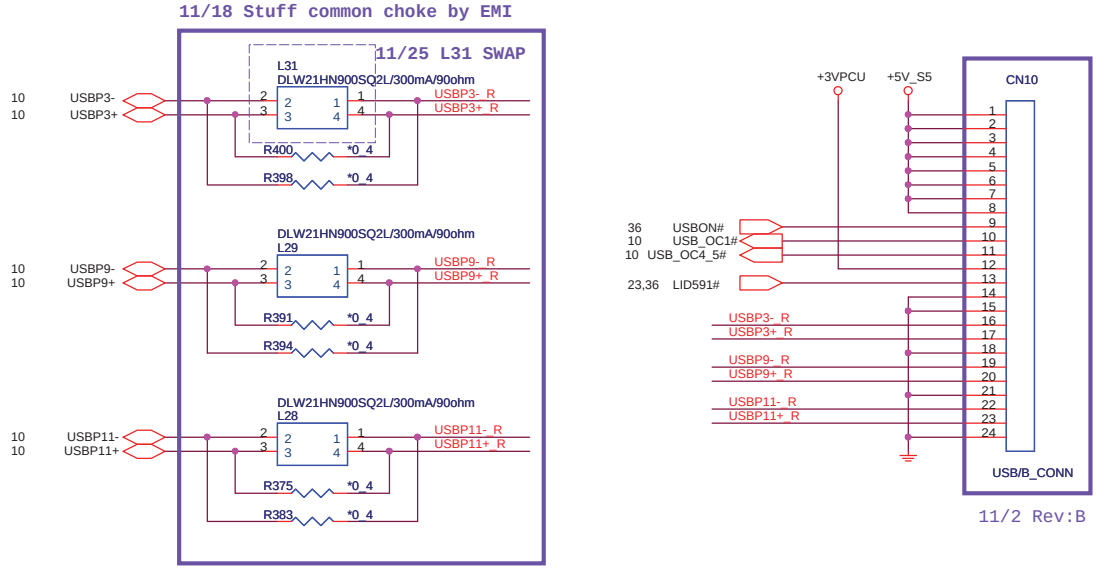


BLUETOOTH CONNECTOR

11/16 Rev:B Modify Footprint to 5pin.



USB/B



11/2 Rev:B Change CN10 P/N by PDC.

Quanta Computer Inc.		
PROJECT : ZR7		
Size	Document Number: USB/ BT	Rev: 3B
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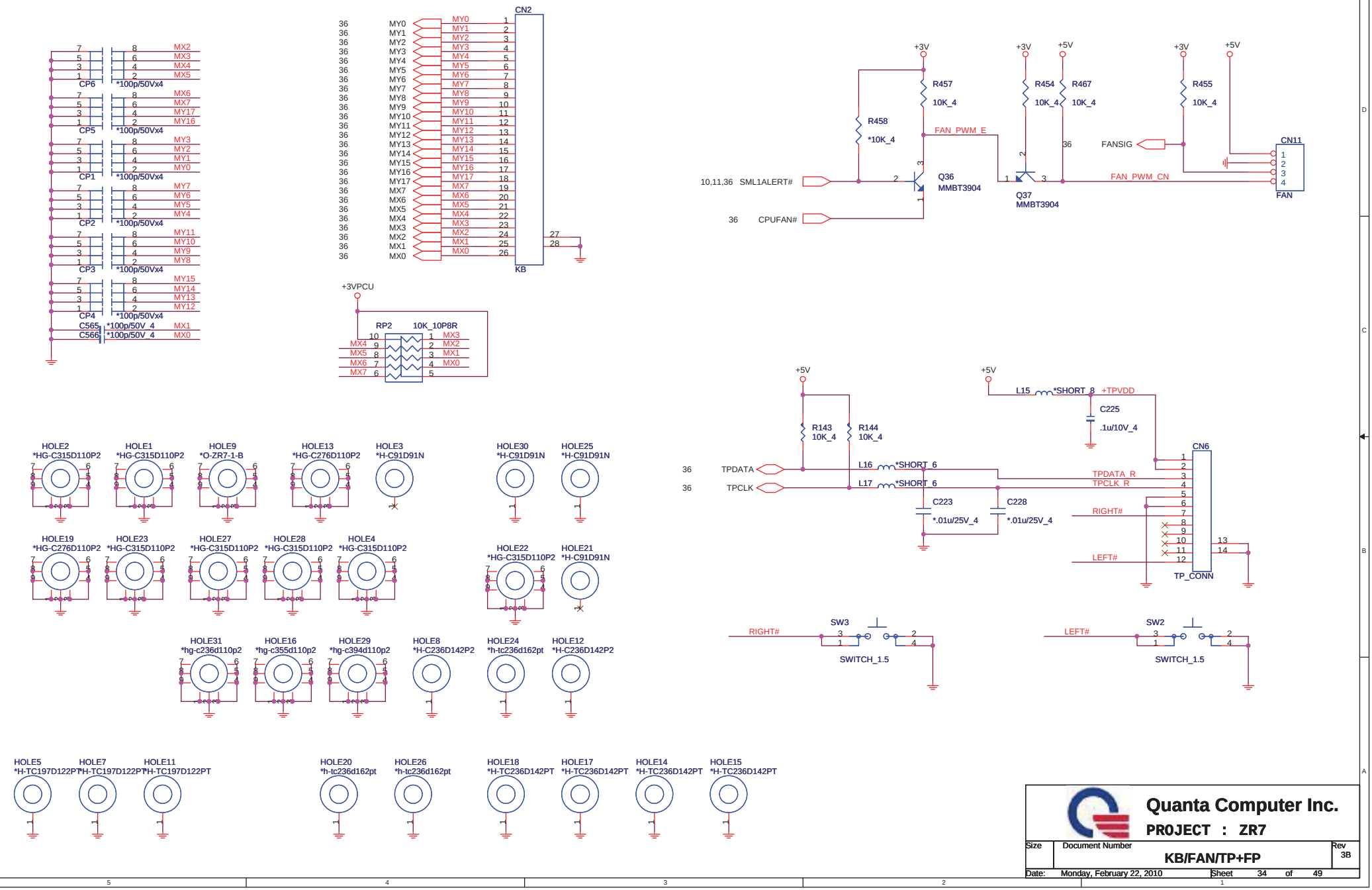

Quanta Computer Inc.		
PROJECT : ZR7		
Size	Document Number: KB/FAN/TP+FP	Rev: 3B
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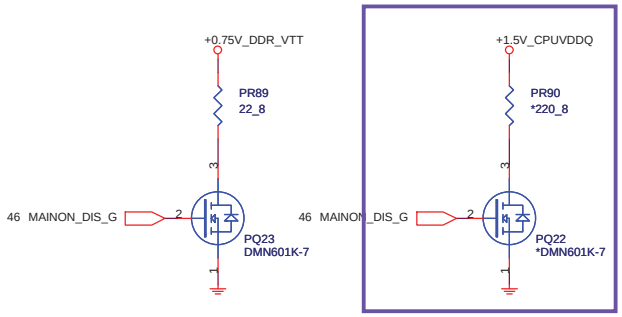
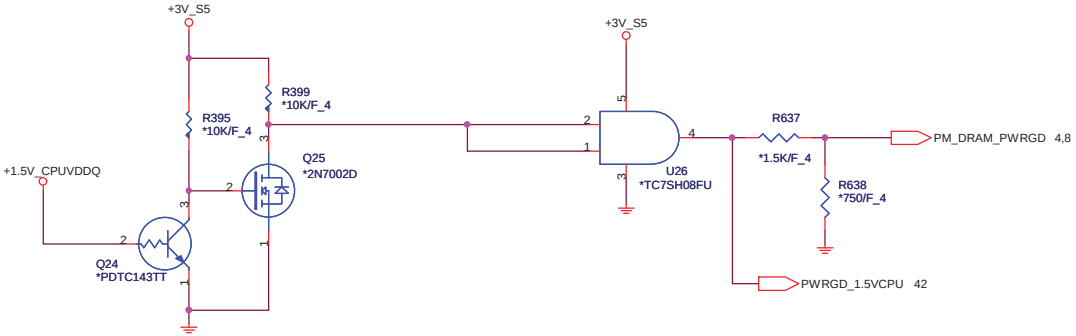
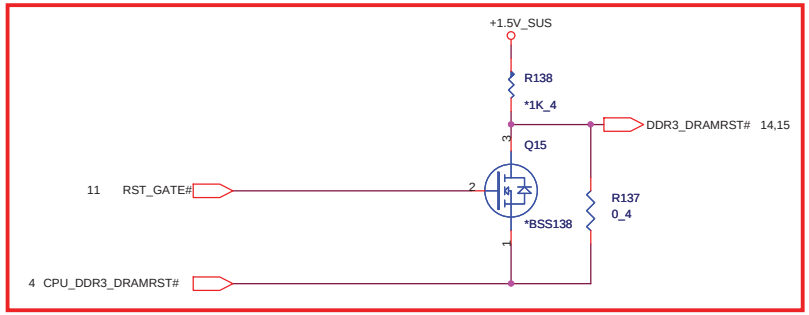
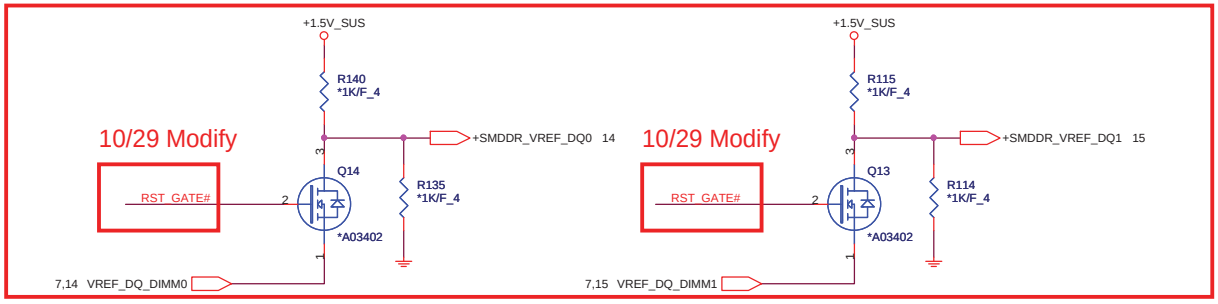
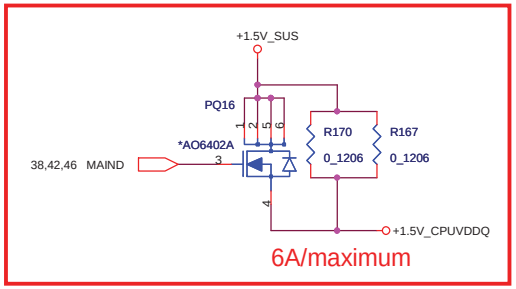
11/12 PR90,PQ22 no stuff.











Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	S3 power saving	3B
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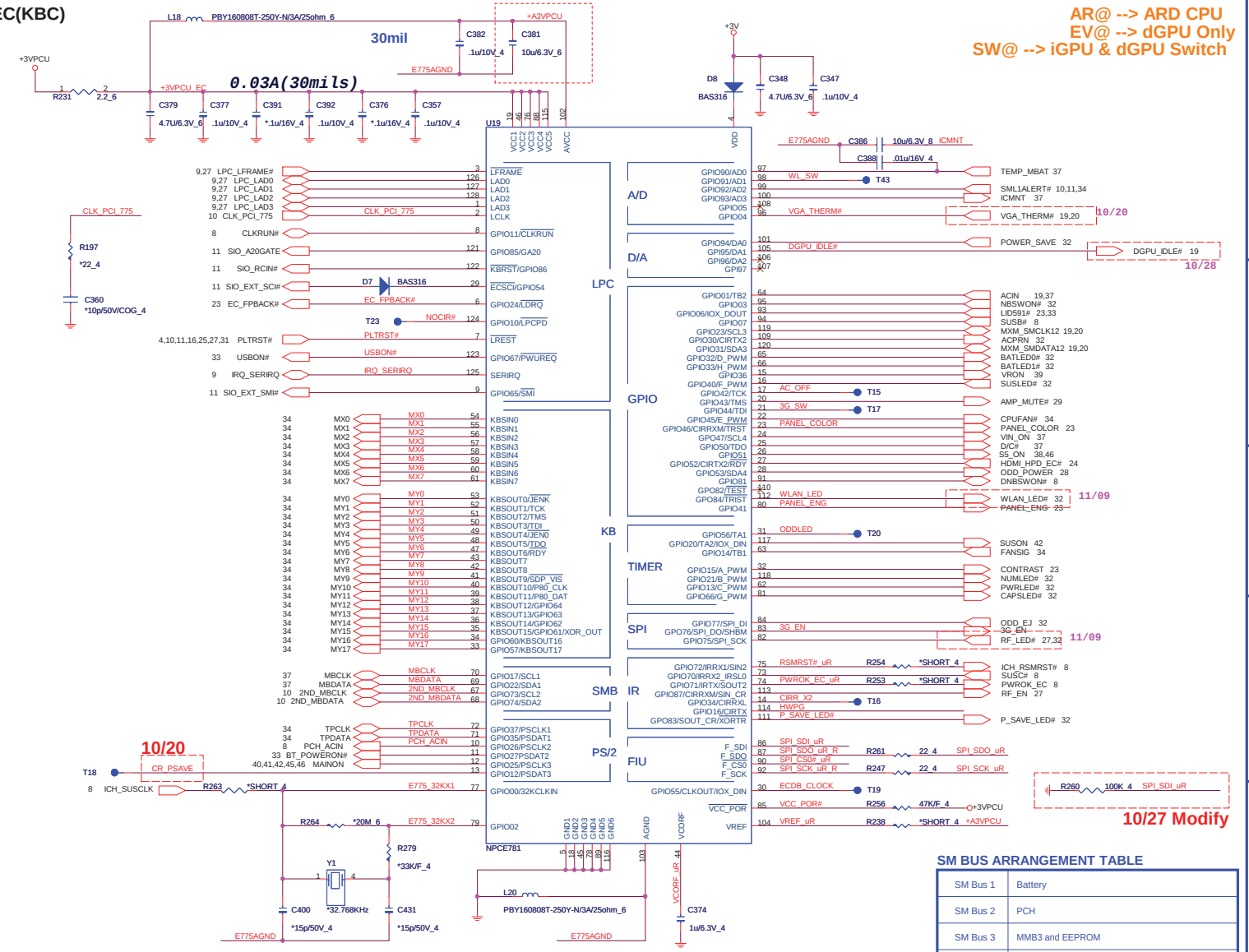
EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

SHBM — 3G_EN — R255 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

11/25 Modify unstuff.
2ND_MBCLK R249 *10K_4
2ND_MBDATA R250 *10K_4

11/25 Modify.
DGPU_IDLE# R425 SW@10K_4
VGA_THERM# R428 SW@10K_4

SW@ --> iGPU & dGPU Switch

MBCLK R252 10K_4
MBDATA R251 10K_4

11/25 Modify.
MXM_SMCLK12 R208 2.2K_4
MXM_SMDATA12 R207 2.2K_4

ODD_EJ R265 *10K_4
ODD_POWER R180 *10K_4

10/26 UnStuff

ACER ID(KBC)

8/11 modify

U22 — *ACER_ID_EEPROM
MXM_SMCLK12
MXM_SMDATA12
C417 *1u/10V_4

SPI FLASH(KBC)

12/7 Change to 512K

U21 — W25X40BVSSIG
SPI_SDI_uR R266 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
R259 10K_4
C449 .1u/10V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

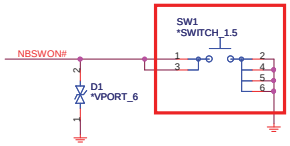
HWPG(KBC)

R217 10K_4 HWPG
R222 *SHORT_4 MPWROK_4

40,45	HWPG_VTT	D17	BAS316
45	HWPG_1.8V	D12	BAS316
41	HWPG_1.05V	D14	BAS316
42	HWPG_1.5V	D13	BAS316
38	SYS_HWPG	D15	BAS316
44	HWPG_AXF	D16	AR@BAS316
Add 11,18	dGPU_PWROK	D23	EV@BAS316

AR@ --> ARD CPU
EV@ --> dGPU Only

POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

10/26 UnStuff
MY0 R230 *10K_4 +3VPCU

Quanta Computer Inc.
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Size	Document Number	Rev
	WPCE781 & FLASH	3B

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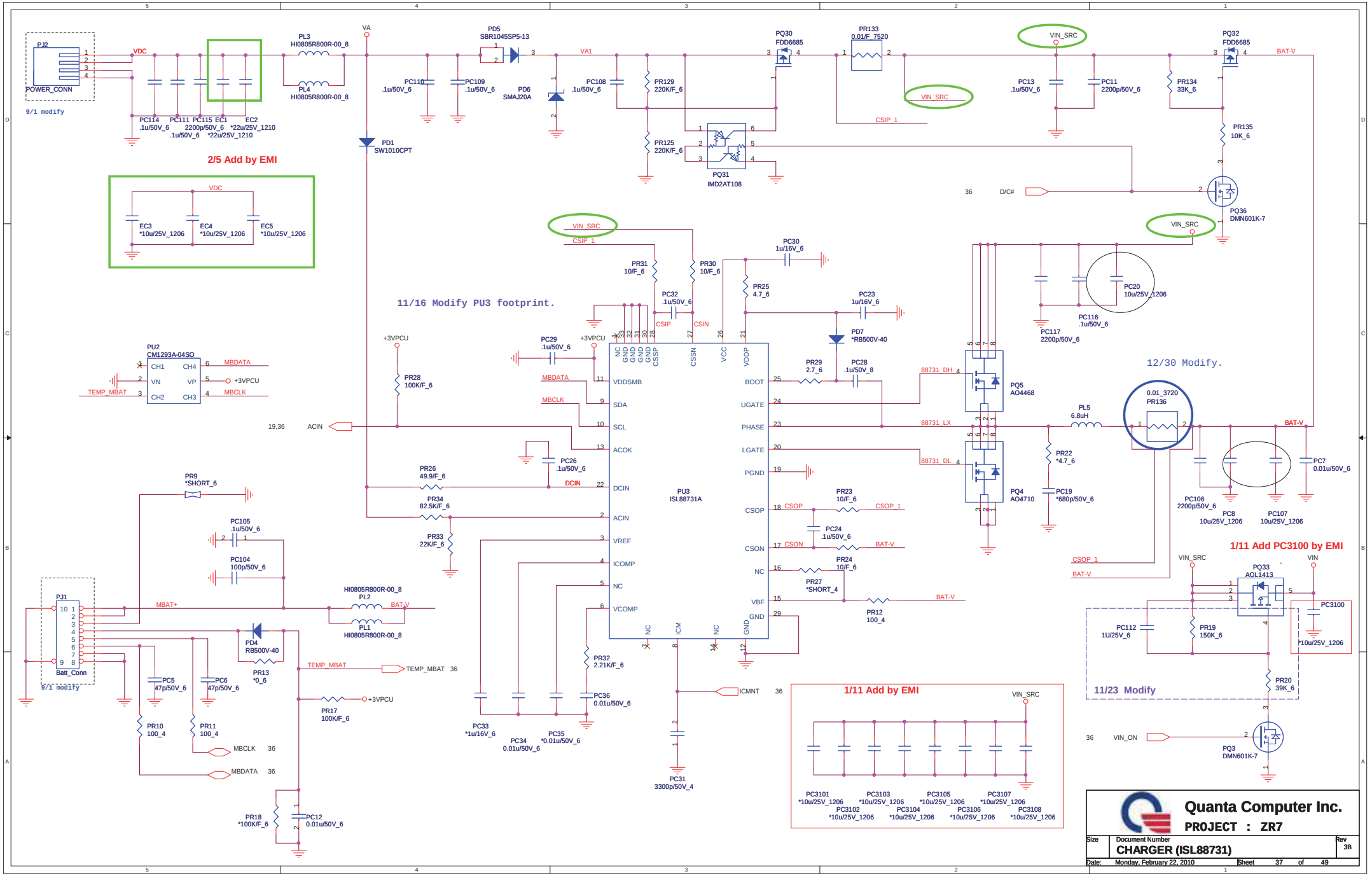
PJ2
POWER_CONN
9/1 modify
VDC
PC114 .1u/50V_6
PC111 .1u/50V_6
PC115 2200p/50V_6
EC1 *22u/25V_1210
EC2 *22u/25V_1210
2/5 Add by EMI
EC3 *10u/25V_1206
EC4 *10u/25V_1206
EC5 *10u/25V_1206
PL3 HI0805R800R-00_8
PL4 HI0805R800R-00_8
VA
PD1 SW1010CPT
PC110 .1u/50V_6
PC109 .1u/50V_6
PD5 SBR1045SP5-13
PD6 SMAJ20A
VA1
PC108 .1u/50V_6
PR129 220K/F_6
PR125 220K/F_6
PQ31 IMD2AT108
PQ30 FDD6685
PR133 0.01/F_7520
VIN_SRC
CSIP_1
PC13 .1u/50V_6
PC11 2200p/50V_6
PQ32 FDD6685
BAT-V
PR134 33K_6
PR135 10K_6
36 D/C#
PQ36 DMN601K-7
PU2 CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
11/16 Modify PU3 footprint.
PR31 10/F_6
PR30 10/F_6
PC32 .1u/50V_6
PC30 1u/16V_6
PR25 4.7_6
PC23 1u/16V_6
PD7 *RB500V-40
CSIP
CSIN
PC29 .1u/50V_6
PR28 100K/F_6
19,36 ACIN
PC26 .1u/50V_6
DCIN
PR26 49.9/F_6
PR34 82.5K/F_6
PR33 22K/F_6
PU3 ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
VDDP
CSSN
CSSP
VCC
PR29 2.7_6
PC28 .1u/50V_8
88731_DH
88731_LX
88731_DL
PQ5 AO4468
PQ4 AO4710
PL5 6.8uH
PR22 *4.7_6
PC19 *680p/50V_6
PC20 10u/25V_1206
PC116 .1u/50V_6
PC117 2200p/50V_6
12/30 Modify.
0.01_3720 PR136
PC106 2200p/50V_6
PC8 10u/25V_1206
PC107 10u/25V_1206
PC7 0.01u/50V_6
PR23 10/F_6
PC24 .1u/50V_6
PR24 10/F_6
PR27 *SHORT_4
PR12 100_4
CSOP_1
BAT-V
1/11 Add PC3100 by EMI
PQ33 AOL1413
PC3100
*10u/25V_1206
PC112 1U/25V_6
PR19 150K_6
PR20 39K_6
11/23 Modify
36 VIN_ON
PQ3 DMN601K-7
PR9 *SHORT_6
PC105 .1u/50V_6
PC104 100p/50V_6
PJ1
Batt_Conn
9/1 modify
MBAT+
HI0805R800R-00_8 PL2
PL1 HI0805R800R-00_8
PD4 RB500V-40
PR13 *0_6
TEMP_MBAT
36 TEMP_MBAT
PR17 100K/F_6
+3VPCU
PC5 47p/50V_6
PC6 47p/50V_6
PR10 100_4
PR11 100_4
MBCLK 36
MBDATA 36
PR18 *100K/F_6
PC12 0.01u/50V_6
PR32 2.21K/F_6
PC36 0.01u/50V_6
PC33 *1u/16V_6
PC34 0.01u/50V_6
PC35 *0.01u/50V_6
ICMNT 36
PC31 3300p/50V_4
1/11 Add by EMI
PC3101 *10u/25V_1206
PC3103 *10u/25V_1206
PC3105 *10u/25V_1206
PC3107 *10u/25V_1206
PC3102 *10u/25V_1206
PC3104 *10u/25V_1206
PC3106 *10u/25V_1206
PC3108 *10u/25V_1206
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
CHARGER (ISL88731)
Rev 3B
Date: Monday, February 22, 2010
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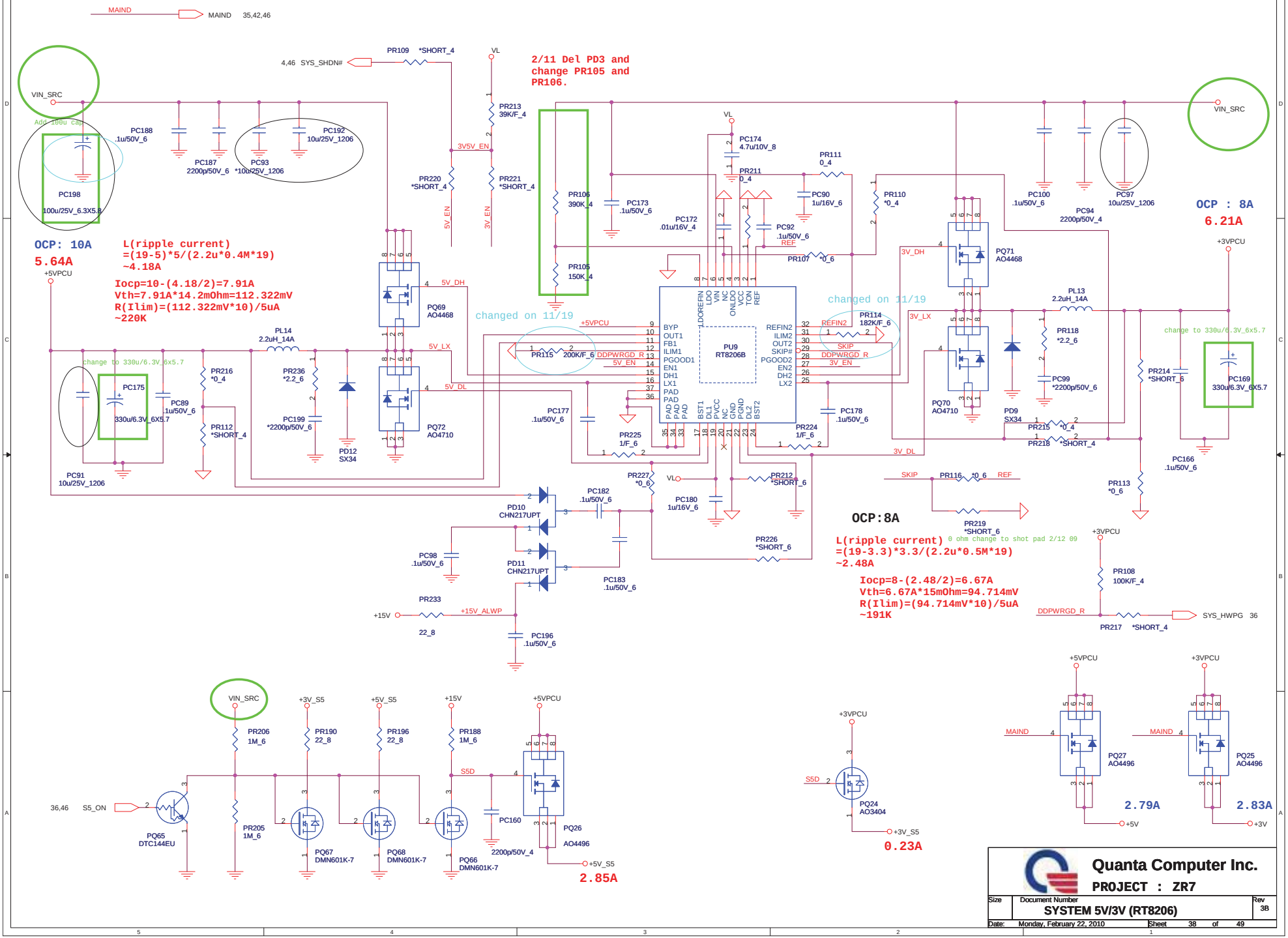
MAIND
MAIND 35,42,46
4,46 SYS_SHDN#
PR109 *SHORT_4
VL
2/11 Del PD3 and change PR105 and PR106.
VIN_SRC
Add 100u cap
PC188 .1u/50V_6
PC187 2200p/50V_6
PC93 *10u/25V_1206
PC192 10u/25V_1206
PC198 100u/25V_6.3X5.8
PR213 39K/F_4
PR221 *SHORT_4
PR220 *SHORT_4
3V5V_EN
5V EN
3V EN
PR106 390K_4
PR105 150K_4
PC173 .1u/50V_6
PC172 .01u/16V_4
PC174 4.7u/10V_8
PR211 0_4
PR111 0_4
PC90 1u/16V_6
PC92 .1u/50V_6
REF
PR107 *0_6
PR110 *0_4
PC100 .1u/50V_6
PC94 2200p/50V_4
PC97 10u/25V_1206
VIN_SRC
OCP: 10A
5.64A
L(ripple current) =(19-5)*5/(2.2u*0.4M*19) ~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
changed on 11/19
changed on 11/19
OCP : 8A
6.21A
+5VPCU
+3VPCU
PQ69 AO4468
5V_DH
5V_LX
5V_DL
PQ72 AO4710
PD12 SX34
PL14 2.2uH_14A
PR236 *2.2_6
PC199 *2200p/50V_6
PR216 *0_4
PR112 *SHORT_4
PC89 .1u/50V_6
change to 330u/6.3V_6x5.7
PC175 330u/6.3V_6X5.7
PC91 10u/25V_1206
PU9 RT8206B
LDOREFN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR115 200K/F_6
DDPWRGD_R
5V_EN
PR114 182K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
PR225 1/F_6
PC177 .1u/50V_6
PC178 .1u/50V_6
PR224 1/F_6
3V_DH
3V_LX
3V_DL
PQ71 AO4468
PQ70 AO4710
PD9 SX34
PL13 2.2uH_14A
PR118 *2.2_6
PC99 *2200p/50V_6
PR215 *0_4
PR218 *SHORT_4
PR214 *SHORT_6
change to 330u/6.3V_6x5.7
PC169 330u/6.3V_6X5.7
PC166 .1u/50V_6
PR113 *0_6
PR227 *0_6
PR212 *SHORT_6
PC182 .1u/50V_6
PC180 1u/16V_6
PD10 CHN217UPT
PD11 CHN217UPT
PC98 .1u/50V_6
PC183 .1u/50V_6
PR226 *SHORT_6
SKIP
PR116 *0_6
REF
PR219 *SHORT_6
OCP:8A
L(ripple current) 0 ohm change to shot pad 2/12 09
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR108 100K/F_4
DDPWRGD_R
PR217 *SHORT_4
SYS_HWPG 36
PR233
+15V
+15V_ALWP
22_8
PC196 .1u/50V_6
VIN_SRC
+3V_S5
+5V_S5
+15V
+5VPCU
PR206 1M_6
PR190 22_8
PR196 22_8
PR188 1M_6
S5D
36,46 S5_ON
PR205 1M_6
PQ65 DTC144EU
PQ67 DMN601K-7
PQ68 DMN601K-7
PQ66 DMN601K-7
PC160 2200p/50V_4
PQ26 AO4496
+5V_S5
2.85A
+3VPCU
S5D
PQ24 AO3404
+3V_S5
0.23A
+5VPCU
+3VPCU
MAIND
PQ27 AO4496
2.79A
+5V
MAIND
PQ25 AO4496
2.83A
+3V
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 3B
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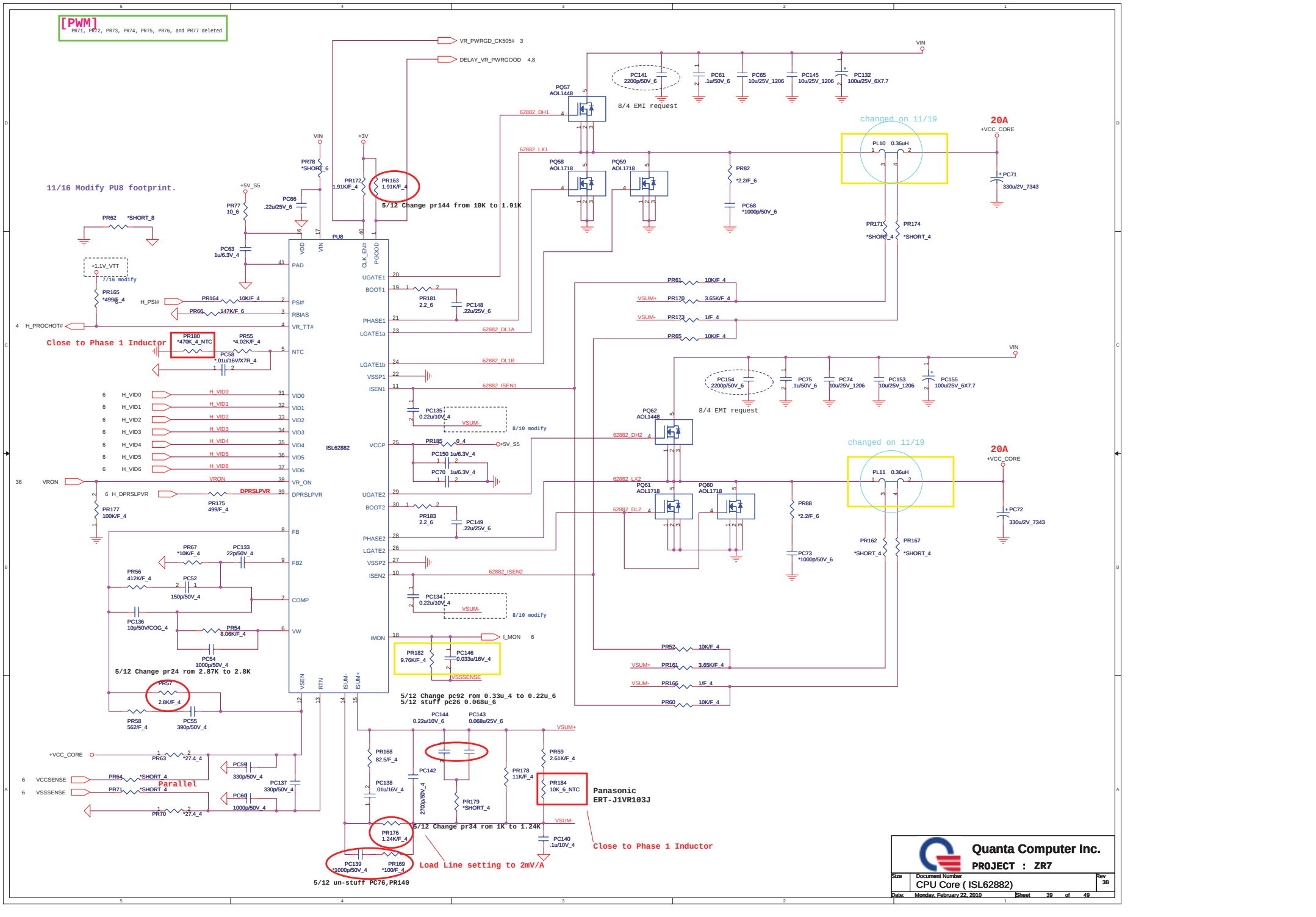
[PWM]
PR71, PR72, PR73, PR74, PR75, PR76, and PR77 deleted
VR_PWRGD_CK505# 3
DELAY_VR_PWRGOOD 4,8
VIN
+3V
+5V_S5
PU8
ISL62882
11/16 Modify PU8 footprint.
5/12 Change pr144 from 10K to 1.91K
PR78 *SHORT_6
PR172 1.91K/F_4
PR163 1.91K/F_4
PC66 .22u/25V_6
PR77 10_6
PC63 1u/6.3V_4
PR62 *SHORT_8
+1.1V_VTT
7/16 modify
PR165 *499/F_4
PR164 10K/F_4
PR166 147K/F_6
H_PSI#
H_PROCHOT#
Close to Phase 1 Inductor
PR180 *470K_4_NTC
PR55 *4.02K/F_4
PC58 *.01u/16V/X7R_4
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
VRON
DPRSLPVR
PR177 100K/F_4
PR175 499/F_4
PR67 *10K/F_4
PC133 22p/50V_4
PR56 412K/F_4
PC52 150p/50V_4
PC136 10p/50V/COG_4
PR54 8.06K/F_4
PC54 1000p/50V_4
5/12 Change pr24 rom 2.87K to 2.8K
PR57 2.8K/F_4
PR58 562/F_4
PC55 390p/50V_4
+VCC_CORE
PR63 *27.4_4
PC59 330p/50V_4
PC137 330p/50V_4
PR64 *SHORT_4
PR71 *SHORT_4
Parallel
PC60 1000p/50V_4
PR70 *27.4_4
VCCSENSE
VSSSENSE
PC135 0.22u/10V_4
PC134 0.22u/10V_4
VSUM-
8/10 modify
PR185 0_4
PC150 1u/6.3V_4
PC70 1u/6.3V_4
PR182 9.76K/F_4
PC146 0.033u/16V_4
I_MON 6
VSSSENSE
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
PC144 0.22u/10V_6
PC143 0.068u/25V_6
PR168 82.5/F_4
PC142 2700p/50V_4
PC138 .01u/16V_4
PR178 11K/F_4
PR179 *SHORT_4
PR59 2.61K/F_4
PR184 10K_6_NTC
Panasonic
ERT-J1VR103J
5/12 Change pr34 rom 1K to 1.24K
PR176 1.24K/F_4
PC140 .1u/10V_4
PC139 *1000p/50V_4
PR169 *100/F_4
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140
Close to Phase 1 Inductor
PQ57 AOL1448
PQ58 AOL1718
PQ59 AOL1718
PQ62 AOL1448
PQ61 AOL1718
PQ60 AOL1718
62882_DH1
62882_LX1
62882_DL1A
62882_DL1B
62882_ISEN1
62882_DH2
62882_LX2
62882_DL2
62882_ISEN2
PC141 2200p/50V_6
PC61 .1u/50V_6
PC65 10u/25V_1206
PC145 10u/25V_1206
PC132 100u/25V_6X7.7
8/4 EMI request
changed on 11/19
20A
+VCC_CORE
PL10 0.36uH
PL11 0.36uH
PR82 *2.2/F_6
PC68 *1000p/50V_6
PR88 *2.2/F_6
PC73 *1000p/50V_6
PC71 330u/2V_7343
PC72 330u/2V_7343
PR171 *SHORT_4
PR174 *SHORT_4
PR162 *SHORT_4
PR167 *SHORT_4
PR61 10K/F_4
PR170 3.65K/F_4
PR173 1/F_4
PR65 10K/F_4
PR52 10K/F_4
PR161 3.65K/F_4
PR166 1/F_4
PR60 10K/F_4
PC154 2200p/50V_6
PC75 .1u/50V_6
PC74 10u/25V_1206
PC153 10u/25V_1206
PC155 100u/25V_6X7.7
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
CPU Core (ISL62882)
Rev 3B
Date: Monday, February 22, 2010
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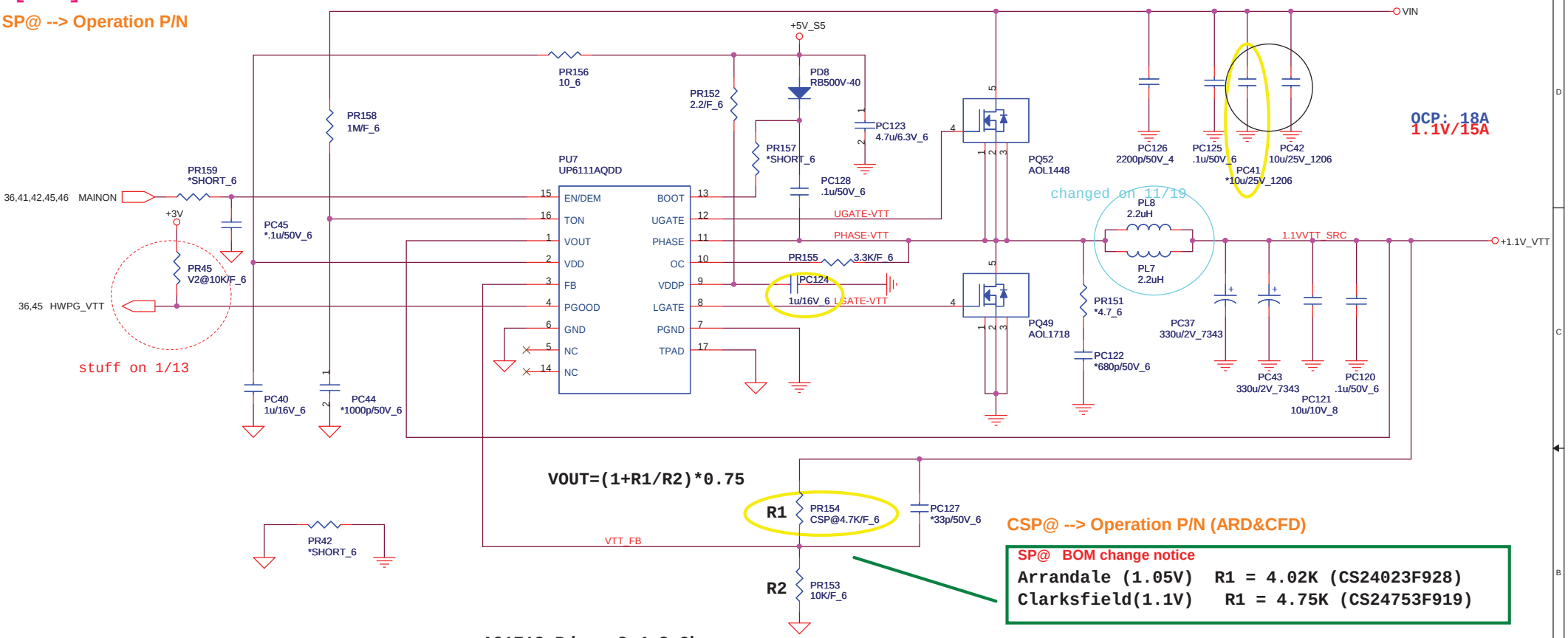
[PWM]

SP@ --> Operation P/N



CSP@ --> Operation P/N (ARD&CFD)

SP@ BOM change notice

Arrandale (1.05V) R1 = 4.02K (CS24023F928)

Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

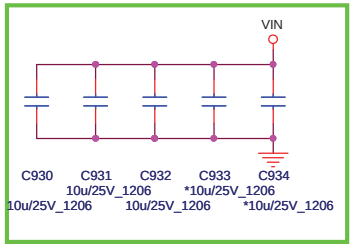
Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA

RILIM=3.87K --- 3.92K



2/11 Add C930~C934 by monitor test.

Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	+VTT (UP6111A)	3B

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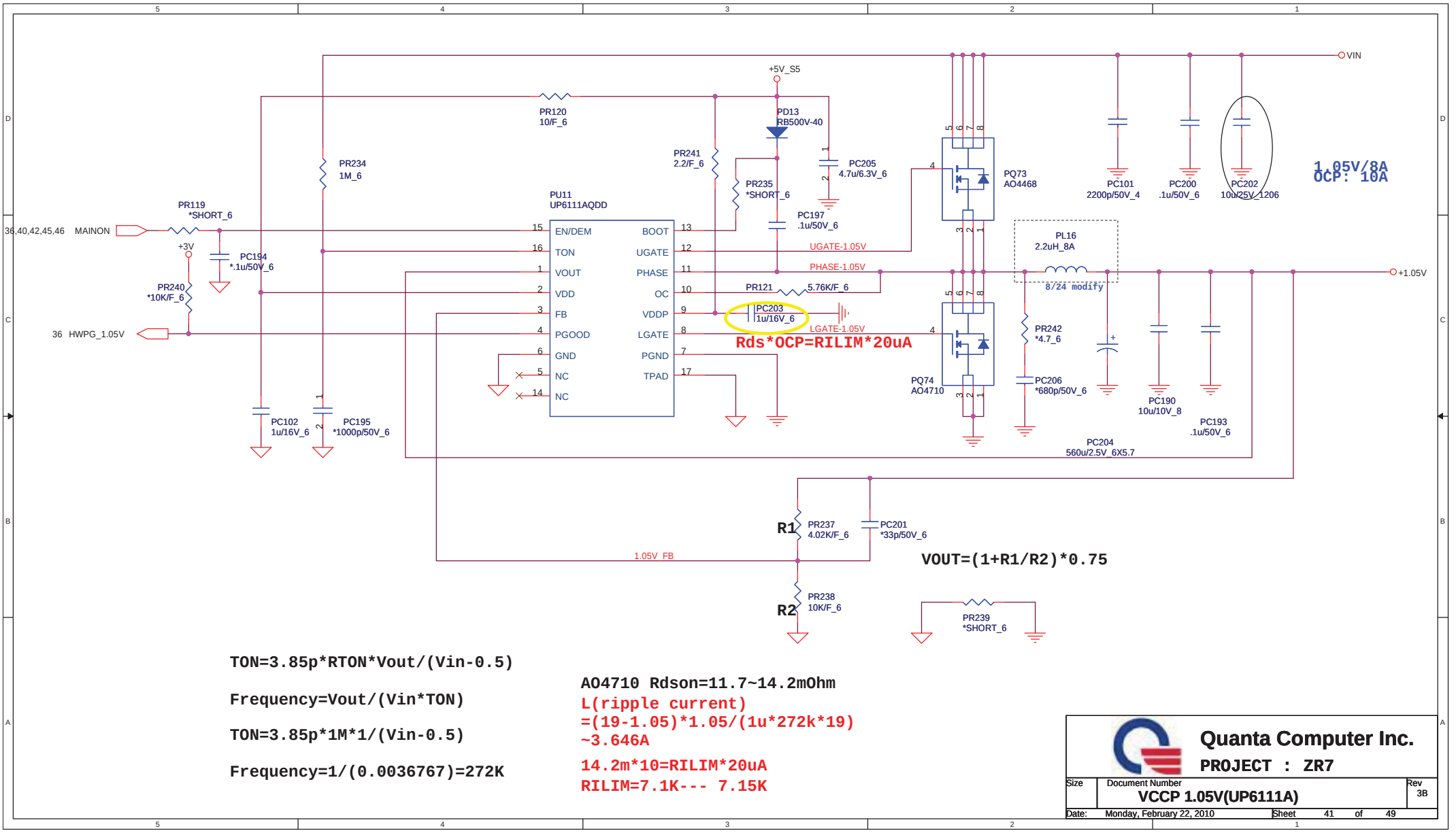

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

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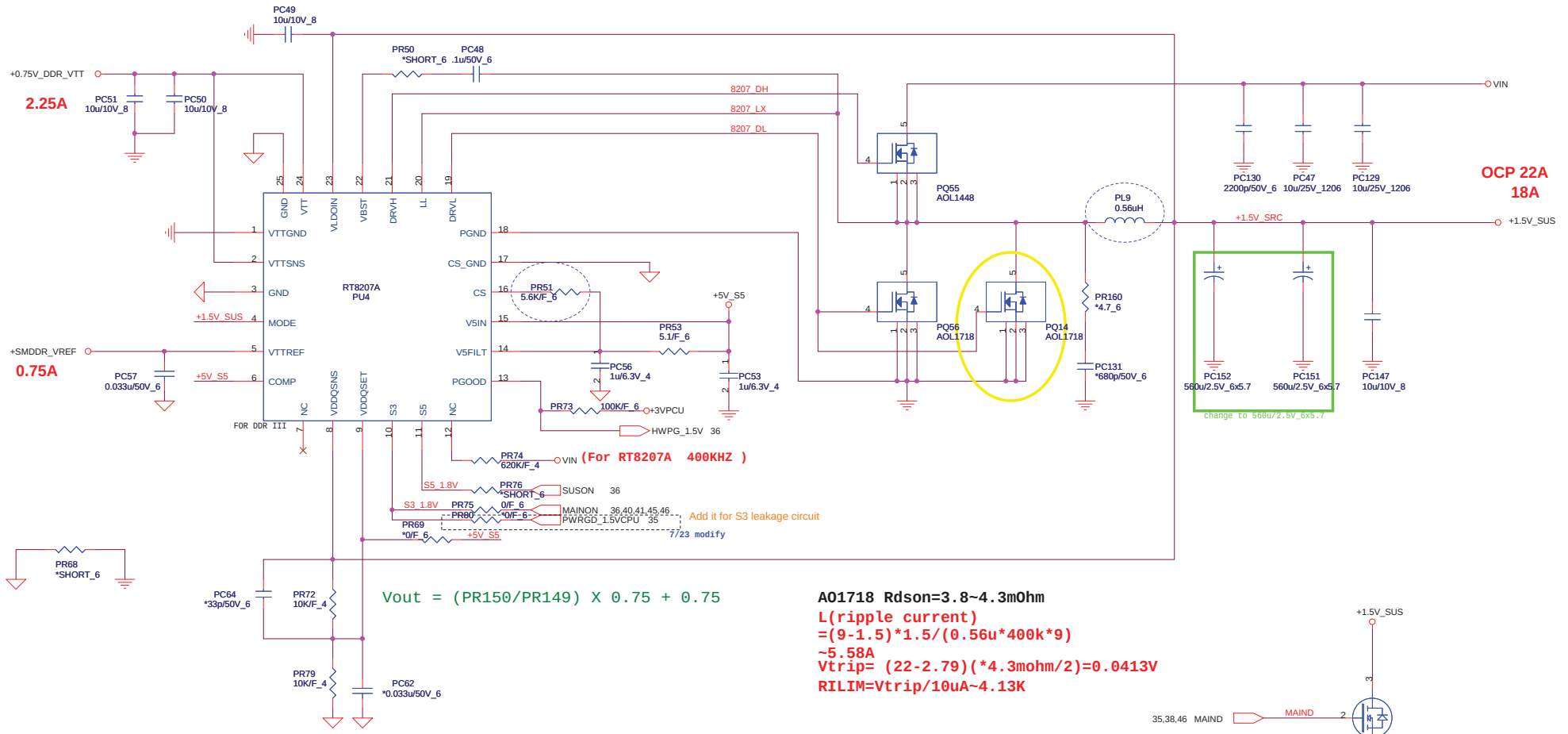
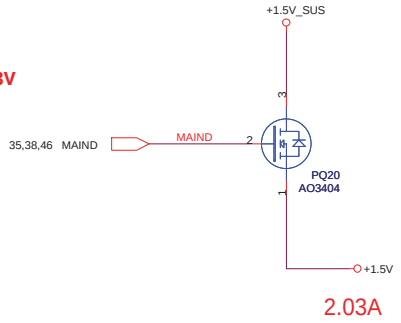
[PWM]



Vout = (PR150/PR149) X 0.75 + 0.75

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K



	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	OFF	ON	ON
S4/S5	0	0	OFF	OFF	OFF

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	DDR III 1.5V(TPS51116)	3B
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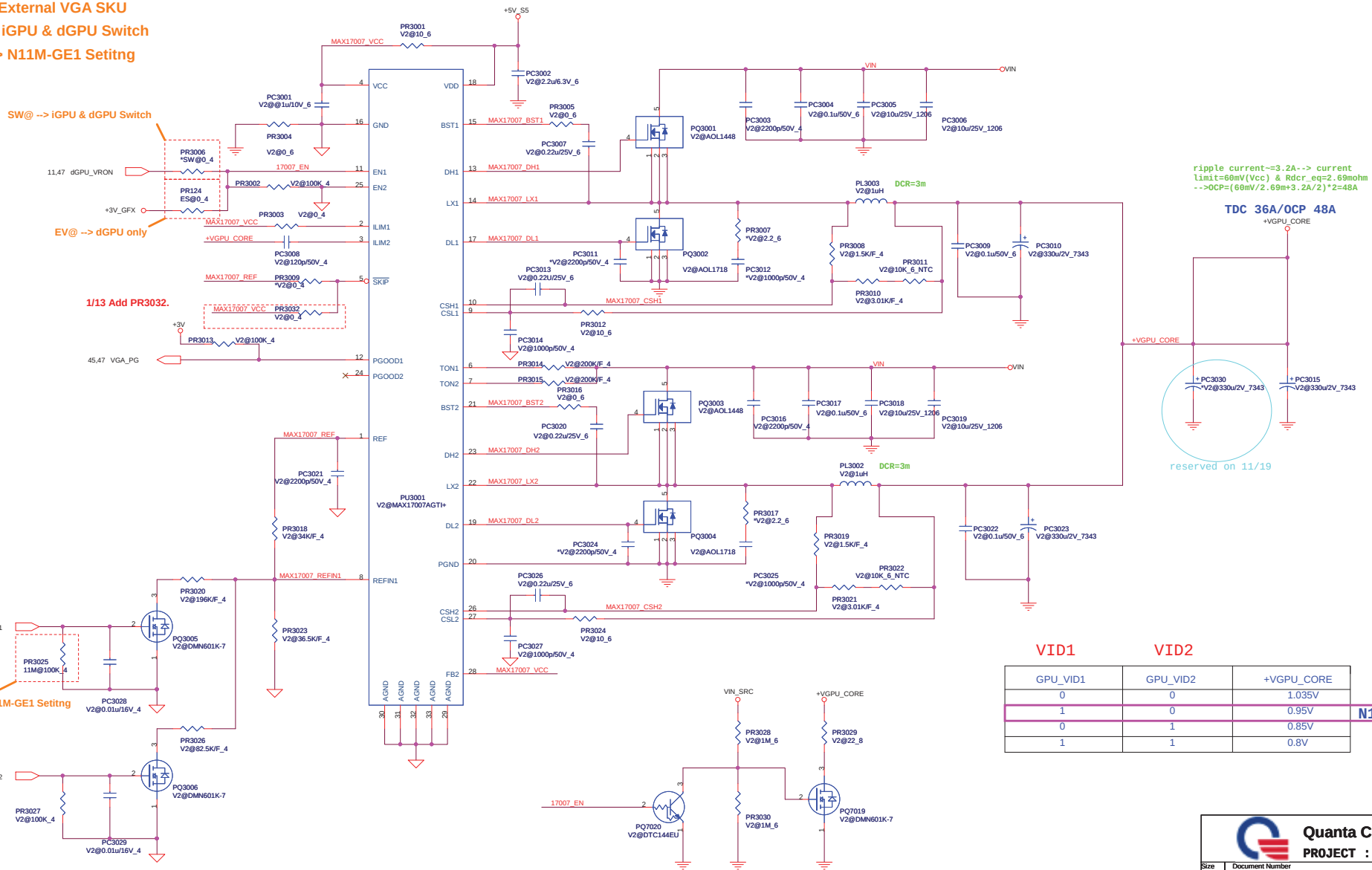
V2@ --> Two Phase dGPU only

EV@ --> External VGA SKU

SW@ --> iGPU & dGPU Switch

11M@ --> N11M-GE1 Setitng

11/16 Change VGPU_CORE to two phase solution.



ripple current~=3.2A--> current limit=60mV(Vcc) & Rdcr_eq=2.69mohm
-->OCP=(60mV/2.69m+3.2A/2)*2=48A

TDC 36A/OCP 48A

reserved on 11/19

VID1 VID2

GPU_VID1	GPU_VID2	+VGPU_CORE	
0	0	1.035V	
1	0	0.95V	N11E/N11P
0	1	0.85V	
1	1	0.8V	

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Size	Document Number	Rev
	GPU CORE(MAX17007)	3B

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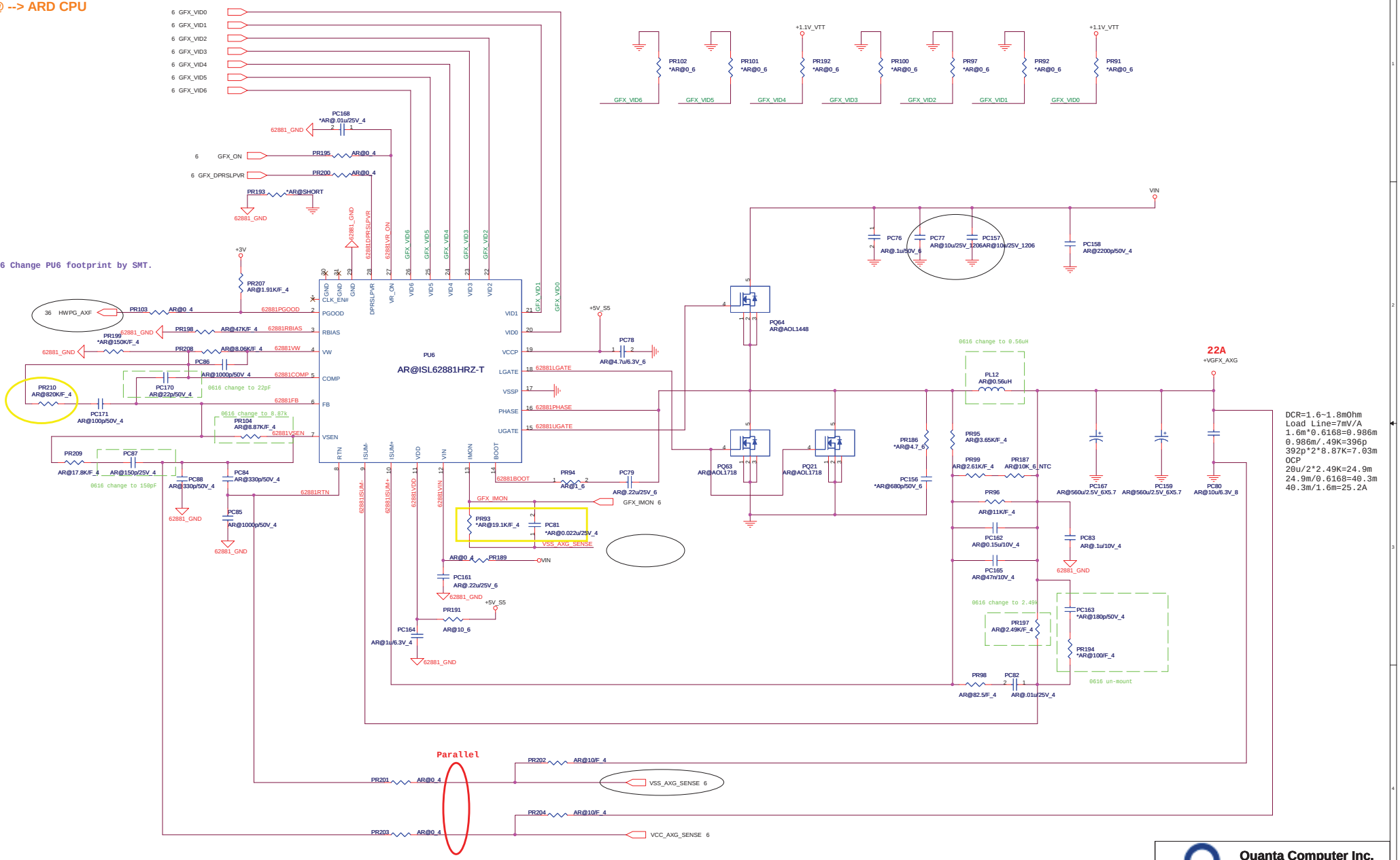
Int_VGA [PWM]

AR@ --> ARD CPU



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	3B
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ES@ --> External VGA SKU
SW@ --> iGPU & GPU Switch

1A

+3VPCU
PC185 10u/10V_8
PC96 0.1u/25V_4
PU10 HPA00835RTER
VIN PH BOOT PWRGD GND RT/CLK SS AGND VSNS COMP EN
11/16 Change PL15 footprint.
DCR(max)=10mohm
PL15 1uH_7X7X3
+1.8V
PR117 *SHORT_4
MAINON
PR223 *SHORT_6
PC179 .1u/50V_6
54418-1.8_VFB
PC176 1000p/50V_4
HWPG_1.8V 36
PR232 51.1/F_4
R1
PR231 100K/F_4
PC181 0.1u/25V_4
PC95 10u/10V_8
PC184 10u/10V_8
PR228 15K/F_4
PR230 182K/F_4
PR222 100K/F_4
+3V
PC189 *100P/50V_4
PC186 .01u/25V_4
MAINON 36,40,41,42,46
PC191 1200p/50V_4
R2
PR229 78.7K/F_4
V0=0.8*(R1+R2)/R2

2A

+5V
5V_LCD
PC3110 V2@10u/10V_8
PC3111 V2@0.1u/25V_4
PU3002 V2@HPA00835RTER
DCR(max)=10mohm
PL3005 V2@1uH_4X4X2
PR3033 V2@0_4
HWPG_VTT
PR3034 V2@0_6
PC3112/2@.1u/50V_6
54418-1.8_VFB_1
HWPG_5V_LCD
PC3113 V2@1000p/50V_4
PR3035 V2@51.1/F_4
R1
PR3038 V2@100K/F_4
PC3114 V2@0.1u/25V_4
PC3115 V2@10u/10V_8
PC3116 V2@10u/10V_8
PR3036 V2@30.1K/F_4
PR3037 V2@182K/F_4
PR3039 *V2@100K/F_4
+3V
PC3117 *V2@100P/50V_4
PC3118 V2@.01u/25V_4
HWPG_VTT HWPG_VTT 36,40
PC3119 V2@1000p/50V_4
5V_LCD 5V_LCD 23
R2
PR3040 V2@26.7K/F_4
V0=0.8*(R1+R2)/R2

1/13 Add 3D LCD power circuit.

11/19 Del 3G power circuit.

VIN_SRC
+1.5V_GFX
+1.8V_GFX
+15V
+1.8V
PR47 ES@1M/F_6
PR46 ES@22_8
PR36 ES@22_8
PR49 ES@1M/F_6
dGPU_D1
PQ53 ES@AO3404
+1.8V_GFX
0.23A(Max0.3A)
10/19
43,47 VGA_PG
PR44 ES@0_4
PR40 ES@1M/F_6
PQ12 ES@DMN601K-7
PQ8 ES@DMN601K-7
PQ13 ES@DMN601K-7
PC46 *ES@2200p/50V_4
PC38 ES@1u/10V_4
PQ11 ES@DTC144EU
+1.5V_SUS
dGPU_D1
PQ50 ES@AO4468
+1.5V_GFX
4.28A(Max5.72A)

VIN_SRC
+3V_GFX
+1.05V_GFX
+15V
+1.05V
+3VPCU
PR38 ES@1M/F_6
PR48 ES@22_8
PR37 ES@22_8
PR43 ES@1M/F_6
dGPU_D
PQ54 ES@AO4468
+1.05V_GFX
2.87A(Max 3.83A)
dGPU_D
PQ51 ES@AO3404
+3V_GFX
1.04A(Max1.38A)
11/12
MAINON
PR243 EV@0_4
PR244 SW@0_4
11 dGPU_PWR_EN
PR39 ES@1M/F_6
PQ9 ES@DMN601K-7
PQ6 ES@DMN601K-7
PQ10 ES@DMN601K-7
PC39 *ES@2200p/50V_4
PQ7 ES@DTC144EU
10/19
PR35 SW@100K_4
SW@ --> iGPU & GPU Switch

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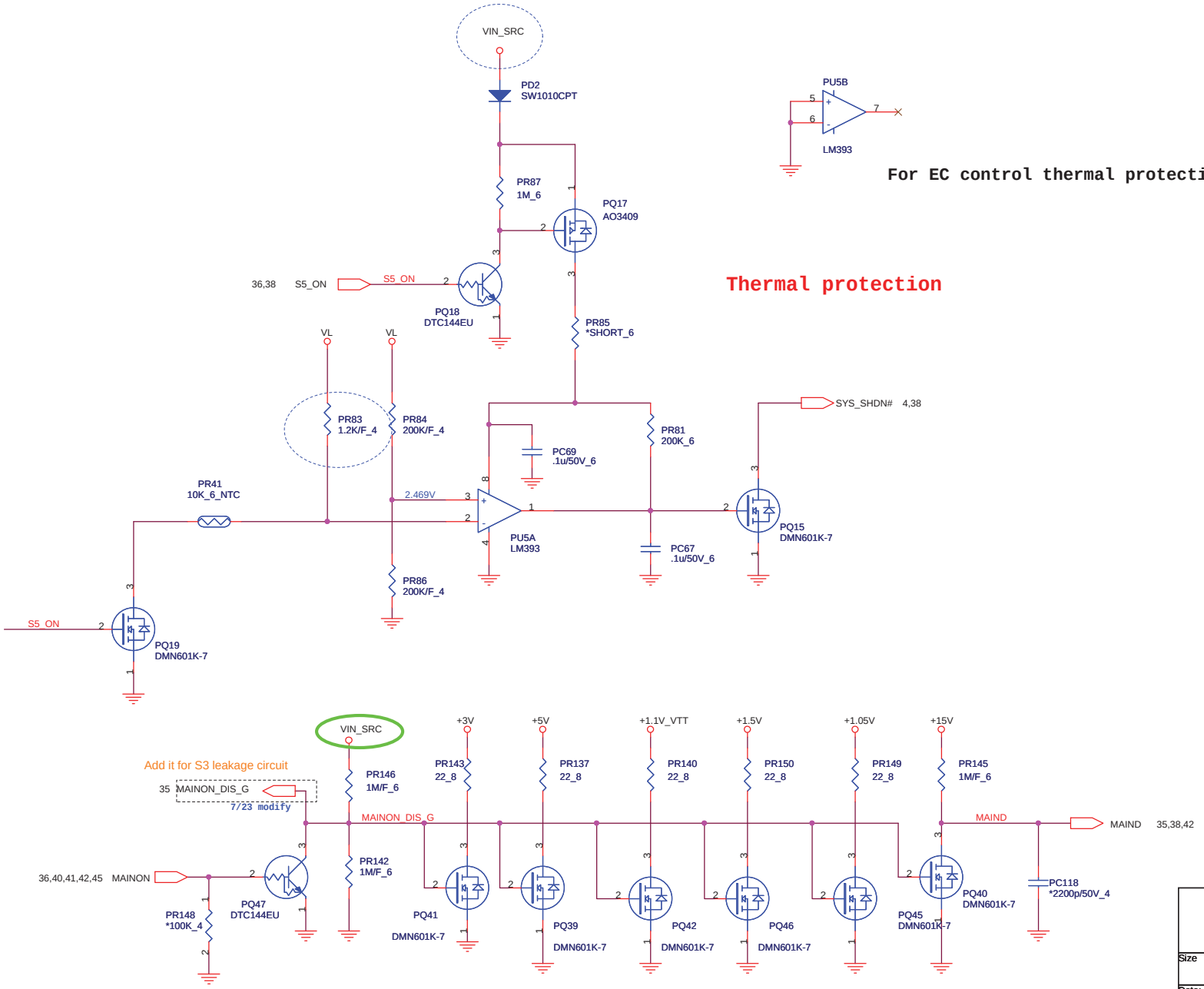

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PROJECT : ZR7

Size	Document Number	Rev
	Thermal Protection	3B
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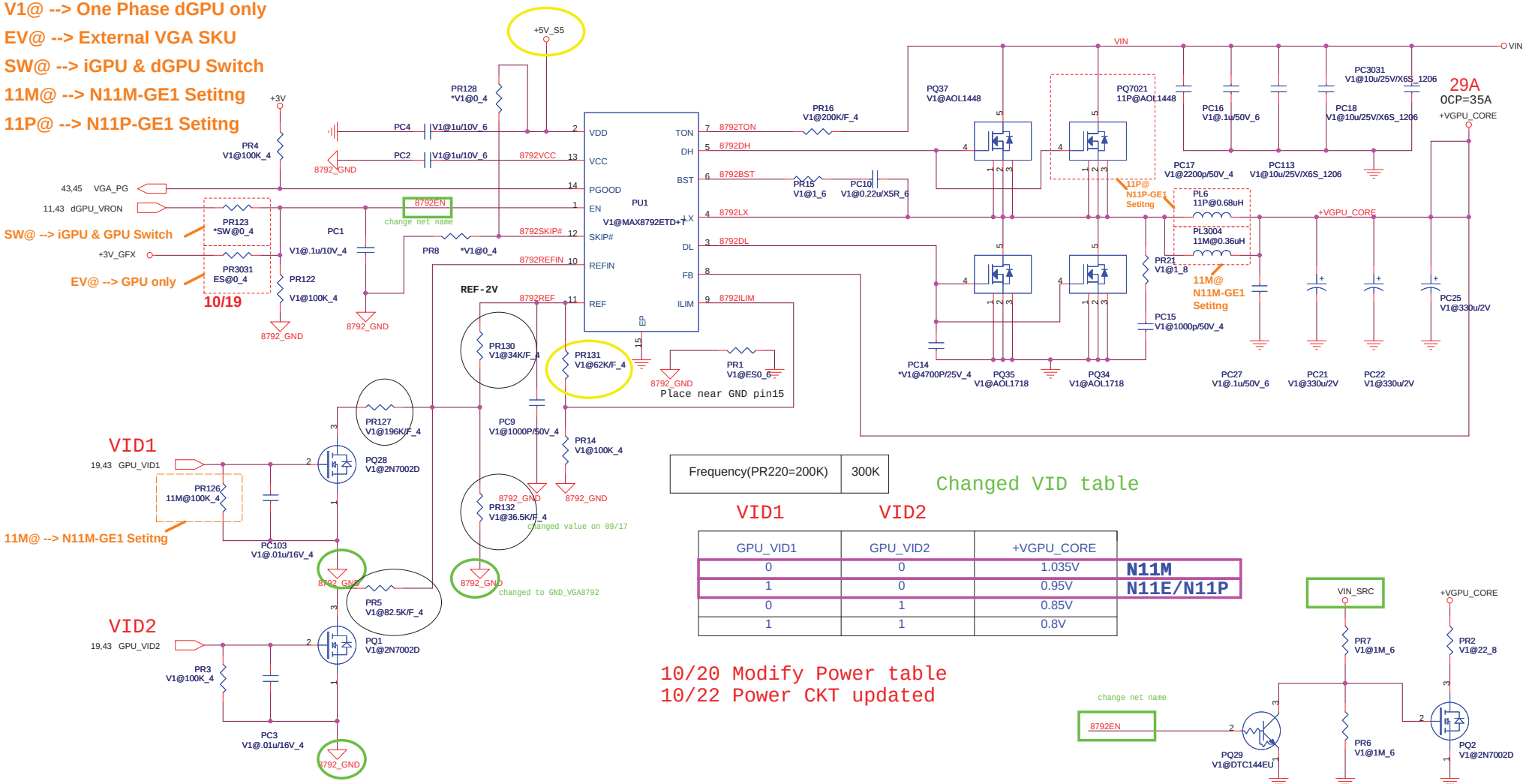
V1@ --> One Phase dGPU only
EV@ --> External VGA SKU
SW@ --> iGPU & dGPU Switch
11M@ --> N11M-GE1 Setitng
11P@ --> N11P-GE1 Setitng



Frequency(PR220=200K)	300K

Changed VID table

VID1 VID2

GPU_VID1	GPU_VID2	+VGPU_CORE	
0	0	1.035V	N11M
1	0	0.95V	N11E/N11P
0	1	0.85V	
1	1	0.8V	

10/20 Modify Power table
10/22 Power CKT updated

Quanta Computer Inc.
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Size	Document Number	Rev
	GPU CORE(MAX8792)	3B
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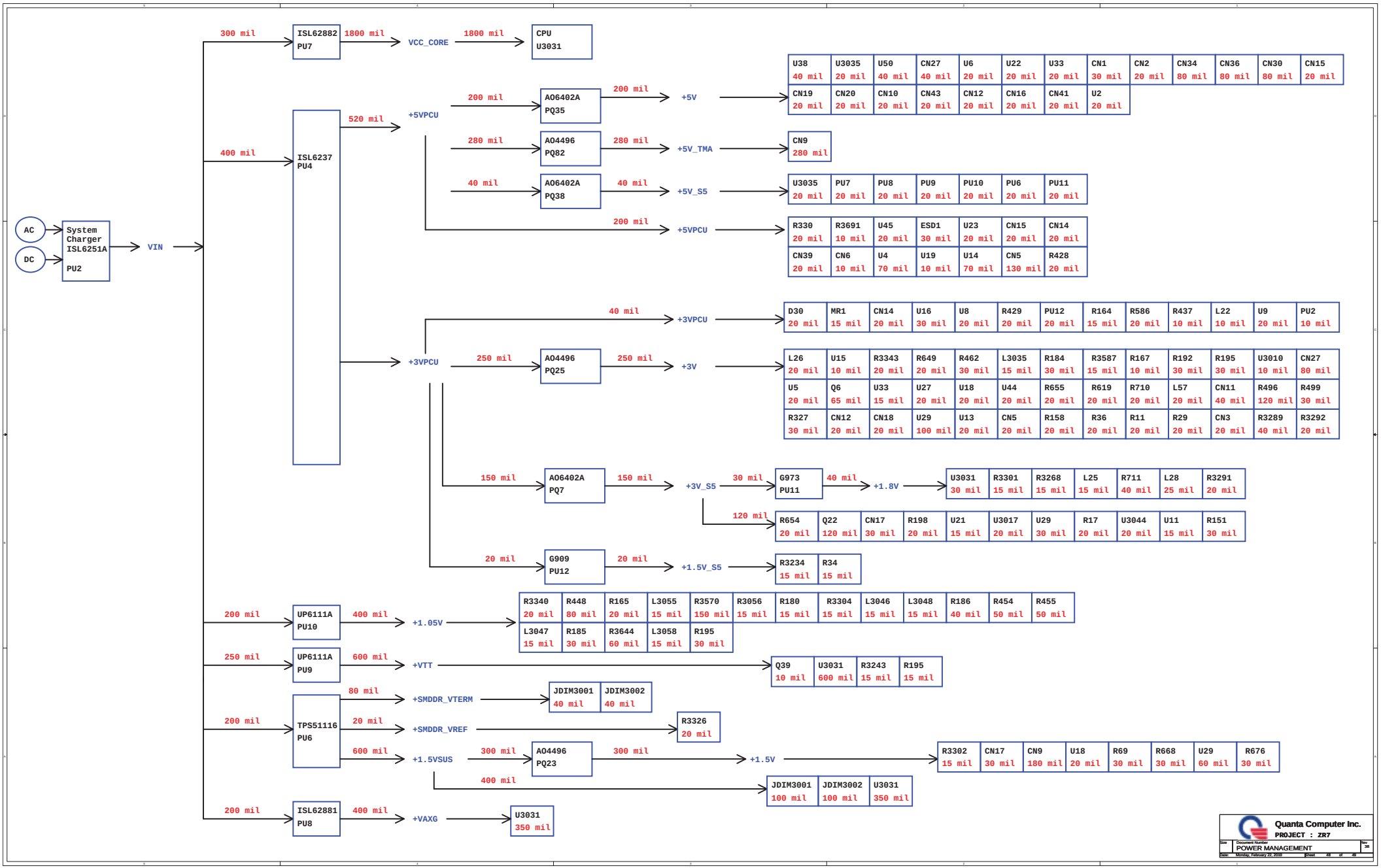
AC
DC
System Charger ISL6251A
PU2
VIN
300 mil
ISL62882 PU7
1800 mil
VCC_CORE
1800 mil
CPU U3031
400 mil
ISL6237 PU4
520 mil
+5VPCU
200 mil
AO6402A PQ35
200 mil
+5V
U38 40 mil
U3035 20 mil
U50 40 mil
CN27 40 mil
U6 20 mil
U22 20 mil
U33 20 mil
CN1 30 mil
CN2 20 mil
CN34 80 mil
CN36 80 mil
CN30 80 mil
CN15 20 mil
CN19 20 mil
CN20 20 mil
CN10 20 mil
CN43 20 mil
CN12 20 mil
CN16 20 mil
CN41 20 mil
U2 20 mil
280 mil
AO4496 PQ82
280 mil
+5V_TMA
CN9 280 mil
40 mil
AO6402A PQ38
40 mil
+5V_S5
U3035 20 mil
PU7 20 mil
PU8 20 mil
PU9 20 mil
PU10 20 mil
PU6 20 mil
PU11 20 mil
200 mil
+5VPCU
R330 20 mil
R3691 10 mil
U45 20 mil
ESD1 30 mil
U23 20 mil
CN15 20 mil
CN14 20 mil
CN39 20 mil
CN6 10 mil
U4 70 mil
U19 10 mil
U14 70 mil
CN5 130 mil
R428 20 mil
40 mil
+3VPCU
D30 20 mil
MR1 15 mil
CN14 20 mil
U16 30 mil
U8 20 mil
R429 20 mil
PU12 20 mil
R164 15 mil
R586 20 mil
R437 10 mil
L22 10 mil
U9 20 mil
PU2 10 mil
+3VPCU
250 mil
AO4496 PQ25
250 mil
+3V
L26 20 mil
U15 10 mil
R3343 20 mil
R649 20 mil
R462 30 mil
L3035 15 mil
R184 30 mil
R3587 15 mil
R167 10 mil
R192 30 mil
R195 30 mil
U3010 10 mil
CN27 80 mil
U5 20 mil
Q6 65 mil
U33 15 mil
U27 20 mil
U18 20 mil
U44 20 mil
R655 20 mil
R619 20 mil
R710 20 mil
L57 20 mil
CN11 40 mil
R496 120 mil
R499 30 mil
R327 30 mil
CN12 20 mil
CN18 20 mil
U29 100 mil
U13 20 mil
CN5 20 mil
R158 20 mil
R36 20 mil
R11 20 mil
R29 20 mil
CN3 20 mil
R3289 40 mil
R3292 20 mil
150 mil
AO6402A PQ7
150 mil
+3V_S5
30 mil
G973 PU11
40 mil
+1.8V
U3031 30 mil
R3301 15 mil
R3268 15 mil
L25 15 mil
R711 40 mil
L28 25 mil
R3291 20 mil
120 mil
R654 20 mil
Q22 120 mil
CN17 30 mil
R198 20 mil
U21 15 mil
U3017 20 mil
U29 30 mil
R17 20 mil
U3044 20 mil
U11 15 mil
R151 30 mil
20 mil
G909 PU12
20 mil
+1.5V_S5
R3234 15 mil
R34 15 mil
200 mil
UP6111A PU10
400 mil
+1.05V
R3340 20 mil
R448 80 mil
R165 20 mil
L3055 15 mil
R3570 150 mil
R3056 15 mil
R180 15 mil
R3304 15 mil
L3046 15 mil
L3048 15 mil
R186 40 mil
R454 50 mil
R455 50 mil
L3047 15 mil
R185 30 mil
R3644 60 mil
L3058 15 mil
R195 30 mil
250 mil
UP6111A PU9
600 mil
+VTT
Q39 10 mil
U3031 600 mil
R3243 15 mil
R195 15 mil
200 mil
TPS51116 PU6
80 mil
+SMDDR_VTERM
JDIM3001 40 mil
JDIM3002 40 mil
20 mil
+SMDDR_VREF
R3326 20 mil
600 mil
+1.5VSUS
300 mil
AO4496 PQ23
300 mil
+1.5V
R3302 15 mil
CN17 30 mil
CN9 180 mil
U18 20 mil
R69 30 mil
R668 30 mil
U29 60 mil
R676 30 mil
400 mil
JDIM3001 100 mil
JDIM3002 100 mil
U3031 350 mil
200 mil
ISL62881 PU8
400 mil
+VAXG
U3031 350 mil
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POWER MANAGEMENT
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Model	REV	CHANGE LIST	MODEL ZR7 FROM	MODEL ZR7 To
ZR7 MB	2A	11/2 Page33 Change CN10 P/N by PDC.	1A	2A
		11/5 Page9 change R338 and R594 to 10K ohm by checklist.	1A	2A
		11/5 Page10 Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.	1A	2A
		11/5 Page12 un-stuff R318 and del C499 and add R698 contact VCCLAN to GND by checklist.	1A	2A
		11/9 Page32 change W/L LED signal to control by EC.	1A	2A
		11/9 Page36 Add EC pin82/112 for W/L LED control by EC.	1A	2A
		11/12 Page35 PR90,PQ22 no stuff.	1A	2A
		11/12 Page45 Add PR243,PR244 for option.	1A	2A
		11/16 Page23 CN5 Add LVDS signal to two channel and change CN3 to 8pin conn.	1A	2A
		11/16 Page43 GPU VCORE power change to two phase solution.	1A	2A
		11/16 Page27 Add CN12 8pin conn for Touch Screen by ME.	1A	2A
		11/16 Page44 Change PU6 footprint by SMT.	1A	2A
		11/16 Page45 Change PL15 footprint to CHOKE-PCMC063T-3R3MN-NB4 by SMT.	1A	2A
		11/16 Page39 Change PU8 footprint to qfn40-5x5-4-41p-0_75h-smt by SMT.	1A	2A
		11/16 Page37 Change PU3 footprint to QFN28-5X5-5-33P-SMT by SMT.	1A	2A
		11/18 Page10 Delete R597, C444,C445 for cancel 3G function.	1A	2A
		11/18 Page30 R368,R393 modify from 47ohm to 56ohm by Realtek.	1A	2A
		11/18 Page10 Change BOARD_ID0~2 to BOARD_ID1~3.	1A	2A
		11/18 Page11 Change GPIO7 to BOARD_ID0 and reserve R439 PD.	1A	2A
		11/18 Page36 Add D23 to connect to dGPU_PWROK on EV sku.	1A	2A
		11/18 Page9 Change P/N follow ZR7B that use right angle connector.	1A	2A
		11/18 Page27 Reserve C919, CN22 for NV IR signals on B-test.	1A	2A
		11/19 Page3 Change U39 PN to AL003197002 by vendor.	1A	2A
		11/19 Page31 Change CN9 footprint & P/N follow ZR7B.	1A	2A
		11/19 Page27 Add R697 for WI-FI.	1A	2A
		11/19 Page11 Add R442, R440 to dGPU_PWROK_R and stuff R321 on EV sku.	1A	2A
		11/19 Page23 Modify CN5 pin define.	1A	2A
		11/20 Page43 Add PR124 on EV sku.	1A	2A
		11/20 Page12~14 Change core logic cap .1uF CH41003ZB35 to CH4102K1B03 by SMT.	1A	2A
		11/20 Page45 del 3G power circuit.	1A	2A
		11/20 Page34 del HOLE10,Add HOLE5,HOLE6,HOLE7,HOLE8,HOLE11,HOLE12,HOLE14,HOLE15,HOLE17,HOLE18,HOLE20,HOLE24,HOLE25,HOLE26,HOLE30 P/N	1A	2A
		11/25 Page10 Q26,Q29 change to unstuff , Add R700,R701 0 ohm for S3 leakage	1A	2A
		11/25 Page20 C151 change to CC7343 package	1A	2A
		11/25 Page34 Change HOLE8,HOLE12 footprint to H-C236D142P2 , Change HOLE5,HOLE7,HOLE11 footprint to H-TC197D122PT , Change HOLE14,HOLE15,HOLE17,HOLE18 footprint to H-TC236D142PT , Change HOLE20,HOLE24,HOLE26 footprint to H-TC236D162PT , Change HOLE9 footprint to O-ZR7-1-B	1A	2A
		11/25 Page36 R425 change to DGPU_IDLE# signal and value to SW SKU , R428 change value to SW SKU , R249,R250 change to unstuff	1A	2A
		11/25 Page28 Add C920,C921,C923,C924 0.1uF for EMI	1A	2A
		11/25 Page33 L31 SWAP for Layout House	1A	2A
		11/25 Page27 Modify LTRST#_7726 net name to PLTRST#	1A	2A
		11/26 Page33 Change L19/L25 footprint , Stuff L25 common choke & unstuff R301,R302 by EMI	1A	2A
		11/26 Page23 Change L2 footprint	1A	2A
		11/26 Page23 Change R589,R590 to FLITER for EMI	1A	2A
		11/26 Page28 Add C925,C926,C927 for EMI	1A	2A
		11/26 Page11 Modify R422 Value to IV@ SKU	1A	2A
		11/27 Page11 Del R440	1A	2A
		11/27 Page20 C81,C105 change CC0603 package	1A	2A
		11/27 Page16 C84,C109 change CC0603 package	1A	2A
		11/27 Page23 Add CN5 pin45 to GND	1A	2A
		11/27 Page27 Add L46,L47,R702,R703,R704,R705 by EMI	1A	2A
		11/27 Page10 Modify C699,C703 to 27pF	1A	2A
		11/27 Page18 Modify C601,C600 to 27pF	1A	2A
		12/1 Page27 Modify CN12 to 6 pin connector	1A	2A
		12/1 Page32 Modify LED3 & Add R706,R707 PD by EC ODD_EJ & POWER_SAVE	1A	2A
		12/1 Page9 Add R708,R709 by SPI ROM	1A	2A
	3A	12/18 Page32 Add R710,R711,Q57 by EC.	2A	3A
		12/18 Page23 Add R712,R713 by 3D feature.	2A	3A
		12/18 Page47 Change PL6 footprint to choke-mpl136-2r2-smt by SMT.	2A	3A
		12/29 Page27 Change CN21 footprint to MIPCI-800055FB052GX00pl-52P-smt by SMT.	2A	3A
		12/29 Page23 Add F1 by safety.	2A	3A
		12/29 Page24 Change Q16, Q45 P/N & add F2 by HMDI submit and safety; del U15, U16, U18.	2A	3A
		12/29 Page30 Change CN19 color to black P/N: DFTJ08FR130 by ACER.	2A	3A
		1/5 Page33 Change CN17 footprint to USB-UB111GC-RABED-7F-4P-R-V-SMT by PDC.	2A	3A
		1/7 Page23 Change Q12 of dGPU_select# signal design by leakage issue.	2A	3A
		1/7 Page9 Change BT1 P/N to DFHD02MS784 by ME issue.	2A	3A
		1/8 Page27 Change CN12,CN22 6pin conn footprint for Touch Screen and IR.	2A	3A
		1/11 Page23 Add L48 & stuff L2 and un-stuff R28 and R29 by EMI.	2A	3A
		1/11 Page24 Add C928 by EMI.	2A	3A
		1/13 Page12,36 Change C711,C382 to 10U 6.3V.	2A	3A
		1/14 Page23 Change LVDS connector Pin4 define from NC to LCDVCC & add J3 by 3D PWR.	2A	3A
		1/14 Page28 Change C218,C678 to 10U/10V_8 and footprint 0805.	2A	3A
	3B	2/3 Page 16~22 Change U33 footprint to fcbga973-nvidia-n11p-es-a1 by NV.	3A	3B
		2/3 Page 30 Change R368,R393 to 75ohm.	3A	3B
	2A	Power modify:	1A	2A
		11/19 Take out JP12, JP9, JP5, JP6, JP7, JP19, JP20, JP8, JP10, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.	1A	2A
		11/19 Page38 Change PC198 value; change PR114 from 191K to 182K, PR115 from 220K to 200K,PR106 from 100K to 1K,PR105 from 200K to 150K.	1A	2A
		11/19 Page40 Change PL7,PL8 from 1.0uH to 2.2uH.	1A	2A
		11/19 Page39 Change PL10,PL11 from DC+36T0M000 to CV+18V0MZ04.	1A	2A
		11/19 Page43 Reserve PC3030.	1A	2A
		11/23 Page37 PR19 change to 150K , PR20 change to 39K , PC112 change to 1U 25V	1A	2A
	3A	12/29 Page47 Change PL7,PL8,PL15,PL16 footprint to CHOKE-PCMC063T-3R3MN-SMT by SMT.	2A	3A
		12/29 Page37 Change PR136 footprint to RC3720-SMT by SMT.	2A	3A
		1/5 Page37~48 Change footprint from CHOKE-ETQP4LR36WFC to CHOKE-ETQP4LR36WFC-SMT by PDC.	2A	3A
		1/11 Page37 Add PC3100~PC3109 by EMI.	2A	3A
		1/11 Page47 Change value of PQ7021,PL6,PL3004 by BOM.	2A	3A
		1/13 Page43 Reserve PR3032 by PWR.	2A	3A
		1/13 Page45 Reserve circuit of LCDVCC by PWR.	2A	3A
	3B	2/10 Page37 Reserve EC1~EC5 by EMI.	3A	3B
		2/11 Page38 Del PD3 by power.	3A	3B
		2/11 Page40 Add C930~C934 by monitor test.	3A	3B
			3A	3B

Quanta Computer Inc. PROJECT : ZR7	DOC NO.	PROJECT MODEL : ZR7	APPROVED BY:	DATE:	2009/11/06
Size: Document Number: Change list2 Rev: 3B		PART NUMBER:	DRAWING BY:	REVISON:	1A
Date: Monday, February 29, 2009 Sheet 49 of 49					