

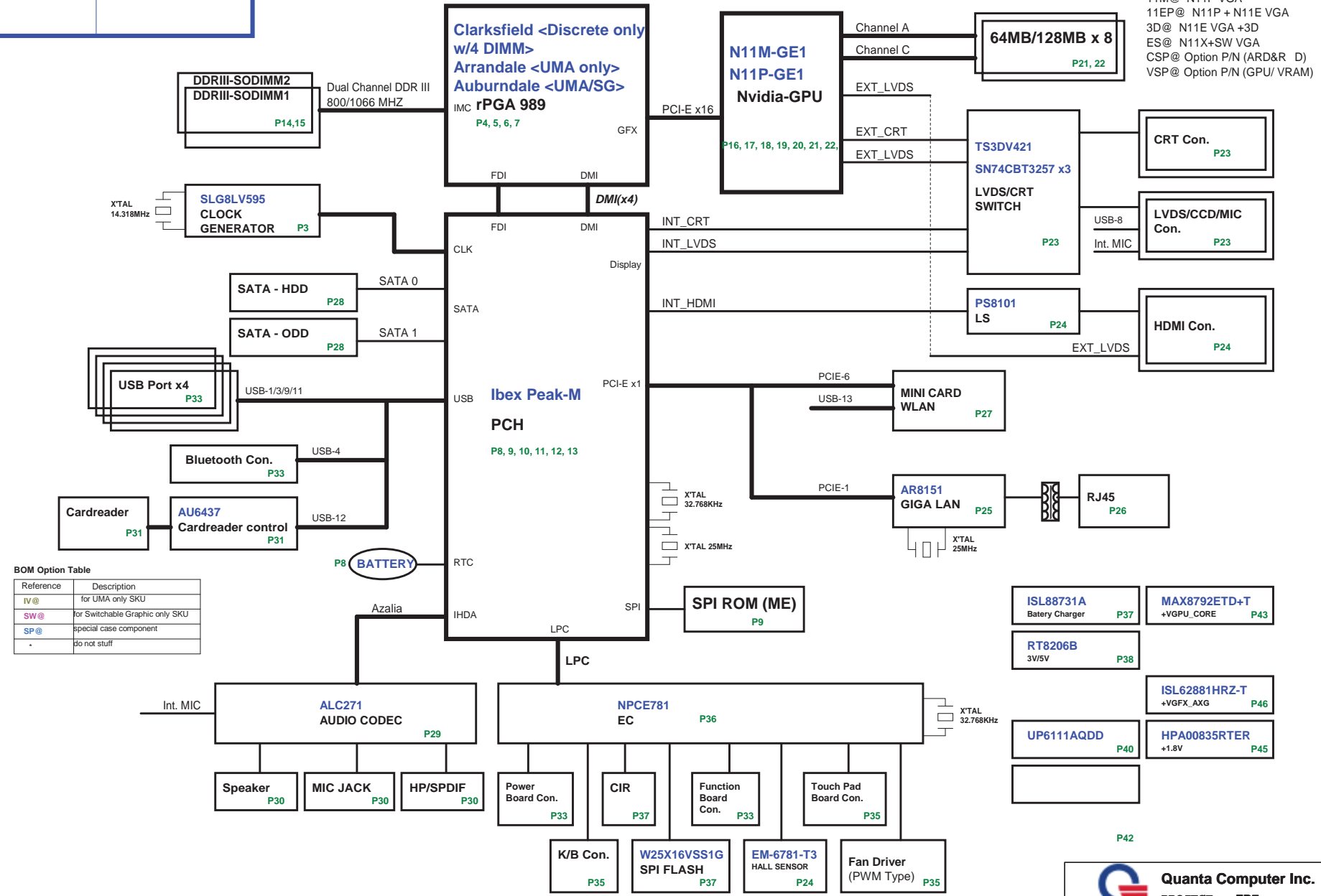
VER : 1A

# ZR7 SYSTEM BLOCK DIAGRAM

## BOM MARK

IV@ INT VGA  
 EV@ DISCRETE  
 SW@ SW VGA  
 11P@ N11P VGA  
 11M@ N11P VGA  
 11EP@ N11P + N11E VGA  
 3D@ N11E VGA +3D  
 ES@ N11X+SW VGA  
 CSP@ Option P/N (ARD&R D)  
 VSP@ Option P/N (GPU/ VRAM)

BOM P/N	Description



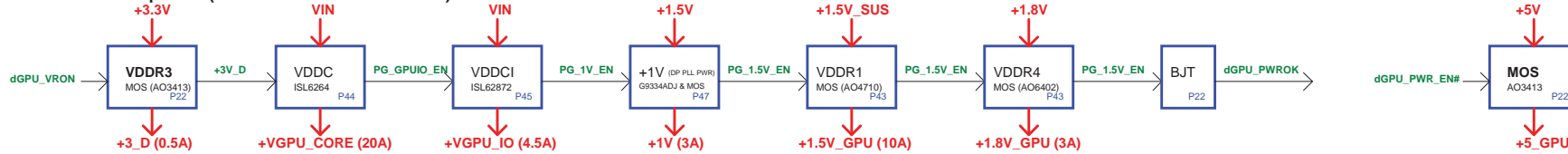
**BOM Option Table**

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU
SP@	special case component
.	do not stuff

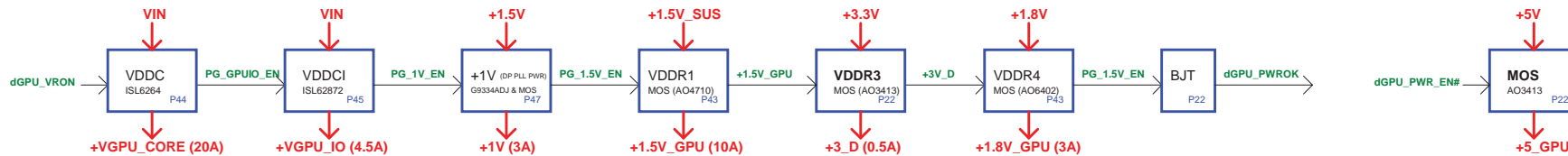
- ISL88731A** Battery Charger P37
- MAX8792ETD+T** +VGPU\_CORE P43
- RT8206B** 3V/5V P38
- ISL62881HRZ-T** +VGFX\_AXG P46
- UP6111AQDD** P40
- HPA00835RTER** +1.8V P45

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 Block Diagram  
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**GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)**



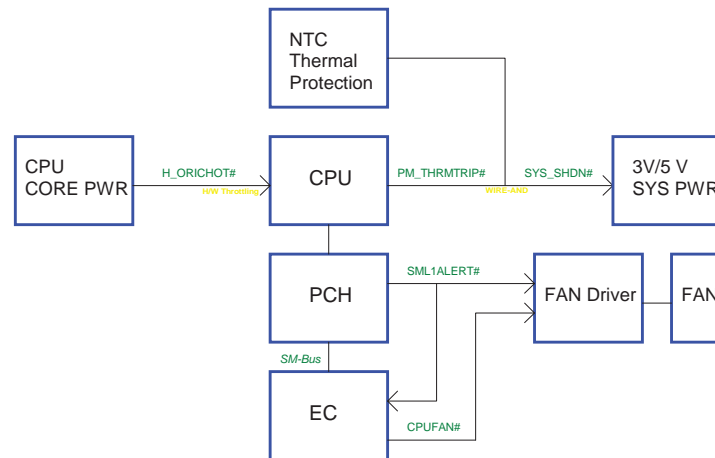
**GPU PWR CTRL Option 2 (VDDR3 after VDDR1)**



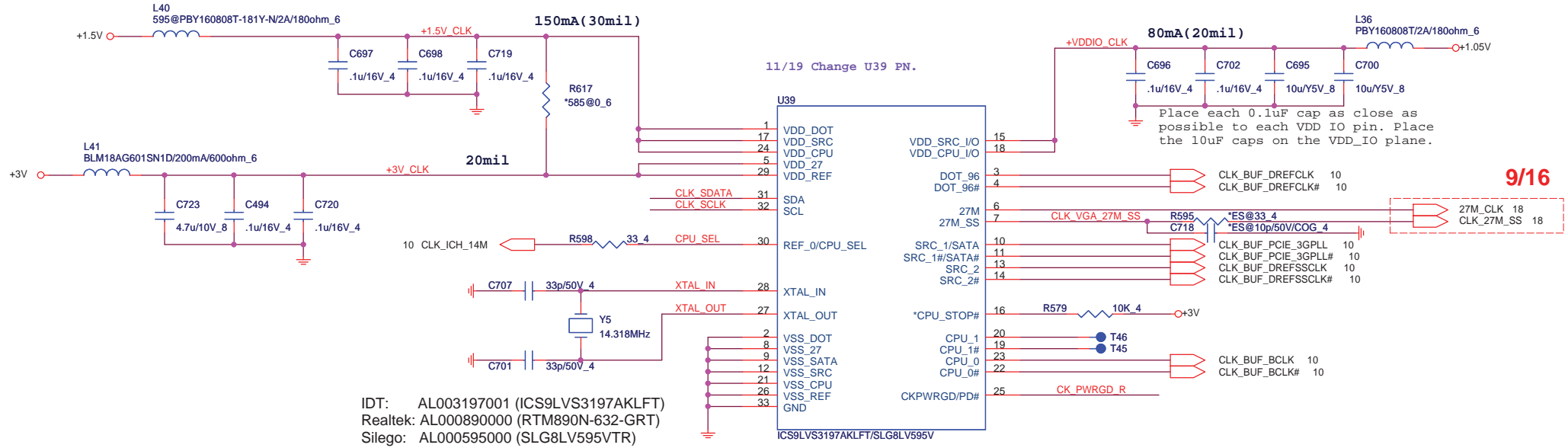
**Power States**

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

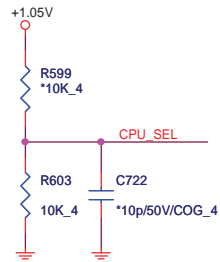
**Thermal Follow Chart**



# CLK GEN.

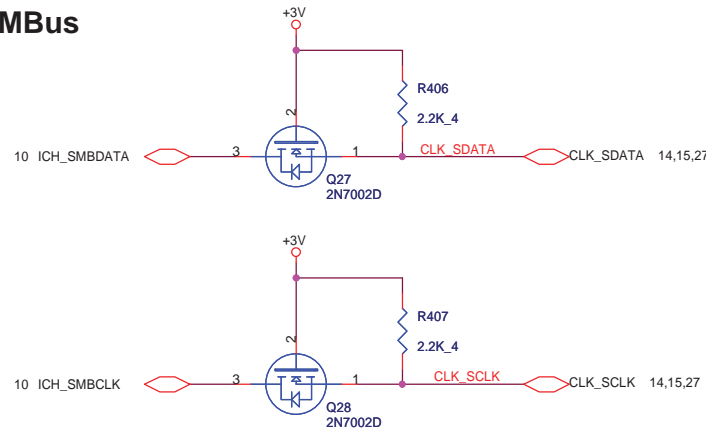


## CPU\_CLK select

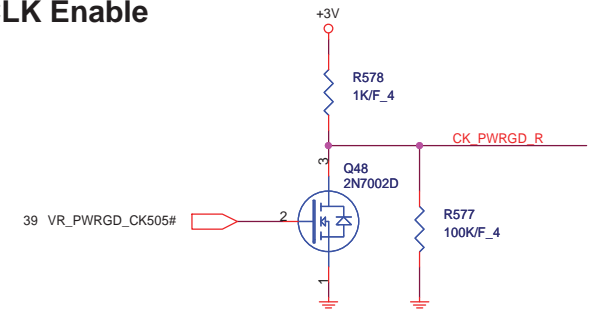



CPU_SEL	0	1
CPU0/1=133MHz (default)		CPU0/1=100MHz

## SMBus



## CLK Enable





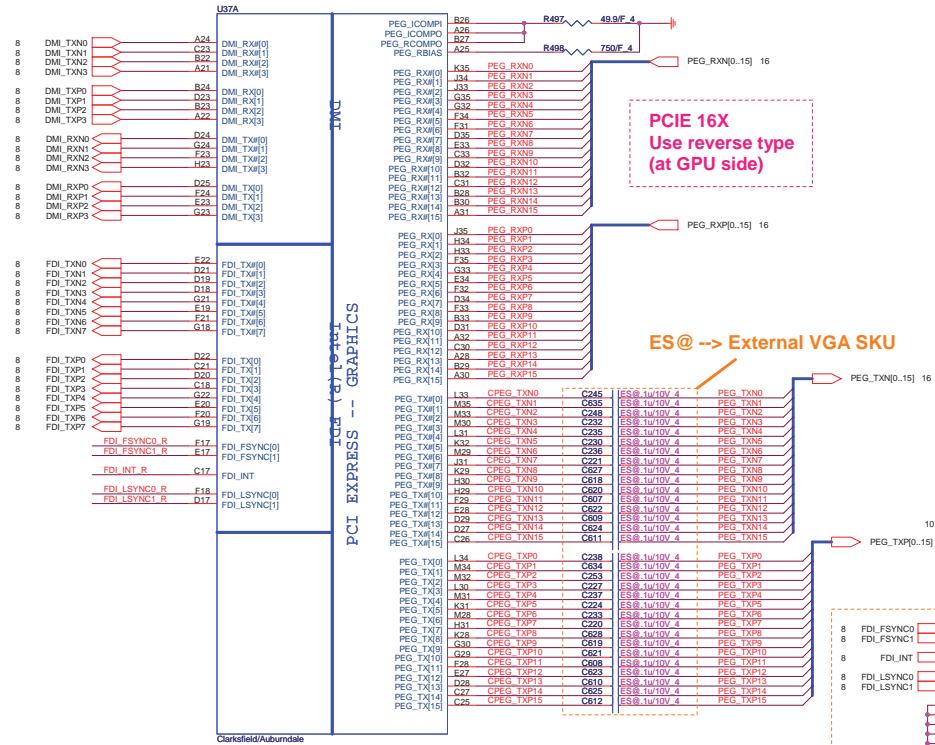
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AR@ --> ARD CPU  
 CF@ --> CFD CPU  
 ES@ --> External VGA SKU

ARRANDALE/CLARKSFIELD PROCESSOR (DMI, PEG, FDI)

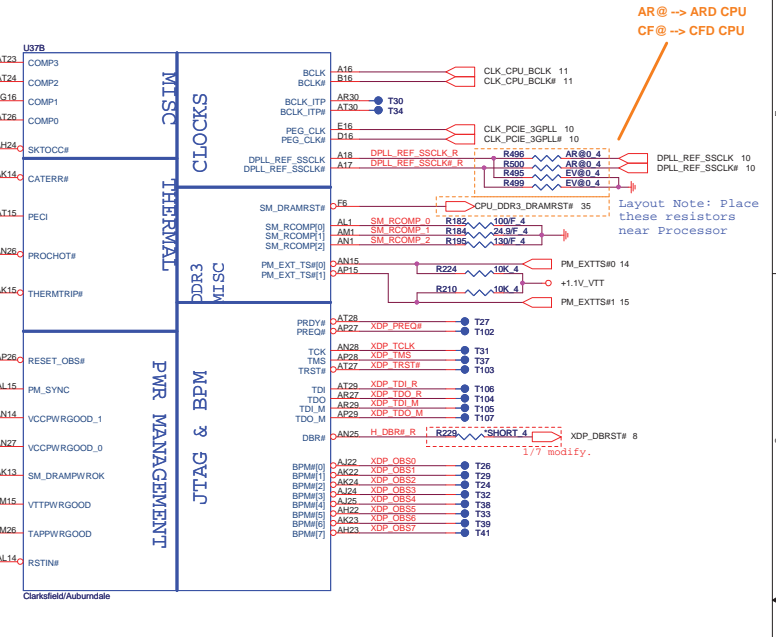
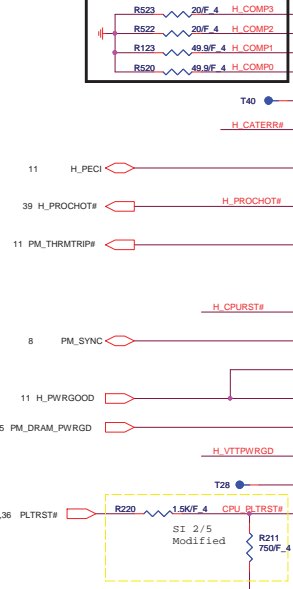
ARRANDALE/CLARKSFIELD PROCESSOR (CLK, MISC, JTAG)



PCI-E 16X  
 Use reverse type  
 (at GPU side)

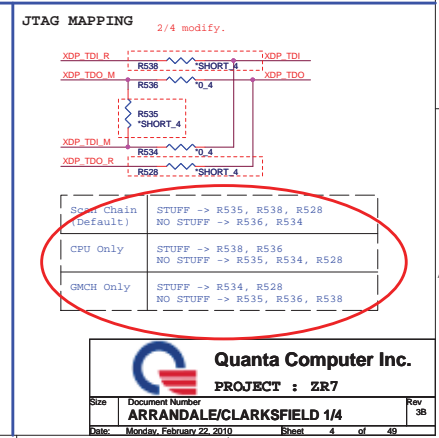
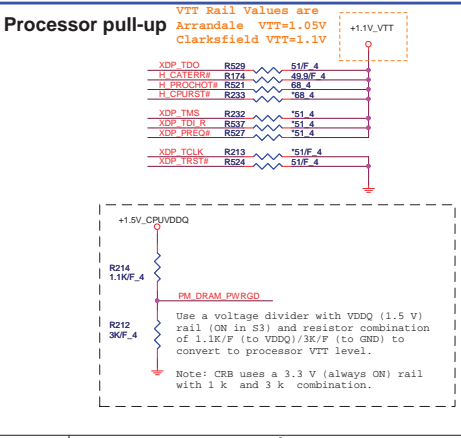
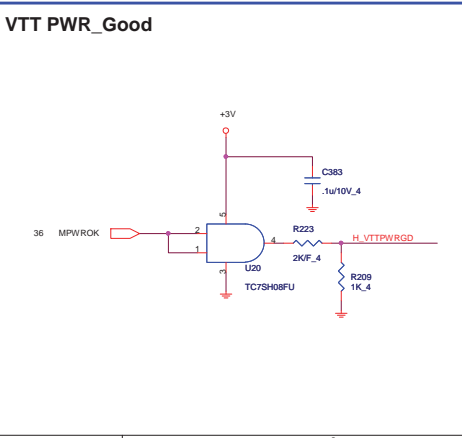
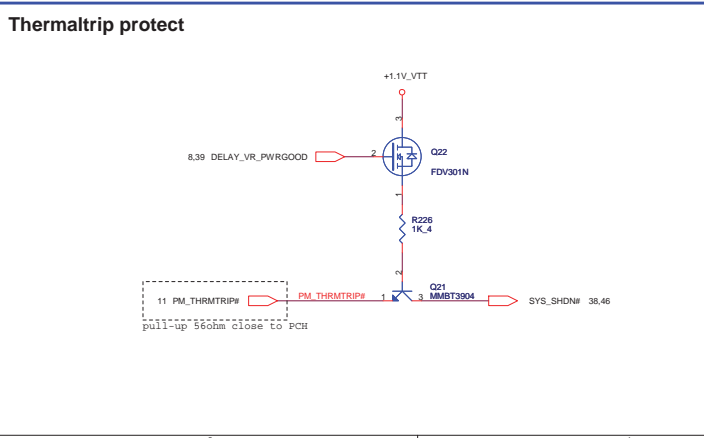
ES@ --> External VGA SKU

Processor Compensation Signals

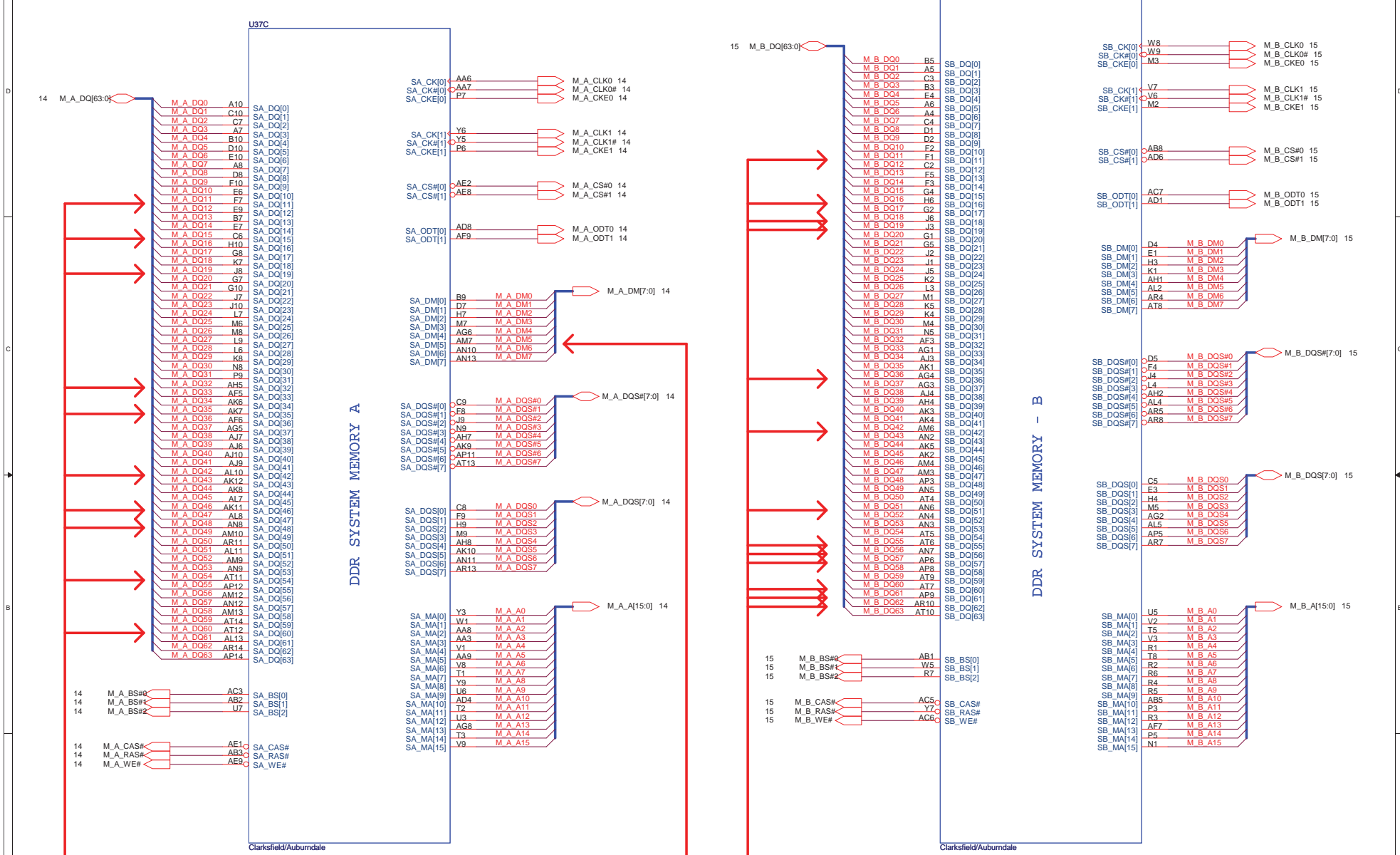


AR@ --> ARD CPU  
 CF@ --> CFD CPU

Layout Note: Place these resistors near Processor



# ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[11,15,19,32,35,42,46,48,54,60], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[11,16,18,19,36,42,51,55,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

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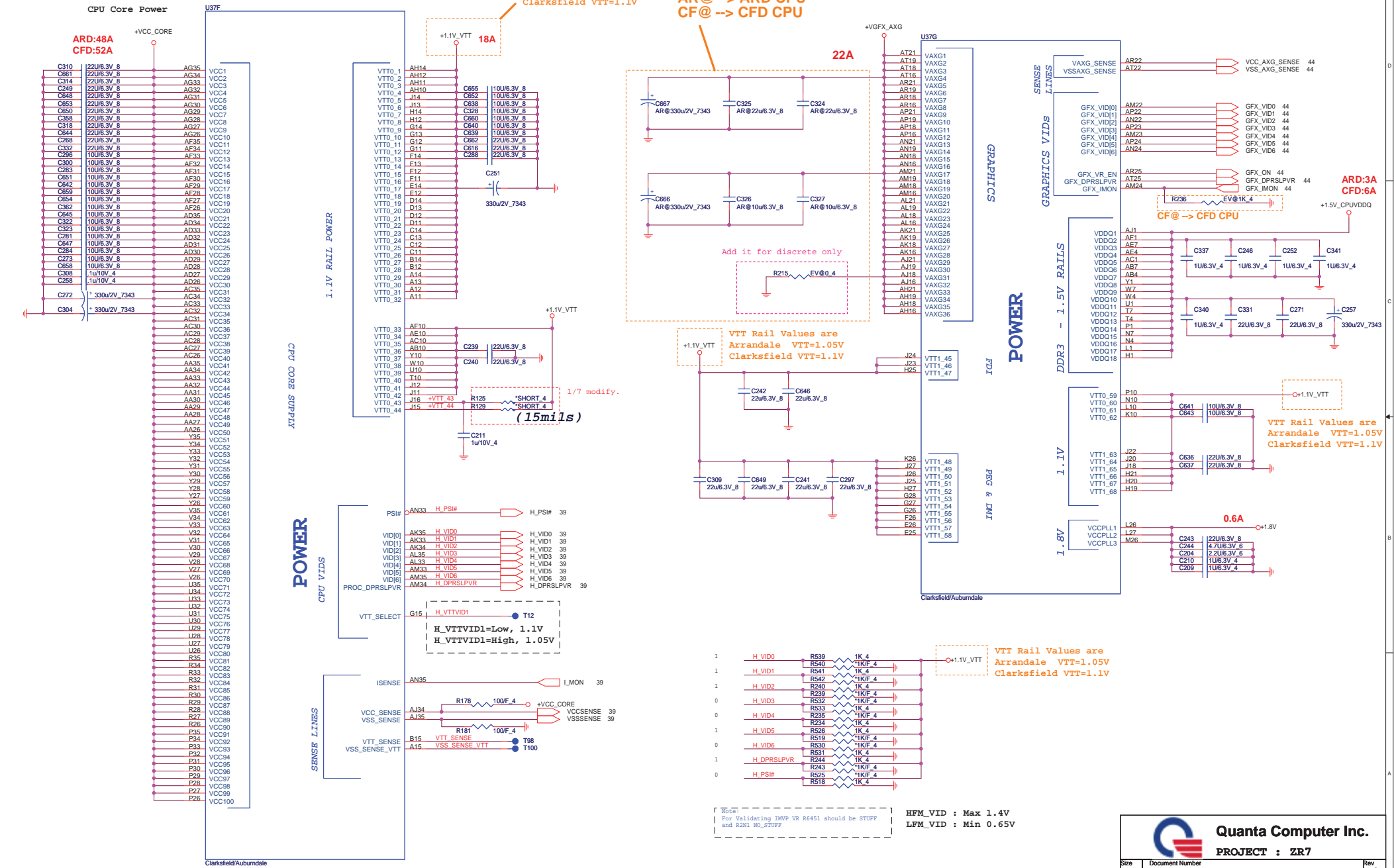
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	<b>ARRANDALE/CLARKSFIELD 2/4</b>	3B
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AR@ --> ARD CPU  
CF@ --> CFD CPU

ARRANDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

VTT Rail Values are  
Arrandale VTT=1.05V  
Clarksfield VTT=1.1V

AR@ --> ARD CPU  
CF@ --> CFD CPU



Note:  
For Validating IMVP VR R6451 should be STUFF  
and R2M1 NO\_STUFF

HFM\_VID : Max 1.4V  
LFM\_VID : Min 0.65V

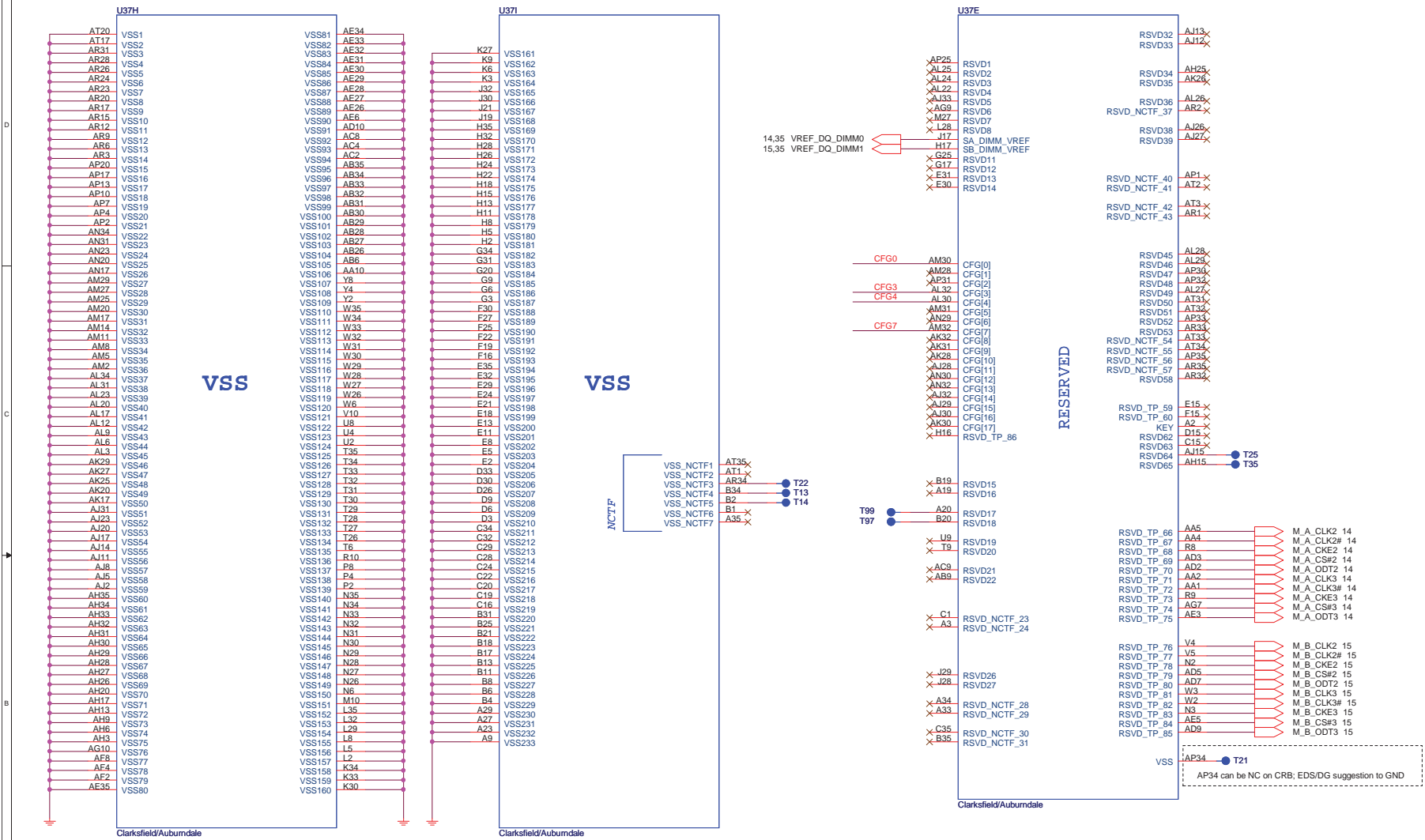
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Doc# : ARRANDALE/CLARKSFIELD 3/4 (PWR)  
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ARRANDALE/CLARKSFIELD PROCESSOR (GND)

ARRANDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

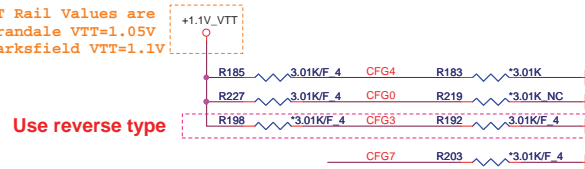


Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

VTT Rail Values are  
Arrandale VTT=1.05V  
Clarksfield VTT=1.1V



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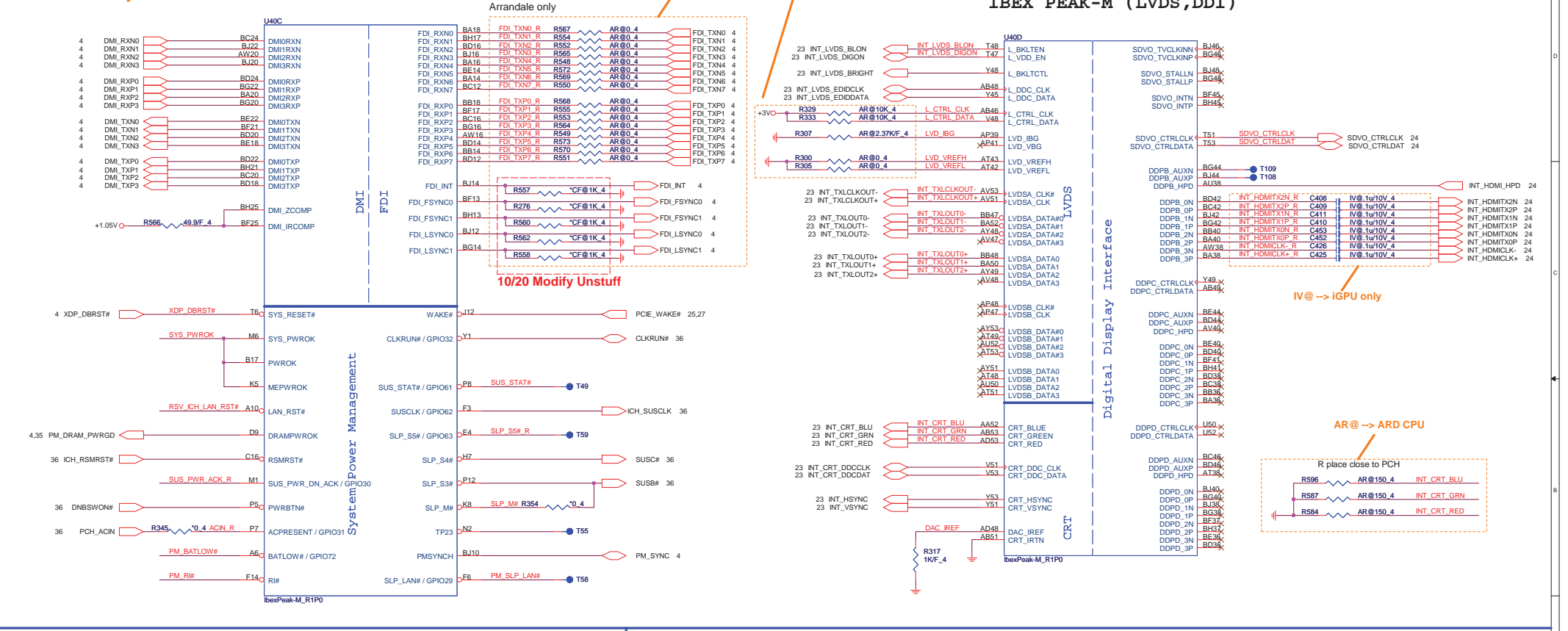
AR@ --> ARD CPU  
 CF@ --> CFD CPU  
 IV@ --> iGPU only

### IBEX PEAK-M (DMI, FDI, GPIO)

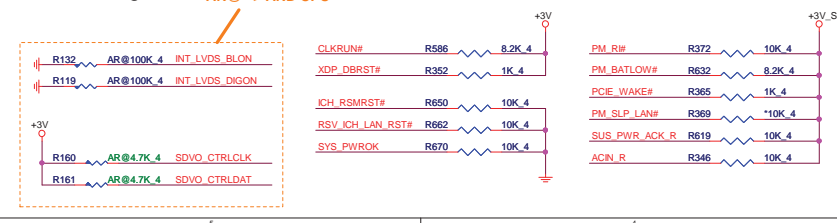
AR@ --> ARD CPU  
 CF@ --> CFD CPU

AR@ --> ARD CPU

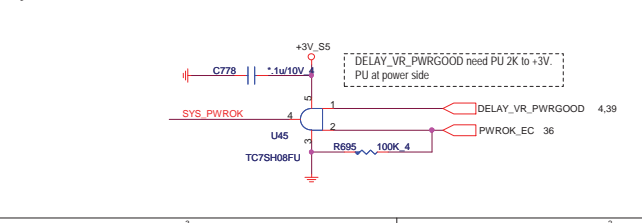
### IBEX PEAK-M (LVDS, DDI)



#### PCH Pull-high/low AR@ --> ARD CPU



#### System PWR\_OK

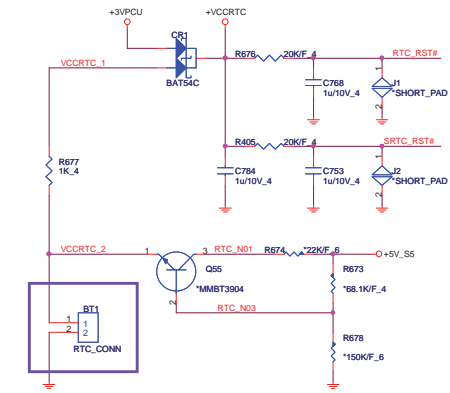


**Quanta Computer Inc.**  
**PROJECT : ZR7**

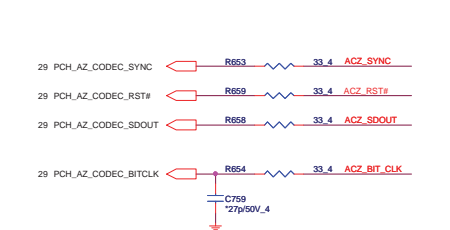
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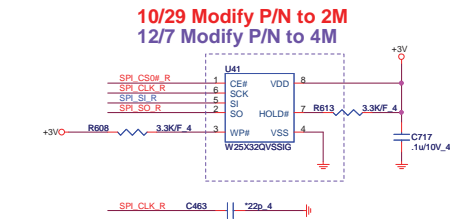
### RTC Circuitry



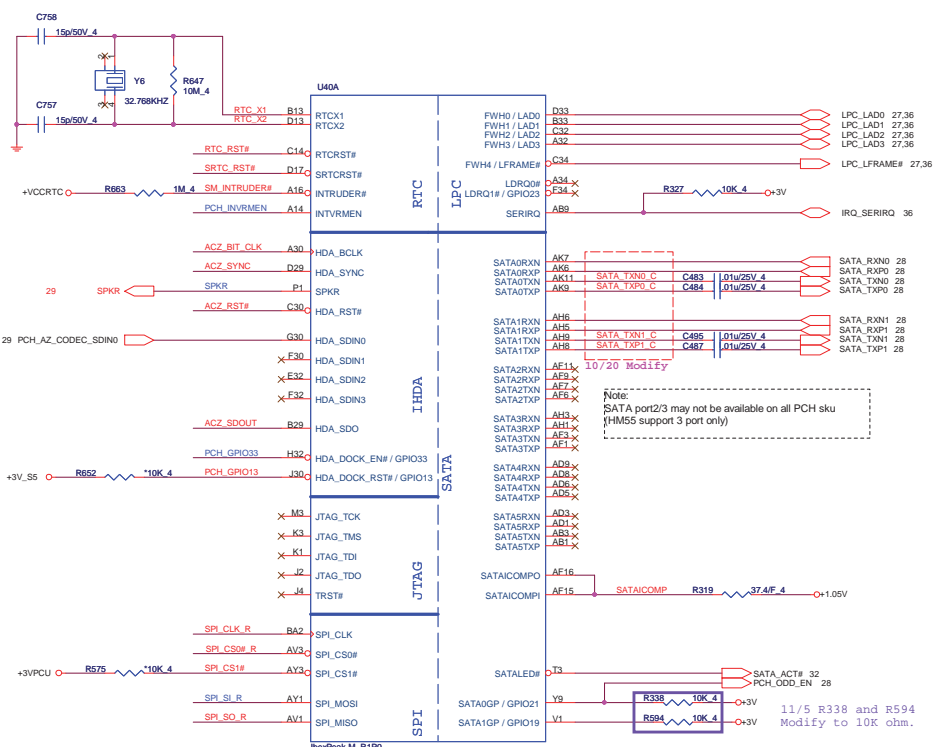
### HDA Bus



### PCH SPI



**HDA\_SYNC (PCH strap pin)**  
 Internal weak pull-down  
 VCCVRM=>+1.8V (default)  
 external pull-up  
 VCCVRM=>+1.5V



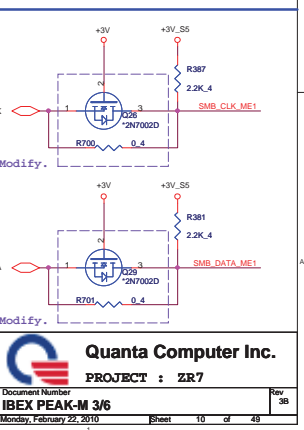
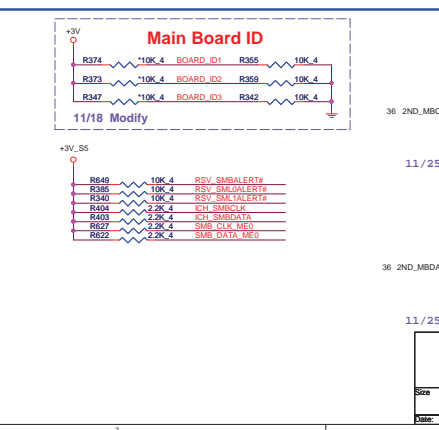
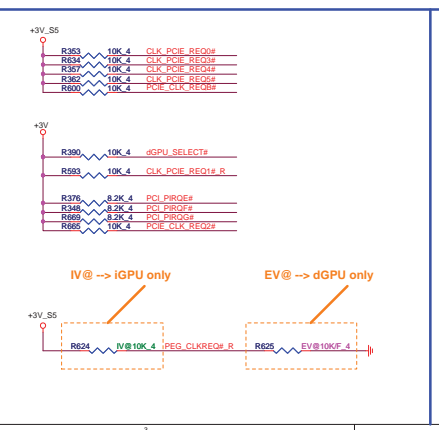
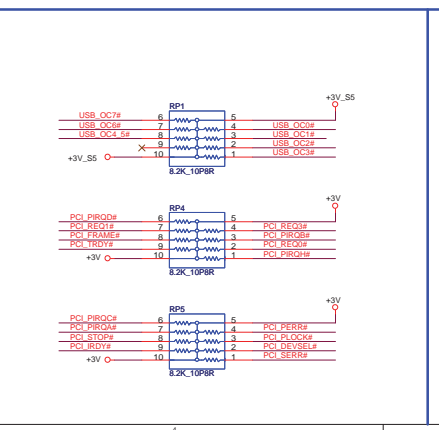
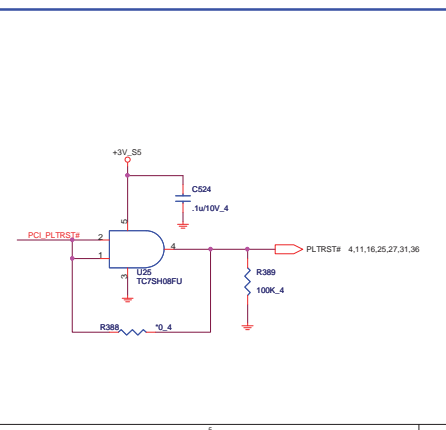
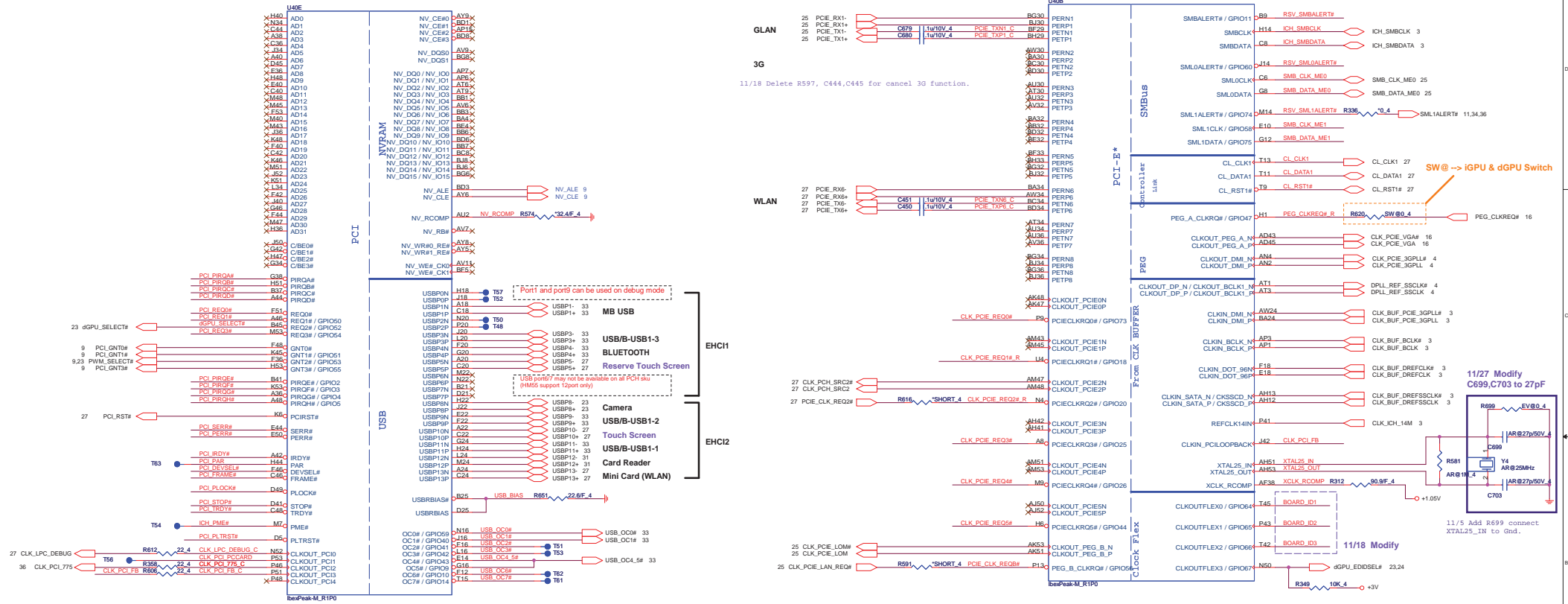
PCH Strap Pin Configuration Table-1

Signal	Function	Default / Options	Configuration
INTRVMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRRTC - R695 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disabled	+3V - R618 1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V - R611 1K1F_4SPKR
HDA_DOCK#/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPI033 - R370 1K1F_4 R362 10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	PCH_GNT0# - R360 1K_4 PCH_GNT1# - R363 1K_4 PCH_GNT1# - R709 1K_4
GNT2#/GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10,23 PWM_SELECT# - R364 1K1F_4
GNT3#/GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	0 PCH_GNT3# - R628 10K1F_4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE - R296 1K1F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE - R295 1K1F_4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPC08 - R380 10K_4 +3V_S5 R371 1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# - R341 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPI027 - R324 10K_4

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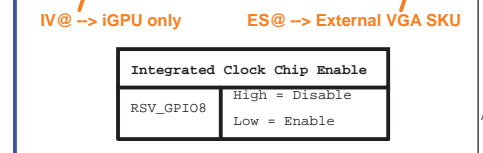
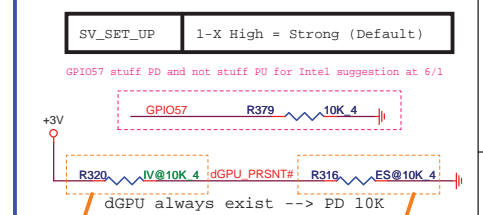
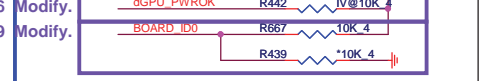
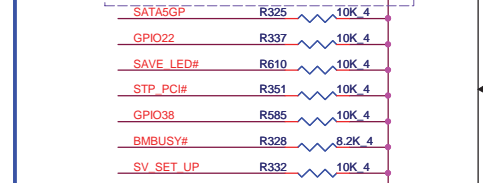
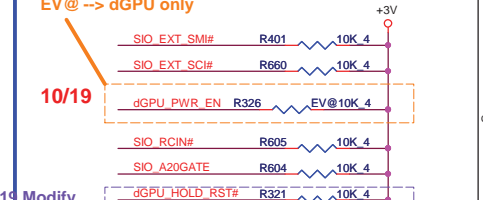
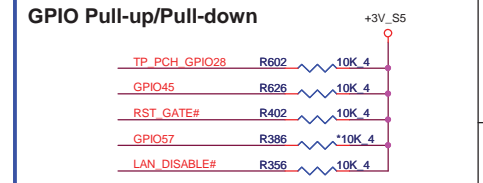
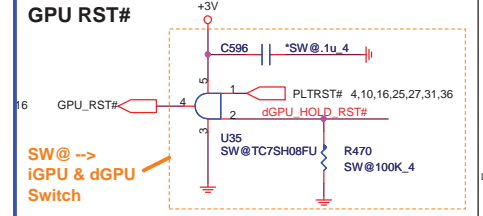
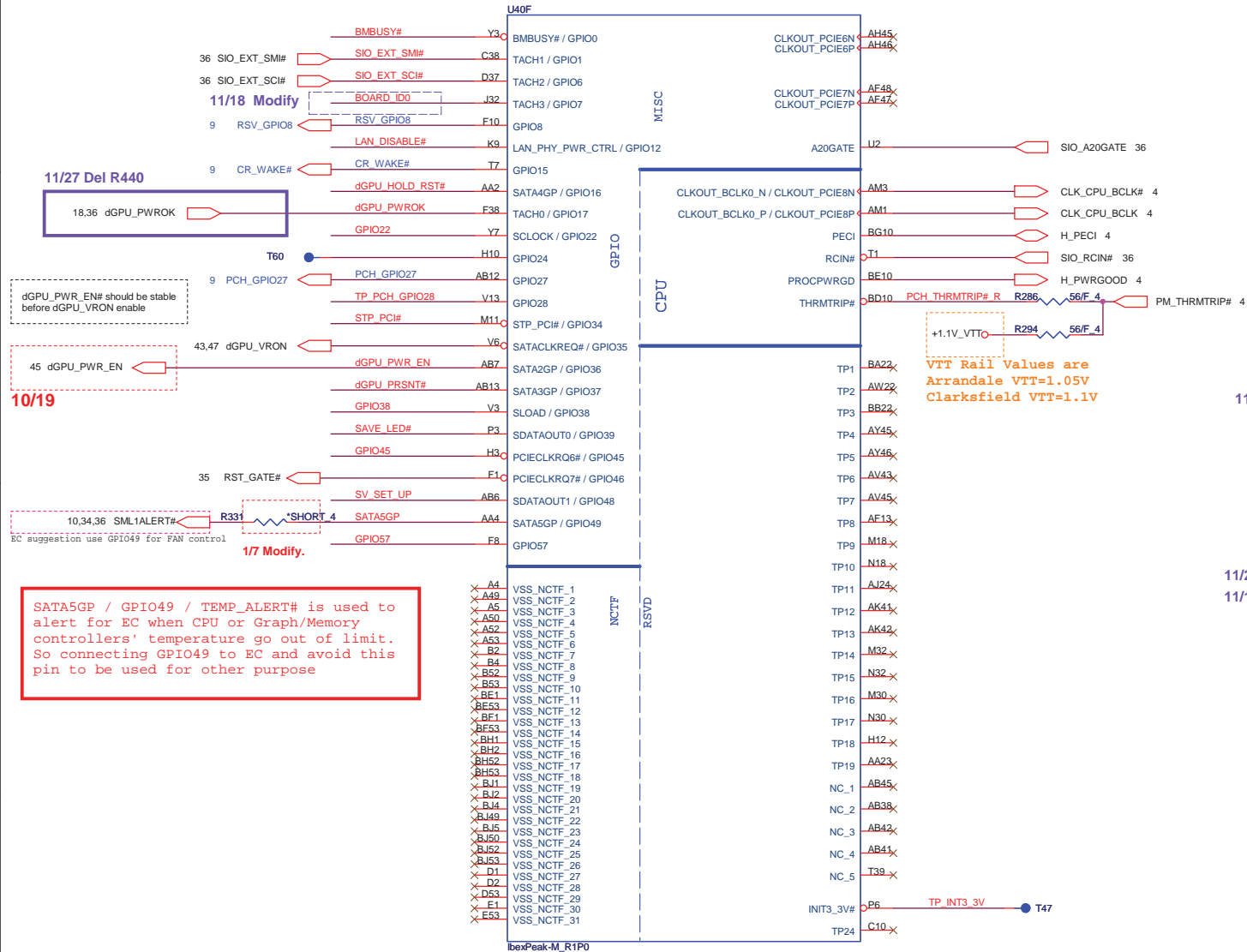
IV@ --> iGPU only  
 EV@ --> dGPU only  
 SW@ --> iGPU & dGPU Switch



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IV@ --> iGPU only  
 EV@ --> dGPU only  
 SW@ --> iGPU & dGPU Switch  
 ES@ --> External VGA SKU

### IBEX PEAK-M (GPIO, VSS\_NCTF, RSVD)



**IBEX PEAK-M (POWER)**

AR@ -> ARD CPU  
CF@ -> CFD CPU

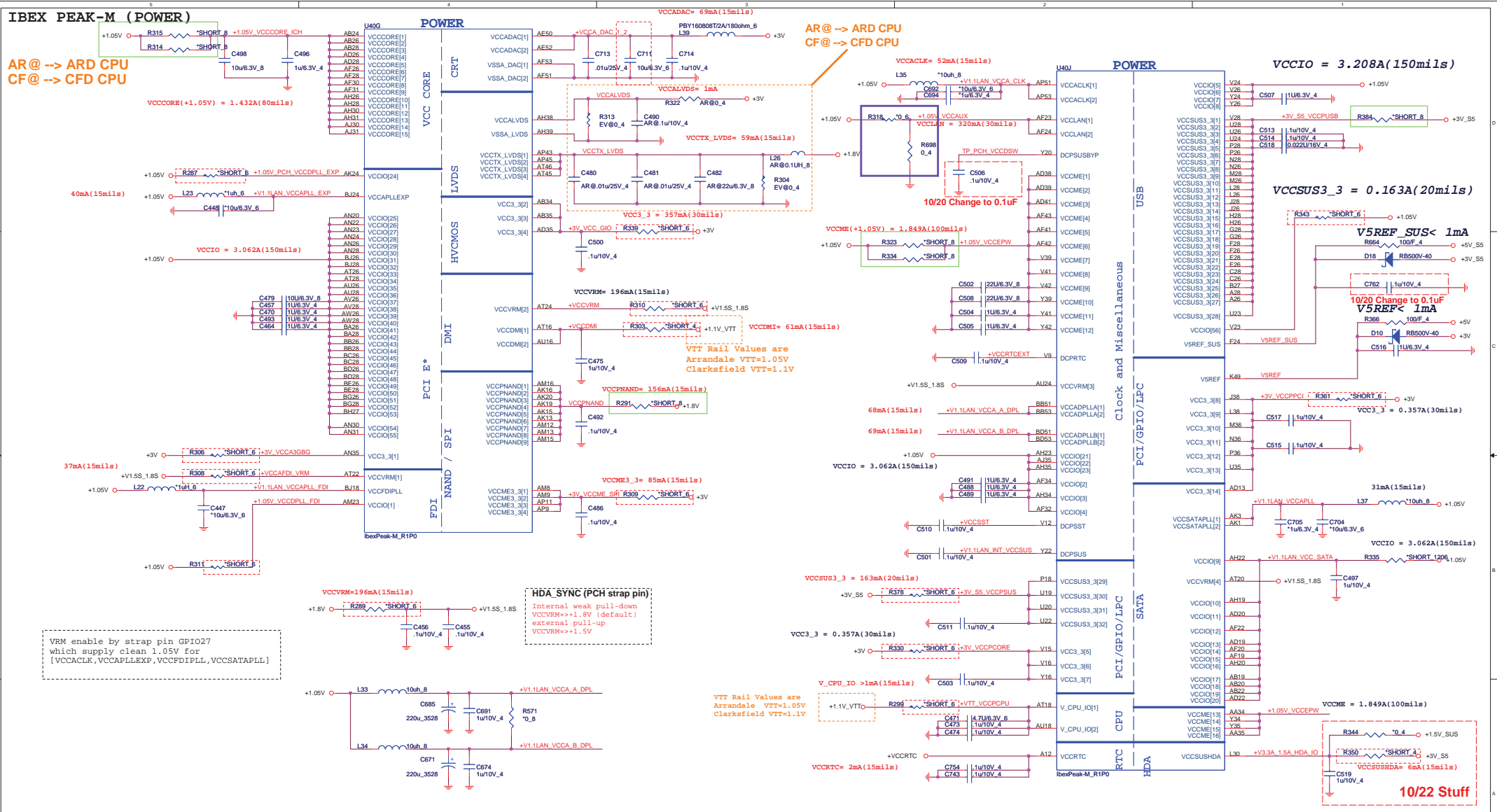
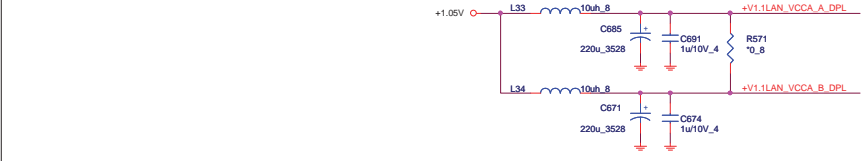
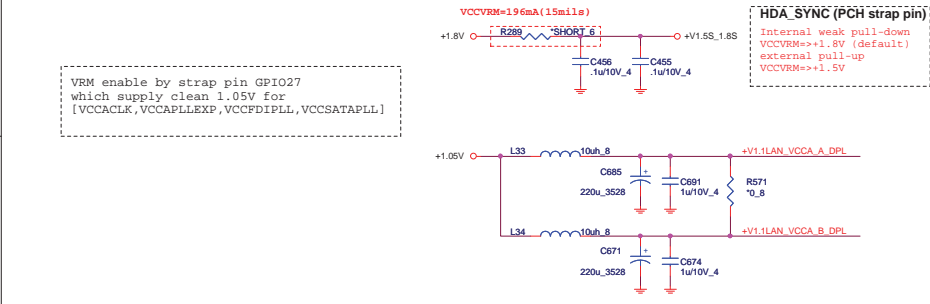
VCCCORE(+1.05V) = 1.432A(80mils)

40mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

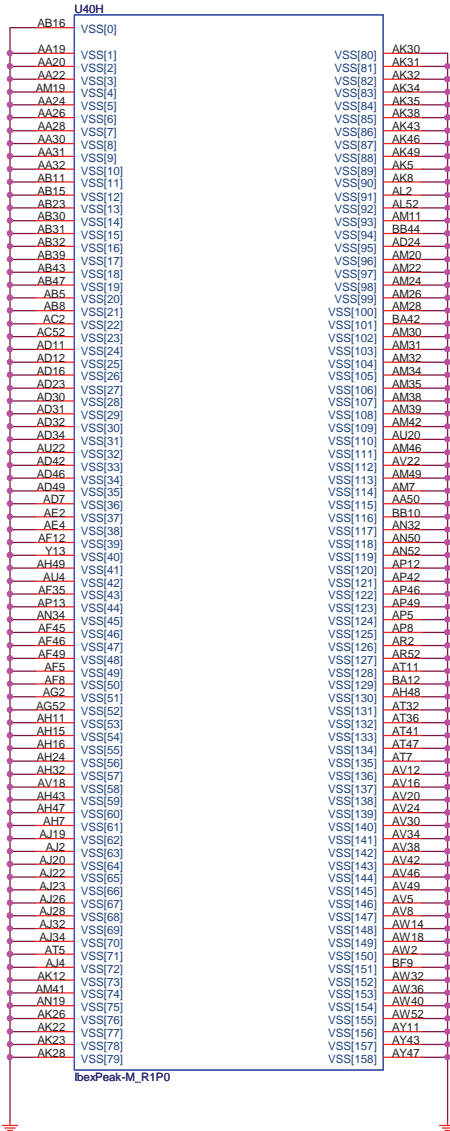
VRM enable by strap pin GPIO27  
which supply clean 1.05V for  
[VCCACLK, VCCAPLLEXP, VCCFDIPLL, VCCSATAPLL]



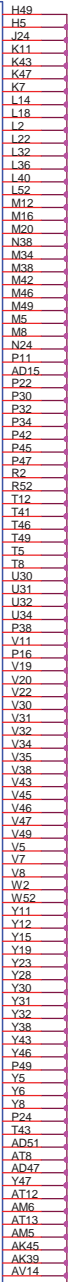
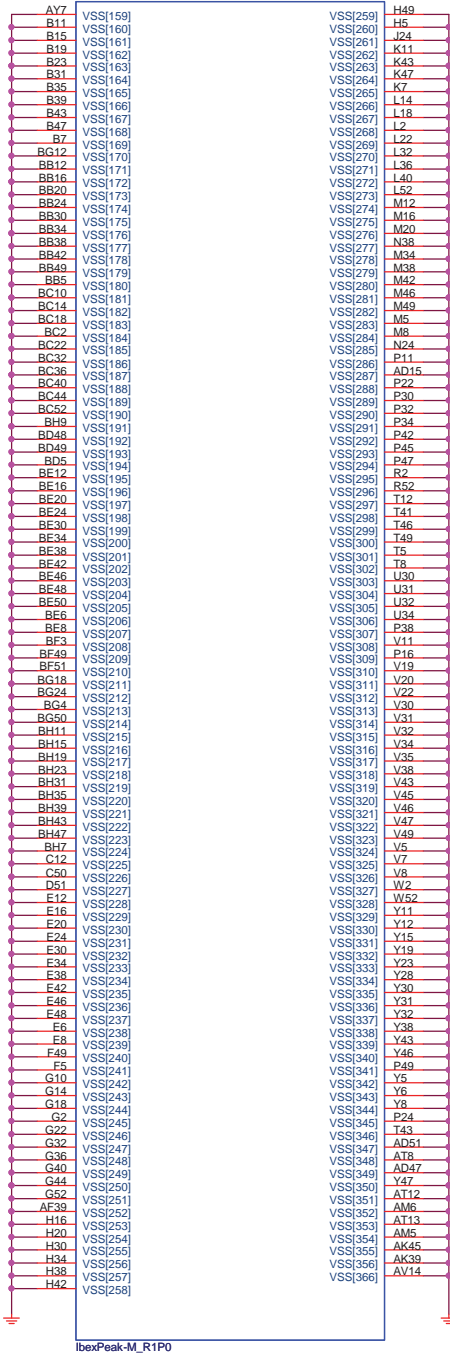
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**IBEX PEAK-M (GND)**



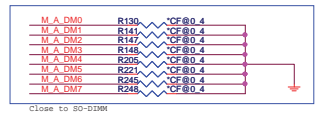
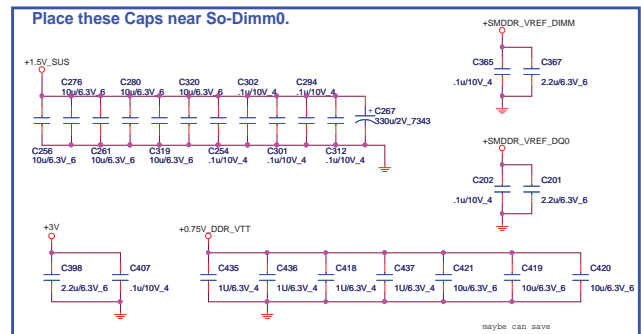
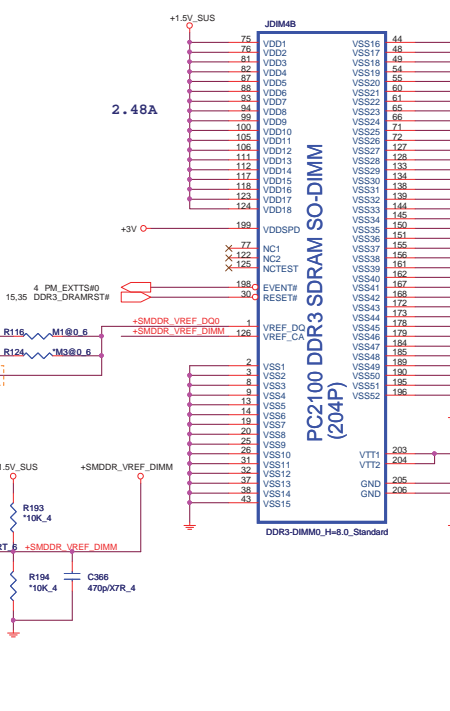
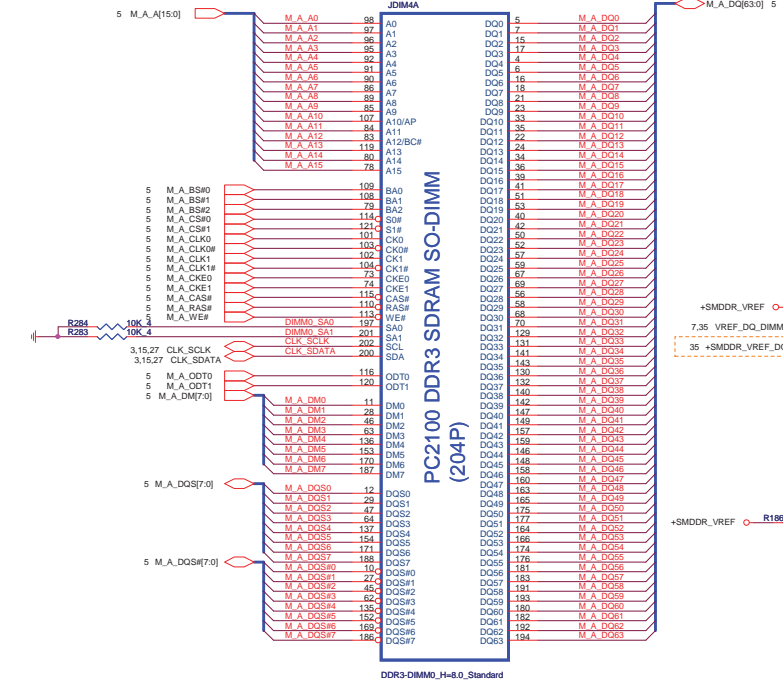
**U40I**



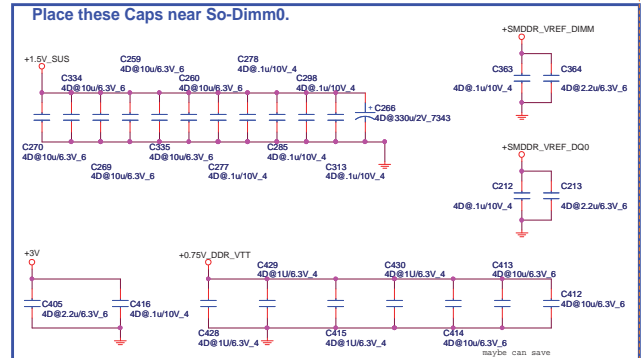
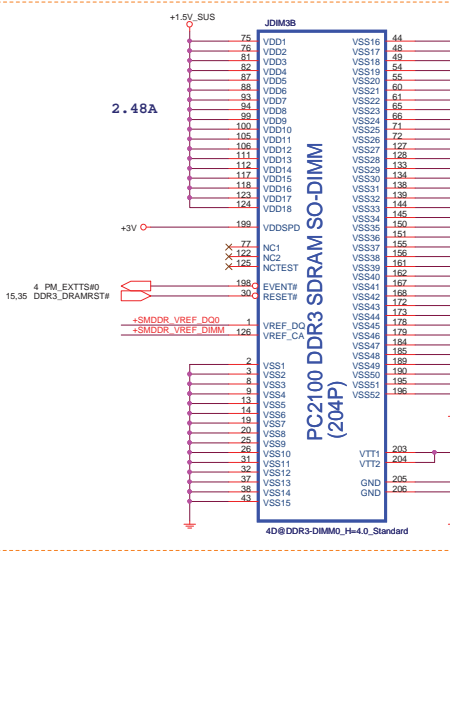
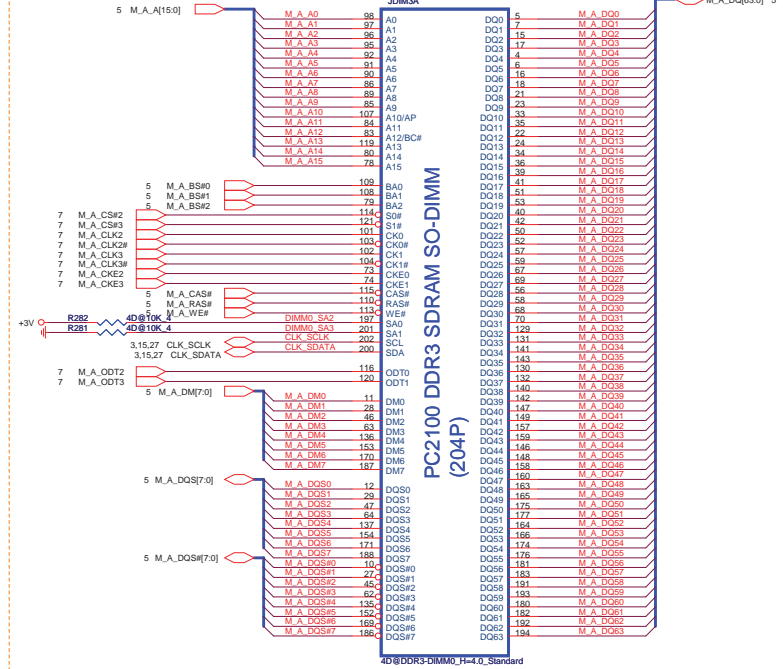
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**DIMM A0**

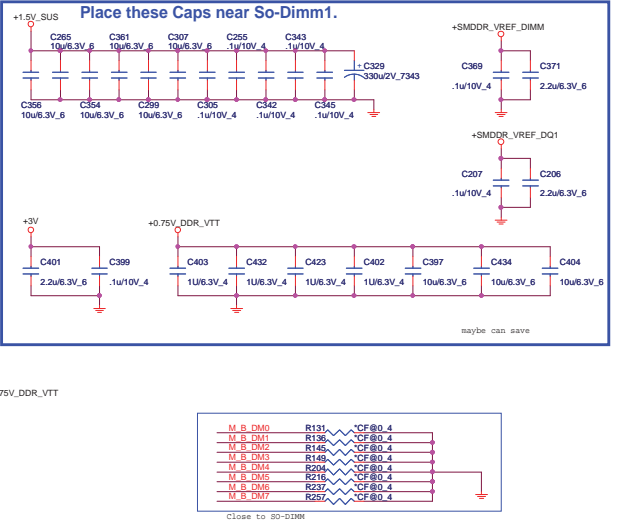
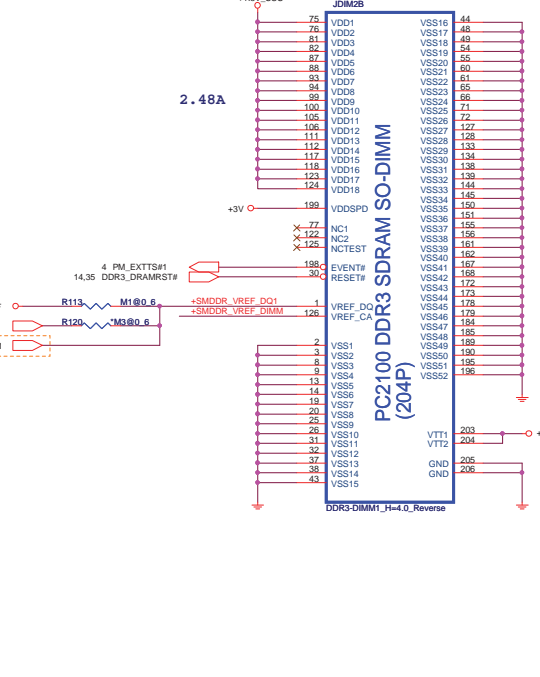
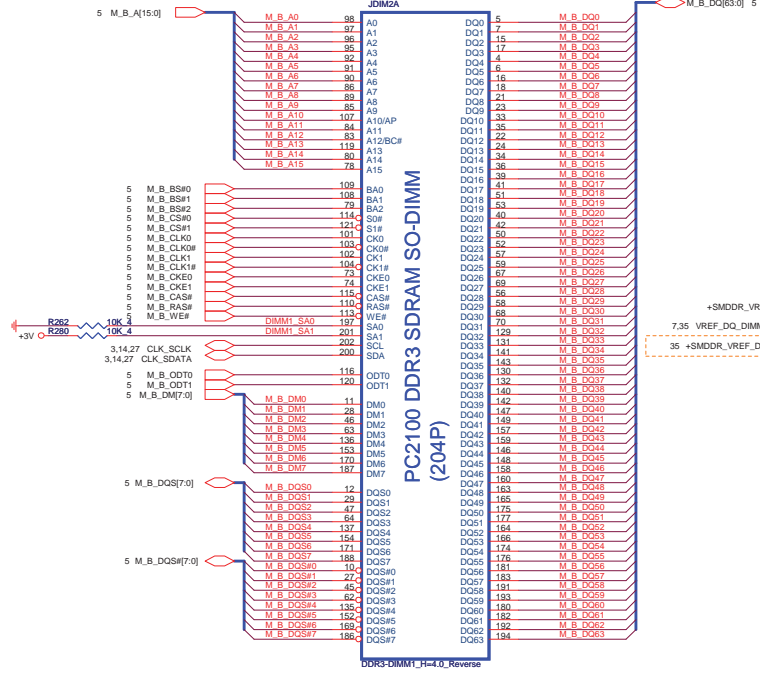


**DIMM A1 4D@ --> 4 SO-DIMM**

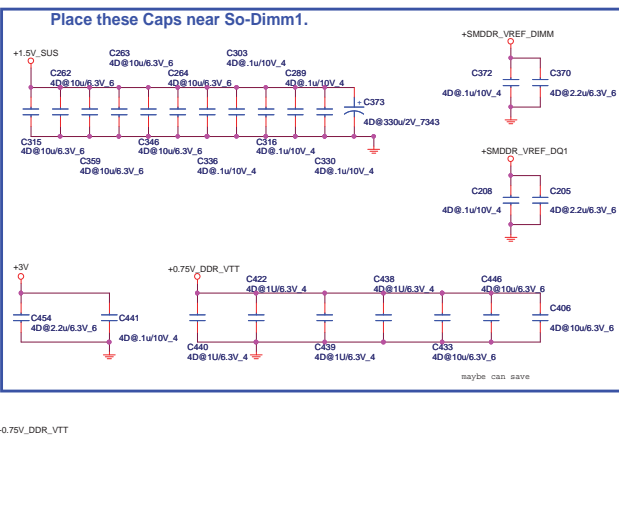
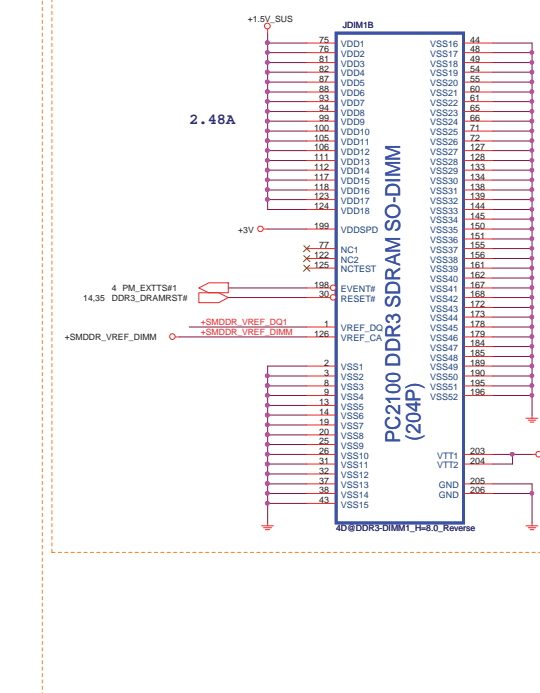
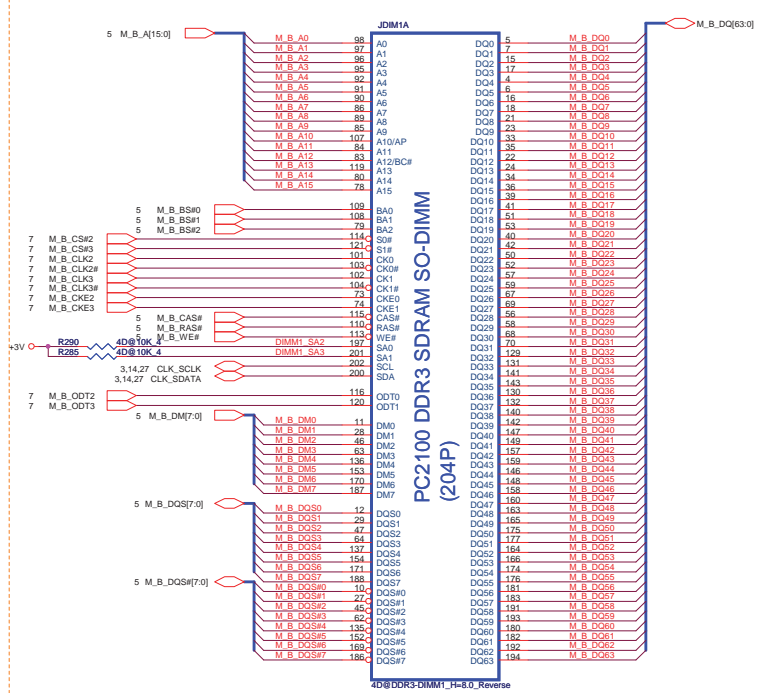


**Quanta Computer Inc.**  
 PROJECT : ZR7  
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**DDR3 SO-DIMM-A0/A1**  
 Date: Monday, February 22, 2010 Sheet 14 of 49

**DIMM B0**



**DIMM B1 4D@ -> 4 SO-DIMM**

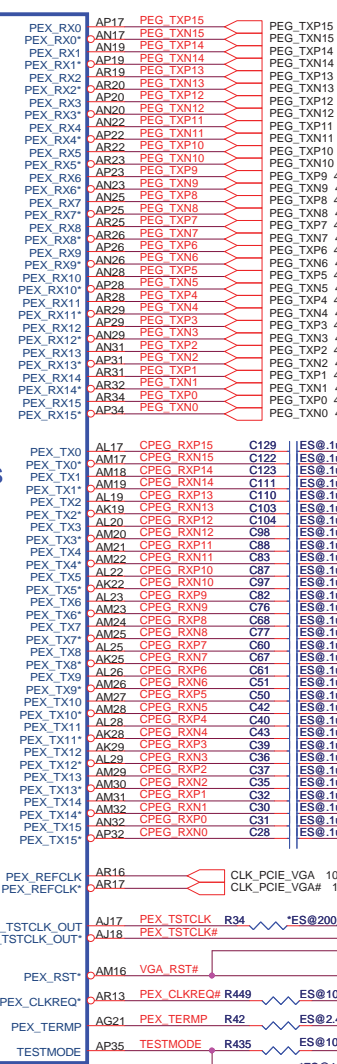
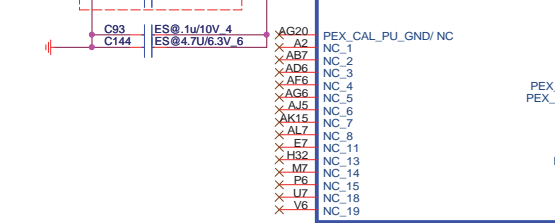
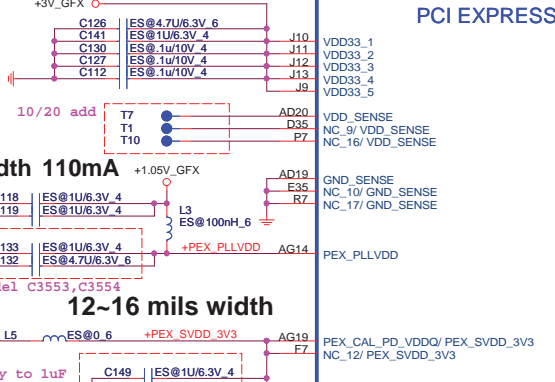
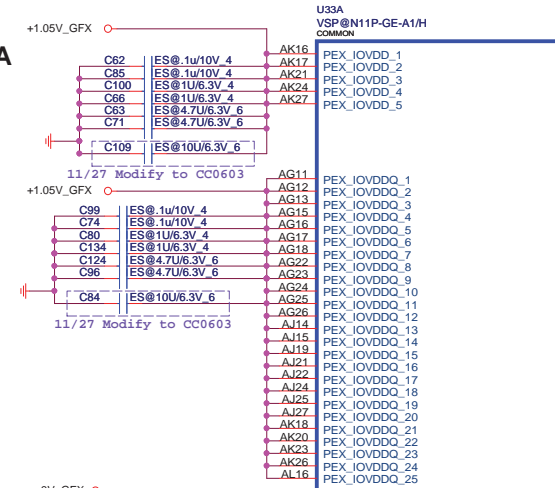


PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD >2.2A

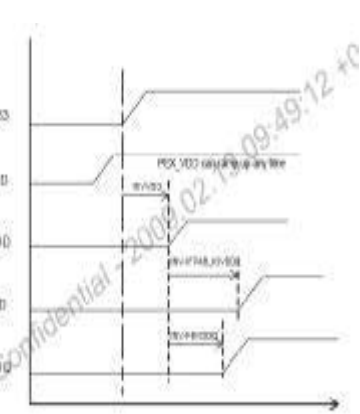
~ 500mA

1600mA

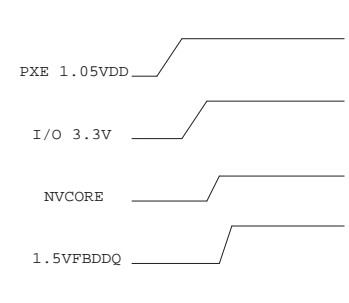
Near BGA



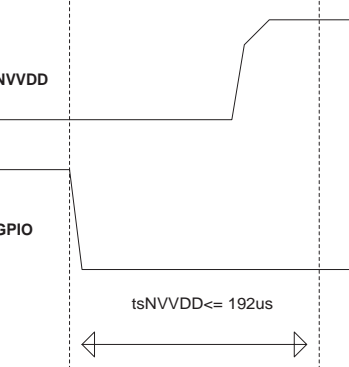
EV@ --> dGPU only  
 SW@ --> iGPU & dGPU Switch  
 ES@ --> External VGA SKU  
 VSP@ --> Operation P/N (VGA)



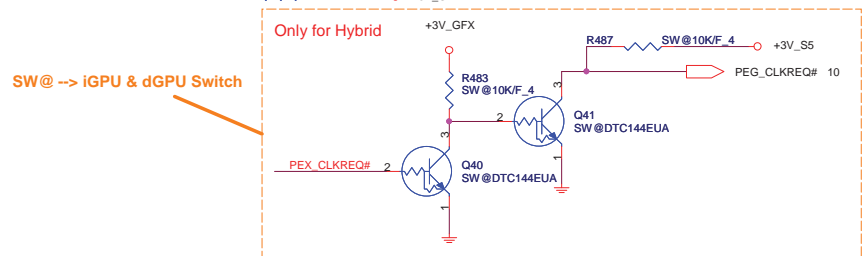
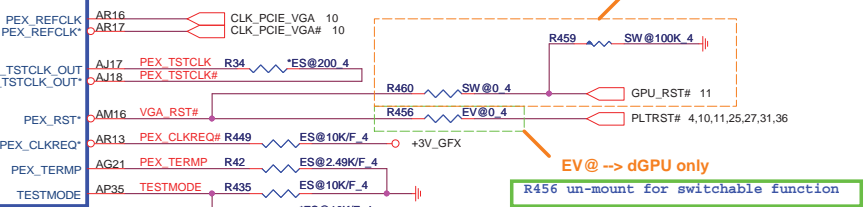
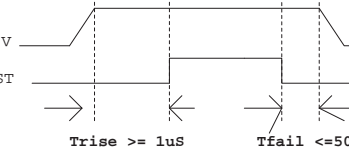
### power up sequence



NB9M: VGACORE +0.90V (Normal), +1.09V  
 NVVDD Maximum Settling Time



### PEX\_RST timing

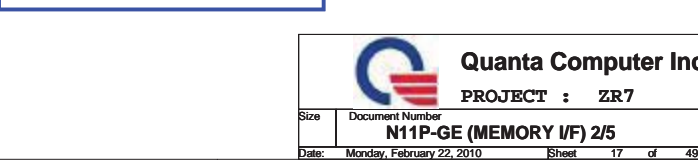
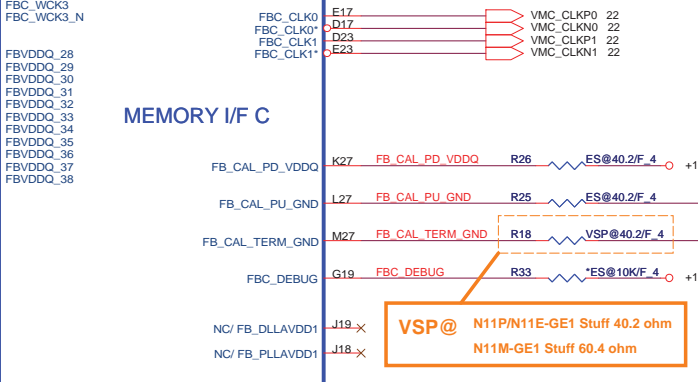
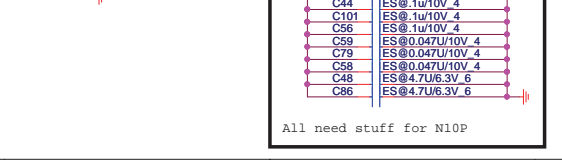
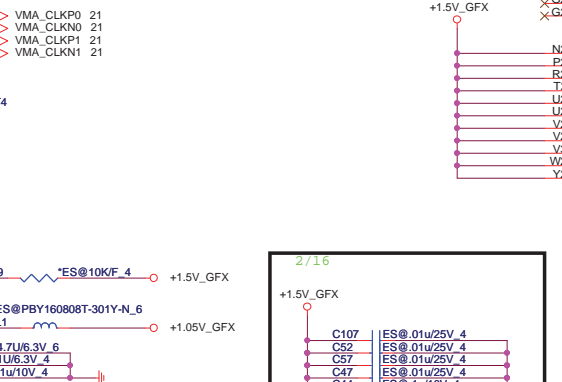
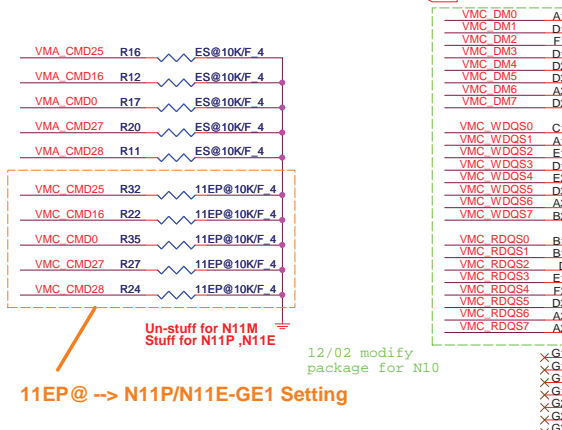
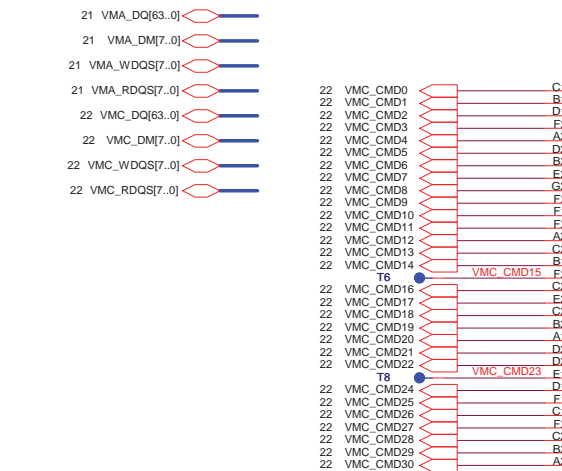
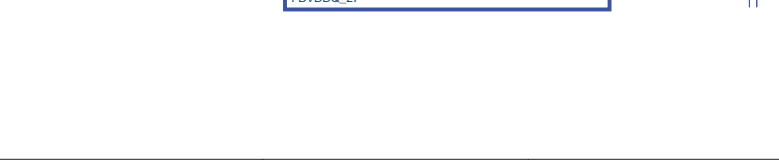
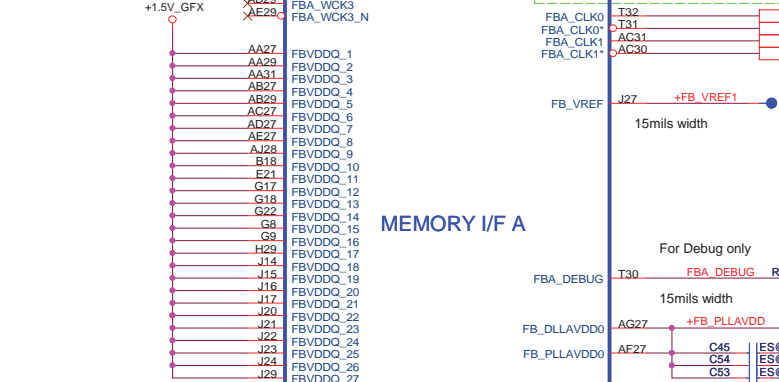
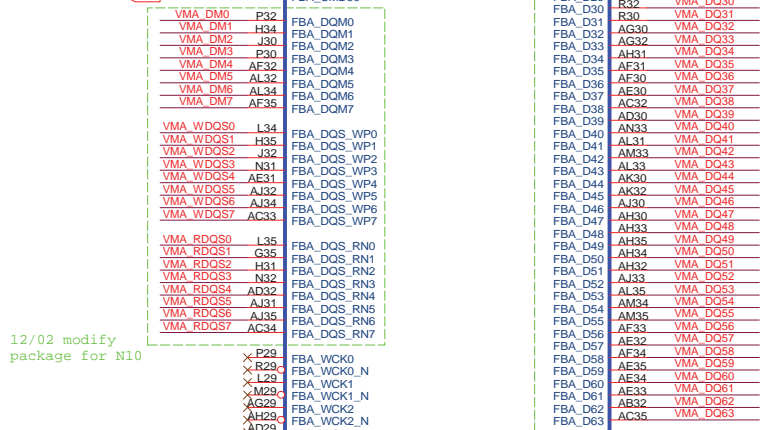
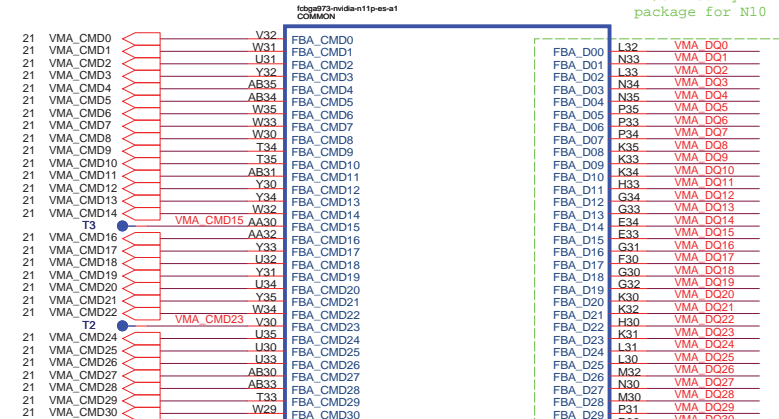


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 PROJECT : ZR7

Size	Document Number	Rev
	<b>N11P-GE (PCIE I/F) 1/5</b>	3B
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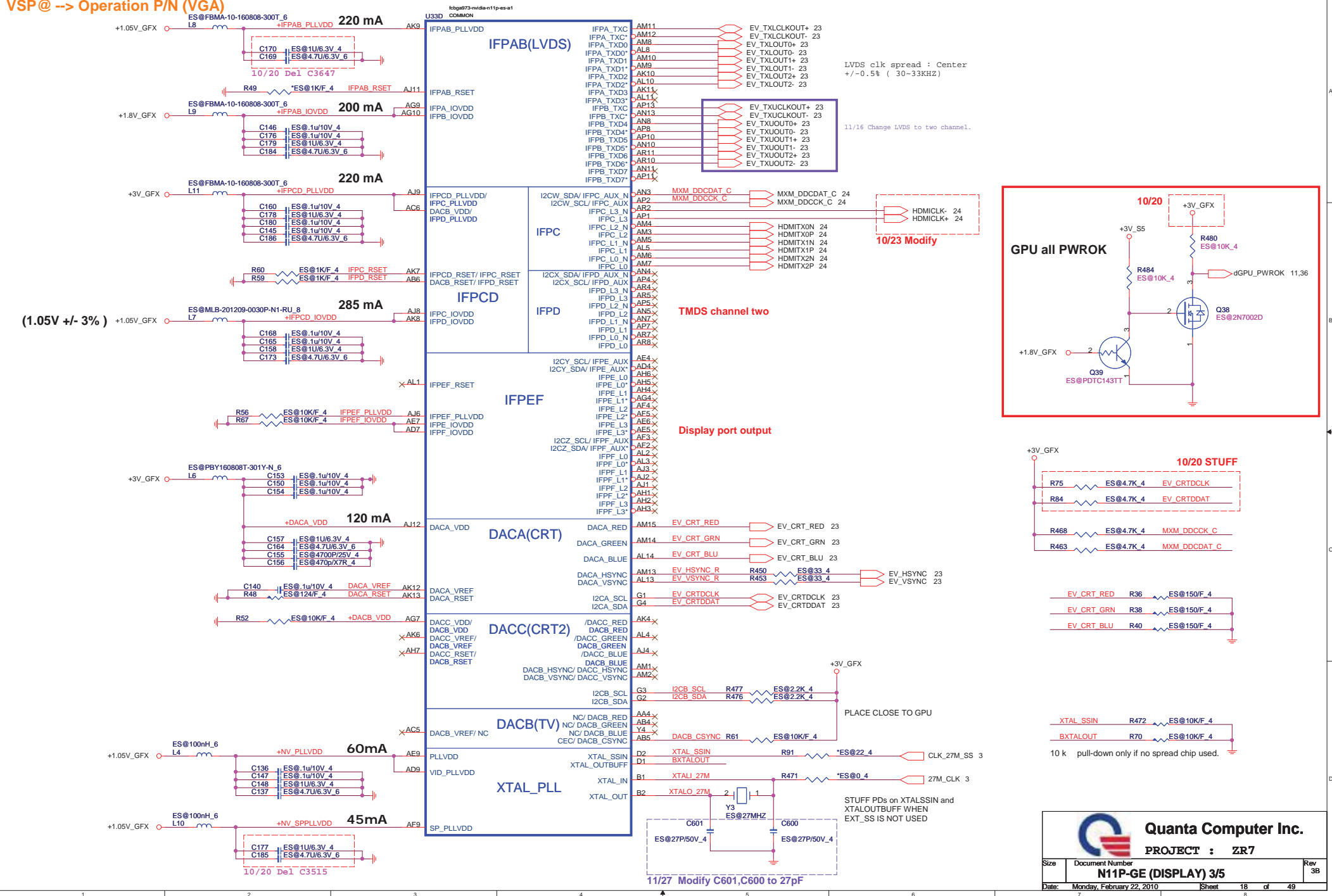
VSP@ --> Operation P/N (VGA) 11EP@ --> N11P/N11E-GE1 Setting  
 ES@ --> External VGA SKU



12/02 modify package for N10  
 11EP@ --> N11P/N11E-GE1 Setting  
 Un-stuff for N11M Stuff for N11P, N11E  
 12/02 modify package for N10

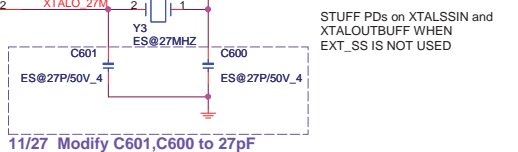
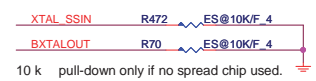
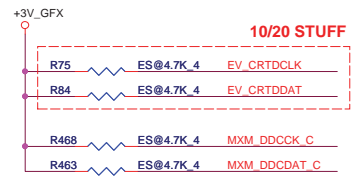
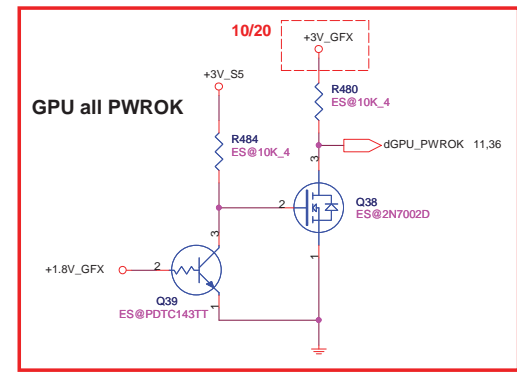


ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)



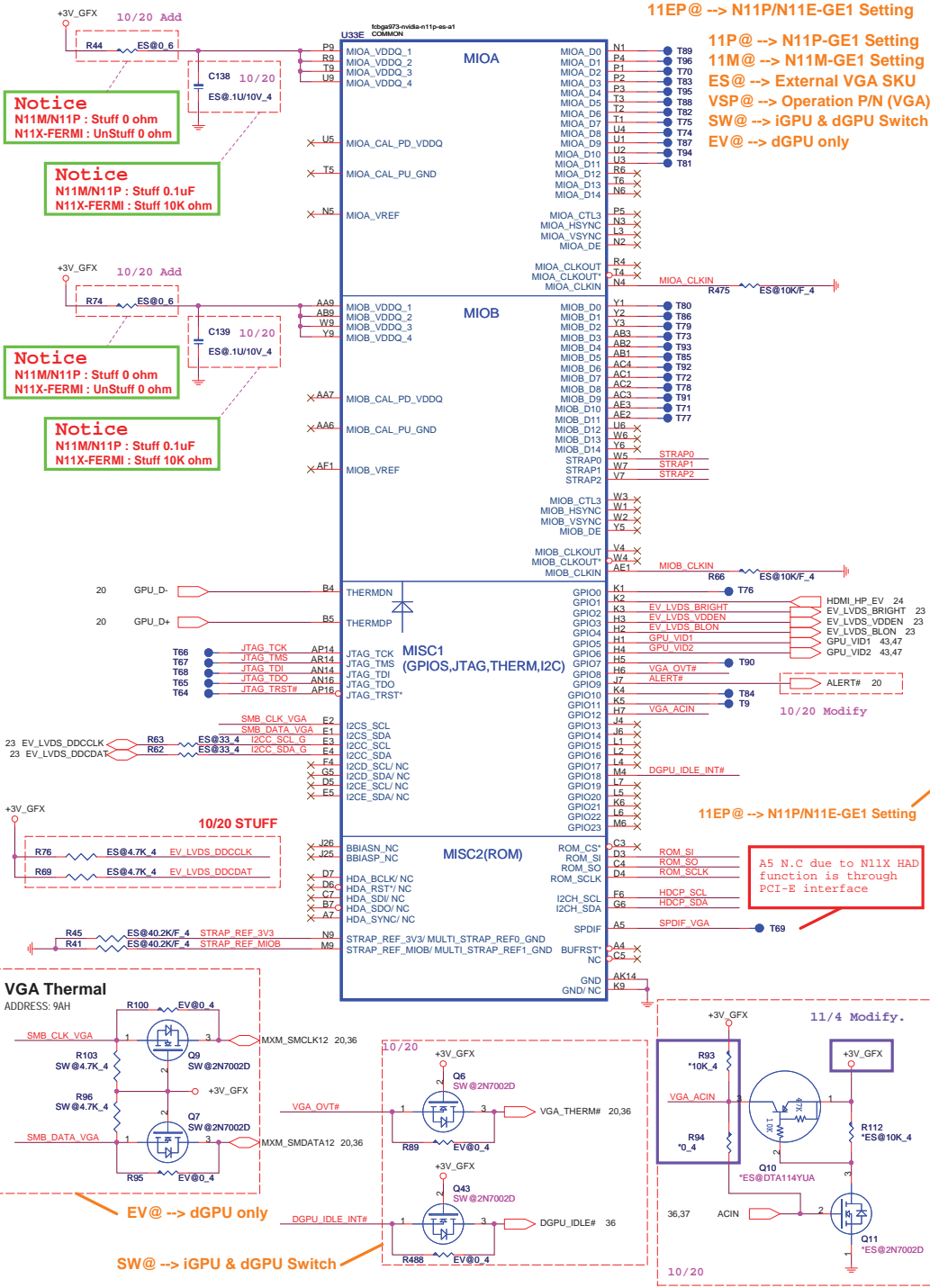
LVDS clk spread : Center  
+/-0.5% ( 30-33KHZ)

11/16 Change LVDS to two channel.



**Quanta Computer Inc.**  
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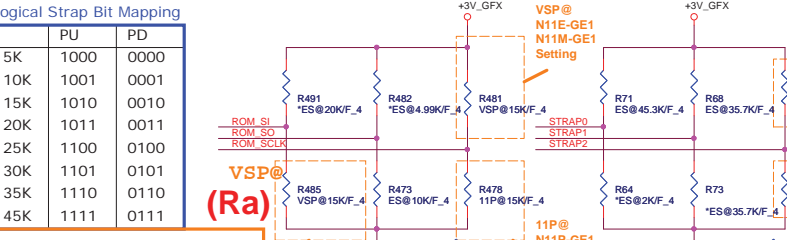
Size	Document Number	Rev
	<b>N11P-GE (DISPLAY) 3/5</b>	3B
Date:	Monday, February 22, 2010	Sheet 18 of 49



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM		X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]		XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]		1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI (Ra)
0000	Reserved	Reserved	Reserved	AKDSLZGTW04
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0100	Reserved	Reserved	Reserved	AKDSLZGTW04
0110	Reserved	Reserved	Reserved	AKDSLZGTW04
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	



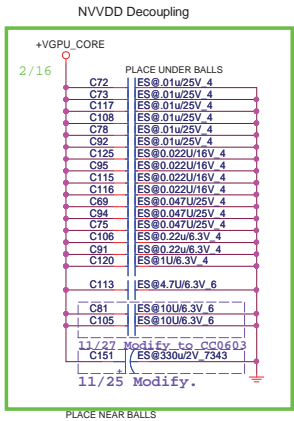
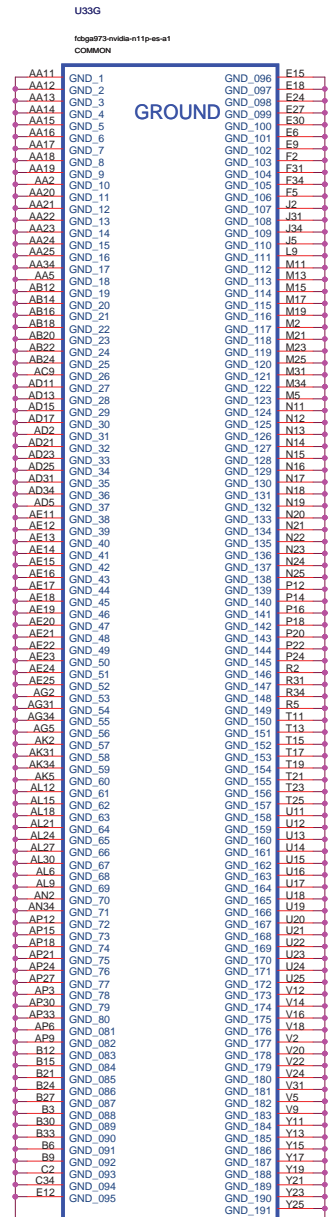
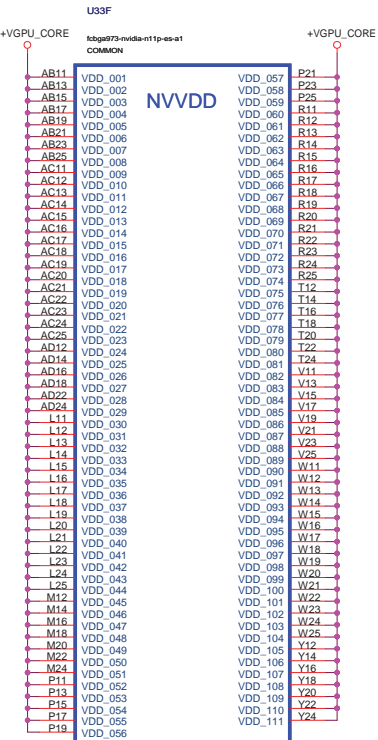
CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PD 15K	PU 10K	0x0A29
N11E-GE1	PU 15K	PD 5K	0x0C8D

4.99K/4 : CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]  
 10K/4 : CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]  
 15K/4 : CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]  
 20K/4 : CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]  
 30.1K/4 : CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]  
 35.7K/4 : CS3352FB13 [RES CHIP 35.7K 1/16W +1%(0402)]  
 45.3K/4 : CS3452FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

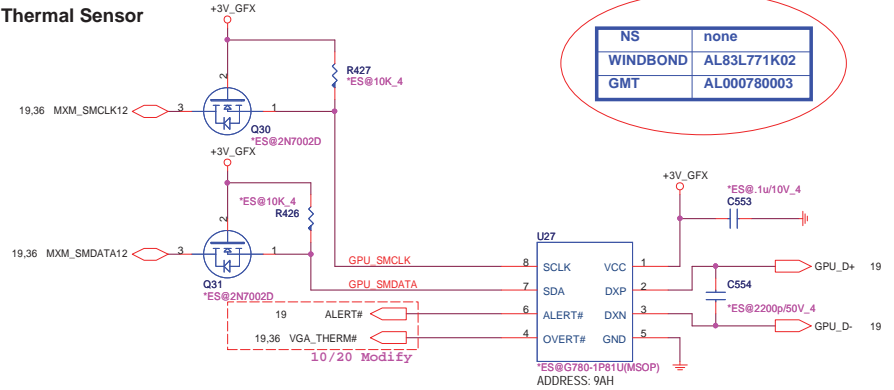
### GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFF link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

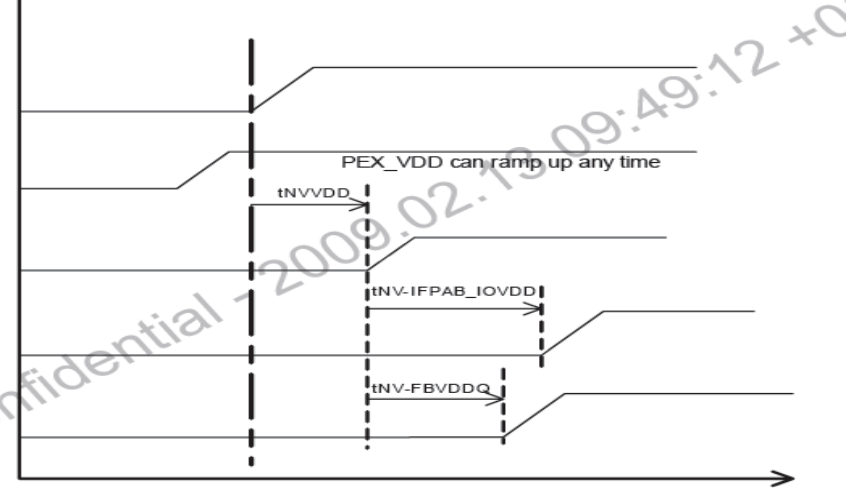
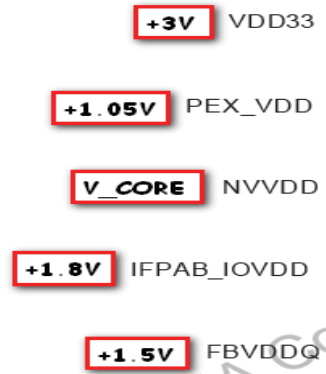
ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)



Thermal Sensor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



Quanta Computer Inc.

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Size Document Number N11P-GE (POWER & GND&THM) 5/5 Rev 3B

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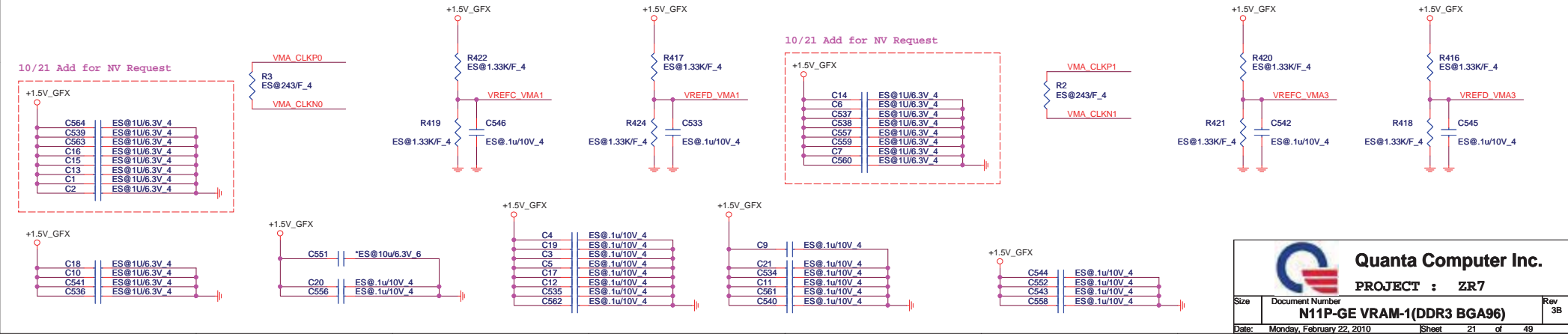
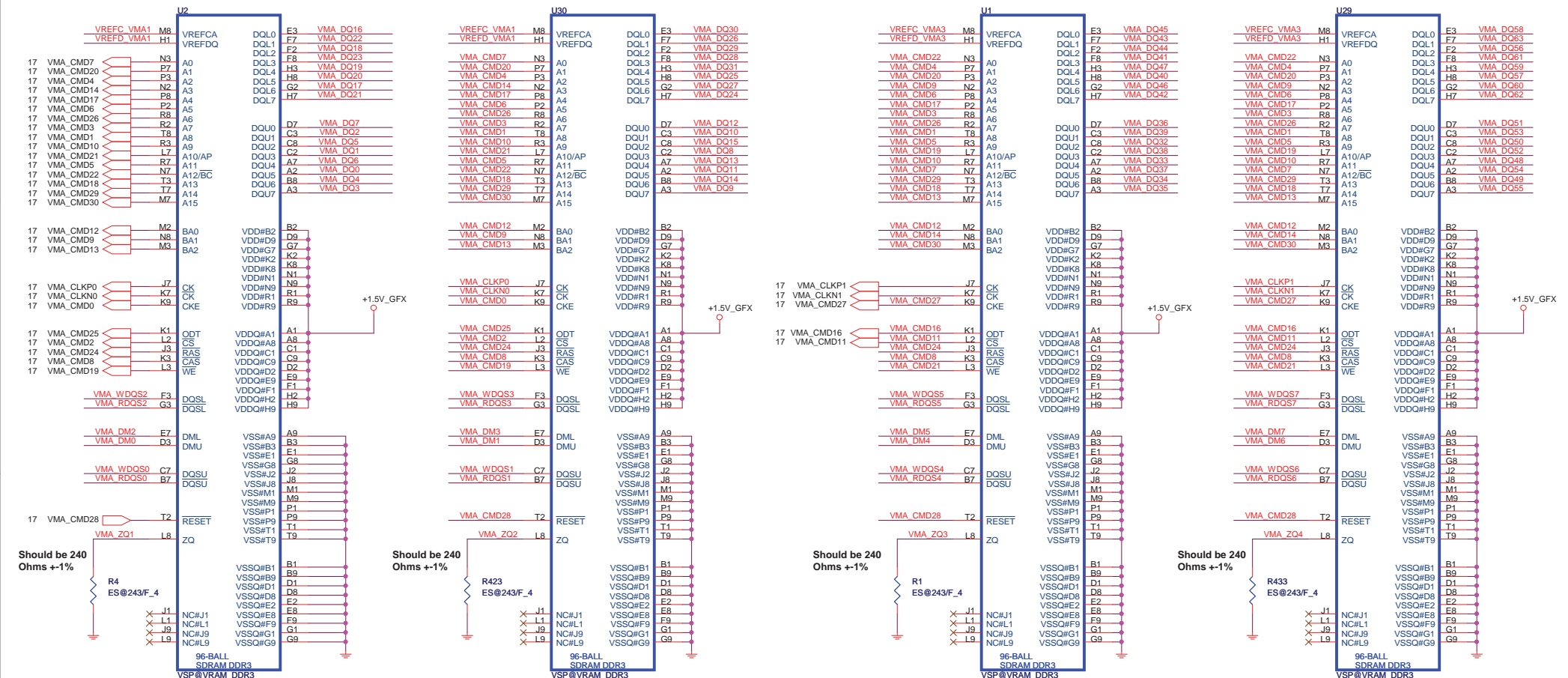
ES@ --> External VGA SKU

VSP@ --> Operation P/N (VGA-VRAM)

17 VMA\_DQ[63..0]  
17 VMA\_DM[7..0]  
17 VMA\_WDQS[7..0]  
17 VMA\_RDQS[7..0]



# CHANNEL A: 256MB/512MB DDR3

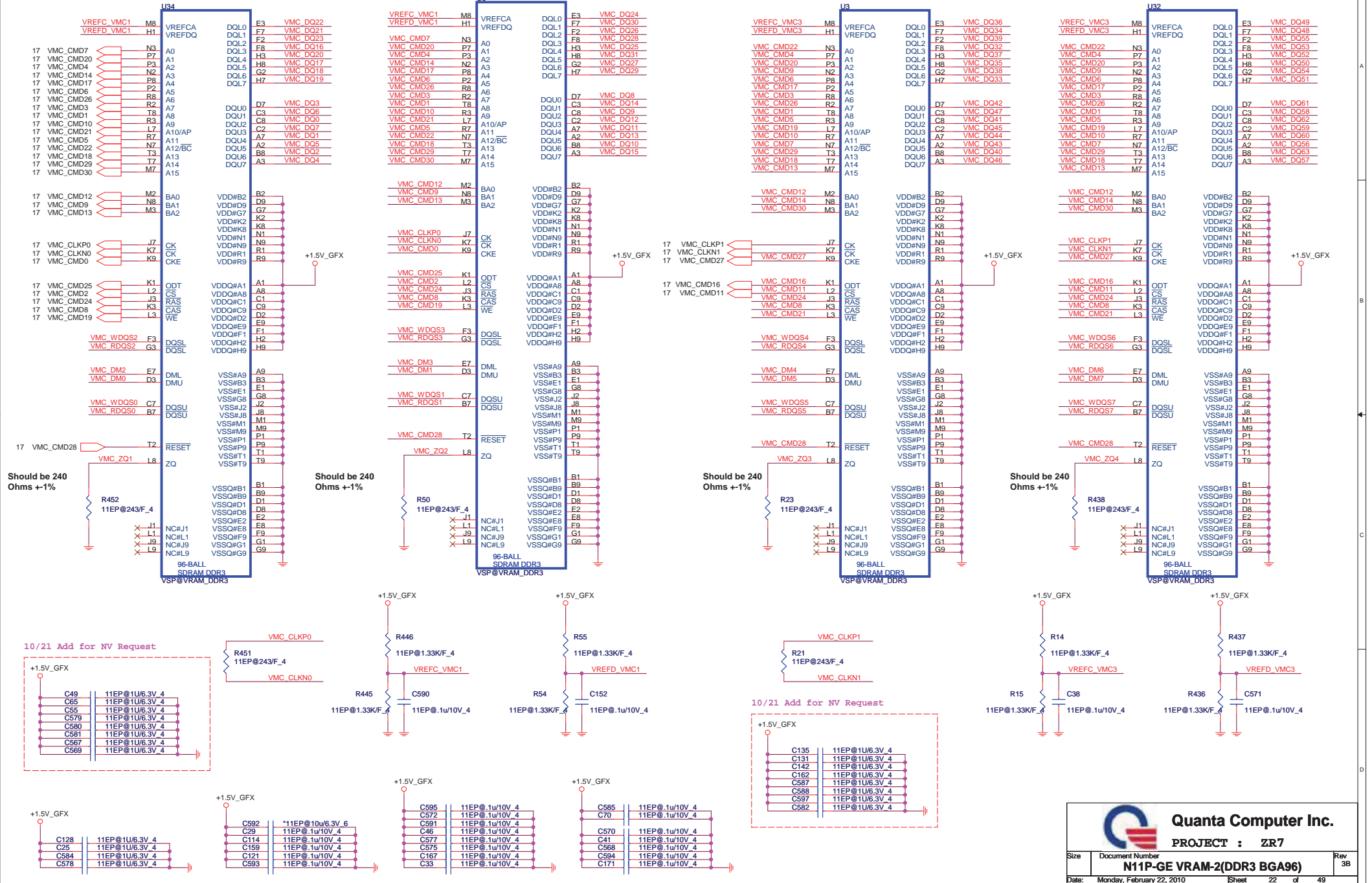


**Quanta Computer Inc.**  
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	<b>N11P-GE VRAM-1(DDR3 BGA96)</b>	3B
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**11EP@ --> N11P/N11E-GE1 Setting**  
**VSP@ --> Operation P/N (VGA-VRAM CH:B N11P/N11E only)**

# CHANNEL B: 256MB/512MB DDR3



**Quanta Computer Inc.**

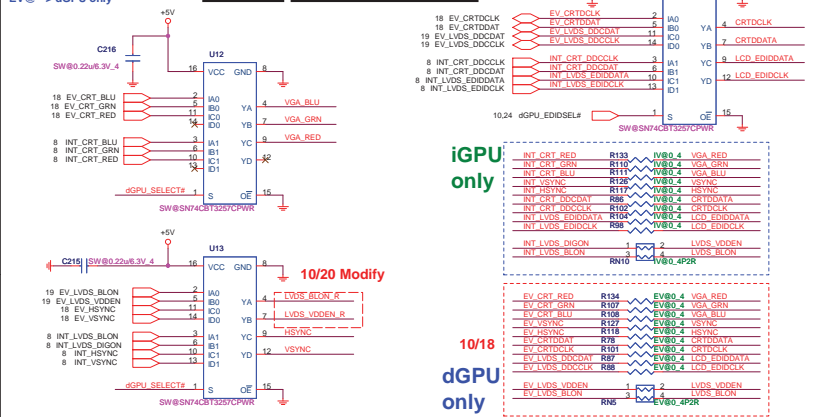
**PROJECT : ZR7**

Size	Document Number	Rev
	<b>N11P-GE VRAM-2(DDR3 BGA96)</b>	3B
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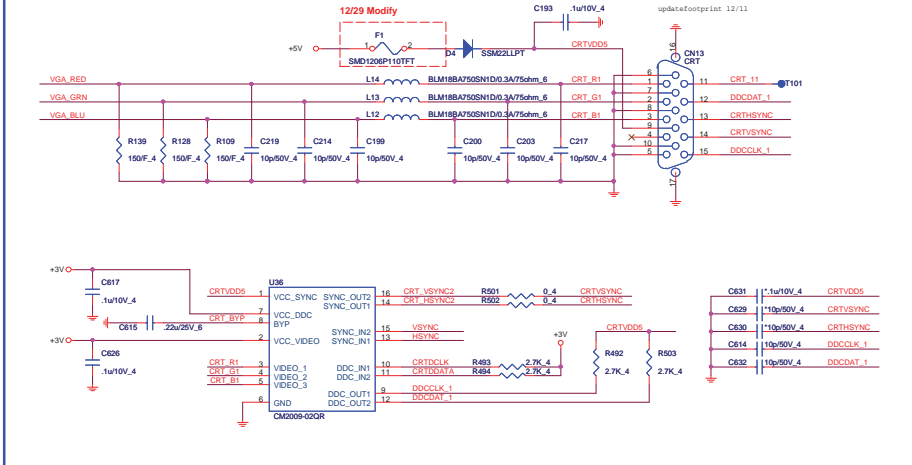
### CRT Switch

SW@ -> iGPU & dGPU Switch  
 IV@ -> iGPU only  
 EV@ -> dGPU only

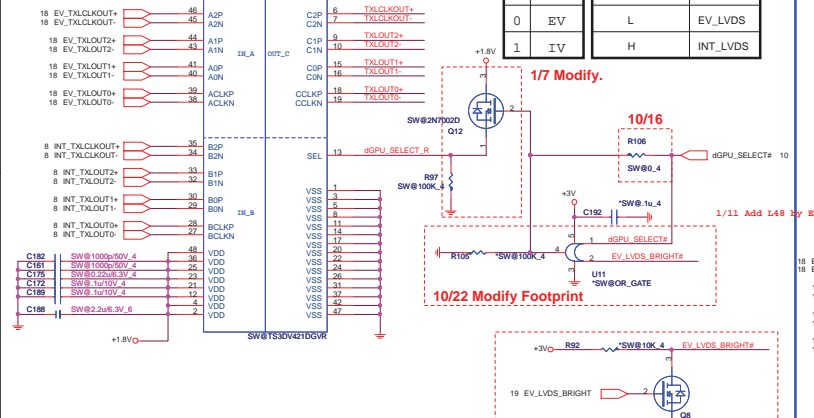
S	Yn	dGPU_SELECT#	Output
0	EV	L	EV_LVDS/CRT
1	IV	H	INT_LVDS/CRT



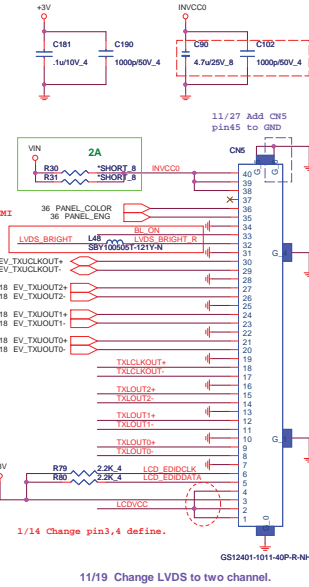
### CRT



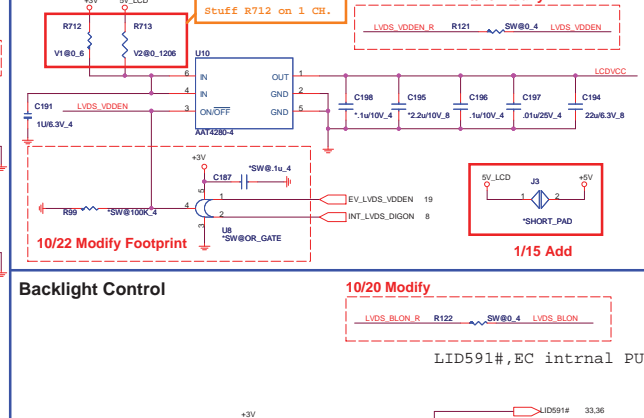
### LVDS Switch



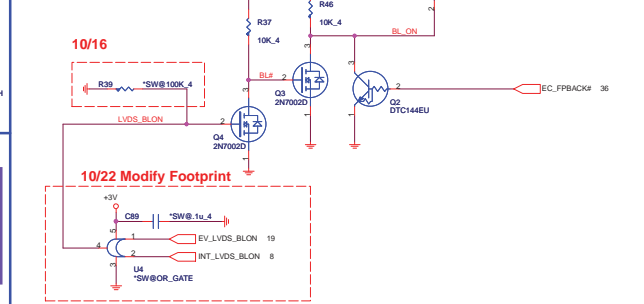
### LVDS



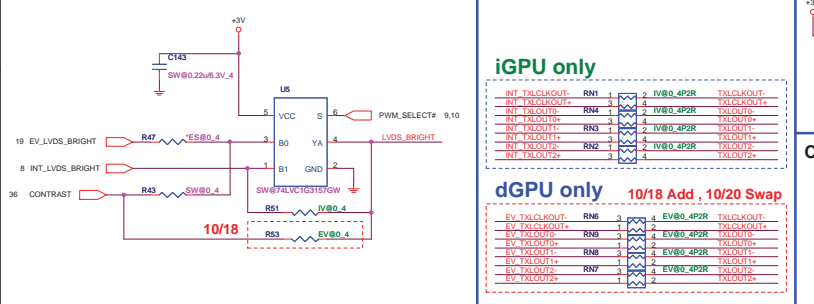
### LCD\_ON (LCD Power)



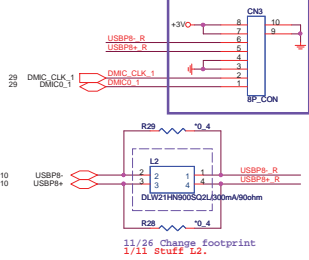
### Backlight Control



### Brightness



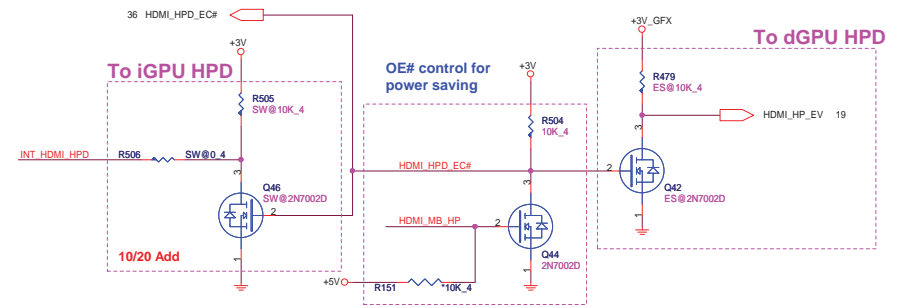
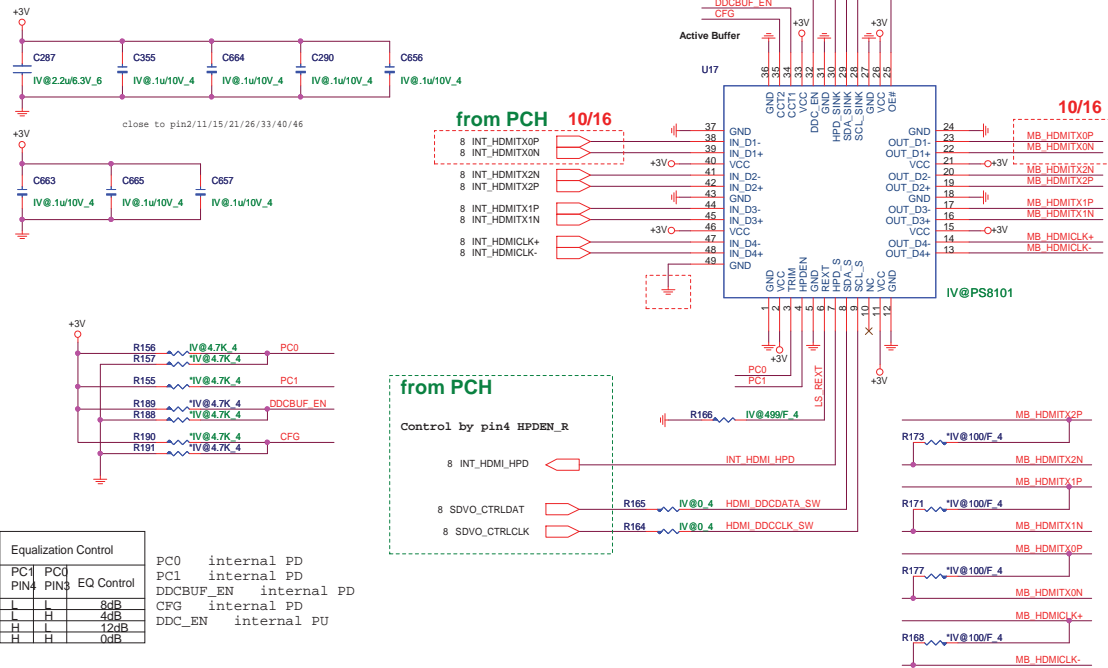
### CCD & MIC



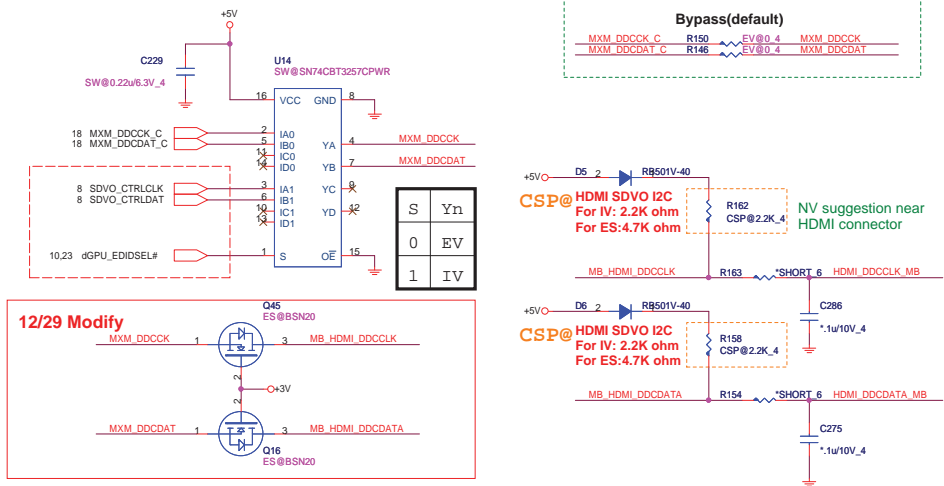
**Quanta Computer Inc.**  
 PROJECT : ZR7  
 Size Document Number CRT/LVDS/CAMERA/LID Rev 3B  
 Date Monday, February 22, 2010 Sheet 23 of 49

# iGPU HDMI LEVEL SHIFTER

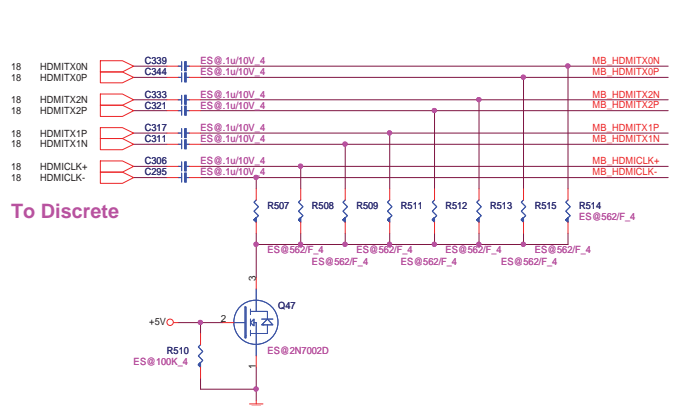
- IV@ -> iGPU only
- EV@ -> dGPU only
- ES@ -> External VGA SKU
- SW@ -> iGPU & dGPU Switch
- CSP@ -> Operation P/N



# SDVO I2C Control



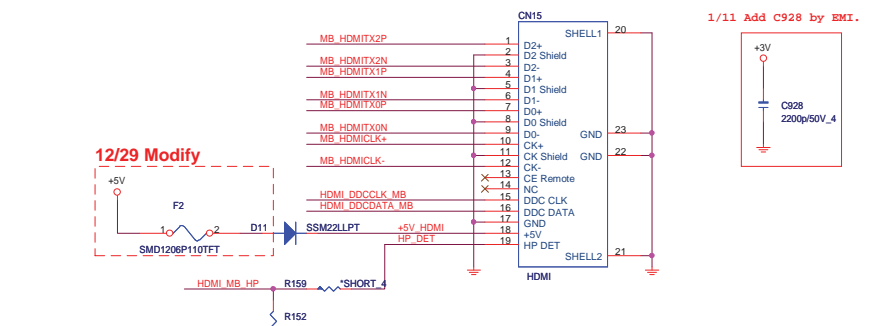
# GPU Switchable Graphic HDMI source



# ESD Protect

12/29 Delete U15, U16, U18.

# HDMI connector



**Quanta Computer Inc.**

**PROJECT : ZR7**

**HDMI (PS8101)**

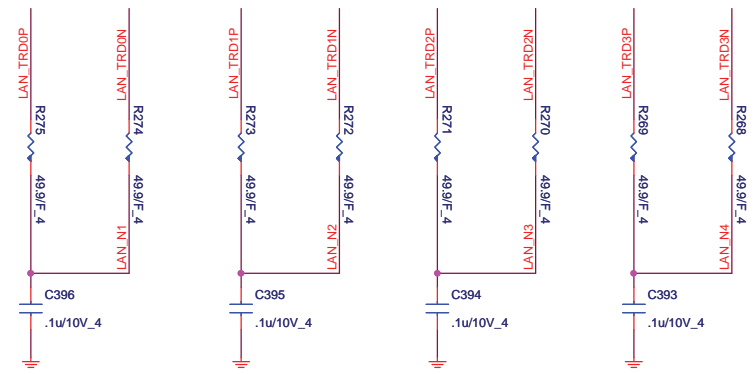
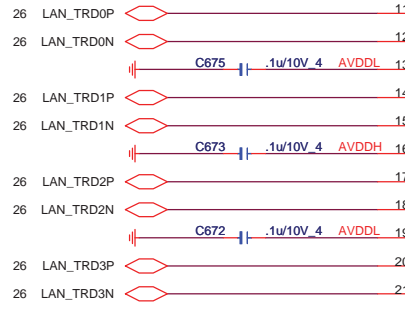
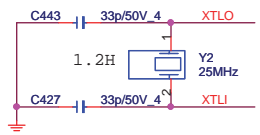
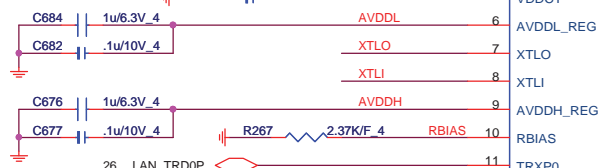
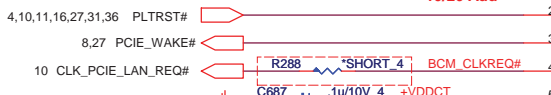
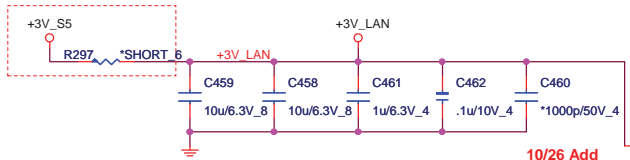
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		3B

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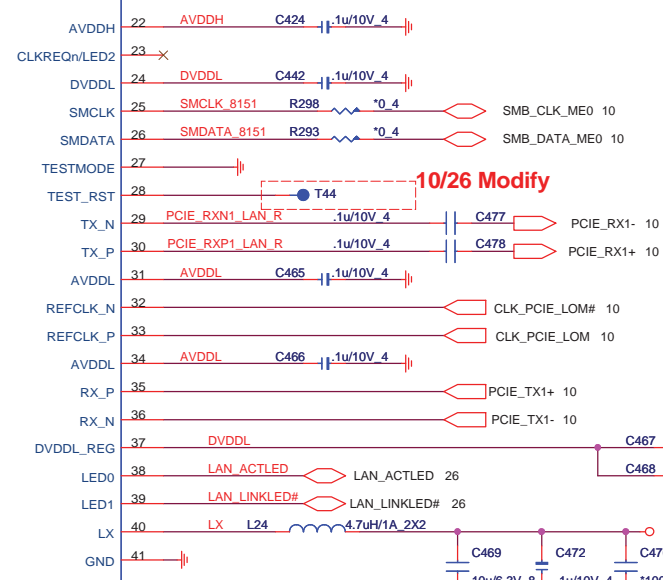
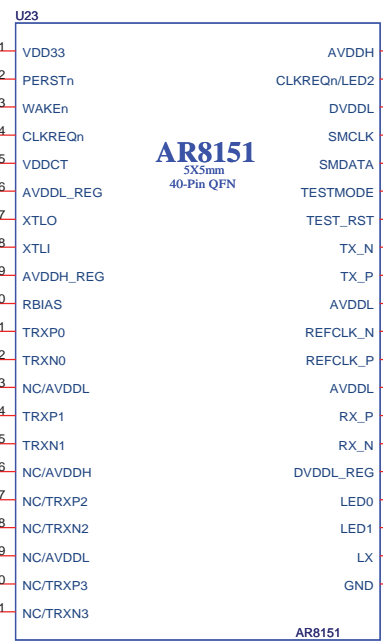


# Giga-LAN AR8151

10/26 Add



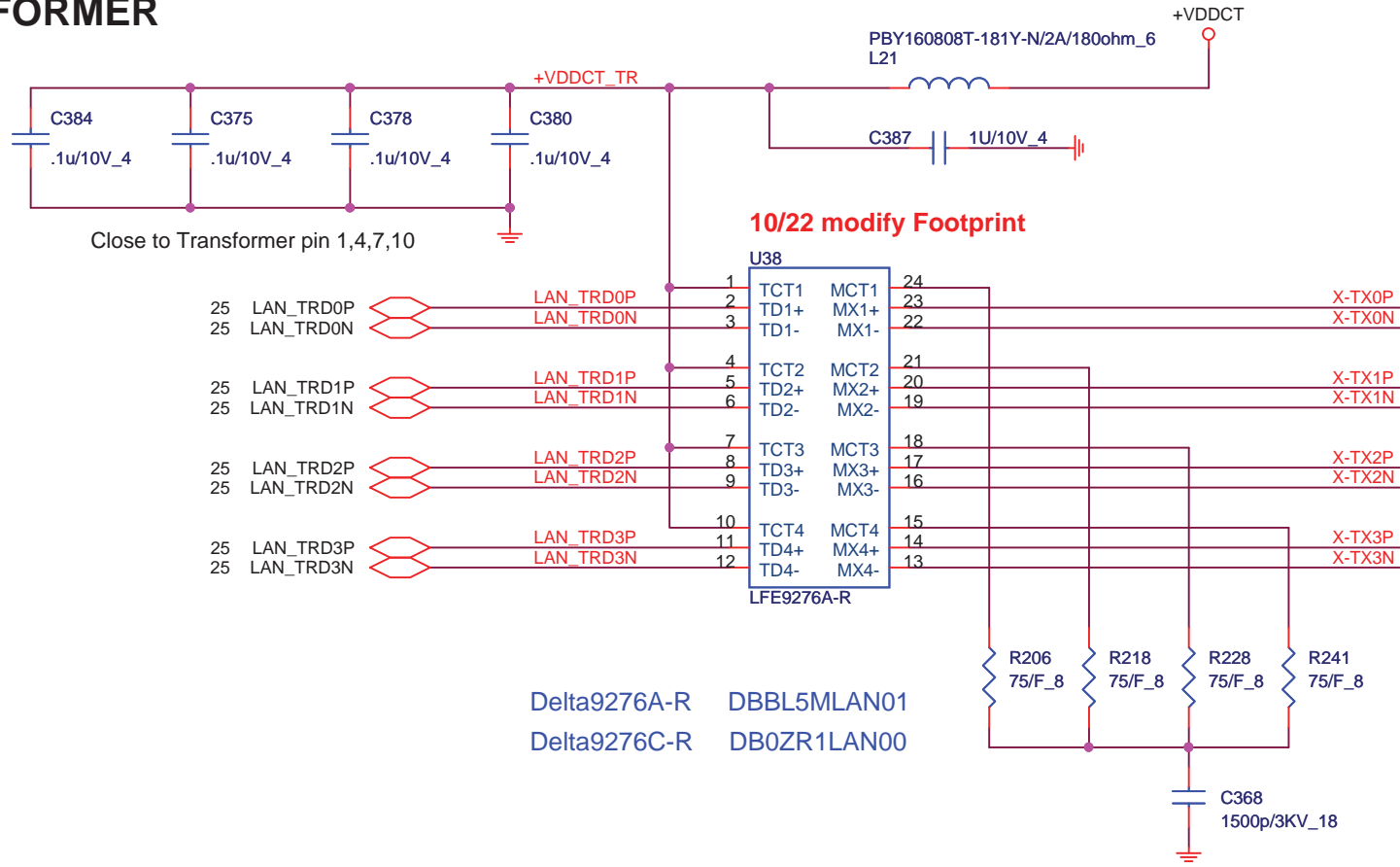
AR8151  
5X5mm  
40-Pin QFN



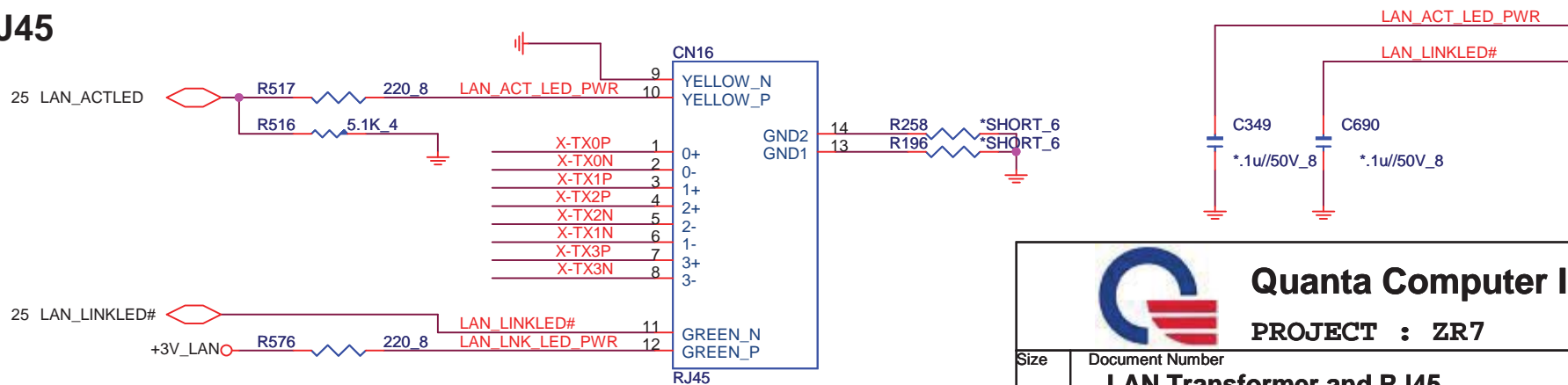
10/26 Modify

		<b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>	
		Size Document Number <b>GLAN BCM57780</b>	Rev 3B
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# TRANSFORMER



# RJ45



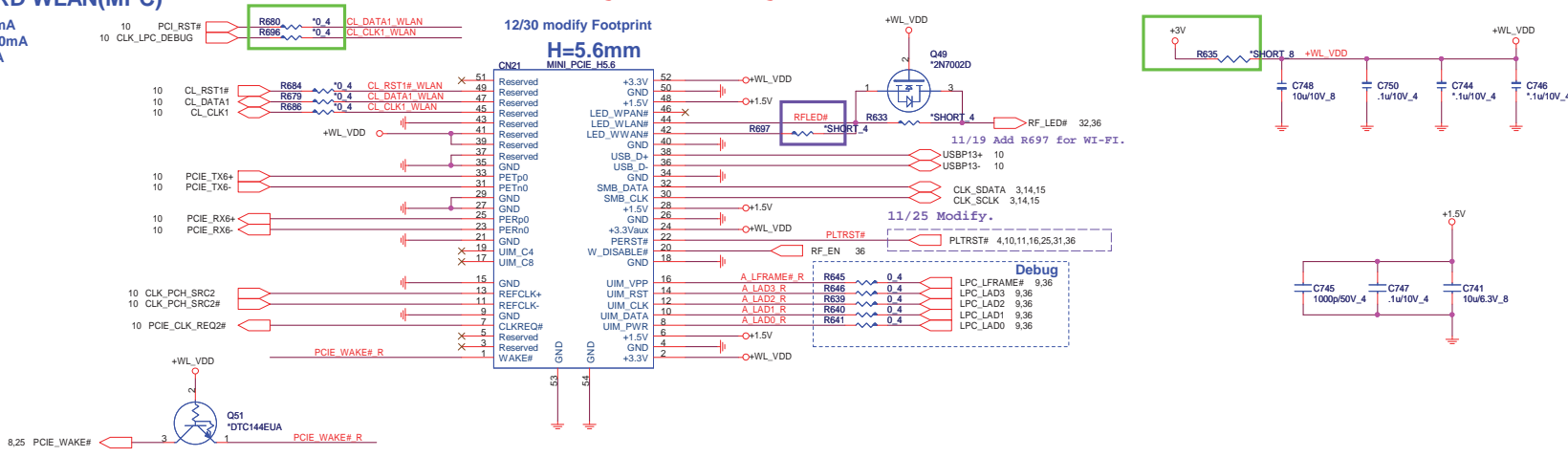
**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	<b>LAN Transformer and RJ45</b>	3B
Date:	Monday, February 22, 2010	Sheet 26 of 49

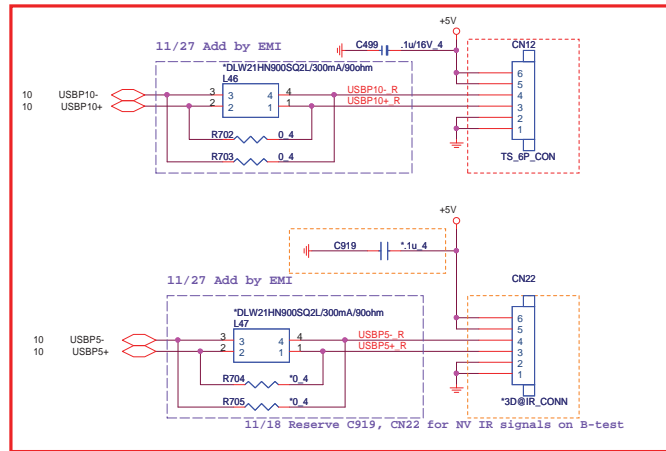
# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
 +3.3Vaux: 330mA  
 +1.5V: 500mA

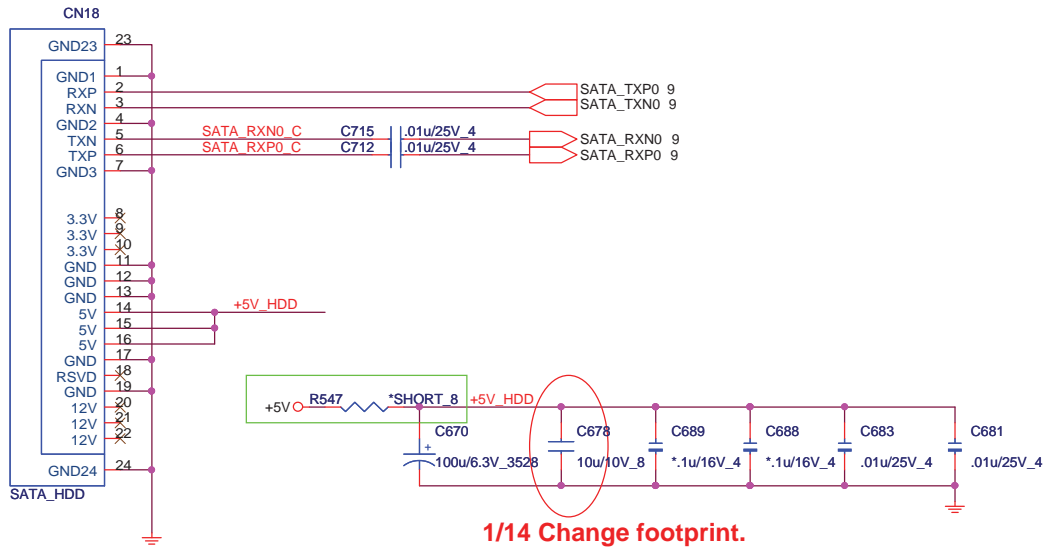
Check LED signal. (active high or low)



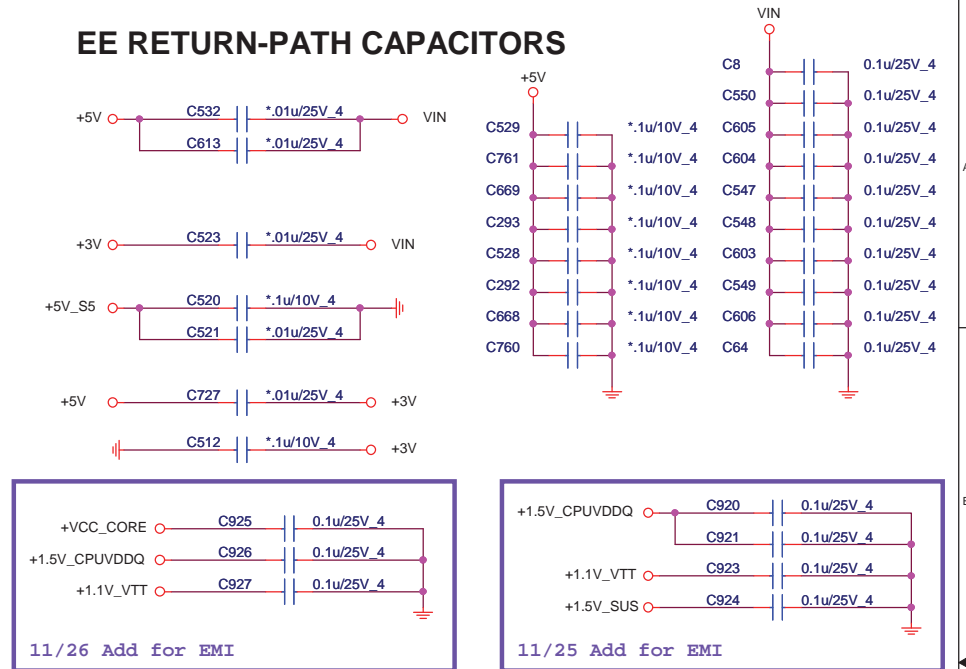
## 1/8 Change CN12, CN22 6pin conn footprint for Touch Screen.



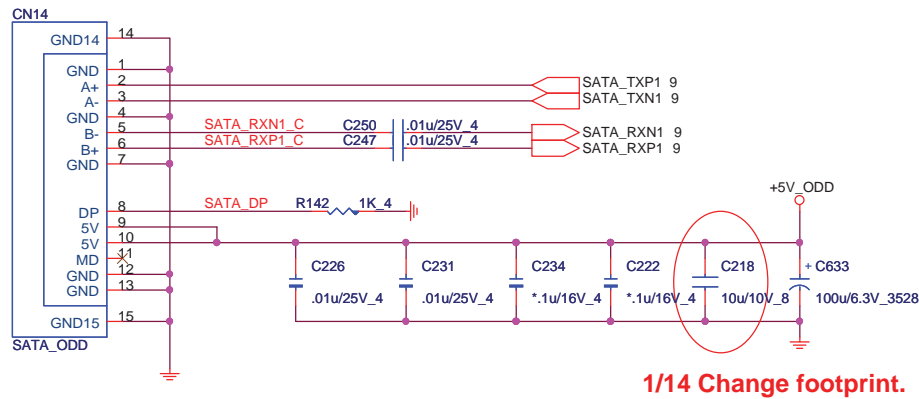
### MAIN SATA HDD



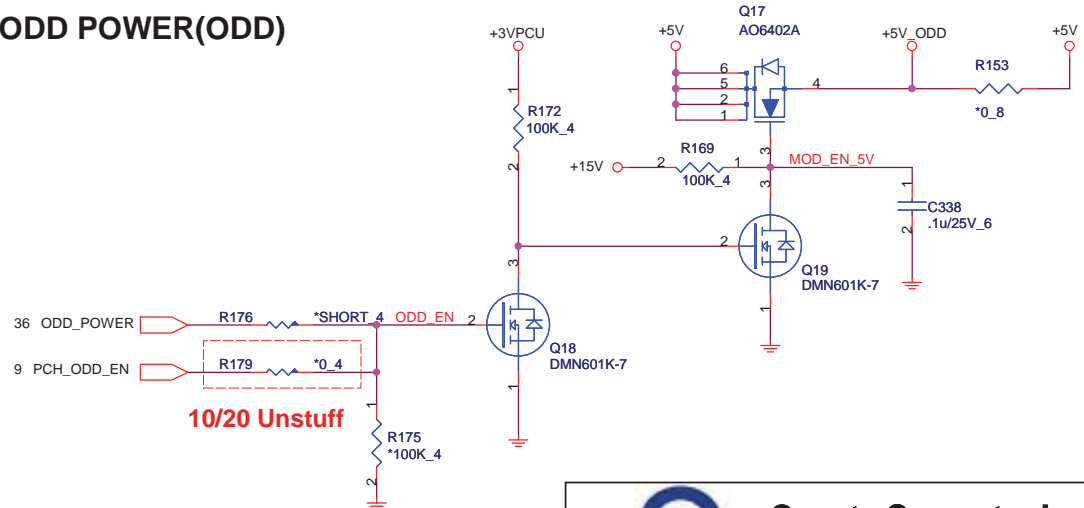
### EE RETURN-PATH CAPACITORS




### ODD (SATA)



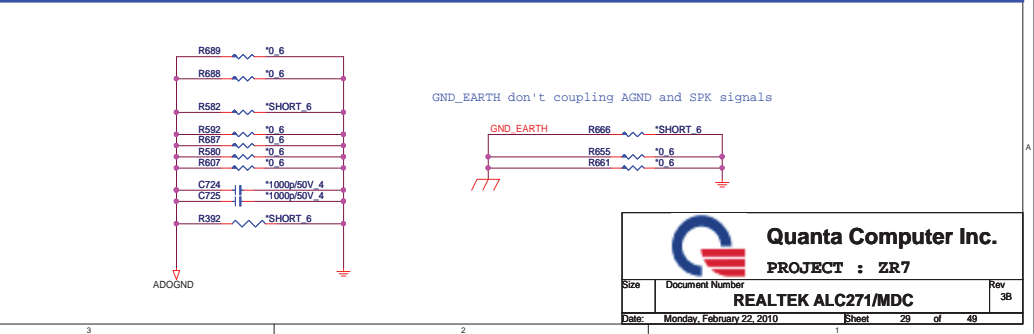
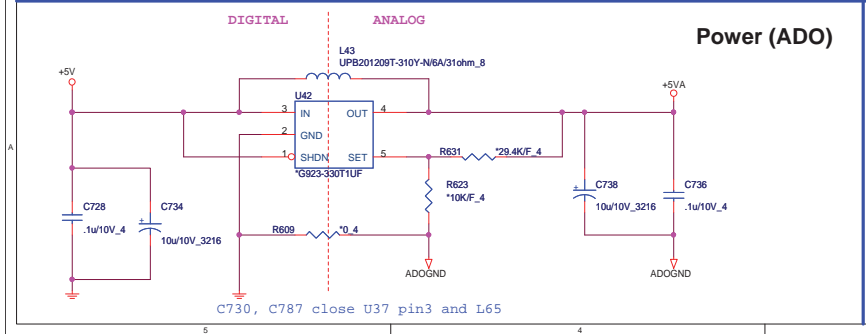
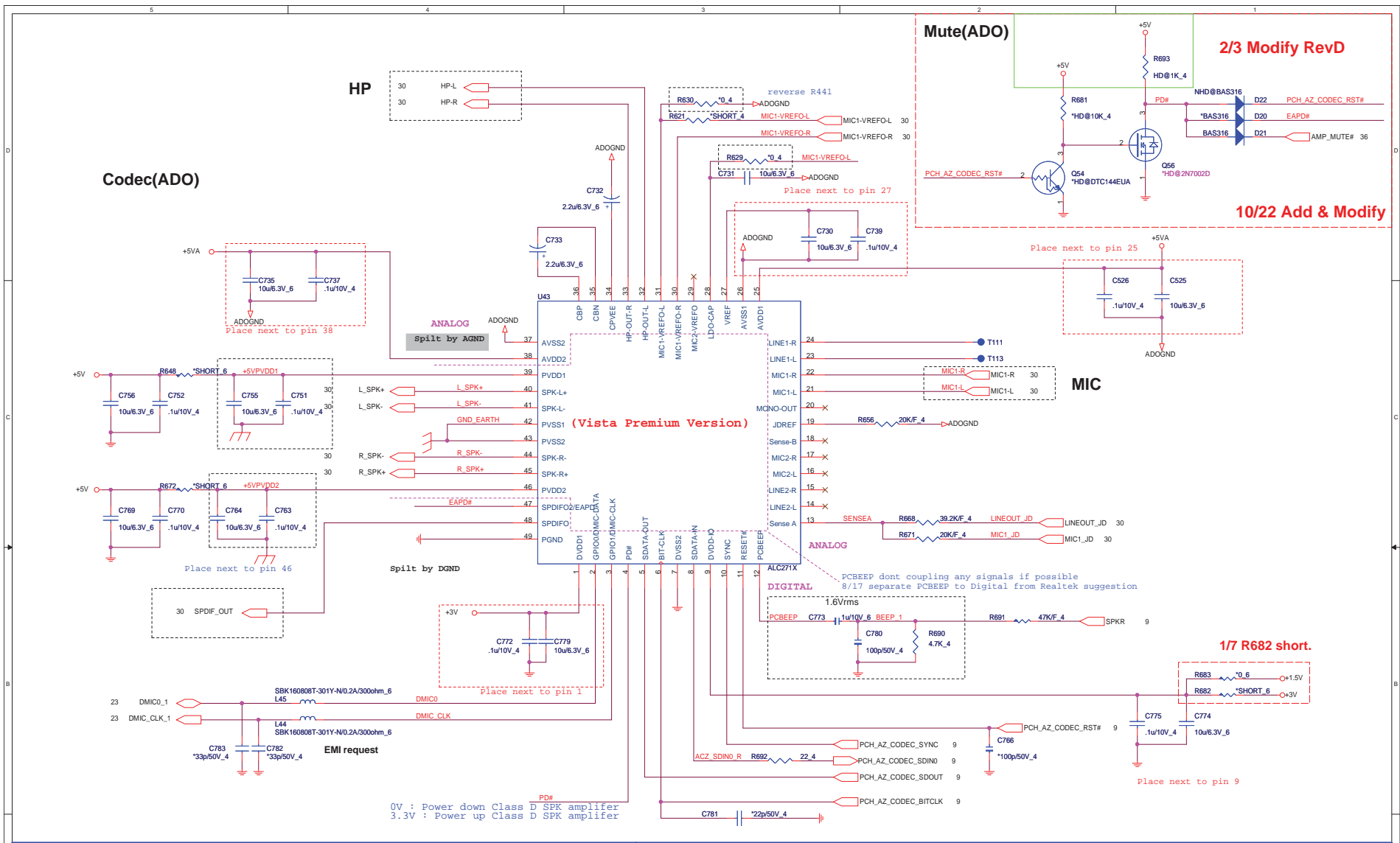
### ODD POWER(ODD)





**Quanta Computer Inc.**  
PROJECT : ZR7

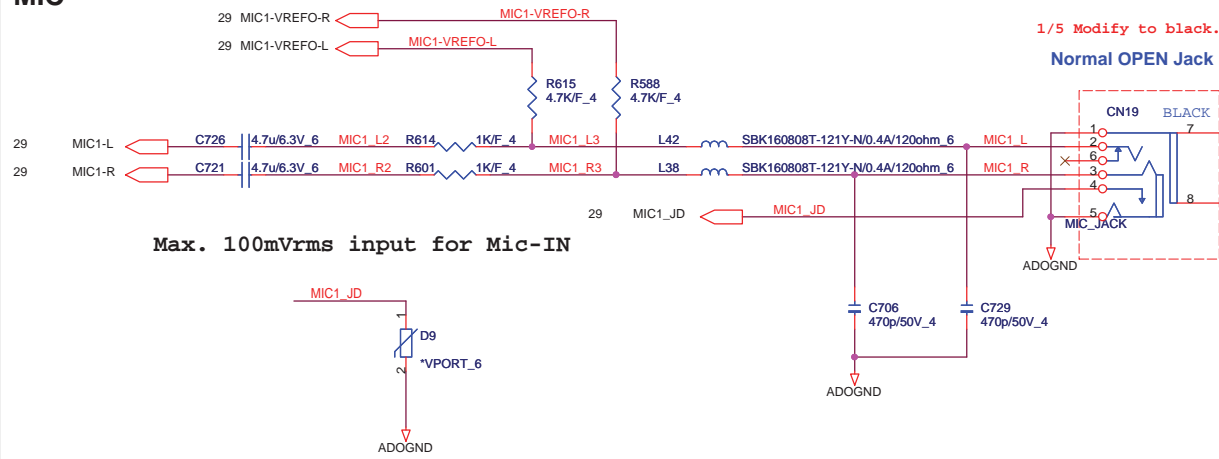
Size	Document Number	Rev
	<b>SATA-HDD/ODD/USB-ESATA</b>	3B
Date:	Monday, February 22, 2010	Sheet 28 of 49



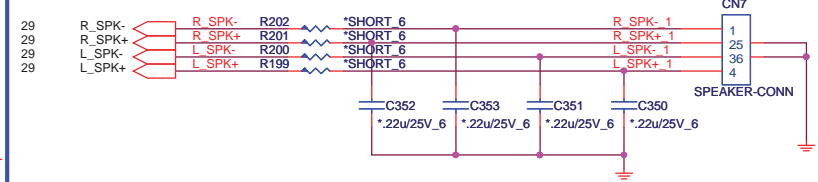
**Quanta Computer Inc.**  
**PROJECT : ZR7**  
**REALTEK ALC271/MDC**

Size	Document Number	Rev
		38
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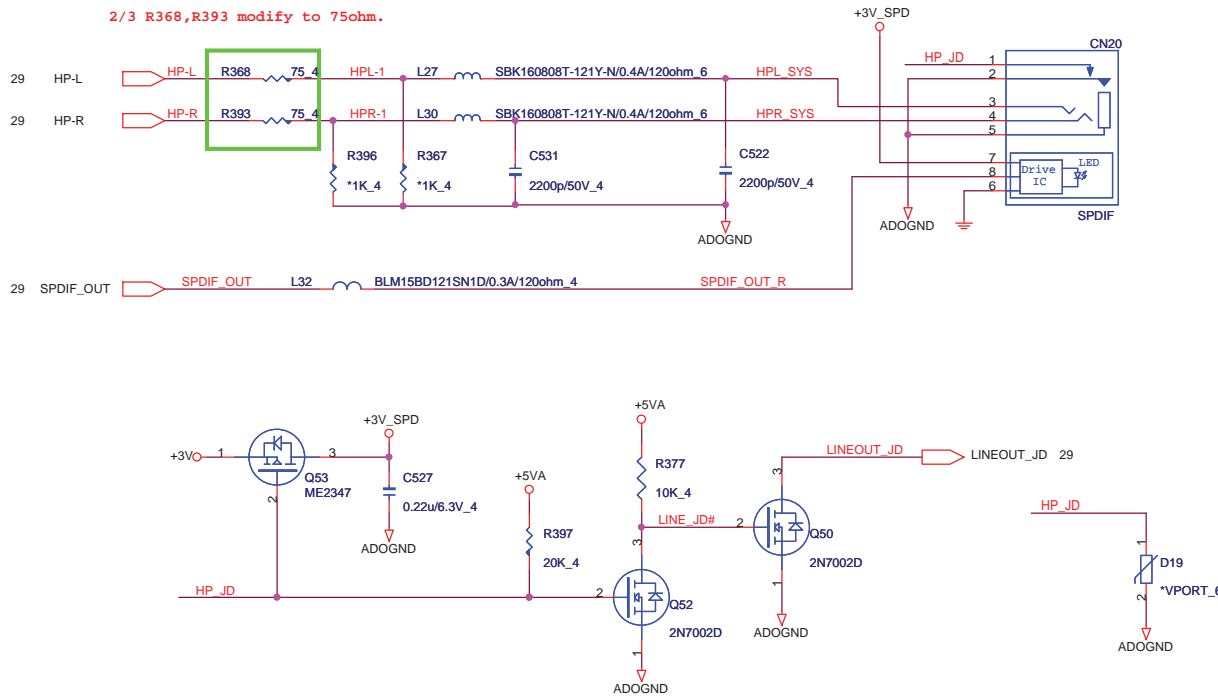
### MIC




### Internal Speaker

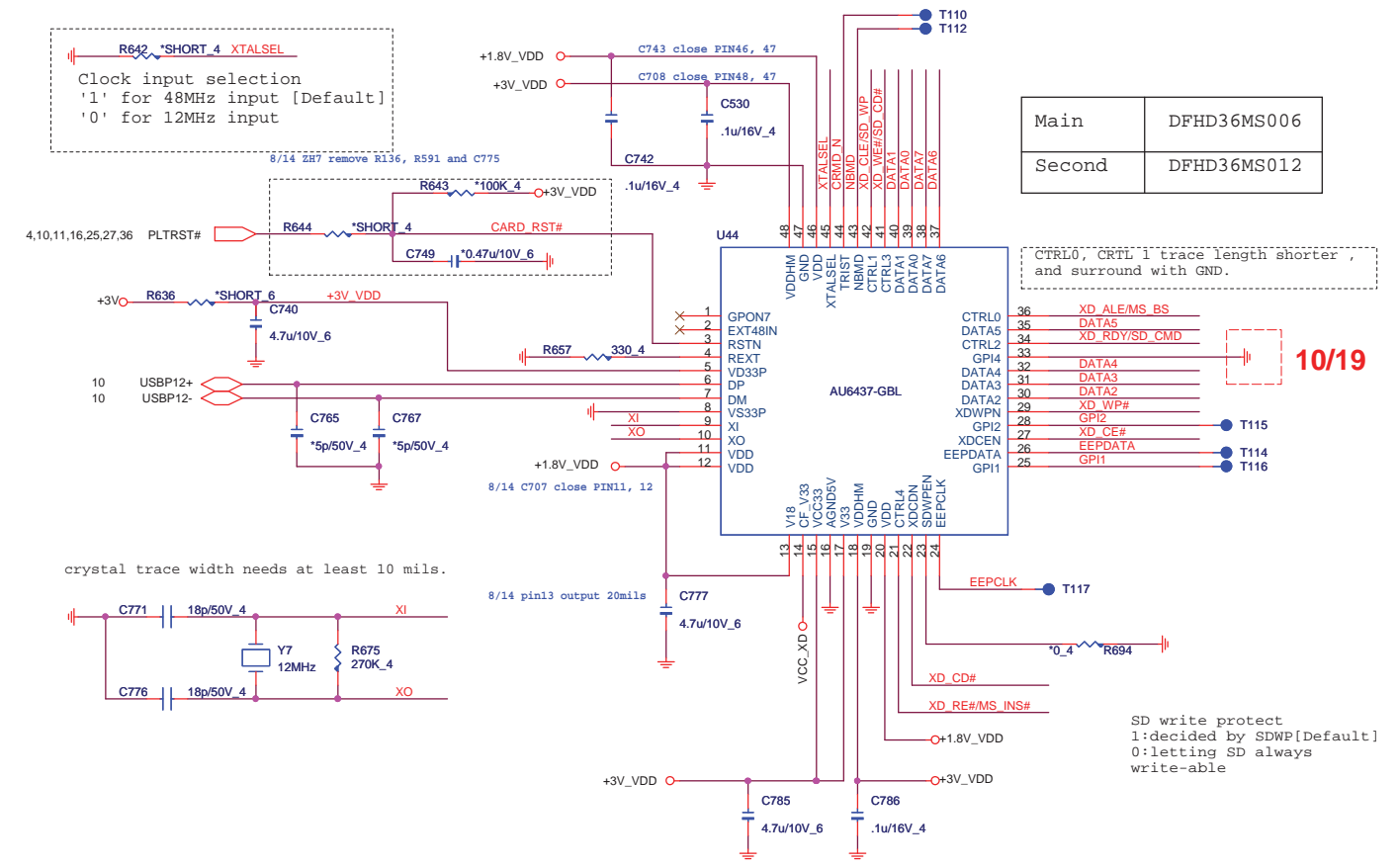


### HP/SPDIF

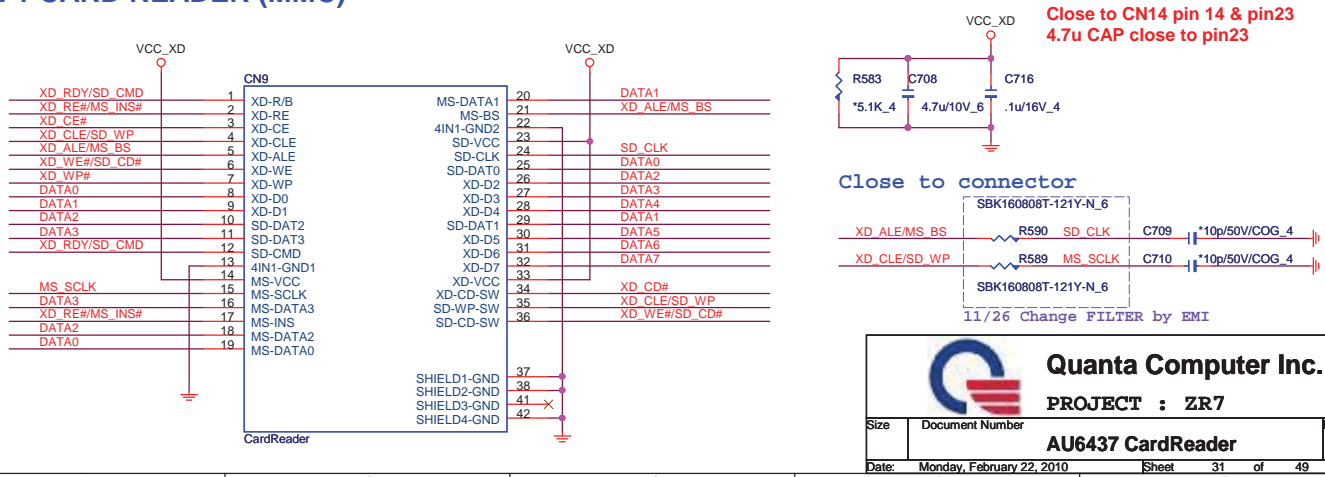


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>			Rev 3B
<b>AMP /AUDIO JACK CONN</b>			Sheet 30 of 49
Date:	Monday, February 22, 2010		

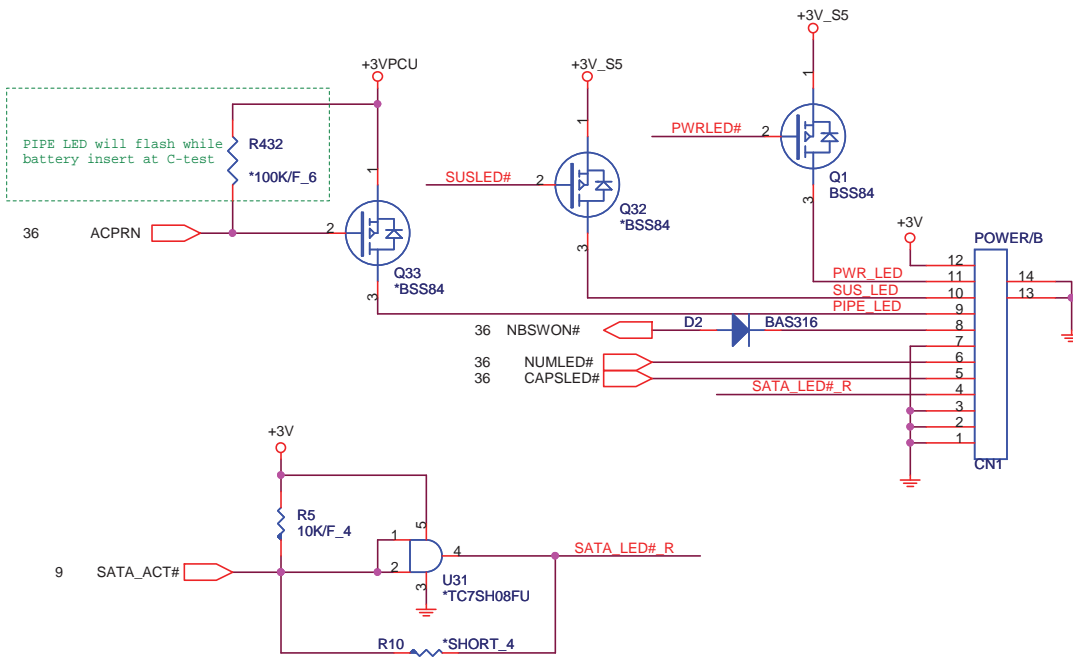
# CARD READER Controller



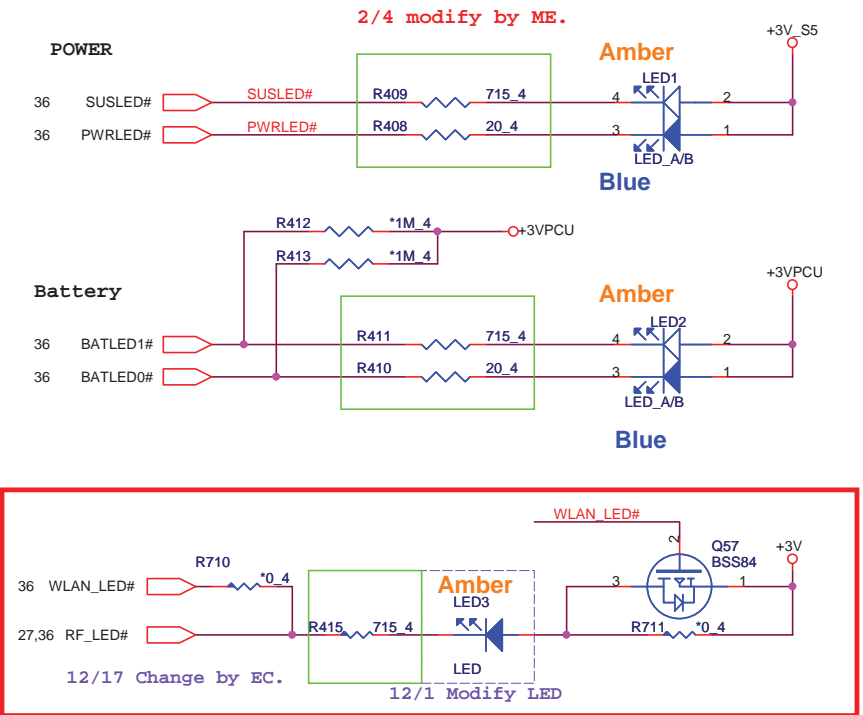
## 4 IN 1 CARD READER (MMC)



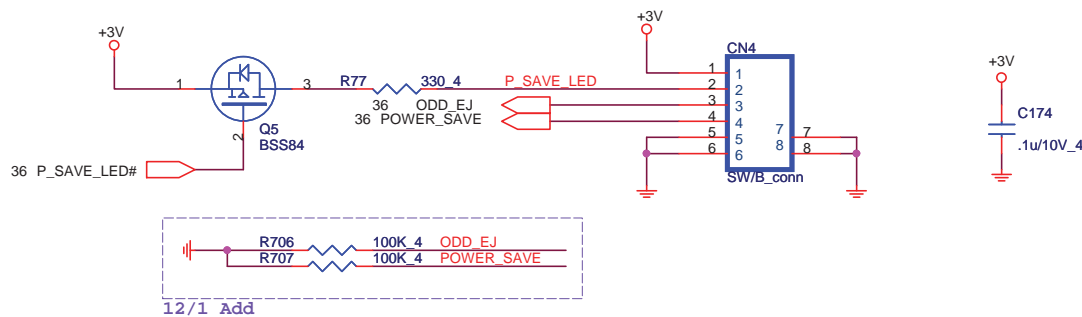
# POWER BOARD CONN(UIF)



# LED



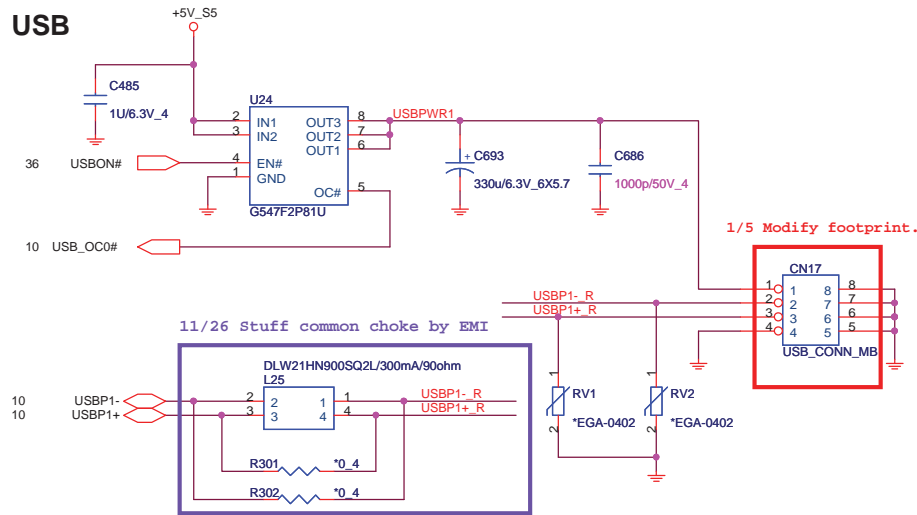
# SW /B



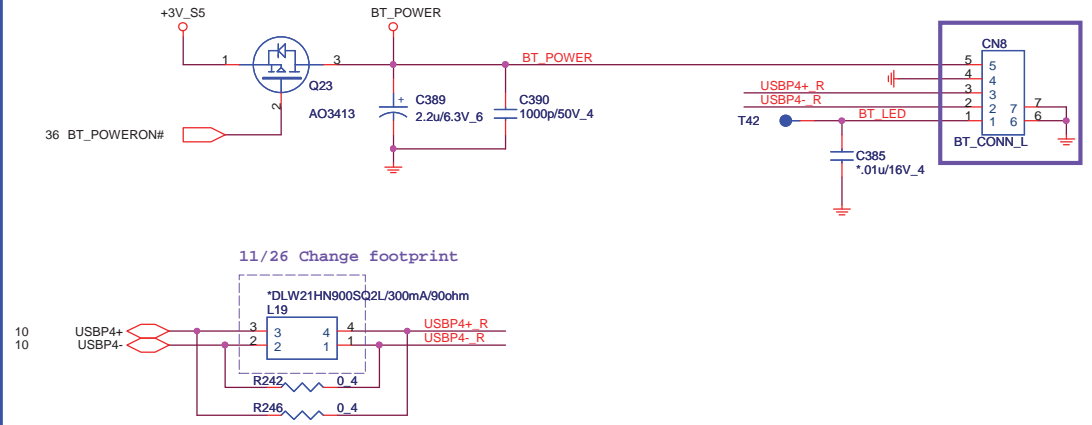
		<b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>
Size	Document Number	Rev
	<b>POWER/MMB/LAUNCH/LED</b>	<b>3B</b>
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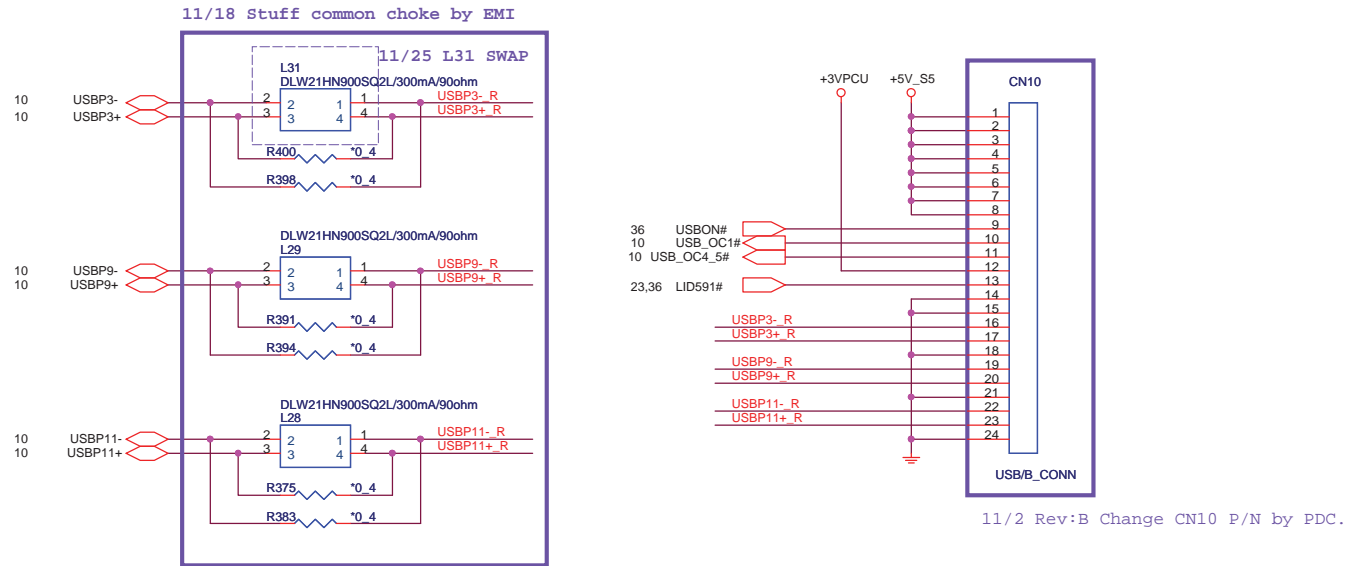
### USB



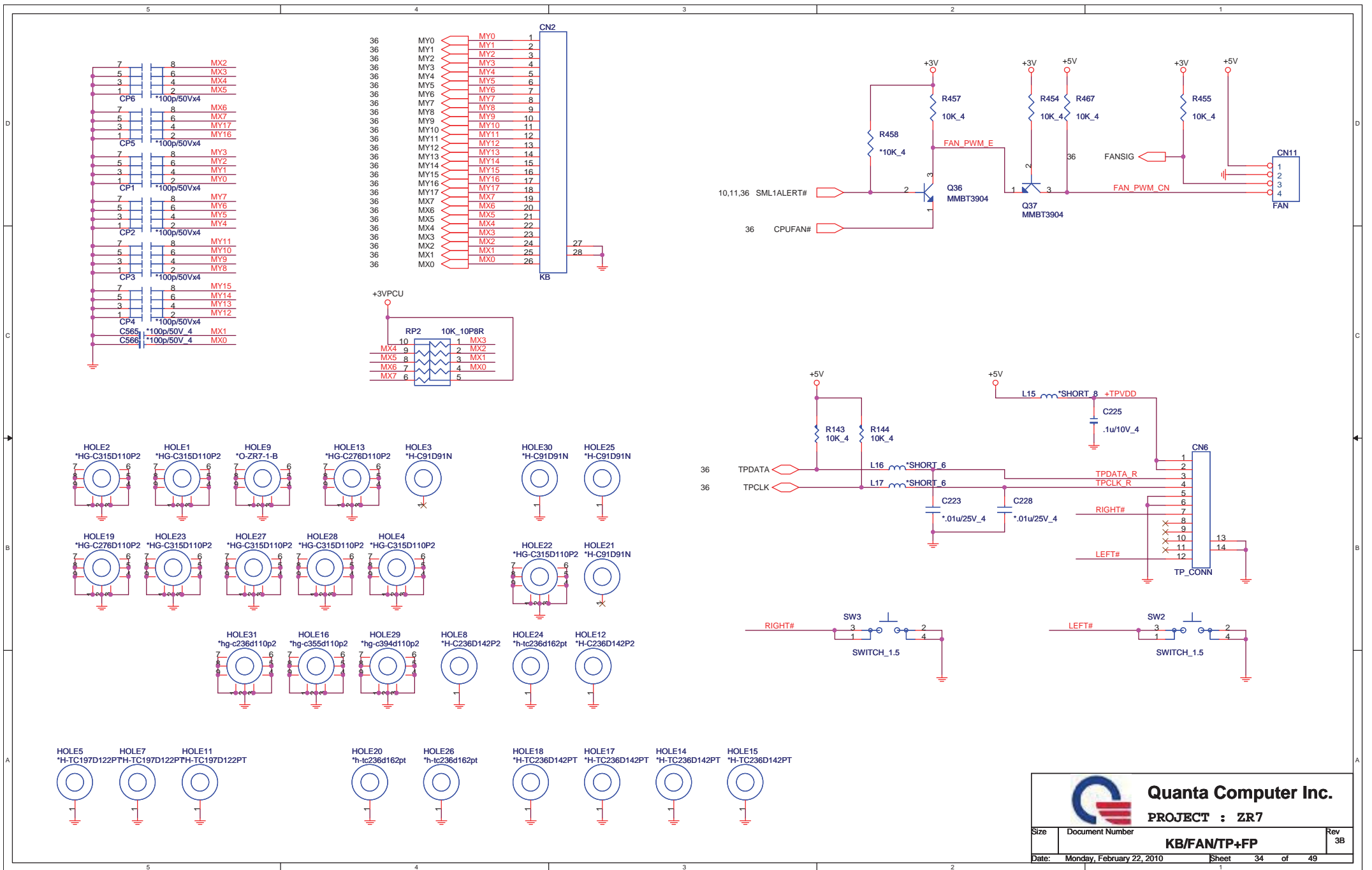
### BLUETOOTH CONNECTOR



### USB/B

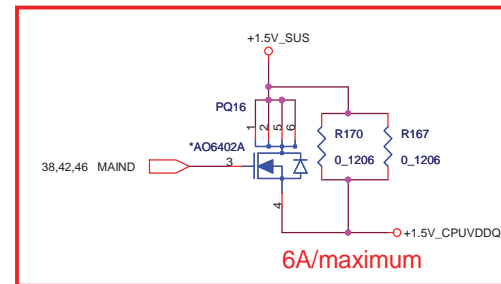
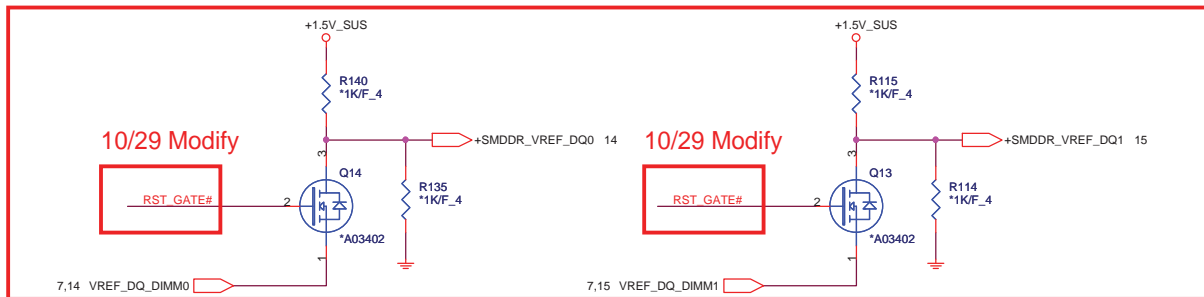
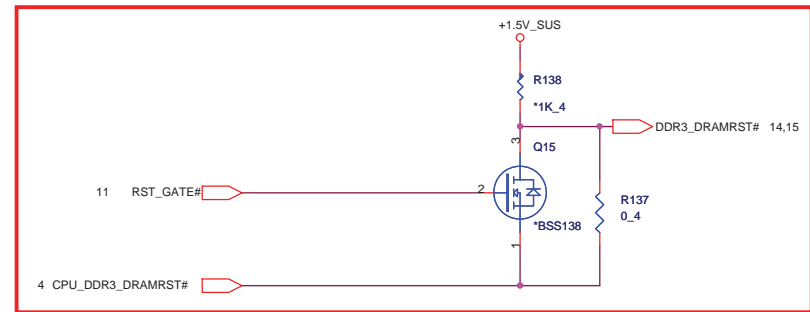
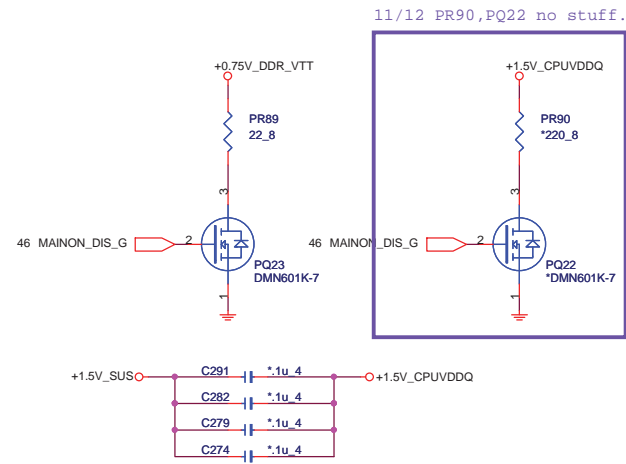
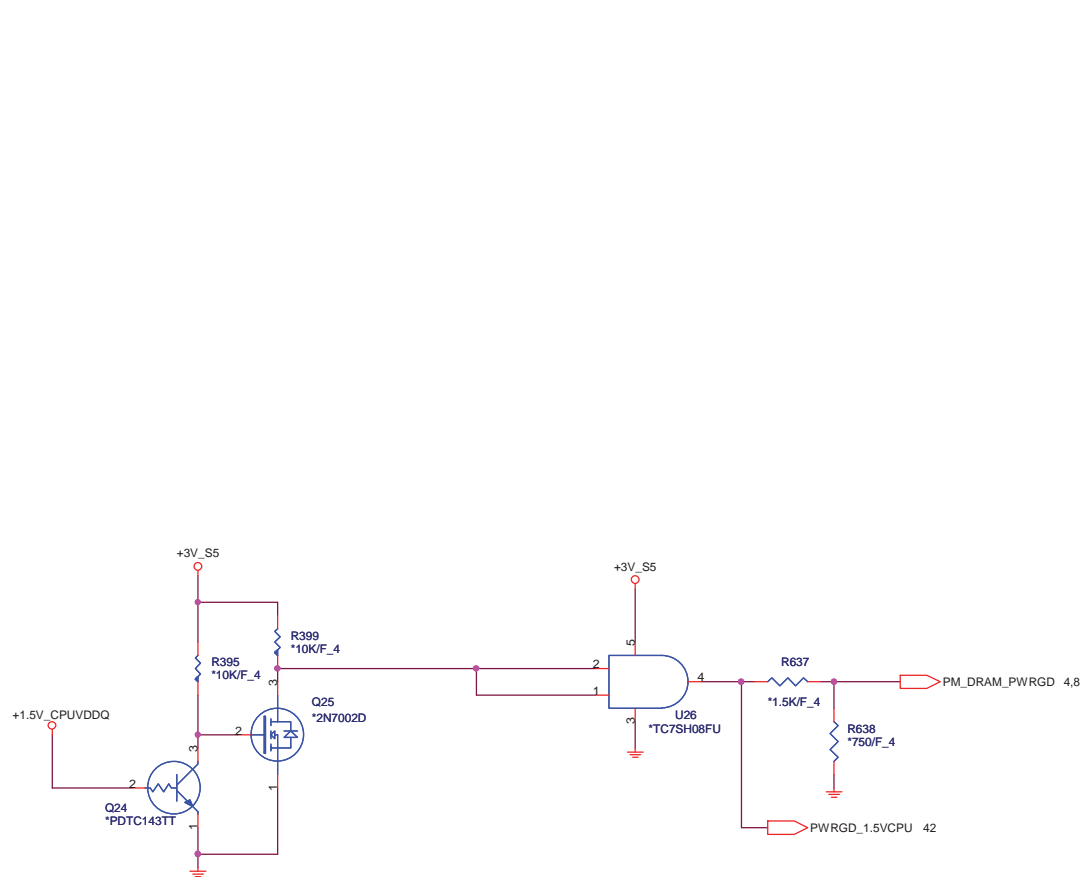


		<b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>	
		Size Document Number <b>USB/ BT</b>	Rev 3B
Date: Monday, February 22, 2010		Sheet 33 of 49	

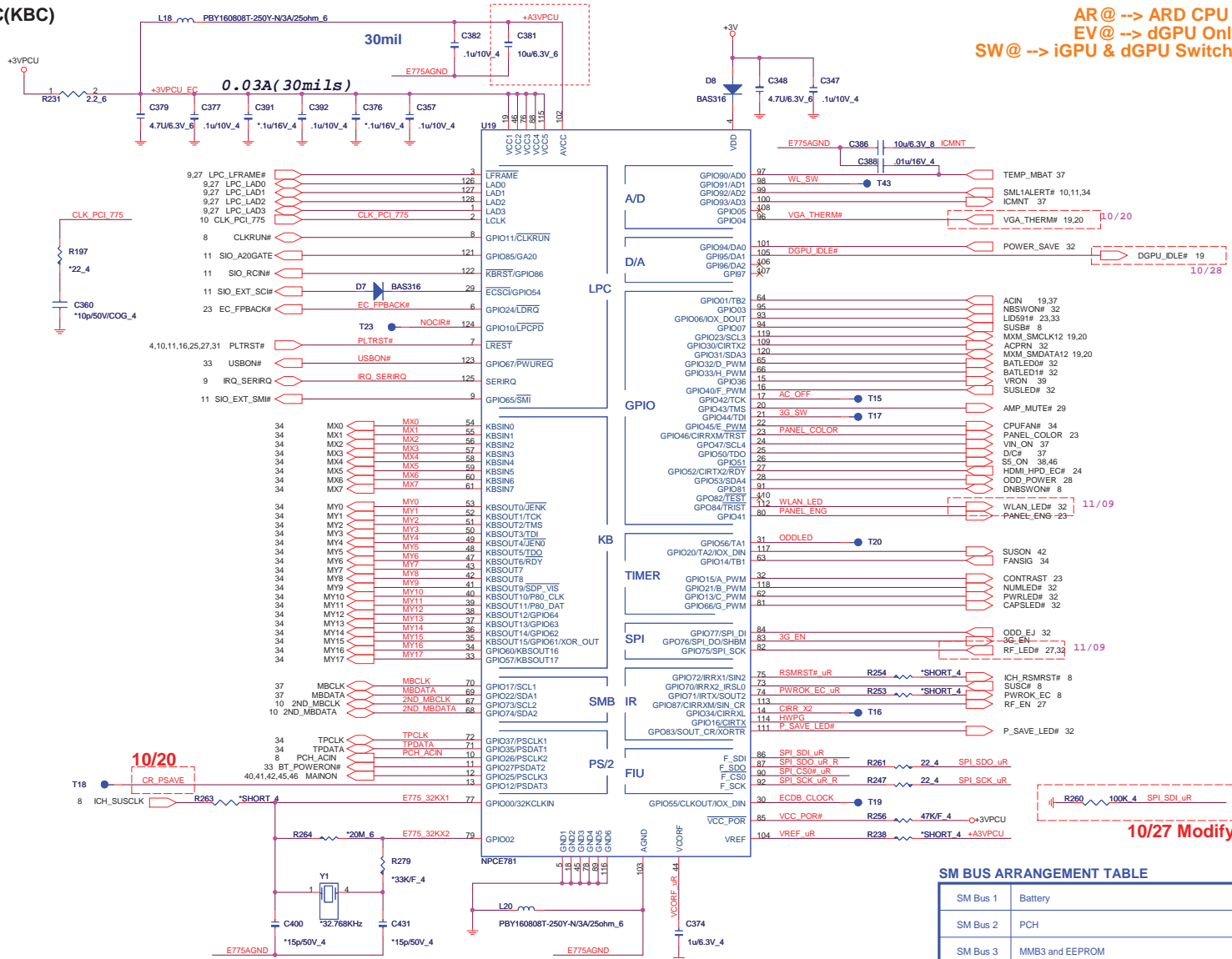


**Quanta Computer Inc.**  
**PROJECT : ZR7**

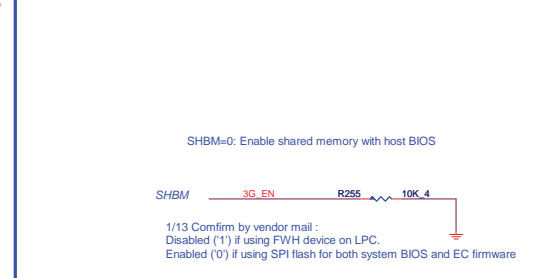
Size	Document Number	Rev
	<b>KB/FAN/TP+FP</b>	3B
Date:	Monday, February 22, 2010	Sheet 34 of 49



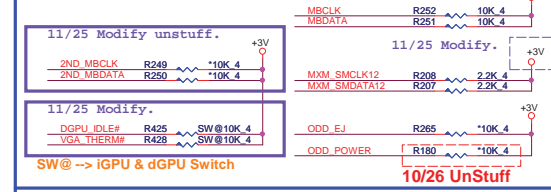
EC(KBC)



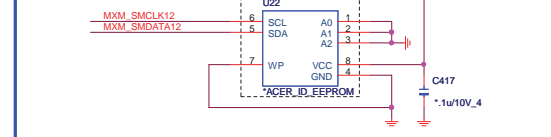
I/O ADDRESS SETTING(KBC)



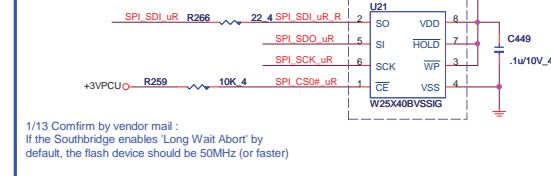
SM BUS PU(KBC)



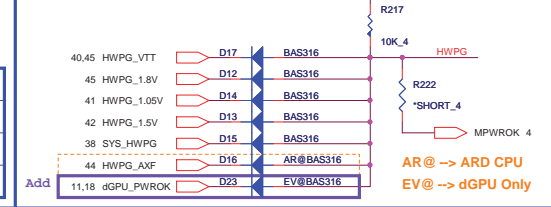
ACER ID(KBC)



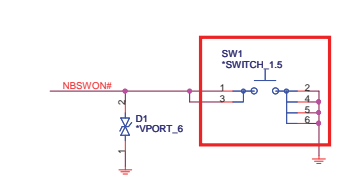
SPI FLASH(KBC)



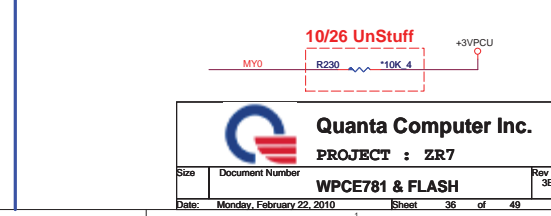
HWPG(KBC)

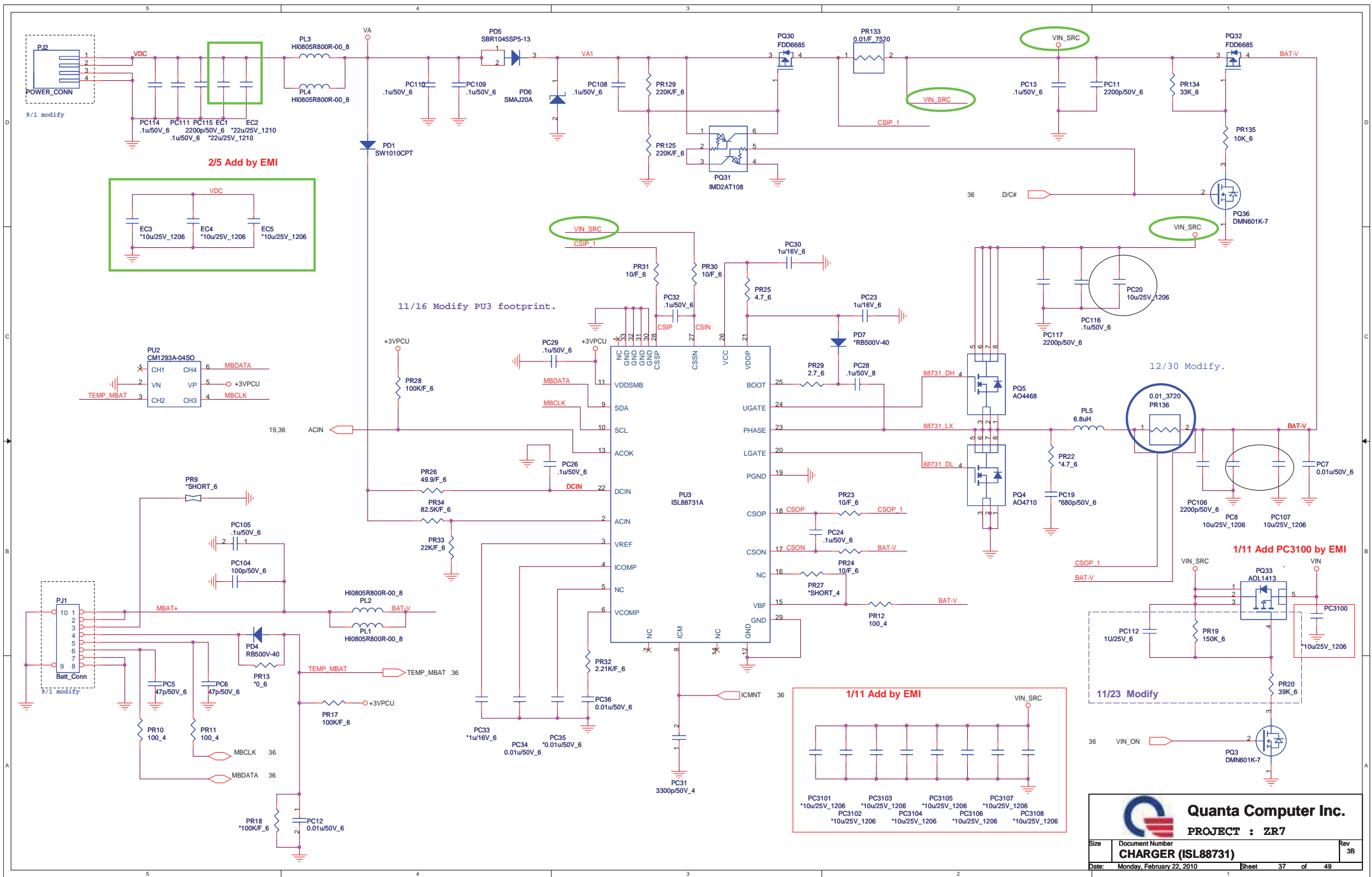


POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)





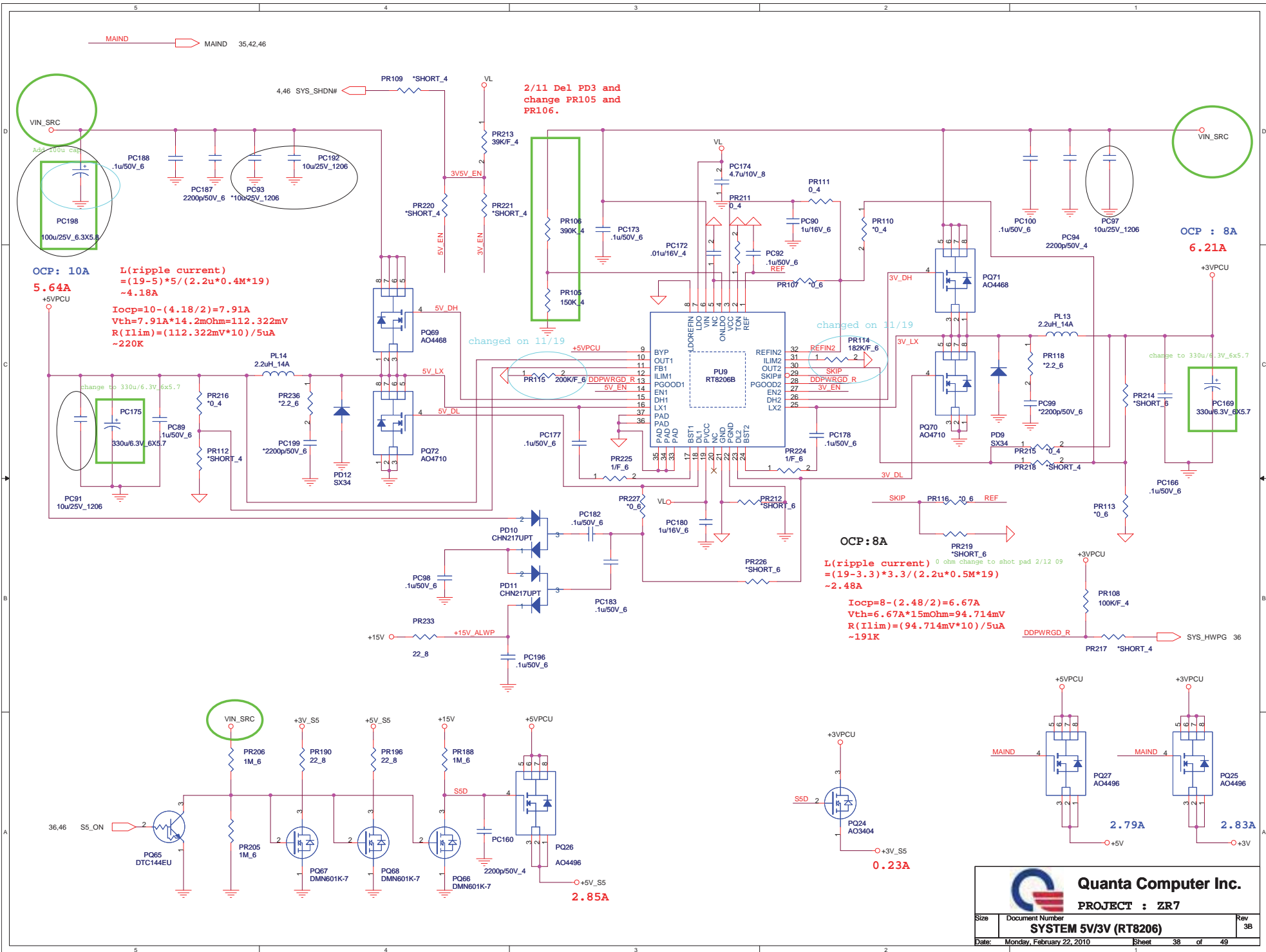
**Quanta Computer Inc.**

**PROJECT : ZR7**

**CHARGER (ISL88731)**

Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: 3B

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**Quanta Computer Inc.**  
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Size	Document Number	Rev
	<b>SYSTEM 5V/3V (RT8206)</b>	3B
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[PWM]  
PR73, PR72, PR73, PR74, PR75, PR76, and PR77 deleted

11/16 Modify PUS footprint.

Close to Phase 1 Inductor

Parallel

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

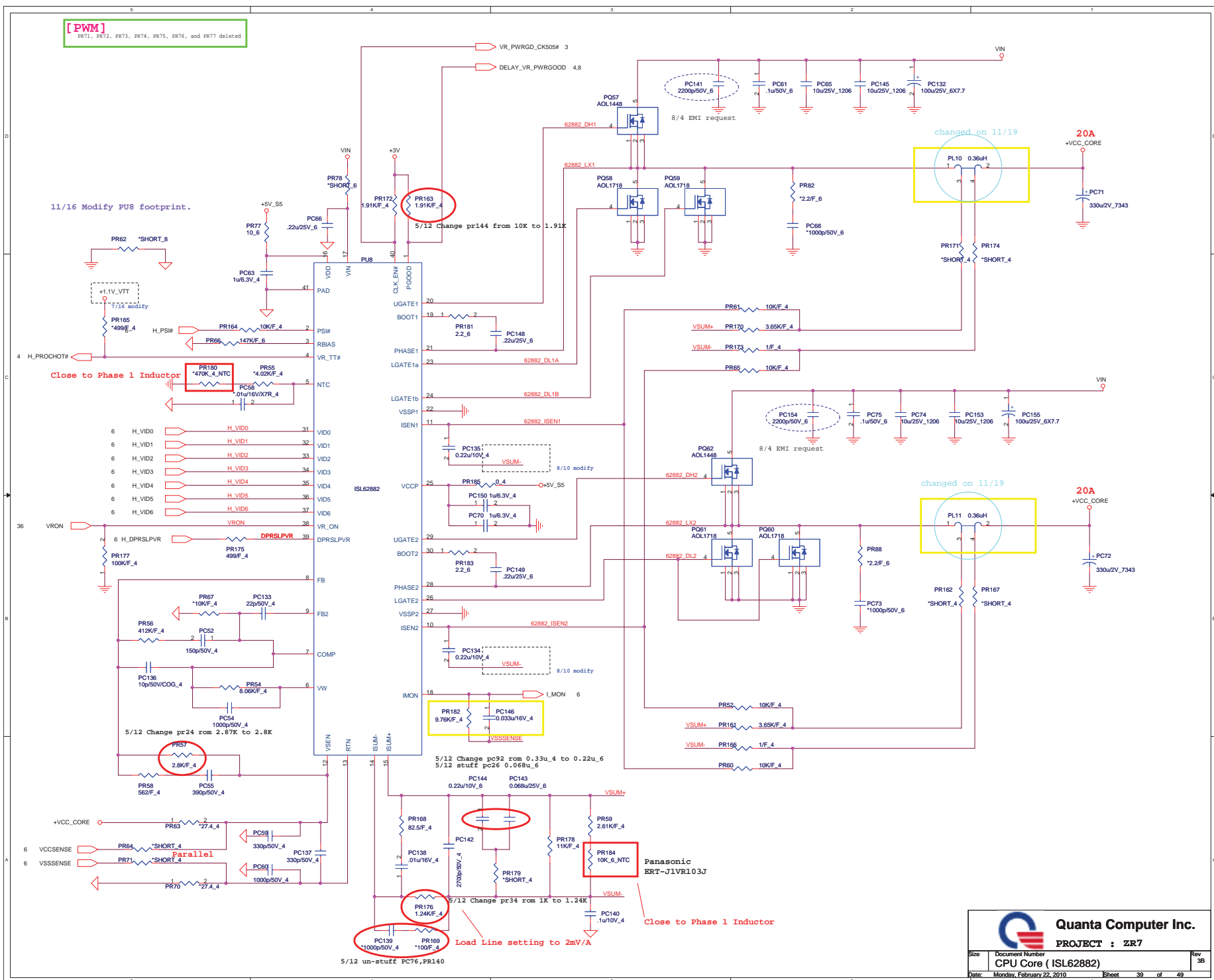
5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K

5/12 Change pr24 rom 2.87K to 2.8K



Load Line setting to 2mV/A

Close to Phase 1 Inductor

changed on 11/19

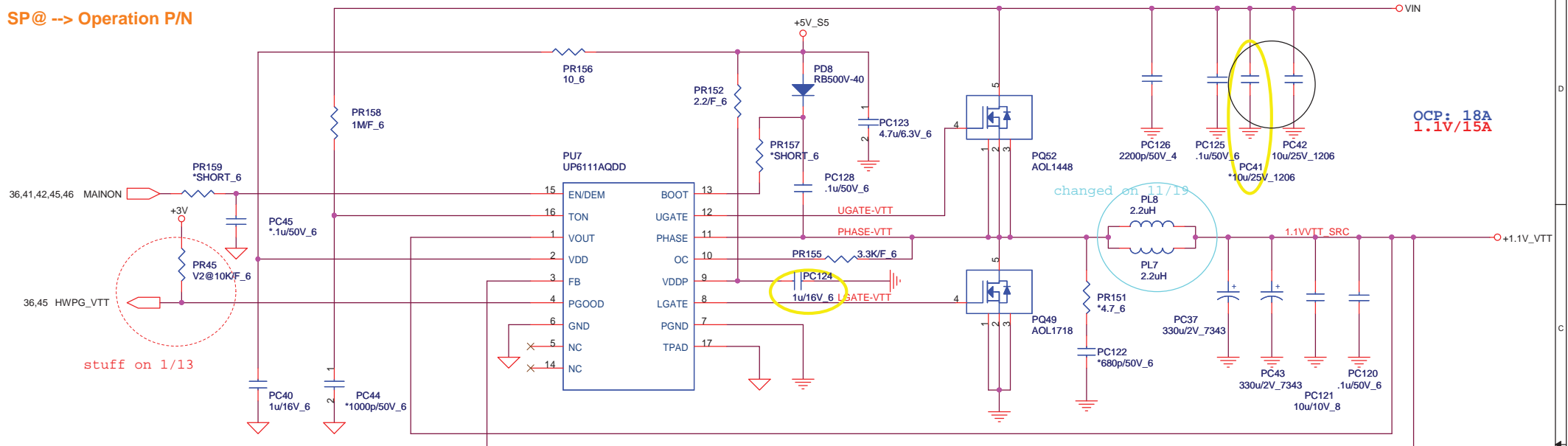
changed on 11/19

**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	CPU Core (ISL62882)	38
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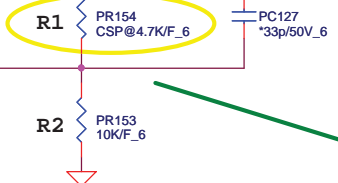
[ PWM ]

SP@ --> Operation P/N



OCP: 18A  
1.1V/15A

$$V_{OUT} = (1 + R1/R2) * 0.75$$

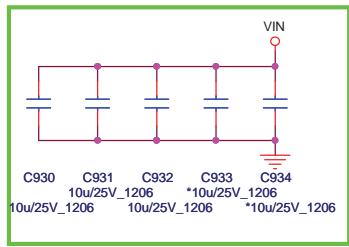


CSP@ --> Operation P/N (ARD&CFD)

**SP@ BOM change notice**  
 Arrandale (1.05V) R1 = 4.02K (CS24023F928)  
 Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$   
 $Frequency = V_{out} / (V_{in} * TON)$   
 $TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$   
 $Frequency = 1 / (0.0036767) = 272K$

AO1718  $R_{dson} = 3 \sim 4.3m\Omega$   
 $L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$   
 $4.3m * 18 = RILIM * 20uA$   
 $RILIM = 3.87K \text{ --- } 3.92K$

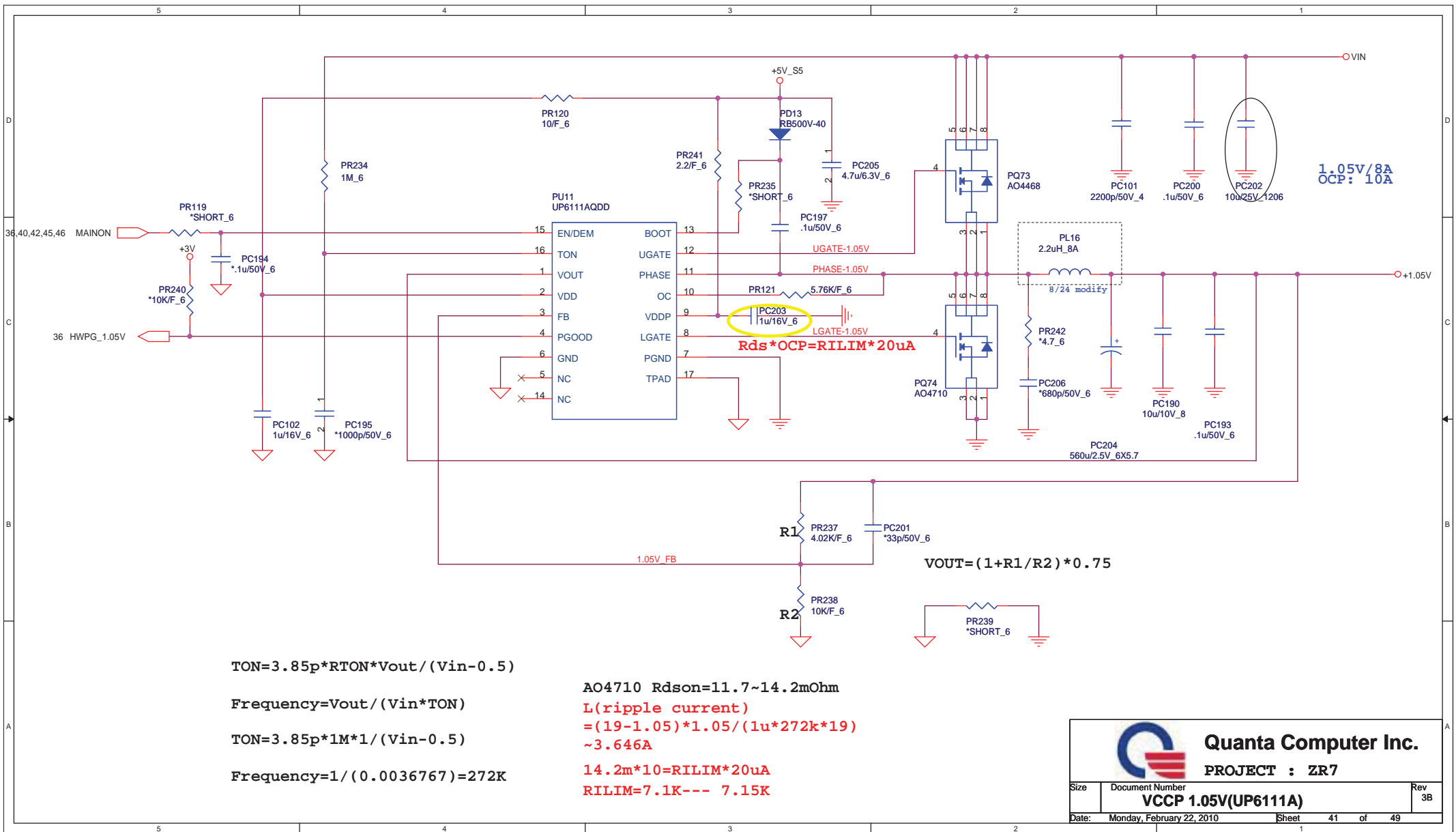


2/11 Add C930-C934 by monitor test.

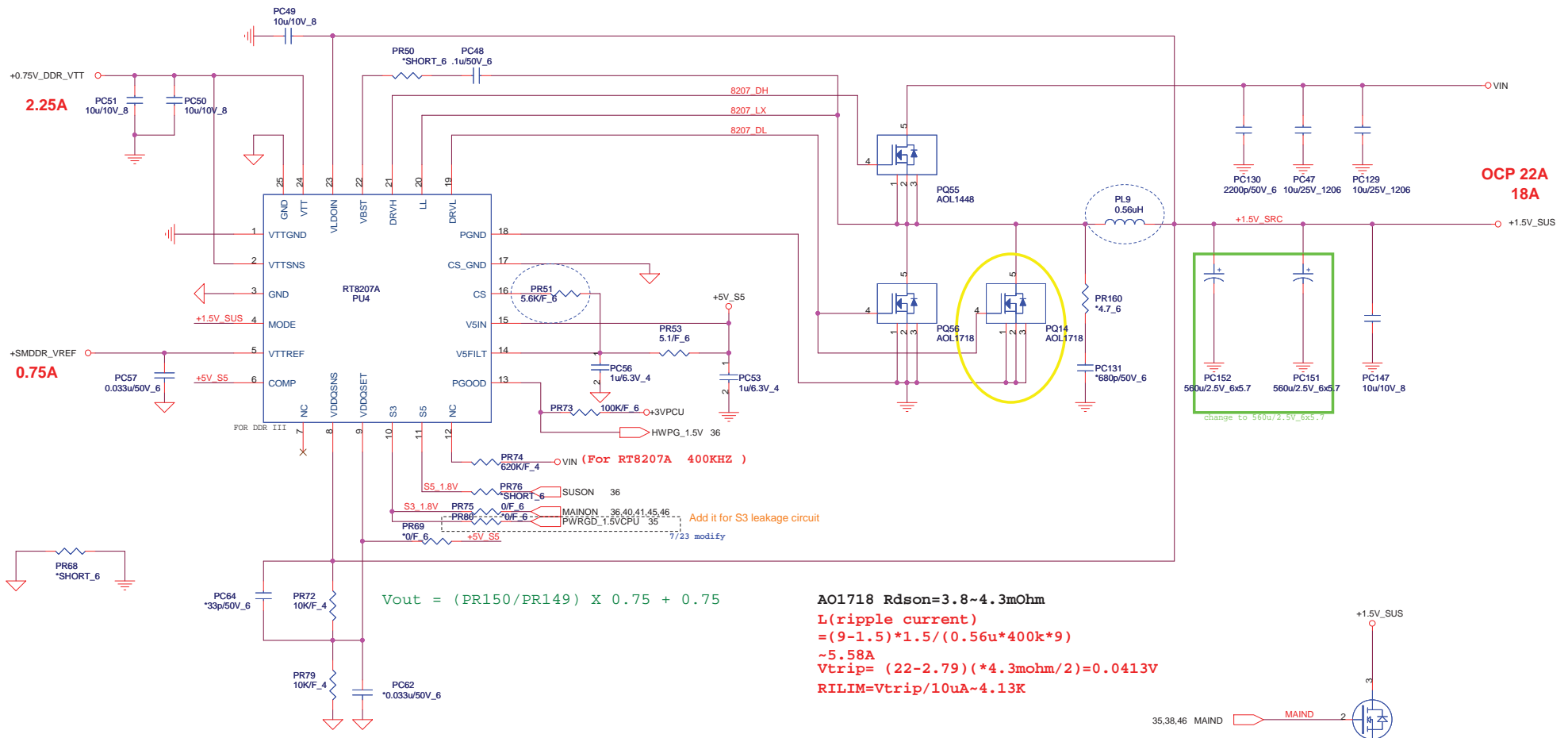
**Quanta Computer Inc.**  
 PROJECT : ZR7

Size	Document Number <b>+VTT (UP6111A)</b>	Rev 3B
Date:	Monday, February 22, 2010	Sheet 40 of 49





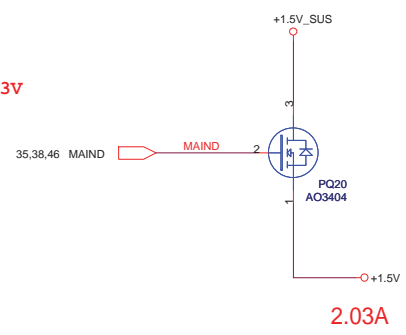
[ PWM ]



$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1718  $R_{dson}=3.8\sim 4.3m\Omega$   
 $I$ (ripple current)  
 $= (9-1.5) \times 1.5 / (0.56\mu \times 400k \times 9)$   
 $\sim 5.58A$   
 $V_{trip} = (22-2.79) \times (4.3m\Omega / 2) = 0.0413V$   
 $RILIM = V_{trip} / 10\mu A \sim 4.13K$

	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	OFF	ON	ON
S4/S5	0	0	OFF	OFF	OFF

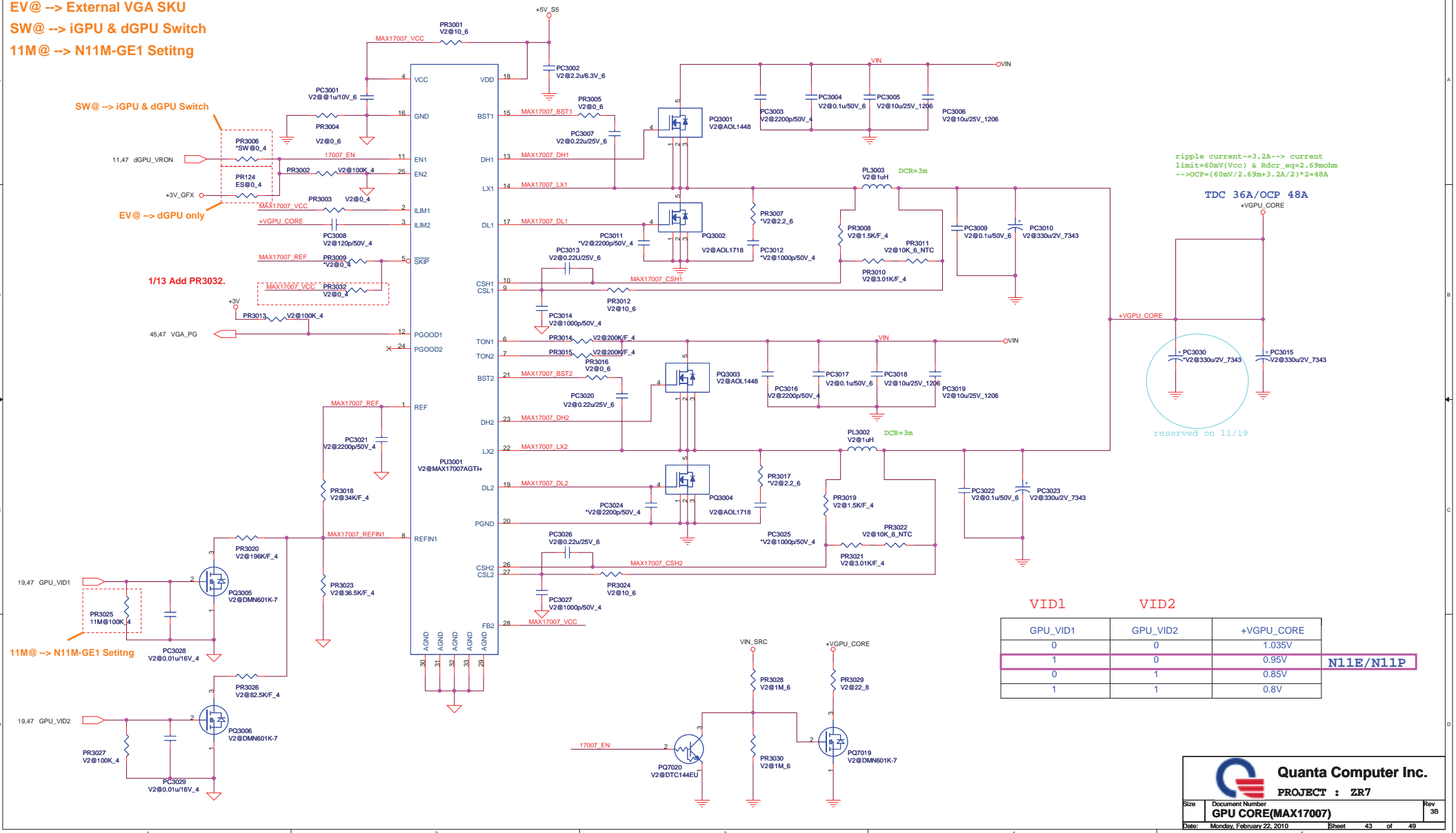


**Quanta Computer Inc.**  
**PROJECT : ZR7**

Size	Document Number	Rev
	DDR III 1.5V(TPS51116)	3B
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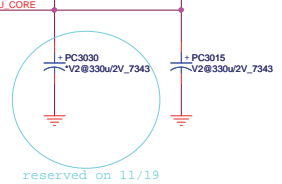
V2@ --> Two Phase dGPU only  
 EV@ --> External VGA SKU  
 SW@ --> iGPU & dGPU Switch  
 11M@ --> N11M-GE1 Seting

11/16 Change VGPU\_CORE to two phase solution.



ripple current=3.2A--> current  
 limit=60mV(Vcc) & RdcR\_eq=2.69mohm  
 --> OCP=(60mV/2.69m+3.2A/2)\*2=48A

TDC 36A/OCF 48A  
 +VGPU\_CORE



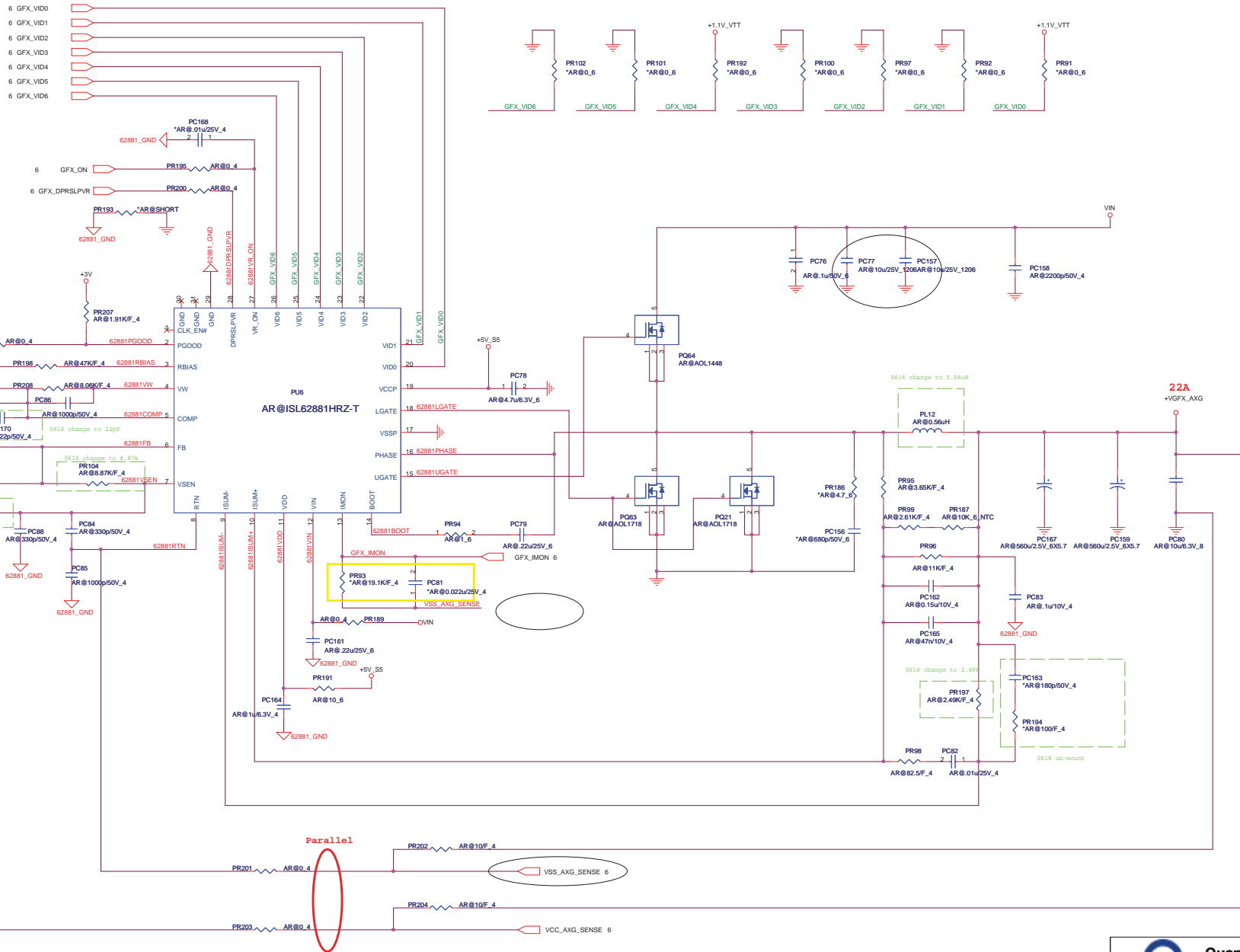
GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.035V
1	0	0.95V
0	1	0.85V
1	1	0.8V

N11E/N11P

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 PROJECT : ZR7

Size	Document Number	Rev
	<b>GPU CORE(MAX17007)</b>	3B
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AR@ --> ARD CPU



11/16 Change PU6 footprint by SMT.

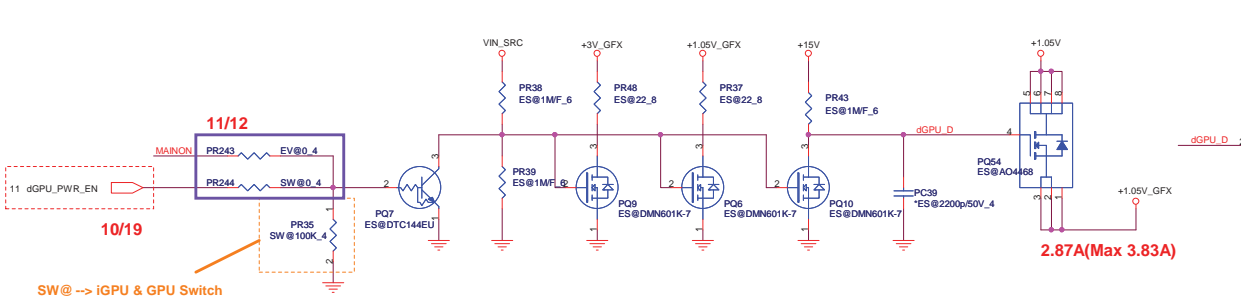
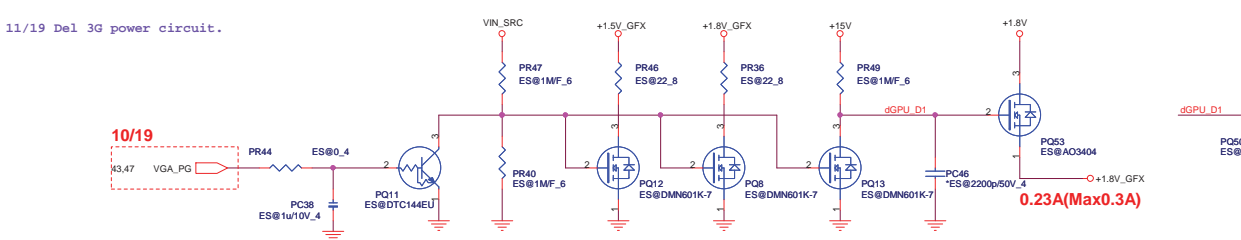
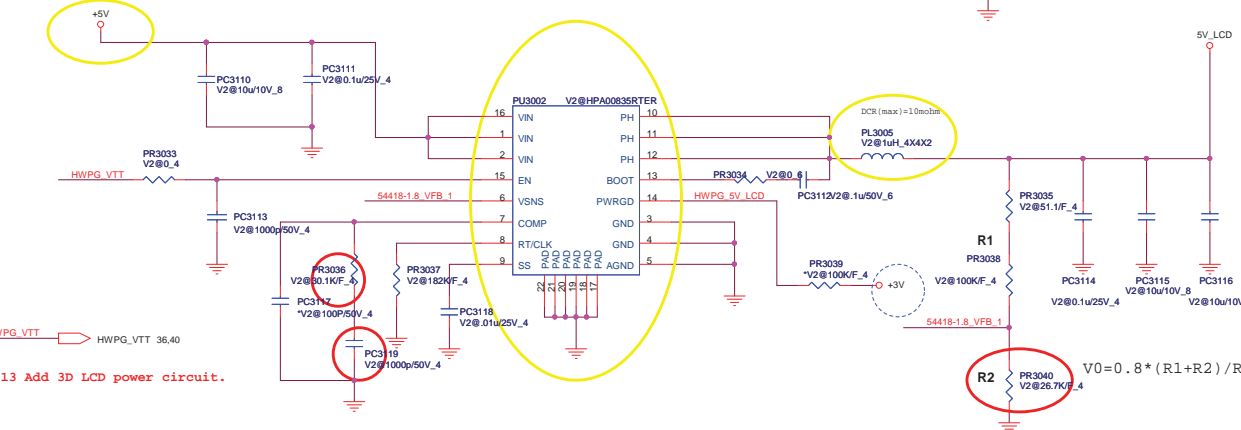
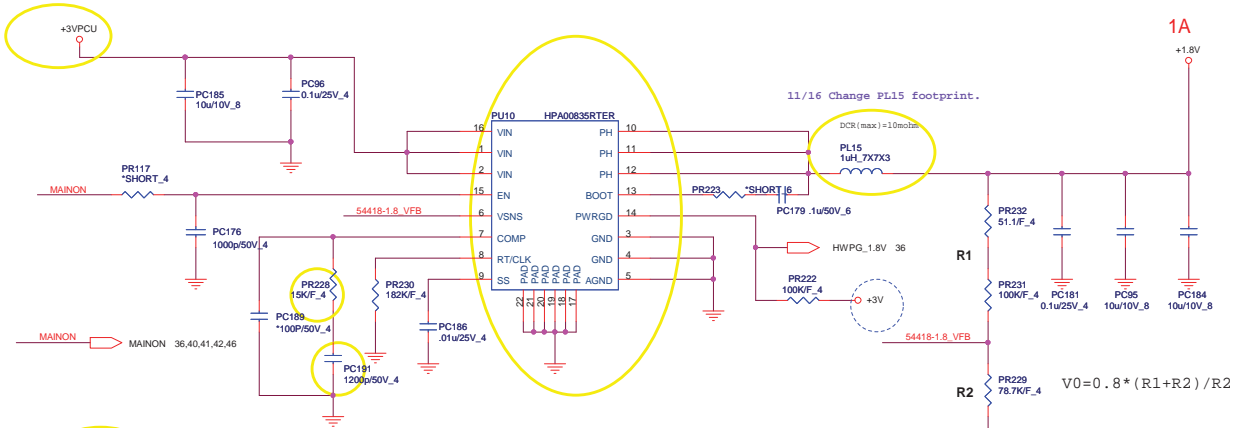
DCR=1.6~1.8mOhm  
 Load Line=7mV/A  
 $1.6m \times 0.6168 = 0.986m$   
 $0.986m / .49K = 396p$   
 $392p \times 2 \times 8.87K = 7.03m$   
 OCP  
 $20u / 2 \times 2.49K = 24.9m$   
 $24.9m / 0.6168 = 40.3m$   
 $40.3m / 1.6m = 25.2A$

Parallel

		<b>PROJECT : ZR7</b>	
		Size: Document Number <b>+VGFX_AXG (ISL62881)</b>	Rev: 38
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1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partner.

ES@ --> External VGA SKU  
 SW@ --> iGPU & GPU Switch



$V0 = 0.8 * (R1+R2) / R2$

$V0 = 0.8 * (R1+R2) / R2$

0.23A(Max0.3A)

4.28A(Max5.72A)

2.87A(Max 3.83A)

1.04A(Max1.38A)

1/13 Add 3D LCD power circuit.

11/19 Del 3G power circuit.

10/19

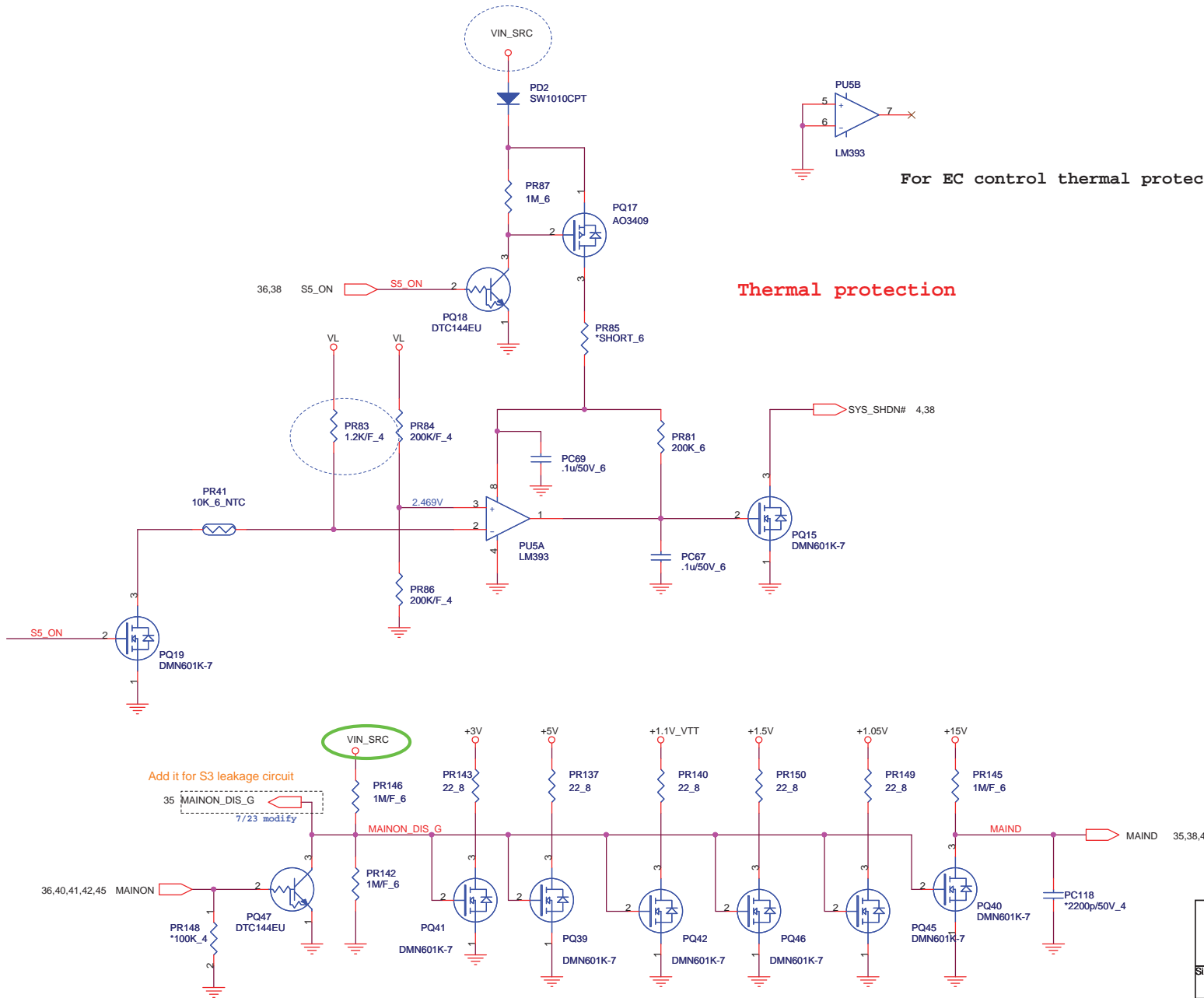
11/12

10/19

SW@ --> iGPU & GPU Switch


**Quanta Computer Inc.**  
 PROJECT : ZR7

Size	Document Number	Rev
	Discharge/1.8V)	3B
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Thermal protection

For EC control thermal protection (output 3.3V)

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		3B
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<b>Thermal Protection</b>		
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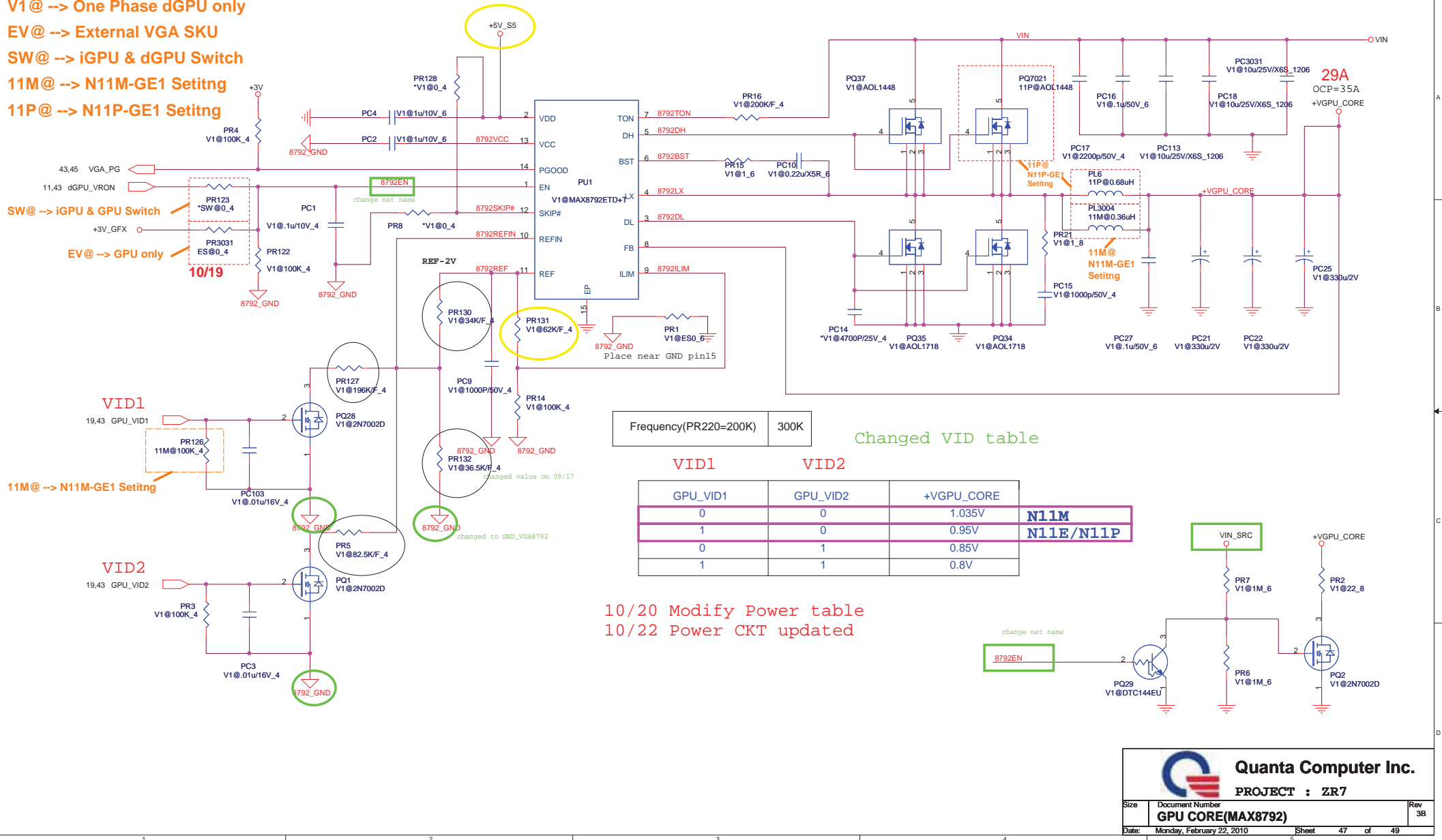
V1@ --> One Phase dGPU only  
 EV@ --> External VGA SKU  
 SW@ --> iGPU & dGPU Switch  
 11M@ --> N11M-GE1 Setting  
 11P@ --> N11P-GE1 Setting

SW@ --> iGPU & GPU Switch  
 EV@ --> GPU only

11M@ --> N11M-GE1 Setting

VID1  
 19,43 GPU\_VID1

VID2  
 19,43 GPU\_VID2



Frequency(PR220=200K) 300K

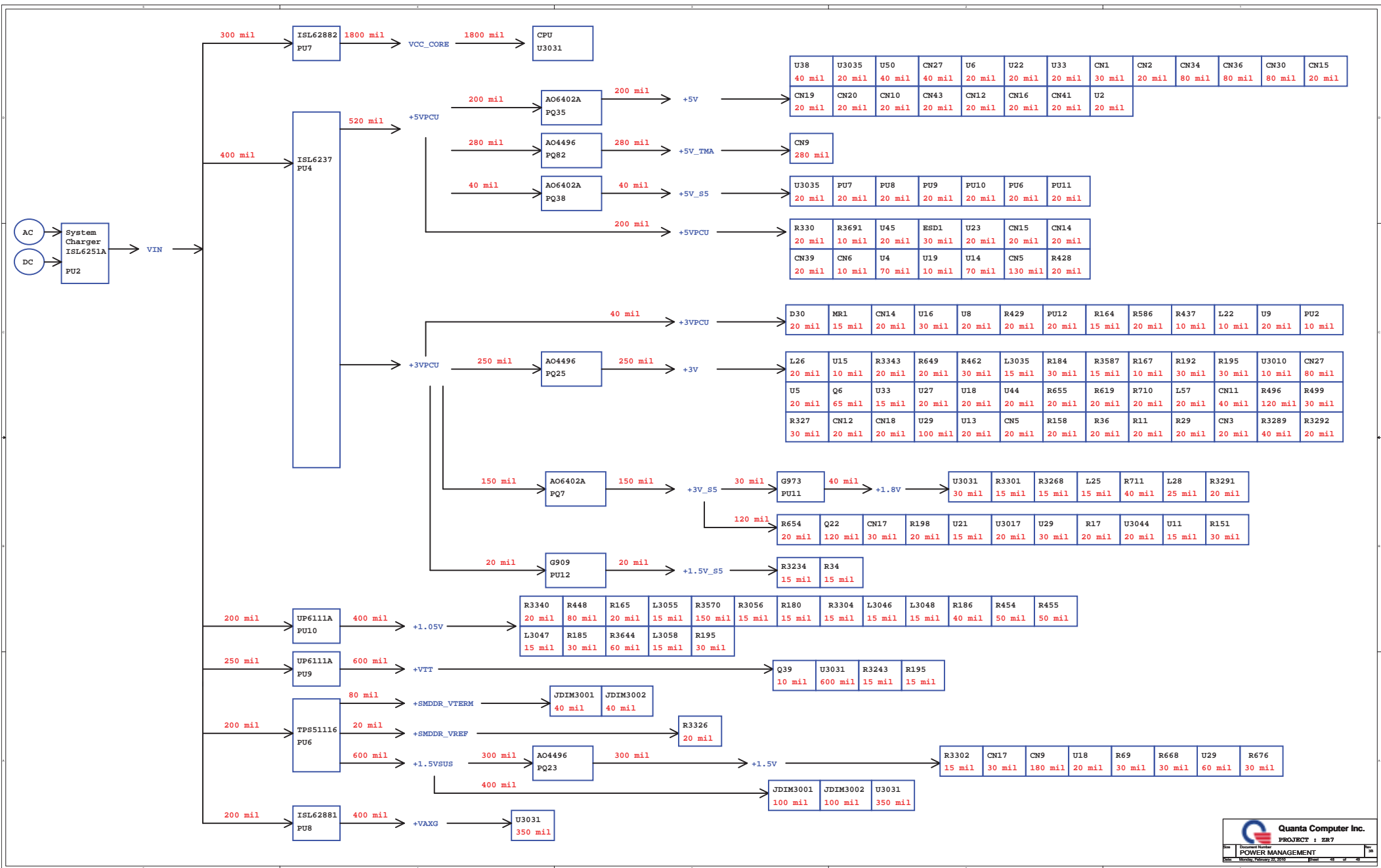
Changed VID table

VID1		VID2			
GPU_VID1	GPU_VID2	+VGPU_CORE			
0	0	1.035V			N11M
1	0	0.95V			N11E/N11P
0	1	0.85V			
1	1	0.8V			

10/20 Modify Power table  
 10/22 Power CKT updated

**Quanta Computer Inc.**  
**PROJECT : ZR7**

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	<b>GPU CORE(MAX8792)</b>	3B
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Model	REV	CHANGE LIST	MODEL	
			FROM	To
ZR7 MB	2A	11/2 Page33 Change CN10 P/N by PDC.	1A	2A
		11/5 Page9 change R338 and R594 to 10K ohm by checklist.	1A	2A
		11/5 Page10 Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.	1A	2A
		11/5 Page11 un-stuff R318 and del C169 and add R698 contact VCCLAN to GND by checklist.	1A	2A
		11/9 Page12 change W/L LED signal to control by EC.	1A	2A
		11/9 Page16 Add EC pin2/112 for W/L LED control by EC.	1A	2A
		11/12 Page35 PR90,PQ22 no stuff.	1A	2A
		11/12 Page45 Add PR243,PR244 for option.	1A	2A
		11/16 Page23 CMS Add LVDS signal to two channel and change CN3 to spin comm.	1A	2A
		11/16 Page43 GPU VCCHE power change to two phase solution.	1A	2A
		11/16 Page47 Add CN12 spin comm for Touch screen by MR.	1A	2A
		11/16 Page44 Change P06 footprint by SMT.	1A	2A
		11/16 Page45 Change PL15 footprint to CHOKR-PCM063T-3R3M-NB4 by SMT.	1A	2A
		11/16 Page39 Change P08 footprint to qfn40-5x5-4-41p-0.75h-smt by SMT.	1A	2A
		11/16 Page37 Change P03 footprint to QFN28-5X5-5-33P-SMT by SMT.	1A	2A
		11/18 Page10 Delete R597, C444,C445 for cancel 3G function.	1A	2A
		11/18 Page10 R368,R393 modify from 47ohm to 56ohm by Realtek.	1A	2A
		11/18 Page10 Change BOARD_ID0-2 to BOARD_ID0-1.	1A	2A
		11/18 Page11 Change GPIO7 to BOARD_ID0 and reserve R439 PD.	1A	2A
		11/18 Page36 Add D23 to connect to dGPU_PWR0K on EV sku.	1A	2A
		11/18 Page9 Change P/N follow ZR7B that use right angle connector.	1A	2A
		11/18 Page27 Reserve C919, CN22 for NV IR signals on B-test.	1A	2A
		11/19 Page1 Change U39 PN to AL00197002 by vendor.	1A	2A
		11/19 Page31 Change CN5 footprint a P/N follow ZR7B.	1A	2A
		11/19 Page27 Add R597 for MI-PI.	1A	2A
		11/19 Page11 Add R442, R440 to dGPU_PWR0K_R and stuff R321 on EV sku.	1A	2A
		11/19 Page23 Modify CN5 pin define.	1A	2A
		11/20 Page43 Add PR124 on EV sku.	1A	2A
		11/20 Page12-14 Change core logic cap .1uF CH41003ZB35 to CH4102K1B03 by SMT.	1A	2A
		11/20 Page45 del 3G power circuit.	1A	2A
		11/20 Page14 del HOLE10,Add HOLE5,HOLE6,HOLE7,HOLE8,HOLE11,HOLE12,HOLE14,HOLE15,HOLE17,HOLE18,HOLE20,HOLE24,HOLE25,HOLE26,HOLE30 P/N	1A	2A
		11/25 Page10 Q26,Q29 change to unstuff, Add R700,R701 0 ohm for S1 leakage	1A	2A
		11/25 Page20 C151 change to CC7343 package	1A	2A
		11/25 Page14 Change HOLE8,HOLE11 footprint to H-C216D142P2, Change HOLE5,HOLE7,HOLE11 footprint to H-TC19V1D122PT, Change HOLE14,HOLE15,HOLE17,HOLE18 footprint to H-TC136D142PT, Change HOLE20,HOLE24,HOLE26 footprint to H-TC136D142PT, Change HOLE8 footprint to O-SMT-1-8	1A	2A
		11/25 Page36 R425 change to dGPU_IDLE5 signal and value to SW SKU, R428 change value to SW SKU, R249,R250 change to unstuff	1A	2A
		11/25 Page28 Add C920,C921,C923,C924 0.1uF for EMI	1A	2A
		11/25 Page33 L31 SWAP for Layout House	1A	2A
		11/25 Page27 Modify LTRST8_7726 net name to PLTRST8	1A	2A
		11/26 Page33 Change L19/L25 footprint, Stuff L25 common choke & unstuff R301,R302 by EMI	1A	2A
		11/26 Page23 Change L2 footprint	1A	2A
		11/26 Page23 Change R598,R599 to FILTER for SMI	1A	2A
		11/26 Page28 Add C925,C926,C927 for EMI	1A	2A
		11/26 Page11 Modify R422 Value to 1V5 SKU	1A	2A
		11/27 Page11 Del R440	1A	2A
		11/27 Page20 C81,C105 change CC0603 package	1A	2A
		11/27 Page16 C84,C109 change CC0603 package	1A	2A
		11/27 Page23 Add CN5 pin45 to GND	1A	2A
		11/27 Page27 Add L46,L47,R702,R703,R704,R705 by EMI	1A	2A
		11/27 Page10 Modify C599,C703 to 27pF	1A	2A
		12/1 Page27 Modify CN12 to 6 pin connector	1A	2A
12/1 Page32 Modify LED3 & Add R706,R707 PD by EC CDD_EJ & POWER_SAVE	1A	2A		
12/1 Page9 Add R708,R709 by SPI ROM	1A	2A		
3A	12/18 Page32 Add R710,R711,Q57 by EC.	2A	3A	
	12/18 Page23 Add R712,R713 by 3D feature.	2A	3A	
	12/18 Page47 Change P16 footprint to choke-mp1136-2r2-smt by SMT.	2A	3A	
	12/29 Page27 Change CN21 footprint to MIPCI-800055F8052GX00p1-52P-smt by SMT.	2A	3A	
	12/29 Page23 Add F1 by safety.	2A	3A	
	12/29 Page24 Change Q16, Q49 P/N & add F2 by HMDI submit and safety; del U15, U16, U18.	2A	3A	
	12/29 Page10 Change CN19 color to black P/N: DPH08PR110 by ACM.	2A	3A	
	1/5 Page33 Change CN17 footprint to USB-UB1110C-RABED-7F-4P-8-V-SMT by PDC.	2A	3A	
	1/7 Page23 Change Q12 of dGPU_select# signal design by leakage issue.	2A	3A	
	1/7 Page9 Change BT1 P/N to DPHD02M8784 by MR issue.	2A	3A	
	1/8 Page27 Change CN12,CN22 spin comm footprint for Touch Screen and IR.	2A	3A	
	1/11 Page21 Add L48 & stuff I2 and un-stuff R28 and R29 by EMI.	2A	3A	
	1/11 Page41 Add C928 by EMI.	2A	3A	
	1/13 Page12_36 Change C111,C182 to 10V 6.JV.	2A	3A	
	1/14 Page23 Change LVDS connector Pin4 define from NC to LCDVCC & add J3 by 3D PWR.	2A	3A	
1/14 Page28 Change C218,C578 to 10V/10V_8 and footprint 0805.	2A	3A		
3B	2/3 Page 16-22 Change U33 Footprint to Fcbga973-nv14a-nlp-ee-a1 by NV.	3A	3B	
	2/3 Page 30 Change R368,R393 to 75ohm.	3A	3B	
2A	Power modify:	1A	2A	
	11/19 Take out JP12, JP9, JP5, JP6, JP7, JP19, JP20, JP8, JP10, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.	1A	2A	
	11/19 Page38 Change PC198 value; change PR14 from 191K to 182K, PR15 from 220K to 200K,PR106 from 100K to 1K,PR105 from 200K to 150K.	1A	2A	
	11/19 Page40 Change P17,P18 from 1.0uH to 2.2uH.	1A	2A	
	11/19 Page39 Change PL10,PL11 from DC-36T0M000 to CV-18V0M204.	1A	2A	
	11/19 Page43 Reserve PC3030.	1A	2A	
	11/23 Page27 PR19 change to 150K, PR20 change to 39K, PC112 change to IU 25V	1A	2A	
	12/29 Page47 Change P17,P18,PL15,PL16 Footprint to CHOKR-PCM063T-3R3M-NB4-SMT by SMT.	2A	3A	
	12/29 Page37 Change PR136 footprint to RC3720-SMT by SMT.	2A	3A	
	1/5 Page37-48 Change Footprint from CHOKR-ETQP4L36WPC-SMT by PDC.	2A	3A	
3A	1/11 Page37 Add PC1100-PC1109 by EMI.	2A	3A	
	1/11 Page47 Change value of PQ7021,PL6,PL1004 by BOM.	2A	3A	
	1/13 Page43 Reserve PR3032 by PWR.	2A	3A	
	1/13 Page43 Reserve circuit of LCDVCC by PWR.	2A	3A	
	2/10 Page37 Reserve ECL-EC5 by EMI.	3A	3B	
3B	2/11 Page38 Del PD3 by power.	3A	3B	
	2/11 Page40 Add C930-C934 by monitor test.	3A	3B	
		3A	3B	