

# Compal Confidential

## KAWE0 M/B Schematics Document

### Intel Penryn Processor with Cantiga + DDRII + ICH9M

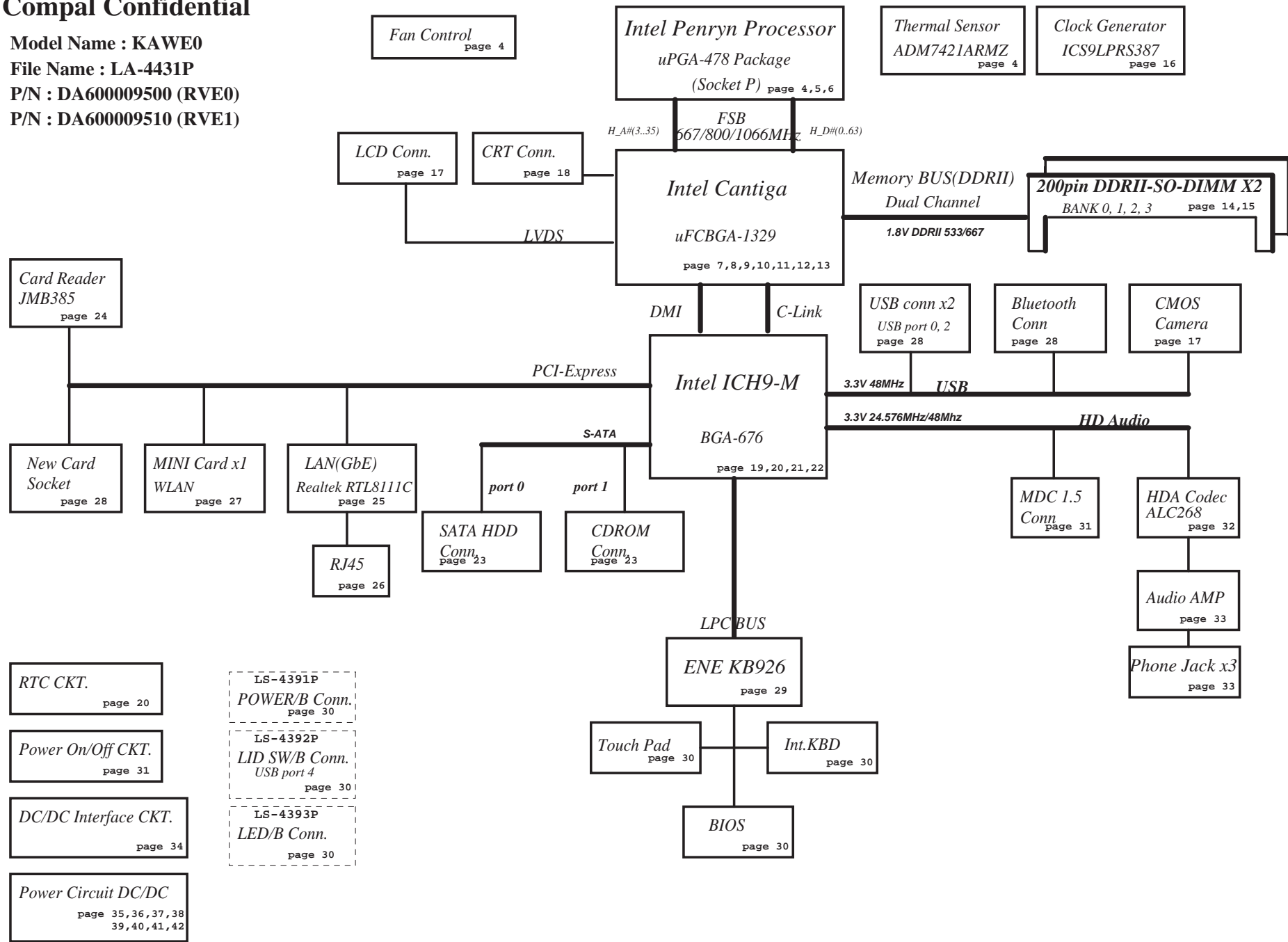
2008-07-28

REV:1.0

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**Model Name : KAWE0**  
**File Name : LA-4431P**  
**P/N : DA600009500 (RVE0)**  
**P/N : DA600009510 (RVE1)**



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

## EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

## ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V




## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

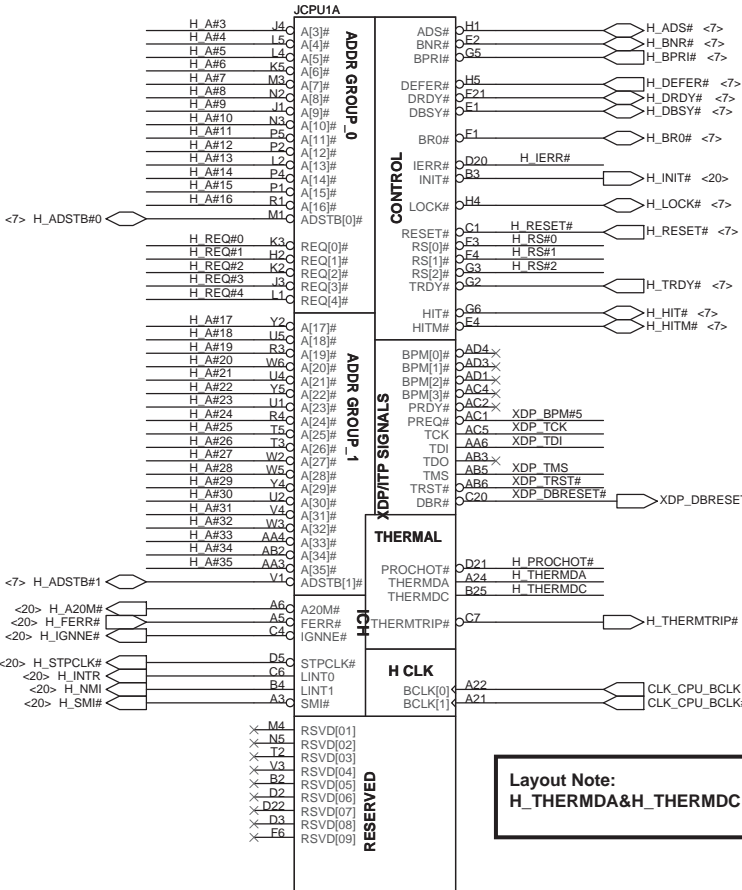
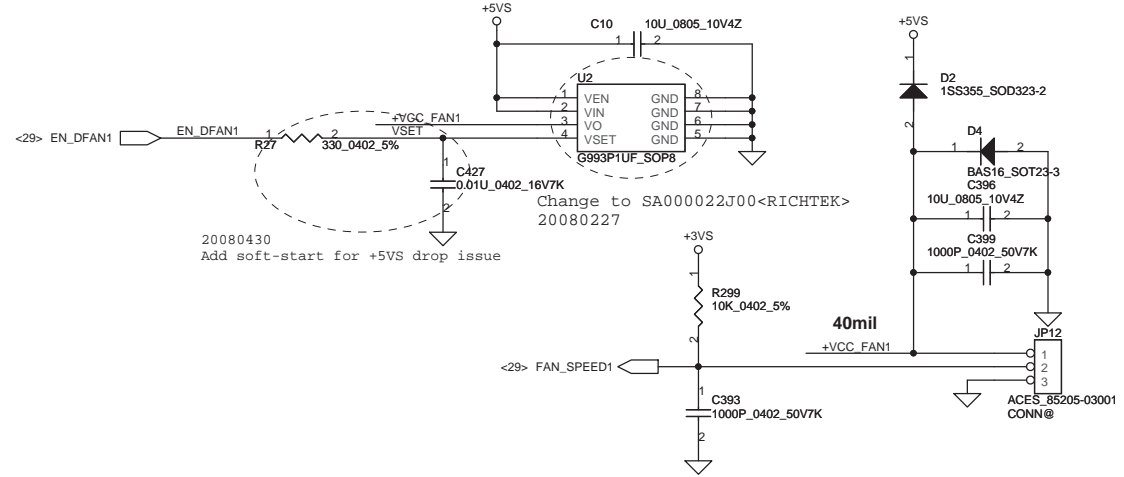
## BTO Option Table

BTO Item	BOM Structure
8111C	8111C@
8102E	8102E@

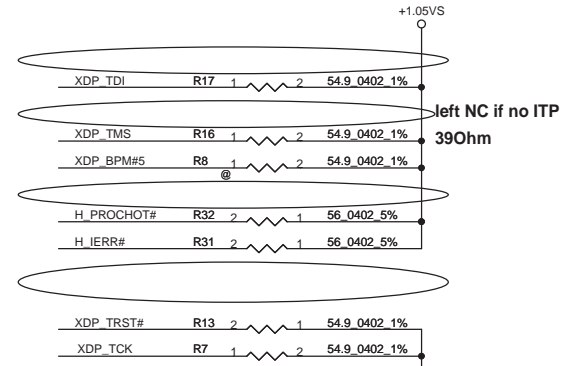
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<7> H\_A#[3..35]  H\_A#[3..35]  
 <7> H\_REQ#[0..4]  H\_REQ#[0..4]  
 <7> H\_RS#[0..2]  H\_RS#[0..2]

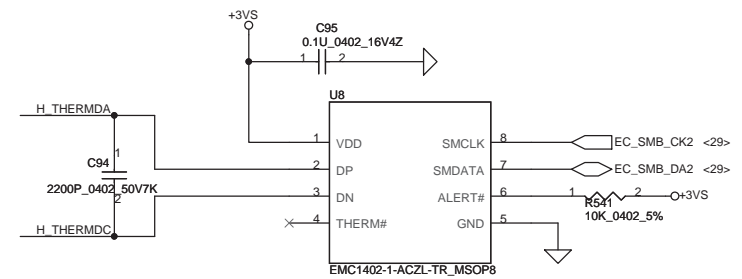
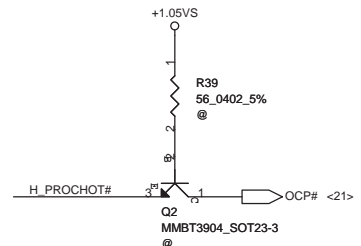
### FAN1 Conn



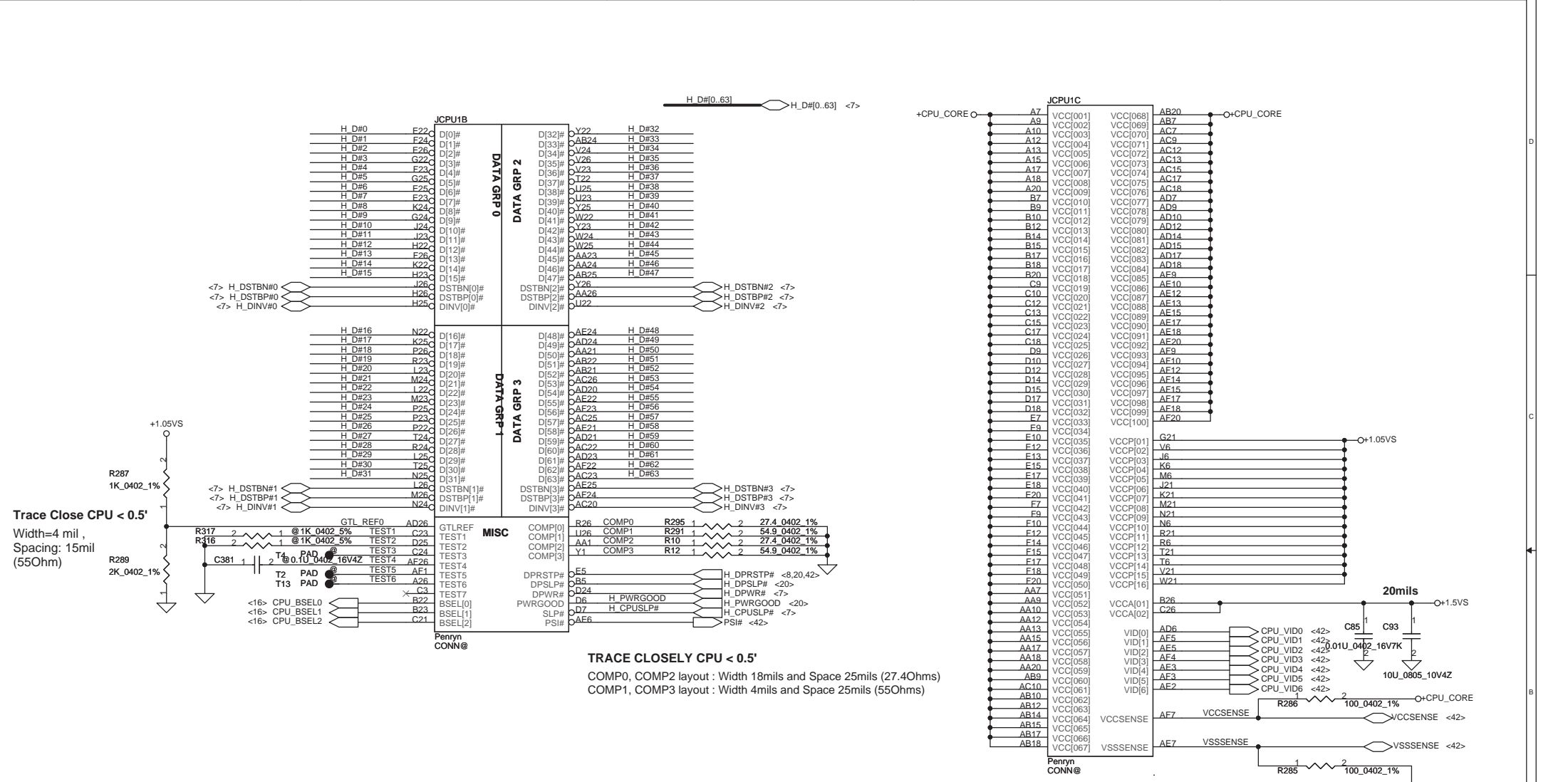
**Layout Note:**  
 H\_THERMDA&H\_THERMDC Trace / Space = 10 / 10 mil



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



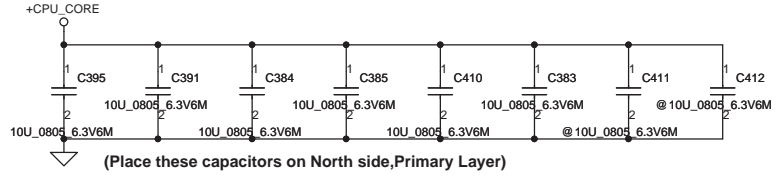
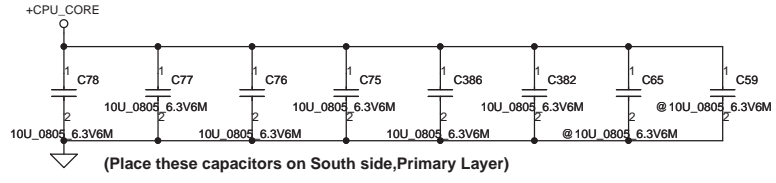
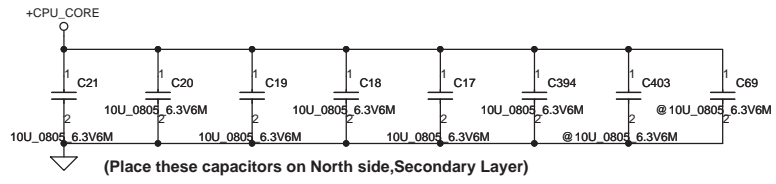
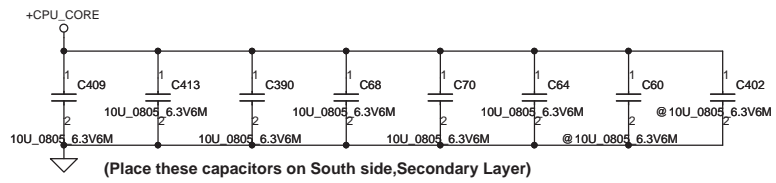
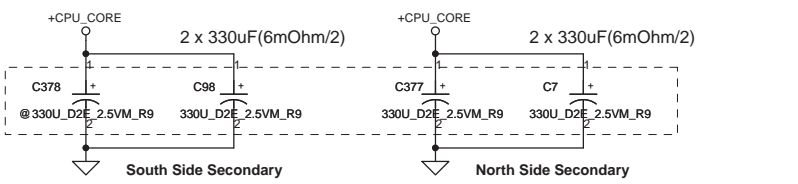
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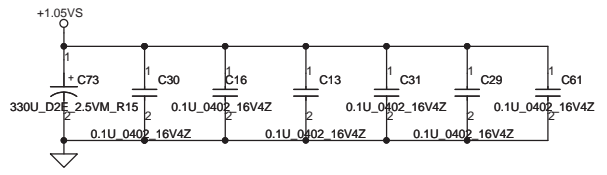
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JCPU1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AE2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
F3	VSS[035]	VSS[116]
F6	VSS[036]	VSS[117]
F8	VSS[037]	VSS[118]
F11	VSS[038]	VSS[119]
F14	VSS[039]	VSS[120]
F16	VSS[040]	VSS[121]
F19	VSS[041]	VSS[122]
F21	VSS[042]	VSS[123]
F24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

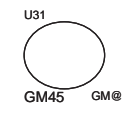
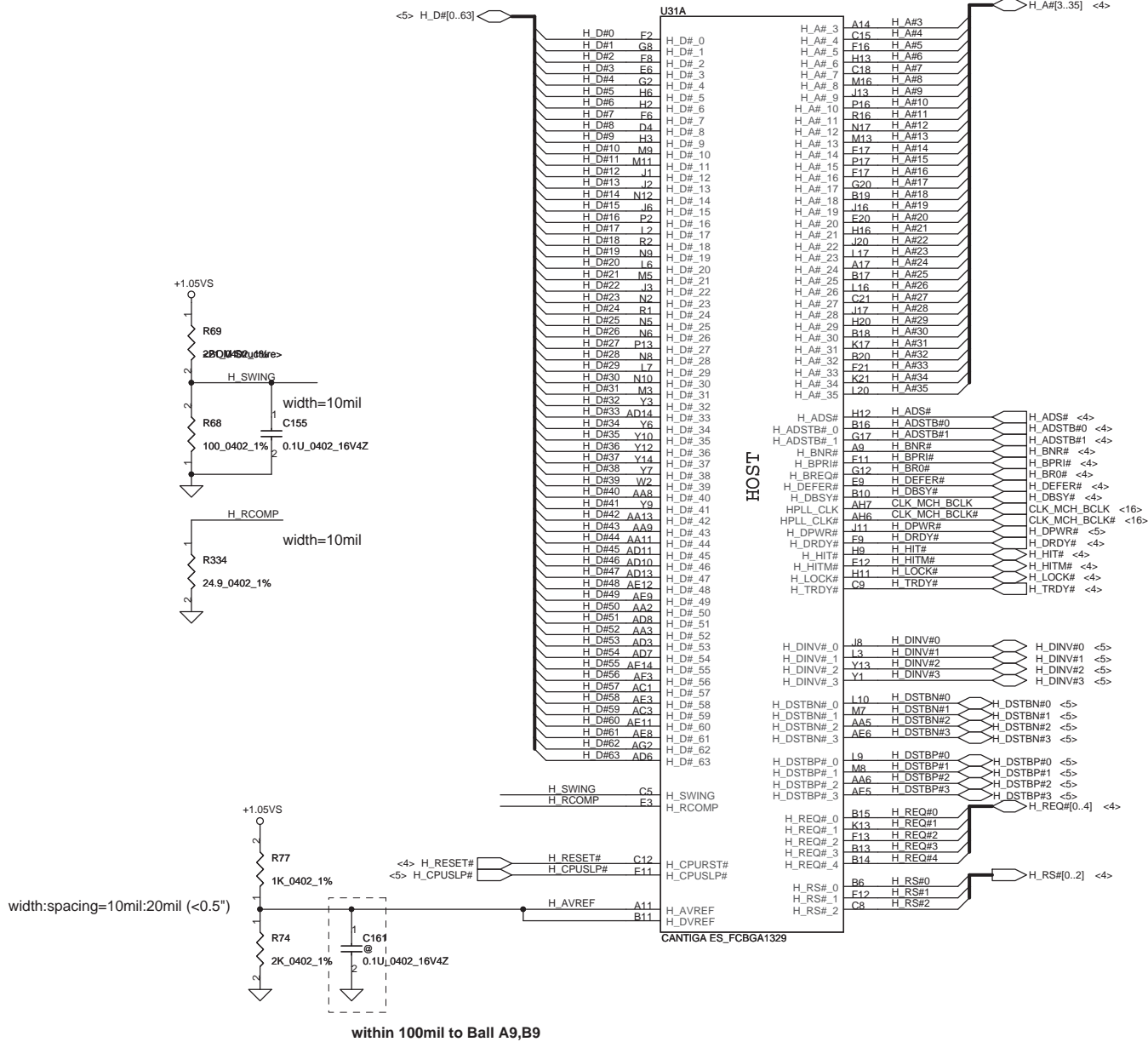
Penryn  
CONN@



+CPU-CORE Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



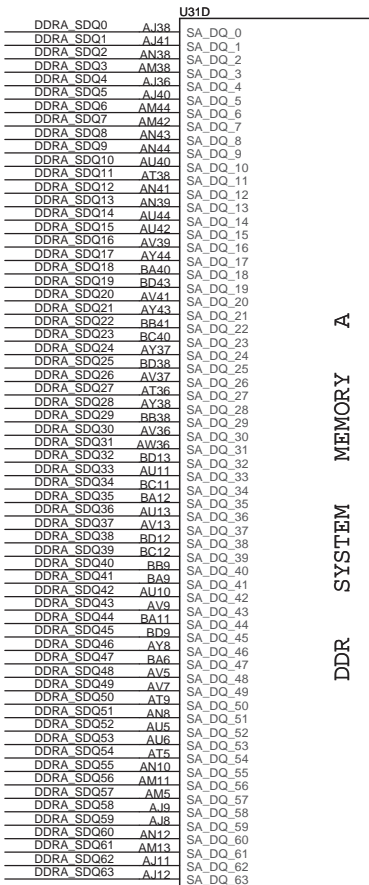
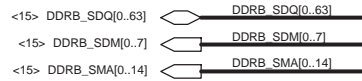
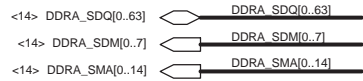
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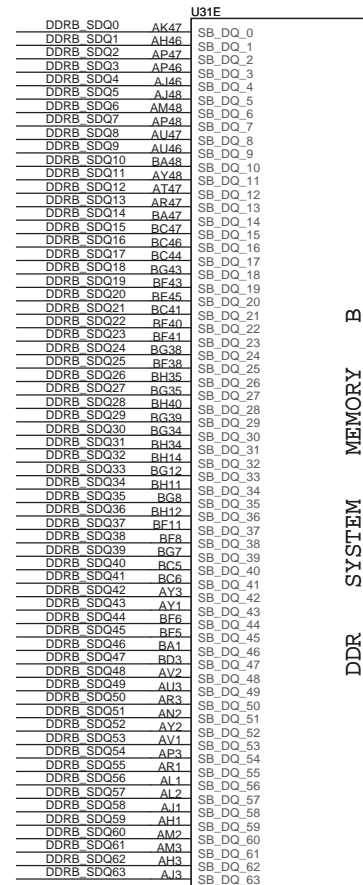




DDR SYSTEM MEMORY A

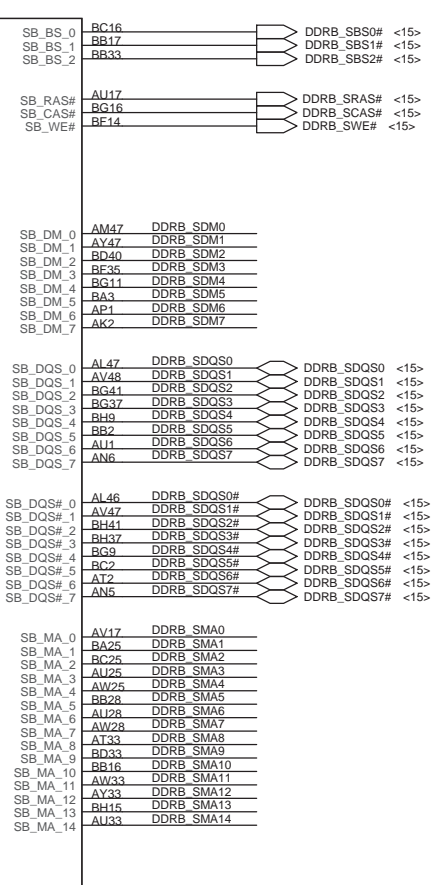
DDR SYSTEM MEMORY B

CANTIGA ES\_FCBGA1329



DDR SYSTEM MEMORY B

CANTIGA ES\_FCBGA1329

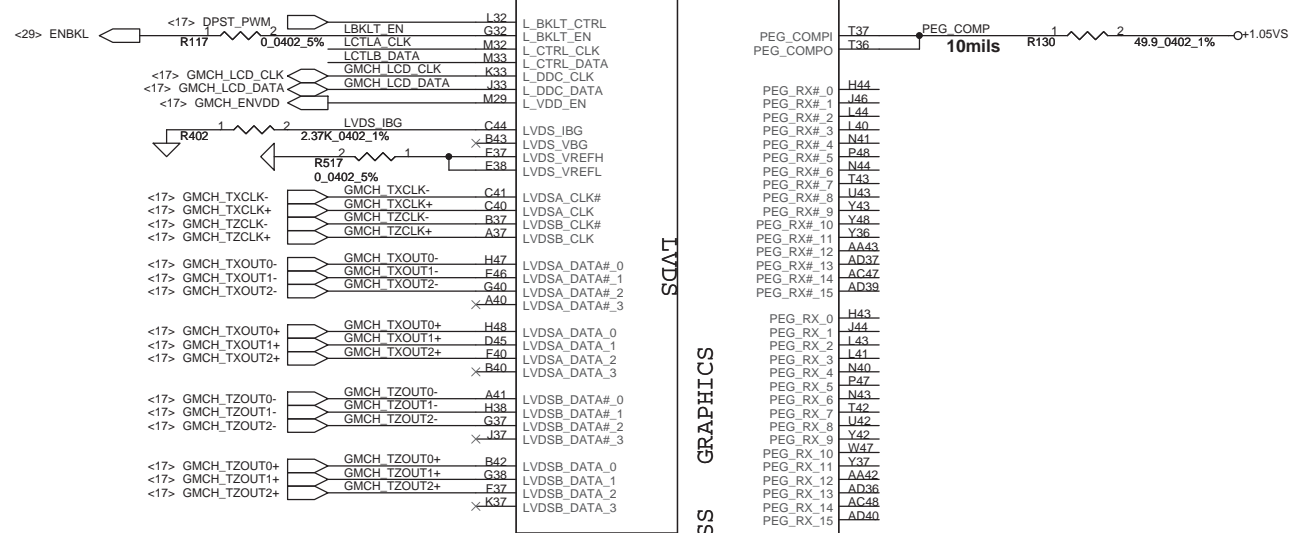


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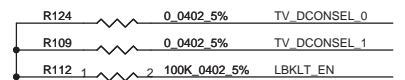
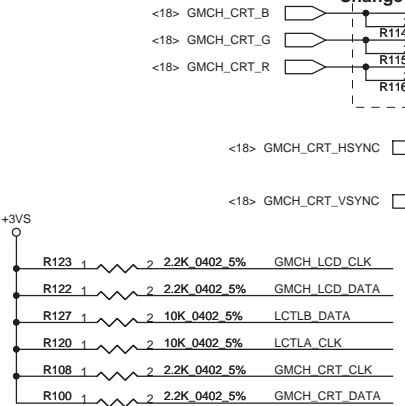
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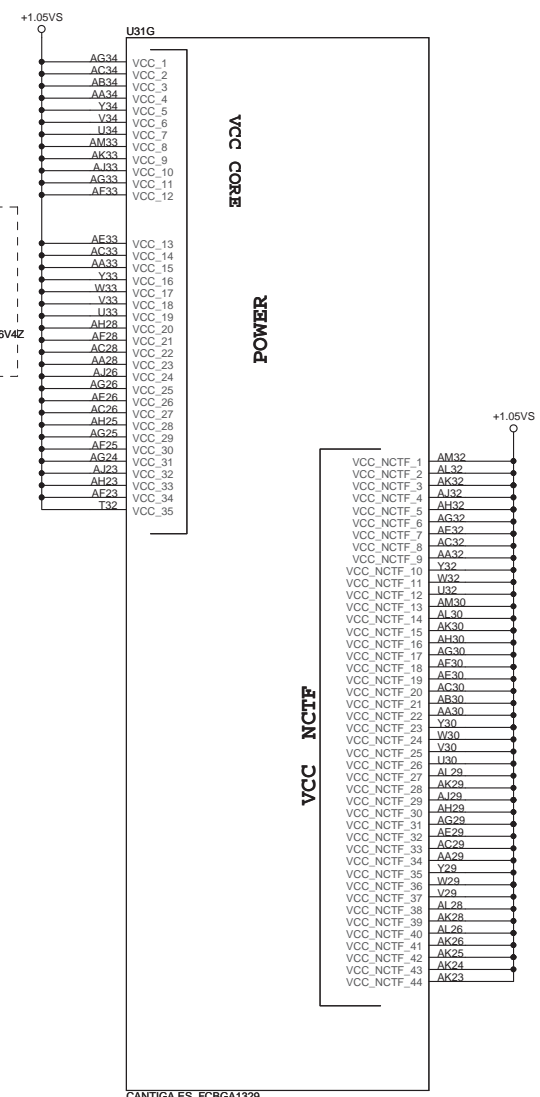
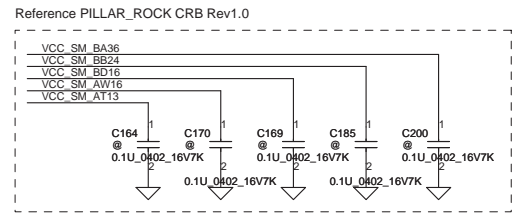
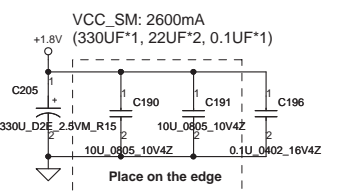
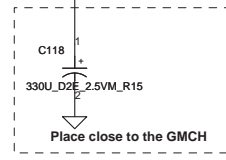
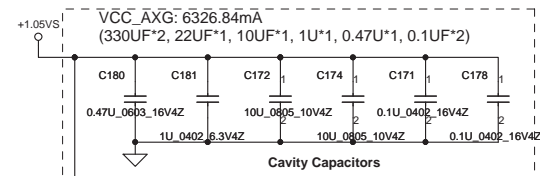
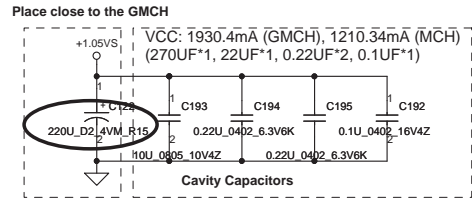
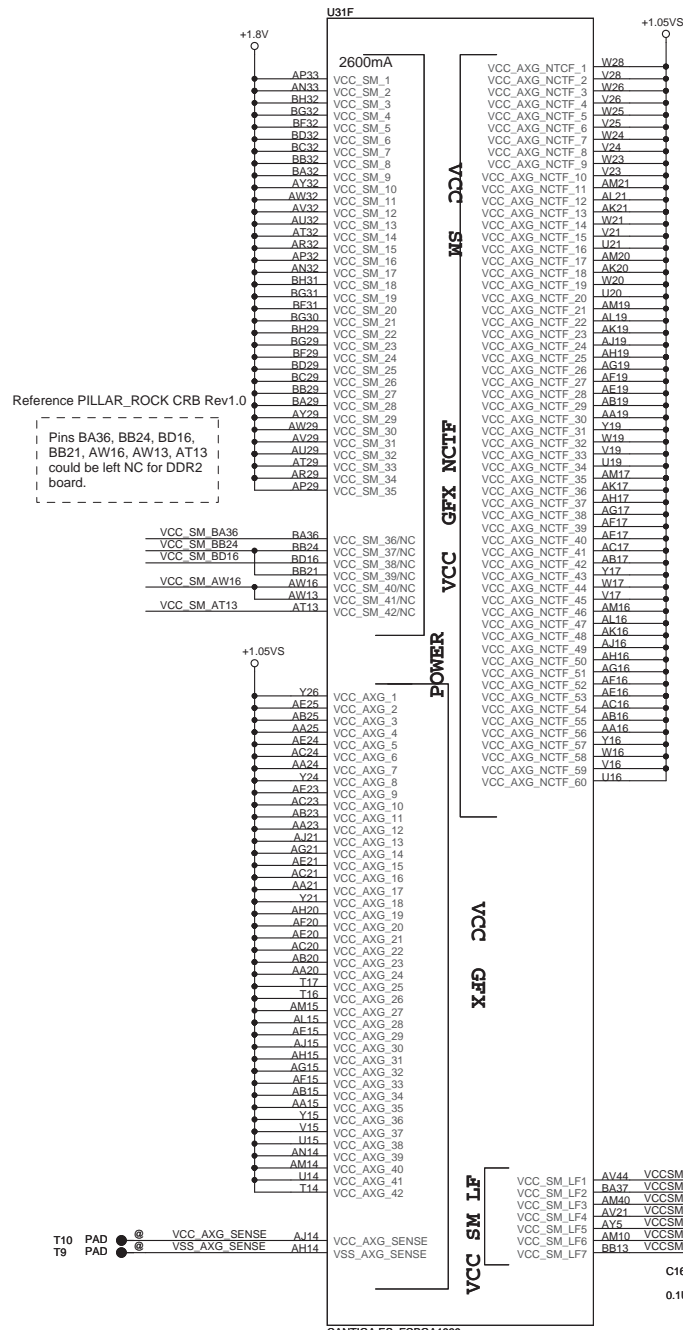


Change to 00hm when use PM chip



CANTIGA ES\_FCBGA1329

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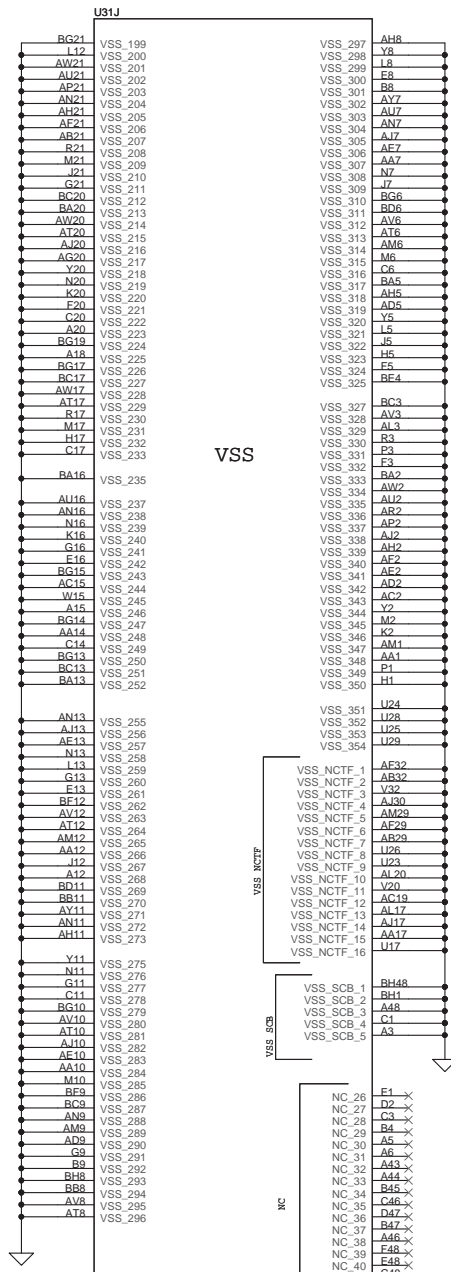
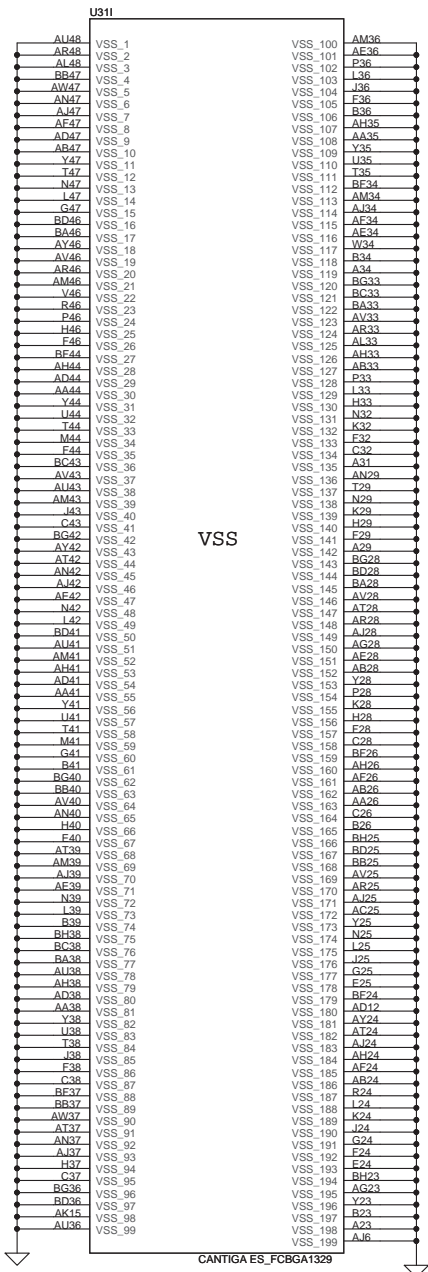
T10 PAD @ VCC\_AGX\_SENSE AH14  
T9 PAD @ VSS\_AGX\_SENSE AH14

CANTIGA\_ES\_FCBGA1329

CANTIGA\_ES\_FCBGA1329

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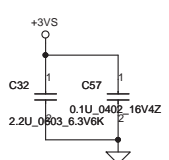
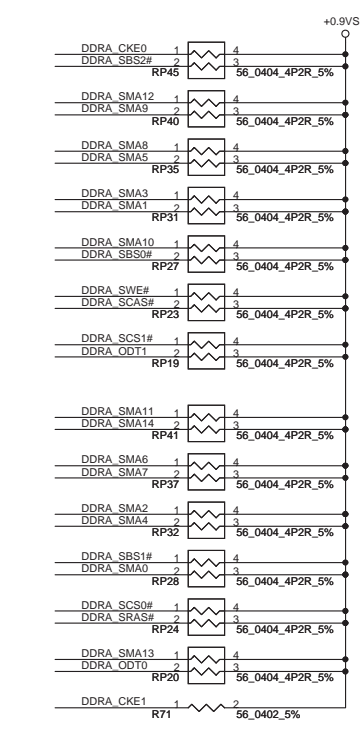
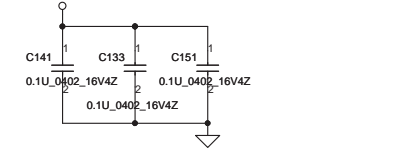
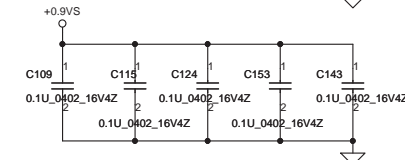
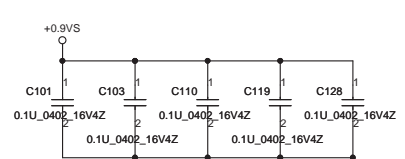
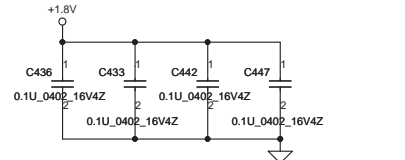
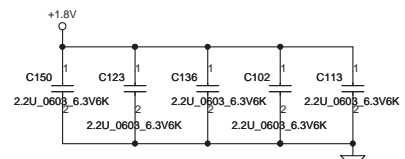
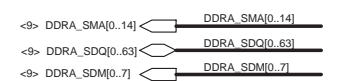
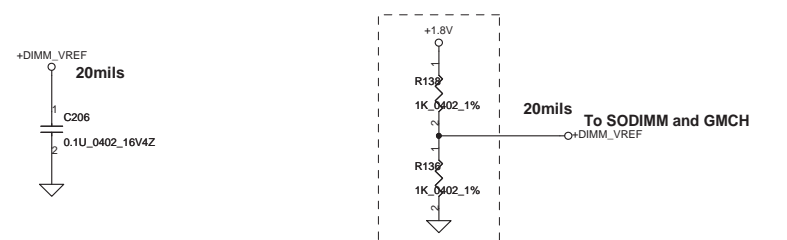
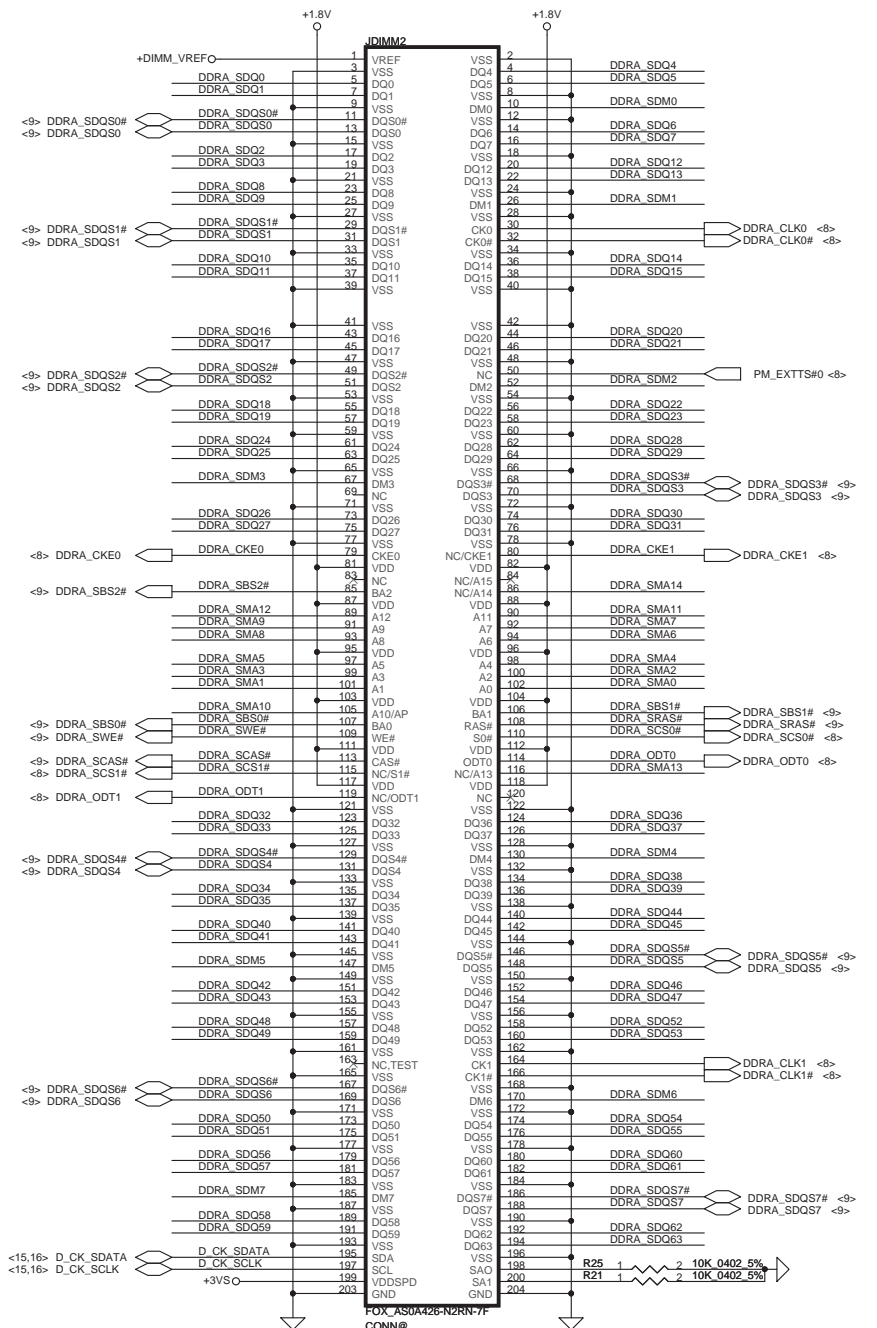


VSS

CANTIGA ES. FCBG1329

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**DIMM0 REV H:5.2mm (BOT)**

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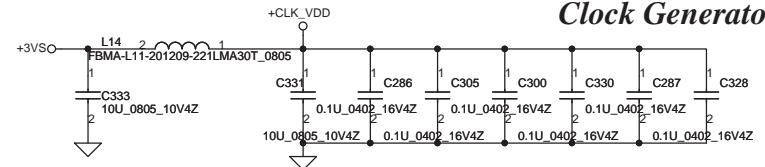
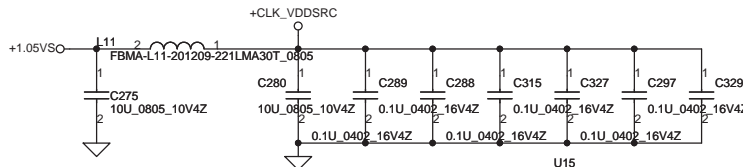
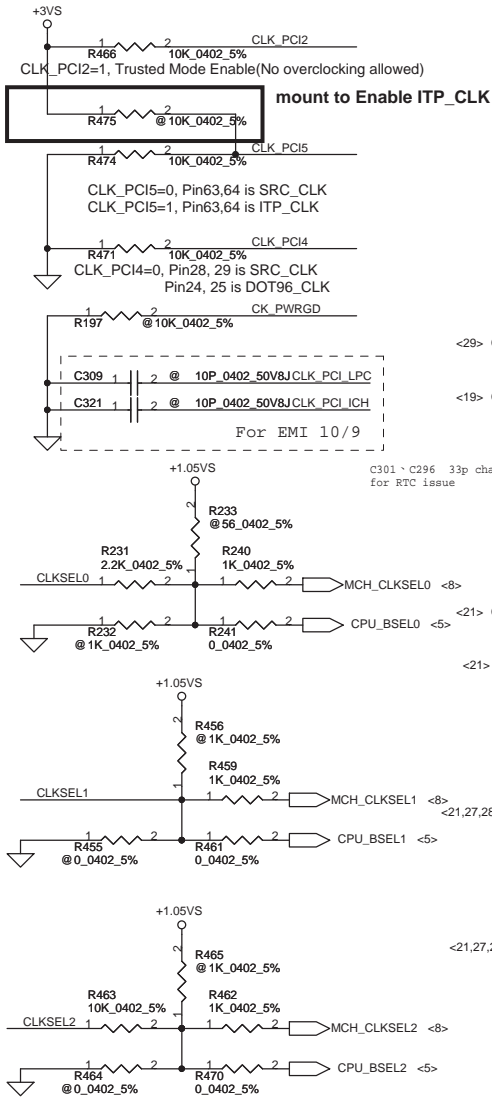


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

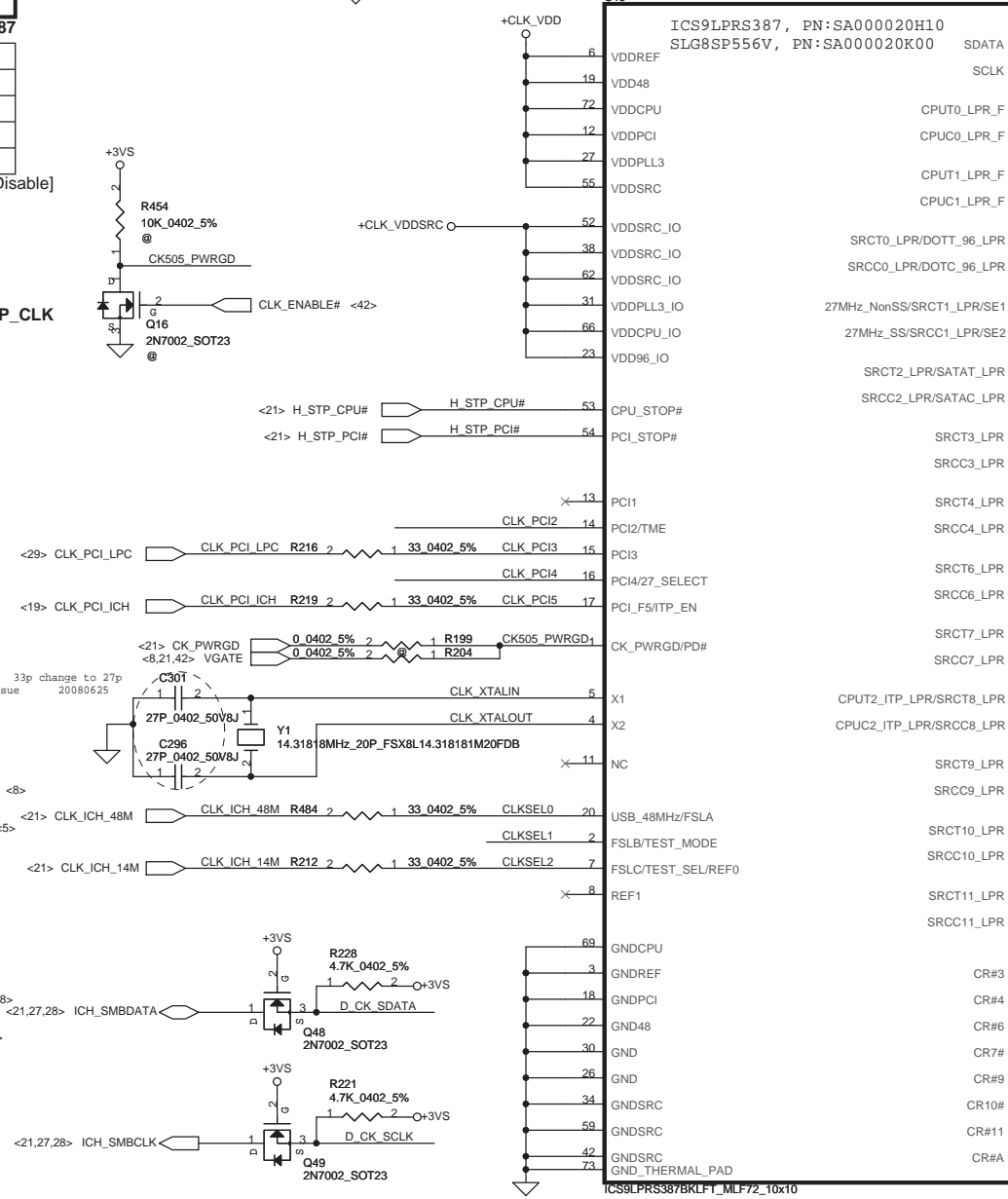
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



### Clock Generator



VGA: disable this pair by BIOS

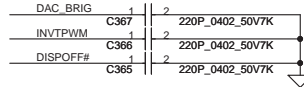
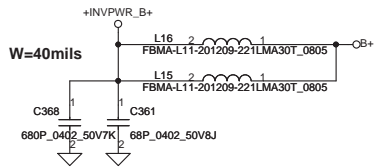
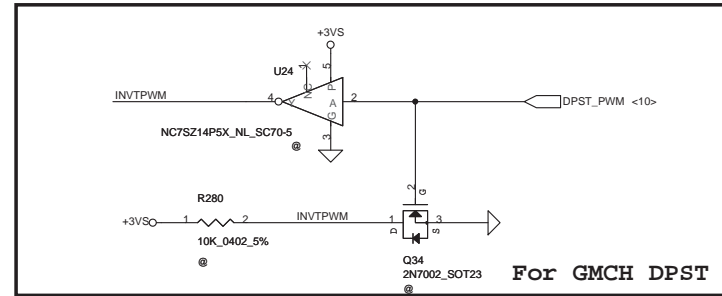
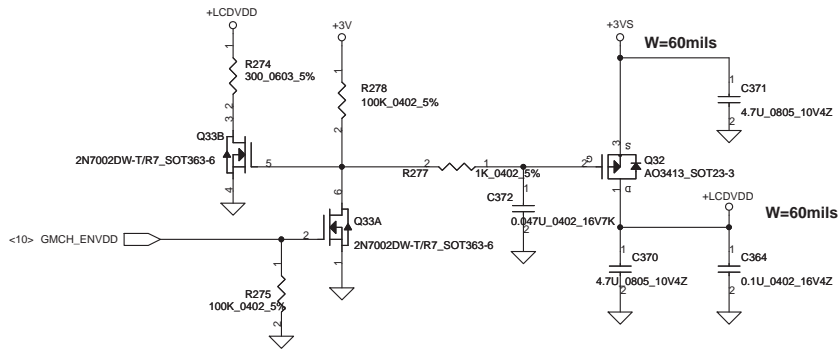
VGA: disable this pair by BIOS

UMA: disable this pair by BIOS

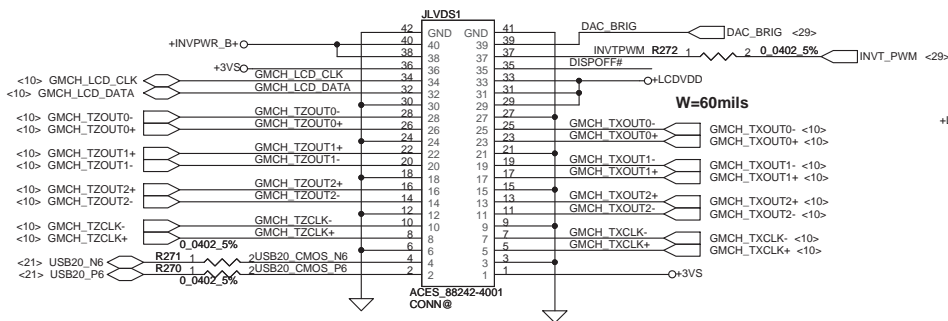
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### LCD POWER CIRCUIT

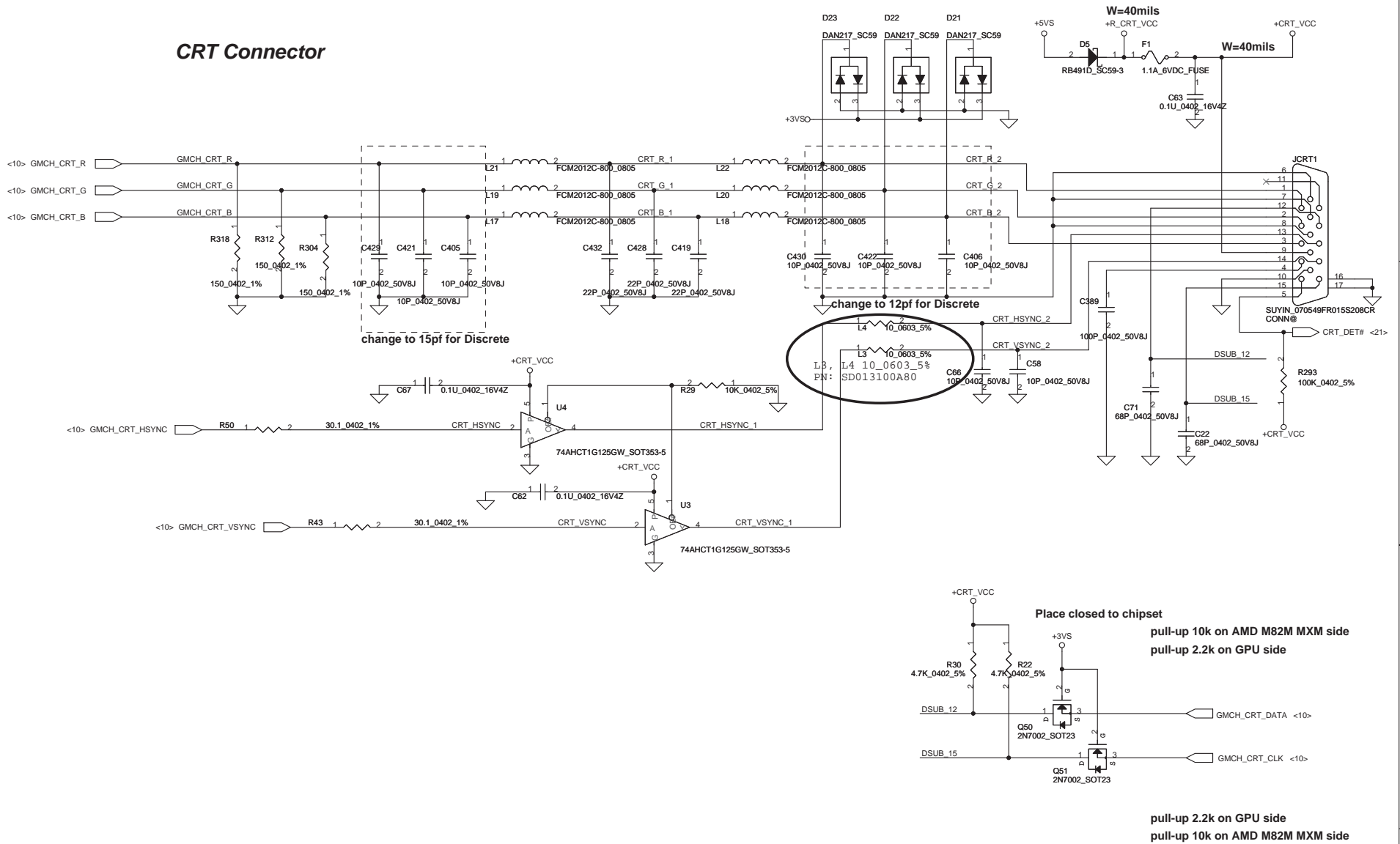


### LCD/PANEL BD. Conn.

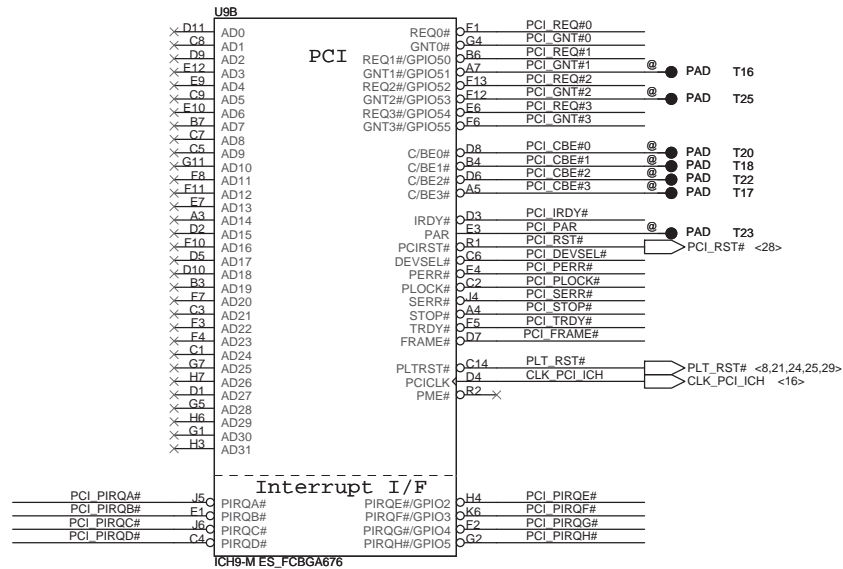
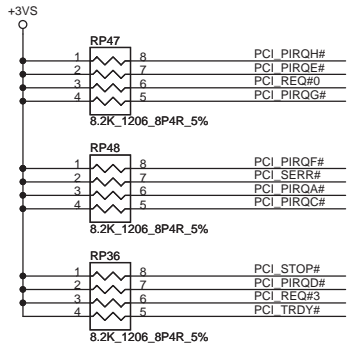
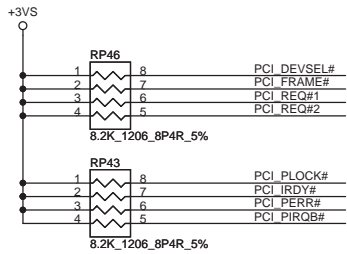


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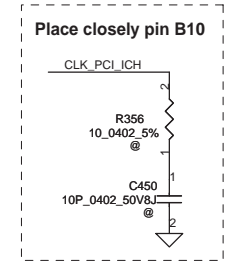
# CRT Connector



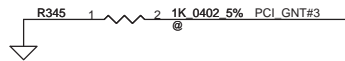
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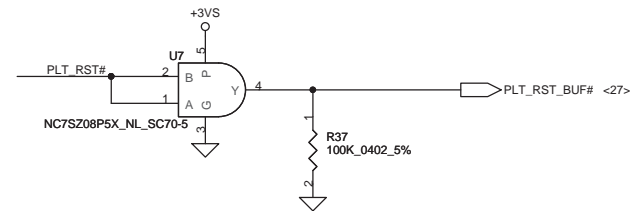
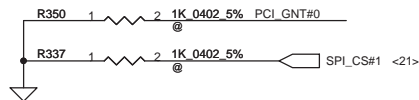
**DMI for ESI-compatible operation**  
**PCI\_GNT#1** Low= DMI for ESI-compatible operation  
 High= Default\* (Internal pull-up)



**A16 Swap Override Strap**  
**PCI\_GNT#3** Low= A16 swap override Enable  
 High= Default\*



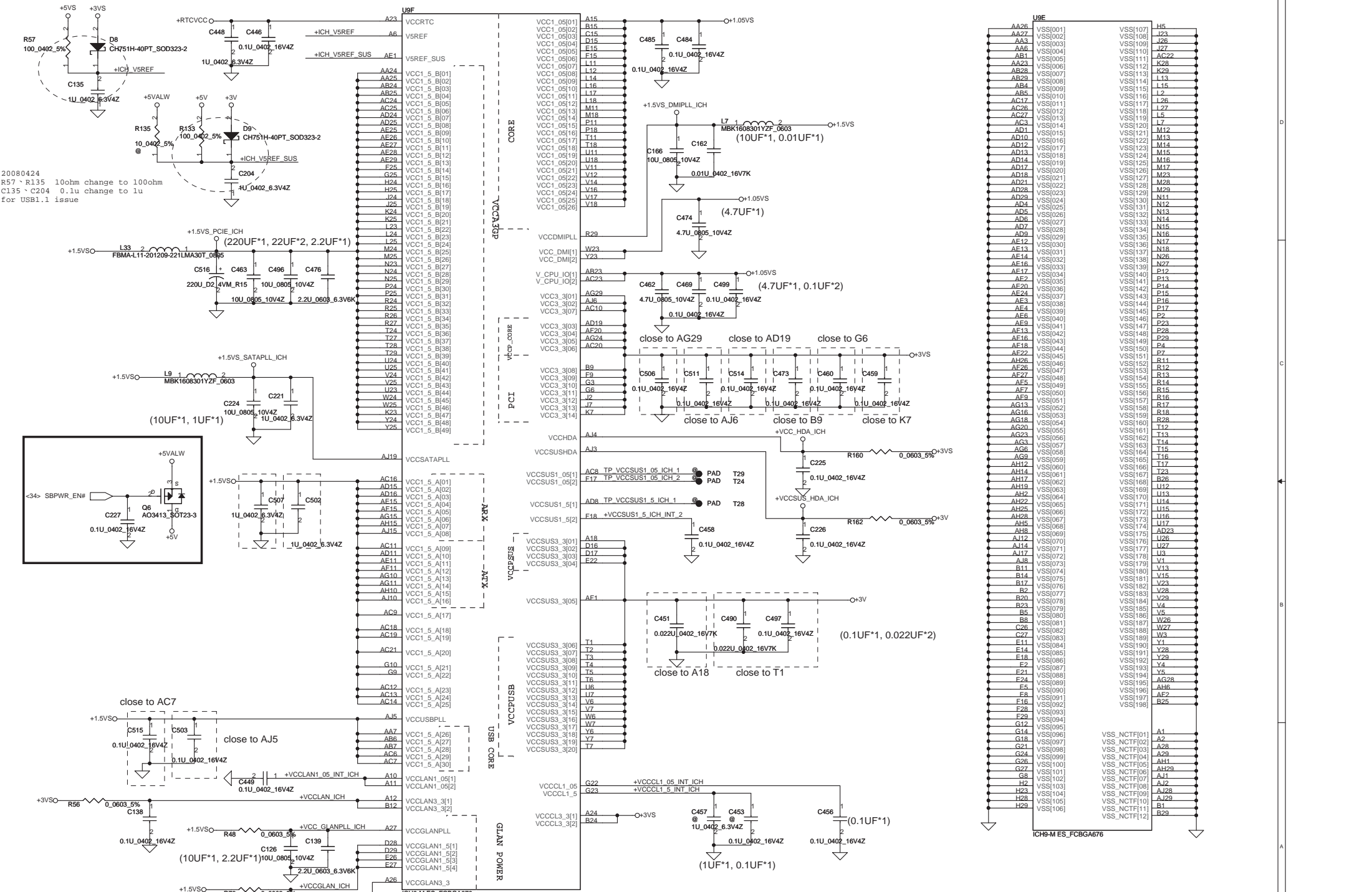
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



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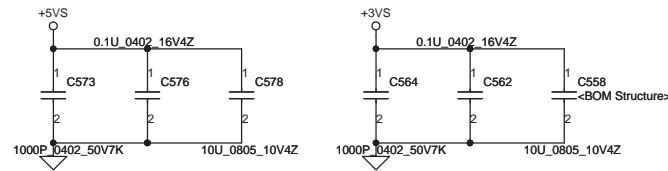


20080424  
 R57 ~ R135 100ohm change to 100ohm  
 C135 ~ C204 0.1u change to 1u  
 for USB1.1 issue

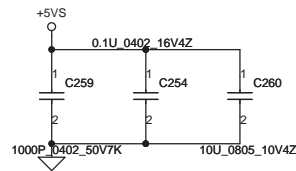
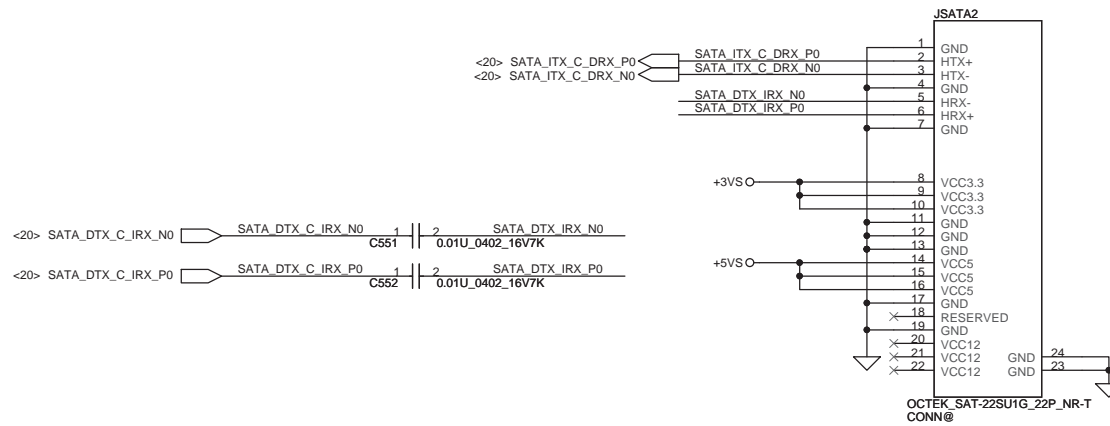
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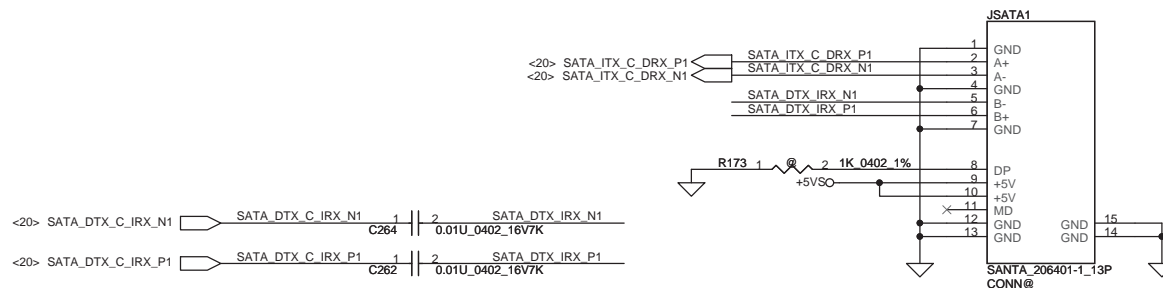
Compal Electronics, Inc.		Schematics, MB A4431	
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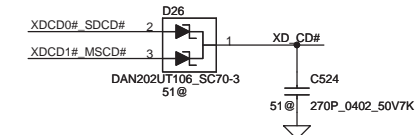
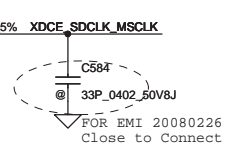
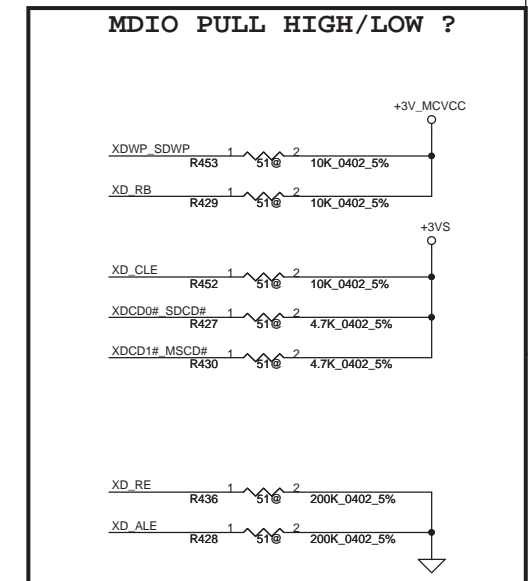
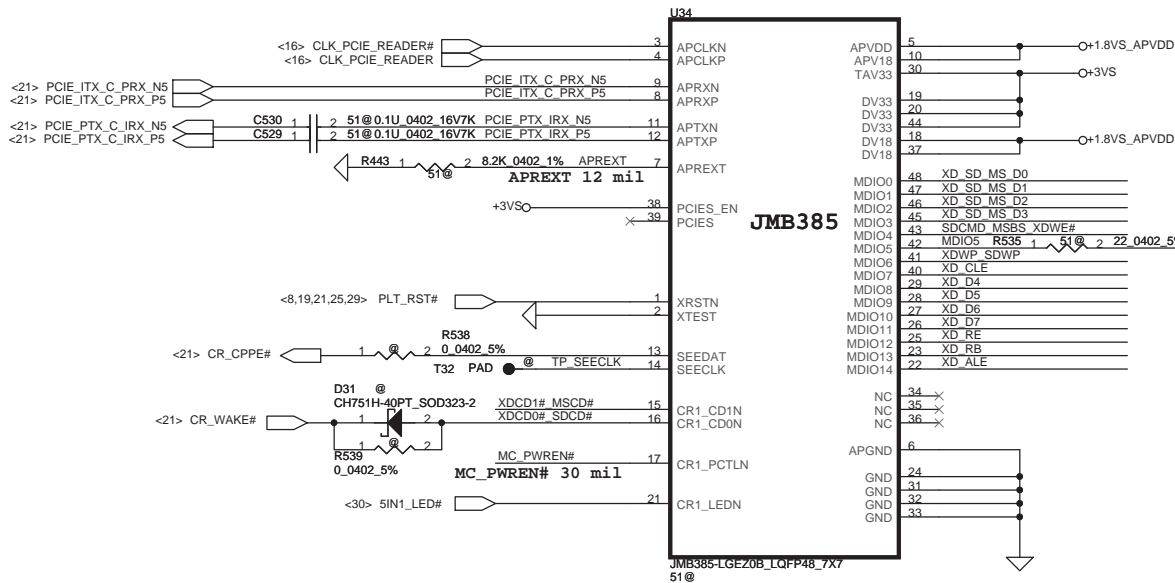
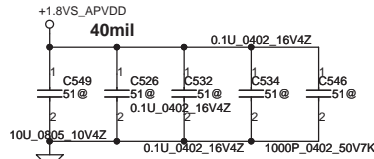
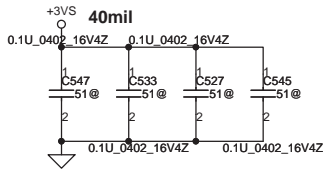
### SATA HDD Conn.



### SATA ODD Conn.

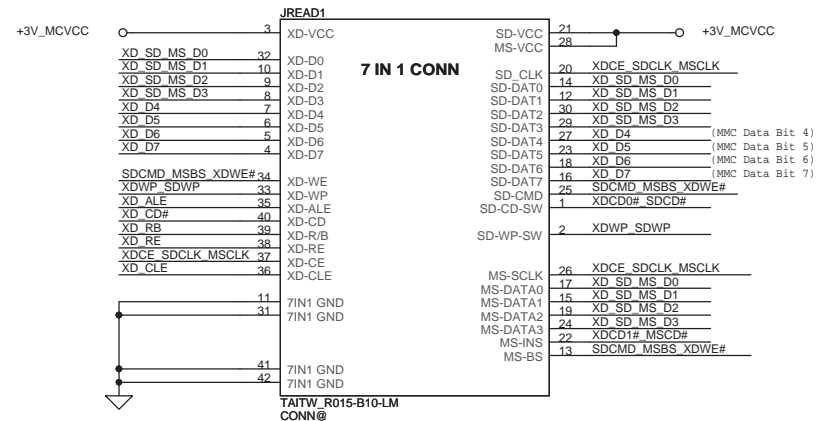
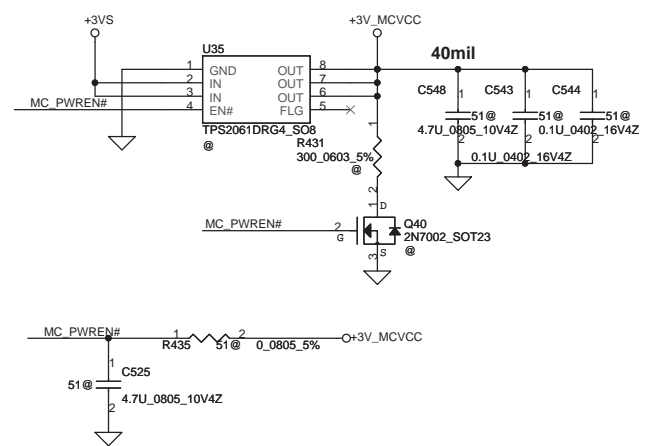


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**4 IN 1 Socket Push Type(New)**

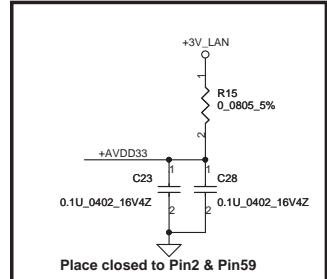
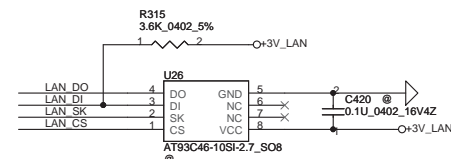
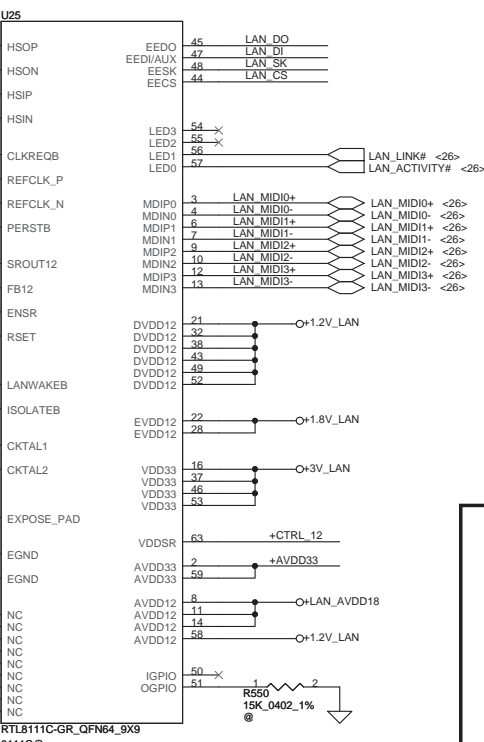
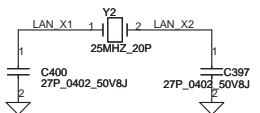
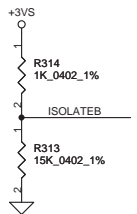
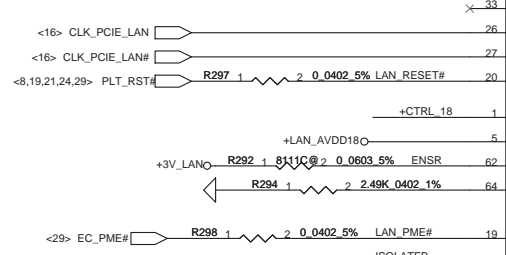
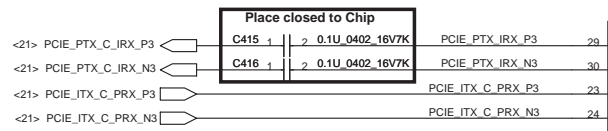
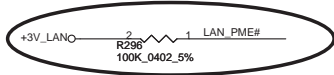
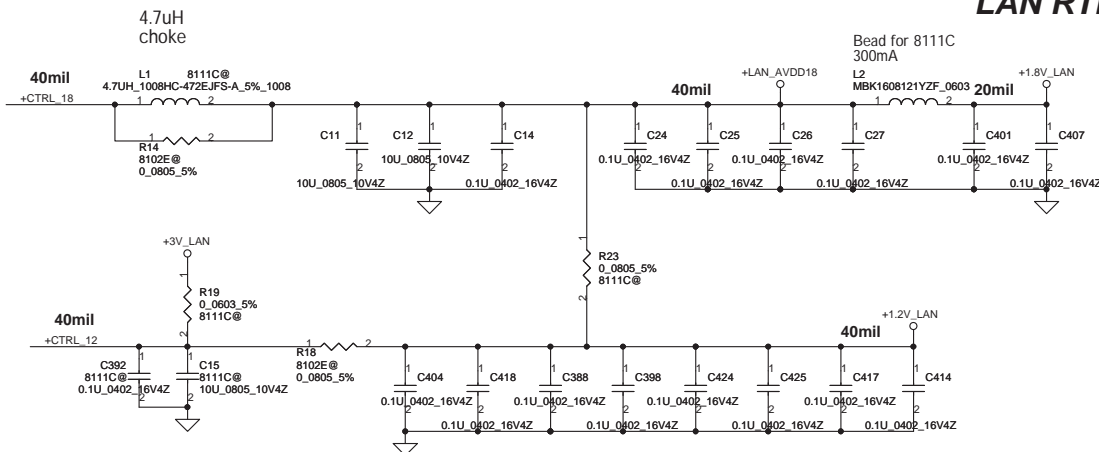
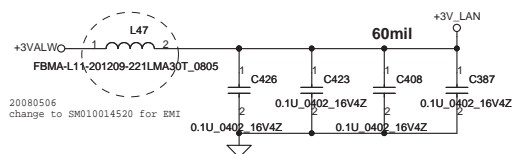
**Memory Card Power Switch**



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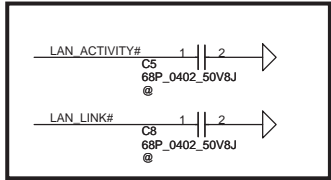
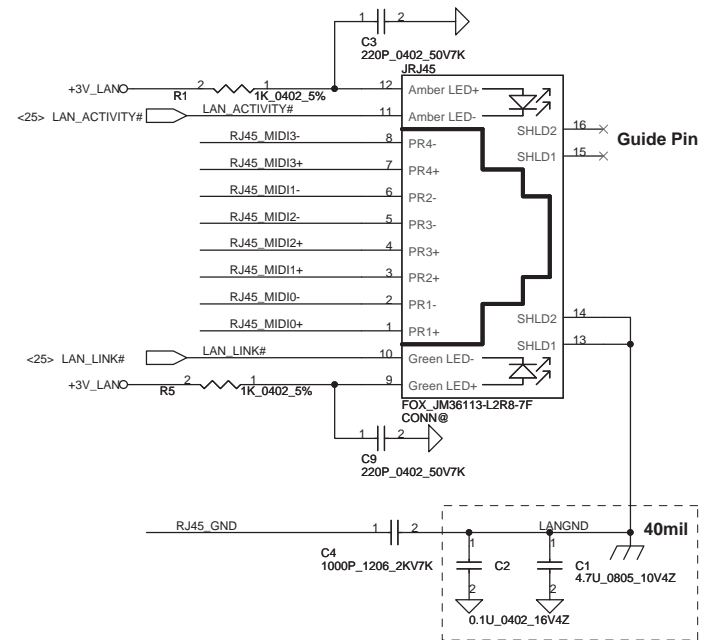
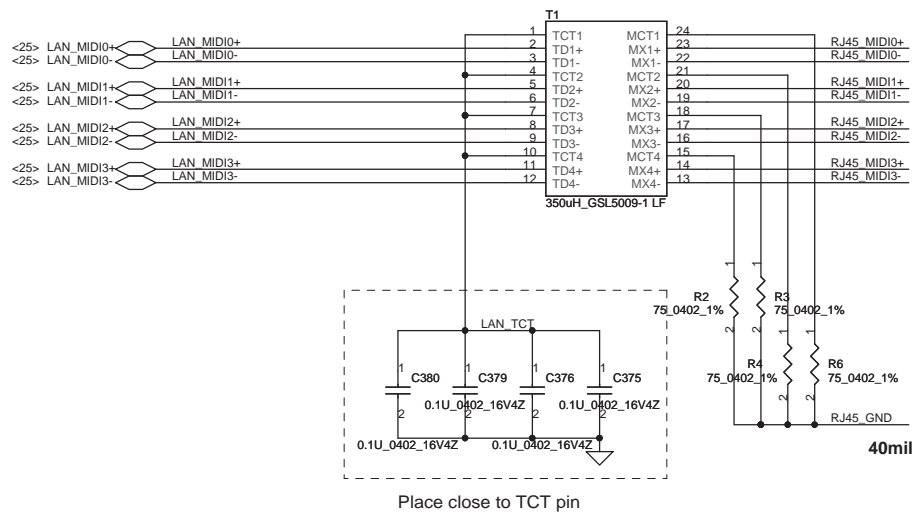
# LAN RTL8111C/8102E



RTL8111C-GR\_QFN64\_9x9  
8111C@

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# LAN RTL8111C/8102E

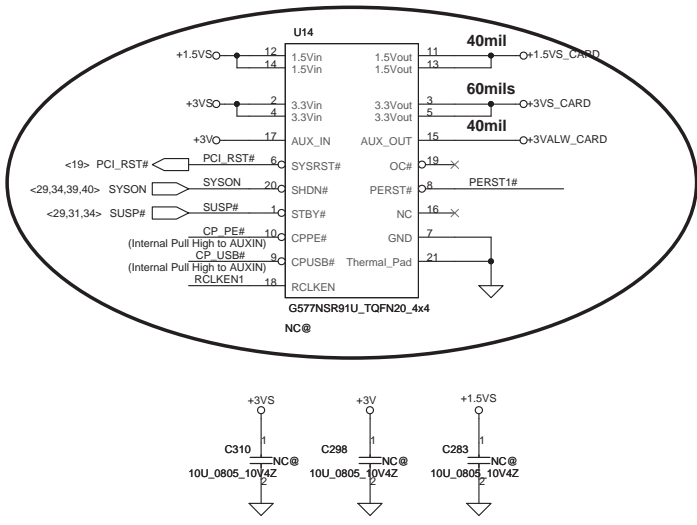


For EMI

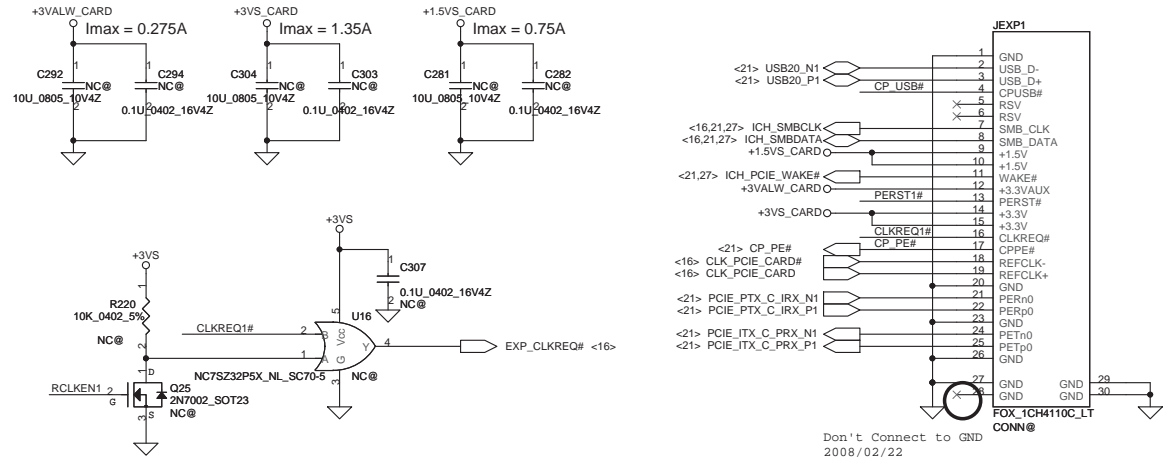
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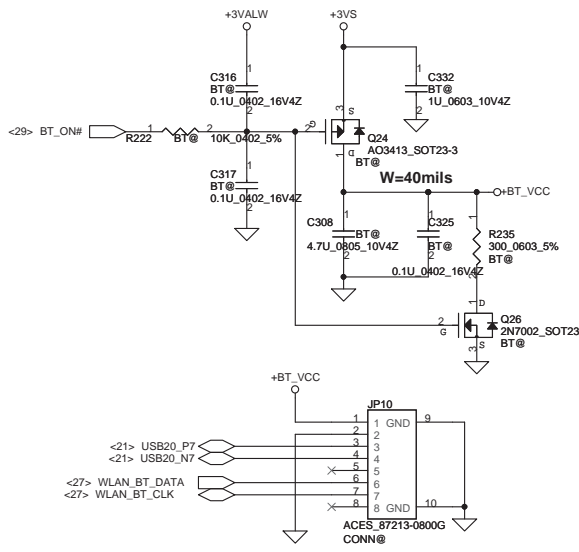
### New Card Power Switch



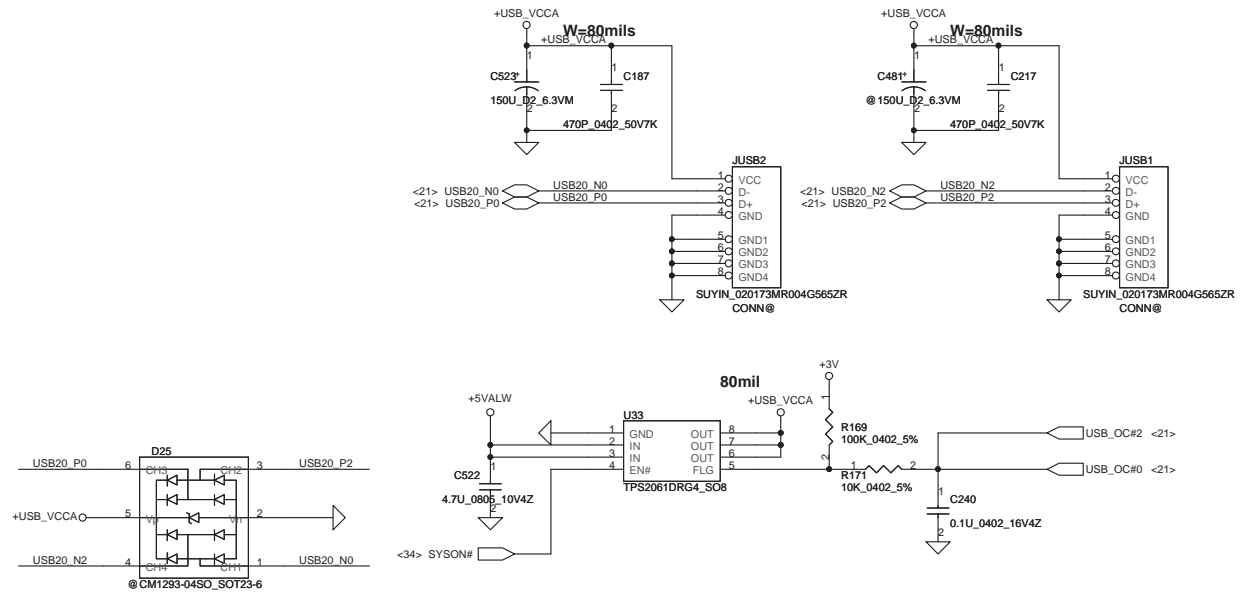
### New Card Socket (Left/TOP)



### Bluetooth Conn.

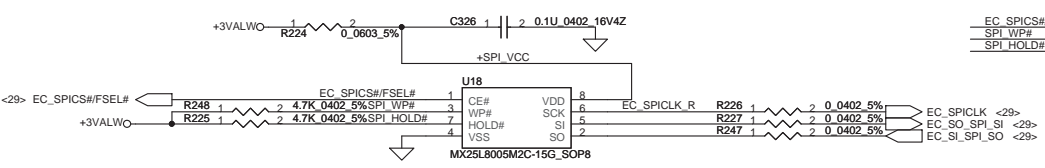


### USB CONN. (Stack-up Type)



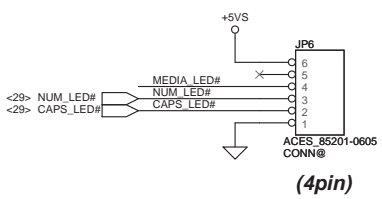
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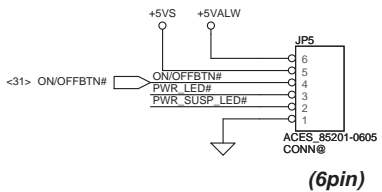


ENE suggestion SPI Frequency over 66MHz  
 SST: 50MHz  
 MXIC: 70MHz  
 ST: 40MHz

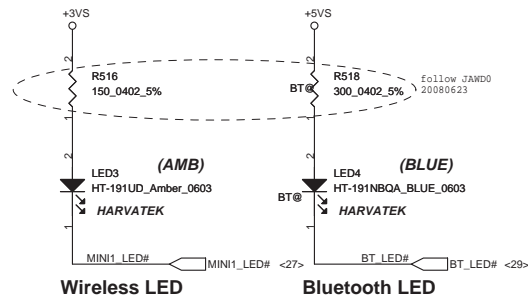
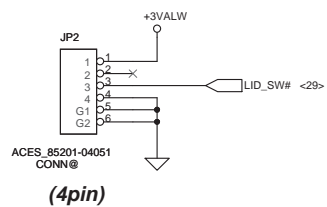
**To LED/B**



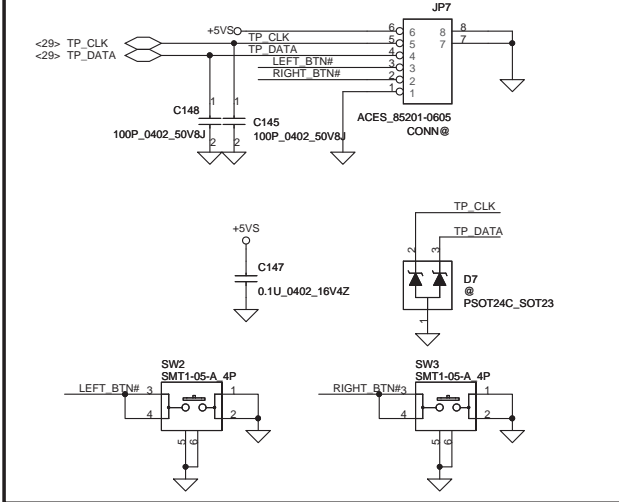
**To POWER/B**



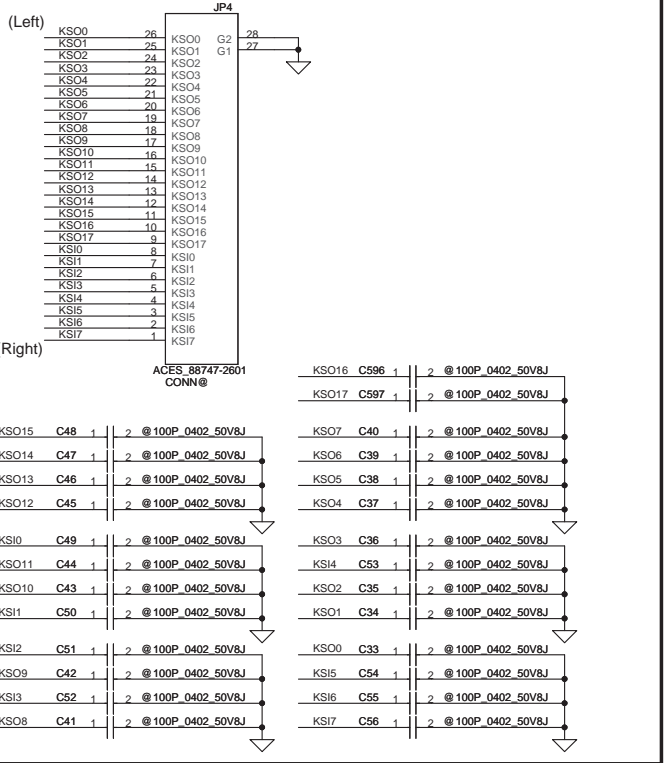
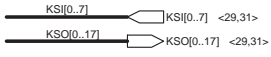
**To LID SW/B**



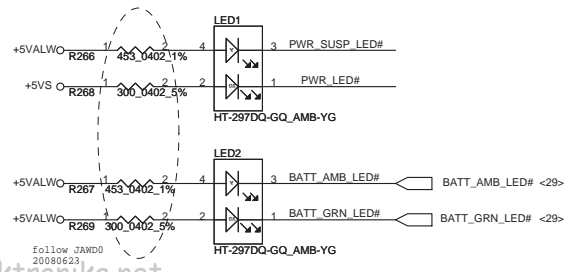
**To TP/B Conn.**



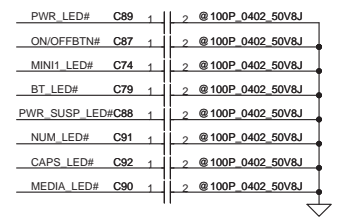
**INT\_KBD Conn.**



**Compal Footprint**



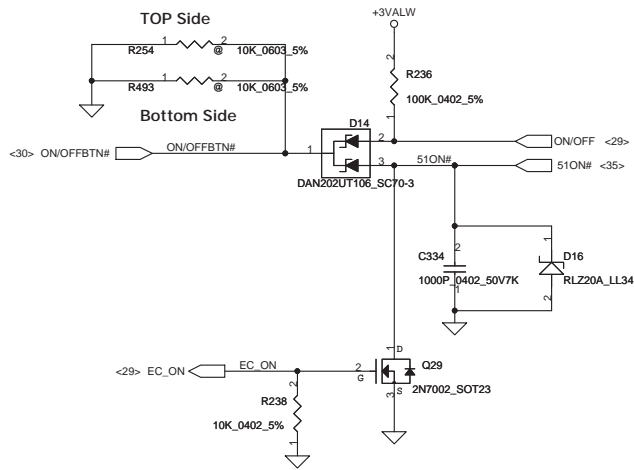
**FOR EMI**



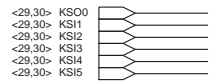
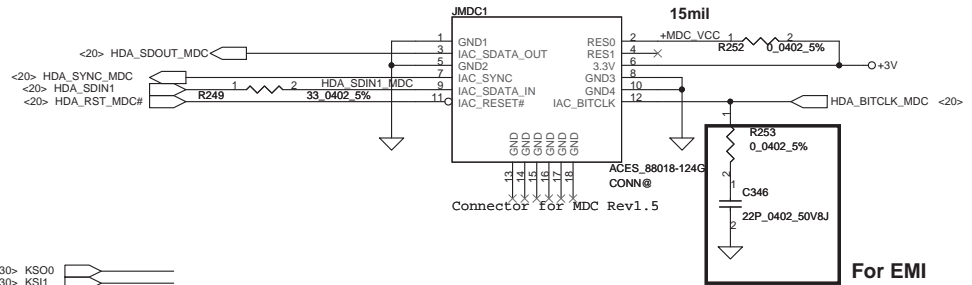
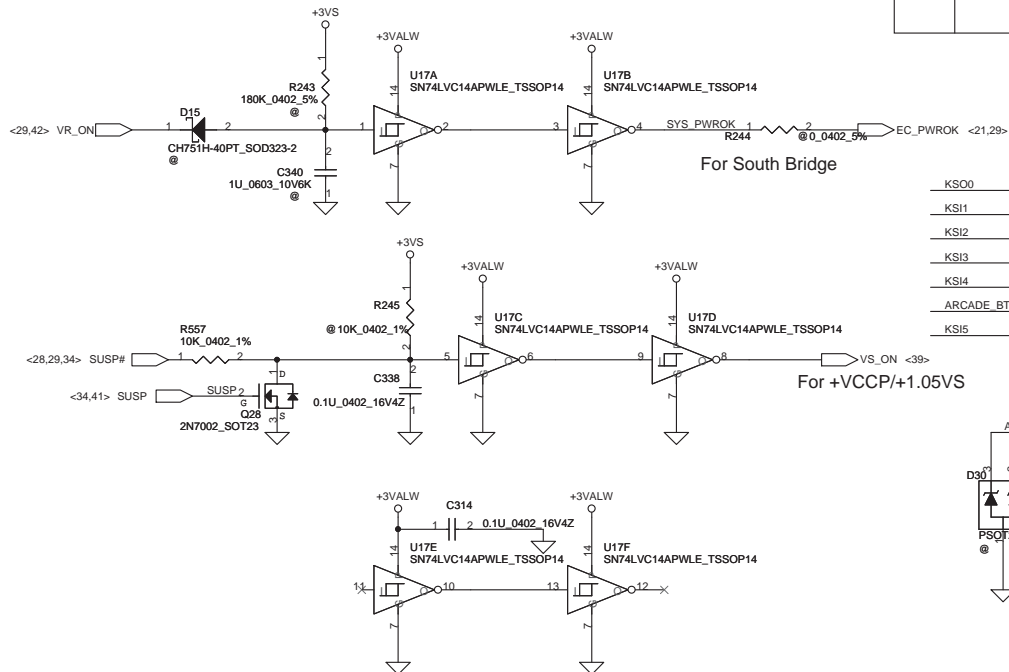
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# Power Button

ON/OFF switch



# Power ON Circuit

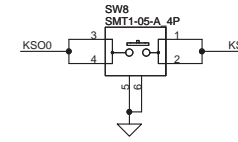


# To BTN/B Conn.

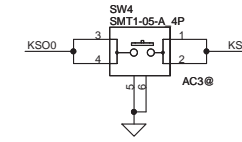
KSO0	
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

# HDA MDC Conn.

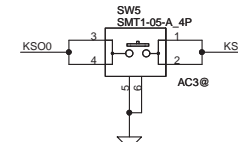
# Wireless Button



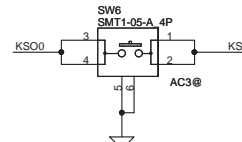
# Bluetooth Button



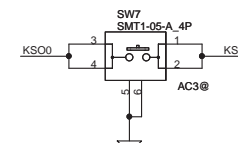
# Volume UP BTN



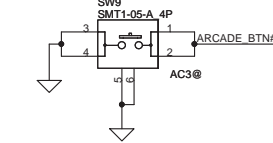
# Volume DOWN BTN



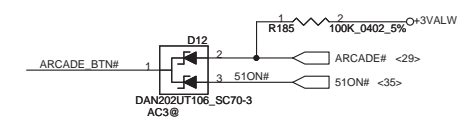
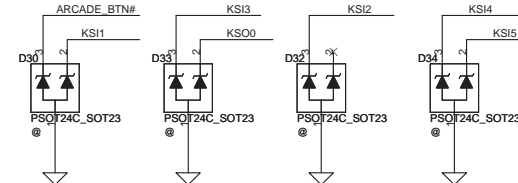
# e-Key BTN



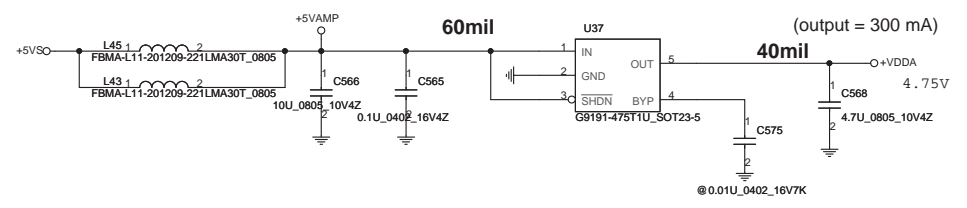
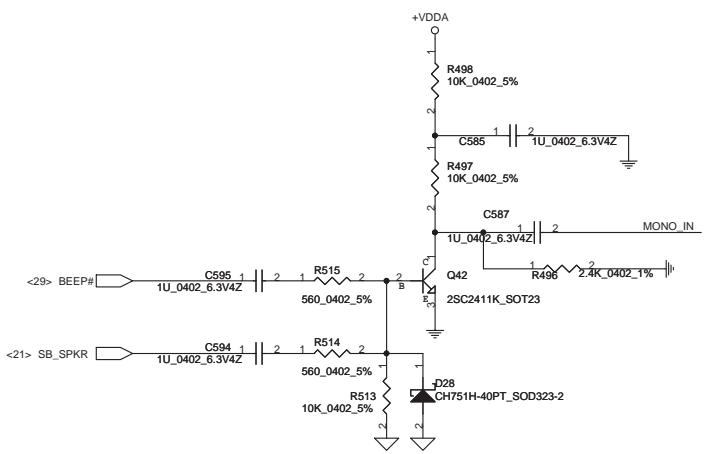
# ARCADE BTN



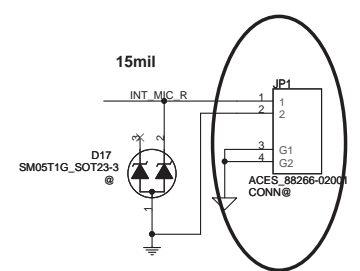
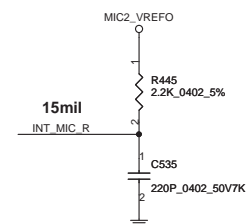
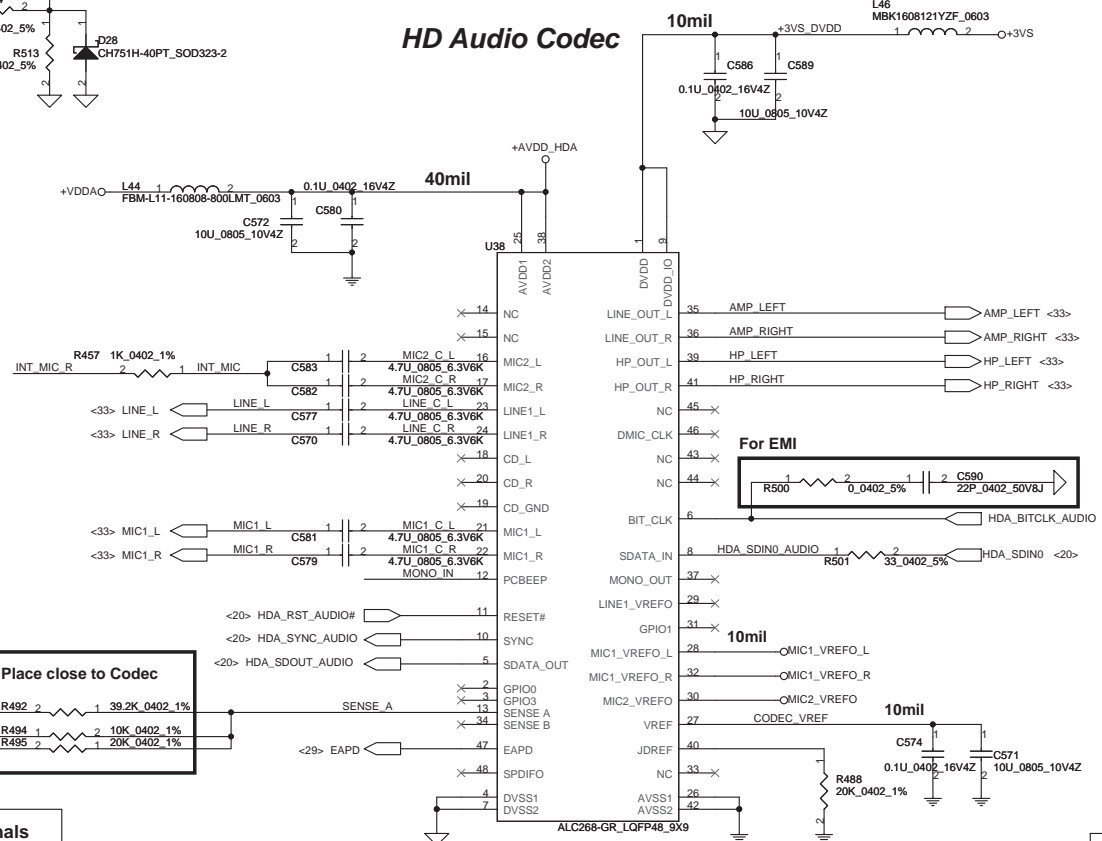
KSO0	C80	1	2	@ 100P_0402_50V8J
KSI1	C81	1	2	@ 100P_0402_50V8J
KSI2	C82	1	2	@ 100P_0402_50V8J
KSI3	C83	1	2	@ 100P_0402_50V8J
KSI4	C84	1	2	@ 100P_0402_50V8J
ARCADE_BTN#	C86	1	2	@ 100P_0402_50V8J
KSI5	C373	1	2	@ 100P_0402_50V8J



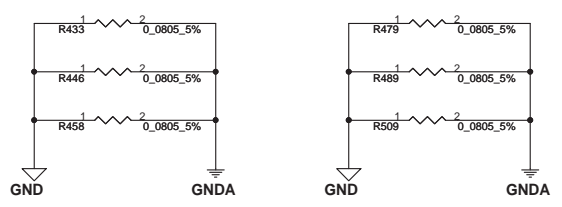
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### HD Audio Codec

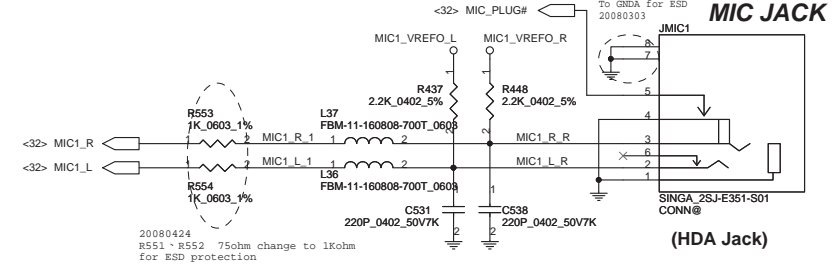
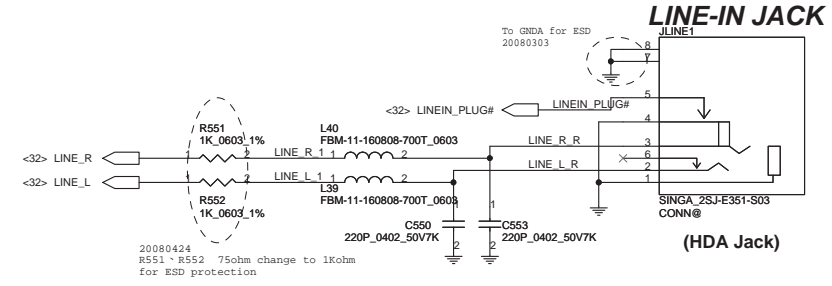
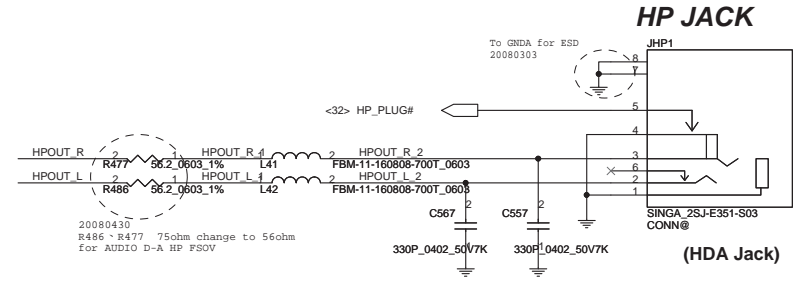
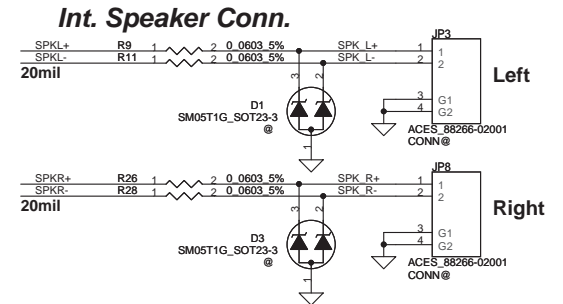
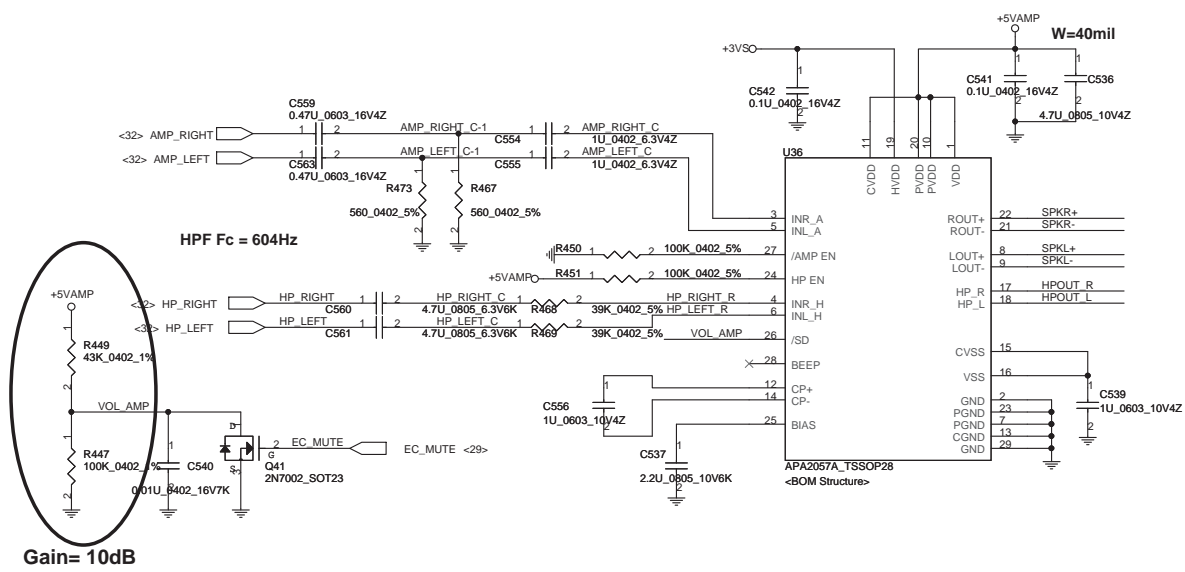


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



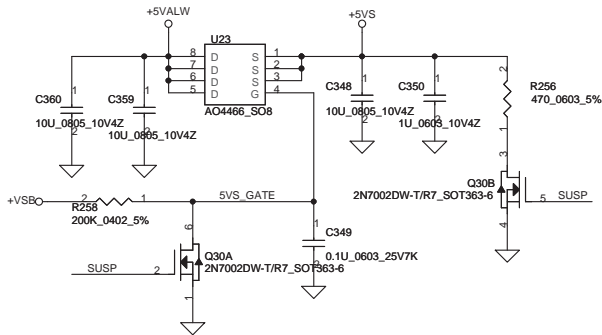
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				SHEMATICS, MB A4431 Sheet 32 of 45



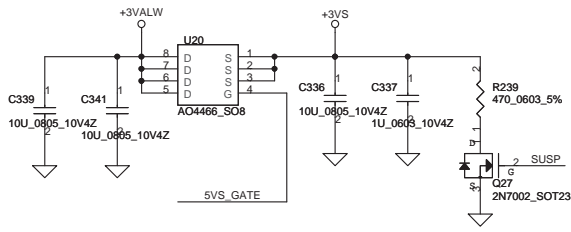


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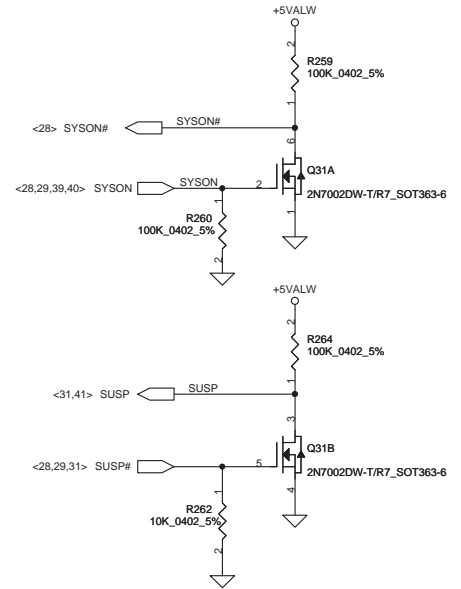
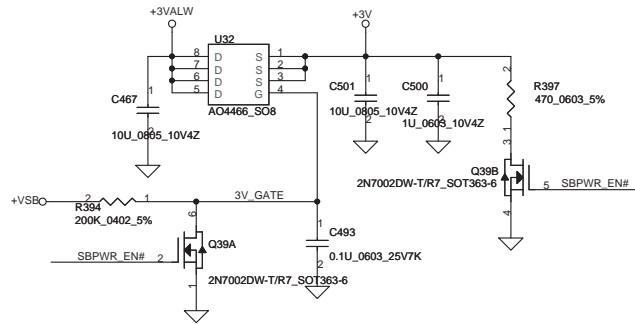
**+5VALW TO +5VS**



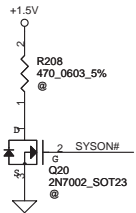
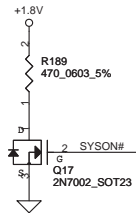
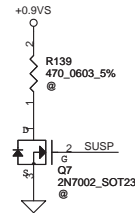
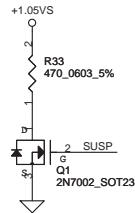
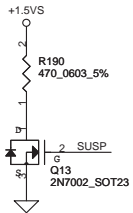
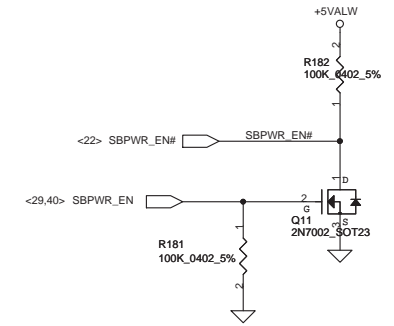
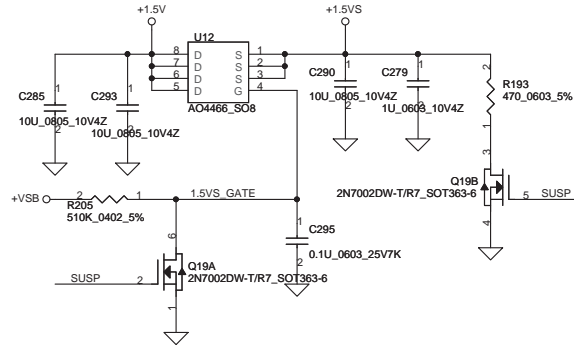
**+3VALW TO +3VS**



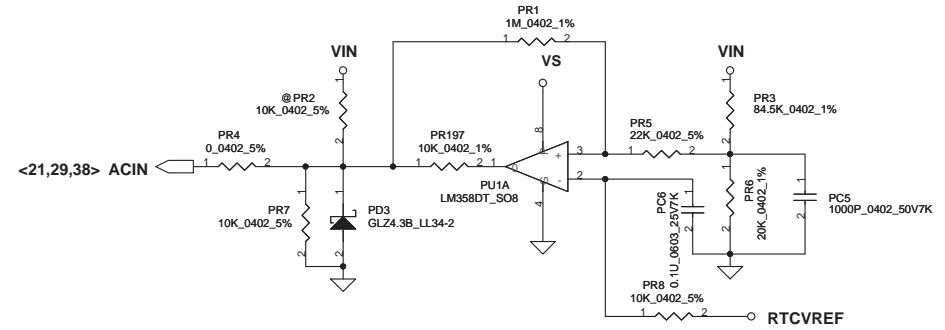
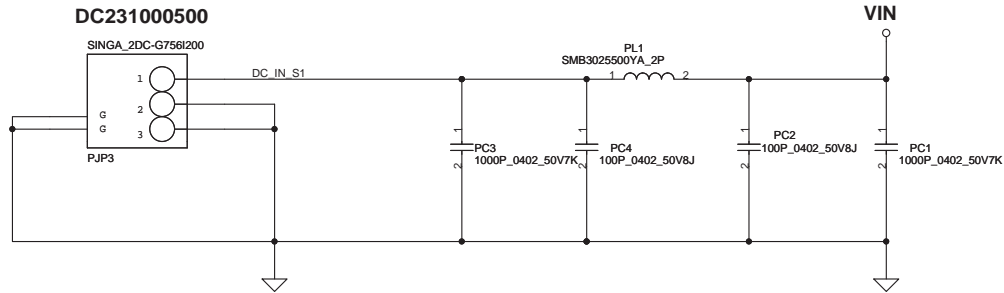
**+3VALW TO +3V\_SB(ICH8M AUX Power)**



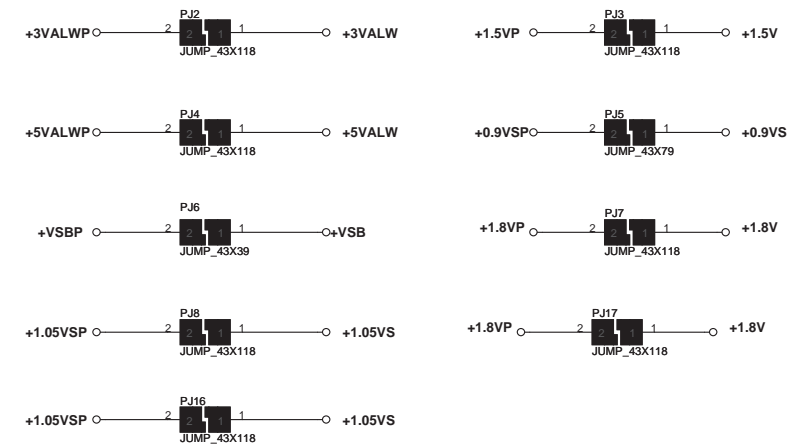
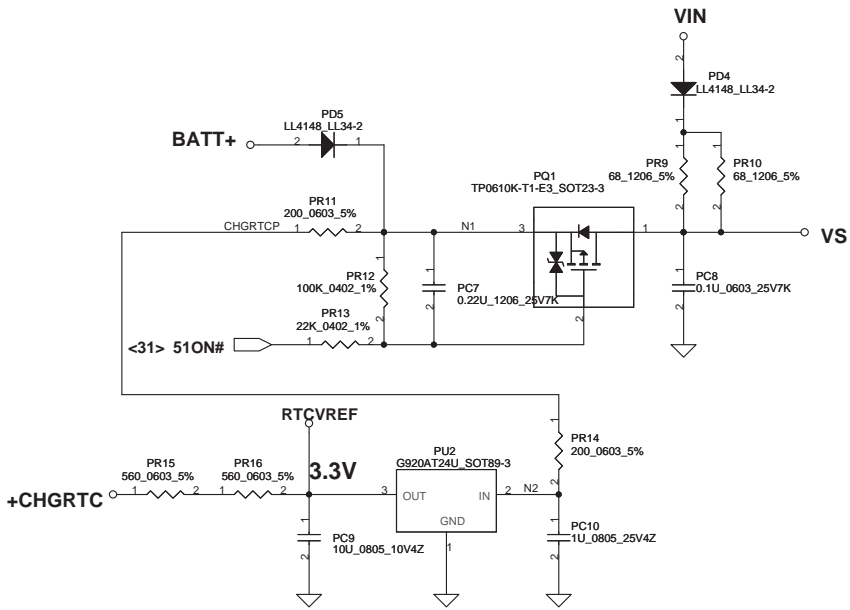
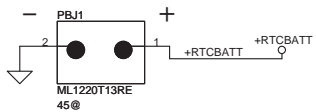
**+1.5V to +1.5VS**



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Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

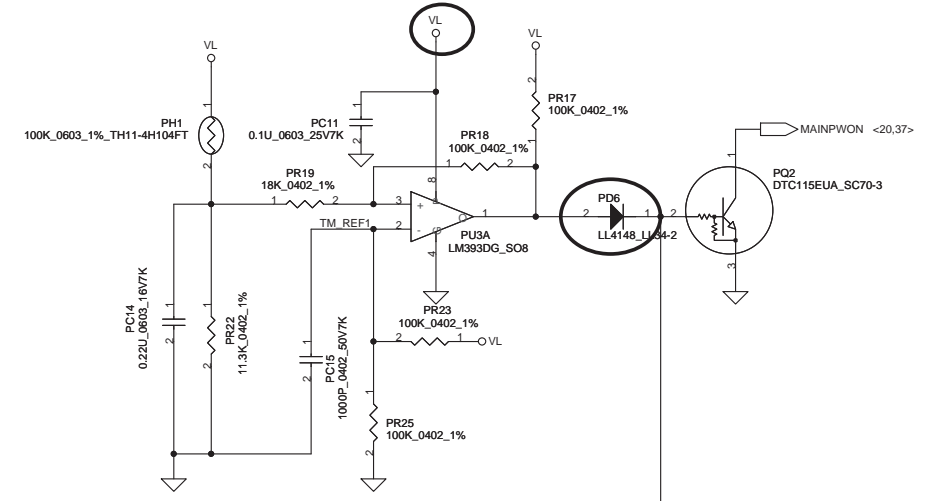
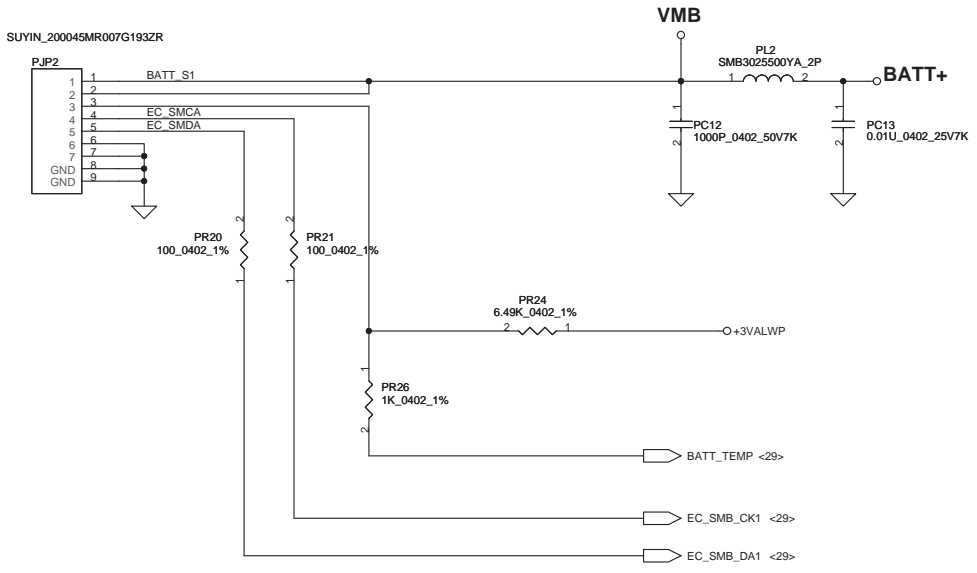


<http://hobi-elektronika.net>

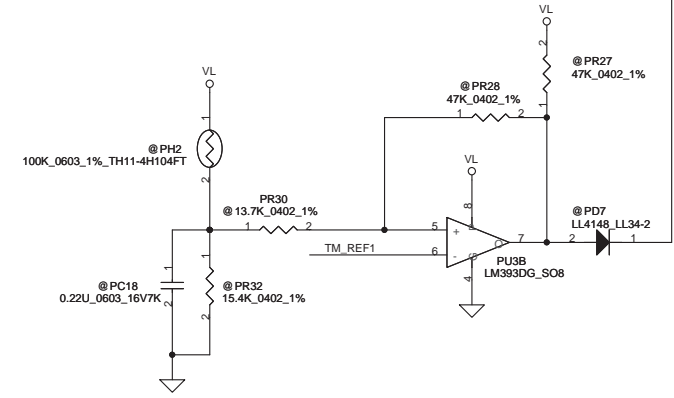
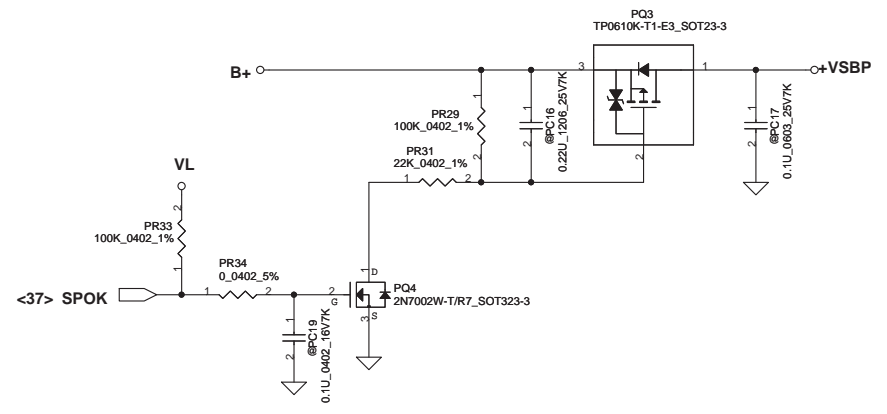
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PH1 under CPU botten side :  
 CPU thermal protection at 90 degree C  
 Recovery at 70 degree C

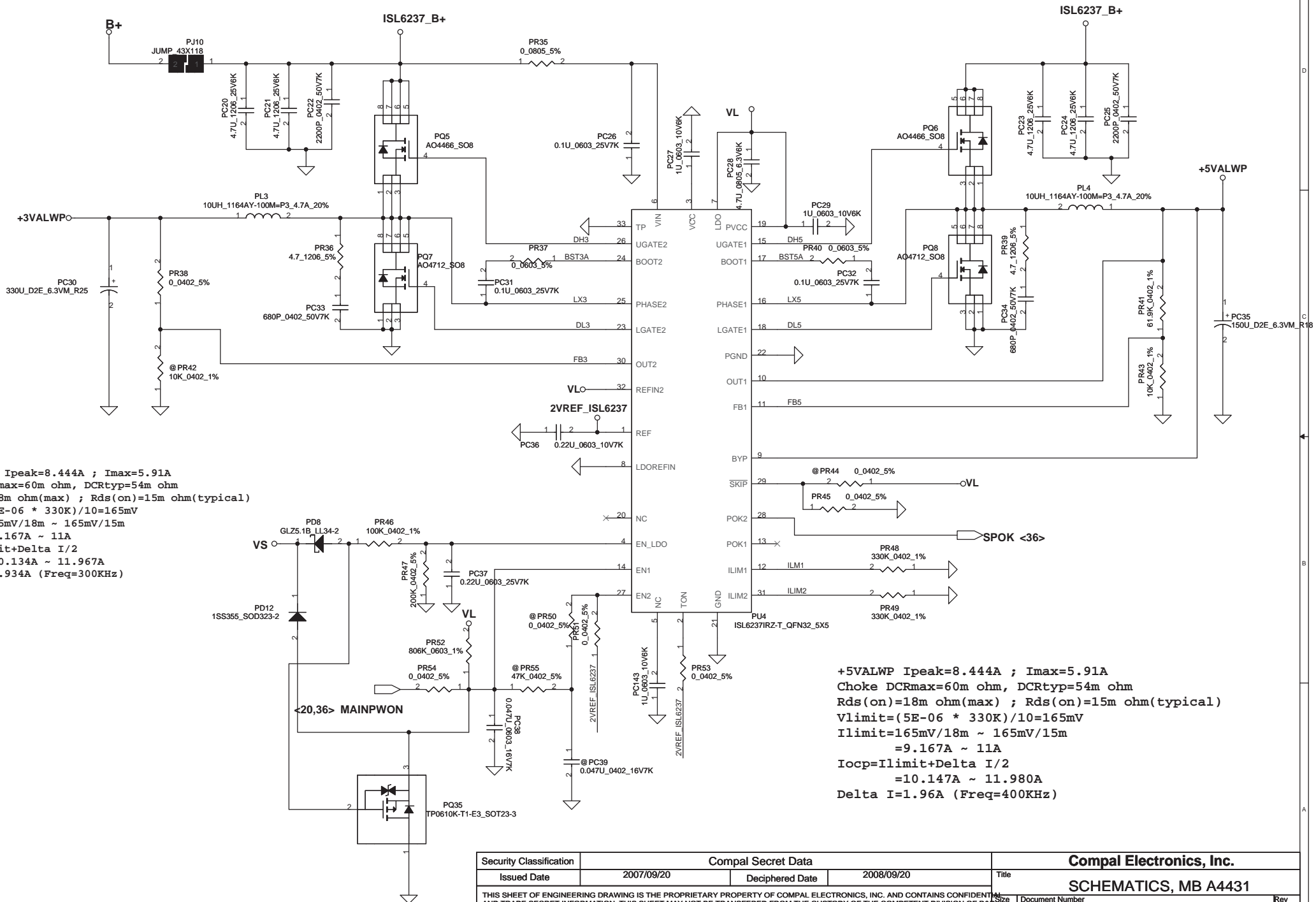
SUYIN\_200045MR007G193ZR



PH2 near main Battery CONN :  
 BAT. thermal protection at 90 degree C  
 Recovery at 70 degree C



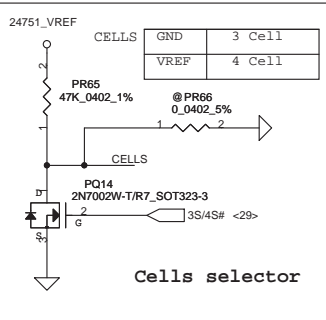
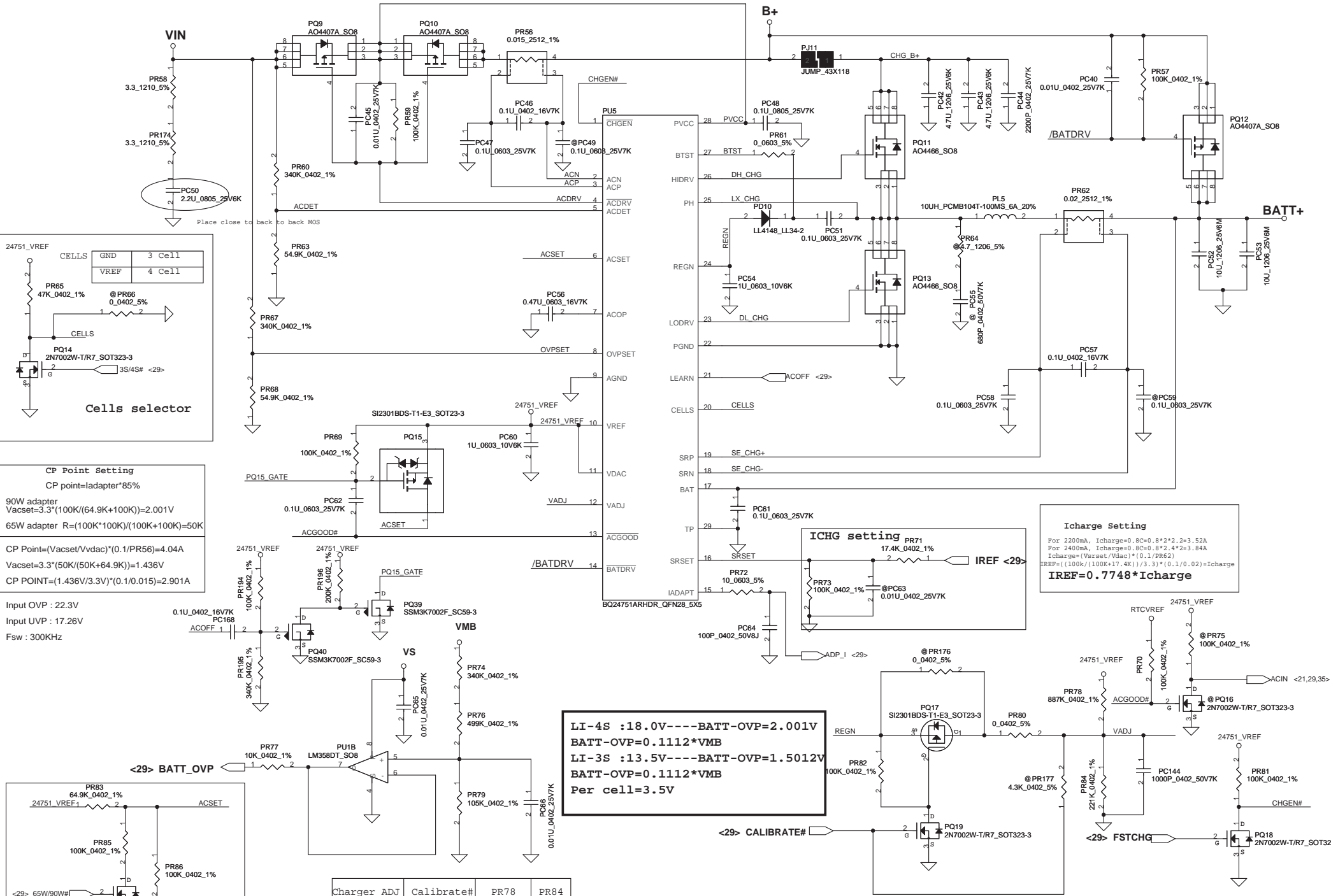
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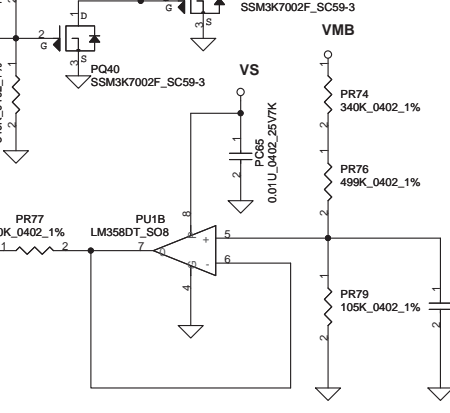
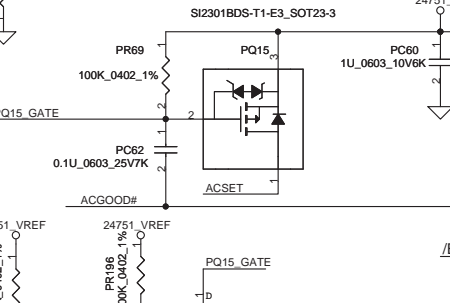
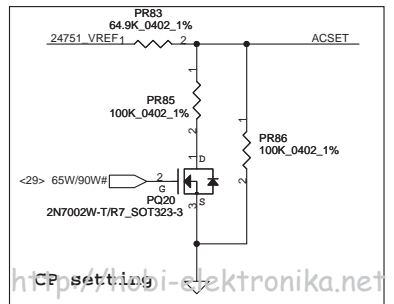
**+3.3VALWP** Ipeak=8.444A ; Imax=5.91A  
 Choke DCRmax=60m ohm, DCRtyp=54m ohm  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(5E-06 \* 330K)/10=165mV  
 Ilimit=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
 Iocp=Ilimit+Delta I/2  
 =10.134A ~ 11.967A  
 Delta I=1.934A (Freq=300KHz)

**+5VALWP** Ipeak=8.444A ; Imax=5.91A  
 Choke DCRmax=60m ohm, DCRtyp=54m ohm  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(5E-06 \* 330K)/10=165mV  
 Ilimit=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
 Iocp=Ilimit+Delta I/2  
 =10.147A ~ 11.980A  
 Delta I=1.96A (Freq=400KHz)

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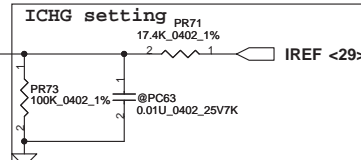


**CP Point Setting**  
 CP point=ladapter\*85%  
 90W adapter  
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$   
 65W adapter  $R = (100K \cdot 100K) / (100K + 100K) = 50K$   
 CP Point =  $(V_{acset} / V_{dca}) \cdot (0.1 / PR56) = 4.04A$   
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$   
 CP POINT =  $(1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$   
 Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz



**LI-4S : 18.0V --- BATT-OVP=2.001V**  
**BATT-OVP=0.1112\*VMB**  
**LI-3S : 13.5V --- BATT-OVP=1.5012V**  
**BATT-OVP=0.1112\*VMB**  
**Per cell=3.5V**

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

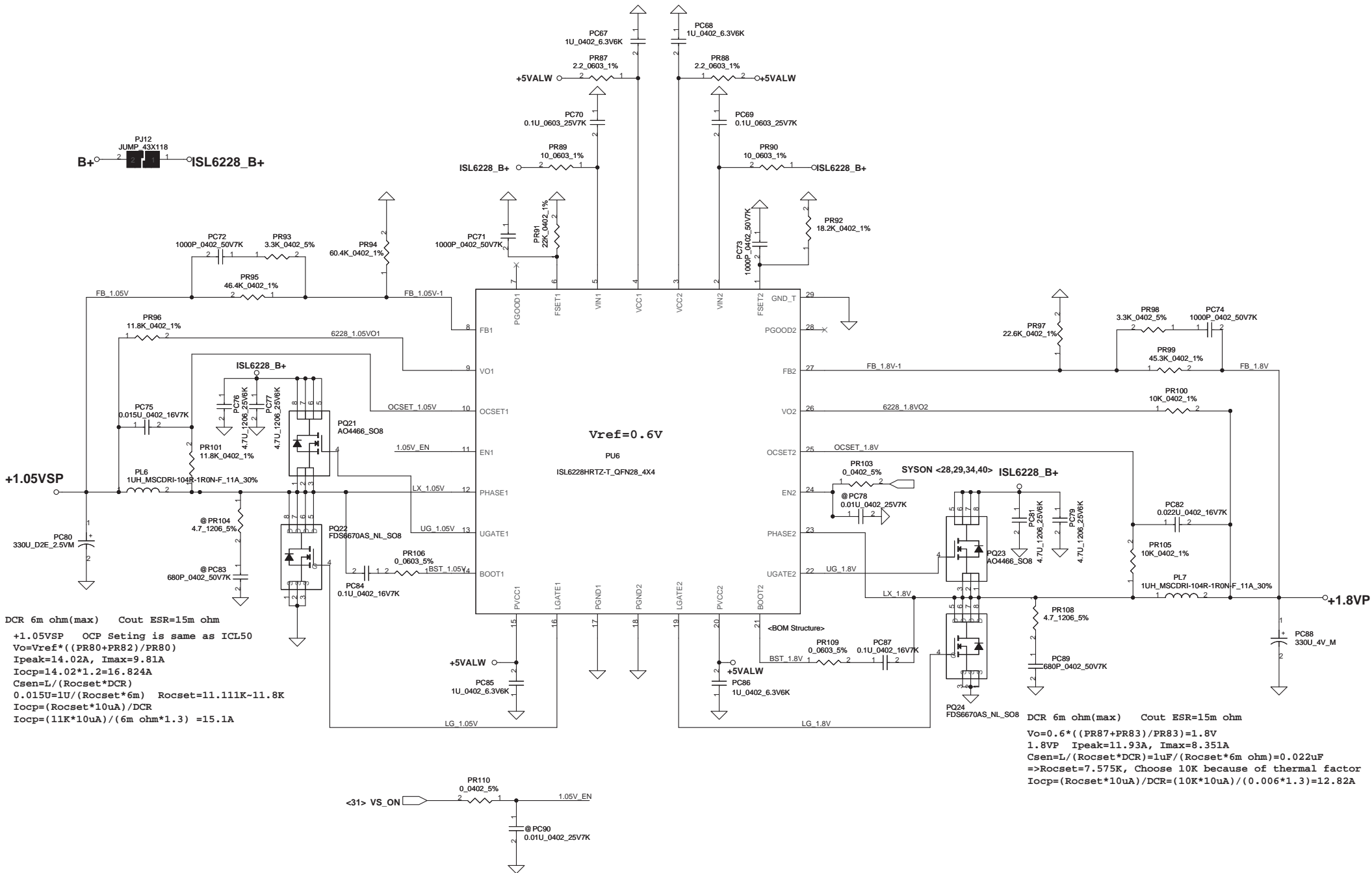


**Icharge Setting**  
 For 2200mA, Icharge=0.8C=0.8\*2.2=3.52A  
 For 2400mA, Icharge=0.8C=0.8\*2.4=3.84A  
 $I_{charge} = (V_{acset} / V_{dca}) \cdot (0.1 / PR62)$   
 $I_{REF} = ((100K / (100K + 17.4K)) / 3.3) \cdot (0.1 / 0.02) = I_{charge}$   
**IREF=0.7748\*Icharge**

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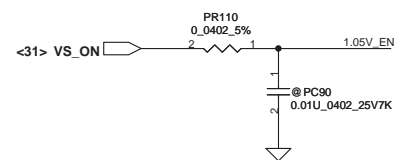
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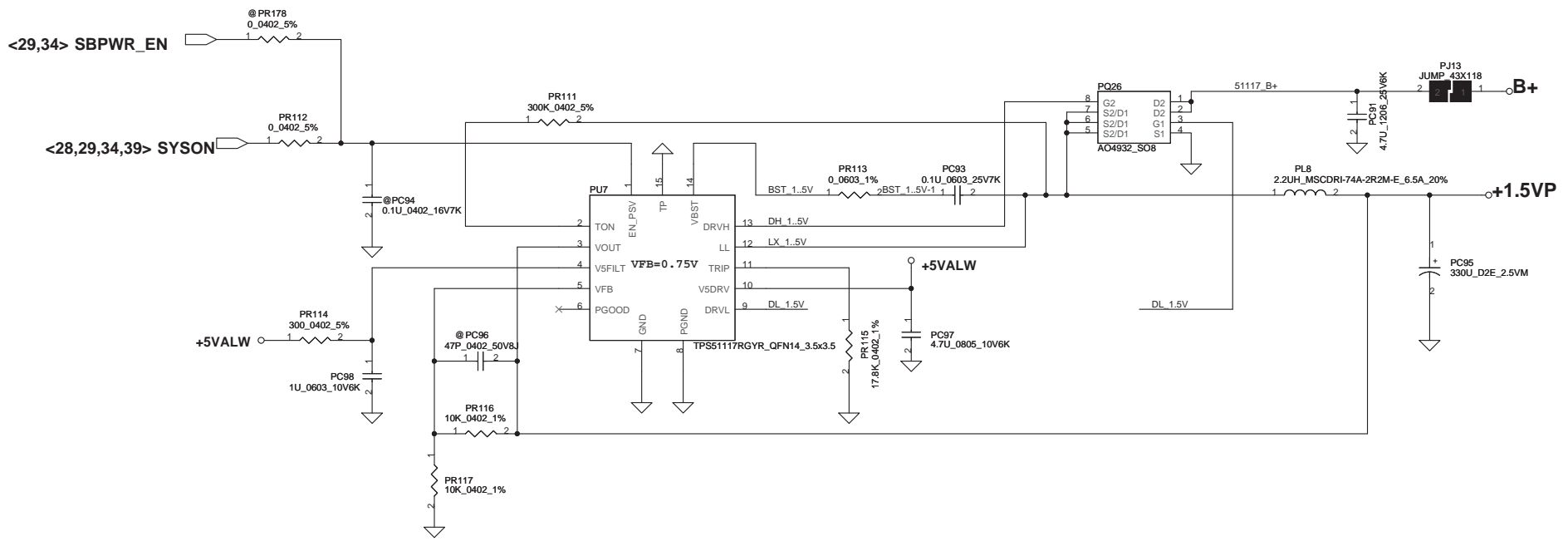


DCR 6m ohm(max) Cout ESR=15m ohm  
 +1.05VSP OCP Setting is same as ICL50  
 $V_o = V_{ref} * ((PR80 + PR82) / PR80)$   
 $I_{peak} = 14.02A$ ,  $I_{max} = 9.81A$   
 $I_{ocp} = 14.02 * 1.2 = 16.824A$   
 $C_{sen} = L / (Rocset * DCR)$   
 $0.015u = 1u / (Rocset * 6m)$  Rocset = 11.111K - 11.8K  
 $I_{ocp} = (Rocset * 10uA) / DCR$   
 $I_{ocp} = (11K * 10uA) / (6m ohm * 1.3) = 15.1A$

DCR 6m ohm(max) Cout ESR=15m ohm  
 $V_o = 0.6 * ((PR87 + PR83) / PR83) = 1.8V$   
 $1.8VP$   $I_{peak} = 11.93A$ ,  $I_{max} = 8.351A$   
 $C_{sen} = L / (Rocset * DCR) = 1uF / (Rocset * 6m ohm) = 0.022uF$   
 $\Rightarrow Rocset = 7.575K$ , Choose 10K because of thermal factor  
 $I_{ocp} = (Rocset * 10uA) / DCR = (10K * 10uA) / (0.006 * 1.3) = 12.82A$



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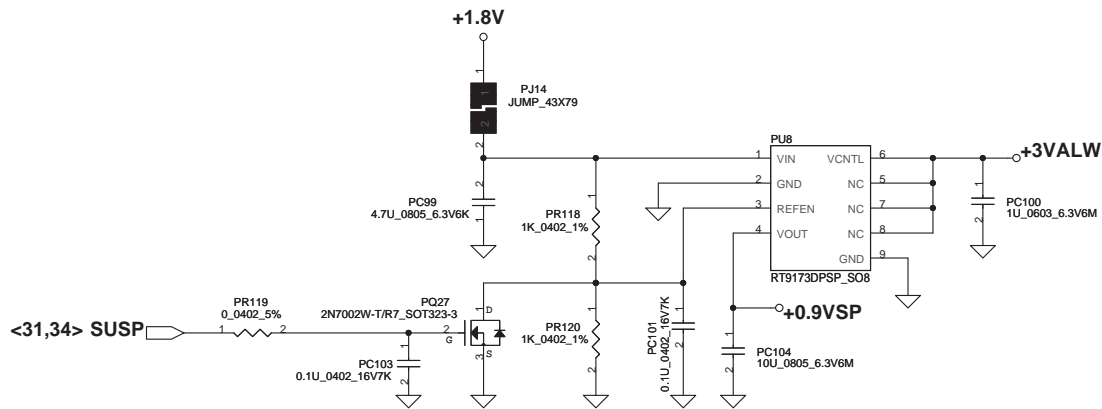


VFB=0.75V  
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19 * e^{-1.2} * 143000 * ((2/3) * V_o + 100mV) / 19 + 50ns$   
 $= 2.645e-7 \text{ us}$   
 $=> V_o / Vin = D = Ton / Ts \Rightarrow Ts = 3.35us$   
 $Fsw = 298KHz$

Cout ESR=15m ohm  
 $I_{peak} = 4.71A, I_{max} = 3.297A, I_{ocp} = 5.652A$   
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.107A$   
 $=> 1/2 \Delta I = 1.053A$   
 $V_{trip} = R_{trip} * I_{ocp} = 17.8K * 10uA = 0.178V$   
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.053A$   
 $= 0.178 / (0.027 * 1.2) + 1.053 = 5.493A + 1.053A = 6.546A$   
 $I_{ocpmax} = (0.178 / (0.021 * 1.1)) + 1.053A = 7.705A + 1.053A$   
 $= 8.758A$   
 $I_{ocp} = 6.546A - 8.758A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ISL6237 can't shutdown while battery only.	ISL6237 can't shutdown while battery only.	0.1	41	Add PQ35 SB906100210 TP0610K.	20071031	EVT
2	Delete PD1	Because we can cost down and B+ has another one.	0.2	39	Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071115	DVT
3	Change PQ9,PQ10,PQ12 to A04407A	Change PQ9,PQ10,PQ12 to A04407A	0.2	38	Change PQ9,PQ10,PQ12 to A04407A	20080509	DVT
4	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PD2 change to PR197 10K 0402 %1	20080509	DVT
5	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR2 unpop	20080509	DVT
6	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR4 change to 0 0402 %5	20080509	DVT
7	Change PR65	Cells voltage must over 2.5V	0.4	38	PR65 change to 47K 0402 %1	20080613	PVT
8	Node of PR70 is changed	Node of PR70 is changed	0.5	38	Node of PR70_100K_0402_1% change from VREF to RTCVREF	20080620	PVT
9	Add PC89,PR108	for EMI solution	0.6	39	Add PC89:680P_0402_50V7K PR108:4.7_1206_5%	20080620	PVT
10	Add PC169,PC170 on CPUB+	for EMI solution	0.6	42	Add PC169,PC170(470P_0402_50V7K) on CPUB+	20080620	PVT
11	Add PC171 on B+	for EMI solution	0.6	42	Add PC171(1000P_0402_50V7K) on B+	20080620	PVT
12	Change PR138 ,PR152	for EMI solution	0.6	42	PR138 ,PR152 change to 2.2_0603_1%	20080620	PVT
13	Change PR95	pull up the output voltage from 1.05v to 1.06 v	0.7	39	Change PR95 from 45.3K_0402_1% to 46.4K_0402_1%	20080623	PVT
14	Change PR17,PR18,PR19,PR22	Thermal protection 90oC & Recovery at 70oC	0.8	36	Change PR17 and PR18 to 100K_0402_1% Change PR19 to 18K_0402_1% and PR22 to 11.3K_0402_1%	20080701	PVT
15							
16							
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### A --> B Change List

4/24  
 <Page 22>  
 -R57 \ R133 10ohm change to 100ohm  
 -C135 \ C204 0.1u change to 1u  
 for ICH9 USB1.1 issue  
 <Page 33>  
 -R551 \ R552 \ R553 \ R554 75ohm change to 1K  
 for Audio ESD protection

4/30  
 -Update Power SCH  
 <Page 4>  
 -Add R27 \ C427  
 for +5VS drop issue  
 -R541 pull high 3.3V  
 <Page 33>  
 -R486 \ R477 75ohm change to 56.2ohm  
 for AUDIO D-A HP FSOV

5/2  
 -Bluetooth USBP5P/5N change to USBP7P/7N

5/5  
 -Modify LED test value  
 -Add 51@ \ NC@ \ GL@

5/6  
 -Update Power SCH  
 <Page 25>  
 -R290 change to L47(SM010014520)  
 for EMI

5/7  
 -add BT@ \ GM@

### B --> C Change List

6/25  
 <Page 16>  
 -C301 \ C296 33p change to 27p  
 for RTC issue

### C --> Pre MP Change List

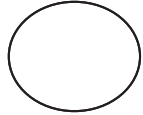
7/14  
 <Page 16>  
 -U31 SA00002Q830(QU37) change SA00002Q810(QU56)

7/28  
 -update Power SCH

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PCB KAWE0 LA-4431P LS-4391P/4392P/4393P

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