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<tr>
<td>04/25/05</td>
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</table>

**CHECKIN 01004**
- Checkin No. 01004
- Topic: RADAR 3848850
- Description: 2.5V VREG COST REDUCTION
- Details: CHANGED SOURCE OF Q1003 TO PP1V2_ALL

**CHECKIN 01001**
- Checkin No. 01001
- Topic: RADAR 3848846
- Description: UPDATE OF 2.5V RUN FET COST REDUCTION
- Details: ADDED DEVELOPMENT LEDS TO REGULATORS

**CHECKIN 00004**
- Checkin No. 00004
- Description: ADDED RV351LE GPU
- Details: REMOVED GPU VTT VREG

**CHECKIN 04001**
- Checkin No. 04001
- Description: CHANGED LINE AND NECK WIDTHS TO METRIC
- Details: CONVERTED DISCRETES TO LEAD FREE

**CHECKIN 03002**
- Checkin No. 03002
- Description: CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING
- Details: CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING

**CHECKIN 02004**
- Checkin No. 02004
- Description: <RADAR 3849718, 3849767, 3849854>
- Details: MADE ON & VISHAY FETS ALTERNATES

**CHECKIN 02003**
- Checkin No. 02003
- Description: MORE PHYSICAL & SPACING UPDATES
- Details: <RADAR 3877855> TP_VDD SET TO 1.80V

**CHECKIN 01006**
- Checkin No. 01006
- Description: CHECKIN 01007 / BOM RELEASE REV 02
- Details: CONVERTED DISCRETES TO LEAD FREE

**CHECKIN 13002**
- Checkin No. 13002
- Description: REMOVED OPTICAL TEMP SENSOR (U1602) FOR BETTER I2C BUS ROUTING
- Details: NOSTUFF R5950, STUFF R5923 FOR 17 INCH PANEL POWER FROM PP3V3_RUN

**CHECKIN 09004**
- Checkin No. 09004
- Description: NOSTUFF R5950, STUFF R5923 FOR 17 INCH PANEL POWER FROM PP3V3_RUN
- Details: <RADAR 3849662> STUFFED PANEL POWER SEQUENCING FOR BOTH 17 AND 20 INCH VESTA RESET AND LOWPWR DELAY

**CHECKIN 09002**
- Checkin No. 09002
- Description: REMOVED SOME FUNC_TEST PROPERTIES
- Details: CHANGED SDF7601 TO PART 860-0567

**CHECKIN 05004**
- Checkin No. 05004
- Description: CHECKIN 05003
- Details: ADDED KQA (337S3093) TO ALTERNATE PROCESSOR TABLE

**CHECKIN 05003**
- Checkin No. 05003
- Description: ADD 2.5V LDO FOR VESTA
- Details: USING PWM FROM ATI GPU

**CHECKIN 09002**
- Checkin No. 09002
- Description: REMOVED HYNIX FRAME BUFFER TO 333S0341 (NEW HYNIX SCREEN, SAME PART)
- Details: ADDED NET_PHYSICAL_TYPE = USB2 TO TABLE

**CHECKIN 05003**
- Checkin No. 05003
- Description: REMOVED SOME FUNC_TEST PROPERTIES
- Details: ADDED KQA (337S3093) TO ALTERNATE PROCESSOR TABLE

**CHECKIN 05004**
- Checkin No. 05004
- Description: CHECKIN 05003
- Details: REMOVED SMU DOWNLOAD CONNECTOR FROM DEVELOPMENT BOM

**CHECKIN 04001**
- Checkin No. 04001
- Description: ADDED RV351LE GPU
- Details: REMOVED GPU VTT VREG

**CHECKIN 03002**
- Checkin No. 03002
- Description: ADDED RV351LE GPU
- Details: REMOVED GPU VTT VREG

**CHECKIN 02004**
- Checkin No. 02004
- Description: ADDED RV351LE GPU
- Details: REMOVED GPU VTT VREG
### Processors

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<th>Reference Designator(s)</th>
<th>Alternate For</th>
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<tbody>
<tr>
<td>U2900</td>
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<td>IC, GPUL, DD3.1, 2.0G, 85C, KPA</td>
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### ASICS

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<td>CPU_1_8GHZ</td>
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### Misc Parts

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<tr>
<td>IC, SMU, Q45C/D</td>
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### Alternates

<table>
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<tr>
<th>Description</th>
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<tr>
<td>MOSFET, N-CH, VISHAY</td>
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### Table Items

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BARCODE LABEL, MLB, Q45</td>
</tr>
</tbody>
</table>

**Notes:**
- **Critical:** RV351 GPU EUTECTIC
- **Critical:** LM1117 LEAD
- **Critical:** DS1338, L-F PART
- **Critical:** MOSFET, N-CH, VISHAY
- **Critical:** KINGBRIGHT LED
2.5V VOLTAGE REGULATOR

**Note:**
- VOUT = VREF*(R903+R905)/R905 = 2.588VDC
- Set OUTPUT = 2.588V for FRAMEBUFFER.

**Peak Current:**
- 9.24A without DIMM termination
- 12.68A with DIMM termination

**Component Values:**
- R900: 1.1K 5%
- R901: 27.4K 1%
- R902: 10.7K 5%
- R903: 402 5%
- R904: 470K 5%
- R905: 1/16W 1%
- R906: 4.7 5%
- R907: 240 5%
- R908: 2.0X1.25A
- D900: IRF7413 SO-8
- D901: MBR0520LXXG SOD-123
- D902: MBR0520LXXG SOD-123
- C901: 603 2200PF
- C902: 603 1800UF
- C903: 603 1800UF
- C904: 603 1UF
- C905: 603 1UF
- C906: 603 20%
- C907: 603 10%
- C908: 603 20%
- C909: 603 20%
- C910: 603 20%
- C911: 603 20%
- C912: 603 20%
- C913: 603 20%
- C914: 603 20%
- C915: 603 20%
- C916: 603 20%
- C917: 603 20%

**Reference:**
- www.vinafix.vn
Ethernet Low Pwr

2.5V LDO

To keep Vesta from being held
in reset when system is off
NOTE: reset GPIO in active mode.
NOTE:

SET OUTPUT=1.5VDC FOR U3LITE CORE

VOUT=VREF/(R2203+R2205)/R2205=1.53VDC

7.73A OF PEAK CURRENT DRAW ON IPDANTLRB

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
AGREES TO THE FOLLOWING

1.5V RUN FET

IN D5 STATE

CHECK POS

U3LITE CORE POWER

PPVIRCH1-PPVCORE_NB

REV.

=PPVIRCH1

=PPVCORE_NB

U3LITE CORE POWER

PPVIRCH1-PPVCORE_NB

REV.

=PPVIRCH1

=PPVCORE_NB

www.vinafix.vn
**Page Notes**

- **Power Sequencing:**
  - PCI bus voltage and appropriate PCI bus voltage and
  - Connect _PPPCI32_PWRON_SB to same if 64-bit
  - PCI pads use the VIO supply to meet
  - NOTE: PCI pads use the VIO supply to meet

**BOM options provided by this page:**

- Power Sequencing:
  - Note power Shasta Worse rail before any other Shasta supplies.
Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP1V2_PWRON_SB_PLL45VDD
- _PP3V3_PWRON_SB

Power aliases required by this page (OPRER):
- _R2557

New options provided by this page:
- PCI 64-bit select

NorthBridge / SouthBridge MPIC Routing

Interrupt controller.
Selects whether NorthBridge or MPIC NB/MPIC SB.

Signal aliases required by this page:
- _PP3V3_PCI

www.vinafix.vn
PROCESSOR LOGIC I/O
NONE

MEM TERM VREGS

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
PP1V25_RAM_VTT
VOLTAGE=1.25V

TURN_ON_VTT
SYS_SLEEP
U4600_REFOUT
=PP3V3_PWRON_RAM
=PP2V5_PWRON_RAM
VR4600_SHTDWN

SYNC_MASTER=N/A
SYNC_DATE=N/A
MEM TERM VREGS

www.vinafix.vn
Page Notes

Power aliases required by this page:
- PP1V2_PWRON_HT

Options provided by this page:
- SB_HT_200M
- PP1V2_PWRON_HT_PLLDVDD

Resistor to select 200MHz HT I/F.

www.vinafix.vn
SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2

www.vinafix.vn
ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

- Pack fits with components across all samples except (hole)

<table>
<thead>
<tr>
<th>Component</th>
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<td>PCI_SB_FRAME_L</td>
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<td>PCI_SB_CBE_L&lt;2&gt;</td>
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</table>

PLACE CLOSE TO SHAFTA

- MF-LF 1/16W 5% 402

- MF-LF 1/16W 5% 547

- MF-LF 1/16W 5% 547
Q85 WIRELESS CONNECTOR

NOTE: This AirPort implementation does not support PME.

PCI_CLK33M_AIRPORT (33MHz PCI clock)

Signal aliases required by this page:
- _PP3V3_PCI

Power aliases required by this page:
- _PCI_CLK_AIRPORT

APPLE COMPUTER INC.
www.vinafix.vn
NOTE: This USB2 implementation supports AD27 (Slot "G") - USB2 (0x1033/0x0035)

BOM options provided by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

Signal aliases required by this page:

Power aliases required by this page:

www.vinafix.vn
## Page Notes

**Power aliases required by this page:**
- PP2V5_PWRON_SB

**Signal aliases required by this page:**
- None

**BOM options provided by this page:**
- None

**Page Ending:**
- 74 25

---

**Shasta FireWire**

**Device:**
- U2300 (V1.0) SHASTA

**Notes:**
- SHASTA FireWire

---

**Table:**

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<td>FW_LPS</td>
<td>FW_PCLK</td>
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<td>FW_DATA&lt;7..0&gt;</td>
<td>FW_CLK98M_LCLK</td>
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<tr>
<td>FW_CTL&lt;1..0&gt;</td>
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**Shasta FireWire**

**Device:**
- U2300 (V1.0) SHASTA

**Notes:**
- SHASTA FireWire

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**Shasta FireWire**

**Device:**
- U2300 (V1.0) SHASTA

**Notes:**
- SHASTA FireWire

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<tr>
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</table>
NOTE: Target differential impedance for Secondary Length: 500 mils
Length Tolerance: 50 mils

Net Spacing Type: USB2
Line To Line: 78.5 mils
Line To Ground: 75.5 mils
Primary Max: 75.5 mils
Secondary Max: 75.5 mils
Secondary Length: 800 mils

USB2 data pairs in ESSD.

Page Notes
Power aliases required by this page:
- PP3V3_PWRON_USB

OMIT options provided by this page:
- ELECTRICAL_CONSTRAINT_SET

BOM options provided by this page:
- USB2_NEC_XTAL
- USB2_2
- USB2_4
- USB2_3
- USB2_1
- USB2_0
- NC28
- NC27
- NC26
- NC25
- NC23
- NC21
- NC20
- NC19
- NC18
- NC15
- NC13
- NC12
- NC11
- NC10
- NC9
- NC8
- NC7
- NC6
- NC4
- Y1
- W3
- V2
- U6
- U5
- U3
- T8
- T7
- T5
- T4
- T2
- T1
- R4
- P7
- TP_SB_NC_Y3
- TP_SB_NC_V3
- TP_SB_NC_V2
- TP_SB_NC_U6
- TP_SB_NC_U3
- TP_SB_NC_U1
- TP_SB_NC_T6
- TP_SB_NC_T4
- TP_SB_NC_T2
- TP_SB_NC_R6
- TP_SB_NC_R5
- TP_SB_NC_R4
- TP_SB_NC_R3
- TP_SB_NC_P7

www.vinafix.vn
External USB Ports

**USB Device Interfaces**

**Page Notes**
- Power intent required by this page:
  - TP_USB2_PWREN<4>
  - TP_USB2_PWREN<2>
  - TP_USB2_PWREN<1>
  - TP_USB2_PWREN<0>

- Voltage constraint MAN TYPED:
  - VOLTAGE=5V

**neoborg Implementation**
- Notes: This design does not provide power control on USB ports e.g., PWR, D+/D- XNets.

- terminations and/or to properly terminate unused signals.

- Net Spacing Type:
  - MIN_NECK_WIDTH=0.25MM
  - MIN_LINE_WIDTH=0.6MM

- USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to mating USB ports.

- Unnamed provided by this page:
  - VOLTAGE=0V

- USB ports are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to mating USB ports.

**NOTE:** This design does not provide power control on USB ports e.g., PWR, D+/D- XNets.

**NOTE:** This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.
Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

---

Q52 Modem Connector
SDP9400
STDOFF-3MM-5MM-I-B

---

C9401
C9402

---

SDP9401
STDOFF-5MM-5MM-I

---

RJ11 CONNECTOR

---

From Intel Mobile Audio/Modem

---

Modem Interface

---

APPENDIX OF PROPRIETARY PROPERTY

---

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---

www.vinafix.vn
LINE OUT LOW-PASS FILTER

FC = 37 Hz, NO = -1.4

LINE OUT AMP

APPLE P/N 35100687

SYNC_DATE=02/16/2005

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SYNC_MASTER=AUDIO

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Notice of Proprietary Property

Scale

Size

D

NONE

051-6772

E

102

A

B
