1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

PRODUCTION RELEASED

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
M		508667	PRODUCTION RELEASED	06/04/07	06/22/04

PDF	CSA	CONTENTS	MASTER	DATE
2	2	System Block Diagram	M51_PAUL	08/04/2006
3	3	Power Block Diagram	M51_PAUL	08/04/2006
4	4	BOM Config	M51_DAVE	(MASTER)
5	5	FUNC TEST 1 OF 2	M51_HENRY	08/04/2006
6	6	POWER CONN / MISC	M51_PAUL	08/04/2006
7	7	CPU 1 OF 2-FSB	M50_HENRY	08/04/2006
8	8	CPU 2 OF 2-PWR/GND	M50_HENRY	08/04/2006
9	9	CPU DECAPS & VID<>	M51_HENRY	08/04/2006
10	10	ASIC TEMP SENSORS	M51_DAVE	(MASTER)
11	11	CPU ITP700FLEX DEBUG	M50_HENRY	08/04/2006
12	12	NB CPU Interface	M50_HENRY	08/04/2006
13	13	NB PEG / Video Interfaces	M50_HENRY	08/04/2006
14	14	NB Misc Interfaces	M50_HENRY	08/04/2006
15	15	NB DDR2 Interfaces	M50_HENRY	08/04/2006
16	16	NB Power 1	M51_HENRY	08/04/2006
17	17	NB Power 2	M51_HENRY	08/04/2006
18	18	NB Grounds	M50_HENRY	08/04/2006
19	19	NB (GM) Decoupling	M51_DAVE	(MASTER)
20	20	NB Config Straps	M50_HENRY	08/04/2006
21	21	SB: 1 OF 4	M50_DOUG	08/04/2006
22	22	SB: 2 OF 4	M51_DOUG	08/04/2006
23	23	SB: 3 OF 4	M51_DOUG	08/04/2006
24	24	SB: 4 OF 4	M50_DOUG	08/04/2006
25	25	SB:DECOUPLING	M51_DOUG	08/04/2006
26	26	SB: MISC	M50_DOUG	08/04/2006
27	27	M51 SMBus Connections	M51_DAVE	(MASTER)
28	28	DDR2 SO-DIMM Connector A	M51_HENRY	08/04/2006
29	29	DDR2 SO-DIMM Connector B	M51_HENRY	08/04/2006
30	30	Memory Active Termination	M50_HENRY	08/04/2006
31	31	Memory Vtt Supply	M50_HENRY	08/04/2006
32	33	CLOCKS	M50_HENRY	08/04/2006
33	34	CLOCKS: TERMINATIONS	M51_HENRY	08/04/2006
34	38	Disk Connectors	M51_DOUG	08/04/2006
35	41	ETHERNET CONTROLLER	M50_DOUG	08/04/2006
36	42	ETHERNET MISC	M51_DOUG	08/04/2006
37	43	ETHERNET CONNECTOR	M51_DOUG	08/04/2006

PDF	CSA	CONTENTS	MASTER	DATE
38	44	FW: 1394B-LINK/PHY	M51_DOUG	08/04/2006
39	45	FW: 1394B MISC	M51_DOUG	08/04/2006
40	46	FIREWIRE CONNECTORS	M51_DOUG	08/04/2006
41	47	USB Device Interfaces	M51_DOUG	08/04/2006
42	53	AIRPORT CONN	M51_DOUG	08/04/2006
43	54	PCI-E CONNECTIONS	M51_DOUG	08/04/2006
44	58	SMC	M51_HENRY	08/04/2006
45	59	SMC & TPM SUPPORT	M51_HENRY	07/31/2006
46	60	LPC+ CONN	M51_HENRY	08/04/2006
47	63	SPI BOOTROM	M50_DOUG	08/04/2006
48	65	HD AND OD FAN	M51_HENRY	08/04/2006
49	66	CPU FAN, HD & OD TEMP	M51_HENRY	08/04/2006
50	67	TPM	M51_HENRY	08/04/2006
51	68	AUDIO: CODEC	AUDIO	08/04/2006
52	69	AUDIO: LINE INPUT AMP	AUDIO	08/04/2006
53	70	AUDIO: COMBO OUT AMP	AUDIO	08/04/2006
54	71	AUDIO: SPEAKER AMP_1	AUDIO	08/04/2006
55	72	AUDIO: SPEAKER AMP	AUDIO	08/04/2006
56	73	AUDIO: CONNECTORS	AUDIO	08/04/2006
57	74	AUDIO: POWER SUPPLIES	AUDIO	08/04/2006
58	75	IMVP6 CPU VCore Regulator	M51_PAUL	08/04/2006
59	76	CPU & SYSTEM SENSE	M51_DAVE	(MASTER)
60	77	PWR GOOD	M51_PAUL	08/04/2006
61	78	3V DC/DC 2.5V	M51_PAUL	08/04/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	08/04/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	08/04/2006
64	82	5V DC/DC	M51_PAUL	08/04/2006
65	83	S0 AND S3 FETS	M51_PAUL	08/04/2006
66	84	MXM PCI-E & PWR	M51_DAVE	(MASTER)
67	85	MXM I/O	M51_DAVE	(MASTER)
68	94	Internal Display Conns	M51_DAVE	(MASTER)
69	97	External Display Conns	M51_DAVE	(MASTER)

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

NEW M51 630 BOMS 9/7
CURRENT: REV F 11/13
SCH: REV K

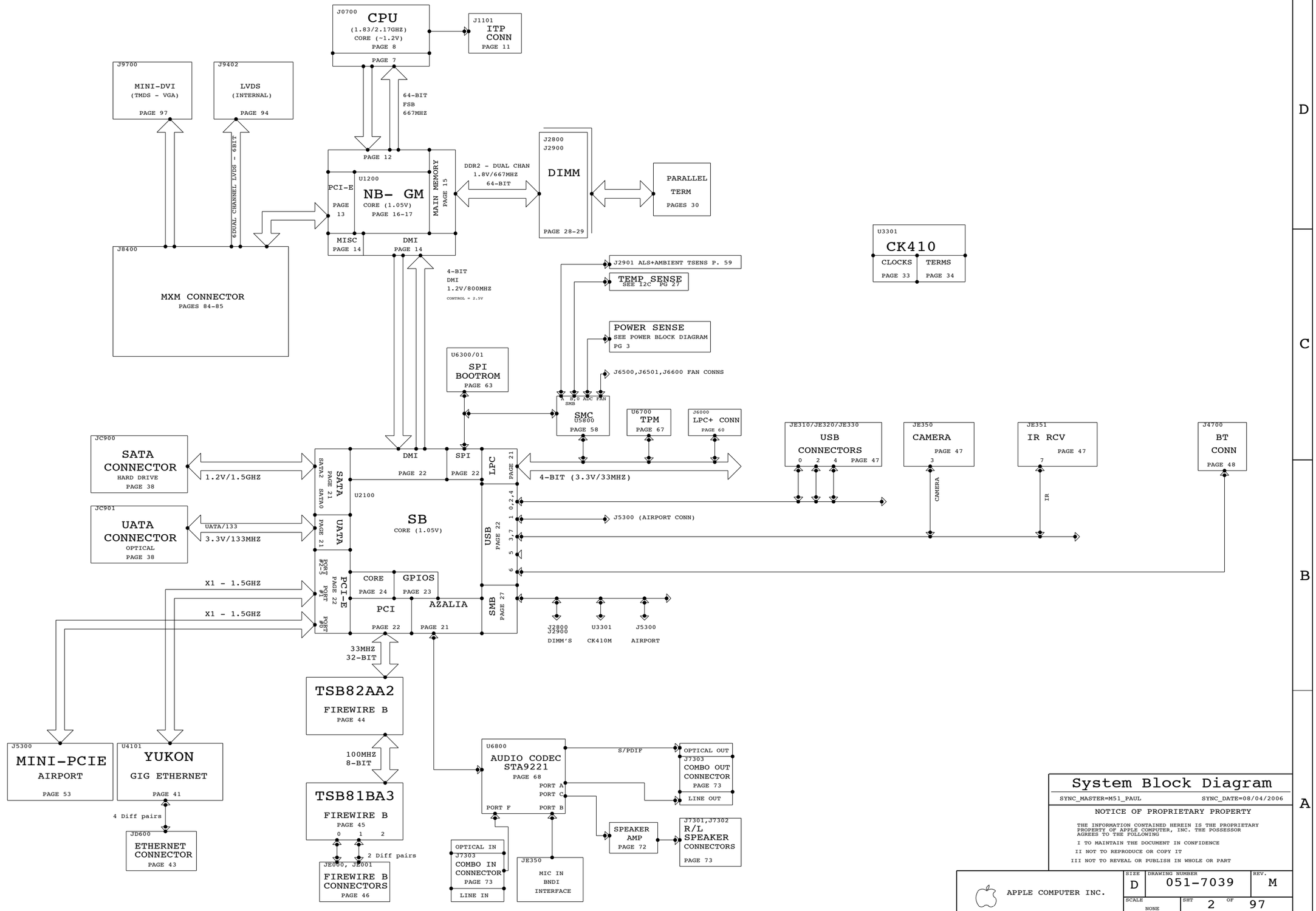
M51A REV A 11/13
M51A CANCELLED 1/16/07
NEW BOOTROM & BOMS 1/16/07

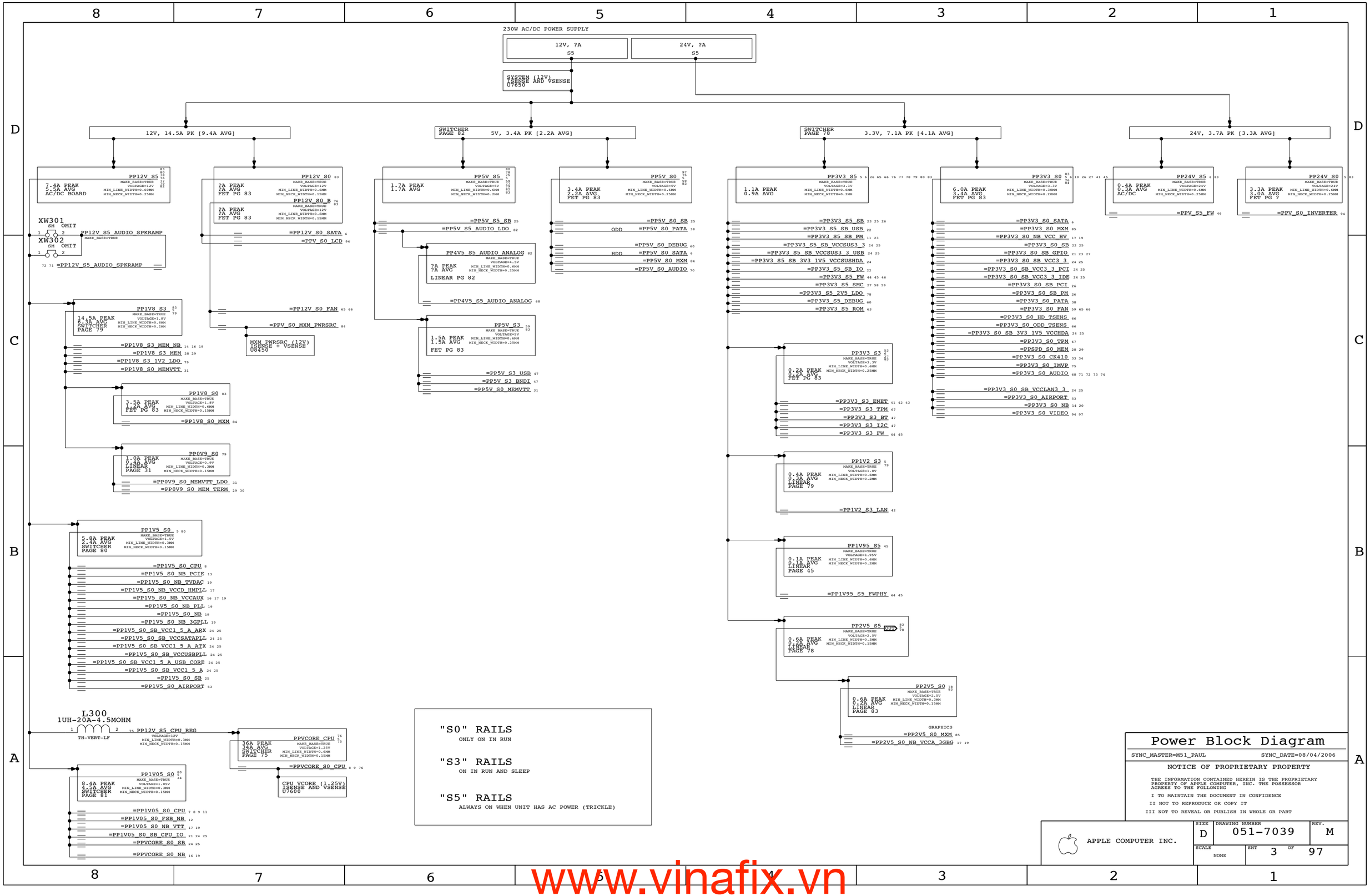
DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC
DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE: SCHEM SANTANA
DRAWING NUMBER 051-7039 REV. M
SHT 1 OF 97





Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7899	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_WZD,PRODUCTION,M51
630-7898	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_WZC,PRODUCTION,M51
630-8043	PCBA,MLB,2.33GHZ,M51,NEWROM,EEE:XCX	M51_COMMON,M51_BEST,EEE_XCX,PRODUCTION,M51A
630-8673	PCBA,MLB,2.16GHZ,M51,NEWROM,EEE:XY9	M51_COMMON,M51_BETTER,EEE_XY9,PRODUCTION,M51A

TOP TWO BOMS WERE INITIAL M51 PRODUCTION

BOTTOM TWO USED TO BE M51A, THEN M51 WAS CANCELLED
SO THESE JUST TRACK A NEW BOOT ROM

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSENS_INT,SYS_PWR_SENSE,MXM_PWR_SENSE

BarCode Label / EEE #'s

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:WZD]	CRITICAL	EEE_WZD
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:WZC]	CRITICAL	EEE_WZC
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:XCX]	CRITICAL	EEE_XCX
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:XY9]	CRITICAL	EEE_XY9

CHIPSET, ROMS, ETC.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0117	1	IC,SLG84435,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(33S80382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM
(33S80384)	341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	M51
341T0060	1	IC,EFI BOOT ROM,M51A	U6301	CRITICAL	M51A
(33S80274)	341T0020	1	IC,SMC,M51	U5800	CRITICAL	

PROCESSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3392	1	MEROM 2.33GHZ, M51	CPU	CRITICAL	M51_BEST
337S3390	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)
138S0567	138S0516		ALL	CAP CONSOLIDATION
376S0388	376S0444		ALL	ON SEMI 2ND SRC FOR IR
138S0608	138S0576		ALL	2ND SRC FOR SUPPLY

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8458	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8459	PRODUCTION

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M

SCALE NONE SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 OMIT P4MM

34 22 PCI_CLK_SB PP6D0 OMIT P4MM
44 34 PCI_CLK_FW PP626 OMIT P4MM
58 34 PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 OMIT P4MM
38 21 IDE_PDIORDY PP6C7 OMIT P4MM
38 21 IDE_PDD<9> PP6C8 OMIT P4MM

54 22 PCIE_B_D2R_P PP600 OMIT P4MM
54 22 PCIE_B_D2R_N PP601 OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 OMIT P4MM
63 58 22 SPI_SO PP612 OMIT P4MM
63 58 22 SPI_SI PP613 OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 OMIT P4MM
27 SMBUS_SB_SDA PP605 OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 OMIT P4MM
14 NB_RST_IN_L_R PP666 OMIT P4MM

22 14 DMI_S2N_N<0> PP673 OMIT P4MM
22 14 DMI_S2N_P<0> PP674 OMIT P4MM
19 14 MEM_VREF_NB_0 PP6E1 OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 OMIT P4MM

I473
14 NB_CFG<17> — I474 — NC_NB_CFG<17> MAKE_BASE=TRUE
14 NB_CFG<15> — I475 — NC_NB_CFG<15> MAKE_BASE=TRUE
14 NB_CFG<14> — I476 — NC_NB_CFG<14> MAKE_BASE=TRUE
14 NB_CFG<13> — I477 — NC_NB_CFG<13> MAKE_BASE=TRUE
14 NB_CFG<12> — I478 — NC_NB_CFG<12> MAKE_BASE=TRUE
14 NB_CFG<11> — I479 — NC_NB_CFG<11> MAKE_BASE=TRUE
14 NB_CFG<10> — I481 — NC_NB_CFG<10> MAKE_BASE=TRUE
14 NB_CFG<8> — I480 — NC_NB_CFG<8> MAKE_BASE=TRUE
14 NB_CFG<6> — I482 — NC_NB_CFG<6> MAKE_BASE=TRUE
14 NB_CFG<4> — I483 — NC_NB_CFG<4> MAKE_BASE=TRUE
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

I513
22 PCI_GNT3_L — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN 19 MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 78 3 IN PP2V5_S5 FUNC_TEST=TRUE
83 79 3 IN PP1V8_S3 FUNC_TEST=TRUE
79 3 IN PP1V2_S3 FUNC_TEST=TRUE
80 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 34 3 IN PP1V05_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
84 83 76 45 41 27 26 10 6 3 IN PP3V3_S0 FUNC_TEST=TRUE
83 3 IN PP24V_S0 FUNC_TEST=TRUE

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 59 21 IN FWH_INIT_L FUNC_TEST=TRUE
60 34 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
67 60 58 23 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
60 58 IN SMC_MD1 FUNC_TEST=TRUE
60 59 58 IN SMC_RST_L FUNC_TEST=TRUE
60 58 IN SMC_NMI FUNC_TEST=TRUE
60 23 IN SV_SET_UP FUNC_TEST=TRUE
76 58 IN ISENSE_CAL_EN FUNC_TEST=TRUE
94 85 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 IN LCD_PWM FUNC_TEST=TRUE
75 8 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
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11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA 1
ZH510 HOLE-VIA 1
ZH520 HOLE-VIA 1
ZH501 HOLE-VIA 1
ZH511 HOLE-VIA 1
ZH521 HOLE-VIA 1
ZH502 HOLE-VIA 1
ZH512 HOLE-VIA 1
ZH522 HOLE-VIA 1
ZH503 HOLE-VIA 1
ZH513 HOLE-VIA 1
ZH523 HOLE-VIA 1
ZH504 HOLE-VIA 1
ZH514 HOLE-VIA 1
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ZH527 HOLE-VIA 1
ZH508 HOLE-VIA 1
ZH518 HOLE-VIA 1
ZH528 HOLE-VIA 1
ZH509 HOLE-VIA 1
ZH519 HOLE-VIA 1
ZH529 HOLE-VIA 1

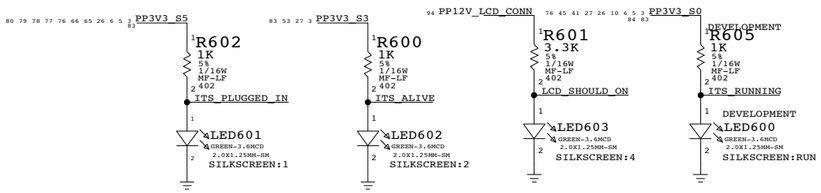
FUNC TEST 1 OF 2

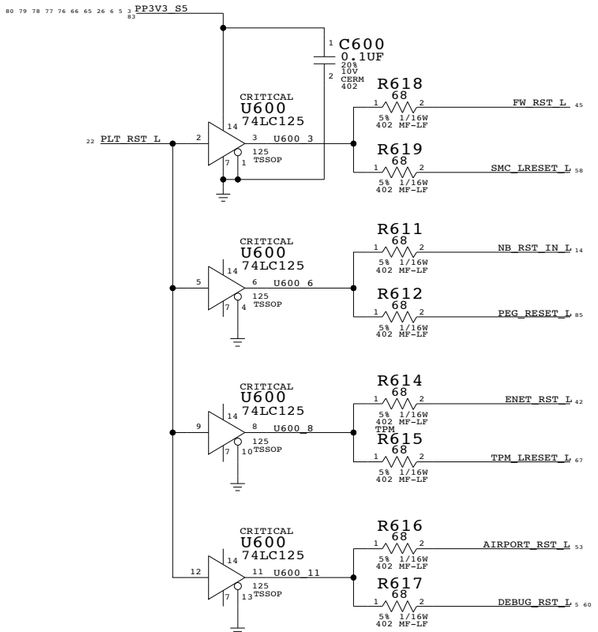
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

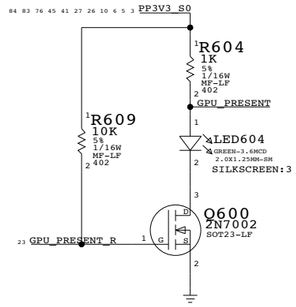
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 5 OF 97	

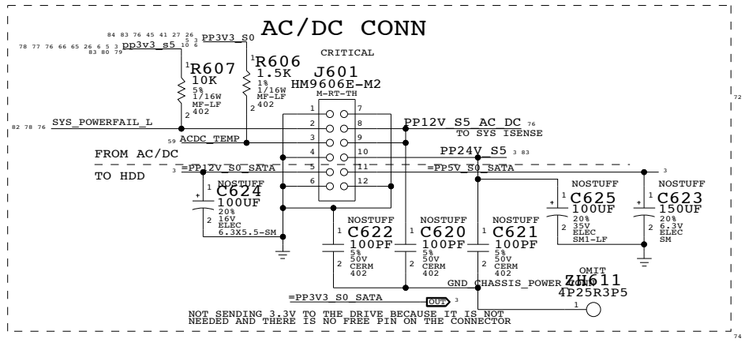
SYSTEM STATUS



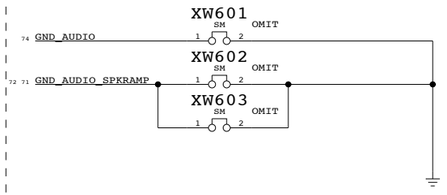




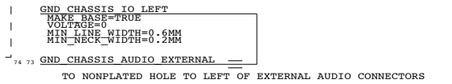
AC/DC CONN

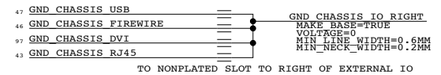


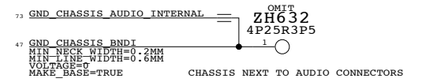
GND RAILS

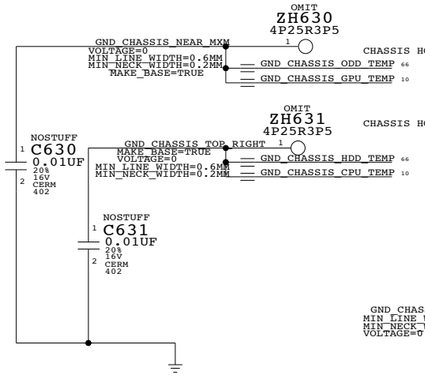


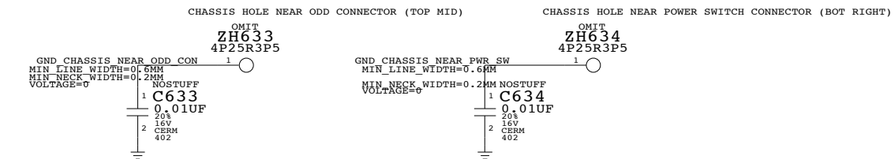
CHASSIS GND





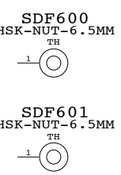






HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU

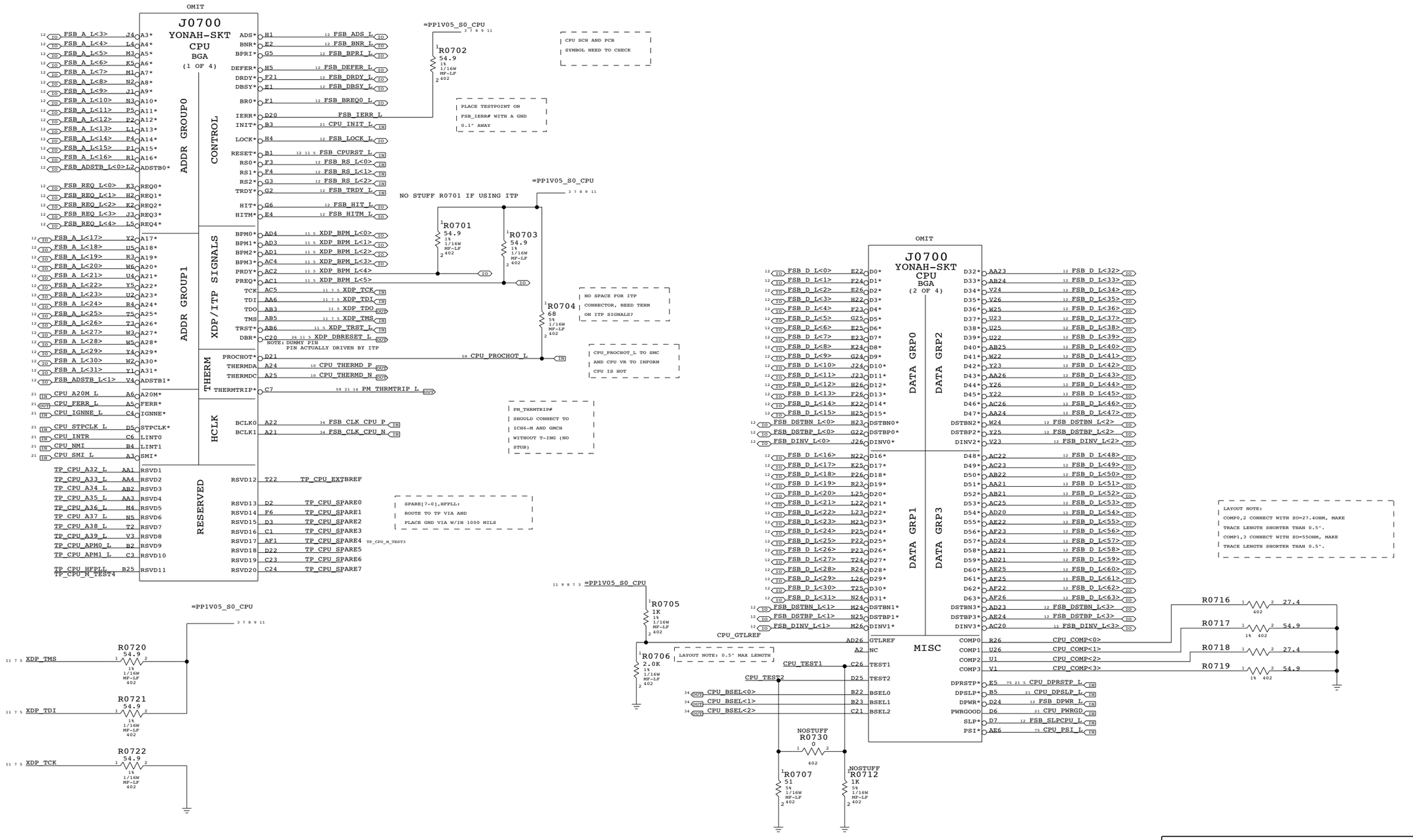


POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 6 OF 97	

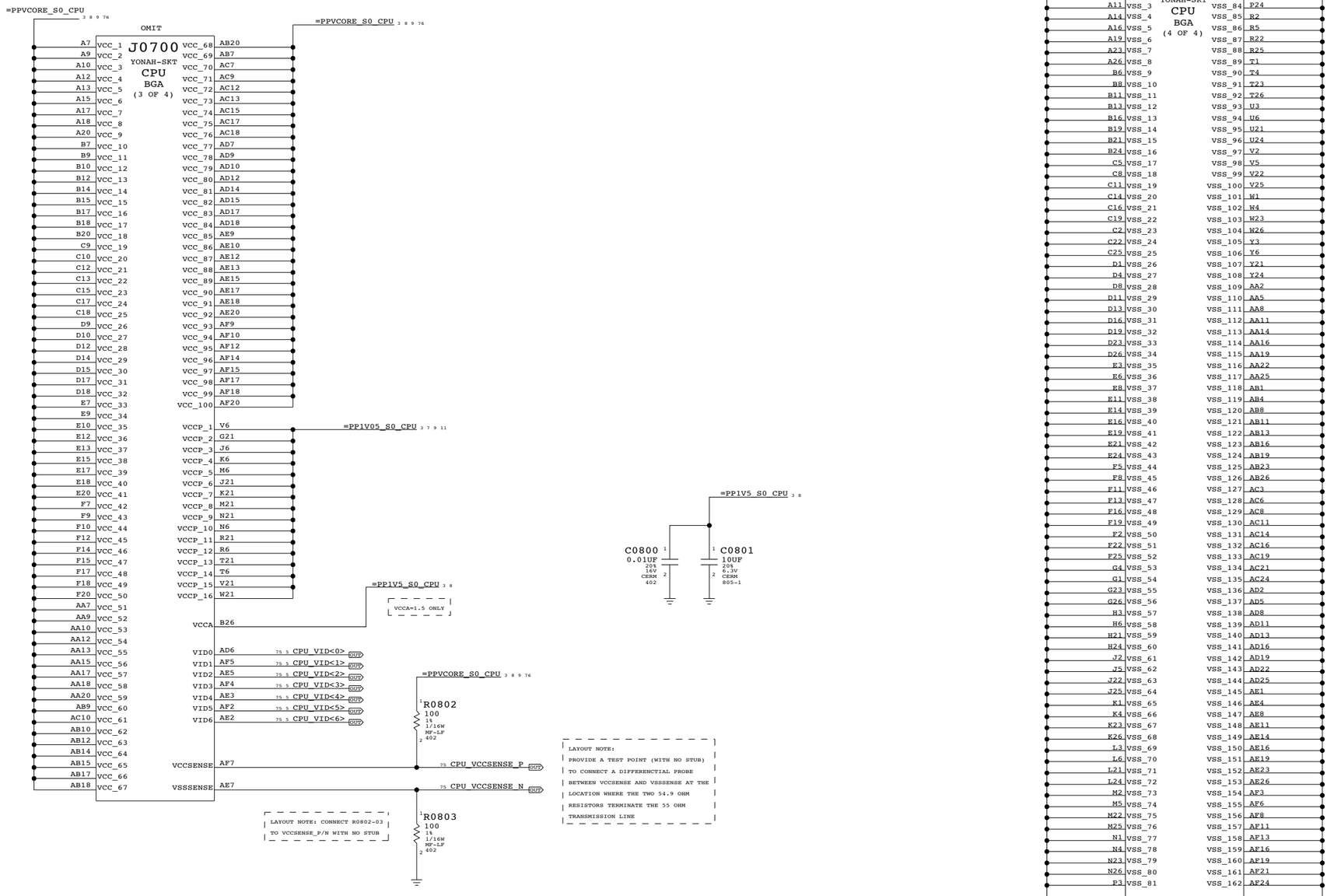


CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 7 OF 97	



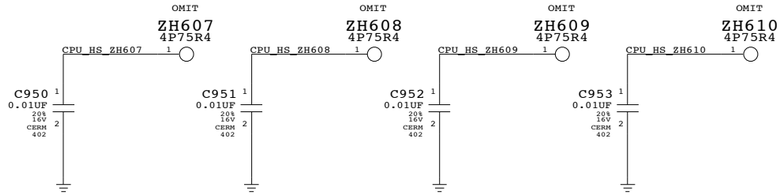
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

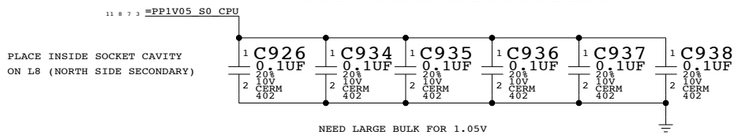
SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 8 OF 97	

CPU HEATSINK MOUNTING HOLES

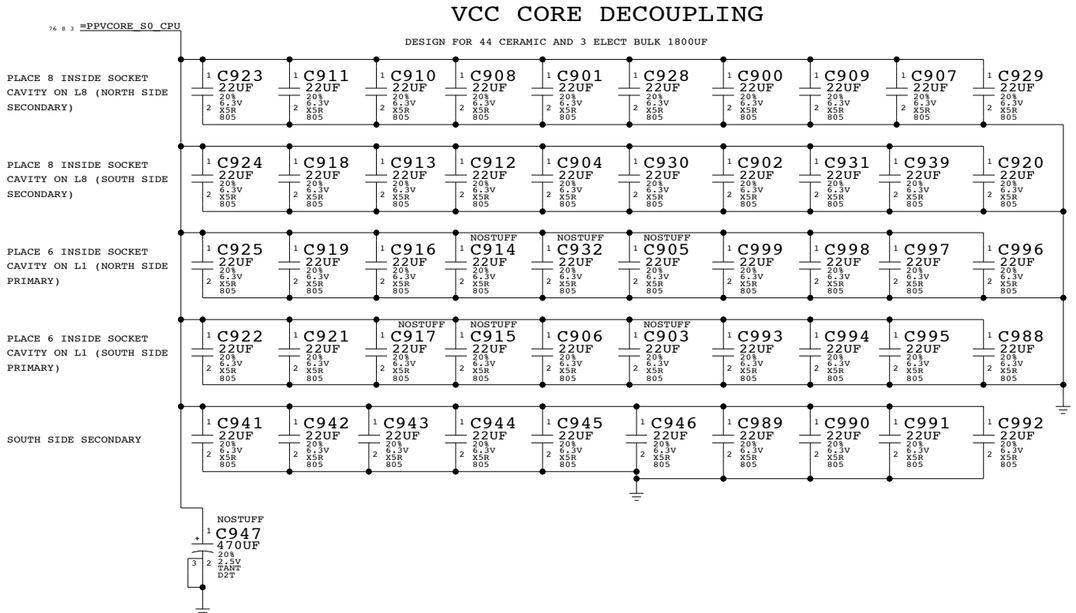


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

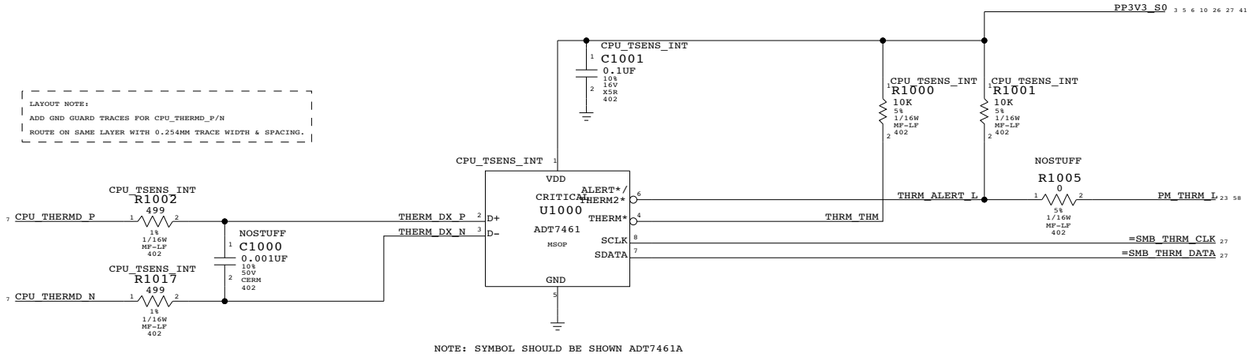
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 9 OF 97	

CPU INTERNAL DIODE THERMAL SENSOR

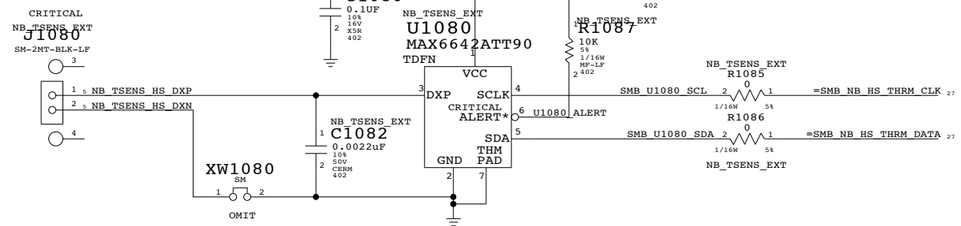
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



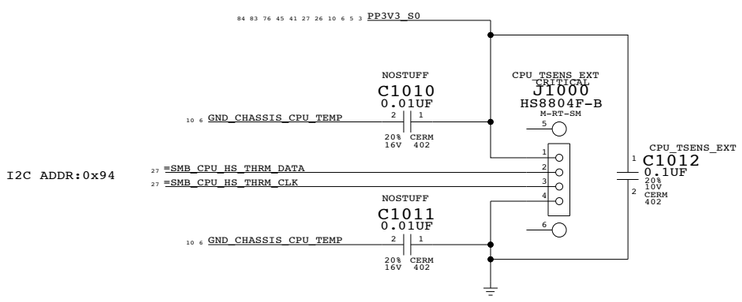
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

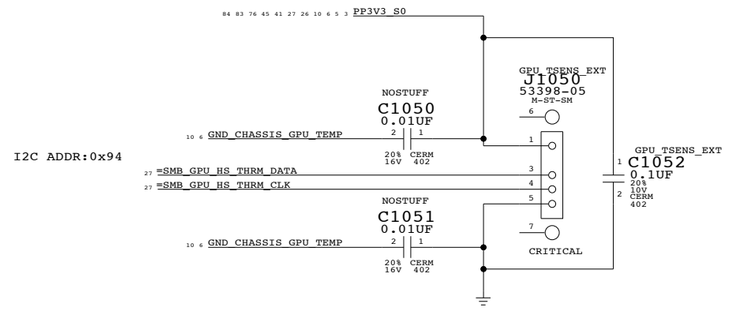
NB HEATSINK TEMPERATURE SENSE



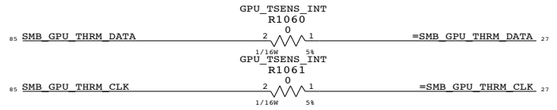
I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS



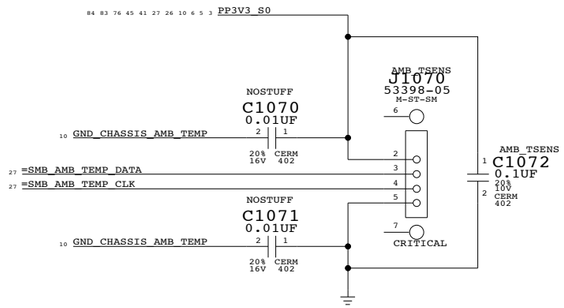


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



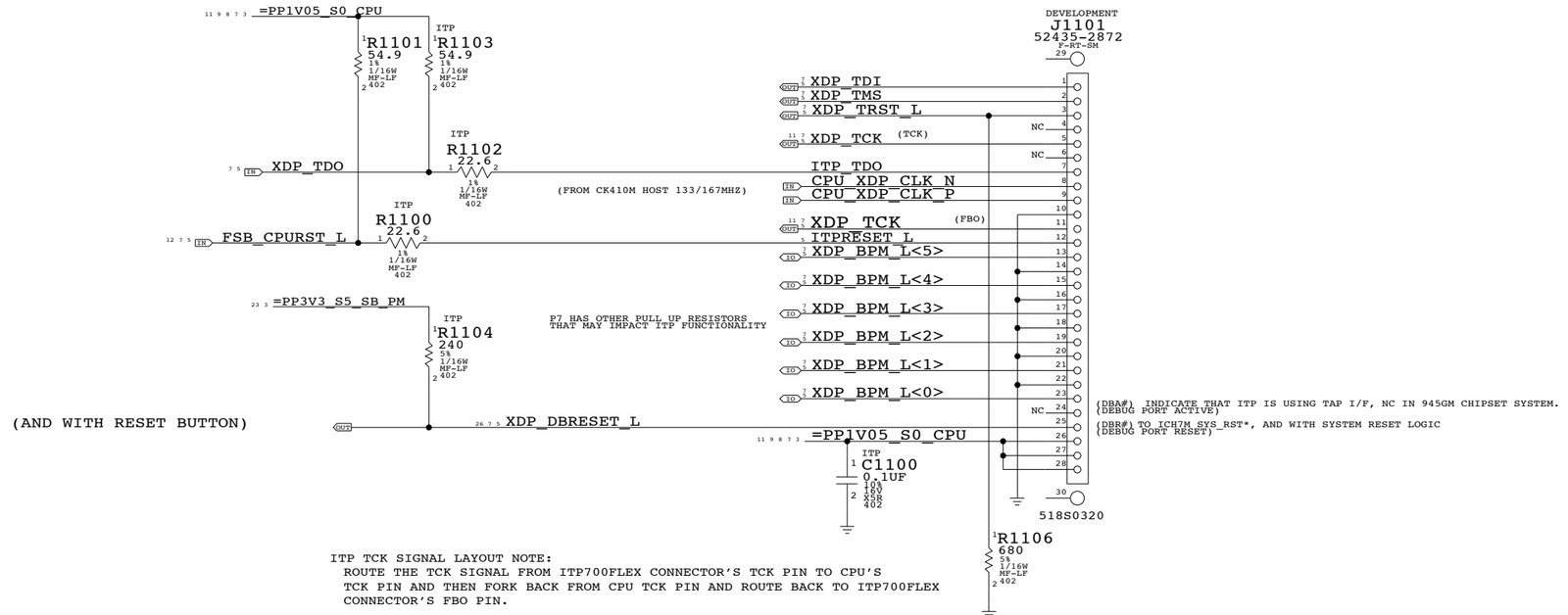
ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 10 OF 97	

CPU ITP700FLEX DEBUG SUPPORT



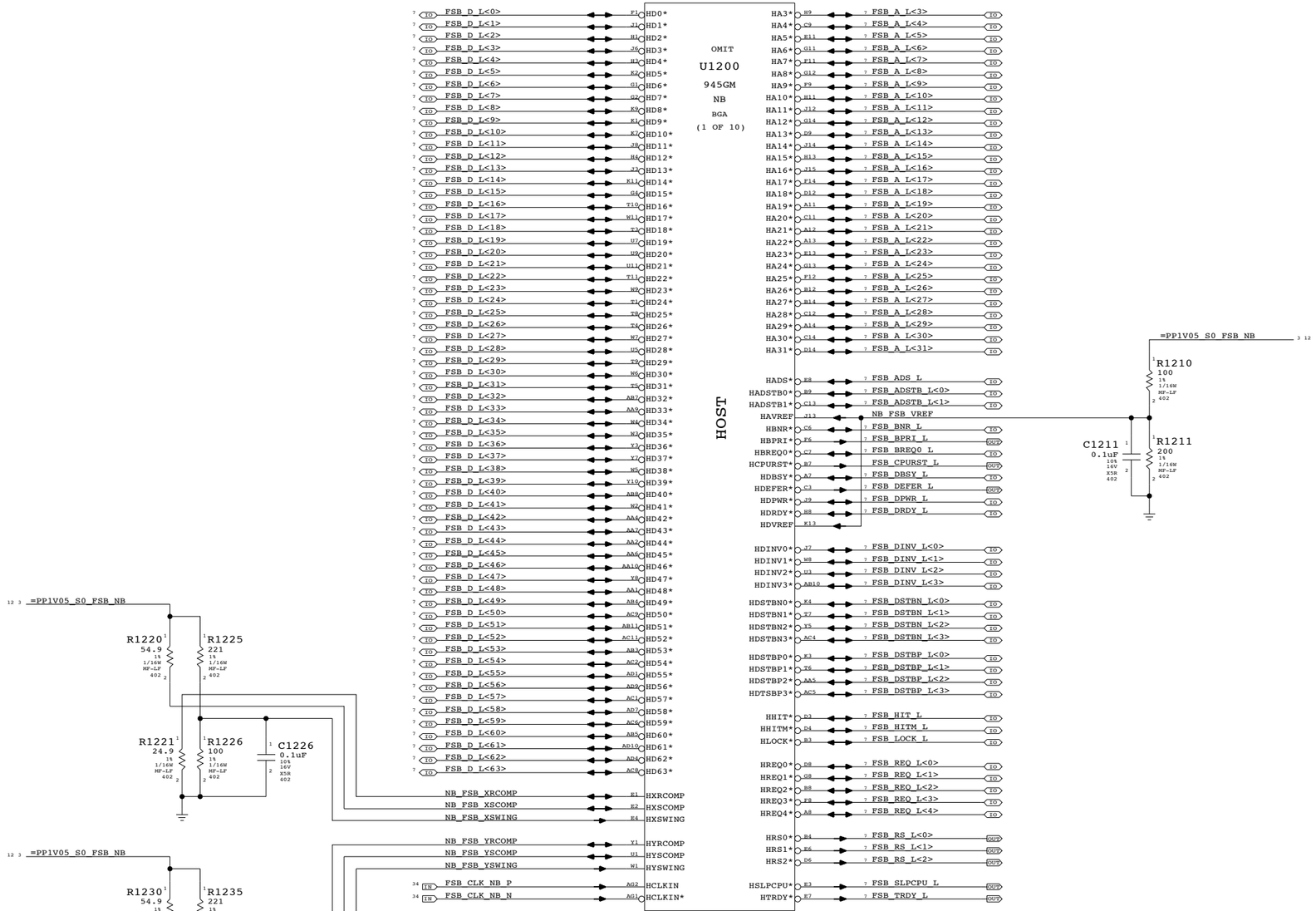
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 11 OF 97	



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 12 OF 97	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

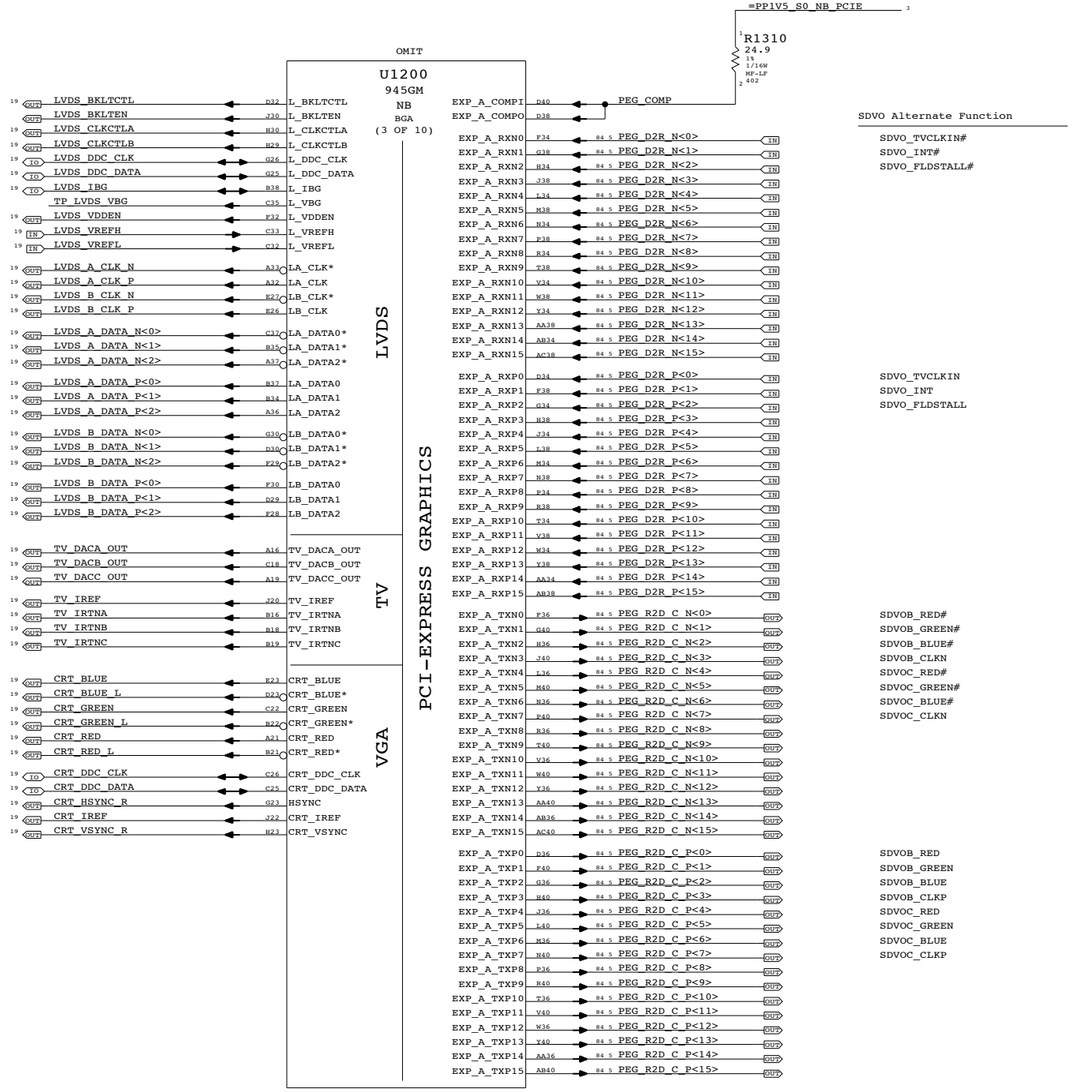
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

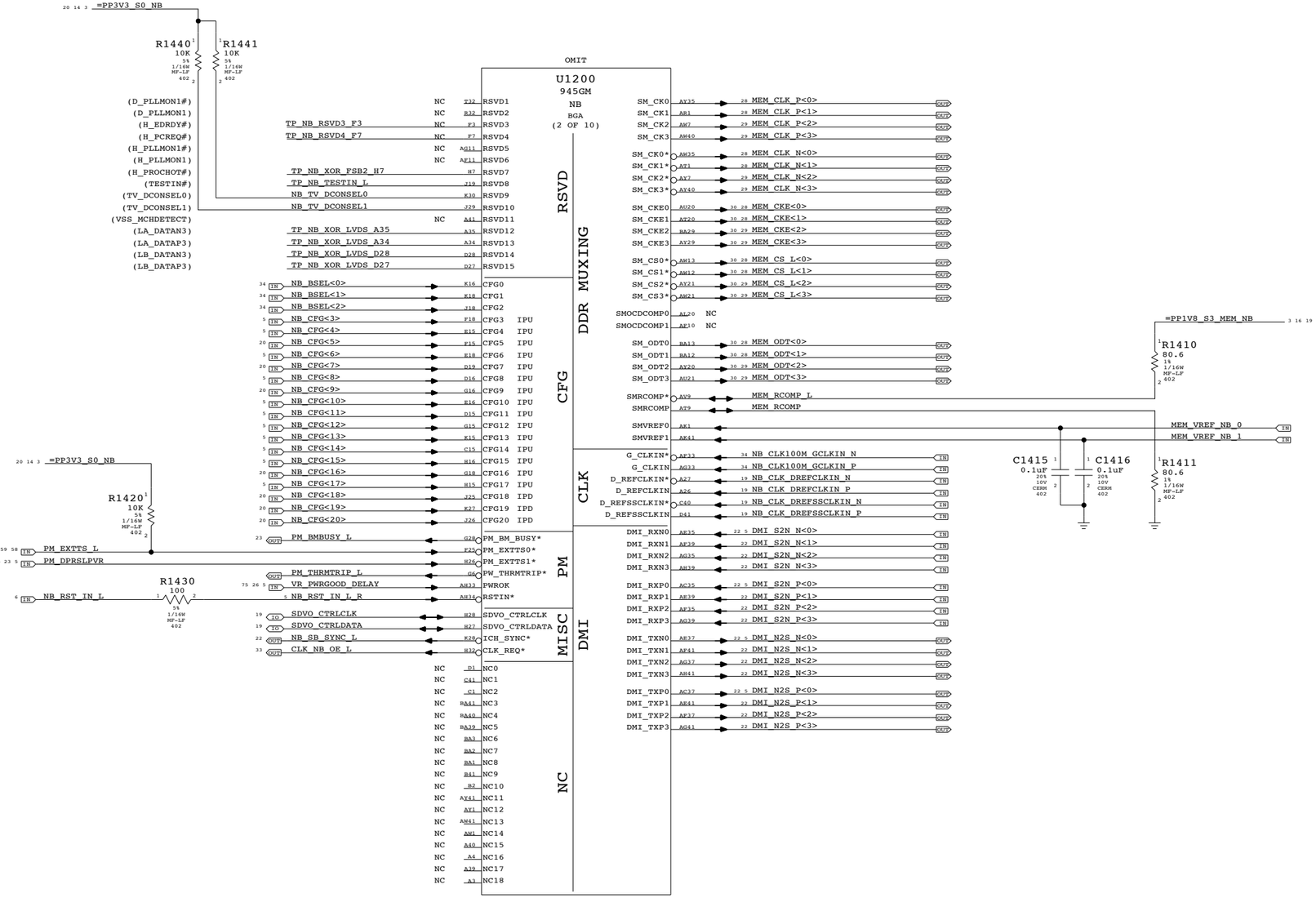


NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 13 OF 97	

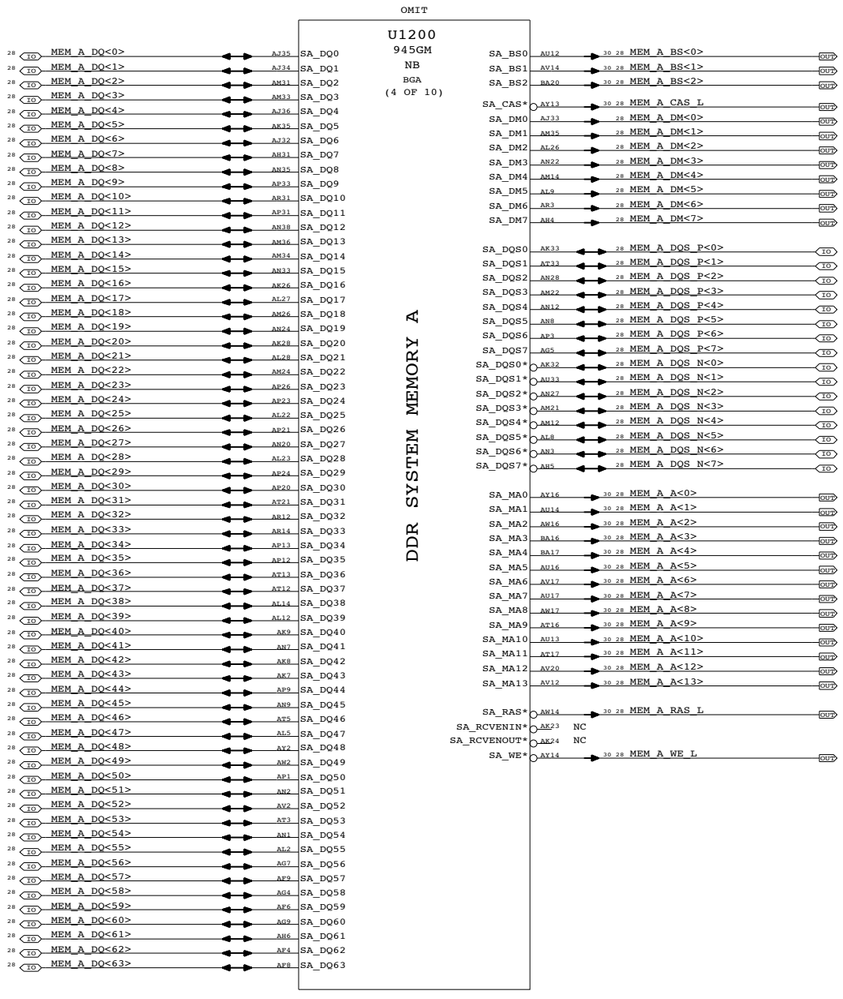


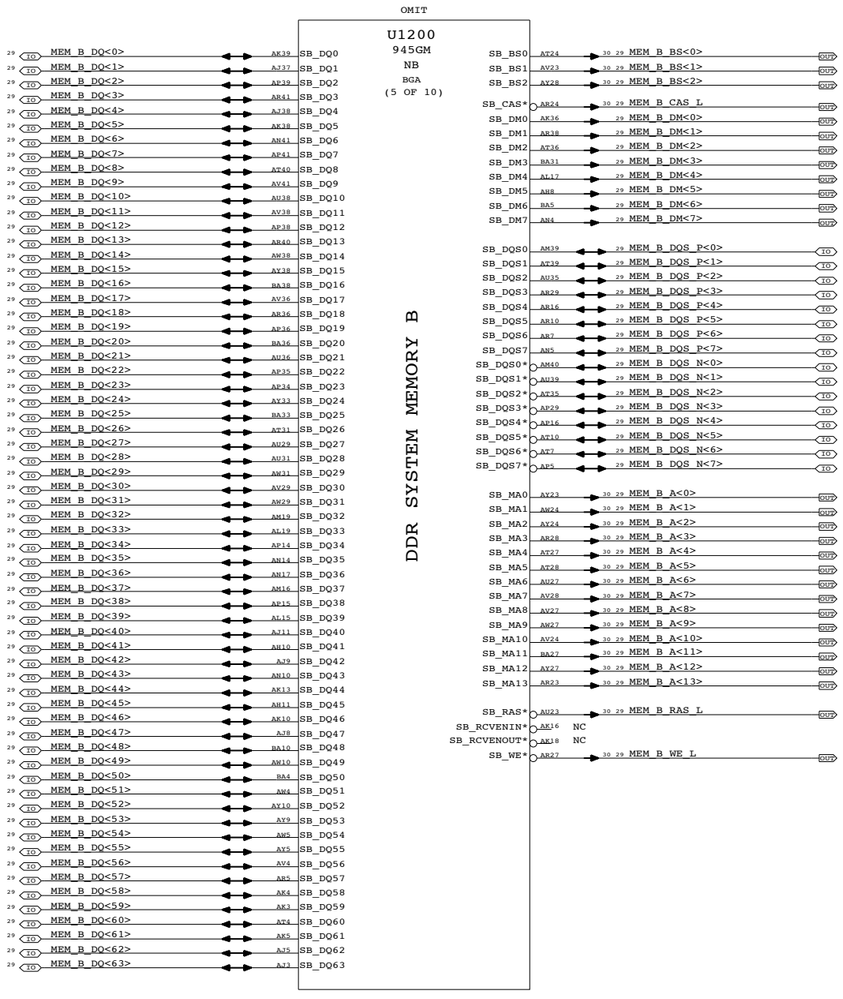
NB Misc Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 14 OF 97	



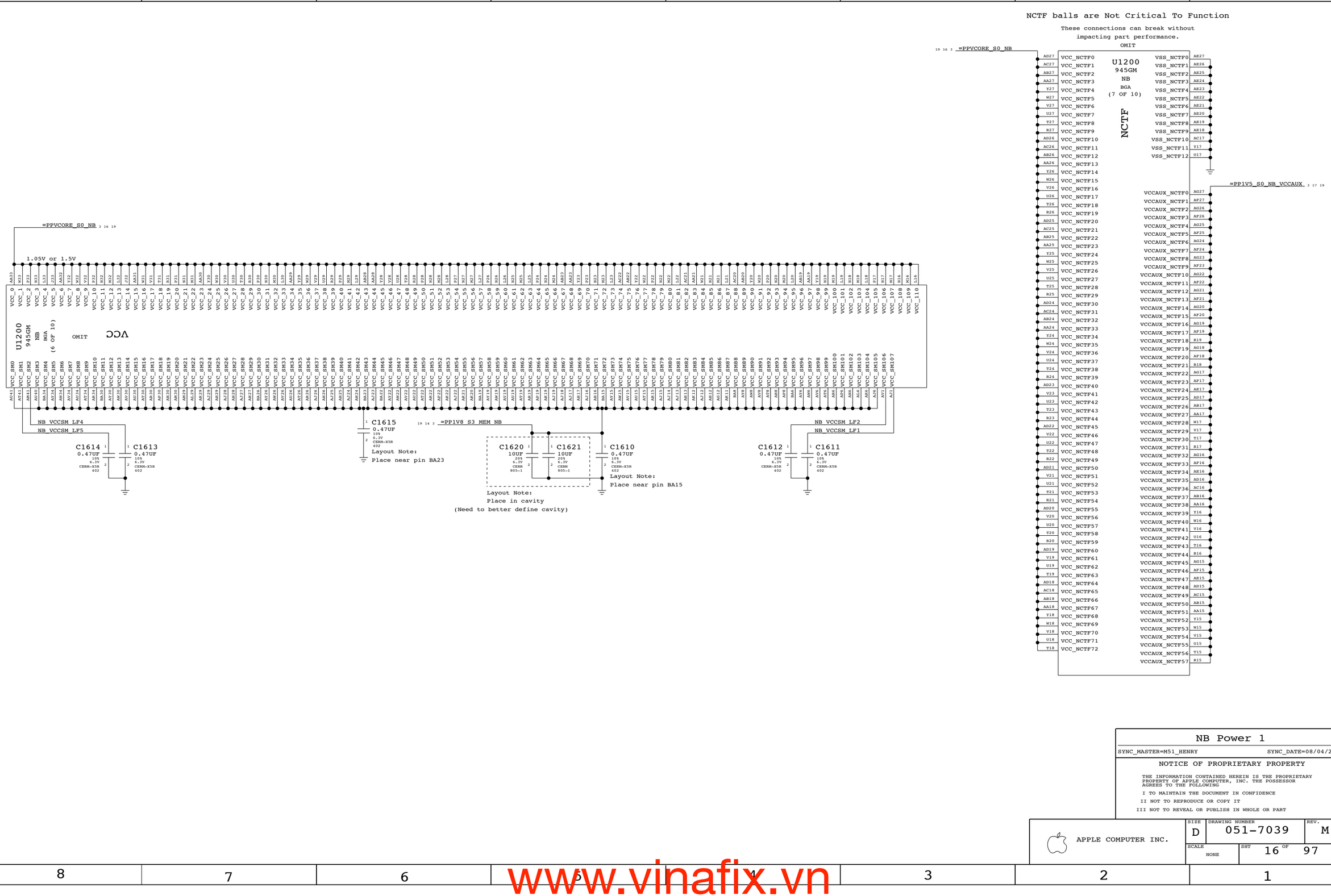


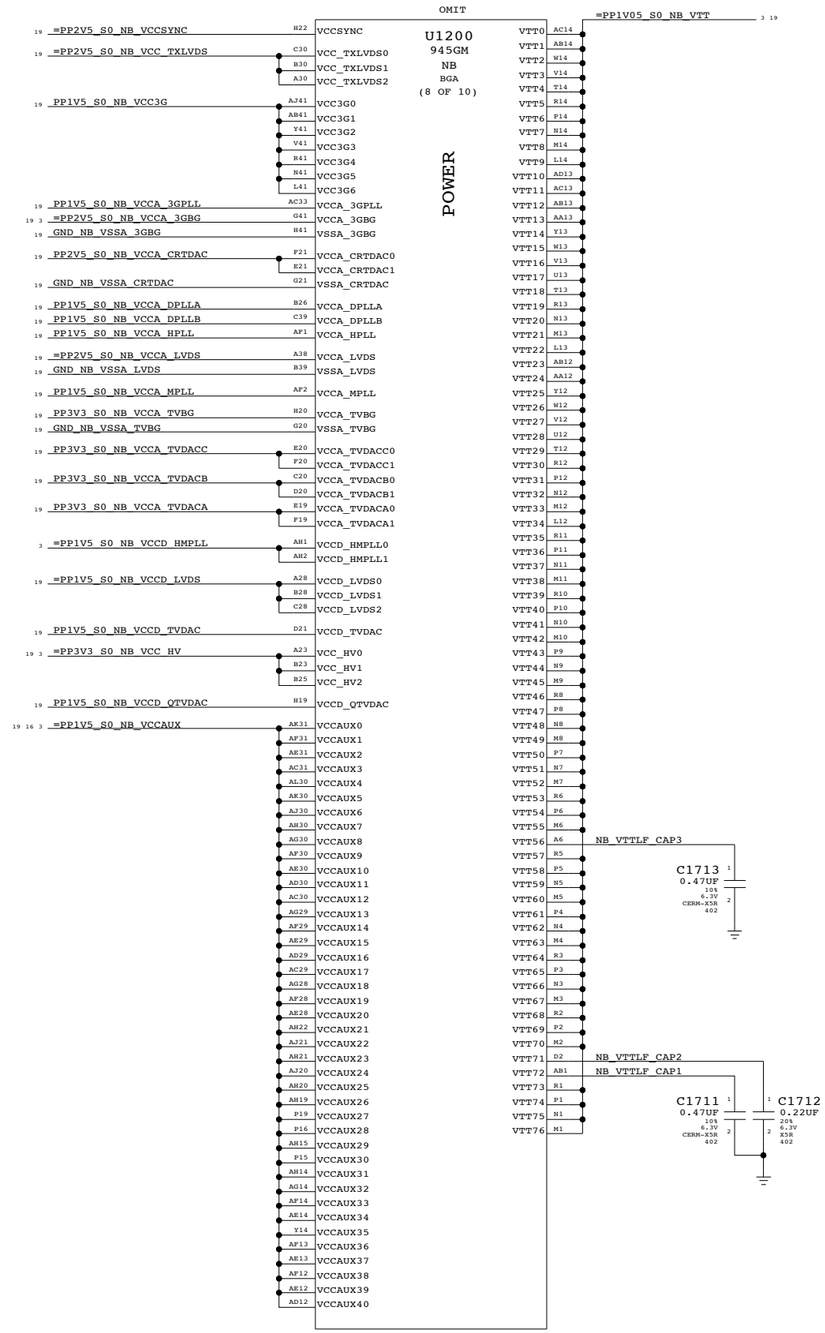
NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 15 OF 97	



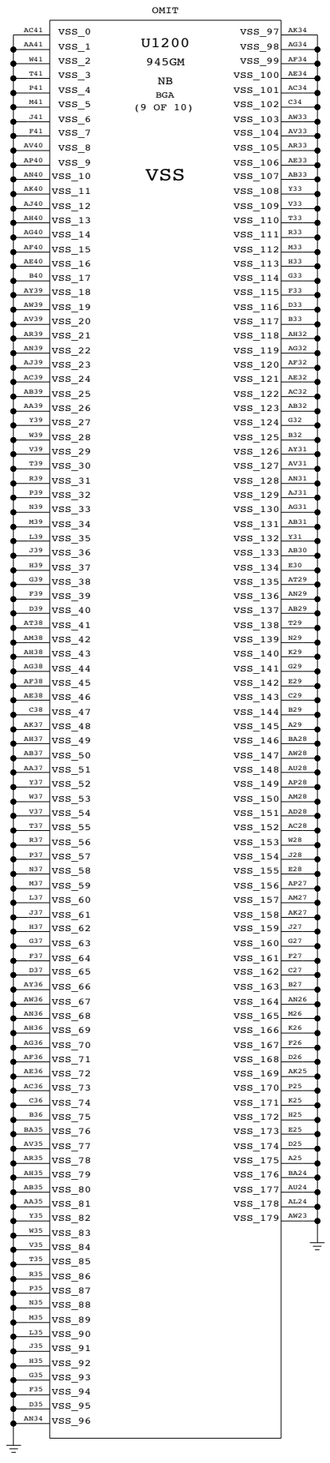


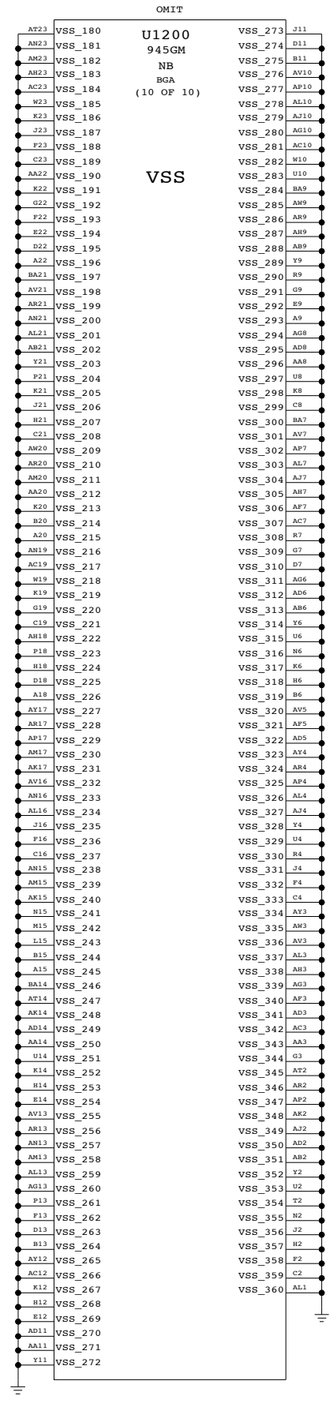
SYNC_MASTER=M51_HENRY	SYNC_DATE=08/04/2006

NB Power 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 17 OF 97	





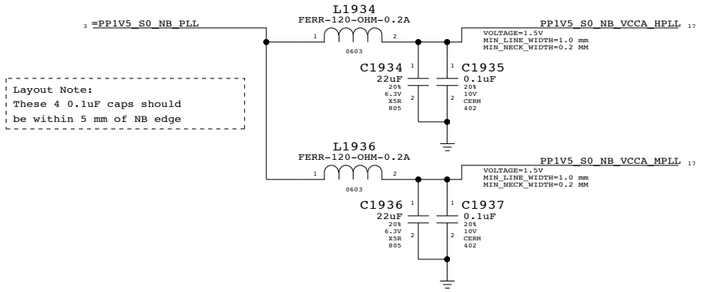
NB Grounds

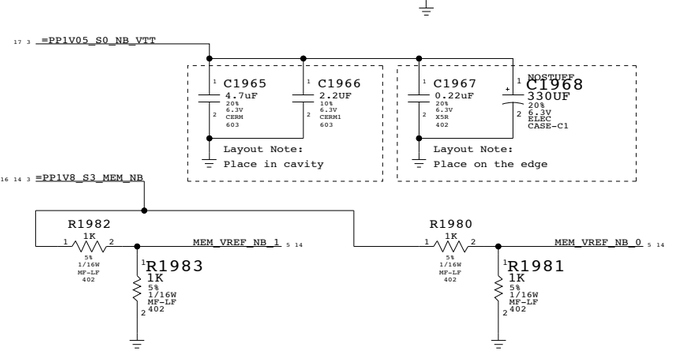
SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

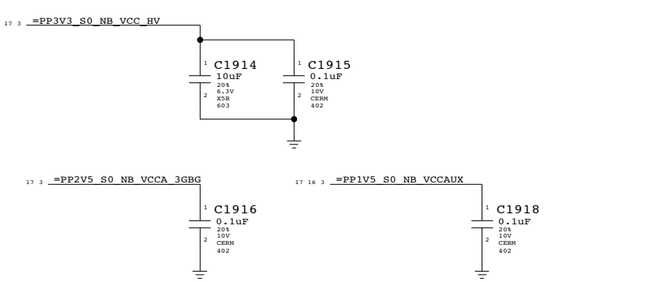
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M

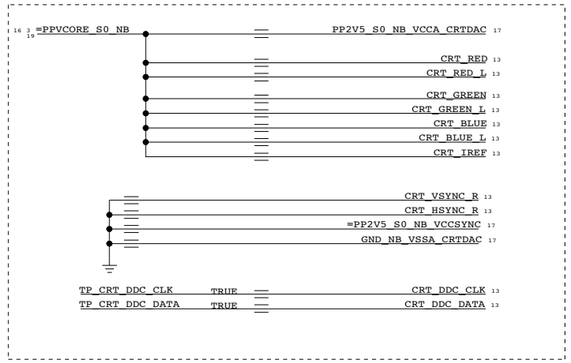
SCALE NONE SHT 18 OF 97



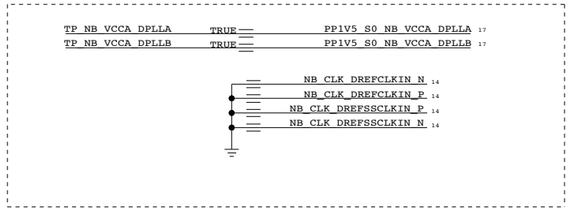


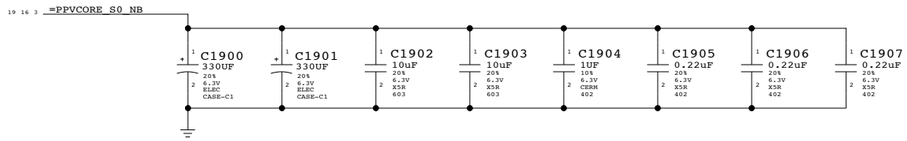


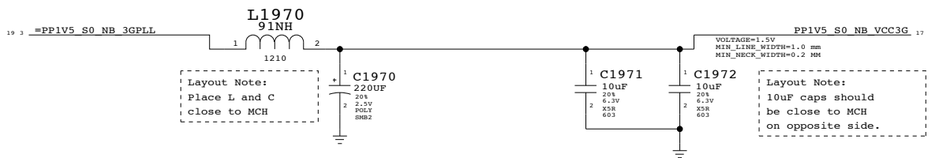
TVOUT DISABLE

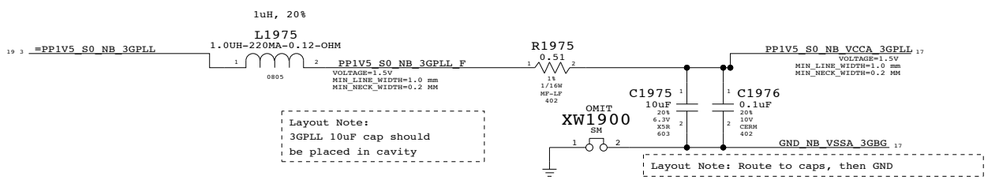


DISPLAY DISABLE









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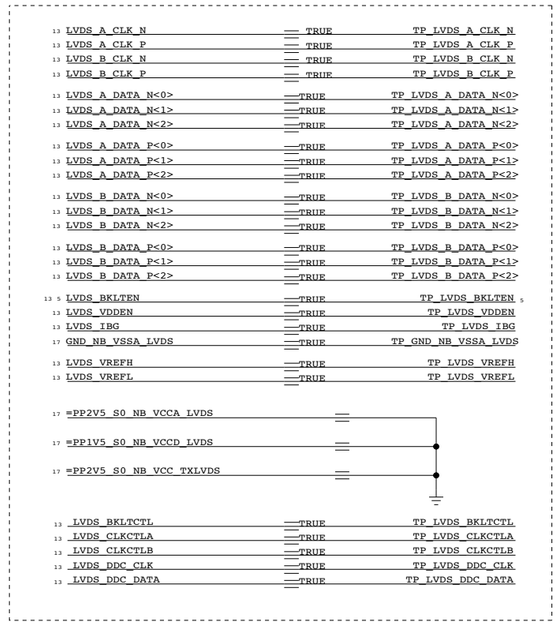

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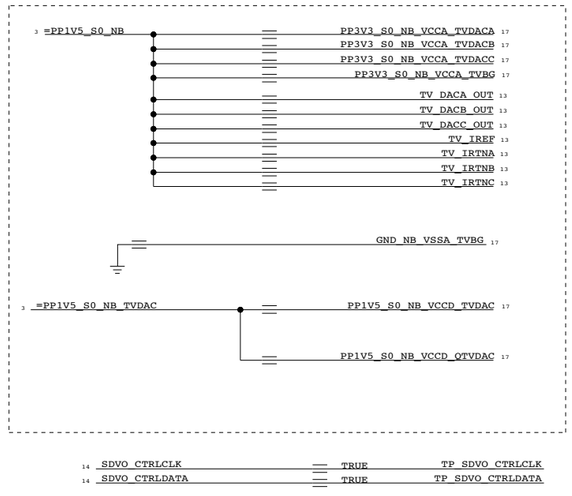

14 SDVO_CTRLCLK TRUE TP_SDVO_CTRLCLK
14 SDVO_CTRLDATA TRUE TP_SDVO_CTRLDATA

NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075 2.2K 5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077 2.2K 5% 1/16W MF-LF 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079 2.2K 5% 1/16W MF-LF 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085 2.2K 5% 1/16W MF-LF 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058 2.2K 5% 1/16W MF-LF 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059 2.2K 5% 1/16W MF-LF 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060 2.2K 5% 1/16W MF-LF 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

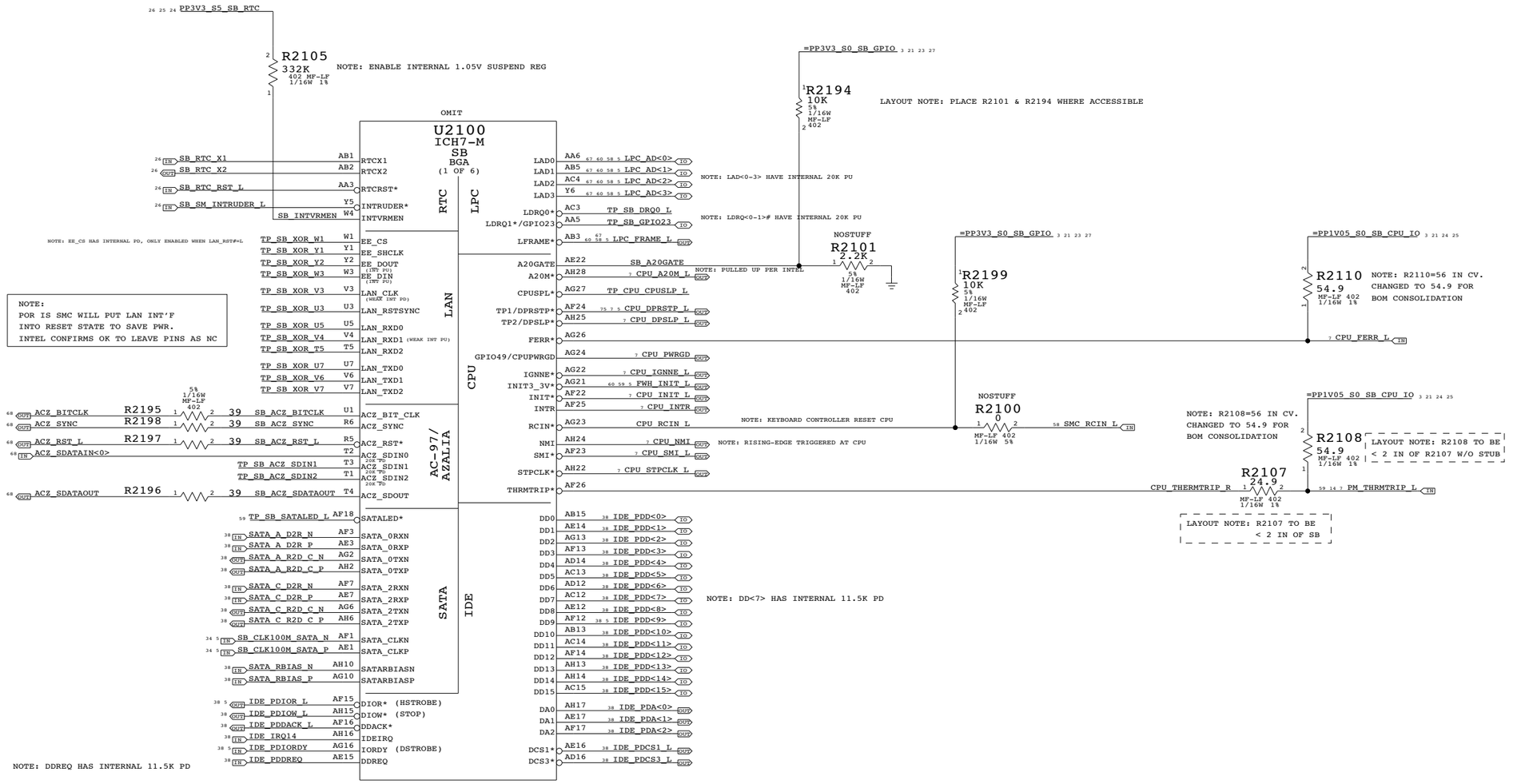
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 20 OF 97	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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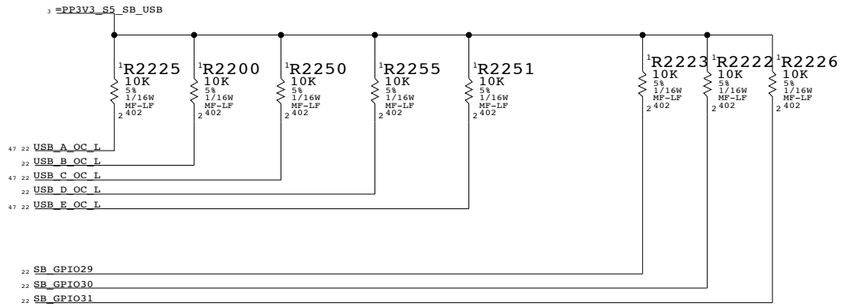
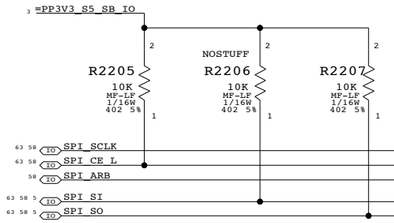
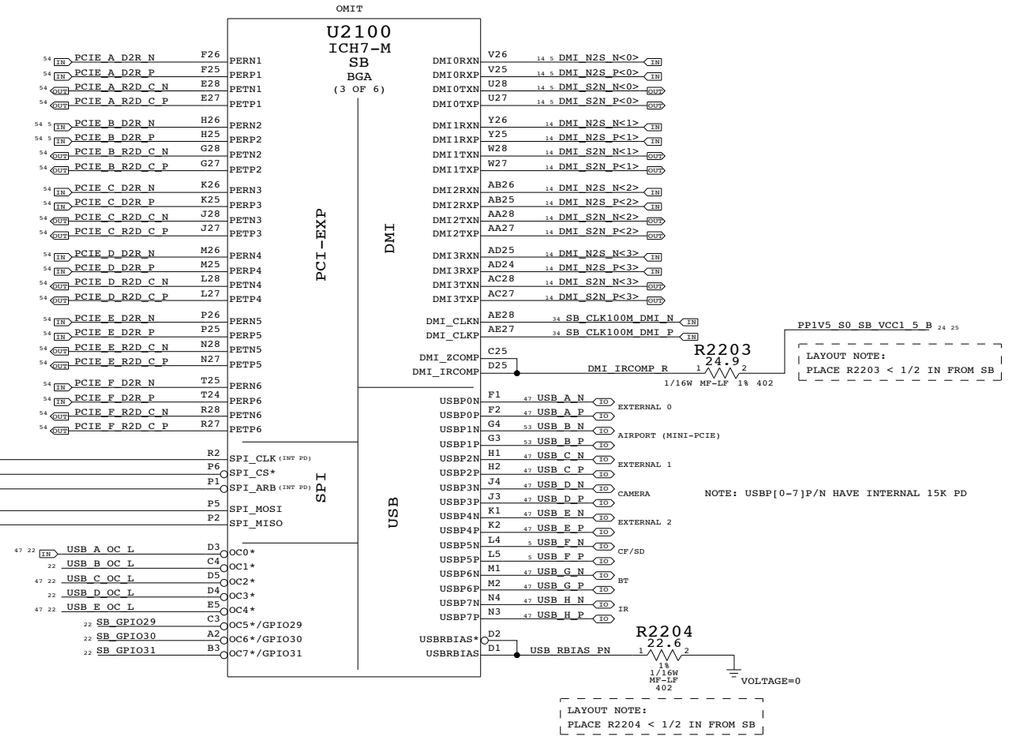
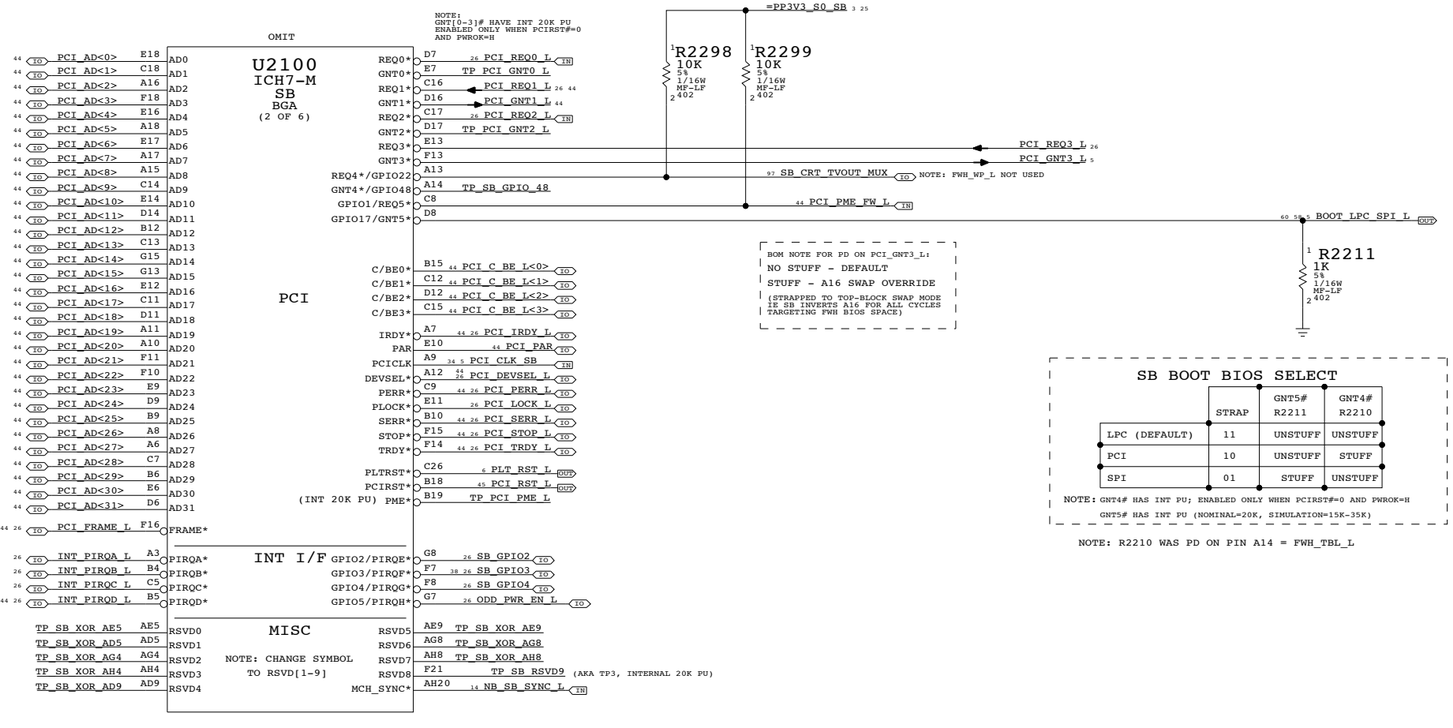
SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 21 OF 97	









	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

SB: 2 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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D	051-7039	M
SCALE: NONE	SHT 22 OF 97	

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

26 25 23 3 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

27 TO SMB_CLK — C22 SMBCLK
27 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 5 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 IN PM_SYSRST_L — A22 SYS_RST*
14 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
34 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 5 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 5 TO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THRM*
26 5 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
6 GPU_PRESENT_R — AC21 GPIO6
58 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
58 IN SMC_EXTSMI_L — E21 GPIO8

SMB

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS
CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 50 SUS_CLK_SB OUT

SYS GPIO / PWR MNGT
SLP_S3* — B24 — 79 77 80 5 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 5 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 — 75 14 5 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO
GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 5 23 60
GPIO24 — R3 — TP_SB_GPIO24
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 23 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 3 11

R2387 10K 1/16W 402 MF-LF 5% NOSTUFF
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
58 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

26 25 23 3 =PP3V3_S5_SB

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5% NOSTUFF
R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 60
EFI_OK_R

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 3 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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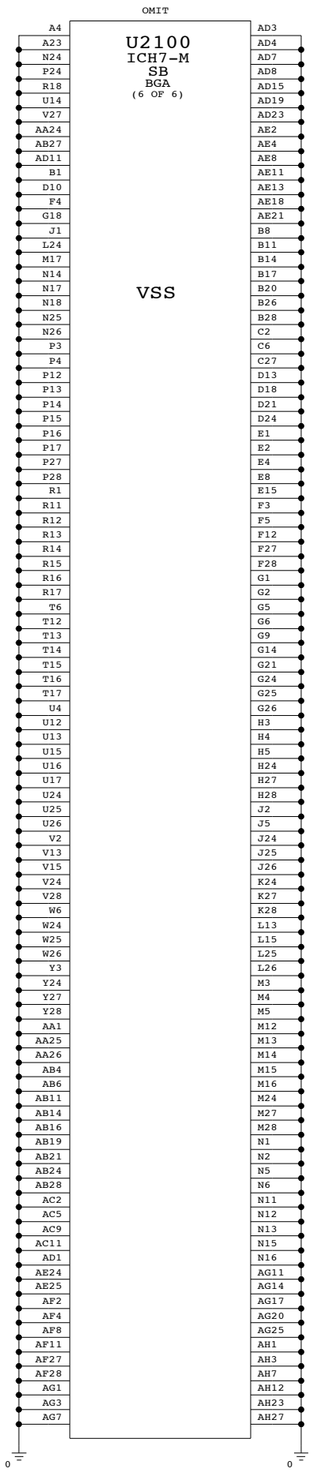
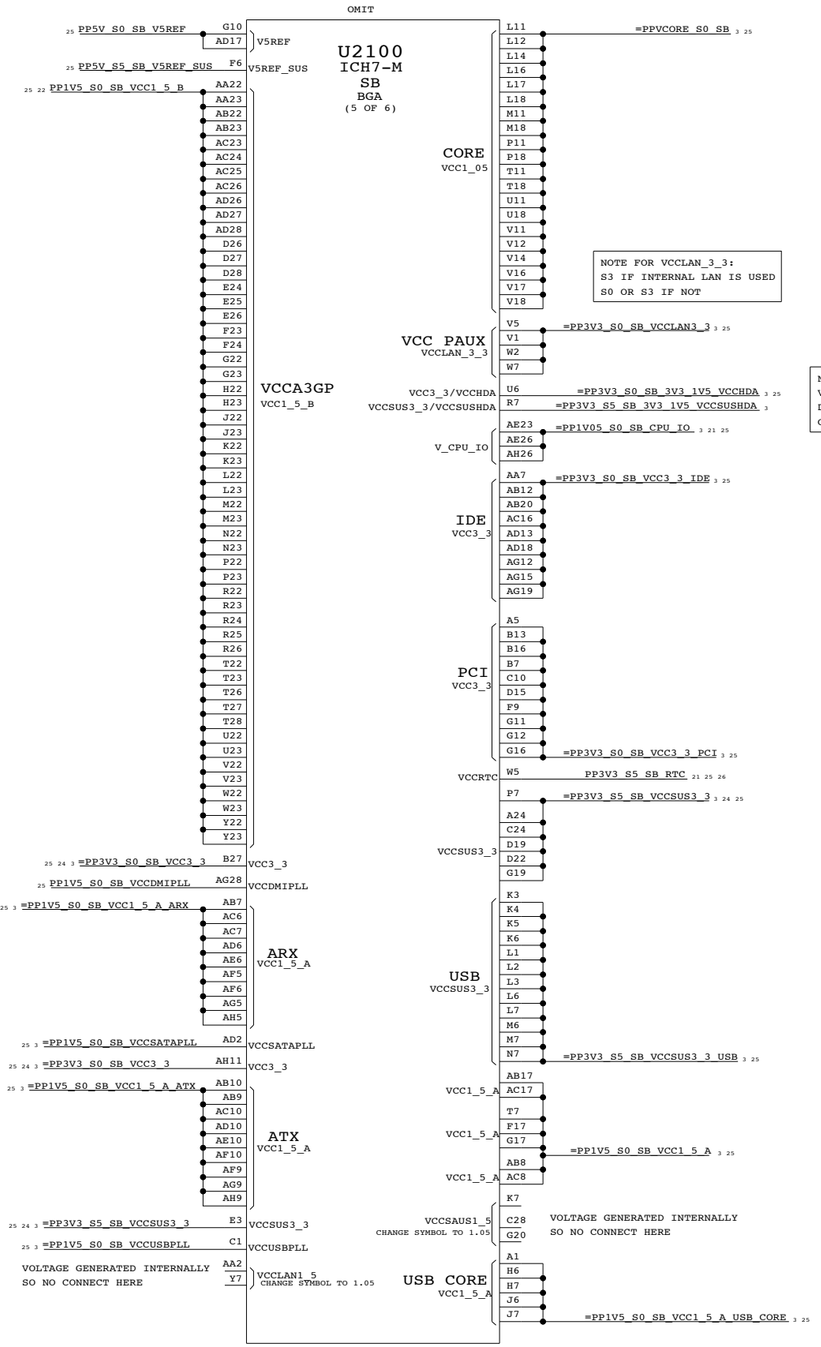
SCALE: NONE	SHT 23 OF 97	





SB: 4 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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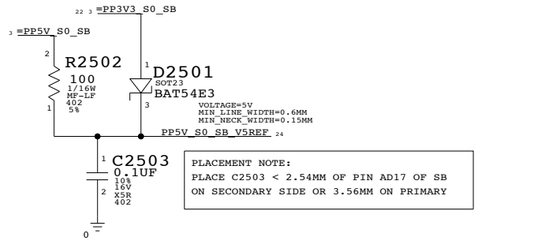
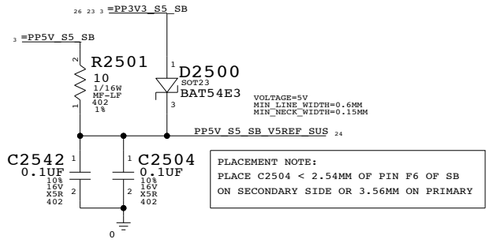
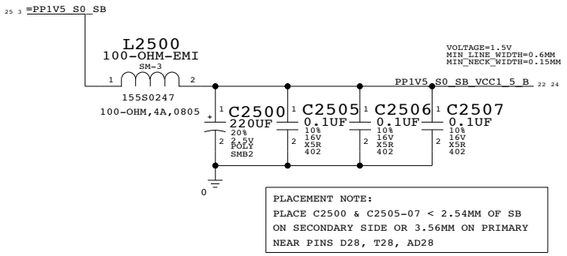
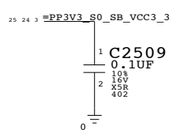
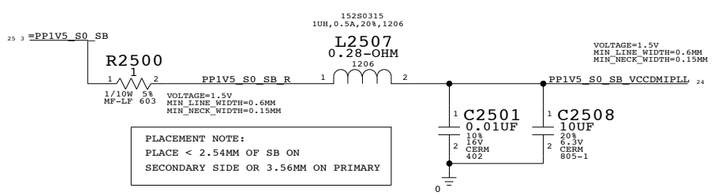
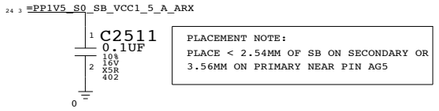


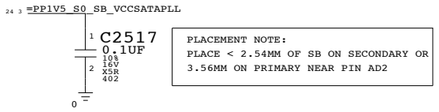


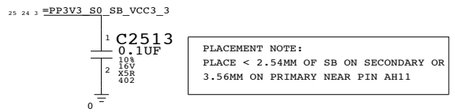


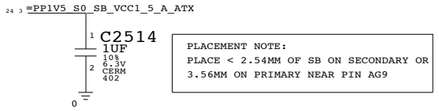


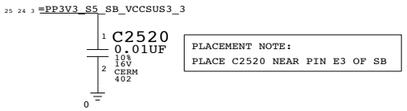


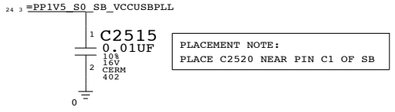


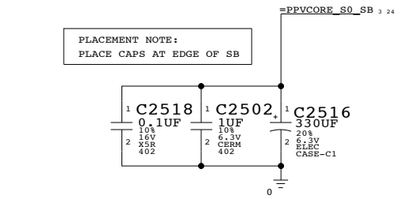


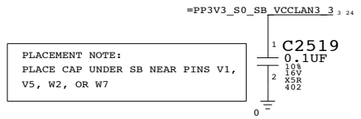


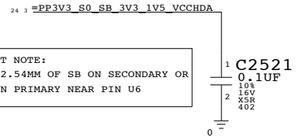


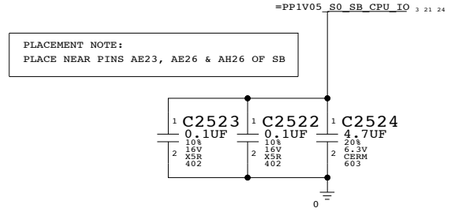


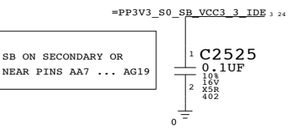


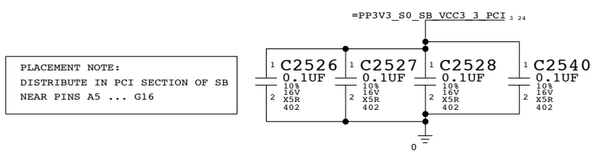


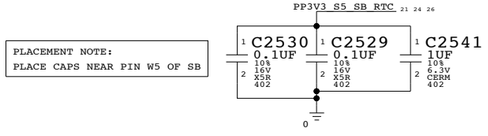


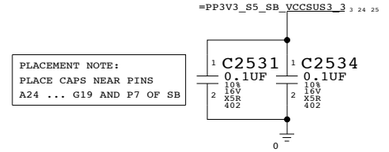


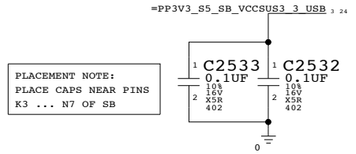


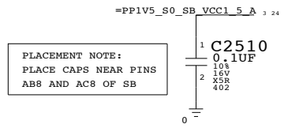


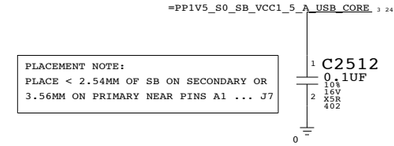










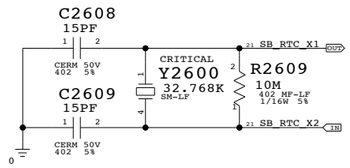


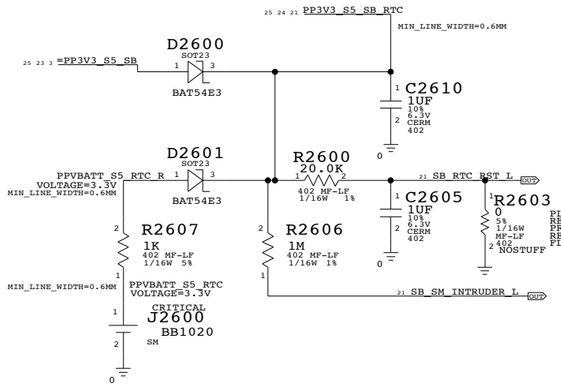
SB:DECOUPLING

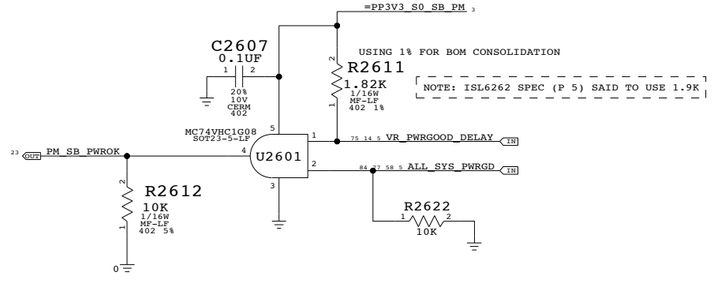
SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

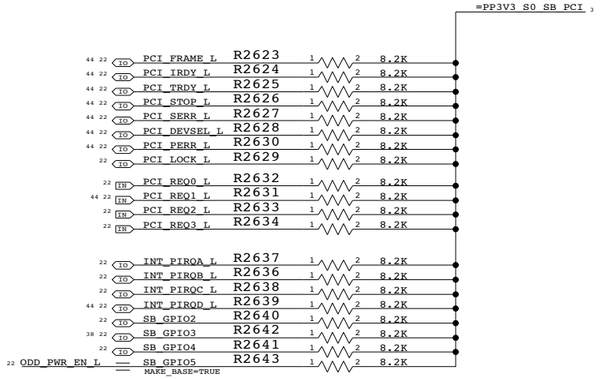
APPLE COMPUTER INC.

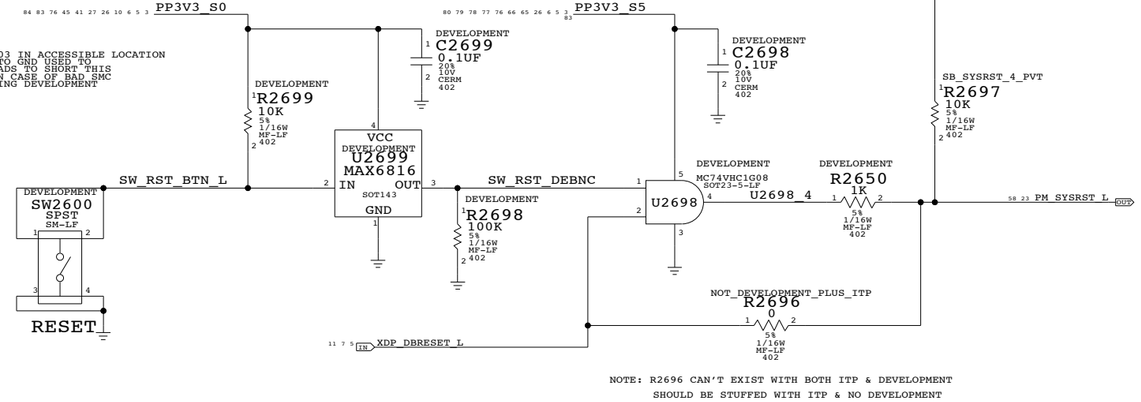
SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 25 OF 97	



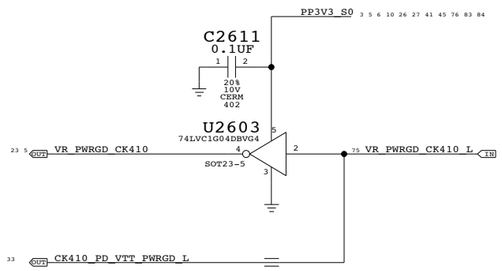








NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT



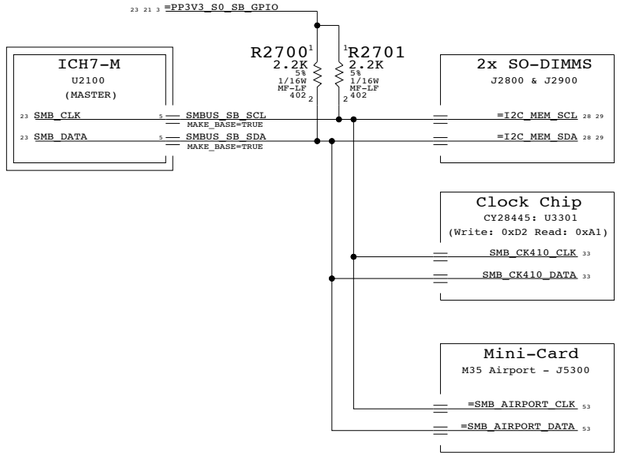
SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

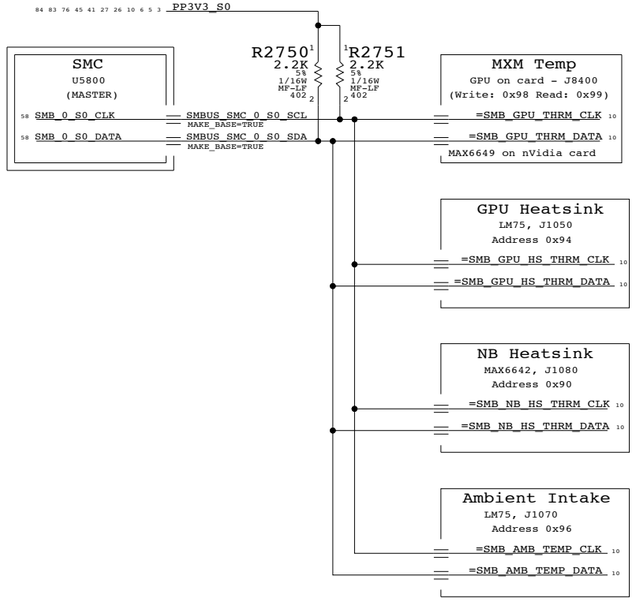
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 26 OF 97	

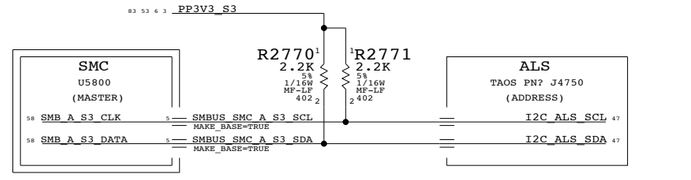
ICH7-M SMBus Connections



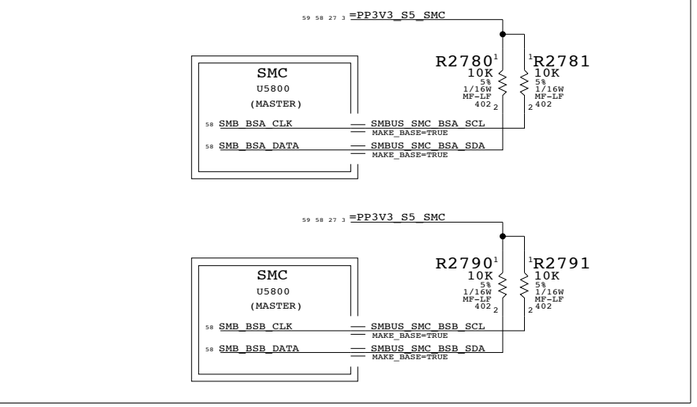
SMC "0" SMBus Connections



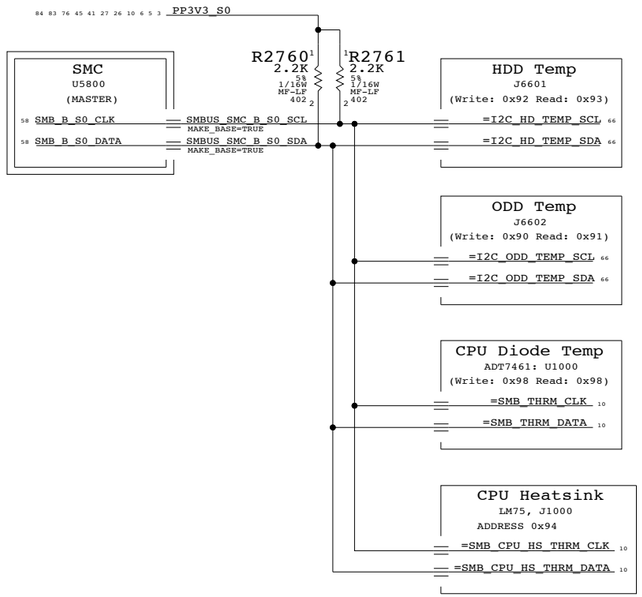
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 27 OF 97	

Page Notes

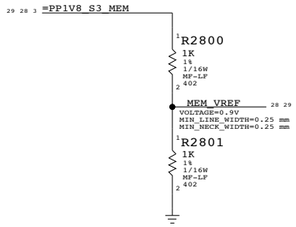
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

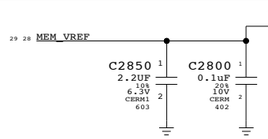
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

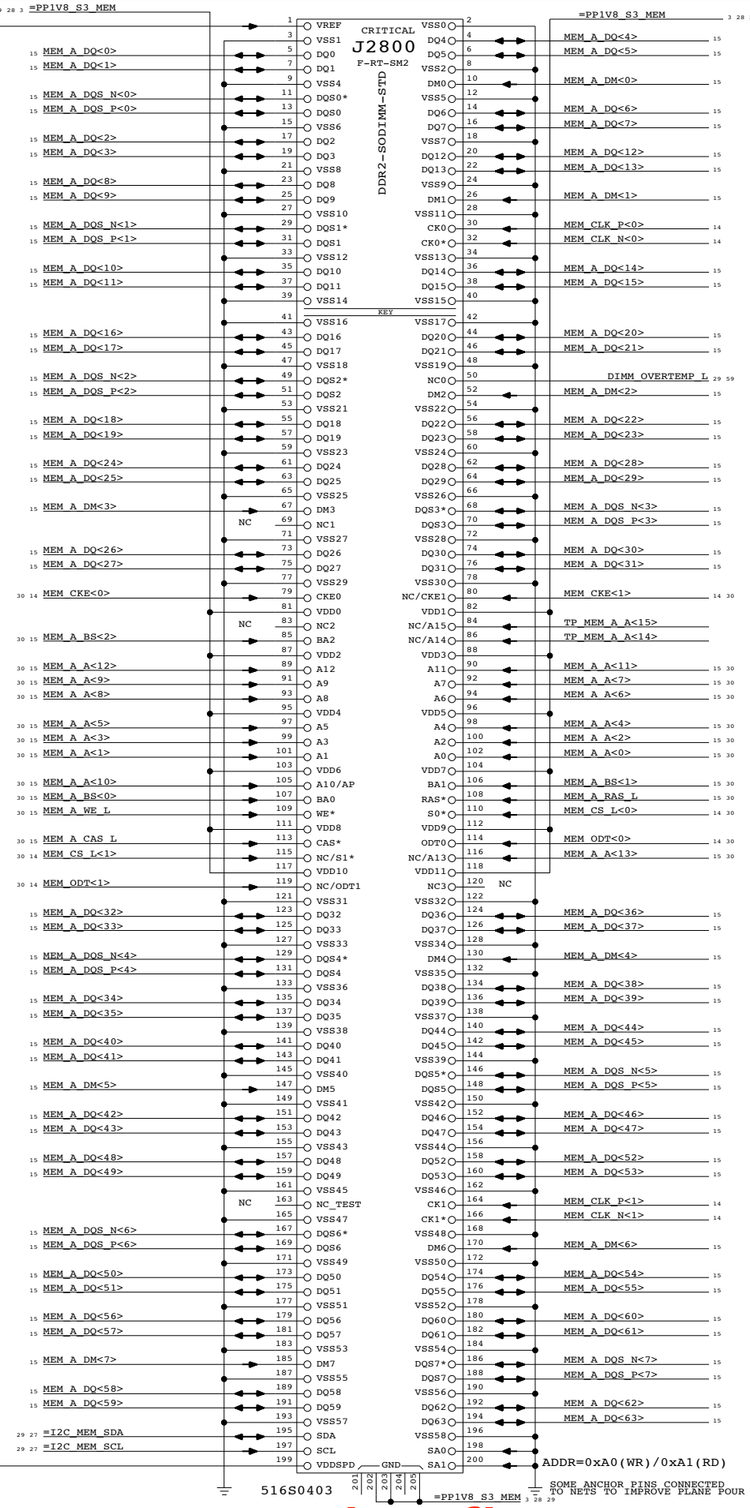
BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

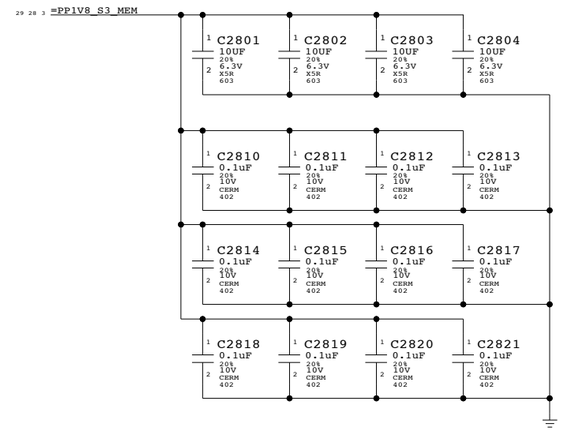


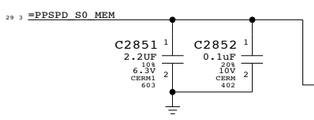




DDR2 Bypass Caps

(For return current)





DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 28 OF 97	

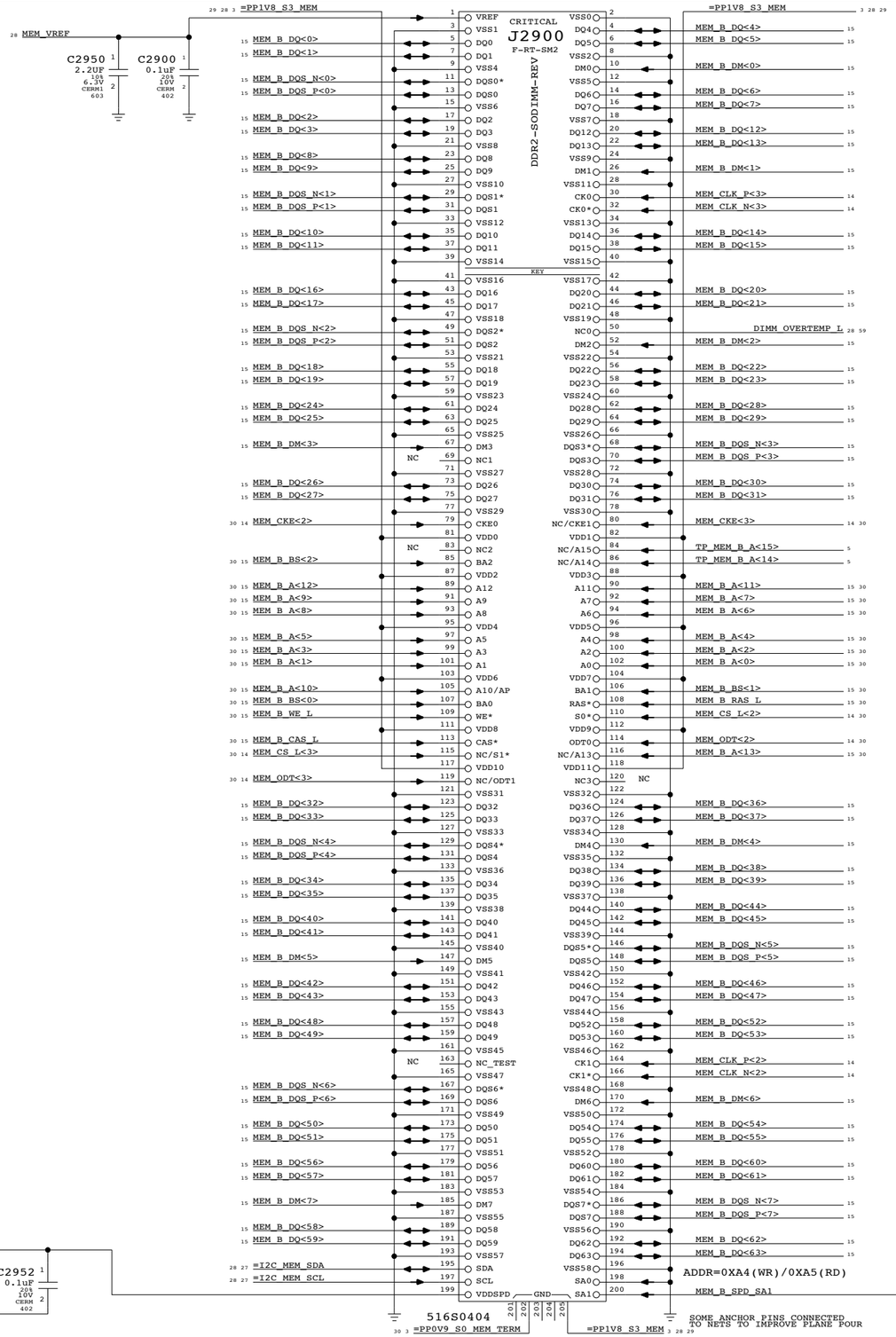
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

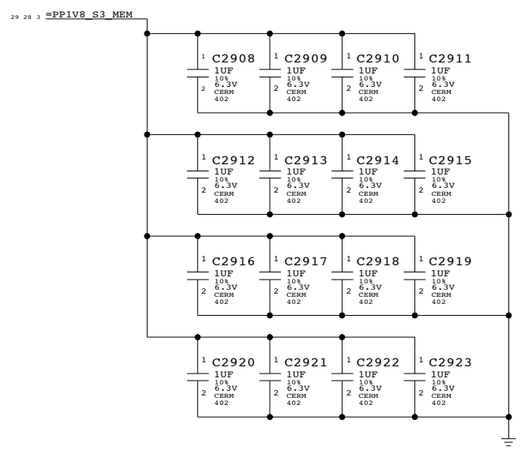
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



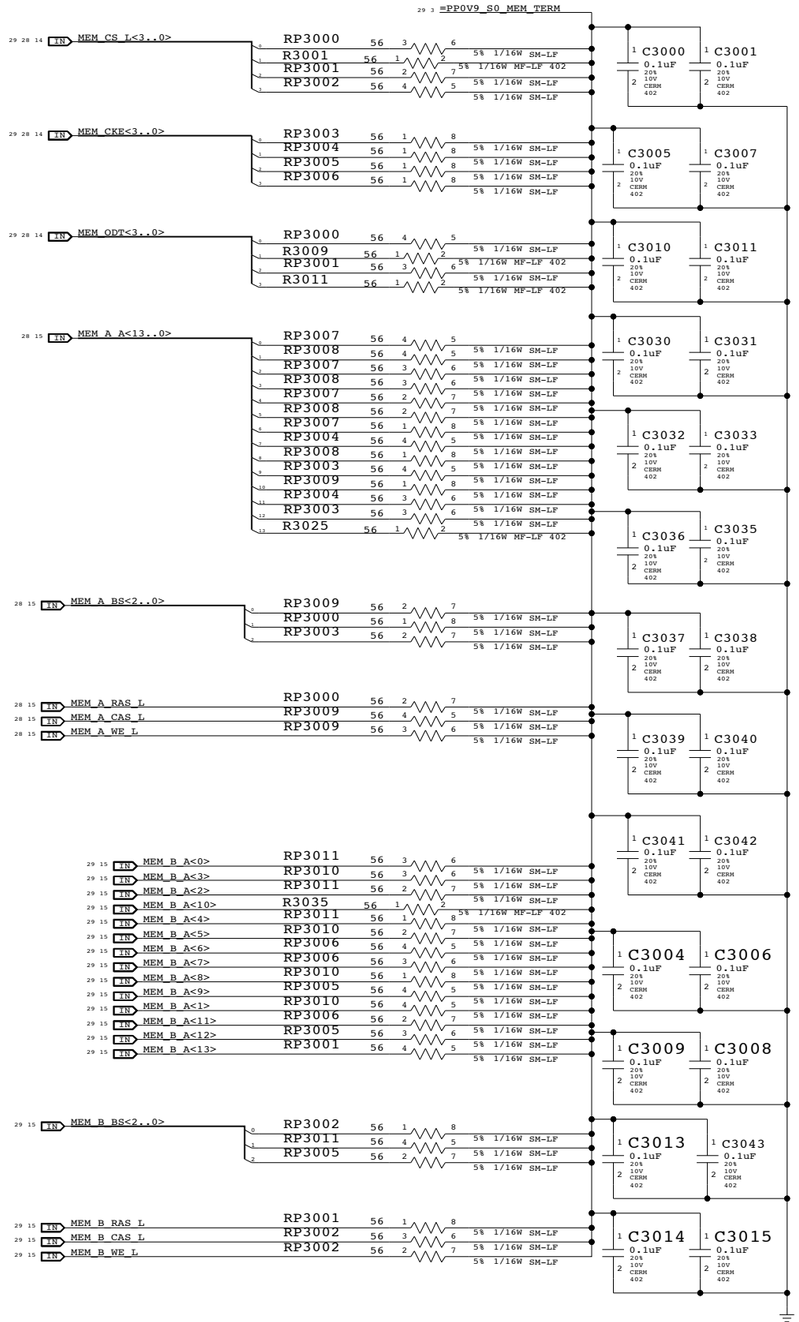
DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7039 | REV. M

SCALE NONE | SHT 30 OF 97

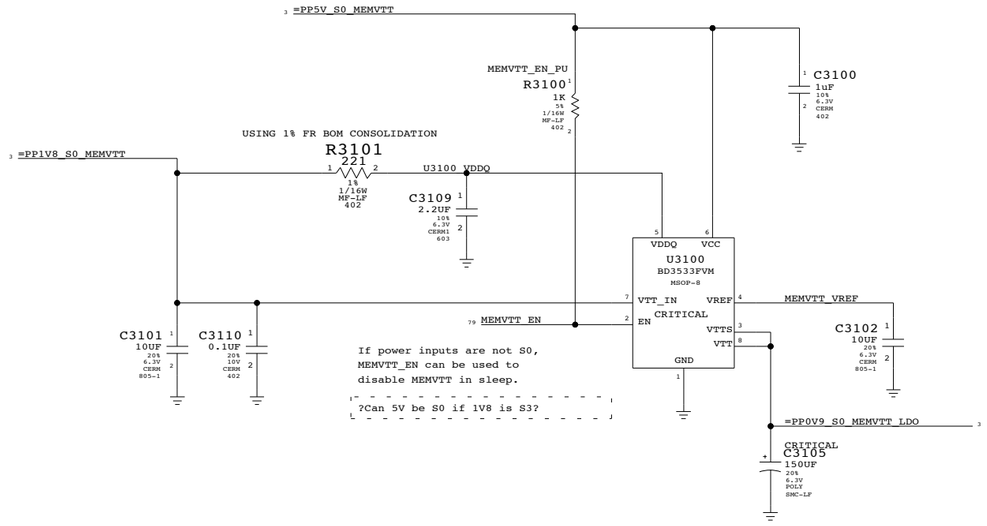
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator

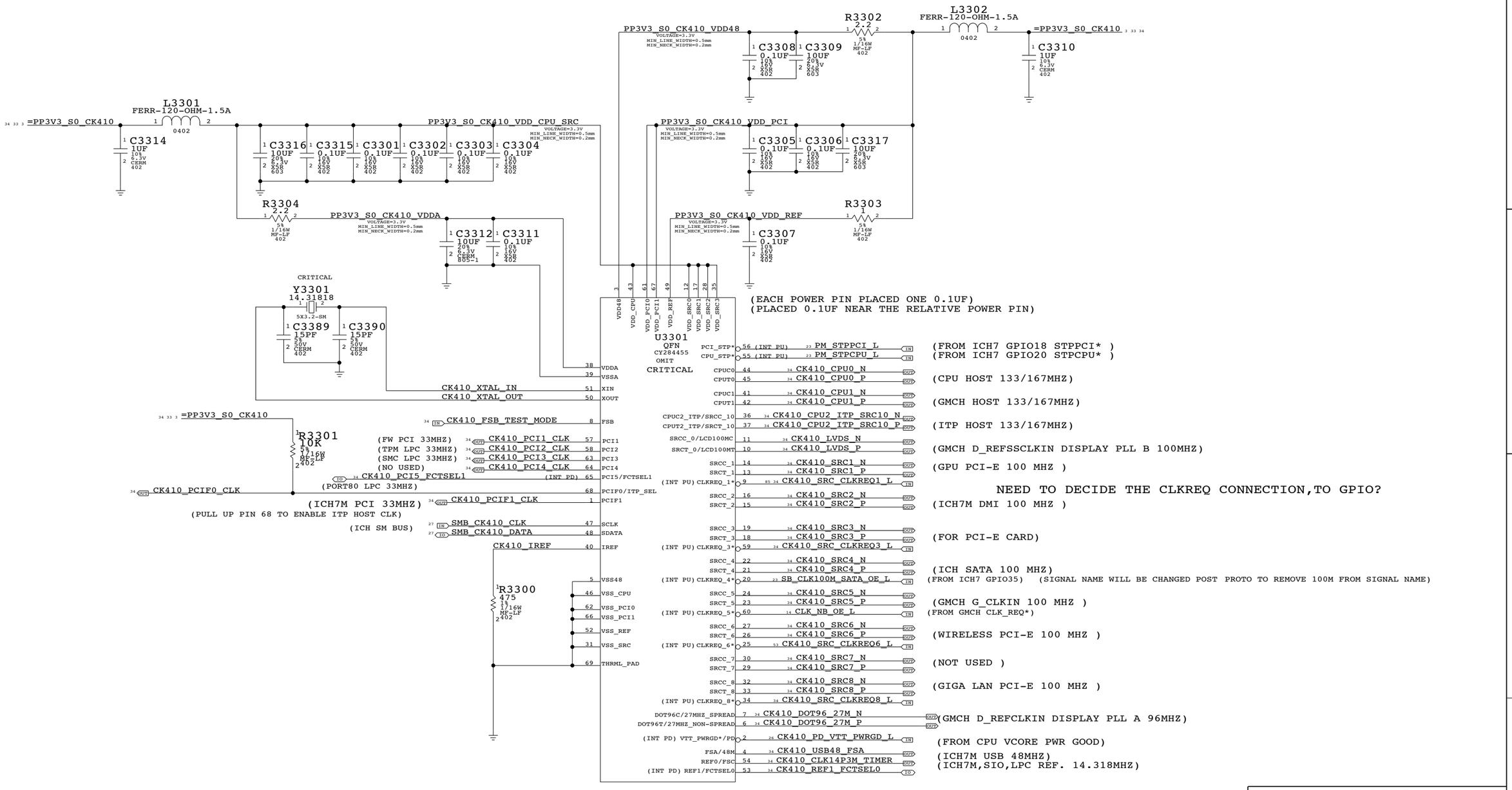


Memory Vtt Supply

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 31 OF 97	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 33 OF 97	

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 5 3 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>

NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

80 34 5 3 PP1V05_S0

R3456 1K 5% 1/16W MF-LF 402
R3458 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>

NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

80 34 5 3 PP1V05_S0

R3460 1K 5% 1/16W MF-LF 402
R3462 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>

NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

=PP3V3_S0_CK410 3 33

33 CK410_PCI5_FCTSEL1 — R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 — CK410_FSC 34

33 CK410_CLK14P3M_TIMER — R3498 33 1/16W 5% MF-LF 402 — SB_CLK14P3M_TIMER 5 23

33 CK410_REF1_FCTSEL0 — R3496 33 — TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 — CK410_FSA 34

33 CK410_USB48_FSA — R3400 33 1/16W 5% MF-LF 402 — SB_CLK48M_USBCTLR 5 23

33 CK410_PCI4_CLK — R3406 33 — TP_PCI_CLK_SPARE

33 CK410_PCI3_CLK — R3405 33 — PCI_CLK_SMC 5 58

33 CK410_PCI2_CLK — R3404 33 NOSTUFF — PCI_CLK_TPM 67

33 CK410_PCI1_CLK — R3403 33 — PCI_CLK_FW 5 44

TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF

33 CK410_PCIF1_CLK — R3401 33 — PCI_CLK_SB 5 22

33 CK410_PCIF0_CLK — R3402 33 — PCI_CLK_PORT80 5 60

33 CK410_CPU1_P	33	R3407	12 FSB_CLK_NB_P	R3429	1% 402 1/16W MF-LF	49.9
33 CK410_CPU1_N	33	R3408	12 FSB_CLK_NB_N	R3430	1% 402 1/16W MF-LF	49.9
33 CK410_CPU0_P	33	R3409	7 FSB_CLK_CPU_P	R3431		49.9
33 CK410_CPU0_N	33	R3410	7 FSB_CLK_CPU_N	R3432		49.9
33 CK410_CPU2_ITP_SRC10_P	33	R3411	11 5 CPU_XDP_CLK_P = MAKE_BASE=TRUE FSB_CLK_XDP_P	R3433		49.9
33 CK410_CPU2_ITP_SRC10_N	33	R3412	11 5 CPU_XDP_CLK_N = FSB_CLK_XDP_N MAKE_BASE=TRUE	R3434		49.9
33 CK410_SRC6_P	33	R3413	53 AIRPORT_CLK100M_PCIE_P	R3435		49.9
33 CK410_SRC6_N	33	R3414	53 AIRPORT_CLK100M_PCIE_N	R3436		49.9
33 CK410_SRC5_P	33	R3415	14 NB_CLK100M_GCLKIN_P	R3438		49.9
33 CK410_SRC5_N	33	R3416	14 NB_CLK100M_GCLKIN_N	R3437		49.9
33 CK410_SRC4_P	33	R3417	21 5 SB_CLK100M_SATA_P	R3439		49.9
33 CK410_SRC4_N	33	R3418	21 5 SB_CLK100M_SATA_N	R3440		49.9
33 CK410_SRC2_P	33	R3419	22 SB_CLK100M_DMI_P	R3442		49.9
33 CK410_SRC2_N	33	R3420	22 SB_CLK100M_DMI_N	R3441		49.9
33 CK410_SRC8_P	33	R3421	41 ENET_CLK100M_PCIE_P	R3443		49.9
33 CK410_SRC8_N	33	R3422	41 ENET_CLK100M_PCIE_N	R3444		49.9
33 CK410_SRC1_P	33	R3423	85 GPU_CLK100M_PCIE_P	R3446		49.9
33 CK410_SRC1_N	33	R3424	85 GPU_CLK100M_PCIE_N	R3445		49.9

33 CK410_LVDS_P = MAKE_BASE=TRUE — TP_CK410_LVDS_P
33 CK410_LVDS_N = MAKE_BASE=TRUE — TP_CK410_LVDS_N

33 CK410_DOT96_27M_N = MAKE_BASE=TRUE — TP_CK410_27M_SPREAD
33 CK410_DOT96_27M_P = MAKE_BASE=TRUE — TP_CK410_27M_NONSPREAD

33 CK410_SRC3_P — 33 — R3492 — SPARE_SRC3_P — R3488 — 49.9
33 CK410_SRC3_N — 33 — R3491 — SPARE_SRC3_N — R3487 — 49.9
33 CK410_SRC7_P — 33 — R3490 — SPARE_SRC7_P — R3486 — 49.9
33 CK410_SRC7_N — 33 — R3489 — SPARE_SRC7_N — R3485 — 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) — R3495 NOSTUFF 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) — R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) — R3493 1K

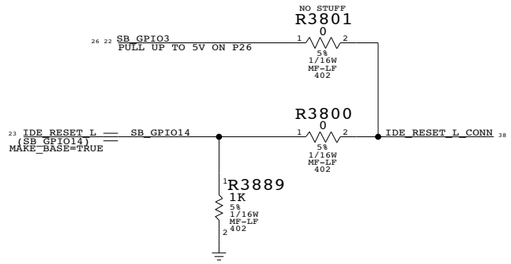
NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

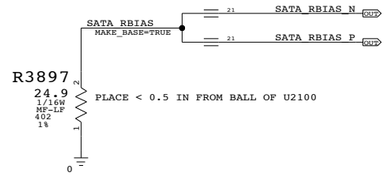
CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

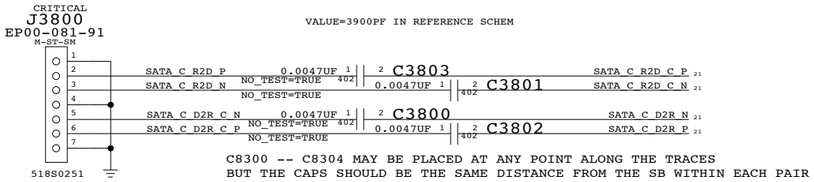
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 34 OF 97	

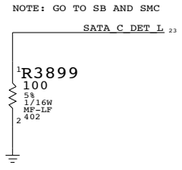


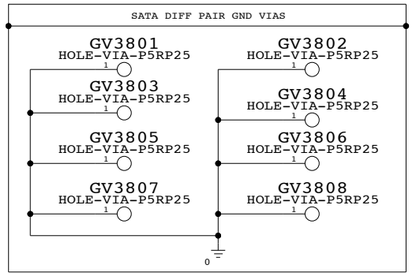


SATA CONNECTOR

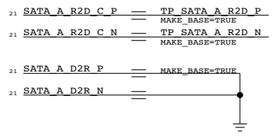


C8300 -- C8304 MAY BE PLACED AT ANY POINT ALONG THE TRACES
BUT THE CAPS SHOULD BE THE SAME DISTANCE FROM THE SB WITHIN EACH PAIR

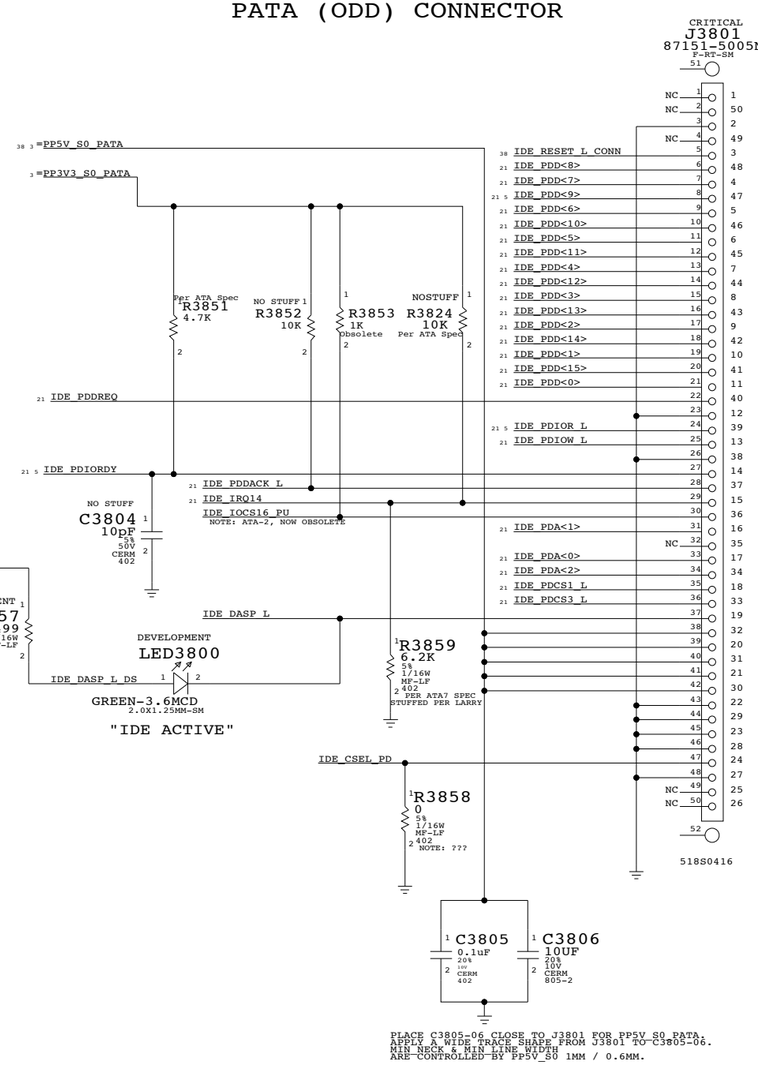




SATA PORT 0 IS NOT USED



PATA (ODD) CONNECTOR



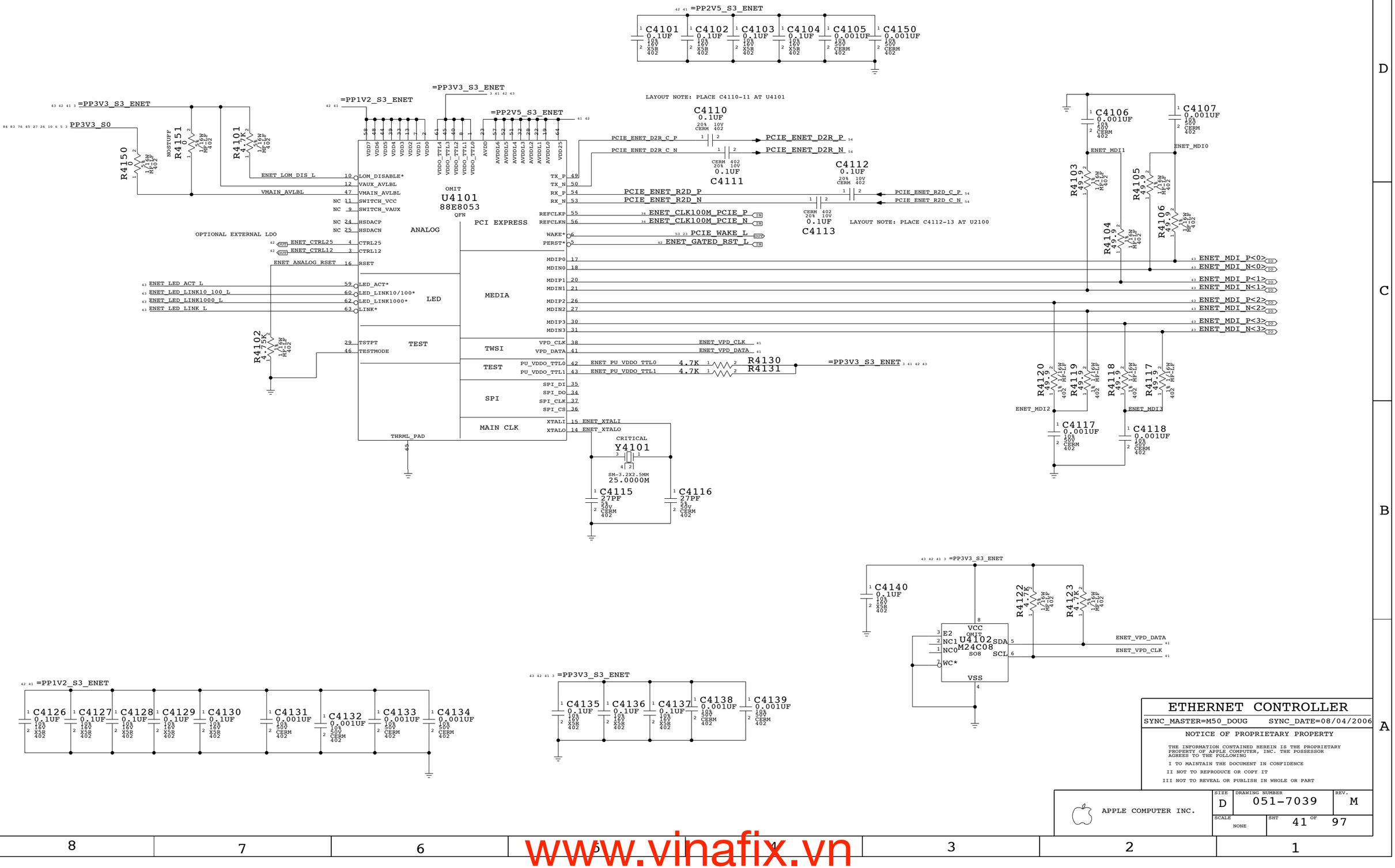
PLACE C3805-06 CLOSE TO J3801 FOR PP5V_S0_PATA.
APPLY A WIDE TRACE SHAPE FROM J3801 TO C3805-06.
MIN NECK & MIN LINE WIDTH
ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

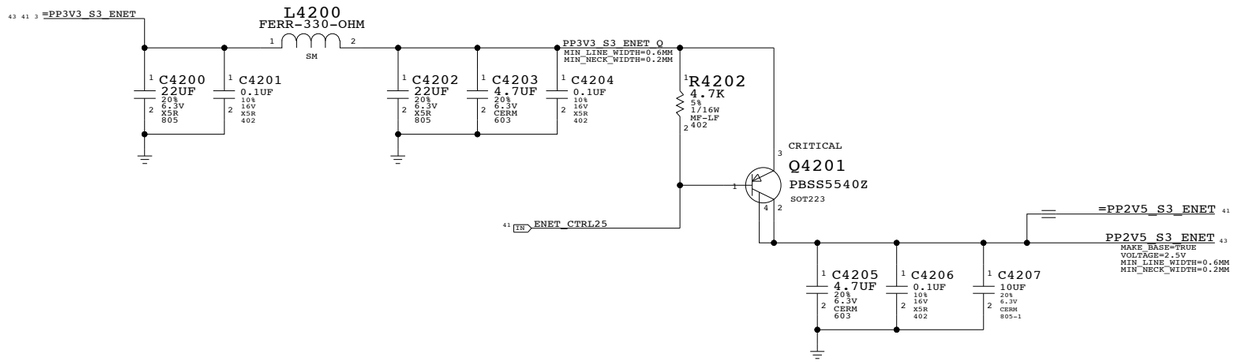
Disk Connectors

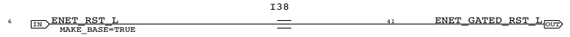
SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

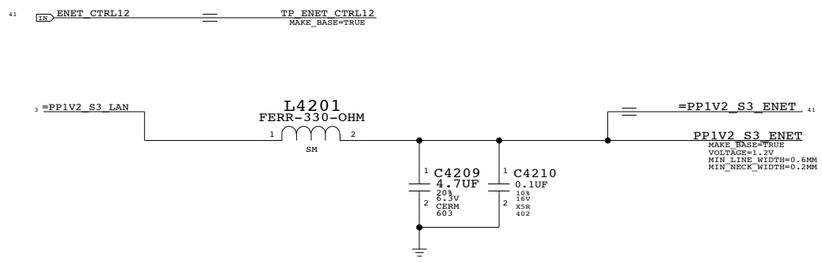
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 38 OF 97	









ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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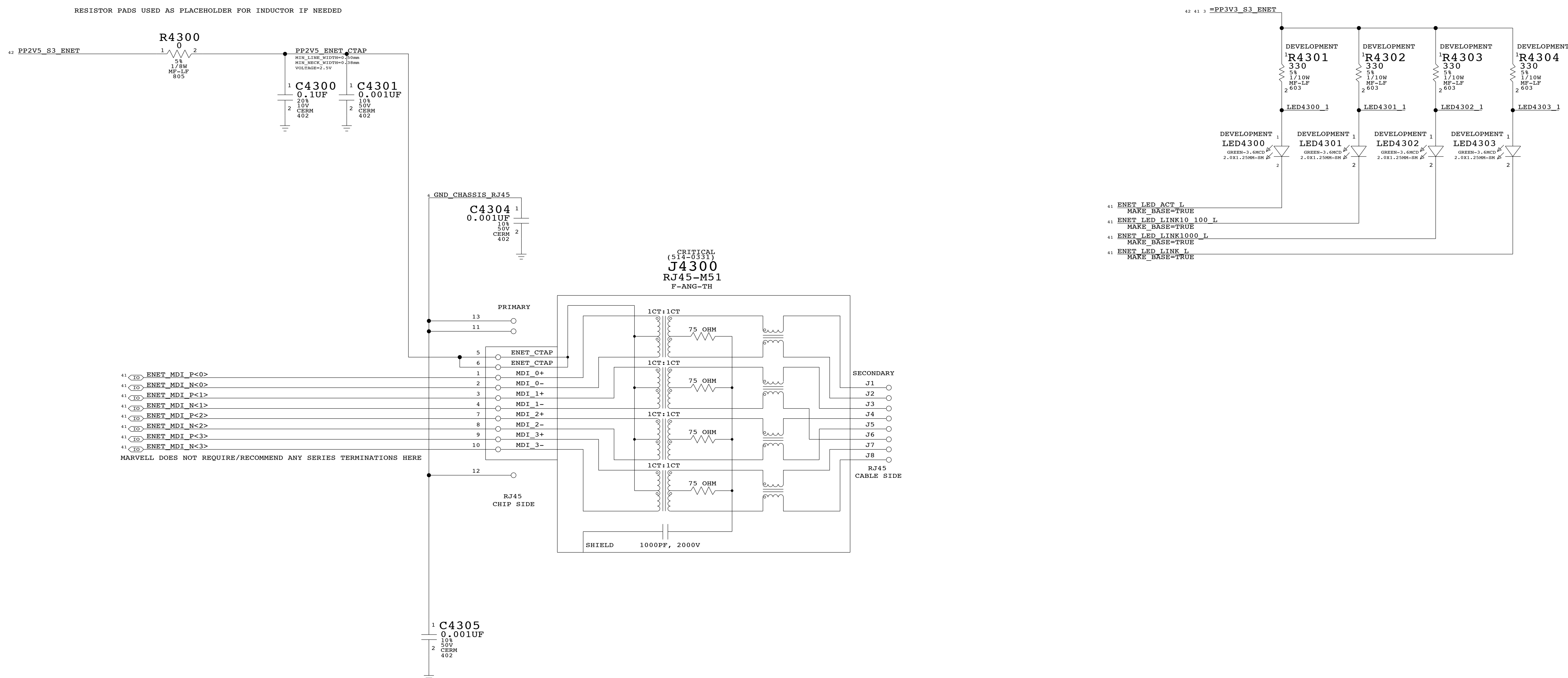
D	051-7039	M
SCALE: NONE	SHT 42 OF 97	


RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED
PP2V5_S3_ENET
R4300
0
5%
1/8W
MF-LF
805
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=2.5V
C4300
0.1UF
20%
10V
CERM
402
C4301
0.001UF
10%
50V
CERM
402
GND_CHASSIS_RJ45
C4304
0.001UF
10%
50V
CERM
402
CRITICAL
(514-0331)
J4300
RJ45-M51
F-ANG-TH
PRIMARY
SECONDARY
ENET_CTAP
MDI_0+
MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
MDI_3+
MDI_3-
1CT:1CT
75 OHM
J1
J2
J3
J4
J5
J6
J7
J8
RJ45
CABLE SIDE
RJ45
CHIP SIDE
SHIELD
1000PF, 2000V
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE
C4305
0.001UF
10%
50V
CERM
402
=PP3V3_S3_ENET
DEVELOPMENT
R4301
R4302
R4303
R4304
330
5%
1/10W
MF-LF
603
LED4300_1
LED4301_1
LED4302_1
LED4303_1
LED4300
LED4301
LED4302
LED4303
GREEN-3.6MCD
2.0X1.25MM-SM
ENET_LED_ACT_L
MAKE_BASE=TRUE
ENET_LED_LINK10_100_L
MAKE_BASE=TRUE
ENET_LED_LINK1000_L
MAKE_BASE=TRUE
ENET_LED_LINK_L
MAKE_BASE=TRUE

ETHERNET CONNECTOR

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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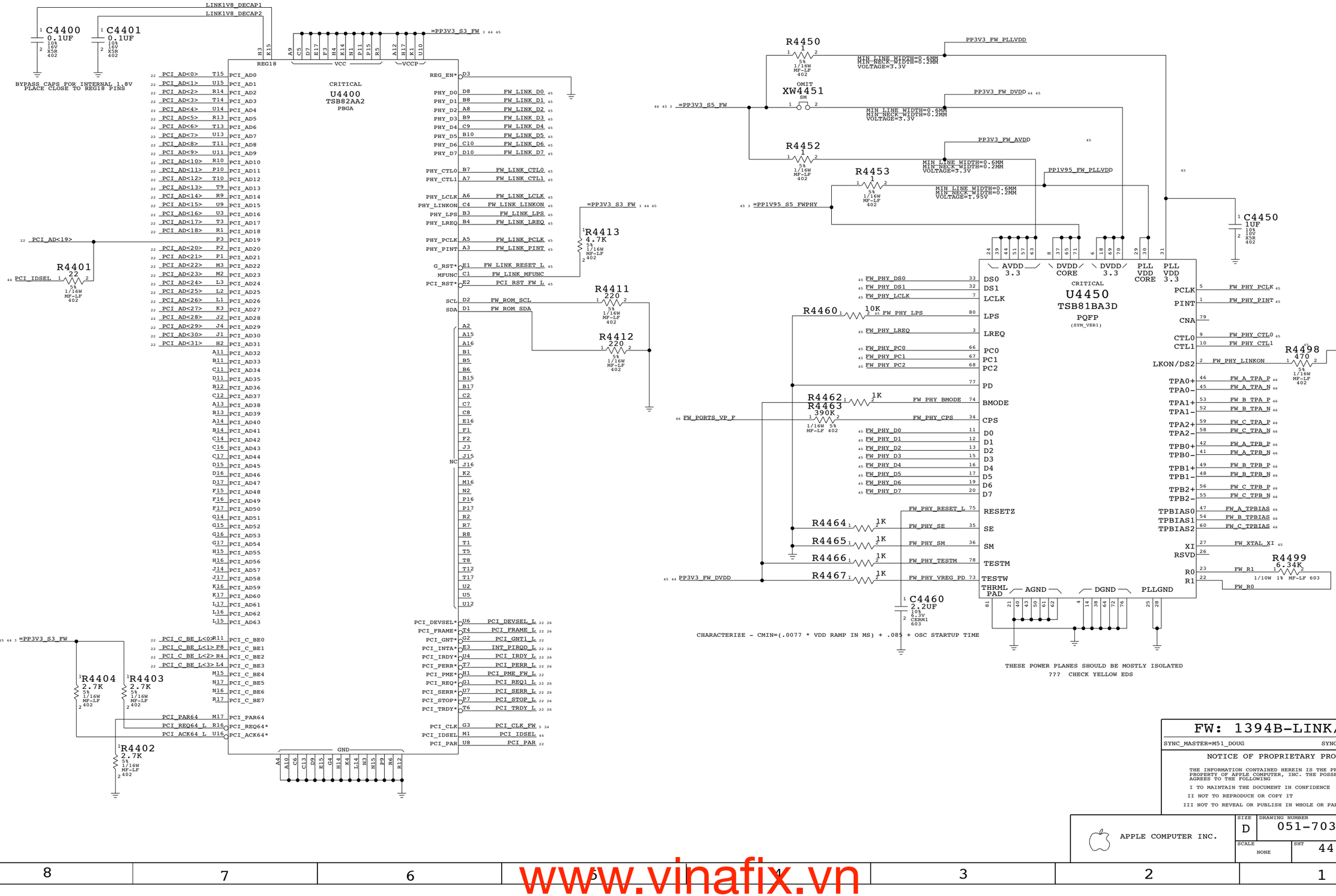
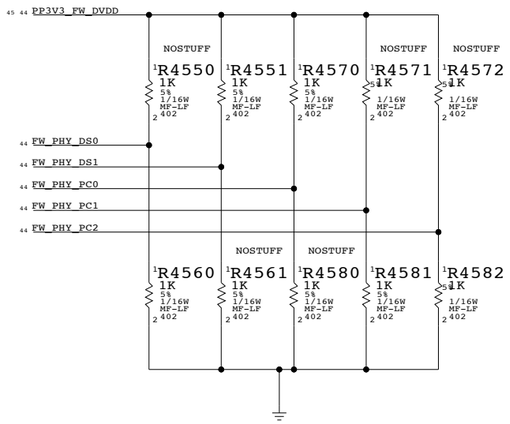
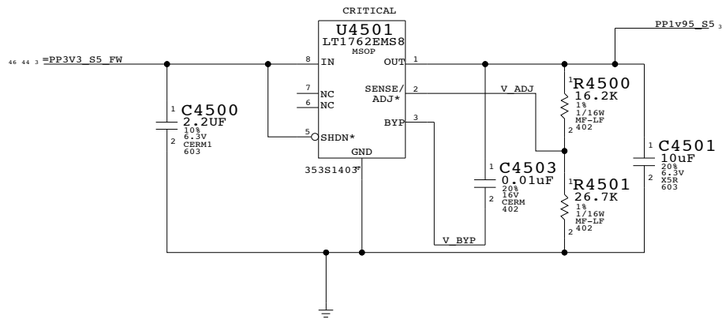


1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



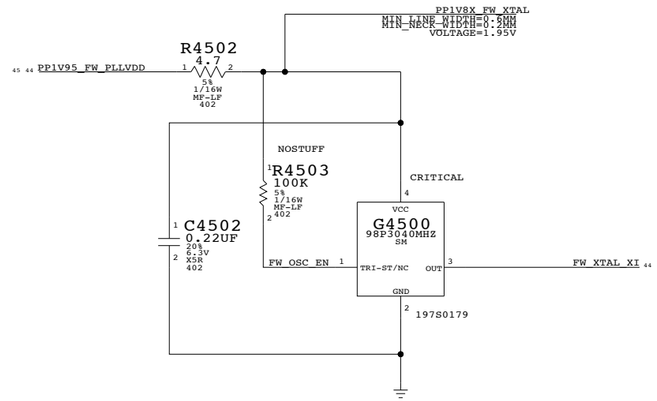
1394 PHY 1.95V REGULATOR



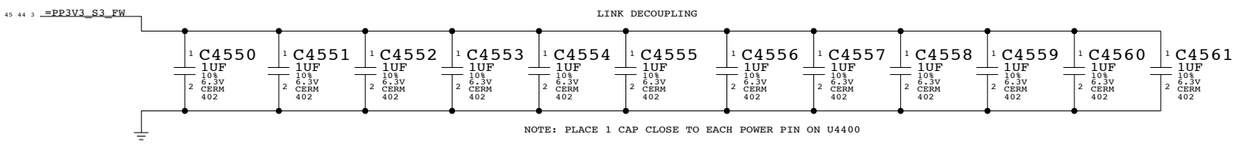
VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

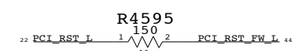


LINK DECOUPLING

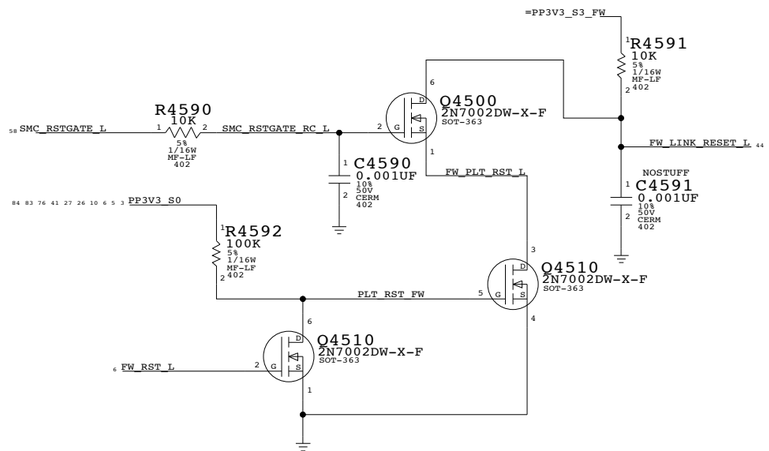


NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

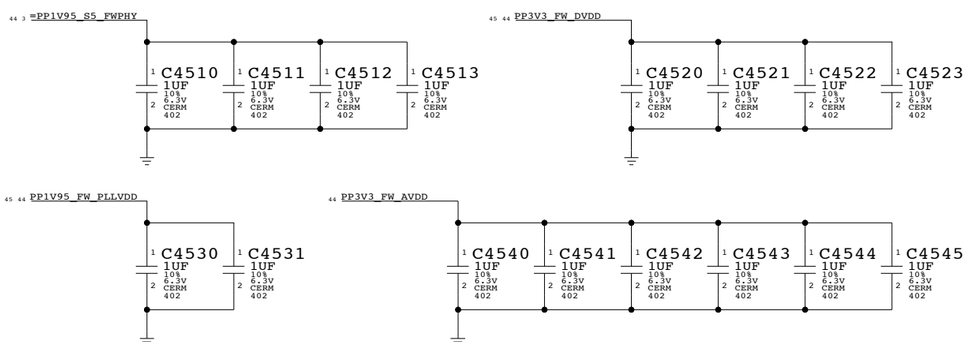
1394 LINK POWER ON RESET AND PCI RESET



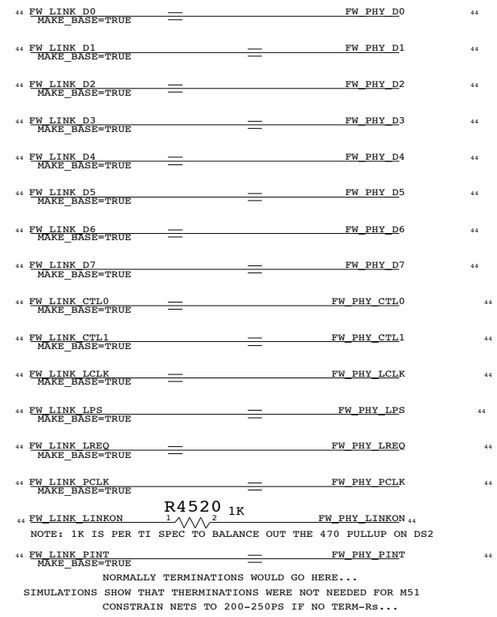
NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT



PHY DECOUPLING



NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450



NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2

NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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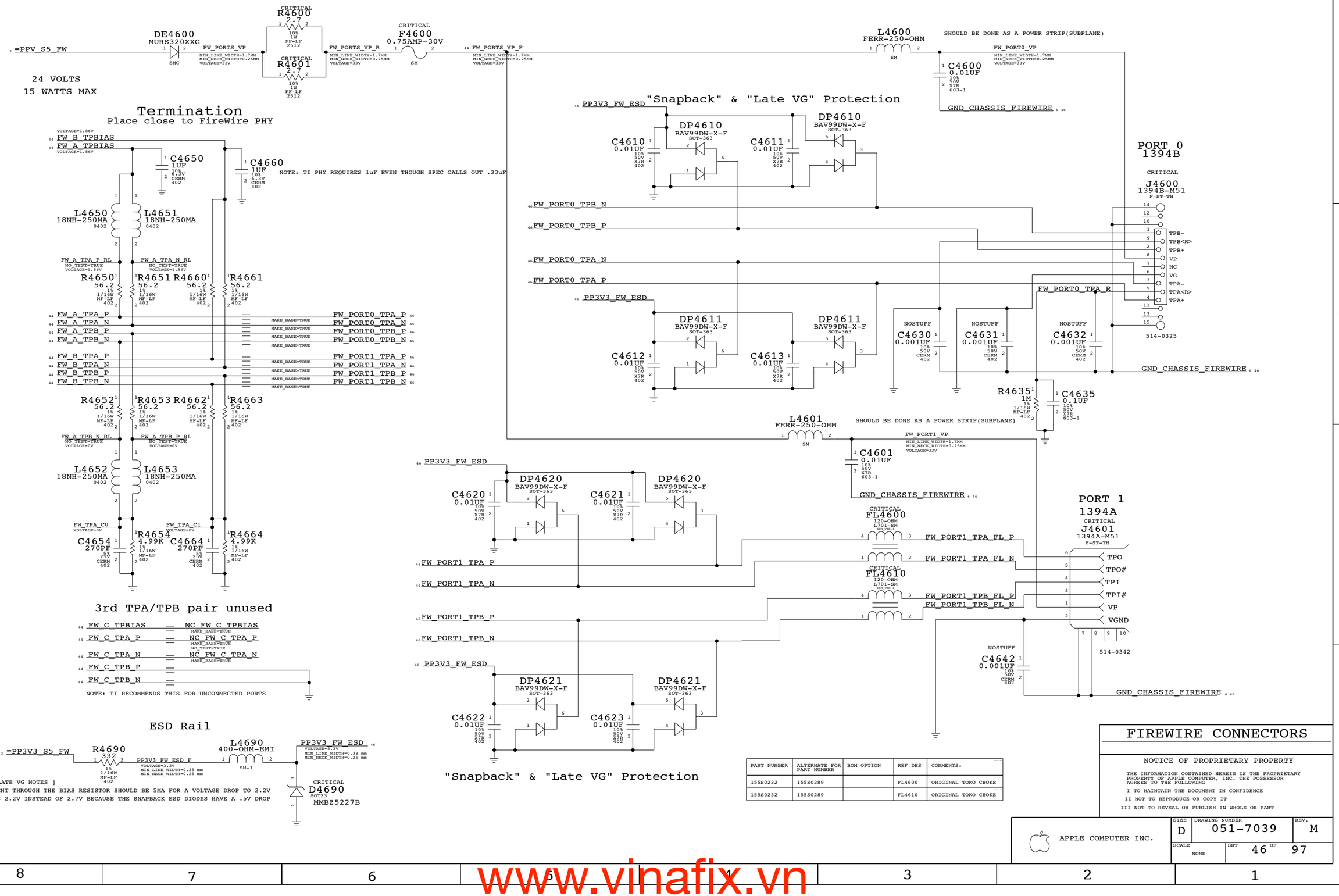

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

APPLE COMPUTER INC.

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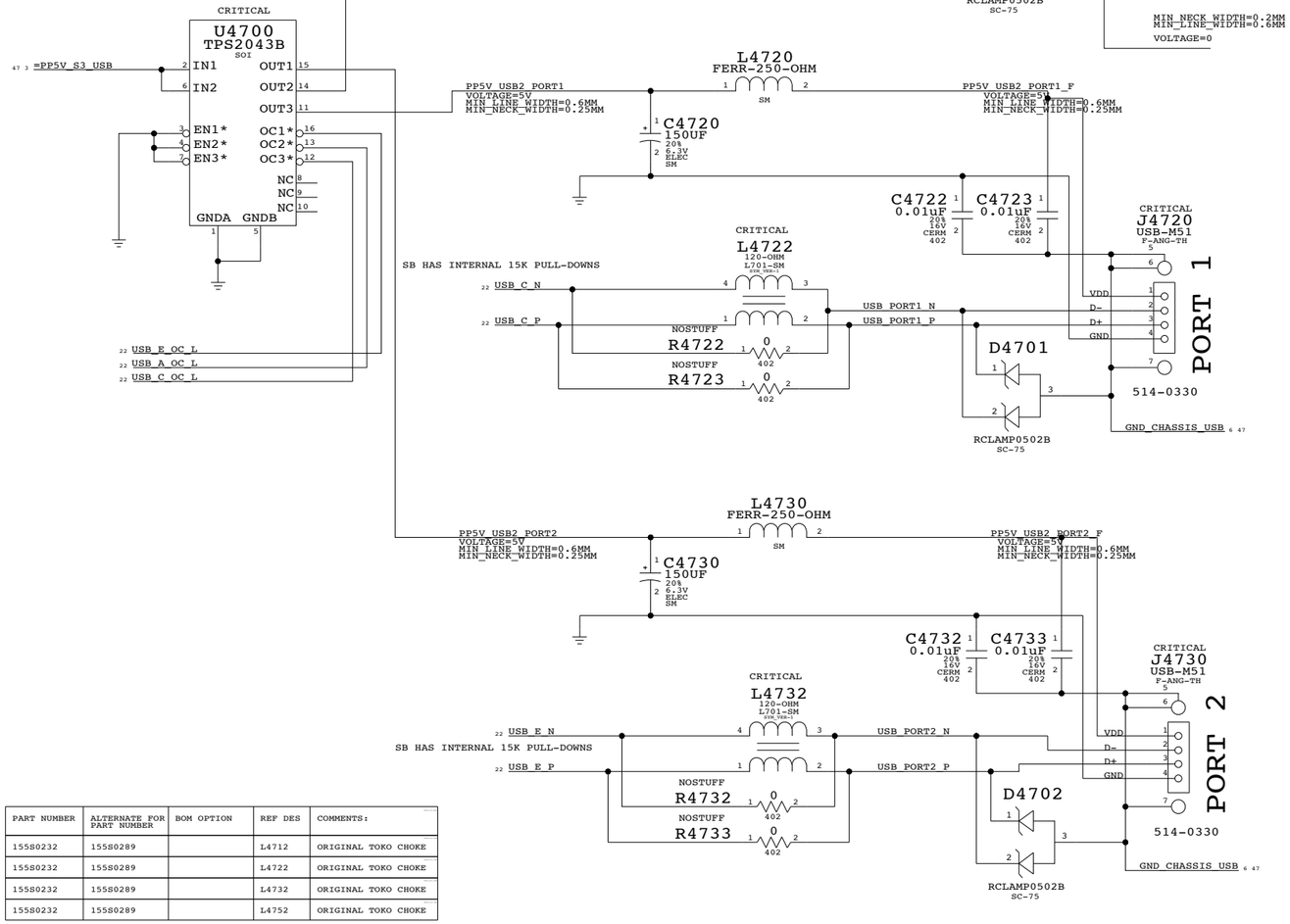
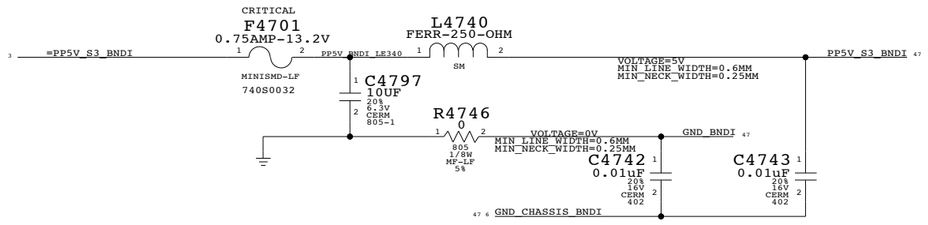
SCALE: NONE	SHT 46 OF 97	

External USB Ports



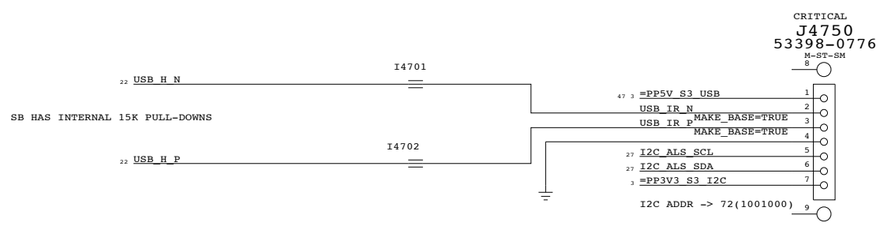
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



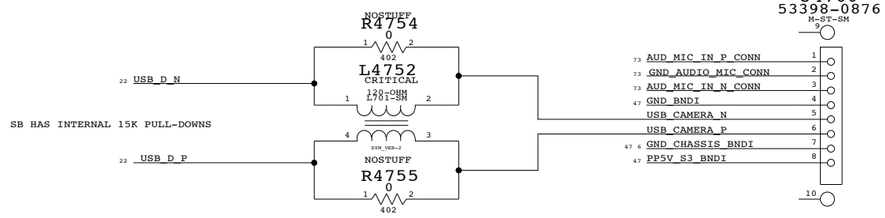
LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR J4760 PIN 8 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO J4760.

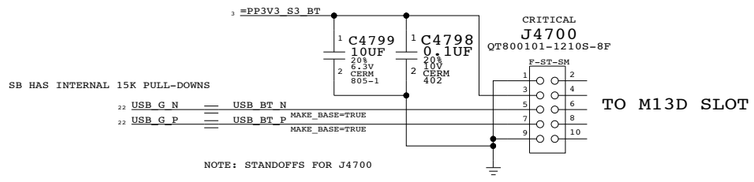
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



CRITICAL
SDF4700
STDOFF-4OD4.5H-1.35-TH

CRITICAL
SDF4701
STDOFF-4OD4.5H-1.35-TH

USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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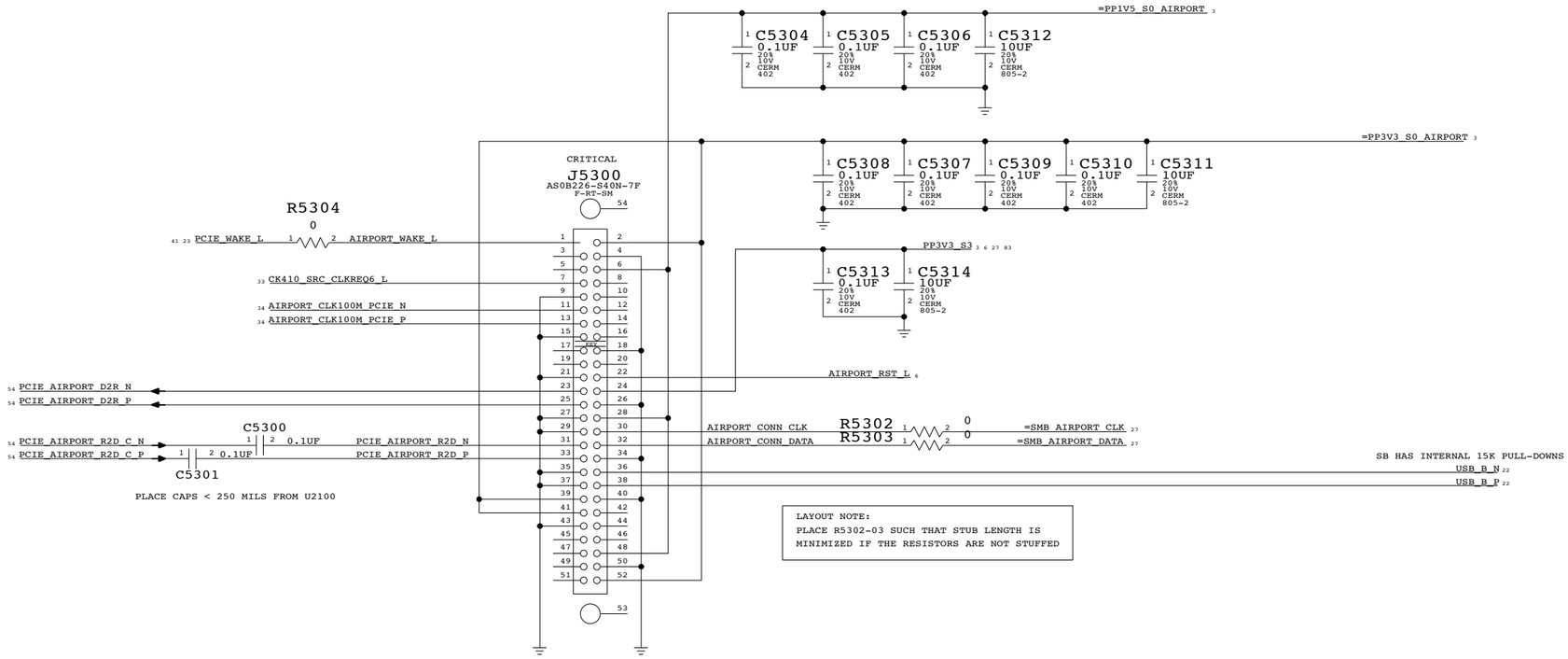

AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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SCALE: NONE	SHT 53 OF 97	

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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SCALE: NONE	SHT 54 OF 97	

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

23 OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	59 SMC_PM_G2_EN OUT
45 OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	59 SMC_ADAPTER_EN OUT
84 77 26 5 IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22 SPI_ARB IN
76 IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22 SPI_SCLK IN
23 OUT	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22 5 SPI_SI OUT
23 OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22 5 SPI_SO IN
75 OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59 SMC_PROCHOT_3_3_L IN
23 OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59 SMC_CPU_INIT_3_3_L IN
59	SMC_P20	D13	P20	P70/AN0	N12	76 SMC_CPU_ISENSE IN
59	SMC_P21	D14	P21	P71/AN1	R13	76 SMC_CPU_VSENSE IN
59	SMC_P22	D15	P22	P72/AN2	P13	84 SMC_GPU_ISENSE IN
59	SMC_P23	E12	P23	P73/AN3	R14	84 SMC_GPU_VSENSE IN
59 OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76 SMC_DCIN_ISENSE IN
59 OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76 SMC_PBUS_VSENSE IN
59	SMC_P26	E13	P26	P76/AN6	N13	59 SMC_BATT_ISENSE IN
59	SMC_P27	F14	P27	P77/AN7	P15	59 SMC_FWIRE_ISENSE IN
67 60 21 5 IO	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23 SMC_WAKE_SCI_L IN
67 60 21 5 IO	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59 SMC_TPM_GPIO OUT
67 60 21 5 IO	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 23 5 PM_CLKRUN_L IO
67 60 21 5 IO	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23 5 PM_SUS_STAT_L IN
67 60 21 5 IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59 SC_TX_L OUT
6 IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59 SC_RX_L IN
34 5 IN	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27 SMB_BSB_CLK IO
67 60 23 5 OUT	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59 SMC_ONOFF_L IN
59 OUT	SMC_XDP_TMS	A5	P40/TMIO	P91/IRQ1*	J2	59 SMC_BC_ACOK IN
59 OUT	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	59 SMC_BS_ALRT_L IN
27 IO	SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	80 79 77 23 5 PM_SLP_S3_L IN
59 OUT	SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23 5 PM_SLP_S4_L IN
59 OUT	SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23 PM_SLP_S5_L IN
59 OUT	SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59 SMC_SUS_CLK IN
59 OUT	SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27 SMB_0_S0_DATA IO
59 OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
60 59 5 OUT	SMC_TX_L	G1	P50			
60 59 5 IN	SMC_RX_L	G4	P51			
27 IO	SMB_0_S0_CLK	F2	P52/SCL0			

OMIT
U5800
SMC_H8S2116
BGA
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21 OUT	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	59 SMC_CASE_OPEN IN
60 22 5 IN	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5 SMC_TCK IN
26 23 IN	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5 SMC_TDI IN
67 59 OUT	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5 SMC_TDO OUT
59 14 IN	PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5 SMC_TMS IN
23 10 IO	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0 59
59 IO	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1 59
23 OUT	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59 SMC_LID IN
23 IN	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59 SMC_CPU_RESET_3_3_L IN
23 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59 SMC_BATT_ISET OUT
59 IN	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59 SMC_BATT_VSET OUT
76 5 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59 SMC_SYS_ISET OUT
59 IN	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59 SMC_SYS_VSET OUT
59 OUT	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22 SPI_CE_L IO
59 IN	SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59 SMC_XDP_TCK_3_3 IN
59 IN	SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27 SMB_BSA_DATA IO
65 OUT	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27 SMB_BSA_CLK IO
65 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27 SMB_A_S3_DATA IO
66 OUT	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27 SMB_A_S3_CLK IO
59 OUT	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27 SMB_B_S0_DATA IO
65 IN	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27 SMB_B_S0_CLK IO
65 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59 SMC_PROCHOT OUT
66 IN	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59 SMC_THRMTRIP OUT
59 IN	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59 SMC_FWE IN
59 IN	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59 ALS_GAIN OUT
59 IN	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23 SMS_INT_L OUT
59 IN	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59 SMS_ONOFF_L OUT
59 IN	SMC_ANALOG_ID	N11	PD3/AN11			
59 IN	SMC_NB_ISENSE	P10	PD4/AN12			
59 IN	SMC_MEM_ISENSE	R10	PD5/AN13			
59 IN	ALS_LEFT	N10	PD6/AN14			
59 IN	ALS_RIGHT	M10	PD7/AN15			

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 27 3 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 27 3 =PP3V3_S5_SMC
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
84 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 27 3 =PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

AVCC	N14	VCC	P2
AVCC	N15	VCC	P1
VCC	J15	VCC	A1
VCC	F1	AVREF	M14
AVREF	M15		

60 59 5 IN SMC_RST_L — RES* E3
59 SMC_XTAL — XTAL A2
59 SMC_EXTAL — EXTAL B2
MD1 E2 — SMC_MD1 5 60
MD2 K1 — KBC_MDE
NMI F4 — SMC_NMI IN
ETRST* L1 — SMC_TRST_L IN
AVSS P12, R12
VSS D1, F4, R4, F12, F13, B13, A13, A4, B4, D2

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

OMIT
XW5800
GND_SMC_AVSS 58 59 76 84

SMC

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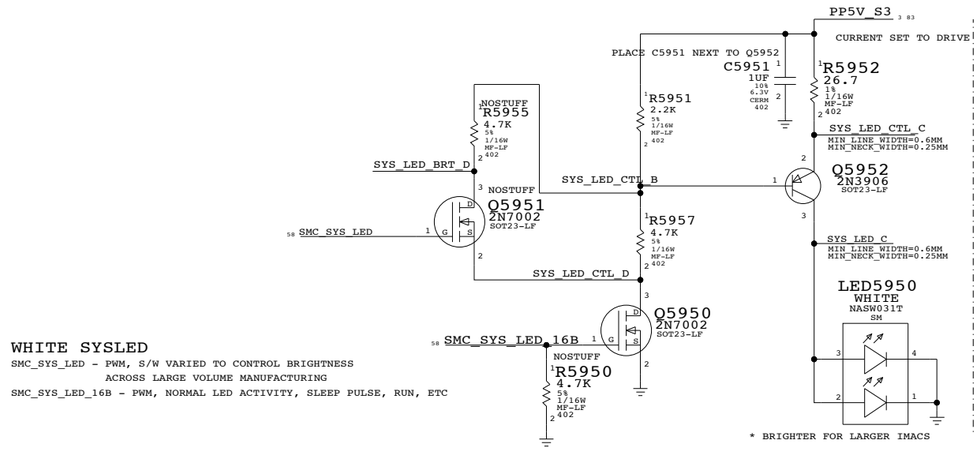
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 58 OF 97	

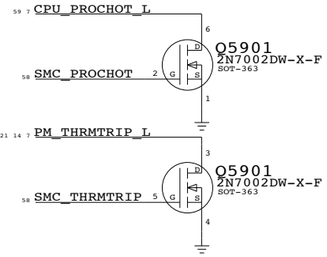


WHITE SYSLED

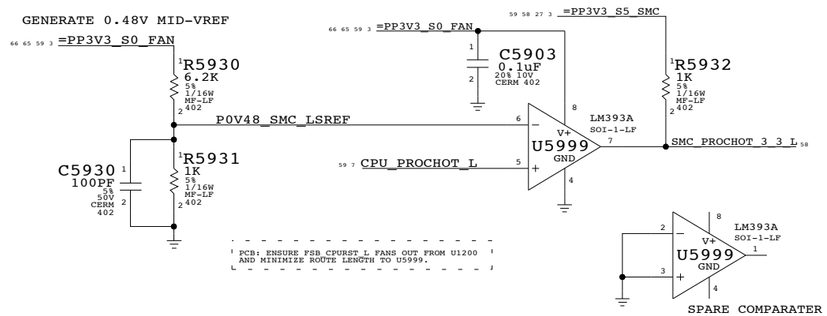
SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING

SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

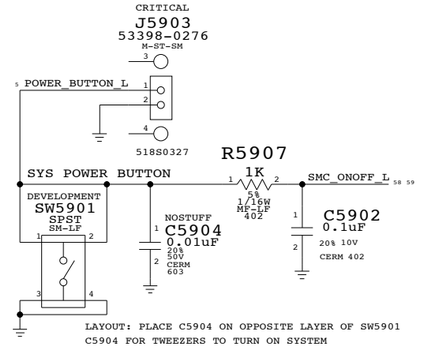
SMC 3.3V -> CPU 1.05V SHIFTER



CPU 1.05V -> SMC 3.3V SHIFTER

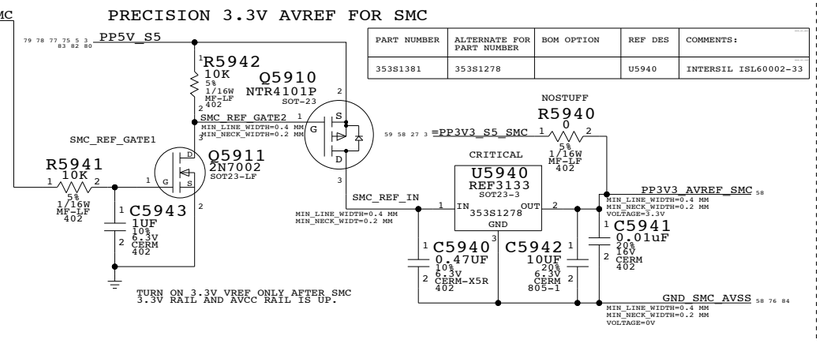


POWER BUTTON HEADER

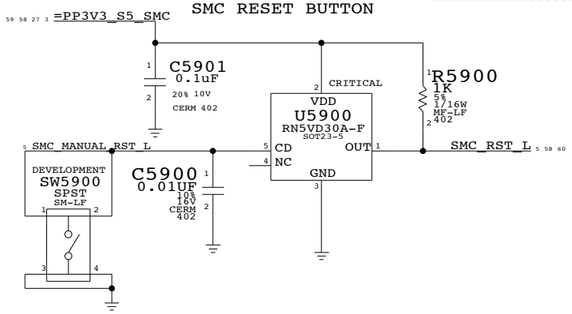


PRECISION 3.3V AVREF FOR SMC

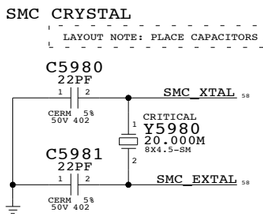
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	INTERSIL ISL60002-33



SMC RESET BUTTON

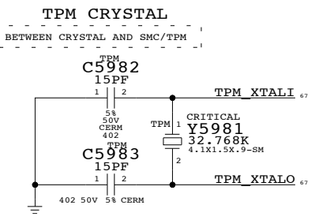


SMC CRYSTAL



TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_PM_G2_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE; FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE
SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE; FUNC_TEST=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE
SMC_NB_ISENSE	NC_SMC_NB_ISENSE	MAKE_BASE=TRUE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE

UNUSED_SMC_SENSE — 10K — R5924 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE; FUNC_TEST=TRUE

TPM RESET PULLUP

PP3V3_TPM_3VSB — R5827 10K — SMC_TPM_RESET_L

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE

SC_RX_L — 0 R5922 — SMC_RX_L

SC_TX_L — 0 R5923 — SMC_TX_L

SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC — R5808 5% 1/16W MF-LF 402

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K
SMC_LID	R5916	10K
SMC_EXCARD_OC_L	R5831	10K
SMC_XDP_TCK_3_3	R5934	1K
SMC_CPU_RESET_3_3_L	R5933	1K
SMC_EXCARD_CP	R5830	10K
SMC_CASE_OPEN	R5917	10K

POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP

SELECT TPM GPIO

SMC_TPM_GPIO — 0 R5920 SMC_TPM_GPIO1 — TPM_GPIO1

SMC_TPM_GPIO — 0 R5921 SMC_TPM_GPIO2 — TPM_GPIO2

5% 1/16W MF-LF 402

HDD ACTIVITY MONITOR

PP5V_S0

M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING

TP_SB_SATALED_L — PU_HDD_ACTIVITY_LED — R5960 10K

MAKE_BASE=TRUE

SMC_TPM_PP — R5995 0 5% 1/16W MF-LF 402 — TPM_PP

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

GND_NEXT_TO_SMC — XW5900 SM — OMIT

M51 SPECIFIC: GPU MONITORING SIGNALS

I327: SMC_XDP_TMS — MXM_AC_BATT_L

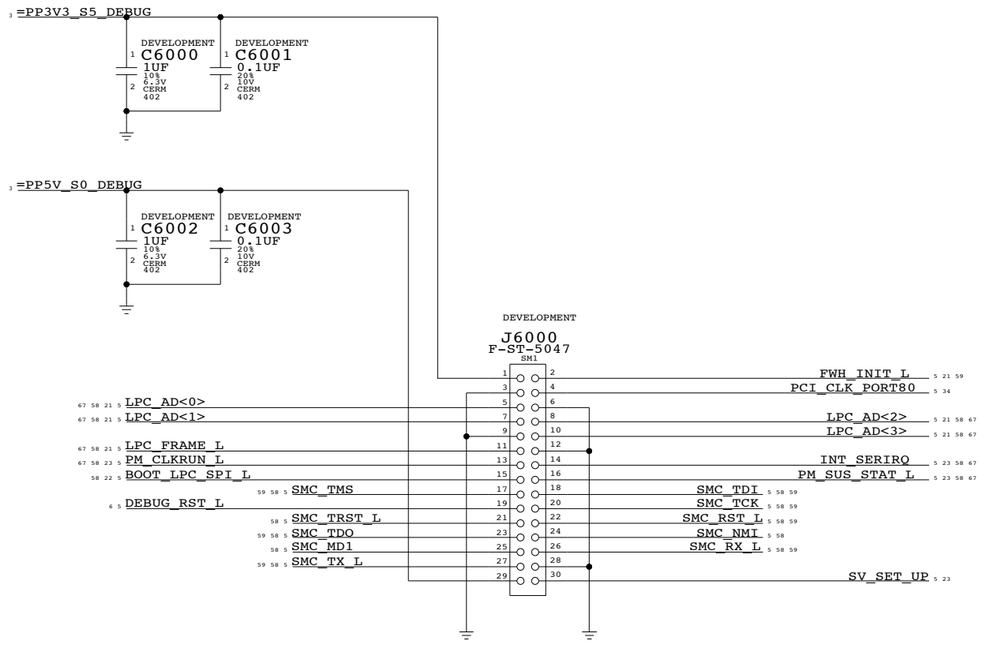
I328: SMC_XDP_TDO_3_3 — GPU_OVERTEMP_L

SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY SYNC_DATE=07/31/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 59 OF 97	

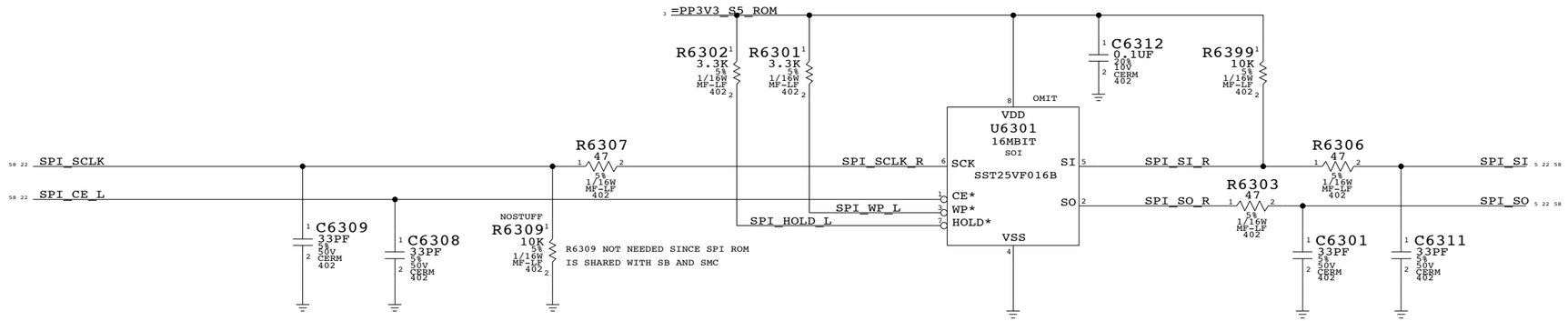


LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 60 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

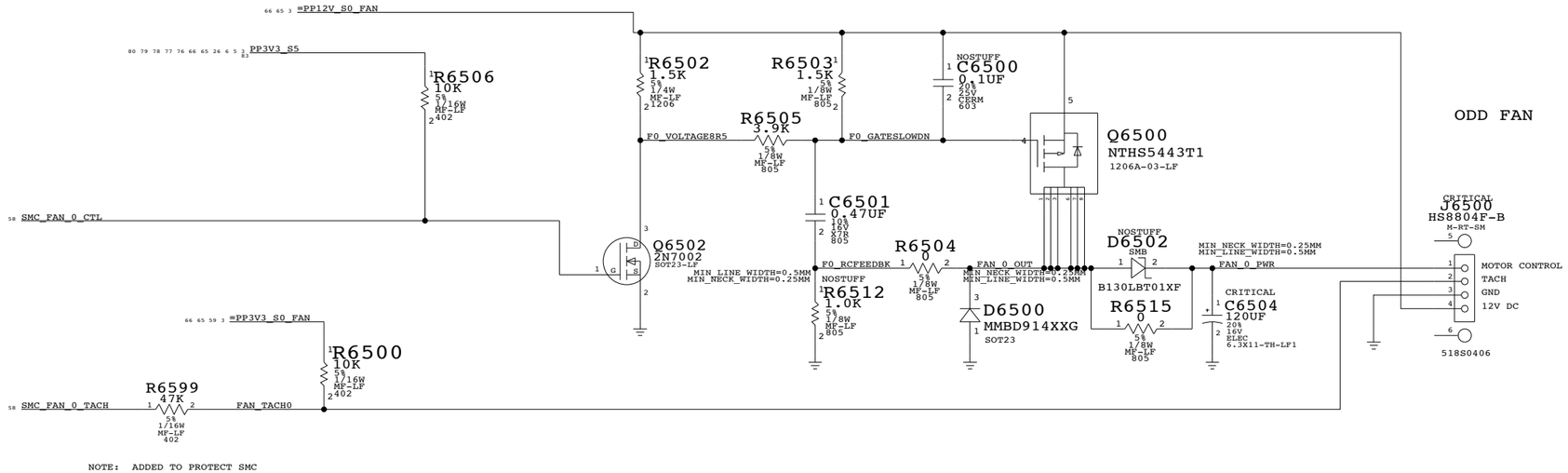
SPI BOOTROM

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

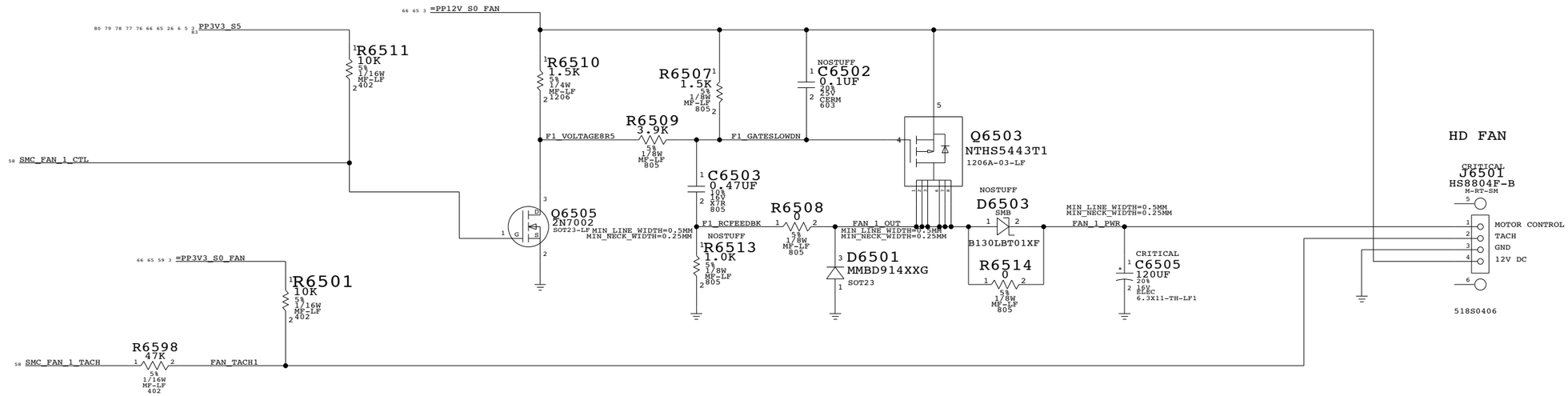
SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 63 OF 97	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



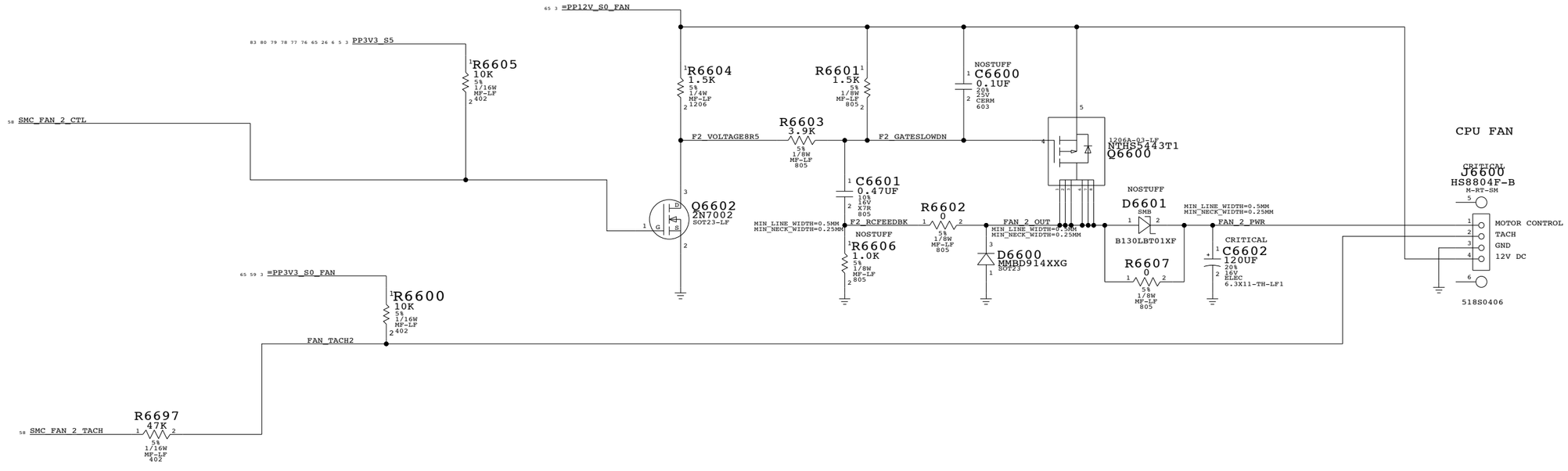
HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

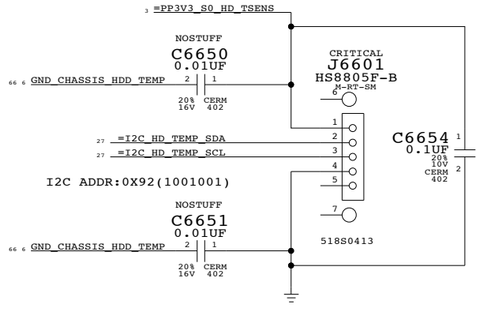
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 65 OF 97	

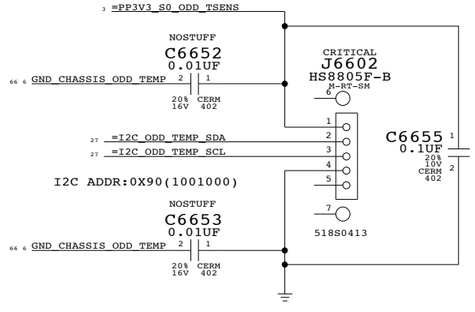
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR

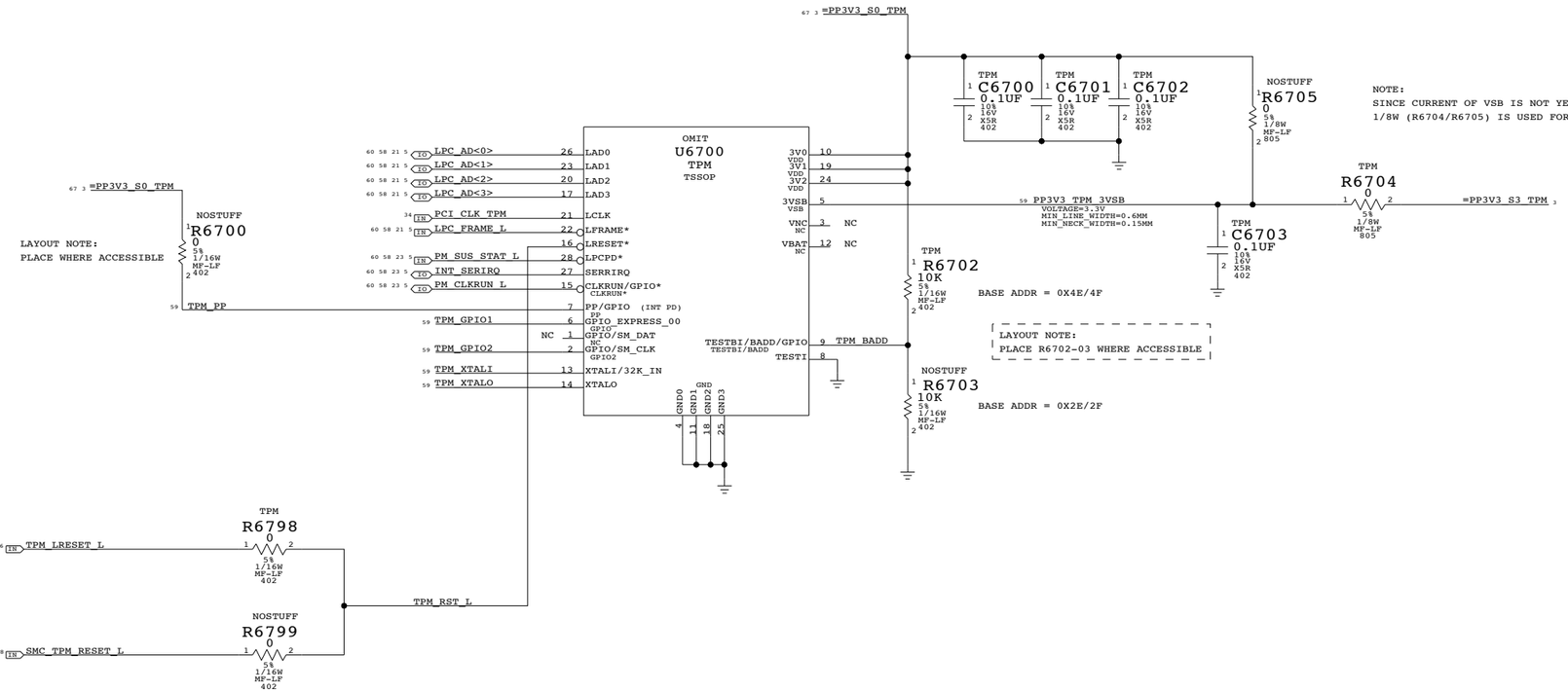


CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 66 OF 97	



TPM

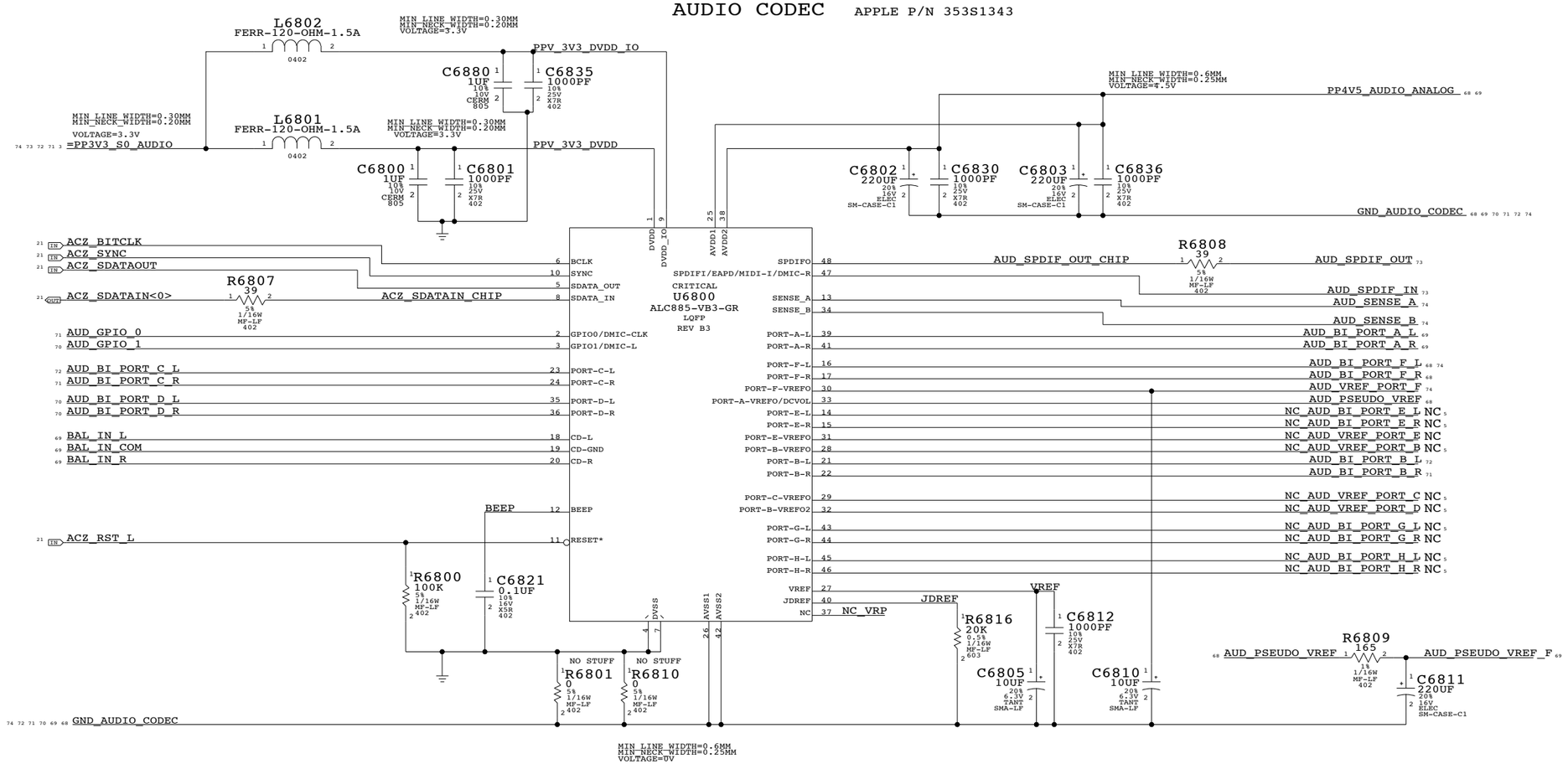
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

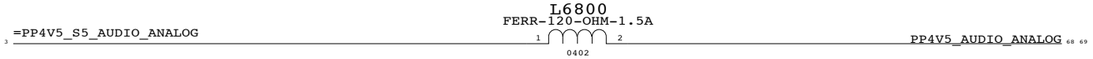
SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 67 OF 97	

AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



MIC INPUT TO BOTH L&R

AUD_BI_PORT_F_L = AUD_BI_PORT_F_R

AUDIO: CODEC			
SYNC_MASTER=AUDIO	SYNC_DATE=08/04/2006		
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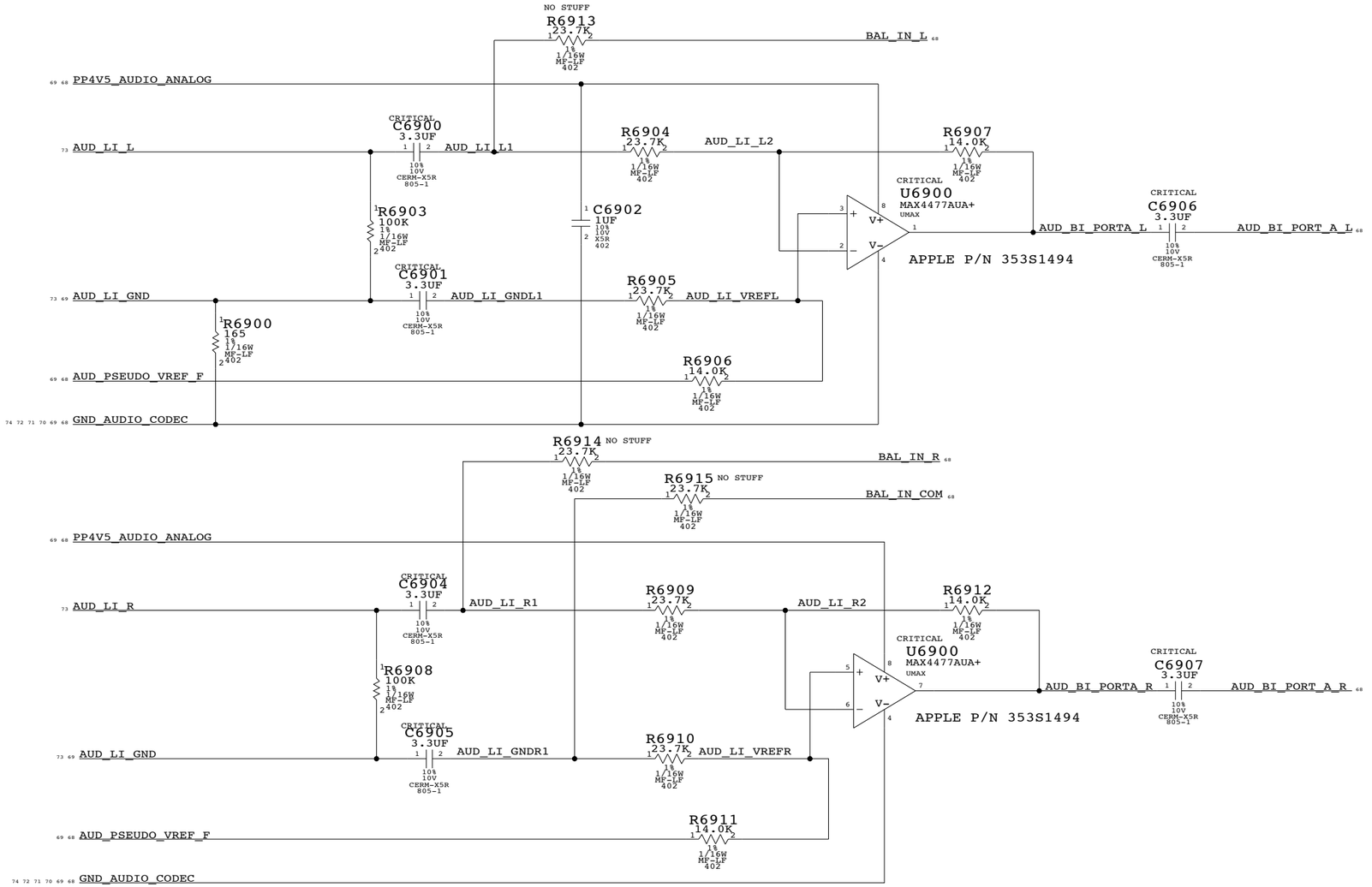
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 68 OF 97	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



AUDIO: LINE INPUT AMP

APPLE COMPUTER INC.

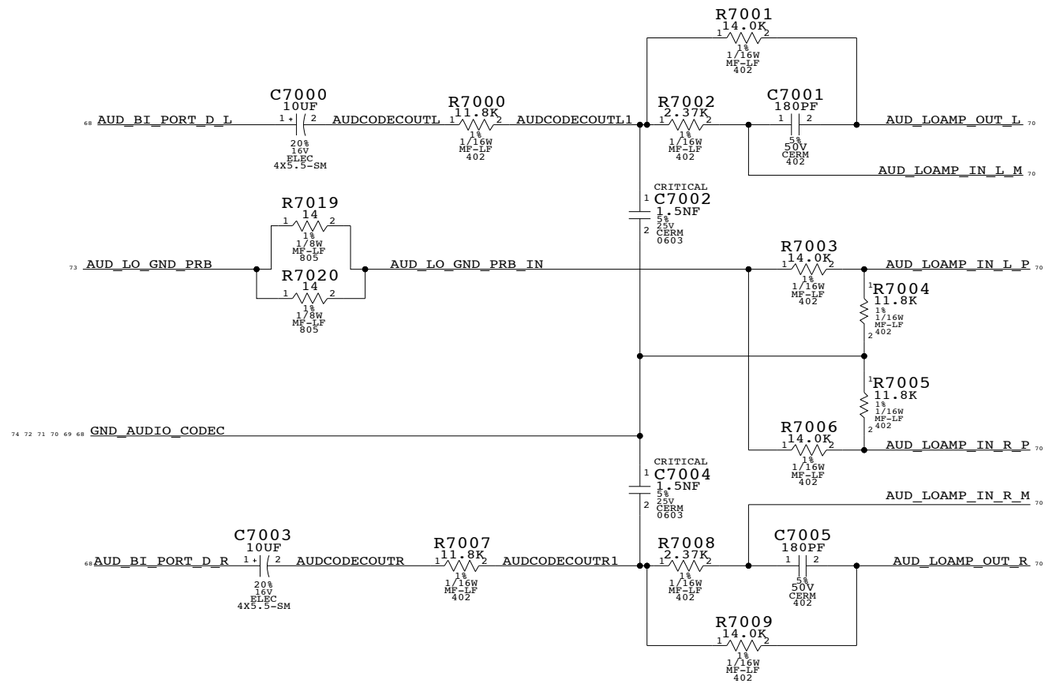
SIZE	DRAWING NUMBER	REV.
D	051-7039	M

SCALE: NONE

SHT 69 OF 97

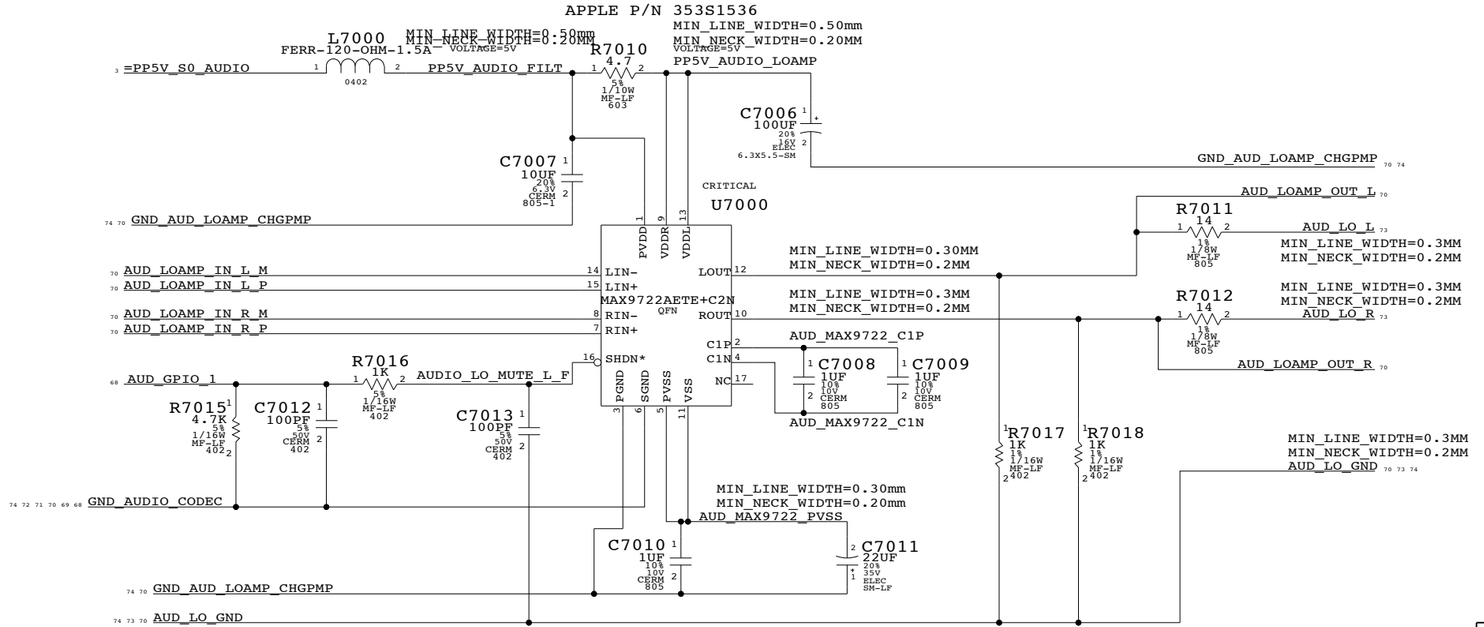
LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18



LINE OUT AMP

APPLE P/N 353S1536



AUDIO: COMBO OUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 70 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
PP12V_AUD_SPKRAMP_PLANE

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
=PP12V_S5_AUDIO_SPKRAMP → R7170 0.005 1% 1/4W MF-LF 1206 → 12V_S5_SPKRAMP

L7122 FERR-250-OHM SM-1
L7100 FERR-250-OHM SM-1

C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V X5R-CERM 1210
C7118 0.1UF 20% 16V CERM 603

GND_AUDIO_SPKRAMP_PLANE

C7102 1UF 10% 35V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V X5R-CERM 1210
GND_AUDIO_SPKRAMP_PLANE

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

AUD_BI_PORT_C_R → L7105 1000-OHM-200MA 0603 → AUDSAMPINLN
C7104 0.47UF 10% 16V X7R 805
C7115 100PF 5% 50V CERM 402

AUD_BI_PORT_B_R → L7108 1000-OHM-200MA 0603 → AUDSAMPINRN
C7107 0.47UF 10% 16V X7R 805

L7106 1000-OHM-200MA 0603 → AUDSAMPINLP
C7105 0.47UF 10% 16V X7R 805

L7107 1000-OHM-200MA 0603 → AUDSAMPINRP
C7106 0.47UF 10% 16V X7R 805
C7116 100PF 5% 50V CERM 402

GND_AUDIO_CODEC

=PP3V3_S0_AUDIO → R7114 47K 5% 1/16W MF-LF 402 → AUD_SAMP_SHDN_L
AUD_SPKRAMP_MUTE
=PP3V3_S0_AUDIO → R7115 47K 5% 1/16W MF-LF 402

AUD_GPIO_0 → R7113 47K 5% 1/16W MF-LF 402 → AUD_SPKRAMP_MUTE_L
Q7100 2N7002DW-X-F SOT-363
R7112 4.7K 5% 1/16W MF-LF 402
C7120 100PF 5% 50V CERM 402
C7121 100PF 5% 50V CERM 402
C7190 100PF 5% 50V CERM 402
GND_AUDIO_CODEC
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
SPKRAMP_SS
Q7100 2N7002DW-X-F SOT-363
C7114 1UF 10% 25V X5R 603

C7109 0.47UF 10% 16V X7R 805

NOSTUFF
R7119 0 5% 1/16W MF-LF 402

U7100 MAX9714 QFN-LF (CRITICAL)

VDD	3, 4, 21, 22		
AUD_SAMP_INL_N	9	INL-	
AUD_SAMP_INL_P	10	INL+	
AUD_SAMP_INR_P	16	INR+	
AUD_SAMP_INR_N	15	INR-	
AUD_SAMP_G1	17	G1	
AUD_SAMP_G2	18	G2	
AUD_SAMP_FS1	19	FS1	
AUD_SAMP_FS2	20	FS2	
AUD_SAMP_SHDN_L	11	SHDN*	
	8	NC	
AUD_MAX9714_VREG	14	REG	
	13	AGND PAD	
	33	THM	
	1, 2, 23, 24	PGND	
	12	SS	
	7	CHOLD	
	31, 32	OUTL+	
	29, 30	OUTL-	
	6	C1+	
	5	C1-	
	27, 28	OUTR+	
	25, 26	OUTR-	

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP
C7108 0.1UF 10% 50V X7R 603-1
AUDSAMPCPN

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP → L7101 180-OHM-1.5A 0603-LF → AUD_SPKR_OUTCR_P
AUDSAMPOUTLN → L7102 180-OHM-1.5A 0603-LF → AUD_SPKR_OUTCR_N
AUDSAMPOURTP → L7103 180-OHM-1.5A 0603-LF → AUD_SPKR_OUTBR_P
AUDSAMPOUTRN → L7104 180-OHM-1.5A 0603-LF → AUD_SPKR_OUTBR_N

C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402

XW7102 SM OMIT
XW7101 SM OMIT
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO → RP7100 47K 5% 1/16W SM-LF (pins 8, 7, 6, 5 / 1, 2, 3, 4)

AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1

NOSTUFF R7118 0 5% 1/16W MF-LF 402
NOSTUFF R7108 0 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO
SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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SCALE: NONE	SHT 71 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP
R7270 0.005 1% 1/4W MF-LF 1206
12V_S5_SPKRAMP1
L7222 FERR-250-OHM SM-1
L7200 FERR-250-OHM SM-1
PP12V_AUD_SPKRAMP1_PLANE
C7217 470UF 20% 25V ELEC 10X10-SM
C7200 470UF 20% 25V ELEC 10X10-SM
C7201 10UF 10% 16V X5R-CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 25V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V X5R-CERM 1210
GND_AUDIO_SPKRAMP1_PLANE

AUD_BI_PORT_C_L
L7205 1000-OHM-200MA 0603
C7204 0.47UF 10% 16V X7R 805
AUDSAMPINLN1
C7215 100PF 5% 50V CERM 402
AUD_SAMP1_INL_N
AUD_SAMP1_INL_P

GND_AUDIO_CODEC
L7206 1000-OHM-200MA 0603
C7205 0.47UF 10% 16V X7R 805
AUDSAMPINLP1

L7207 1000-OHM-200MA 0603
C7206 0.47UF 10% 16V X7R 805
AUDSAMPINRP1
AUD_SAMP1_INR_P
AUD_SAMP1_INR_N
C7216 100PF 5% 50V CERM 402

AUD_BI_PORT_B_L
L7208 1000-OHM-200MA 0603
C7207 0.47UF 10% 16V X7R 805
AUDSAMPINRN1

=PP3V3_S0_AUDIO
R7214 47K 5% 1/16W MF-LF 402
C7290 100PF 5% 50V CERM 402
GND_AUDIO_SPKRAMP1_PLANE
SPKRAMP1_SS

AUD_SPKRAMP_MUTE
Q7200 2N7002 SOT23-LF
GND_AUDIO_SPKRAMP1_PLANE

GND_AUDIO_CODEC

C7214 1UF 10% 25V X5R 603

CRITICAL
U7200 MAX9714 QFN-LF
VDD
INL- INL+ INR+ INR- G1 G2 FS1 FS2 SHDN* NC REG CHOLD OUTL+ OUTL+ OUTL- OUTL- C1+ C1- OUTR+ OUTR+ OUTR- OUTR-
AUD_SAMP1_G1
AUD_SAMP1_G2
AUD_SAMP1_FS1
AUD_SAMP1_FS2
AUD_SAMP1_SHDN_L
AUD_MAX9714_VREG
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
THM PAD AGND PGND SS

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD1

C7209 0.47UF 10% 16V X7R 805

NOSTUFF R7219 0 5% 1/16W MF-LF 402

AUDSAMPOUTLP1
AUDSAMPOUTLN1
AUDSAMPCPP1
AUDSAMPCPN1
C7208 0.1UF 10% 50V X7R 603-1
AUDSAMPOURTP1
AUDSAMPOUTRN1

L7201 180-OHM-1.5A 0603-LF
L7202 180-OHM-1.5A 0603-LF
L7203 180-OHM-1.5A 0603-LF
L7204 180-OHM-1.5A 0603-LF

AUD_SPKR_OUTCL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTBL_N

C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402

XW7202 SM OMIT
XW7201 SM OMIT
GND_AUDIO_SPKRAMP

GND_AUDIO_SPKRAMP1_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

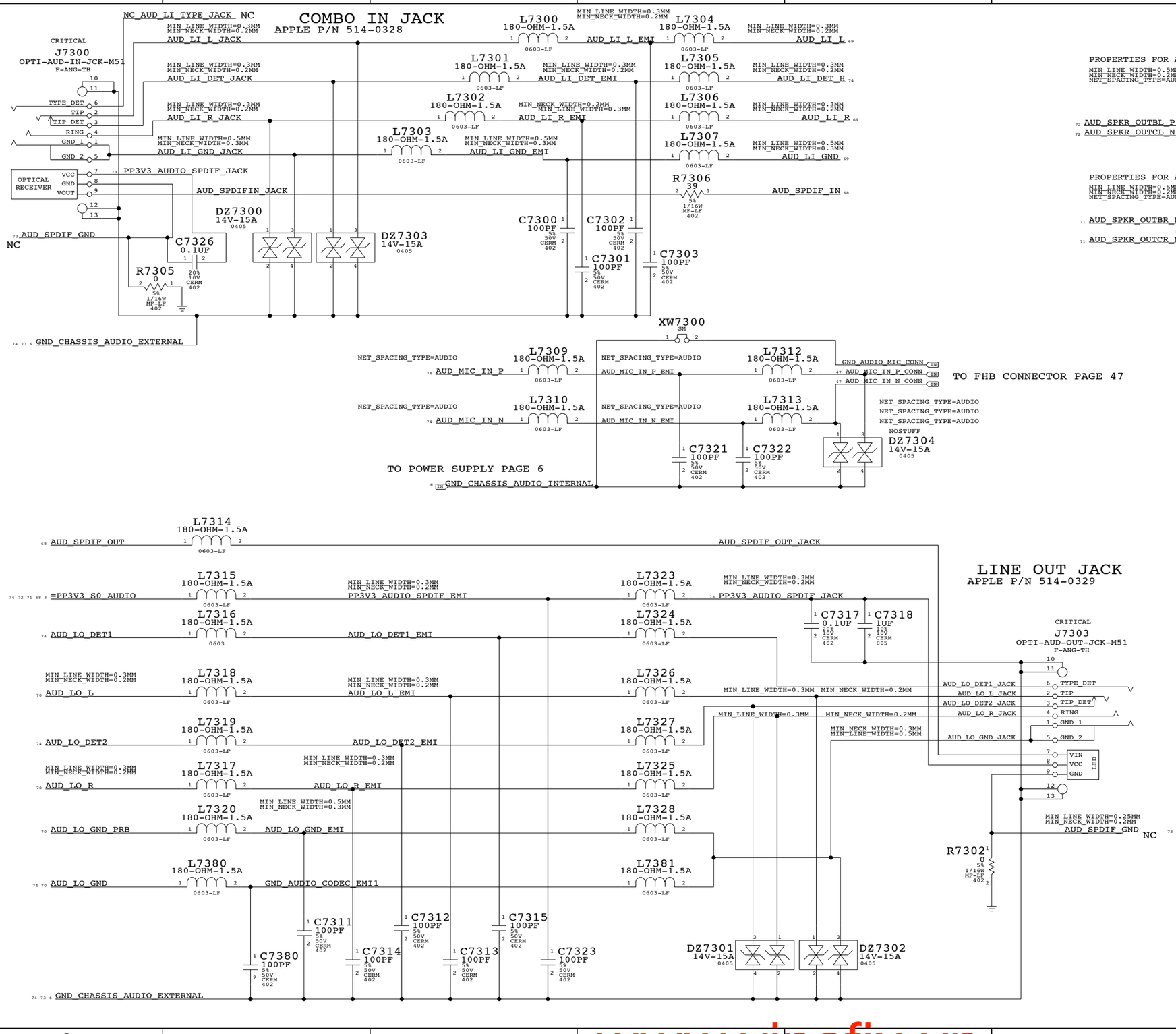
=PP3V3_S0_AUDIO
RP7200 47K 5% 1/16W SM-LF
AUD_SAMP1_FS2
AUD_SAMP1_FS1
AUD_SAMP1_G2
AUD_SAMP1_G1
NOSTUFF R7218 0 5% 1/16W MF-LF 402
NOSTUFF R7208 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP1_PLANE

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 72 OF 97	



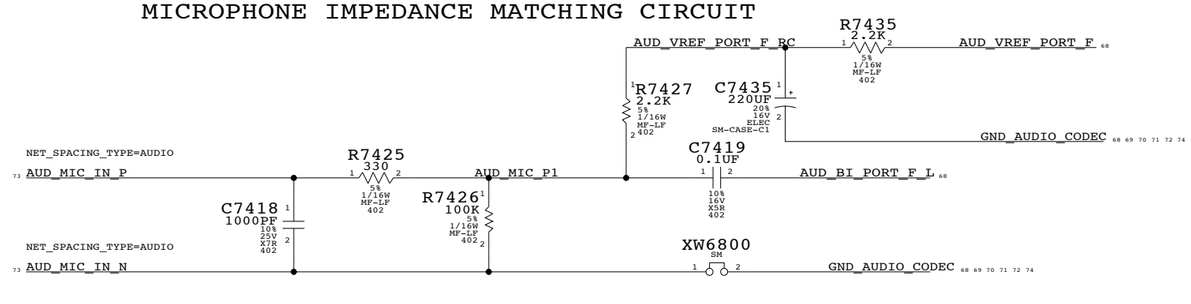
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

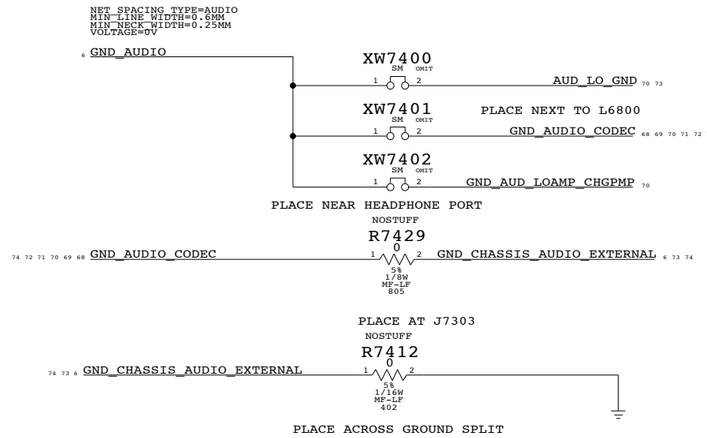
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

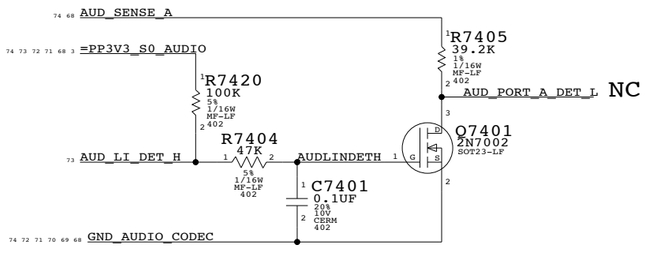
MICROPHONE IMPEDANCE MATCHING CIRCUIT



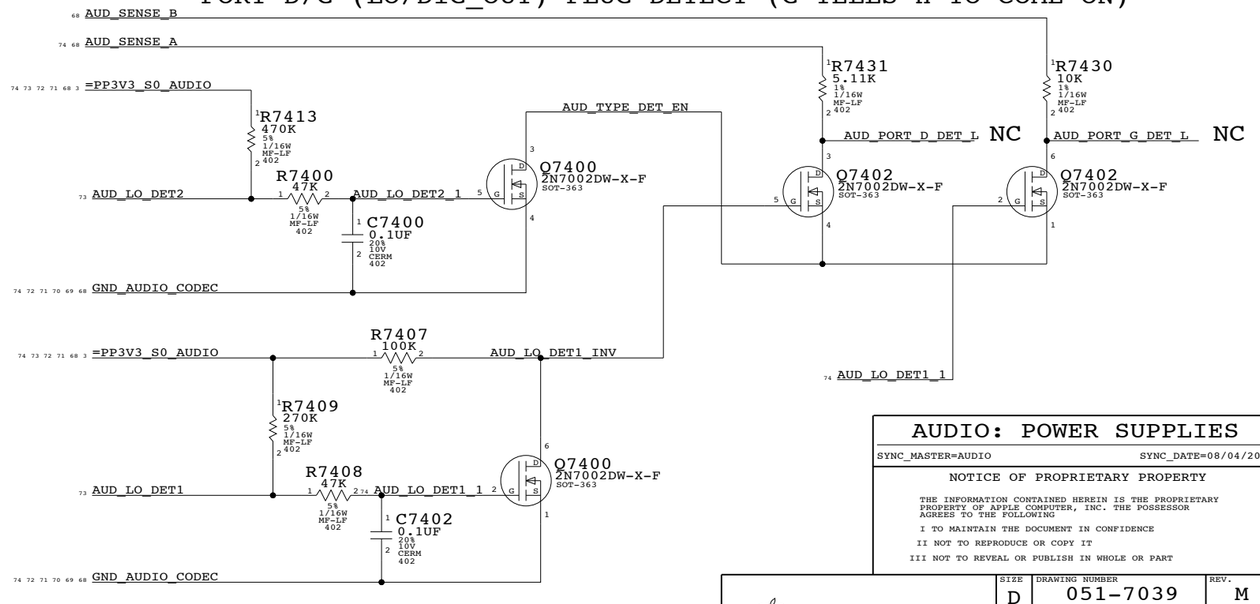
AUDIO GROUND RETURNS



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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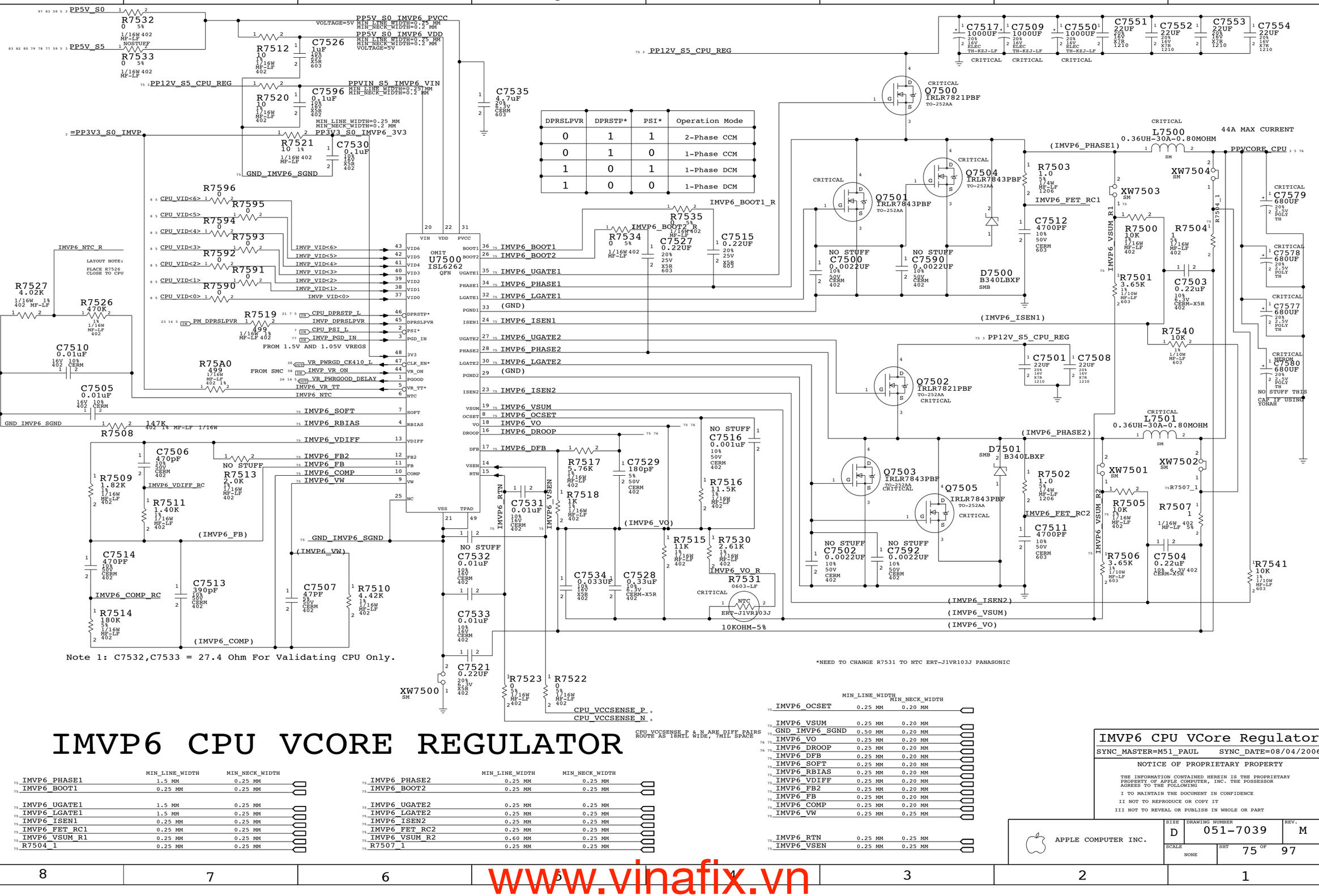
D	051-7039	M
SCALE: NONE	SHT 74 OF 97	



IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

CPU VCCSENSE P & N ARE DIFF PAIRS ROUTE AS 18MIL WIDE, 7MIL SPACE

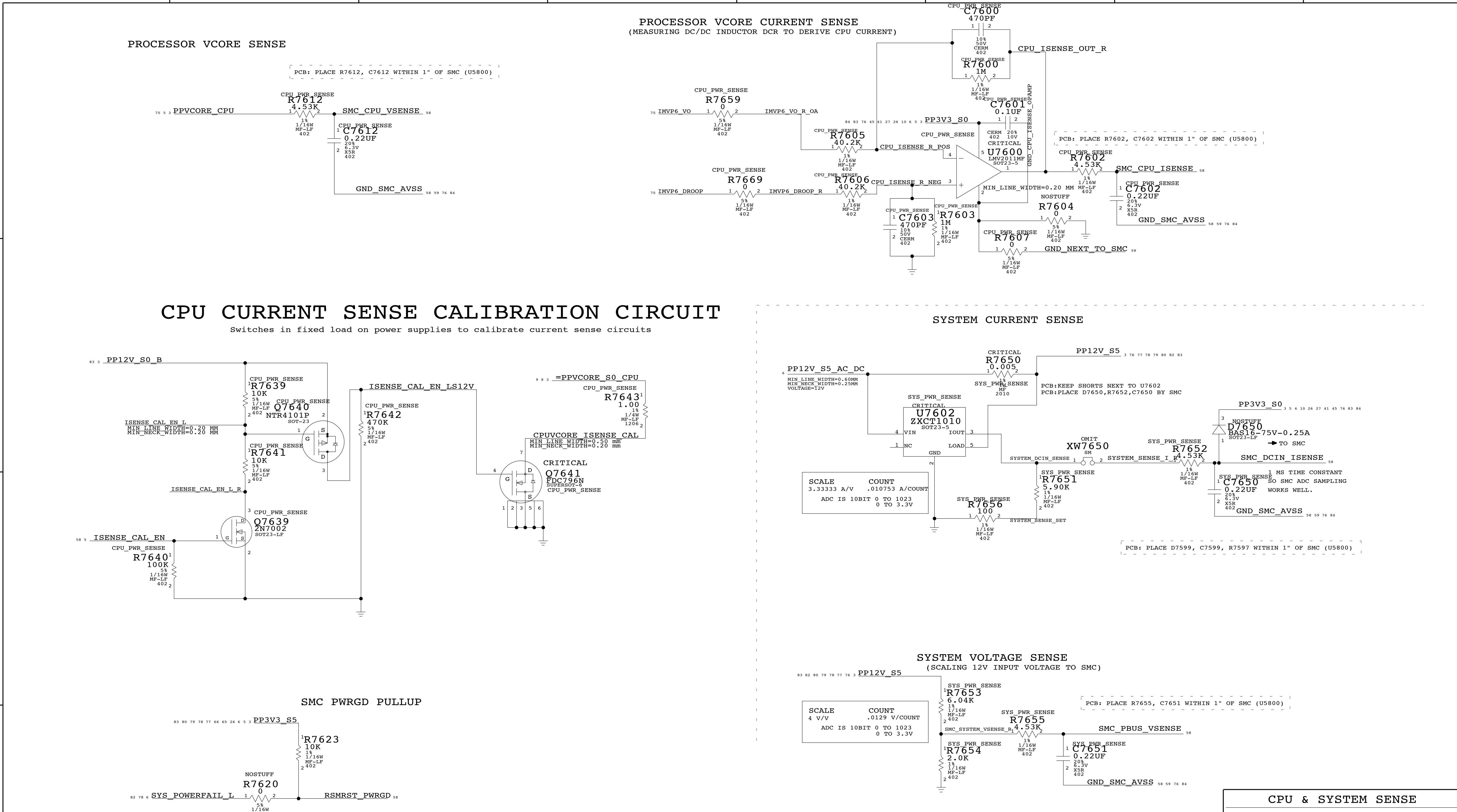
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 75 OF 97	


PROCESSOR VCORE SENSE
PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)
PPVCORE_CPU
CPU_PWR_SENSE
R7612
4.53K
1%
1/16W
MF-LF
402
SMC_CPU_VSENSE
C7612
0.22UF
20%
6.3V
X5R
402
GND_SMC_AVSS
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)
C7600
470PF
R7600
1M
CPU_ISENSE_OUT_R
R7659
0
IMVP6_VO
IMVP6_VO_R_OA
C7601
0.1UF
PP3V3_S0
R7605
40.2K
CPU_ISENSE_R_POS
CRITICAL
U7600
LMV2011MF
SOT23-5
GND_CPU_ISENSE_OPAMP
PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)
R7602
4.53K
SMC_CPU_ISENSE
C7602
0.22UF
R7669
0
IMVP6_DROOP
IMVP6_DROOP_R
R7606
40.2K
CPU_ISENSE_R_NEG
MIN_LINE_WIDTH=0.20 MM
NOSTUFF
R7604
0
C7603
470PF
R7603
1M
R7607
0
GND_NEXT_TO_SMC
CPU CURRENT SENSE CALIBRATION CIRCUIT
Switches in fixed load on power supplies to calibrate current sense circuits
PP12V_S0_B
R7639
10K
Q7640
NTR4101P
SOT-23
ISENSE_CAL_EN_L
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM
ISENSE_CAL_EN_LS12V
R7642
470K
=PPVCORE_S0_CPU
R7643
1.00
1%
1/4W
MF-LF
1206
CPUVCORE_ISENSE_CAL
MIN_LINE_WIDTH=0.50 mm
MIN_NECK_WIDTH=0.20 mm
R7641
10K
ISENSE_CAL_EN_L_R
CRITICAL
Q7641
FDC796N
SUPERSOT-6
Q7639
2N7002
SOT23-LF
ISENSE_CAL_EN
R7640
100K
SYSTEM CURRENT SENSE
CRITICAL
R7650
0.005
PP12V_S5
PP12V_S5_AC_DC
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V
PCB:KEEP SHORTS NEXT TO U7602
PCB:PLACE D7650,R7652,C7650 BY SMC
CRITICAL
U7602
ZXCT1010
SOT23-5
VIN
IOUT
NC
LOAD
GND
PP3V3_S0
NOSTUFF
D7650
BAS16-75V-0.25A
SOT23-LF
TO SMC
OMIT
XW7650
SM
SYSTEM_DCIN_SENSE
SYSTEM_SENSE_I_R
R7652
4.53K
SMC_DCIN_ISENSE
SCALE
3.33333 A/V
COUNT
.010753 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V
R7651
5.90K
R7656
100
SYSTEM_SENSE_SET
C7650
0.22UF
1 MS TIME CONSTANT
SO SMC ADC SAMPLING
WORKS WELL.
GND_SMC_AVSS
PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)
PP12V_S5
R7653
6.04K
SCALE
4 V/V
COUNT
.0129 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V
PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)
R7655
4.53K
SMC_SYSTEM_VSENSE_R
SMC_PBUS_VSENSE
R7654
2.0K
C7651
0.22UF
GND_SMC_AVSS
SMC PWRGD PULLUP
PP3V3_S5
R7623
10K
NOSTUFF
R7620
0
SYS_POWERFAIL_L
RSMRST_PWRGD

CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE   SYNC_DATE=(MASTER)

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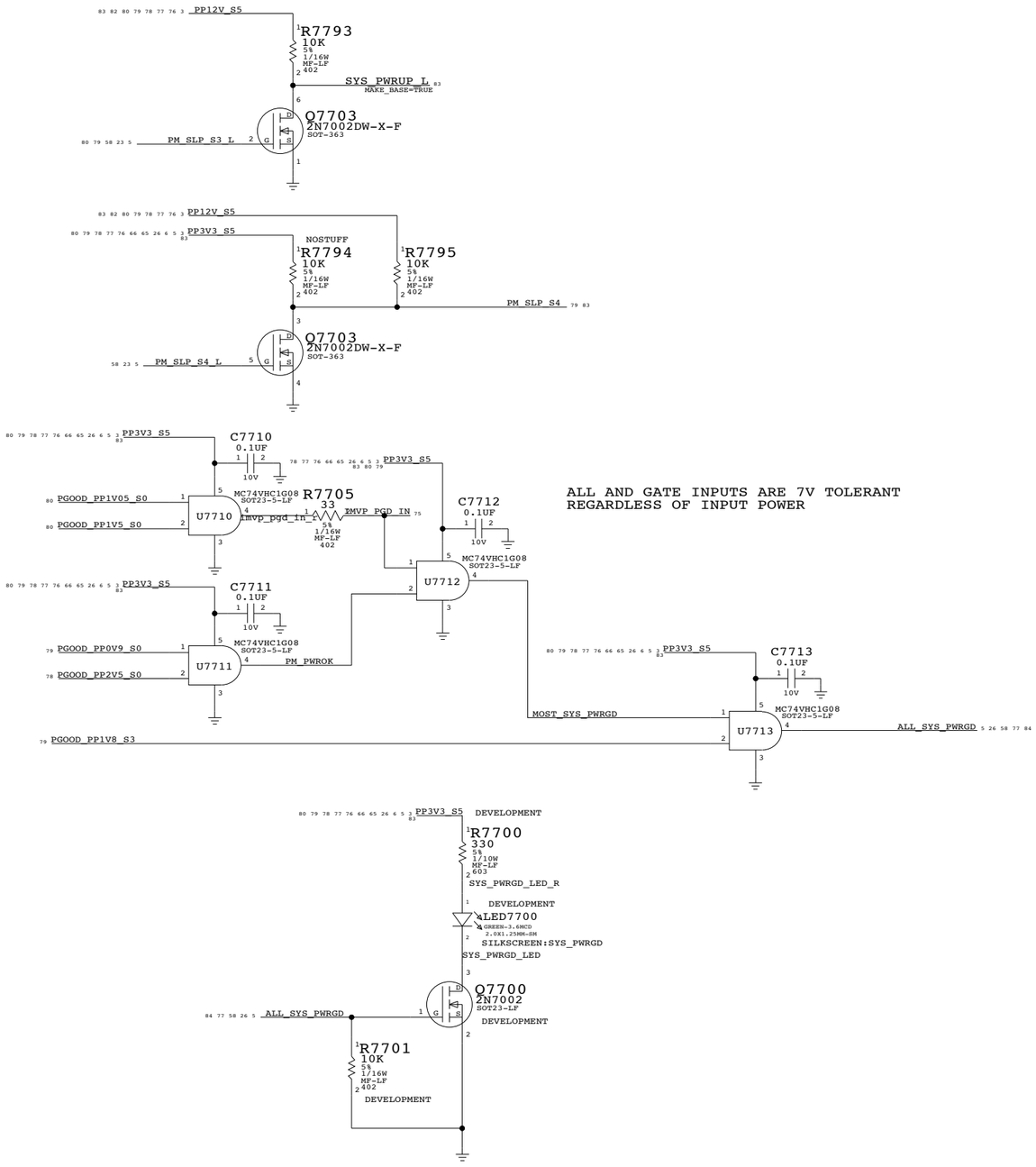
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE NONE	SHT 76 OF 97	



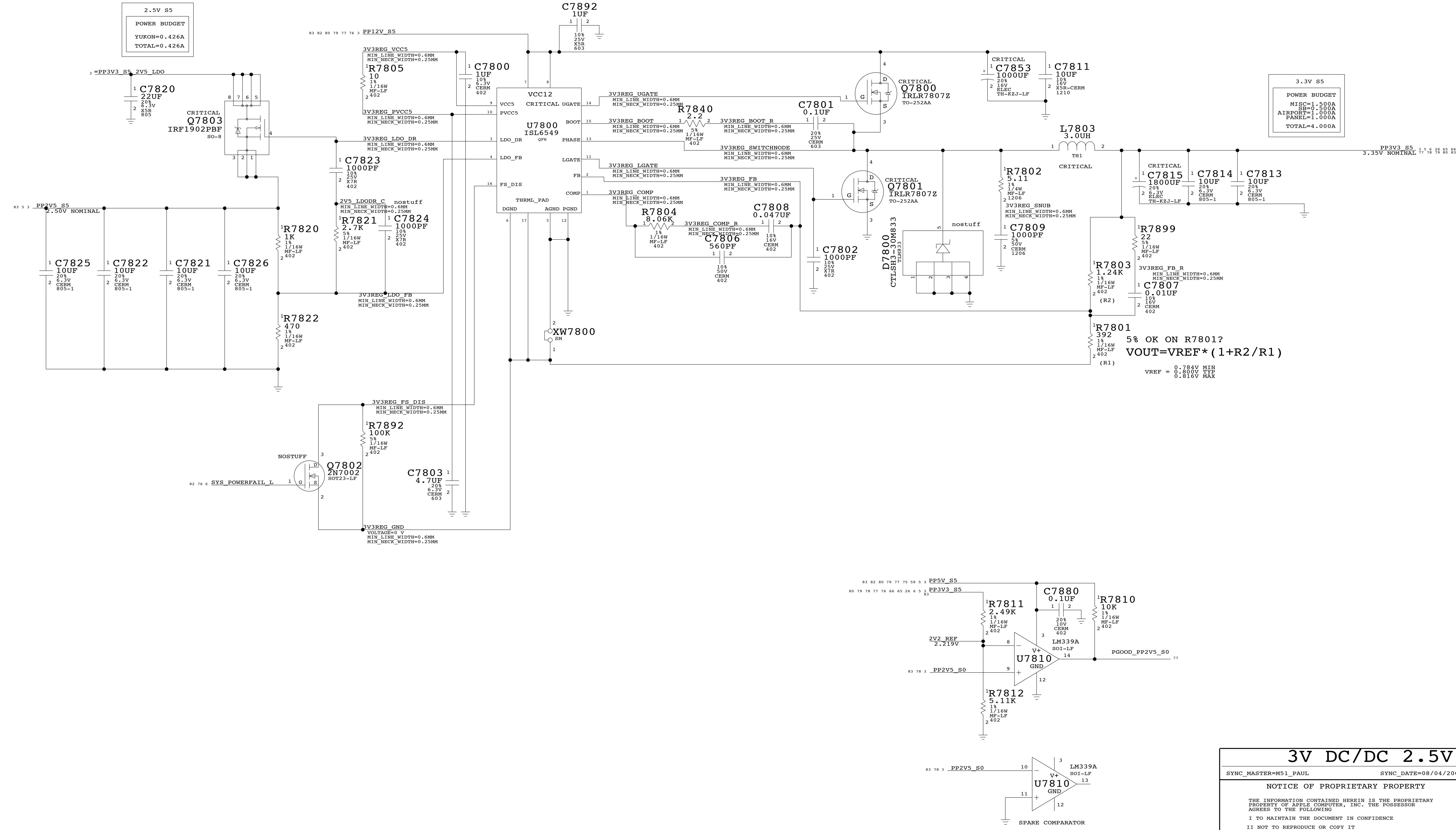
PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 77 OF 97	

3.3V AND 2.5V S5 REGULATOR



2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A
3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A
PP12V_S5
PP3V3_S5_2V5_LDO
PP2V5_S5
2.50V NOMINAL
PP3V3_S5
3.35V NOMINAL
C7892 1UF
C7800 1UF
R7805 10
U7800 ISL6549
VCC12
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND
AGND
PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP
CRITICAL
Q7803 IRF1902PBF
Q7800 IRLR7807Z
Q7801 IRLR7807Z
R7840 2.2
C7801 0.1UF
L7803 3.0UH
C7853 1000UF
C7811 10UF
C7815 1800UF
C7814 10UF
C7813 10UF
R7802 5.11
C7809 1000PF
D7800 CTLSH3-30M833
nostuff
R7899 22
R7803 1.24K
(R2)
C7807 0.01UF
R7801 392
(R1)
5% OK ON R7801?
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN, 0.800V TYP, 0.816V MAX
C7820 22UF
C7823 1000PF
C7824 1000PF
R7821 2.7K
R7820 1K
R7822 470
C7825 10UF
C7822 10UF
C7821 10UF
C7826 10UF
R7804 8.06K
C7806 560PF
C7808 0.047UF
C7802 1000PF
XW7800
R7892 100K
Q7802 2N7002
NOSTUFF
SYS_POWERFAIL_L
C7803 4.7UF
3V3REG_GND
VOLTAGE=0 V
PP5V_S5
PP3V3_S5
R7811 2.49K
C7880 0.1UF
R7810 10K
2V2_REF
2.219V
PP2V5_S0
U7810 LM339A
PGOOD_PP2V5_S0
R7812 5.11K
SPARE COMPARATOR

3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE NONE	SHT 78 OF 97	

1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

=PP1V8_S3_1V2_LDO
C7920 22UF 20% 6.3V X5R 805
CRITICAL Q7903 IRF1902PBF SO-8
PP12V_S5
C7992 1UF 10% 25V X5R 603
C7900 1UF 10% 6.3V CERM 402
1V8REG_DDR_VCC5
R7905 10 1% 1/16W MF-LF 402
1V8REG_DDR_PVCC5
1V8REG_DDR_LDO_DR
C7923 1000PF 10% 25V X7R 402
VCC12
U7900 ISL6549 QFN
CRITICAL
VCC5 PVCC5 LDO_DR LDO_FB FS_DIS
UGATE BOOT PHASE LGATE FB COMP
THRML_PAD DGND AGND PGND
1V8REG_DDR_UGATE
1V8REG_DDR_BOOT
R7940 2.2 5% 1/16W MF-LF 402
1V8REG_DDR_BOOT_R
C7901 0.1UF 20% 25V CERM 603
1V8REG_DDR_SWITCHNODE
1V8REG_DDR_LGATE
1V8REG_DDR_FB
1V8REG_DDR_COMP
R7904 8.06K 1% 1/16W MF-LF 402
C7908 0.047UF 10% 16V CERM 402
C7906 560PF 10% 50V CERM 402
1V8REG_DDR_COMP_R
Q7900 IRLR7807Z TO-252AA
Q7901 IRLR7807Z TO-252AA
D7900 CTLSH3-30M833 TLM833
nostuff
C7902 1000PF 10% 25V X7R 402
L7903 1.53UH CRITICAL TH-LF
R7902 5.11 1% 1/4W MF-LF 1206
1V8REG_DDR_SNUB
C7909 1000PF 5% 50V CERM 1206
CRITICAL C7953 680UF 20% 16V ELEC TH-MCZ
CRITICAL C7954 680UF 20% 16V ELEC TH-MCZ
C7911 10UF 10% 16V X5R-CERM 1210
C7912 10UF 10% 16V X5R-CERM 1210
1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A
CRITICAL C7956 1500UF 20% 6.3V ELEC TH-MCZ
CRITICAL C7957 1500UF 20% 6.3V ELEC TH-MCZ
C7913 10UF 20% 6.3V CERM 805-1
C7958 1UF 10% 6.3V CERM 402
C7959 1UF 10% 6.3V CERM 402
C7960 1UF 10% 6.3V CERM 402
PP1V8_S3 1.81V NOMINAL
PP1V2_S3 1.21V NOMINAL
C7925 10UF 20% 6.3V CERM 805-1
C7922 10UF 20% 6.3V CERM 805-1
C7921 10UF 20% 6.3V CERM 805-1
C7926 10UF 20% 6.3V CERM 805-1
R7920 1K 1% 1/16W MF-LF 402
R7921 2.7K 5% 1/16W MF-LF 402
C7924 1000PF 10% 25V X7R 402
1V2_LDODR_C nostuff
1V8REG_DDR_LDO_FB
R7922 1.96K 1% 1/16W MF-LF 402
XW7900 SM
R7999 22 5% 1/16W MF-LF 402
R7903 1.24K 1% 1/16W MF-LF 402 (R2)
1V8REG_DDR_FB_R
C7907 0.01UF 10% 16V CERM 402
R7901 953 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1V8REG_DDR_FS_DIS
R7992 100K 5% 1/16W MF-LF 402
Q7902 2N7002 SOT23-LF
PM_SLP_S4
C7903 4.7UF 20% 6.3V CERM 603
1V8REG_DDR_GND
VOLTAGE=0 V

PM_SLP_S3_L
MEMVTT_EN

PP5V_S5
PP3V3_S5
R7911 5.49K 1% 1/16W MF-LF 402
R7910 10K 1% 1/16W MF-LF 402
1V2_REF 1.21V
U7810 LM339A SOI-LF GND
PGOOD_PP1V8_S3
R7912 2.7K 5% 1/16W MF-LF 402
R7914 8.45K 1% 1/16W MF-LF 402
R7913 10K 1% 1/16W MF-LF 402
0V7_REF 0.723V
PP0V9_S0
PGOOD_PP0V9_S0
R7915 2.37K 1% 1/16W MF-LF 402

DEVELOPMENT
R7906 330 5% 1/16W MF-LF 402
LED_PP1V8_S3_P
LED7900 GREEN-3.6MCD 2.0X1.25MM-SM
PLACE_LED NEAR VREG
U7901 LM339A SOI-LF GND
1V0_REF
LED_PP1V8_S3_N

1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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1.5V S0 AND 1.05V S0 RAILS

PP1V5_S0
1.50V NOMINAL
C8020 10UF 20% 6.3V CERM 805-1
C8021 10UF 20% 6.3V CERM 805-1
CRITICAL C8022 1500UF 20% 6.3V ELEC TH-MCZ
CRITICAL C8023 1500UF 20% 6.3V ELEC TH-MCZ

1.5V S0
M51
POWER BUDGET
PEAK=5.8A
AVE=2.4A

CRITICAL L8000 1.5UH TH-LF
1V5REG_SWITCHNODE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R8006 5.11 1% 1/4W MF-LF 1206
1V5REG_SNUBBER_R
C8024 1000PF 10% 25V X7R 402

R8001 3.32K 1% 1/10W MF-LF 603
C8012 0.018UF 5% 50V X7R 603
R8002 4.99K 1% 1/10W MF-LF 603
1V5REG_VSEN
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP5V_S5
C8010 4.7UF 20% 6.3V CERM 603

1V5REG_BOOT
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8000 0 5% 1/16W MF-LF 402
CRITICAL Q8000 IRLR7807Z TO-252AA
1V5REG_BOOT_R
C8011 0.1UF 20% 25V CERM 603

BAT54E3 SOT23 D8000
1V5REG_UGATE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8003 2.43K 1% 1/16W MF-LF 402
1V5REG_ISEN
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q8001 IRLR7807Z TO-252AA
1V5REG_LGATE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PM_SLP_S3_L
PGOOD_PP1V5_S0

D8001 CTLSH3-30M833 TLM833 nostuff

CRITICAL U8000 ISL6539 SSOP
VCC
VIN 14
SOFT1 12 ← 1V5REG_SOFT
BOOT1 6
UGATE1 5 → 1V5REG_UGATE
PHASE1 4
ISEN1 7 ← 1V5REG_ISEN
LGATE1 2 → 1V5REG_LGATE
PGND1 3
VSEN1 10
EN1 8 ← PM_SLP_S3_L
PG1 15 → PGOOD_PP1V5_S0
OCSET1 11 ← 1V5REG_OCSET
GND 1 20 9
SOFT2 17 ← 1V05REG_SOFT
BOOT2 23
UGATE2 24 → 1V05REG_UGATE
PHASE2 25
ISEN2 22 ← 1V05REG_ISEN
LGATE2 27 → 1V05_LGATE
PGND2 26
VSEN2 19
EN2 21 ← PM_SLP_S3_L
PG2/REF 16 → PGOOD_PP1V05_S0
OCSET2 18 ← 1V05_OCSET
DDR 13

C8013 0.01UF 10% 50V X7R 603-1
R8004 110K 1% 1/10W MF-LF 603

BAT54E3 SOT23 D8050
1V05REG_BOOT
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8050 0 5% 1/16W MF-LF 402
Q8050 IRLR7807Z TO-252AA
1V05REG_BOOT_R
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8061 0.1UF 20% 25V CERM 603

R8053 2.43K 1% 1/16W MF-LF 402
1V05REG_UGATE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V05REG_ISEN
MIN_NECK_WIDTH=0.25MM
1V05_LGATE
MIN_LINE_WIDTH=0.6MM
PM_SLP_S3_L
PGOOD_PP1V05_S0

Q8051 IRLR7807Z TO-252AA
1V05_SWITCHNODE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

D8051 CTLSH3-30M833 TLM833 nostuff
1V05_OCSET
R8054 110K 1% 1/10W MF-LF 603
C8063 0.01UF 10% 50V X7R 603-1
1V05_VSEN
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP12V_S5
C8000 10UF 10% 16V X5R-CERM 1210
C8001 10UF 10% 16V X5R-CERM 1210
C8002 10UF 10% 16V X5R-CERM 1210
C8003 10UF 10% 16V X5R-CERM 1210
CRITICAL C8004 680UF 20% 16V ELEC TH-MCZ
CRITICAL C8005 680UF 20% 16V ELEC TH-MCZ

1.05V S0
M51
POWER BUDGET
PEAK=8.4A
AVE=4.5A

CRITICAL L8050 1.5UH TH-LF
CRITICAL C8070 1500UF 20% 6.3V ELEC TH-MCZ
CRITICAL C8071 1500UF 20% 6.3V ELEC TH-MCZ
C8072 10UF 20% 6.3V CERM 805-1
C8073 10UF 20% 6.3V CERM 805-1
PP1V05_S0
1.05V NOMINAL

R8056 5.11 1% 1/4W MF-LF 1206
1V05REG_SNUBBER_R
C8064 1000PF 10% 25V X7R 402
R8051 3.65K 1% 1/10W MF-LF 603
C8062 0.018UF 5% 50V X7R 603
R8052 20.0K 1% 1/10W MF-LF 603

PP3V3_S5
DEVELOPMENT R8090 330 5% 1/16W MF-LF 402
LED_PP1V5_S0_P
DEVELOPMENT LED8090 GREEN-3.6MCD 2.0X1.25MM-SM
PP1V5_S0 PP1V5_S0
DEVELOPMENT U7901 LM339A SOI-LF
1V0_REF
LED_PP1V5_S0_N
PLACE_LED NEAR VREG

PP5V_S5
R8005 10K 1% 1/16W MF-LF 402
PGOOD_PP1V5_S0

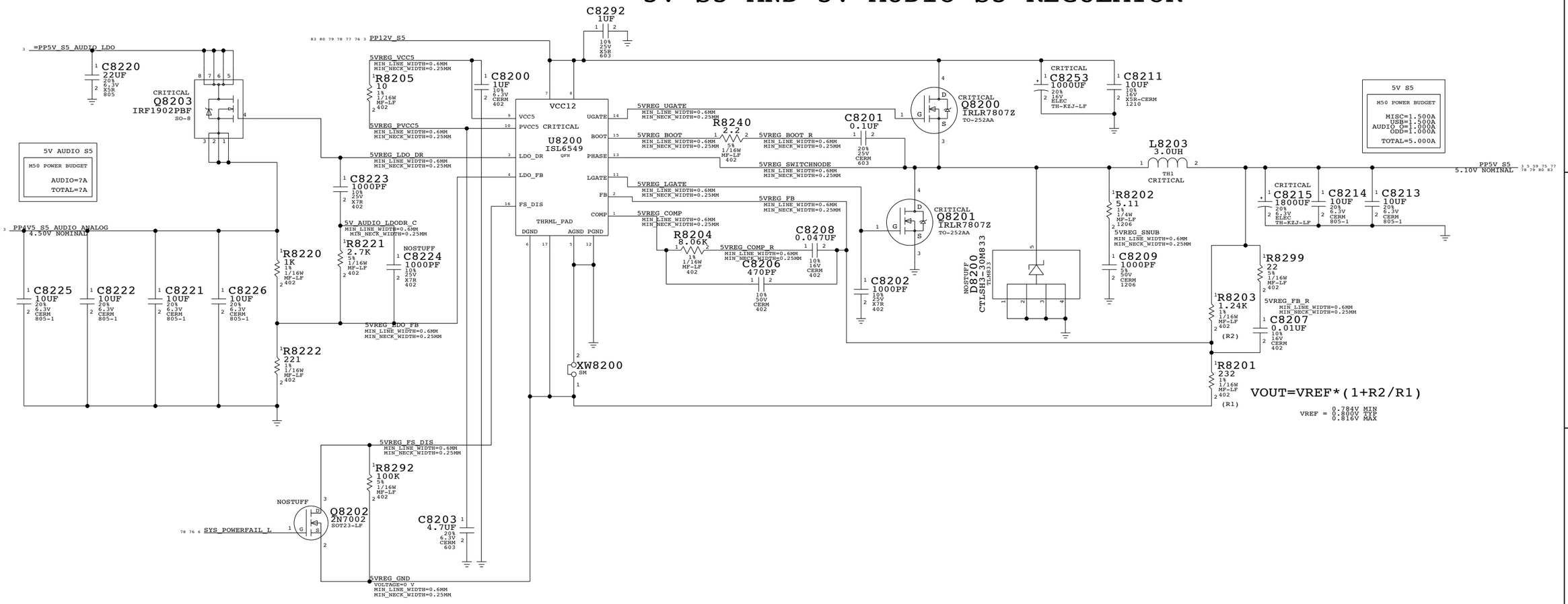
PP5V_S5
R8055 10K 1% 1/16W MF-LF 402
PGOOD_PP1V05_S0

PP3V3_S5
DEVELOPMENT C8090 0.1UF 20% 10V CERM 402
DEVELOPMENT R8091 330 5% 1/16W MF-LF 402
LED_PP1V05_S0_P
DEVELOPMENT LED8091 GREEN-3.6MCD 2.0X1.25MM-SM
PP1V05_S0
PP3V3_S5
DEVELOPMENT U7901 LM339A SOI-LF
LED_PP1V05_S0_N
PLACE_LED NEAR VREG
R8092 8.45K 1% 1/16W MF-LF 402
1V0_REF 0.867V
R8093 3.01K 1% 1/16W MF-LF 402

1.5V_S0 & 1.05V_S0 VREG	
SYNC_MASTER=M51_PAUL	SYNC_DATE=08/04/2006

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 80 OF 97	

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

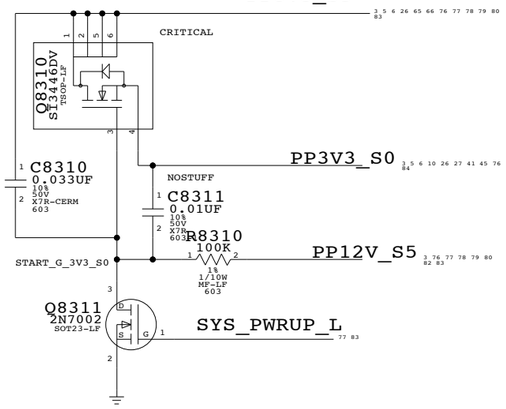
5V DC/DC

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

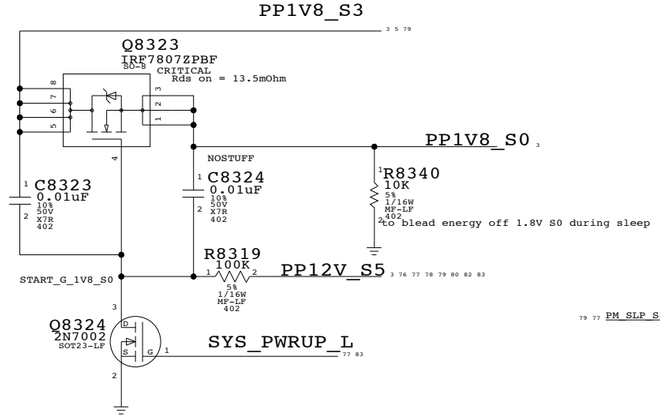
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 82 OF 97	

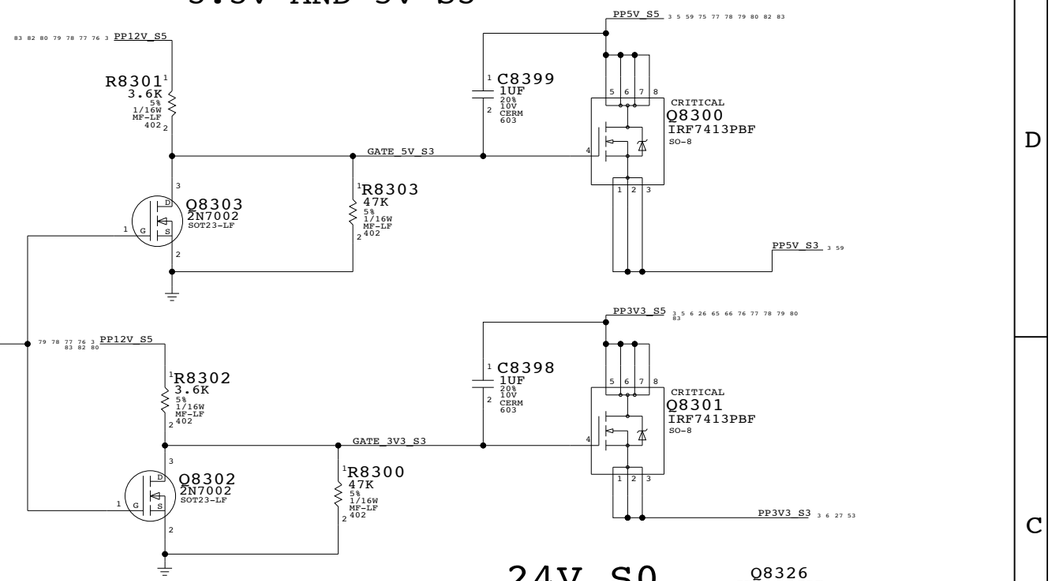
3.3V S0



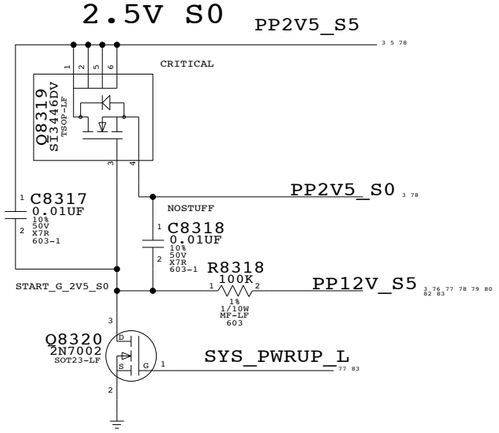
1.8V S0



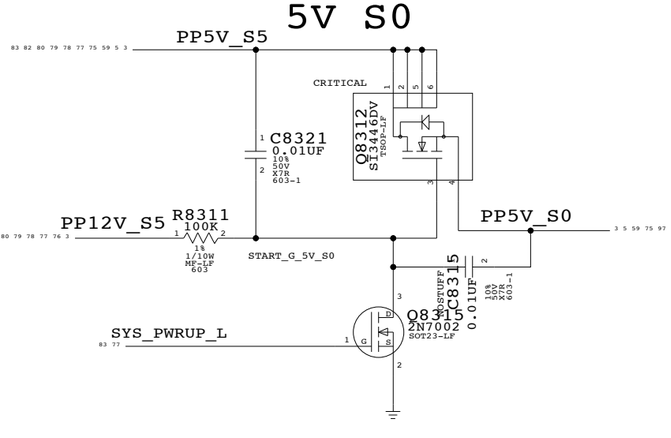
3.3V AND 5V S3



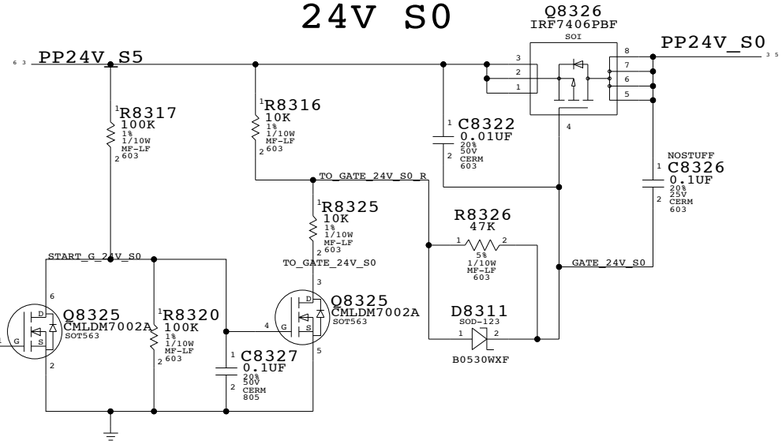
2.5V S0



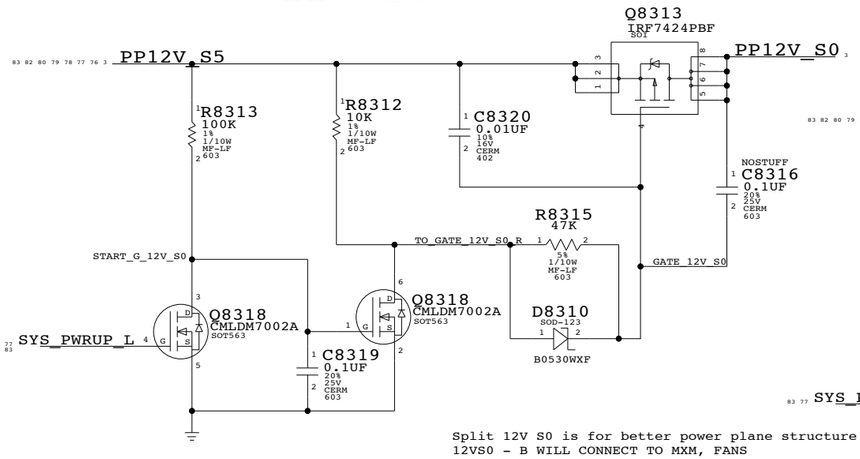
5V S0



24V S0

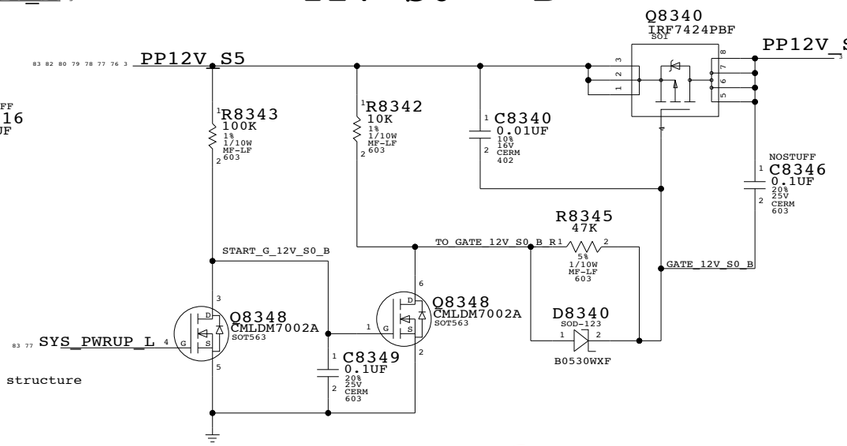


12V S0



Split 12V S0 is for better power plane structure
12VS0 - B WILL CONNECT TO MXM, FANS

12V S0 - B



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 83 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

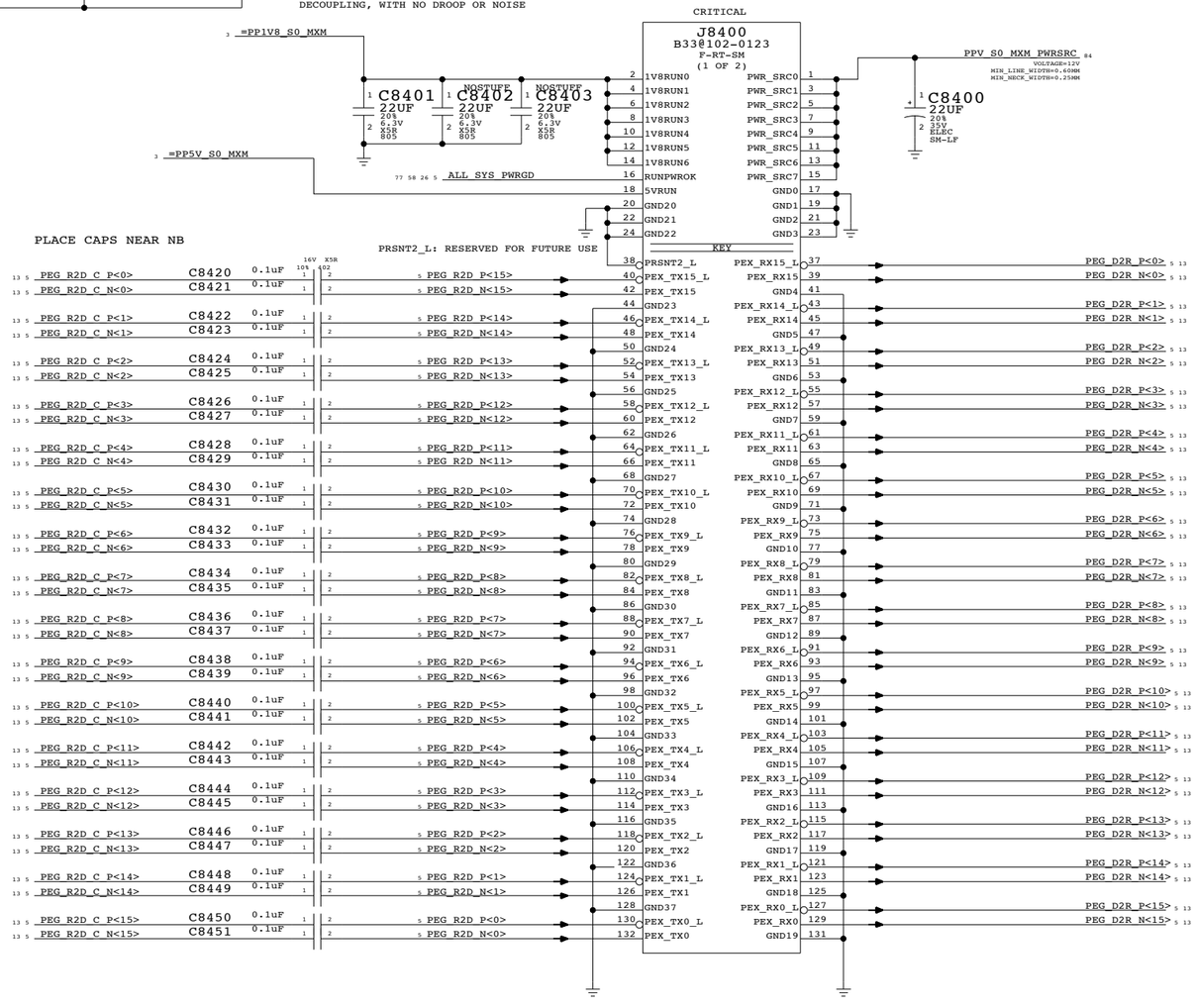
Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS

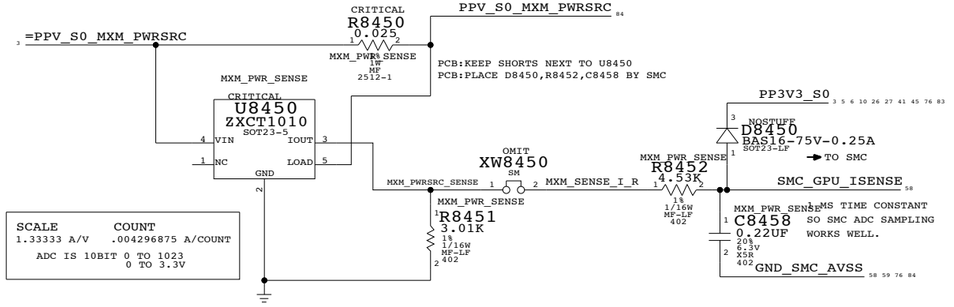
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE



MXM PWRSRC (GPU CORE) CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)

MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 84 OF 97	

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

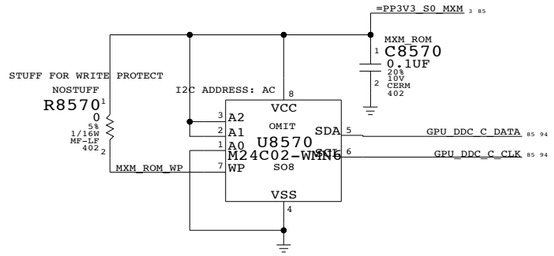
BOM options provided by this page:
(NONE)

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

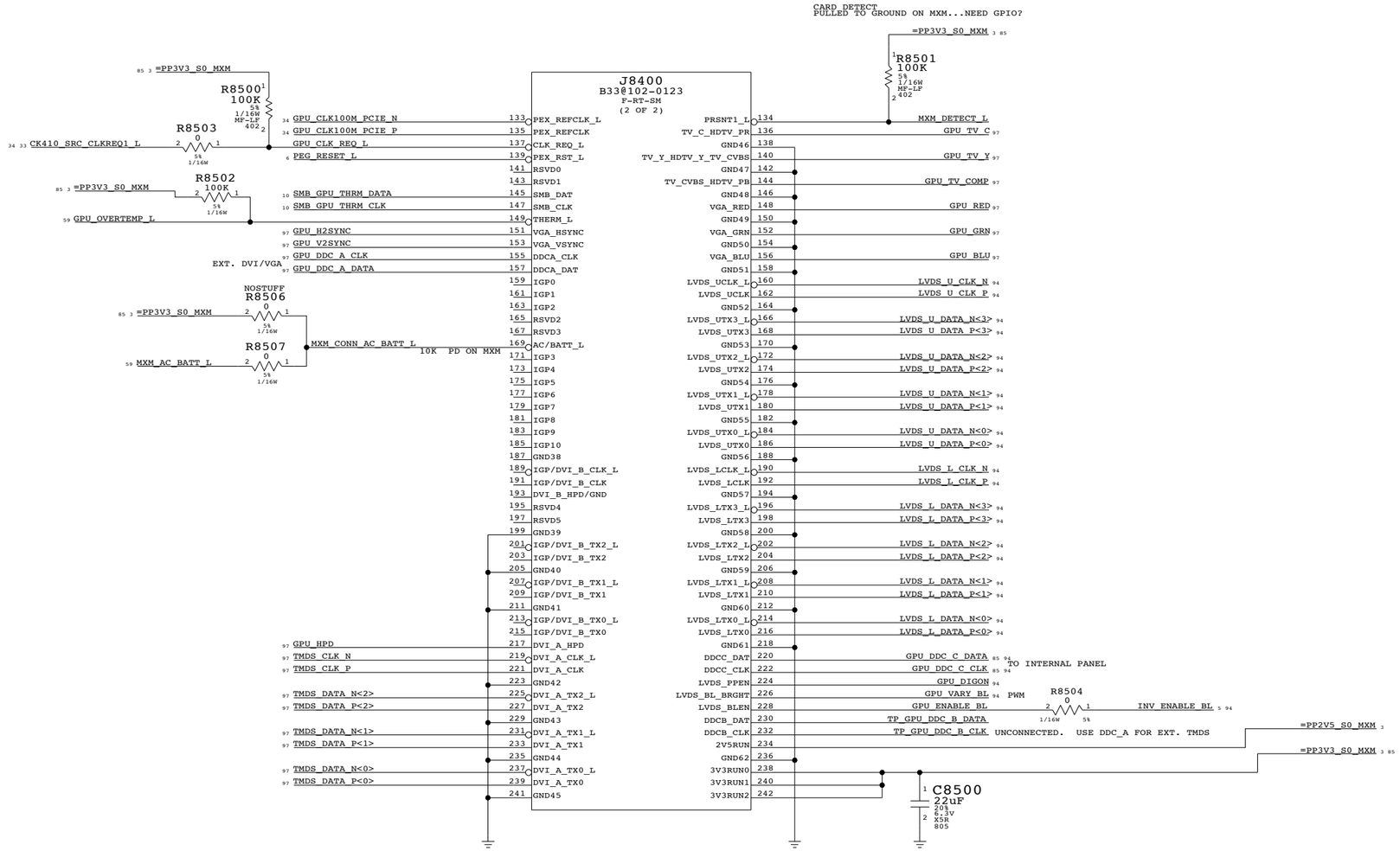
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?



MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 85 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

3 =PPV_S0_LCD

NOSTUFF R9490 0 5% 1/8W MF-LF 805

C9400 0.1UF 10% 50V X7R 603-1

PLACE NEAR J9402

R9400 100K 5% 1/16W MF-LF 402

R9401 29.4K 1% 1/16W MF-LF 402

LCD_PWREN_DIV

LCD_PWREN_L_RC

Q9400 SI3443DV TSOP-LF

PP12V_LCD_SW

L9400 FERR-250-OHM SM

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C9420 10UF 10% 16V X5R-CERM 1210

C9401 0.001uF 20% 50V CERM 402

PP12V_LCD_CONN 6 94

R9499 100K 5% 1/16W MF-LF 402

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

85 GPU_DIGON

R9470 100K 5% 1/16W MF-LF 402

CRITICAL
SDF9400
STDOFF-3MMOD4.6MMH-1.35-TH

CRITICAL
J9402
53307-3072
F-ST-SM

85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85
85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85
85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85
	7	8	LVDS_U_CLK_N 85
85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85
85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85
85 LVDS_L_DATA_P<0>	13	14	
85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85
	17	18	LVDS_L_DATA_N<2> 85
85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85
85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85
94 =PP3V3_DDC_LCD	23	24	
85 LVDS_L_DATA_P<3>	25	26	GPU_DDC_C_DATA 85
85 GPU_DDC_C_CLK	27	28	PP12V_LCD_CONN 6 94
94 6 PP12V_LCD_CONN	29	30	

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9410 0.001uF 20% 50V CERM 402

CRITICAL
SDF9401
STDOFF-3MMOD4.6MMH-1.35-TH

INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS

CRITICAL
J9400
88290-14XG
M-ST-SM

3 =PPV_S0_INVERTER

C9440 2.2UF 10% 50V X7R 1206

97 94 3 =PP3V3_S0_VIDEO

NOSTUFF R9440 10K 5% 1/16W MF-LF 402

85 INV_ENABLE_BL

94 5 LCD_PWM

85 GPU_VARY_BL

R9475 47 5% 1/16W MF-LF 402

NOSTUFF R9474 10K 5% 1/16W MF-LF 402

LCD_PWM 5 94

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

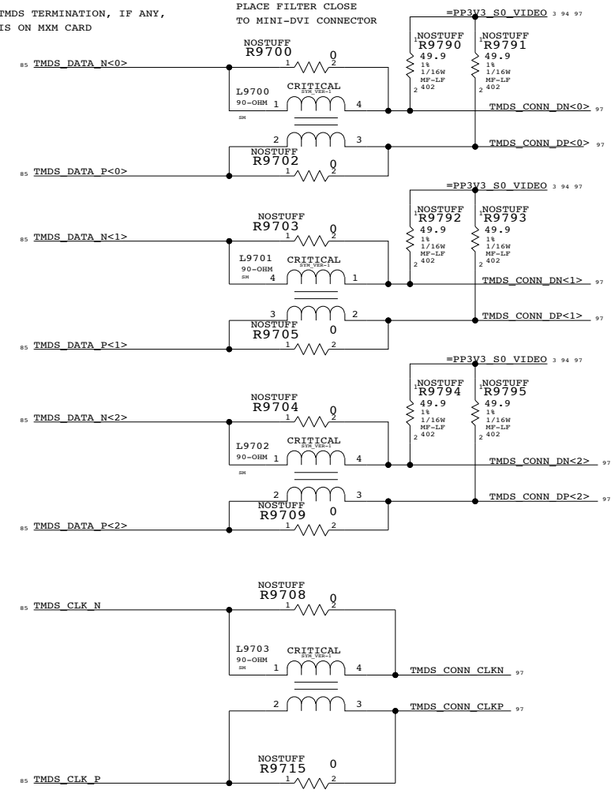
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE: NONE	SHT 94 OF 97	

DVI INTERFACE

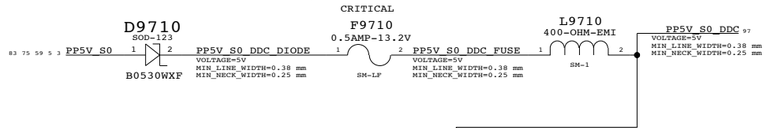
TMDS TERMINATION, IF ANY, IS ON MXM CARD

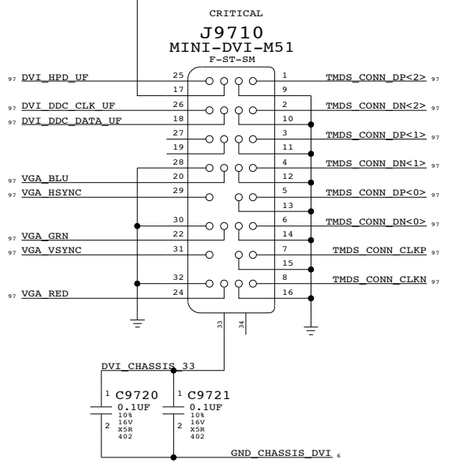
PLACE FILTER CLOSE TO MINI-DVI CONNECTOR



DVI DDC CURRENT LIMIT

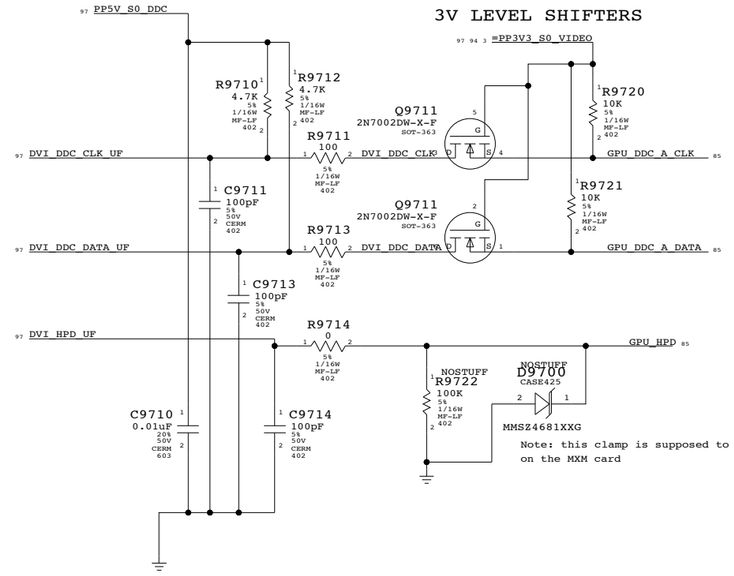
(55mA requirement per DVI spec)





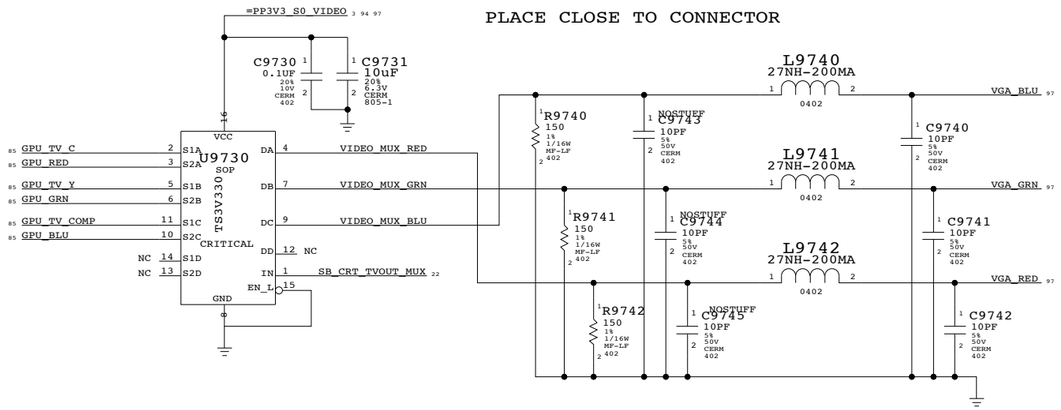
PLACE CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS

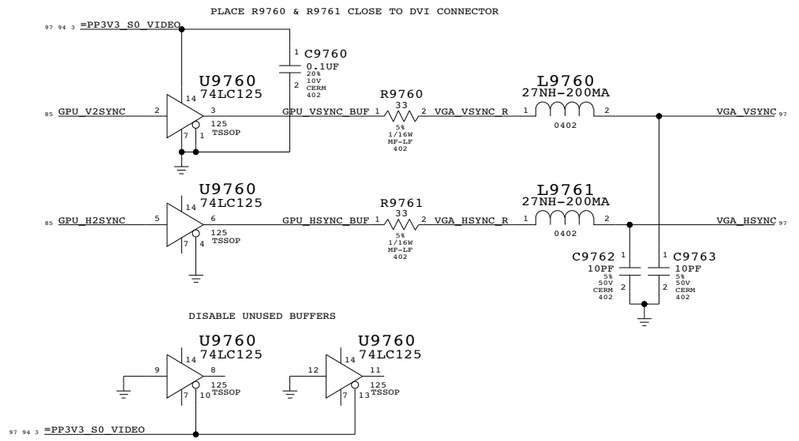


ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



	External Display Conns
SYNC_MASTER=M51_DAVE	SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
	SCALE: NONE	SHT 97 OF 97	