1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,MLB,PROTON-2

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
01		631374	ENGINEERING RELEASED	09/19/08	?

09/19/08

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7867	1	SCHEM,MLB,PROTO2N	SCH	CRITICAL	
820-2510	1	PCBF,MLB.PROTO2N	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Sep 19 16:21:57 2008

DIMENSIONS ARE IN MILLIMETERS
XX ± ____
X.XX ± ____
X.XXX ± ____
ANGLES ± ____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

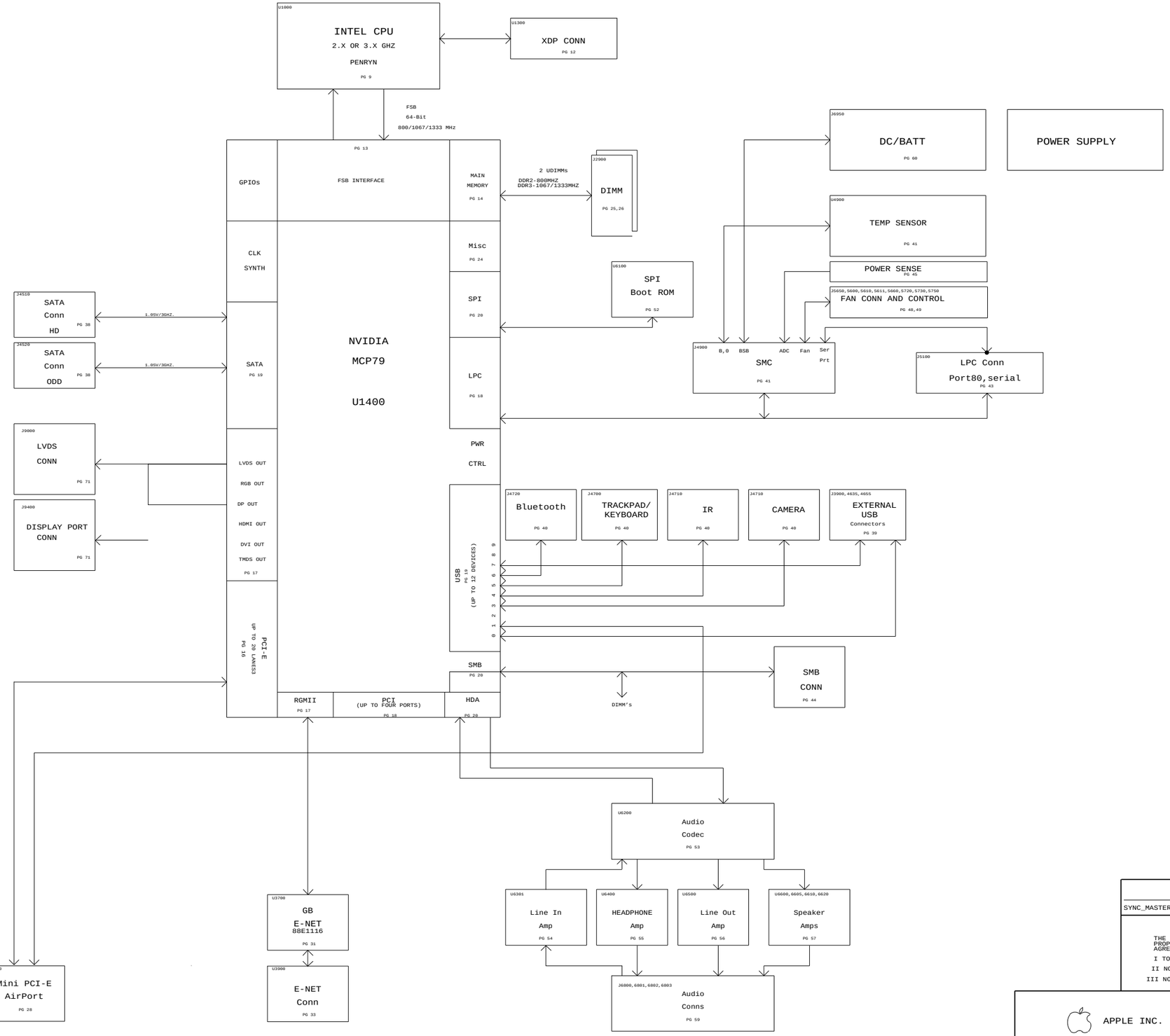
SIZE D

APPLE INC.

TITLE
SCHEMATIC,MLB,PROTON-2

DRAWING NUMBER 051-7867 REV. 01

SHT 1 OF 123



System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	2	123

K20 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(16.5V)
F6905 6A FUSE
R7020
SMC_DCIN_ISENSE
PPDCIN_G3H
R6905
D6905
D6905
U7000 ISL6258A PBUS SUPPLY/ BATTERY CHARGER (PAGE 60)
PPVBAT_G3H_CHGR_REG
F7040
F7041 8A FUSE
R7050 U5303 SMC_BATT_ISENSE
PPBUS_G3H
PPVIN_G3H_P3V42G3H
PPBUS_G3H_VSENSE
Q5315
ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 59)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 42)
SMC_RESET_L
MIC5232-2.8YD5 U2801 (PAGE 25)
PP3V3_G3_RTC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001

J6950
2S4P (6 TO 8.4V)
PPVBATT_G3H_CONN
Q7056 BATT_POS_GATE
Q7055 CHGR_BGATE
PPVBAT_G3H_CHGR_R

GPU VCORE ISL6263C U8900 (PAGE 77)
VIN
VOUT
VR_ON
PGOOD
GPUVCORE_EN
GPUVCORE_PGOOD
U5410
SMC_GPU_ISENSE
SMC_GPU_VSENSE
PPVCORE_GPU
CPUVTTS0_EN
1.05V SC417 U7600 (PAGE 65)
EN_PSV
R7650
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE
CPUVTTS0_PGOOD

SMC_CPU_HI_ISENSE
R5388
CPU VCORE ISL9504B U7100 (PAGE 61)
IMVP_VR_ON
VR_PWRGOOD_DELAY
U7100
SMC_CPU_ISENSE
SMC_CPU_VSENSE
PPVCORE_S0_CPU

MCP_CORE 5V ISL6236 U7500 (PAGE 64)
MCPCORES0_EN
PM_SLP_S3_L_R
EN2
EN1
VOUT2
VOUT1
POK1
POK2
R7505
SMC_MCP_CORE_ISENSE
SMC_MCP_VSENSE
PPVCORE_S0_MCP
PP5V_S0
P5V_RTS0_PGOOD
MCPCORES0_PGOOD

MCP79 U1400 (PAGE 14~22)
MCP_PS_PWRGD
U2850
PWRBTN#
RSTBTN#
PWRGD_SB
PS_PWRGD
CPU_RESET#
CPU_PWRGD
PM_SYSRST_DEBOUNCE_L
FSB_CPURST_L
CPU_PWRGD

CPU U1000 (PAGE 10,11)
PWRGOOD
RESET*

GMUX U9600 XP28 (PAGE 84)
PB16B EG_RAIL1_EN P1V1GPU_EN
PB17A EG_RAIL2_EN P3V3GPU_EN
PB17B EG_RAIL3_EN GPUVCORE_EN
PB18A EG_RAIL4_EN P1V8_S0GPU_EN
PL32A PM_ALL_GPU_PGOOD

SMC U4900 (PAGE 42)
P60
SMC_PM_G2_EN
RC DELAY P3V3S5_EN
RC DELAY PM_G2_P1V05S5_EN

P1V1_GPU_EN
P1V8_S0GPU_EN
EN1 VIN VOUT1 1.103V(L/H)
EN2 VOUT2 1.8V(R/H)
ISL6236 U9500 (PAGE 83)
POK1 P1V1GPU_PGOOD
POK2 PM_ALL_GPU_PGOOD
PP1V1_S0GPU
R5413
PP1V8_S0GPU_ISNS
SMC_GPU_1V8_ISENSE
DDRREG_EN
MEM_VTT_EN
VIN 1.5V VLDOIN
S5 VOUT1 PP1V8R1V5_S3
S3 0.75V VOUT2 PP0V9R0V75_S0_DDRVTT
TPS51116 U7300 (PAGE 63)
Q7901
SMC_MCP_DDR_ISENSE
PPMCPDDR_ISNS
PP1V8R1V5_S0
MCPDDR_EN

MCP79 U1400 (PAGE 14~22)
SLP_RMGT#(J17)
PCI_RESET0#(R10)
SLP_S5#(H17)
SLP_S3#(G17)
PM_SLP_RMGT_L
MEM_VTT_EN
R2870
DDRREG_EN
P5VS3_EN
PM_SLP_S4_L
PM_SLP_S3_L
R7878
PM_SLP_S3_L_R
RC DELAY P1V8S0_EN
RC DELAY MCPDDR_EN
RC DELAY CPUVTTS0_EN
RC DELAY MCPCORES0_EN
RC DELAY P1V05S0_EN
RC DELAY P1V2_S0_EN
RC DELAY P2V5S0_EN

P5VS3_EN
P3V3S5_EN
VIN EN1 VOUT1 5V (L/H)
EN2 VOUT2 3.3V (R/H)
TPS51220 U7201 (PAGE 62)
PGOOD1,2
PP5V_S3
PP3V3_S5
P5V3V3_PGOOD
VIN APP001 U9701 (PAGE 85~86)
BKLT_PLT_RST_L && LCD_BKLT_EN
ENA
VOUT
PPVOUT_S0_LCDBKLT
Q4260
LTC1872 U7790 (PAGE 66)
PP10V_FW
FW_PORTPWR_EN&&(SMC_ADAPTER_EN||PM_SLP_S3_L)
Q7910
Q7930
Q7970
Q3810
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_RMGT_L
PP3V3_S3
PP3V3_S0GPU
P3V3GPU_EN
P3V3_ENET_PHY
R0940
P1V0FW_EN
P1V8S0_EN
LTC3547 U7700 (PAGE 66)
PP1V0_FW
PP1V8_S0
R7894
PM_ALL_GPU_PGOOD
U7880
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P5V3V3_PGOOD
P5V_RTS0_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
S0PGOOD_PWROK
SMC (PAGE 42)
RSMRST_OUT(P15)
99ms DLY
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
SYSRST(PA2)
P17(8TN_OUT)
RES*
PM_RSMRST_L
IMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900 (PAGE 42)

VI TPS62202 U7760 (PAGE 66)
EN
VOUT
PP1V8_S0GPU_EN
PP1V8_GPUIFPX
PP3V3_S0
VCC
U7870 LTC2909 (PAGE 67)
ADJ1
ADJ2
RST*
PP1V8R1V5_S0
PP1V05_S0
TRST = 200mS

P5VS3_EN
P3V3S5_EN
VIN 1.05V AUX ISL6269 U7750 (PAGE 66)
EN
VOUT
PGOOD
PM_G2_P1V05S5_EN
PP1V2R1V05_S5
P1V05_S5_PGOOD
Q7953
PP1V05_S0
P1V05S0_EN
Q3840
PP1V2R1V05_ENET
PM_SLP_RMGT_L

PP3V42_G3H
VDD
U7840 TPS3808G (PAGE 67)
SENSE
RESET*
MR*
PP3V3_S5
RSMRST_PWRGD
P1V05_S5_PGOOD
S5 PWRGD

Power Block Diagram
SYNC_MASTER=RXU_K20
SYNC_DATE=07/24/2008

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APPLE INC.
SIZE D
DRAWING NUMBER 051-7867
REV. 01
SCALE NONE
SHT 3 OF 123

Power Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	4	123

BOM VARIANTS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9804	PCBA,BEST,2.66,512QIM_VRAM,K20	K20_COMMON,EEE_5MR,CPU_2_66GHZ,FB_512_QIMONDA
630-9805	PCBA,BEST,2.66,512SAM_VRAM,K20	K20_COMMON,EEE_5MS,CPU_2_66GHZ,FB_512_SAMSUNG
630-9806	PCBA,BEST,2.93,512QIM_VRAM,K20	K20_COMMON,EEE_5MT,CPU_2_93GHZ,FB_512_QIMONDA
630-9807	PCBA,BEST,2.93,512SAM_VRAM,K20	K20_COMMON,EEE_5MU,CPU_2_93GHZ,FB_512_SAMSUNG

K20 BOM GROUPS

BOM GROUP	BOM OPTIONS
K20_COMMON	ALTERNATE,COMMON,K20_COMMON1,K20_COMMON2,K20_DEBUG,K20_PROGPARTS
K20_COMMON1	ONEWIRE_PU,ISL6258,MEMRESET_HW,MEMRESET_MCP,MCP_B02,MCP_PROD,MCPSEQ_SMC,BMON_ENG,MCP_CS1_NO
K20_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_GMUX,DP_CA_DET_EG_PLD
K20_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,JTAG_ALLDEV,TPAD_DEBUG
K20_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_1024_QIMONDA	VRAM8,VRAM_1024_QIMONDA
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4,VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5MR]	CRITICAL	EEE_5MR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5MS]	CRITICAL	EEE_5MS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5MT]	CRITICAL	EEE_5MT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5MU]	CRITICAL	EEE_5MU

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	514-0608		ALL	FOXLINK ALT TO FOXCONN RCVR
152S0684	152S0421		ALL	MAG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
516S0709	516S0706		ALL	MOLEX ALT TO FOXCONN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3645	1	IC,PDC,QXXX,Q5,2.66,25W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3644	1	IC,PDC,QXXX,Q5,2.86,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_86GHZ
338S0554	1	IC,GPU,NV G96-GS,BGA969,LF	U8000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P TQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0600	1	IC,GMCP,MCP79-B01,35X35MM,BGA1437	U1400	CRITICAL	MCP_B01
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2356	1	IC,EFI ROM,DEVELOPMENT,K20	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
338S0603	1	IC,GMCP,MCP79-A01Q,35x35MM,BGA1437	U1400	CRITICAL	MCP_A01Q
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3643	1	IC,PDC,QXXX,Q5,2.93,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_93GHZ
337S3640	1	IC,PDC,SL3BX,PMQ,2.53,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	IC,PDC,SLB43,PMQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
333S0481	4	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8410,U8500,U8510,U8100,U8110,U8300,U8250	CRITICAL	VRAM_1024_SAMSUNG
333S0472	8	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8410,U8500,U8510,U8100,U8110,U8300,U8250	CRITICAL	VRAM_1024_QIMONDA

BOM Configuration

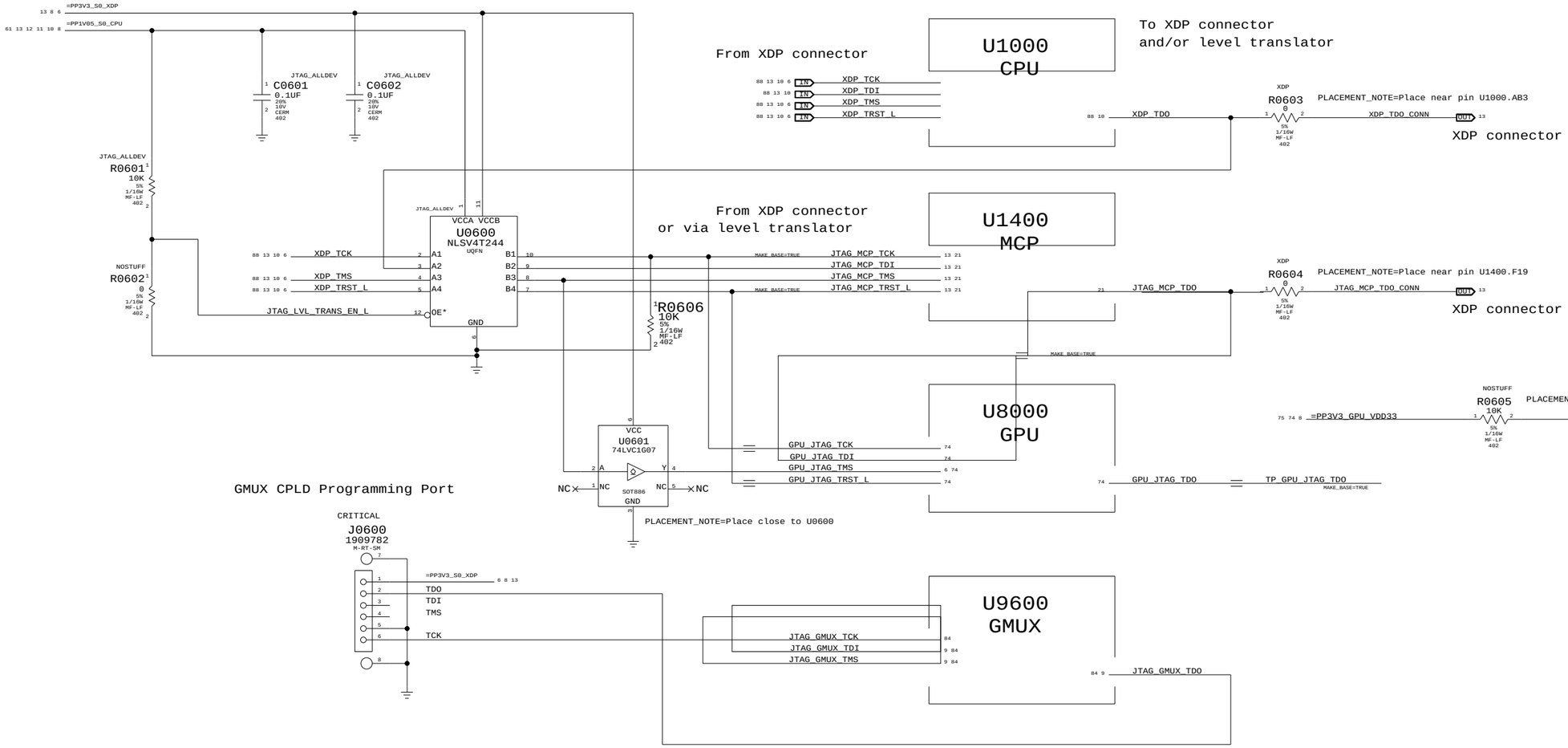
SYNC_MASTER=K20_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 5 OF 123

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 6 OF 123	

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 48	3 TPs per Fan
TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	5 TPs per Fan
TRUE	GND		

J6780 (MIC CONN)

E557	TRUE	BI_MIC_LO	57 58
E558	TRUE	BI_MIC_SHIELD	57 58
E559	TRUE	BI_MIC_HI	57 58

J6781 (LEFT SPEAKER)

E983	TRUE	SPKRAMP_C_OUT_P	7 56 57 96
E982	TRUE	SPKRAMP_C_OUT_N	7 56 57 96
E985	TRUE	SPKRAMP_L1_OUT_P	56 57 96
E987	TRUE	SPKRAMP_L1_OUT_N	56 57 96
E986	TRUE	SPKRAMP_L2_OUT_P	56 57 96
E988	TRUE	SPKRAMP_L2_OUT_N	56 57 96

J6782 (RIGHT & SUB SPEAKER)

E989	TRUE	SPKRAMP_C_OUT_P	7 56 57 96
E990	TRUE	SPKRAMP_C_OUT_N	7 56 57 96
E992	TRUE	SPKRAMP_R1_OUT_P	56 57 96
E991	TRUE	SPKRAMP_R1_OUT_N	56 57 96
E994	TRUE	SPKRAMP_R2_OUT_P	56 57 96
E993	TRUE	SPKRAMP_R2_OUT_N	56 57 96

J9000 (LVDS CONN)

E995	TRUE	PP3V3_SW_LCD	78
E996	TRUE	=PP3V3_S0_DDC_LCD	8 75 78
E997	TRUE	PPVOUT_S0_LCDBKLT	78 85
E998	TRUE	LVDS_DDC_CLK	78 81
E100	TRUE	LVDS_DDC_DATA	78 81
E100	TRUE	LVDS_CONN_A_DATA_P<0>	78 81 95
E100	TRUE	LVDS_CONN_A_DATA_N<0>	78 81 95
E100	TRUE	LVDS_CONN_A_DATA_P<1>	78 81 95
E100	TRUE	LVDS_CONN_A_DATA_N<1>	78 81 95
E100	TRUE	LVDS_CONN_A_DATA_P<2>	78 81 95
E100	TRUE	LVDS_CONN_A_DATA_N<2>	78 81 95
E100	TRUE	LVDS_CONN_A_CLK_F_P	78 95
E100	TRUE	LVDS_CONN_A_CLK_F_N	78 95
E100	TRUE	LVDS_CONN_B_DATA_P<0>	78 81 95
E100	TRUE	LVDS_CONN_B_DATA_N<0>	78 81 95
E100	TRUE	LVDS_CONN_B_DATA_P<1>	78 81 95
E100	TRUE	LVDS_CONN_B_DATA_N<1>	78 81 95
E100	TRUE	LVDS_CONN_B_DATA_P<2>	78 81 95
E100	TRUE	LVDS_CONN_B_DATA_N<2>	78 81 95
E100	TRUE	LVDS_CONN_B_CLK_F_P	78 95
E100	TRUE	LVDS_CONN_B_CLK_F_N	78 95
E101	TRUE	LED_RETURN_1	78 85
E101	TRUE	LED_RETURN_2	78 85
E101	TRUE	LED_RETURN_3	78 85
E101	TRUE	LED_RETURN_4	78 85
E101	TRUE	LED_RETURN_5	78 85
E101	TRUE	LED_RETURN_6	78 85
	TRUE	GND	4 TPs

J4500 (SATA ODD CONN)

E102	TRUE	PP5V_SW_ODD	38
E102	TRUE	SMC_ODD_DETECT	38 41
E102	TRUE	SATA_ODD_D2R_C_P	38 90
E102	TRUE	SATA_ODD_D2R_C_N	38 90
E102	TRUE	SATA_ODD_R2D_P	38 90
E102	TRUE	SATA_ODD_R2D_N	38 90
	TRUE	GND	3 TPs

J4501 (SATA HDD CONN)

E103	TRUE	PP5V_S0_HDD_FLT	38
E103	TRUE	SATA_HDD_R2D_P	38 90
E103	TRUE	SATA_HDD_R2D_N	38 90
E103	TRUE	SATA_HDD_D2R_C_N	38 90
E103	TRUE	SATA_HDD_D2R_C_P	38 90
	TRUE	GND	5 TPs

J5815 (KBD BACKLIGHT CONN)

E114	TRUE	KBDLED_ANODE	50
E114	TRUE	SMC_KDBLED_PRESENT_L	50
	TRUE	GND	

FUNC_TEST

TRUE	GND
TRUE	GND

6 TPs

USB PORTS

E105	TRUE	PP5V_S3_RTUSB_A_F	39
E105	TRUE	USB2_LT1_N	39 96
E105	TRUE	USB2_LT1_P	39 96
	TRUE	GND	
E105	TRUE	PP5V_S3_RTUSB_B_F	39
E105	TRUE	USB_LT2_N	39 96
E105	TRUE	USB_LT2_P	39 96
	TRUE	GND	
E106	TRUE	PP5V_S3_RTUSB_C_F	98
E106	TRUE	USB_LT3_N	96 98
E106	TRUE	USB_LT3_P	96 98
	TRUE	GND	

J3401 (AIRPORT/BT/CAMERA CONN)

E105	TRUE	PCIE_MINI_D2R_P	17 30 90
E105	TRUE	PCIE_MINI_D2R_N	17 30 90
E105	TRUE	PCIE_MINI_R2D_P	30 90
E105	TRUE	PCIE_MINI_R2D_N	30 90
E105	TRUE	PCIE_CLK100M_MINI_CONN_P	30 96
E105	TRUE	PCIE_CLK100M_MINI_CONN_N	30 96
E105	TRUE	MINI_CLKREQ_Q_L	30
E105	TRUE	PCIE_WAKE_L	7 17 30 31
E105	TRUE	MINI_RESET_CONN_L	30
E105	TRUE	PP5V_WLAN	30
E100	TRUE	PP5V_S3_BTCAMERA_F	30
E100	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94
E100	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
E100	TRUE	USB_CAMERA_CONN_P	30 96
E100	TRUE	USB_CAMERA_CONN_N	30 96
E100	TRUE	CONN_USB2_BT_P	30 96
E100	TRUE	CONN_USB2_BT_N	30 96

J3500 (EXPRESS CARD CONN)

E100	TRUE	PP1V5_S0_EXCARD_SWITCH	31
E100	TRUE	PCIE_WAKE_L	7 17 30 31
E100	TRUE	SMBUS_MCP_0_CLK	13 21 44 85 91
E100	TRUE	SMBUS_MCP_0_DATA	13 21 44 85 91
E107	TRUE	PP3V3_S0_EXCARD_SWITCH	31
E107	TRUE	PP3V3_S3_EXCARD_SWITCH	31
E107	TRUE	USB2_EXCARD_CONN_N	31 96
E107	TRUE	USB2_EXCARD_CONN_P	31 96
E107	TRUE	EXCARD_CPUSB_L	31
E107	TRUE	EXCARD_CLKREQ_CONN_L	31
E107	TRUE	EXCARD_CPPE_L	31
E107	TRUE	PLT_RESET_SWITCH_L	31
E107	TRUE	PCIE_EXCARD_D2R_P	17 31 90
E108	TRUE	PCIE_EXCARD_D2R_N	17 31 90
E108	TRUE	PCIE_EXCARD_R2D_P	31 90
E108	TRUE	PCIE_EXCARD_R2D_N	31 90
E108	TRUE	PCIE_CLK100M_EXCARD_CONN_P	31 96
E108	TRUE	PCIE_CLK100M_EXCARD_CONN_N	31 96

J5800 (IPD FLEX CONN)

E108	TRUE	PP3V3_S3_LDO	50
E108	TRUE	PP18V5_S3	7 50
E108	TRUE	TPAD_GND_F	50
E108	TRUE	Z2_DEBUG3	49 50
E108	TRUE	Z2_MISO	49 50
E109	TRUE	Z2_BOOST_EN	50
E109	TRUE	Z2_BOOT_CFG1	49 50
E109	TRUE	Z2_CLKIN	49 50
E109	TRUE	Z2_KEY_ACT_L	49 50
E109	TRUE	Z2_RESET	49 50
E109	TRUE	PSOC_F_CS_L	49 50
E109	TRUE	PICKB_L	49 50
E109	TRUE	PSOC_MISO	49 50
E109	TRUE	PSOC_MOSI	49 50
E109	TRUE	PSOC_SCLK	49 50
E110	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
E110	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94

J6900 (DC POWER CONN)

E113	TRUE	ADAPTER_SENSE	59
E113	TRUE	PP18V5_DCIN_FUSE	59
	TRUE	GND	

J6950 (MAIN BATT CONN)

E113	TRUE	PPVBAT_G3H_CONN_F	59
E113	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
E113	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
E113	TRUE	SMC_BS_ALRT_L	41 42 59
	TRUE	GND	

J6995 (BAT LED CONN)

E114	TRUE	PP3V42_G3H	7 8 42
E114	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
E114	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
E114	TRUE	SMC_BIL_BUTTON_DB_L	42 59
	TRUE	GND	

J5713 (KEY BOARD CONN)

E110	TRUE	PP3V3_S3	7 8 9
E110	TRUE	PP3V42_G3H	7 8 42
E110	TRUE	WS_KBD1	49
E110	TRUE	WS_KBD2	49
E110	TRUE	WS_KBD3	49
E110	TRUE	WS_KBD4	49
E110	TRUE	WS_KBD5	49
E110	TRUE	WS_KBD6	49
E111	TRUE	WS_KBD7	49
E111	TRUE	WS_KBD8	49
E111	TRUE	WS_KBD9	49
E111	TRUE	WS_KBD10	49
E111	TRUE	WS_KBD11	49
E111	TRUE	WS_KBD12	49
E111	TRUE	WS_KBD13	49
E111	TRUE	WS_KBD14	49
E111	TRUE	WS_KBD15_CAP	49
E111	TRUE	WS_KBD16_NUM	49
E111	TRUE	WS_KBD17	49
E112	TRUE	WS_KBD18	49
E112	TRUE	WS_KBD19	49
E112	TRUE	WS_KBD20	49
E112	TRUE	WS_KBD21	49
E112	TRUE	WS_KBD22	49
E112	TRUE	WS_KBD23	49
E112	TRUE	WS_KBD_ONOFF_L	49
E112	TRUE	WS_LEFT_SHIFT_KBD	49
E113	TRUE	WS_LEFT_OPTION_KBD	49
E113	TRUE	WS_CONTROL_KBD	49

J4800 (FRONT CABLE CONN)

E114	TRUE	PP3V42_G3H_LIDSWITCH_R	40
E114	TRUE	PP5V_S3_IR_R	40
E114	TRUE	SMC_LID_R	40
E114	TRUE	IR_RX_OUT	40
E114	TRUE	SYS_LED_ANODE	40 42
	TRUE	GND	

J5502 (SENSOR CONN)

E115	TRUE	MCPTHMSNS_D_P	47 96
E115	TRUE	MCPTHMSNS_D_N	47 96

POWER RAILS

FUNC_TEST

E640	TRUE	PM_SLP_S3_L	21 33 36 41 67 82 84
E802	TRUE	PPBUS_G3H	8 45
E803	TRUE	PPBUS_CPU_IMVP_ISNS	8
E804	TRUE	PP3V42_G3H	7 8 42
E805	TRUE	PP5V_S3	8
E807	TRUE	PP5V_S0	8
E805	TRUE	PPVCORE_S0_CPU	8
E808	TRUE	PPVCORE_S0_MCP	8
E810	TRUE	PP3V3_S5	8 96
E812	TRUE	PP3V3_S3	7 8 9
E811	TRUE	PP3V3_S0	8 9 66 85 96
E813	TRUE	PP2V5_S0	8
E809	TRUE	PP1V2_S0	8
E806	TRUE	PP1V8_S0	8 66
E825	TRUE	PP1V8R1V5_S3	8
E824	TRUE	PP1V8R1V5_S0	8
E823	TRUE	PPMCPDDR_ISNS	7 8
E822	TRUE	PP1V05_S0	8
E820	TRUE	PP1V2R1V05_S5	8
E821	TRUE	PPCPUVTT_S0	8
E818	TRUE	PP0V9R0V75_S0_DDRVTT	8
E817	TRUE	PP1V2R1V05_ENET	8
E815	TRUE	PP3V3_ENET_PHY	8
E816	TRUE	PPVP_FW	8
E814	TRUE	PP1V0_FW	8
E827	TRUE	PP3V3_S0GPU	8
E826	TRUE	PP1V1_S0GPU	8
E828	TRUE	PP1V8_S0GPU_ISNS	8
E829	TRUE	PPVCORE_GPU	8
E837	TRUE	PP1V8_S0GPU_ISNS_R	8
E836	TRUE	PP3V3_S5_AVREF_SMC	41 42
E799	TRUE	PP18V5_S3	7 50
E710	TRUE	PPDCIN_G3H	8
E710	TRUE	PPVCORE_S0_MCP_REG	
E710	TRUE	PPMCPDDR_ISNS	7 8
E710	TRUE	PPCPUFSB_ISNS_R	
E710	TRUE	PPVTTDDR_S3	8
E710	TRUE	PP1V8_GPUIFPX	8

FUNC_TEST

E720	TRUE	SYS_LED_ANODE_R	40
E722	TRUE	LPC_CLK33M_LPCPLUS	25 43 91
E720	TRUE	LPC_AD<0..3>	19 41 43 84 91
E720	TRUE	SPI_ALT_MOSI	43
E720	TRUE	SPI_ALT_MISO	43
E720	TRUE	LPC_FRAME_L	19 41 43 84 91
E727	TRUE	PM_CLKRUN_L	19 41 43
E720	TRUE	SMC_TMS	41 42 43
E720	TRUE	DEBUG_RESET_L	25 43
E720	TRUE	SMC_TDO	41 42 43
E720	TRUE	SMC_TRST_L	41 43
E731	TRUE	SMC_MD1	41 43
E730	TRUE	SMC_TX_L	39 41 42 43
E730	TRUE	SPIROM_USE_MLB	43
E730	TRUE	SPI_ALT_CLK	43
E730	TRUE	SPI_ALT_CS_L	43
E737	TRUE	LPC_SERIRQ	19 41 43
E730	TRUE	LPC_PWRDWN_L	19 41 43
E739	TRUE		41 42 43
E740	TRUE		41 42 43
E741	TRUE	SMC_RESET_L	41 42 43
E742	TRUE		41 43
E743	TRUE	SMC_RX_L	39 41 42 43
E744	TRUE	LPCPLUS_GPIO	18 43
E761	TRUE	ISSP_SCLK_P1_1	49
E762	TRUE	ISSP_SDATA_P1_0	49
	TRUE	SMC_ONOFF_L	41 42 49
E760	TRUE	PM_SYSRST_L	25 41

NC NO_TESTs

NO_TEST

19	TP_PCI_AD<31..8>	TRUE	MAKE_BASE=TRUE	NC_PCI_AD<31..8>
19	TP_PCI_C_BE_L<3..0>	TRUE	MAKE_BASE=TRUE	NC_PCI_C_BE_L<3..0>
19	TP_PCI_CLK0	TRUE	MAKE_BASE=TRUE	NC_PCI_CLK0
19	TP_PCI_CLK1	TRUE	MAKE_BASE=TRUE	NC_PCI_CLK1
19	TP_PCI_DEVSEL_L	TRUE	MAKE_BASE=TRUE	NC_PCI_DEVSEL_L
19	TP_PCI_FRAME_L	TRUE	MAKE_BASE=TRUE	NC_PCI_FRAME_L
19	TP_PCI_GNT0_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT0_L
19	TP_PCI_GNT1_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT1_L
19	TP_PCI_INTW_L	TRUE	MAKE_BASE=TRUE	NC_PCI_INTW_L
19	TP_PCI_INTX_L	TRUE	MAKE_BASE=TRUE	NC_PCI_INTX_L
19	TP_PCI_INTY_L	TRUE	MAKE_BASE=TRUE	NC_PCI_INTY_L
19	TP_PCI_INTZ_L	TRUE	MAKE_BASE=TRUE	NC_PCI_INTZ_L
19	TP_PCI_IRDY_L	TRUE	MAKE_BASE=TRUE	NC_PCI_IRDY_L
19	TP_PCI_PAR	TRUE	MAKE_BASE=TRUE	NC_PCI_PAR
19	TP_PCI_PERR_L	TRUE	MAKE_BASE=TRUE	NC_PCI_PERR_L
19	TP_PCI_RESET1_L	TRUE	MAKE_BASE=TRUE	NC_PCI_RESET1_L
19	TP_PCI_SERR_L	TRUE	MAKE_BASE=TRUE	NC_PCI_SERR_L
19	TP_PCI_STOP_L	TRUE	MAKE_BASE=TRUE	NC_PCI_STOP_L
19	TP_PCI_TRDY_L	TRUE	MAKE_BASE=TRUE	NC_PCI_TRDY_L
17	TP_PCIE_CLK100M_PE4P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
17	TP_PCIE_CLK100M_PE5N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
17	TP_PCIE_CLK100M_PE5P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
17	TP_PCIE_CLK100M_PE6N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
17	TP_PCIE_CLK100M_PE6P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
17	TP_PCIE_PE4_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE4_D2RN
17	TP_PCIE_PE4_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE4_D2RP
17	TP_PE4_CLKREQ_L	TRUE	MAKE_BASE=TRUE	NC_PE4_CLKREQ_L
69	TP_PEX_CLKREQ_L	TRUE	MAKE_BASE=TRUE	NC_PEX_CLKREQ_L
49	TP_PSOC_P1_3	TRUE	MAKE_BASE=TRUE	NC_PSOC_P1_3
20	TP_SATA_C_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_C_D2RN
20	TP_SATA_C_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_C_D2RP
20	TP_SATA_C_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
20	TP_SATA_C_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
20	TP_SATA_D_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RN
20	TP_SATA_D_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RP
20	TP_SATA_D_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
20	TP_SATA_D_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
20	TP_SATA_E_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RN
20	TP_SATA_E_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RP
20	TP_SATA_E_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
20	TP_SATA_E_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
20	TP_SATA_F_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RN
20	TP_SATA_F_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RP
20	TP_SATA_F_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
20	TP_SATA_F_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
21	TP_SB_A20GATE	TRUE	MAKE_BASE=TRUE	NC_SB_A20GATE
42	TP_SMC_P41	TRUE	MAKE_BASE=TRUE	NC_SMC_P41
20	TP_USB_10P	TRUE	MAKE_BASE=TRUE	NC_USB_10P
20	TP_USB_11N	TRUE	MAKE_BASE=TRUE	NC_USB_11N
20	TP_USB_11P	TRUE	MAKE_BASE=TRUE	NC_USB_11P
9	TP_USB_EXTDN	TRUE	MAKE_BASE=TRUE	NC_USB_EXTDN
9	TP_USB_EXTDP	TRUE	MAKE_BASE=TRUE	NC_USB_EXTDP
9	TP_USB_MININ	TRUE	MAKE_BASE=TRUE	NC_USB_MININ
9	TP_USB_MINIP	TRUE	MAKE_BASE=TRUE	NC_USB_MINIP
13	TP_XDP_OBSDATA_B2	TRUE	MAKE_BASE=TRUE	NC_XDP_OBSDATA_B2
13	TP_XDP_OBSDATA_B3	TRUE	MAKE_BASE=TRUE	NC_XDP_OBSDATA_B3

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 88
TRUE	FSB_ADS_L	10 14 88
TRUE	FSB_ADSTB_L<1..0>	10 14 88
TRUE	FSB_D_L<63..0>	10 14 88
TRUE	FSB_DBSY_L	10 14 88
TRUE	FSB_DINV_L<3..0>	10 14 88
TRUE	FSB_DRDY_L	10 14 88
TRUE	FSB_DSTB_L_N<3..0>	10 14 88
TRUE	FSB_DSTB_L_P<3..0>	10 14 88
TRUE	FSB_HIT_L	10 14 88
TRUE	FSB_HITM_L	10 14 88
TRUE	FSB_LOCK_L	10 14 88
TRUE	FSB_REQ_L<4..0>	10 14 88

FB NO_TESTs

NO_TEST

E982	TRUE	FB_A_DQ<63..0>	71 72 79 95
E981	TRUE	FB_B_DQ<63..0>	71 73 80 95

POWER NO_TESTs

NO_TEST

E934	TRUE	P1V2S0_SW	87
E935	TRUE	P1V05S5_LL	66
E937	TRUE	P2V5S0_SW	87

NC NO_TESTs

NO_TEST

9	TP_CPU_PECI_MCP	TRUE	MAKE_BASE=TRUE	NC_CPU_PECI_MCP
10	TP_CPU_TEST3	TRUE	MAKE_BASE=TRUE	NC_CPU_TEST3
18	TP_ENET_INTR_L	TRUE	MAKE_BASE=TRUE	NC_ENET_INTR_L
18	TP_ENET_PWRDWN_L	TRUE	MAKE_BASE=TRUE	NC_ENET_PWRDWN_L
35	TP_FW643_AVREG	TRUE	MAKE_BASE=TRUE	NC_FW643_AVREG
35	TP_FW643_TDI	TRUE	MAKE_BASE=TRUE	NC_FW643_TDI
9	TP_MEM_A_A<15>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_A<15>
16	TP_MEM_A_CKE<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CKE<2>
16	TP_MEM_A_CKE<3>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CKE<3>
15	TP_MEM_A_CLK2N	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK2N
15	TP_MEM_A_CLK2P	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK2P
16	TP_MEM_A_CLK3N	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK3N
16	TP_MEM_A_CLK3P	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK3P
16	TP_MEM_A_CLK4N	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK4N
16	TP_MEM_A_CLK4P	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK4P
16	TP_MEM_A_CLK5N	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK5N
16	TP_MEM_A_CLK5P	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CLK5P
16	TP_MEM_A_CS_L<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CS_L<2>
16	TP_MEM_A_CS_L<3>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_CS_L<3>
16	TP_MEM_A_ODT<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_ODT<2>
16	TP_MEM_A_ODT<3>	TRUE	MAKE_BASE=TRUE	NC_MEM_A_ODT<3>
9	TP_MEM_B_A<15>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_A<15>
16	TP_MEM_B_CKE<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CKE<2>
15	TP_MEM_B_CLK2P	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK2P
16	TP_MEM_B_CLK3N	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK3N
16	TP_MEM_B_CLK3P	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK3P
16	TP_MEM_B_CLK4N	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK4N
16	TP_MEM_B_CLK4P	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK4P
16	TP_MEM_B_CLK5N	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK5N
16	TP_MEM_B_CLK5P	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CLK5P
16	TP_MEM_B_CS_L<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CS_L<2>
16	TP_MEM_B_CS_L<3>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_CS_L<3>
16	TP_MEM_B_ODT<2>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_ODT<2>
16	TP_MEM_B_ODT<3>	TRUE	MAKE_BASE=TRUE	NC_MEM_B_ODT<3>
21	TP_MLB_RAM_SIZE	TRUE	MAKE_BASE=TRUE	NC_MLB_RAM_SIZE
21	TP_MLB_RAM_VENDOR	TRUE	MAKE_BASE=TRUE	NC_MLB_RAM_VENDOR
74	TP_GPU_BUFRST_L	TRUE	MAKE_BASE=TRUE	NC_GPU_BUFRST_L
75	TP_GPU_GSTATE<0>	TRUE	MAKE_BASE=TRUE	NC_GPU_GSTATE<0>
75	TP_GPU_GSTATE<1>	TRUE	MAKE_BASE=TRUE	NC_GPU_GSTATE<1>
75	TP_GPU_MIOA_D<9..0>	TRUE	MAKE_BASE=TRUE	NC_GPU_MIOA_D<9..0>
75	TP_GPU_MIOA_DE	TRUE	MAKE_BASE=TRUE	NC_GPU_MIOA_DE
74	TP_GPU_PGOOD_OUT_L	TRUE	MAKE_BASE=TRUE	NC_GPU_PGOOD_OUT_L
75	TP_GPU_VCORE_VID3	TRUE	MAKE_BASE=TRUE	NC_GPU_VCORE_VID3
19	TP_LPC_DRQ0_L	TRUE	MAKE_BASE=TRUE	NC_LPC_DRQ0_L
75	TP_LVDS_EG_B_CLK_N	TRUE	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_N
75	TP_LVDS_EG_B_CLK_P	TRUE	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_P
75	TP_LVDS_EG_BKL_PWM	TRUE	MAKE_BASE=TRUE	NC_LVDS_EG_BKL_PWM
9	TP_LVDS_IG_B_CLKN	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
9	TP_LVDS_IG_B_CLKP	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
9	TP_LVDS_IG_BKL_PWM	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
21	TP_MCP_BUF_SIO_CLK	TRUE	MAKE_BASE=TRUE	NC_MCP_BUF_SIO_CLK
17	TP_MCP_GPIO_18	TRUE	MAKE_BASE=TRUE	NC_MCP_GPIO_18
21	TP_MCP_KBDRSTIN_L	TRUE	MAKE_BASE=TRUE	NC_MCP_KBDRSTIN_L
20	TP_MCP_SATALED_L	TRUE	MAKE_BASE=TRUE	NC_MCP_SATALED_L

NC NO_TESTs

NO_TEST

E761	TRUE	NC_SMC_FAN_3_CTL	42
E762	TRUE	NC_SMC_FAN_2_TACH	42
E763	TRUE	NC_SMC_FAN_2_CTL	42
E764	TRUE	NC_FW2_TPBP	37
E765	TRUE	NC_FW2_TPBN	37
E767	TRUE	NC_FW2_TPBIAS	37
E766	TRUE	NC_FW2_TPAP	37
E768	TRUE	NC_FW2_TPAN	37
E769	TRUE	NC_FW0_TPBP	37
E770	TRUE	NC_FW0_TPBN	37
E772	TRUE	NC_FW0_TPAP	37
E773	TRUE	NC_ESTARLDO_EN	42
E774	TRUE	NC_ALS_GAIN	42

Functional / ICT Test

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 7 OF 123	

"G3Hot" (Always-Present) Rails

60 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3 62
=PPVIN_S0_CPUVTTS0 65
=PPBUS_S0_LCDBKLT 86
=PPVIN_GPU_GPUVCORE 77
=PPVIN_S5_CPU_IMVP_ISNS_R 45
=PPVIN_S0_P5VRTS0_MCPCORE 64
=PPVIN_S3_DDRREG 63
=PPVIN_S0GPU_P1V8P1V1 83
=PPVBAT_G3H_P3V42G3H 59
=PPVIN_S0_P1V05S5 66
=PPVIN_S0_KBDLED 50
=PPVIN_S5_FWPWRSW 36
=PPVIN_S5_BKL 36

45 =PPVIN_S5_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP 61

59 =PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 60

59 =PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SMCUSBMUX 39
=PP3V42_G3H_SMBUS_SMC_BSA 44
=PP3V42_G3H_LIDSWITCH 40
=PP3V3_S5_SMC 41 42 51
=PP3V3_S5_LPCPLUS 43
=PPVIN_S5_SMCVREF 42
=PP3V42_G3H_PWRCTL 67
=PP3V42_G3H_CHGR 60
=PP3V3_S5_RTC_D 25
=PP3V42_G3H_BATT 59
=PP3V42_G3H_TPAD 49
=PP3V42_G3H_BMON_ISNS 45
=PP3V42_G3H_CPUCOREISNS 45

5V Rails

62 =PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_SYSLED 42
=PP5V_S3_BTCAMERA 30
=PP5V_S3_WLAN 30
=PP5V_S3_IR 40
=PP5V_S3_DDRREG 63
=PP5V_S3_GPUVCORE 77
=PP5V_S3_RTUSB 39 98
=PP5V_S3_TPAD 50
=PP5V_S3_P1V05S0FET 68
=PP5V_S3_MCPDDRFET 68
=PP5V_S3_VTTCLAMP 68
=PP5V_S3_AUDIO_PWR 9

64 =PP5V_S0_REG
PP5V_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_FAN_LT 7 48
=PP5V_S0_FAN_RT 48
=PP5V_S0_CPU_IMVP 61
=PP5V_S0_CPUVTTS0 65
=PP5V_S0GPU_P1V1P1V8_GPU 83
=PP5V_S0_LPCPLUS 43
=PP5V_S0_ODD 38
=PP5V_S0_HDD 38

Chipset "VCore" Rails

61 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12 45

64 =PPMCPCORE_S0_REG
PPVCORE_S0_MCP
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 22 23 45

3.3V-2.5V Rails

62 =PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_ROM 43 52
=PP3V3_S5_MEMRESET 29
=PP3V3_S3_P3V3S3FET 68
=PP3V3_S0_LCD 78
=PP3V3_S0_P3V3S0FET 68
=PP3V3_GPU_P3V3GPUFET 68
=PP3V3_S5_PWRCTL 67
=PP3V3_S5_P1V05FET 68
=PP3V3_S5_MCP 22 23
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_FW_LATEVG_ACTIVE 36
=PP3V3_S5_MCPPWRGD 25
=PP3V3_FW_LATEVG 37
=PP3V3_S5_P1V05ENETFET 33
=PP3V3_S5_P3V3ENETFET 33
=PP3V3_S5_DP_PORT_PWR 82

68 =PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_BT 30
=PP3V3_S3_P1V8S0 66
=PP3V3_S3_SMBUS_SMC_A_S3 44
=PP3V3_S3_SMS 8 51
=PP3V3_S3_TPAD 49
=PP3V3_S3_SMS 8 51
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_VREFMRGN 26
=PP3V3_S3_SMBUS_SMC_MGMT 44
=PP3V3_S3_EXCARD 31
=PP3V3_S3_P1V0EW 9
=PP3V3_S3_P1V5EXPS0 66
=PP3V3_S3_BKL_VDDIO

68 =PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_LPCPLUS 43
=PP3V3_S0_SMC 42
=PP3V3_S0_SMBUS_SMC_B_S0 44
=PP3V3_S0_MCPDDRISNS 46
=PP3V3_S0_GPU1V8ISNS 46
=PP3V3_S0_CPUTHMSNS 47
=PP3V3_S0_GPUTHMSNS 47
=PP3V3_S0_FAN_LT 48
=PP3V3_S0_FAN_RT 48
=PP3V3_S0_IMVP 61
=PP3V3_S0_PWRCTL 67
=PP3V3_S0_DDC_LCD 7 75 78
=PP3V3_S0_XDP 6 8 13
=PP3V3_S0_MCPCOREISNS 46
=PP3V3_S0_XDP 6 8 13
=PPSPD_S0_MEM_A 27
=PPSPD_S0_MEM_B 28
=PP3V3_S0_SMBUS_MCP_0 44
=PP3V3_S0_GMUX 84
=PP3V3_S0_DPMUX 81
=PP3V3_S0_DPCONN 82
=PP3V3_S0_P1V2P2V5 87
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_HDCPROM 24
=PP3V3R1V5_S0_MCP_HDA 21 23
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3_S0_MCP_VPLL_UF 24
=PP3V3_S0_MCP_DAC_UF 24
=PP3V3_S0_MCP 21 22 23
=PP3V3_S0_AUDIO 53 57 58
=PP3V3_S0_ODD 38
=PP3V3_S0_VMON 67
=PP3V3_S0_SMBUS_MCP_1 44
=PP3V3_S3_REMTHMSNS 47
=PP3V3_S0_EXCARD 31
=PP3V3_S0_LVDSDDCMUX 81
=PP3V3_S0_BATTCHARGERTMPSNSR 47
=PP3V3_GPU_SMBUS_SMC_0_S0 44
=PP3V3_S0_TPAD 50

87 =PP2V5_S0_REG
PP2V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=2.5V
MAKE_BASE=TRUE
=PP2V5_S0_GMUX 84

87 =PP1V2_S0_REG
PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PP1V2_S0_GMUX 84

1.8V/DDR 1.5V Rails

66 =PP1V8_S0_REG
500 mA max supply
PP1V8_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
190 mA =PP3V3R1V8_S0_MCP_IFP_VDD 18 24

63 =PPDDR_S3_REG
PP1V8R1V5_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_MCP_FET 68
=PPVIN_S0_DDRREG_LDO 63
=PP1V5_S3_MEM_A 27
=PP1V5_S3_MEM_B 28
=PP1V5_S3_MEMRESET 29

68 =PP1V8R1V5_S0_FET
PP1V8R1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
4771 mA =PPMCPDDR_ISNS_R 46
130 mA =PP1V5_S0_CPU 11 12
500 mA =PP1V5_S0_VMON 67

66 =PP1V5_EXP_S0
PP1V5_EXP_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_EXCARD 31

23 16 =PP1V8R1V5_S0_MCP_MEM
PPMCPDDR_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_MEM_A 27
=PP1V5_S0_MEM_B 28
=PPMCPDDR_ISNS 46

68 66 =PP1V05_S0_FET
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_PEX_DVDD 8 23
=PP1V05_S0_MCP_SATA_DVDD 8 23
=PP1V05_S0_MCP_HDMI_VDD 18 24
=PP1V05_S0_VMON 67
=PP1V05_S0_MCP_PLL_PEX_UF 23
1034 mA
PP1V05_S0_MCP_PLL_UF
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_S0_MCP_PLL_UF 23 66

23 8 =PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PEX_DVDD0 17
=PP1V05_S0_MCP_PEX_DVDD1 17

23 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17

23 8 =PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_SATA_DVDD0 20

23 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_SATA_AVDD0 20

66 =PP1V05_S5_MCP
PP1V2R1V05_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
(1.1V for A01)
241 mA max load
105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC 22 23
139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET 33
=PP1V05_S5_P1V05S0FET 68

65 =PPCPUVTT_S0_REG
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
5300 mA
4500 mA =PP1V05_S0_CPU 6 10 11 12 13 61
=PP1V05_S0_SMC_LS 42
1182 mA =PP1V05_S0_MCP_FSB 9 14 22 23

63 26 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

63 =PPVTT_S0_DDR_LDO
PP0V9R0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A 27
=PP0V75_S0_MEM_VTT_B 28
=PPVTT_S0_VTTCLAMP 68
OR 0.75V

ENET Rails

33 =PP1V05_ENET_FET
PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 23
=PP1V05_ENET_MCP_RMGT 18 23
=PP1V05_ENET_PHY 32

33 =PP3V3_ENET_FET
PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 23
=PP3V3_ENET_PHY 32

"FW" (FireWire) Rails

36 =PPVOUT_FW_FWPWRSW
PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_PFWBOOST 66

66 =PFWBOOST_REG
PP10V_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=10V
MAKE_BASE=TRUE
=PPBOOST_FW_FWPWRSW_F 36

36 =PPBOOST_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=10V
MAKE_BASE=TRUE
=PPVP_FW_PORT1 37
=PPVP_FW_PHY_CPS_FET 37

66 =PP1V0_FW_REG
PP1V0_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY 35

"GPU" Rails

68 =PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33 6 74 75
=PP3V3_GPU_MIO 74 75
=PP3V3_GPU_LVDS_DDC 81
=PP3V3_GPU_PWRCTL 67
=PP3V3_GPU_VCORELOGIC 77
=PP3V3_GPU_P1V8S0 66

83 =PP1V1_S0GPU_REG
PP1V1_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
MAKE_BASE=TRUE
=PP1V1_GPU_PEX_IOVDDQ 69
=PP1V1_GPU_PEX_IOVDD 69
=PP1V1_GPU_PEX_PLLXVDD 69
=PP1V1_GPU_PLLVDD 74
=PP1V1_GPU_H_PLLVDD 74
=PP1V1_GPU_VID_PLLVDD 74
=PP1V1_GPU_FBPLLAVDD 71
=PP1V1_GPU_IFPCD_IOVDD 76

66 =PP1V8_GPUIFPX_REG
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_IFPX 76

46 =PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD 72 73 79 80
=PP1V8_GPU_FB_VDDQ 9 72 73 79 80
=PP1V8_GPU_FBVDDQ 70
=PP1V8_GPU_FBIO 71

77 45 =PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PPVCORE_GPU 70

83 =PP1V8_GPU_REG
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V8_S0GPU_ISNS_R 46

Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	8	123

Thermal Module Holes

ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
Bottom Left GPU TM Hole
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P2 — GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0932 3R2P5 — GND_CHASSIS_RIGHTHS
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0970 3R2P5 — GND_CHASSIS_DIMM
ZT0971 3R2P5 — GND_CHASSIS_TPAD

ZT0931 STDOFF-4.0OD3.0H-SM
ZT0934 STDOFF-4.0OD3.0H-SM

ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

23 22 14 8 =PP1V05_S0_MCP_FSB

NO STUFF R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0990 150 1% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402

88 61 14 10 OUT CPU_DPRSTP_L
88 14 10 OUT FSB_BREQ0_L
88 14 13 10 OUT FSB_CPURST_L
88 14 10 OUT CPU_INTR
88 14 10 OUT CPU_NMI

80 79 73 72 8 =PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402
R0901 10 1% 1/16W MF-LF 402
GPU_FB_A_VREF_DIV 26
=PP1V8_GPU_FB_VREF_A 72
GPU_FB_B_VREF_DIV 26
=PP1V8_GPU_FB_VREF_B 73

Bosses for VRAM HS

ZT0951 4.0OD1.65H-M1.6X0.35
ZT0952 4.0OD1.65H-M1.6X0.35
ZT0953 4.0OD1.65H-M1.6X0.35
ZT0954 4.0OD1.65H-M1.6X0.35
ZT0955 4.0OD1.65H-M1.6X0.35
ZT0956 4.0OD1.65H-M1.6X0.35

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0915 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
(all SM, 1)

=PP1V05_S0_MCP_SATA_DVDD1 20
=PP1V05_S0_MCP_SATA_AVDD1 20

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L 61
88 11 CPU_VID<0..6> — IMVP6_VID<0..6> 61 88
88 10 CPU_BSEL<0..2> — =MCP_BSEL<0..2> 14
25 MEM_VTT_EN — =DDRVTT_EN 63 68
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB 21 43
(MAKE_BASE=TRUE)

GPU signals

90 69 PEG_D2R_P<0..15> — =PEG_D2R_P<0..15> 17
90 69 PEG_D2R_N<0..15> — =PEG_D2R_N<0..15> 17
90 69 PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15> 17
90 69 PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15> 17
(MAKE_BASE=TRUE)

84 LCD_BKLT_EN — LVDS_BKL_ON 86
90 81 DP_IG_ML_P<3> — =MCP_HDMI_TXC_P 18
90 81 DP_IG_ML_N<3> — =MCP_HDMI_TXC_N 18
90 81 DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2> 18
90 81 DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2> 18
81 75 DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK 18
81 75 DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA 18
81 DP_IG_HPD — =MCP_HDMI_HPD 18
(MAKE_BASE=TRUE)

GMUX ALIASES

67 PM_ALL_GPU_PGOOD — ALL_EG_PGOOD 84
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG 84
84 EG_RESET_L — GPU_RESET_L 69
(MAKE_BASE=TRUE)

84 6 JTAG_GMUX_TDI — GMUX_JTAG_TDI 19
84 6 JTAG_GMUX_TMS — GMUX_JTAG_TMS 19
84 6 JTAG_GMUX_TDO — GMUX_JTAG_TDO 17
84 GMUX_INT — =DVI_HPD_GMUX_INT 18
18 LVDS_IG_BKL_ON — IG_BKLT_EN 84
18 LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN 84
BKL_SYNC — TP_BKL_SYNC
(MAKE_BASE=TRUE)

P1V0FW REGULATOR ENABLE RESISTORS

PLACEMENT_NOTE=Place at U7700
96 85 66 9 8 7 PP3V3_S0 — R0940 0 5% 1/16W MF-LF 402 — P1V0FW_EN (MAKE_BASE=TRUE) — =PP3V3_FW_P1V0FW 66
8 =PP3V3_S3_P1V0FW — NO STUFF R0941 0 5% 1/16W MF-LF 402 — P1V0FW_EN
PLACEMENT_NOTE=Place at U7700

66 =P1V5_EXP_S0_EN — PP3V3_S0 7 8 9 66 85 96

PP3V3_FW_FWPHY RESISTORS

PLACEMENT_NOTE=Place at U4100
96 85 66 9 8 7 PP3V3_S0 — R0942 0 5% 1/16W MF-LF 402 — PP3V3_FW_FWPHY (MAKE_BASE=TRUE) — =PP3V3_FW_FWPHY 35 37
8 7 PP3V3_S3 — NO STUFF R0943 0 5% 1/16W MF-LF 402 — PP3V3_FW_FWPHY
PLACEMENT_NOTE=Place at U4100

MCP_MII_PD (MAKE_BASE=TRUE)
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER 18
=MCP_MII_CRS 18
=MCP_MII_COL 18

7 TP_USB_EXTDP — USB_EXTD_P 20 91
7 TP_USB_EXTDN — USB_EXTD_N 20 91
7 TP_USB_MINIP — USB_MINI_P 20 91
7 TP_USB_MININ — USB_MINI_N 20 91
7 TP_MEM_A_A<15> — MEM_A_A<15> 27
7 TP_MEM_B_A<15> — MEM_B_A<15> 28
7 TP_CPU_PECI_MCP — CPU_PECI_MCP 14
(MAKE_BASE=TRUE)

7 TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P 18 90
7 TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N 18 90
7 TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM 18
(MAKE_BASE=TRUE)

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> 18 90
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> 18 90
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> 18 90
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> 18 90
(MAKE_BASE=TRUE, NO_TEST=TRUE)

TP_MCP79_GPIO17 — AUD_IP_PERIPHERAL_DET 17
(MAKE_BASE=TRUE)

AUDIO ALIASES

53 HDA_BITCLK — HDA_BIT_CLK 21 91
(MAKE_BASE=TRUE)

8 =PP5V_S3_AUDIO_PWR
XW0900 (SM) 2 1 PP5V_S3_AUDIO 53 55
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
XW0901 (SM) 2 1 PP5V_S3_AUDIO_AMP 56
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

R0902 10K 5% 1/16W MF-LF 402
1 AUD_IPHS_SWITCH_EN 19 58
MAKE_BASE=TRUE

R0903 0 5% 1/16W MF-LF 402
21 MCP_SPKR — SMC_MCP_SAFE_MODE 41

ETHERNET ALIASES

33 =P3V3ENET_EN — PM_SLP_RMGT_L 21
(MAKE_BASE=TRUE)
33 =P1V05ENET_EN
32 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
(MAKE_BASE=TRUE)
32 =RTL8211_REGOUT — NC_RTL8211_REGOUT
(MAKE_BASE=TRUE)
32 =RTL8211_ENSWREG

MCP79 PCIe PRSNT# Straps

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L (MAKE_BASE=TRUE) OUT 17
NO STUFF R0927 0 5% 1/16W MF-LF 402 — PEG_PRSNT_L (MAKE_BASE=TRUE) OUT 17
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L IN 84

Signal Aliases

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 9 OF 123	

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> M2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L1 REQ4*

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
TP_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

=PP1V05_S0_CPU
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> G22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H22 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H23 D15*
FSB_DSTB_L_N<0> J26 DSTBN0*
FSB_DSTB_L_P<0> H26 DSTBP0*
FSB_DINV_L<0> H25 DINV0*

DATA GRP 1
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L23 D20*
FSB_D_L<21> M24 D21*
FSB_D_L<22> L22 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P23 D25*
FSB_D_L<26> P22 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L25 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N25 D31*
FSB_DSTB_L_N<1> L26 DSTBN1*
FSB_DSTB_L_P<1> M26 DSTBP1*
FSB_DINV_L<1> N24 DINV1*

DATA GRP 2
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 3
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AC23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".

MISC
GTLREF AD26 CPU_GTLREF
TEST1 C23 CPU_TEST1
TEST2 D25 CPU_TEST2
TEST3 C24 TP_CPU_TEST3
TEST4 AF26 CPU_TEST4
TEST5 AF1 TP_CPU_TEST5
TEST6 A26 TP_CPU_TEST6
TEST7 C3 TP_CPU_TEST7
BSEL0 B22 CPU_BSEL<0>
BSEL1 B23 CPU_BSEL<1>
BSEL2 C21 CPU_BSEL<2>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

=PP1V05_S0_CPU
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

XDP_TMS
XDP_TDI
XDP_TDO
R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
=PP1V05_S0_CPU
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

XDP_TCK
XDP_TRST_L
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402

CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

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SCALE	SHT	OF
NONE	10	123

(CPU CORE POWER)

=PPVCORE_S0_CPU 8 11 12 45

Standard Voltage:

44.0 A (Design Target)

41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)

27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)

27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)

25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)

11.5 A (Deeper Sleep)

9.4 A (Enhanced Deeper Sleep)

Low Voltage:

23.0 A (Design Target)

21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

17.0 A (Design Target)

TBD A (HFM)
TBD A (LFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant LFM)

TBD A (Sleep HFM)
TBD A (Sleep LFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AC10, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 8 10 12 13 61

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26, C26

VID0	AD6	CPU_VID<0>	OUT 9 88
VID1	AF5	CPU_VID<1>	OUT 9 88
VID2	AE5	CPU_VID<2>	OUT 9 88
VID3	AF4	CPU_VID<3>	OUT 9 88
VID4	AE3	CPU_VID<4>	OUT 9 88
VID5	AF3	CPU_VID<5>	OUT 9 88
VID6	AE2	CPU_VID<6>	OUT 9 88
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 61 88
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 61 88

=PPVCORE_S0_CPU 8 11 12 45

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3, B1

VSS: P6, P21, P24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

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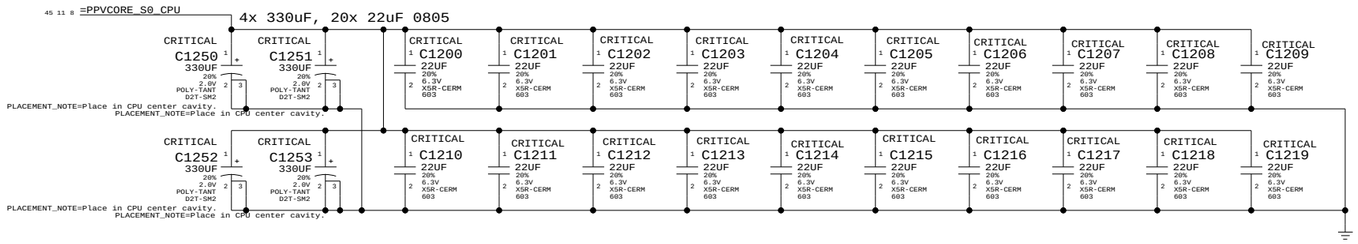
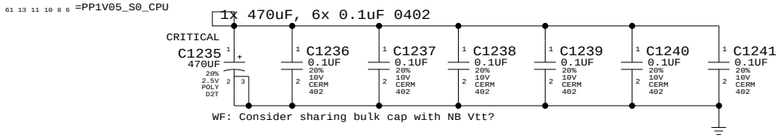
D	051-7867	01
SCALE: NONE	SHT 11 OF 123	

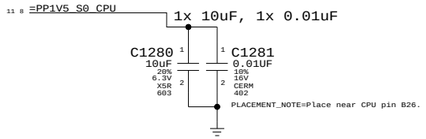
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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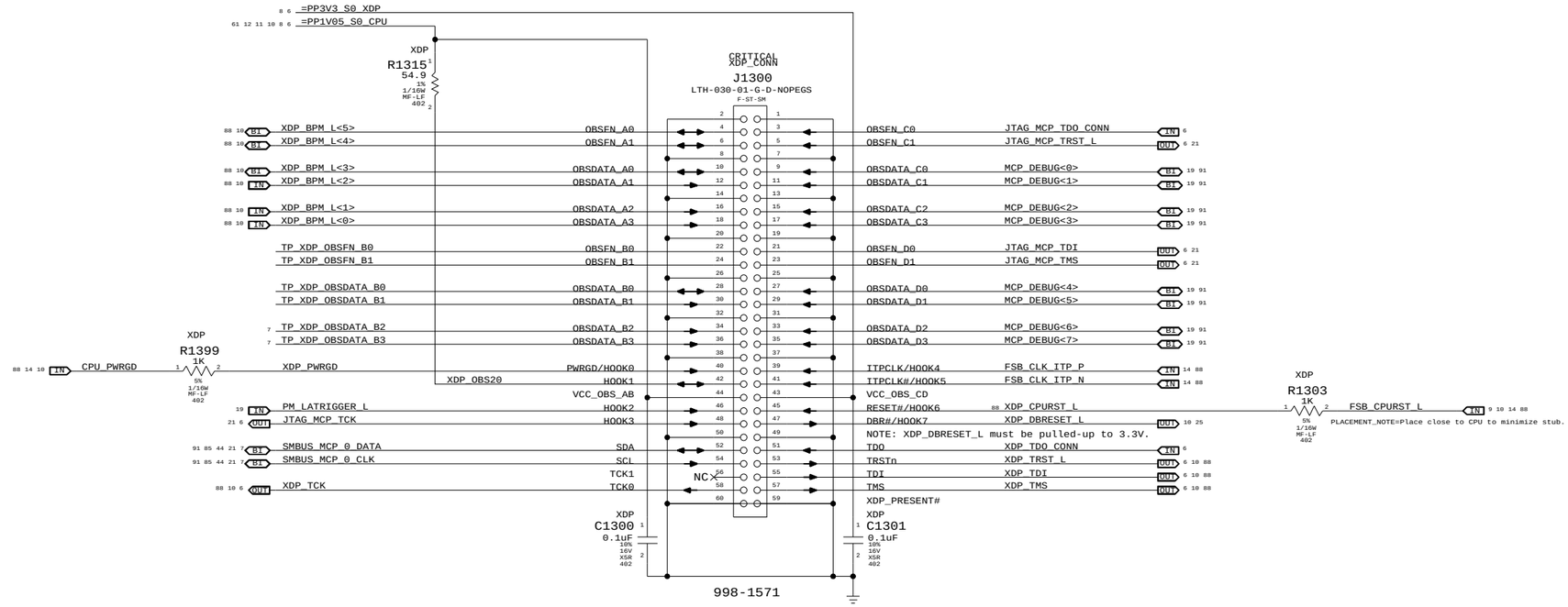
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	CPU_D0#	Y43	FSB_D_L<0>		
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	CPU_D1#	W42	FSB_D_L<1>		
FSB_DINV_L<0>	V41	CPU_DBI0#	CPU_D2#	Y40	FSB_D_L<2>		
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	CPU_D3#	W41	FSB_D_L<3>		
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	CPU_D4#	Y39	FSB_D_L<4>		
FSB_DINV_L<1>	V35	CPU_DBI1#	CPU_D5#	V42	FSB_D_L<5>		
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	CPU_D6#	Y41	FSB_D_L<6>		
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	CPU_D7#	Y42	FSB_D_L<7>		
FSB_DINV_L<2>	N35	CPU_DBI2#	CPU_D8#	P42	FSB_D_L<8>		
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	CPU_D9#	U41	FSB_D_L<9>		
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	CPU_D10#	R42	FSB_D_L<10>		
FSB_DINV_L<3>	J41	CPU_DBI3#	CPU_D11#	T39	FSB_D_L<11>		
			CPU_D12#	T42	FSB_D_L<12>		
FSB_A_L<3>	AC34	CPU_A3#	CPU_D13#	T41	FSB_D_L<13>		
FSB_A_L<4>	AE38	CPU_A4#	CPU_D14#	R41	FSB_D_L<14>		
FSB_A_L<5>	AE34	CPU_A5#	CPU_D15#	T43	FSB_D_L<15>		
FSB_A_L<6>	AC37	CPU_A6#	CPU_D16#	W35	FSB_D_L<16>		
FSB_A_L<7>	AE37	CPU_A7#	CPU_D17#	AA37	FSB_D_L<17>		
FSB_A_L<8>	AE35	CPU_A8#	CPU_D18#	W33	FSB_D_L<18>		
FSB_A_L<9>	AB35	CPU_A9#	CPU_D19#	W34	FSB_D_L<19>		
FSB_A_L<10>	AF35	CPU_A10#	CPU_D20#	AA36	FSB_D_L<20>		
FSB_A_L<11>	AG35	CPU_A11#	CPU_D21#	AA34	FSB_D_L<21>		
FSB_A_L<12>	AG39	CPU_A12#	CPU_D22#	AA38	FSB_D_L<22>		
FSB_A_L<13>	AE33	CPU_A13#	CPU_D23#	AA35	FSB_D_L<23>		
FSB_A_L<14>	AG37	CPU_A14#	CPU_D24#	U38	FSB_D_L<24>		
FSB_A_L<15>	AG38	CPU_A15#	CPU_D25#	U36	FSB_D_L<25>		
FSB_A_L<16>	AG34	CPU_A16#	CPU_D26#	U35	FSB_D_L<26>		
FSB_A_L<17>	AN38	CPU_A17#	CPU_D27#	U33	FSB_D_L<27>		
FSB_A_L<18>	AL39	CPU_A18#	CPU_D28#	U34	FSB_D_L<28>		
FSB_A_L<19>	AG33	CPU_A19#	CPU_D29#	W38	FSB_D_L<29>		
FSB_A_L<20>	AL33	CPU_A20#	CPU_D30#	R33	FSB_D_L<30>		
FSB_A_L<21>	AJ33	CPU_A21#	CPU_D31#	U37	FSB_D_L<31>		
FSB_A_L<22>	AN36	CPU_A22#	CPU_D32#	N34	FSB_D_L<32>		
FSB_A_L<23>	AJ35	CPU_A23#	CPU_D33#	N33	FSB_D_L<33>		
FSB_A_L<24>	AJ37	CPU_A24#	CPU_D34#	R34	FSB_D_L<34>		
FSB_A_L<25>	AJ36	CPU_A25#	CPU_D35#	R35	FSB_D_L<35>		
FSB_A_L<26>	AJ38	CPU_A26#	CPU_D36#	P35	FSB_D_L<36>		
FSB_A_L<27>	AL37	CPU_A27#	CPU_D37#	R39	FSB_D_L<37>		
FSB_A_L<28>	AL34	CPU_A28#	CPU_D38#	R37	FSB_D_L<38>		
FSB_A_L<29>	AN37	CPU_A29#	CPU_D39#	R38	FSB_D_L<39>		
FSB_A_L<30>	AJ34	CPU_A30#	CPU_D40#	L37	FSB_D_L<40>		
FSB_A_L<31>	AL38	CPU_A31#	CPU_D41#	L39	FSB_D_L<41>		
FSB_A_L<32>	AL35	CPU_A32#	CPU_D42#	L38	FSB_D_L<42>		
FSB_A_L<33>	AN34	CPU_A33#	CPU_D43#	N36	FSB_D_L<43>		
FSB_A_L<34>	AR39	CPU_A34#	CPU_D44#	N38	FSB_D_L<44>		
FSB_A_L<35>	AN35	CPU_A35#	CPU_D45#	J39	FSB_D_L<45>		
			CPU_D46#	J38	FSB_D_L<46>		
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	CPU_D47#	J37	FSB_D_L<47>		
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	CPU_D48#	L42	FSB_D_L<48>		
			CPU_D49#	M42	FSB_D_L<49>		
FSB_REQ_L<0>	AC38	CPU_REQ0#	CPU_D50#	P41	FSB_D_L<50>		
FSB_REQ_L<1>	AA33	CPU_REQ1#	CPU_D51#	N41	FSB_D_L<51>		
FSB_REQ_L<2>	AC39	CPU_REQ2#	CPU_D52#	N40	FSB_D_L<52>		
FSB_REQ_L<3>	AC33	CPU_REQ3#	CPU_D53#	M40	FSB_D_L<53>		
FSB_REQ_L<4>	AC35	CPU_REQ4#	CPU_D54#	H40	FSB_D_L<54>		
			CPU_D55#	K42	FSB_D_L<55>		
FSB_ADS_L	AD42	CPU_ADS#	CPU_D56#	H41	FSB_D_L<56>		
FSB_BNR_L	AD43	CPU_BNR#	CPU_D57#	L41	FSB_D_L<57>		
FSB_BREQ0_L	AE40	CPU_BR0#	CPU_D58#	H43	FSB_D_L<58>		
FSB_BREQ1_L	AL32	CPU_BR1#	CPU_D59#	H42	FSB_D_L<59>		
FSB_DBSY_L	AD39	CPU_DBSY#	CPU_D60#	K41	FSB_D_L<60>		
FSB_DRDY_L	AD41	CPU_DRDY#	CPU_D61#	J40	FSB_D_L<61>		
FSB_HIT_L	AB42	CPU_HIT#	CPU_D62#	H39	FSB_D_L<62>		
FSB_HITM_L	AD40	CPU_HITM#	CPU_D63#	M43	FSB_D_L<63>		
FSB_LOCK_L	AC43	CPU_LOCK#					
FSB_TRDY_L	AE41	CPU_TRDY#	CPU_BPRI#	AA41	FSB_BPRI_L		
			CPU_DEFER#	AA40	FSB_DEFER_L		
CPU_PECI_MCP	E41	CPU_PECI					
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P		
	AG43	CPU_THERMTRIP#	BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N		
	AH40	CPU_FERR#					
			BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P		
(MCP_BSEL<2>)	F42	CPU_BSEL2	BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N		
(MCP_BSEL<1>)	D42	CPU_BSEL1					
(MCP_BSEL<0>)	F41	CPU_BSEL0	BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P		
			BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N		
FSB_RS_L<0>	AC41	CPU_RS0#					
FSB_RS_L<1>	AB41	CPU_RS1#	BCLK_IN_N	AK41			
FSB_RS_L<2>	AC42	CPU_RS2#	BCLK_IN_P	AJ40			
PP1V05_S0_MCP_PLL_FSB							
270 mA (A01)	206 mA	AG27 +V_DLL_DLCELL_AVDD	CPU_A20M#	AF41	CPU_A20M_L		
	20 mA	AH27 +V_PLL_MCLK	CPU_IGNNE#	AH39	CPU_IGNNE_L		
	29 mA	AG28 +V_PLL_FSB	CPU_INIT#	AH42	CPU_INIT_L		
	15 mA	AH28 +V_PLL_CPU	CPU_INTR	AF42	CPU_INTR		
			CPU_NMI	AG41	CPU_NMI		
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	CPU_SMI#	AH41	CPU_SMI_L		
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND					
			CPU_PWRGD	AH43	CPU_PWRGD		
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	CPU_RESET#	H38	FSB_CPURST_L		
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND					
			CPU_SLP#	AM33	FSB_CPUSLP_L		
			CPU_DPSLP#	AN33	CPU_DPSLP_L		
			CPU_DPWR#	AM32	FSB_DPWR_L		
			CPU_STPCLK#	AG42	CPU_STPCLK_L		
			CPU_DPRSTP#	AN32	CPU_DPRSTP_L		

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

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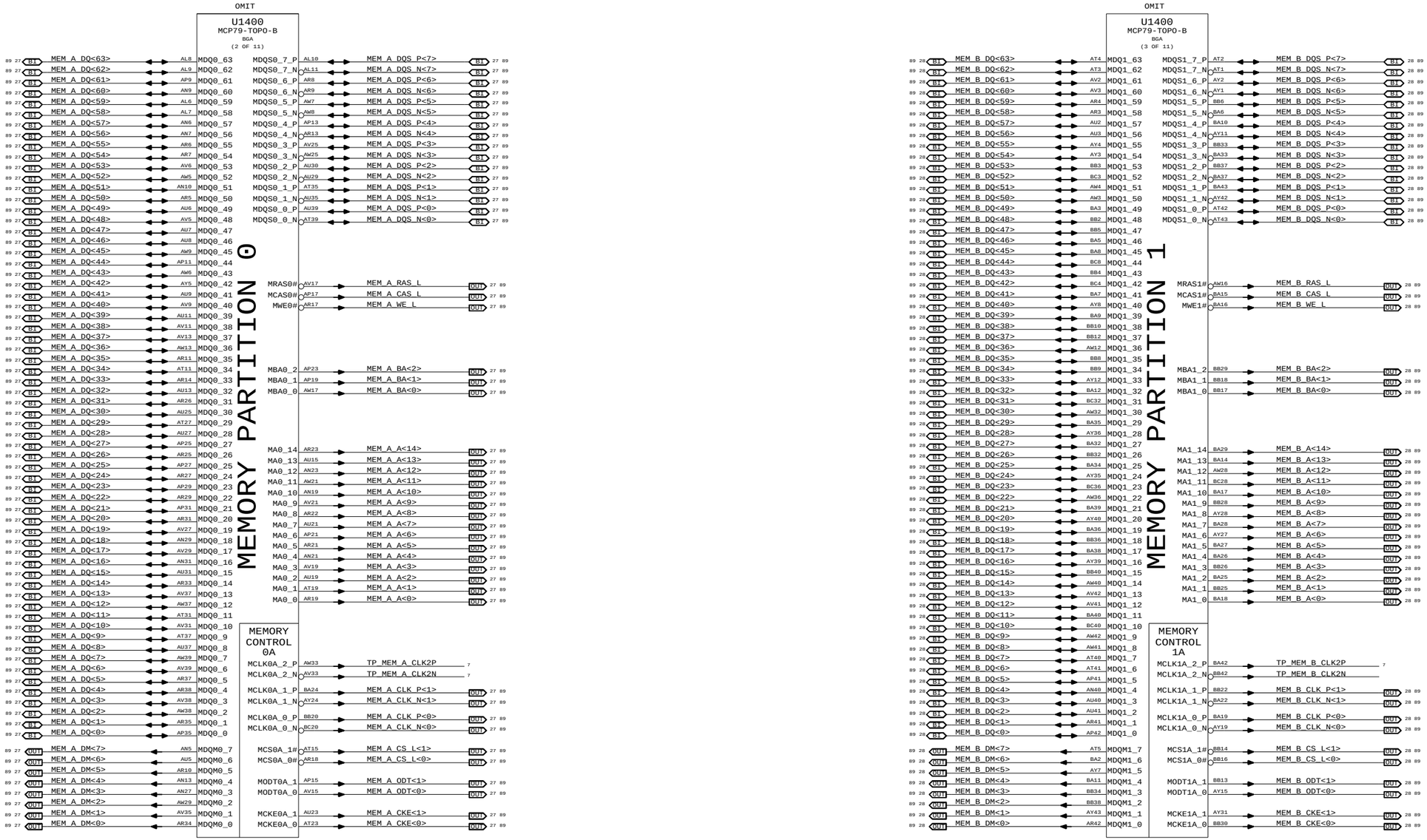
MCP CPU Interface

SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 14 OF 123	



MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	15	123

OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

7 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
7 TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
7 TP_MEM_A_CLK4P	BB24	MCLK0B_1_P	
7 TP_MEM_A_CLK4N	BC24	MCLK0B_1_N	
7 TP_MEM_A_CLK3P	BA21	MCLK0B_0_P	
7 TP_MEM_A_CLK3N	BB21	MCLK0B_0_N	
7 TP_MEM_A_CS_L<2>	AU17	MCS0B_0#	
7 TP_MEM_A_CS_L<3>	AR17	MCS0B_1#	
7 TP_MEM_A_ODT<2>	AN17	MODT0B_0	
7 TP_MEM_A_ODT<3>	AN15	MODT0B_1	
7 TP_MEM_A_CKE<2>	AV23	MCKE0B_0	
7 TP_MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

MCLK1B_2_P	BA41	TP_MEM_B_CLK5P	7
MCLK1B_2_N	BB41	TP_MEM_B_CLK5N	7
MCLK1B_1_P	AY23	TP_MEM_B_CLK4P	7
MCLK1B_1_N	BA23	TP_MEM_B_CLK4N	7
MCLK1B_0_P	BA20	TP_MEM_B_CLK3P	7
MCLK1B_0_N	AY20	TP_MEM_B_CLK3N	7
MCS1B_0#	BC16	TP_MEM_B_CS_L<2>	7
MCS1B_1#	BA13	TP_MEM_B_CS_L<3>	7
MODT1B_0	AY16	TP_MEM_B_ODT<2>	7
MODT1B_1	BC13	TP_MEM_B_ODT<3>	7
MCKE1B_0	BA30	TP_MEM_B_CKE<2>	7
MCKE1B_1	BA31	TP_MEM_B_CKE<3>	

23 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

23 16 8 =PP1V8R1V5_S0_MCP_MEM

R1610 1
40.2
1%
1/16W
MF-LF
402
2

R1611 1
40.2
1%
1/16W
MF-LF
402
2

89 MCP_MEM_COMP_VDD	AN41	MEM_COMP_VDD
89 MCP_MEM_COMP_GND	AM41	MEM_COMP_GND

MRESET0# AY32 → MCP_MEM_RESET_L (OUT) 29
TP or NC for DDR2.

=PP1V8R1V5_S0_MCP_MEM 8 16 23
4771 mA (A01, DDR3)

	AA22	GND1	+VDD_MEM1 AM17
	AP12	GND2	+VDD_MEM2 AM19
	G30	GND3	+VDD_MEM3 AM21
	P10	GND4	+VDD_MEM4 AM23
	T10	GND5	+VDD_MEM5 AM25
	T6	GND6	+VDD_MEM6 AM27
	V10	GND7	+VDD_MEM7 AM29
	V34	GND8	+VDD_MEM8 AN16
	W5	GND9	+VDD_MEM9 BC29
	AA39	GND10	+VDD_MEM10 AN20
	AB22	GND11	+VDD_MEM11 AN24
	AB7	GND12	+VDD_MEM12 AT17
	AD22	GND13	+VDD_MEM13 AP16
	AE20	GND14	+VDD_MEM14 AN22
	AF24	GND15	+VDD_MEM15 AP20
	AG24	GND16	+VDD_MEM16 AP24
	AH35	GND17	+VDD_MEM17 AV16
	AK7	GND18	+VDD_MEM18 AR16
	AM28	GND19	+VDD_MEM19 AR20
	AT25	GND20	+VDD_MEM20 AR24
	AP30	GND21	+VDD_MEM21 AW15
	AR36	GND22	+VDD_MEM22 AP22
	AU10	GND23	+VDD_MEM23 AP18
	F28	GND24	+VDD_MEM24 AU16
	BC21	GND25	+VDD_MEM25 AN18
	AY9	GND26	+VDD_MEM26 AU24
	BC9	GND27	+VDD_MEM27 AT21
	D34	GND28	+VDD_MEM28 AY29
	F24	GND29	+VDD_MEM29 AV24
	G32	GND30	+VDD_MEM30 AU20
	H31	GND31	+VDD_MEM31 AU22
	K7	GND32	+VDD_MEM32 AW27
	M38	GND33	+VDD_MEM33 BC17
	M5	GND34	+VDD_MEM34 AV20
	M6	GND35	+VDD_MEM35 AY17
	M7	GND36	+VDD_MEM36 AY18
	M9	GND37	+VDD_MEM37 AM15
	N39	GND38	+VDD_MEM38 AU18
	N8	GND39	+VDD_MEM39 AY25
	P33	GND40	+VDD_MEM40 AY26
	P34	GND41	+VDD_MEM41 AW19
	P37	GND42	+VDD_MEM42 AW24
	P4	GND43	+VDD_MEM43 BC25
	P40	GND44	+VDD_MEM44 AL30
	P7	GND45	+VDD_MEM45 AM31
	R36	GND46	
	R40	GND47	GND55 T33
	R43	GND48	GND56 T34
	R5	GND49	GND57 T35
	T18	GND50	GND58 T37
	T20	GND51	GND59 T38
	AK11	GND52	GND60 T7
	T24	GND53	GND61 T9
	T26	GND54	GND62 U18
			GND63 U20
			GND64 U22

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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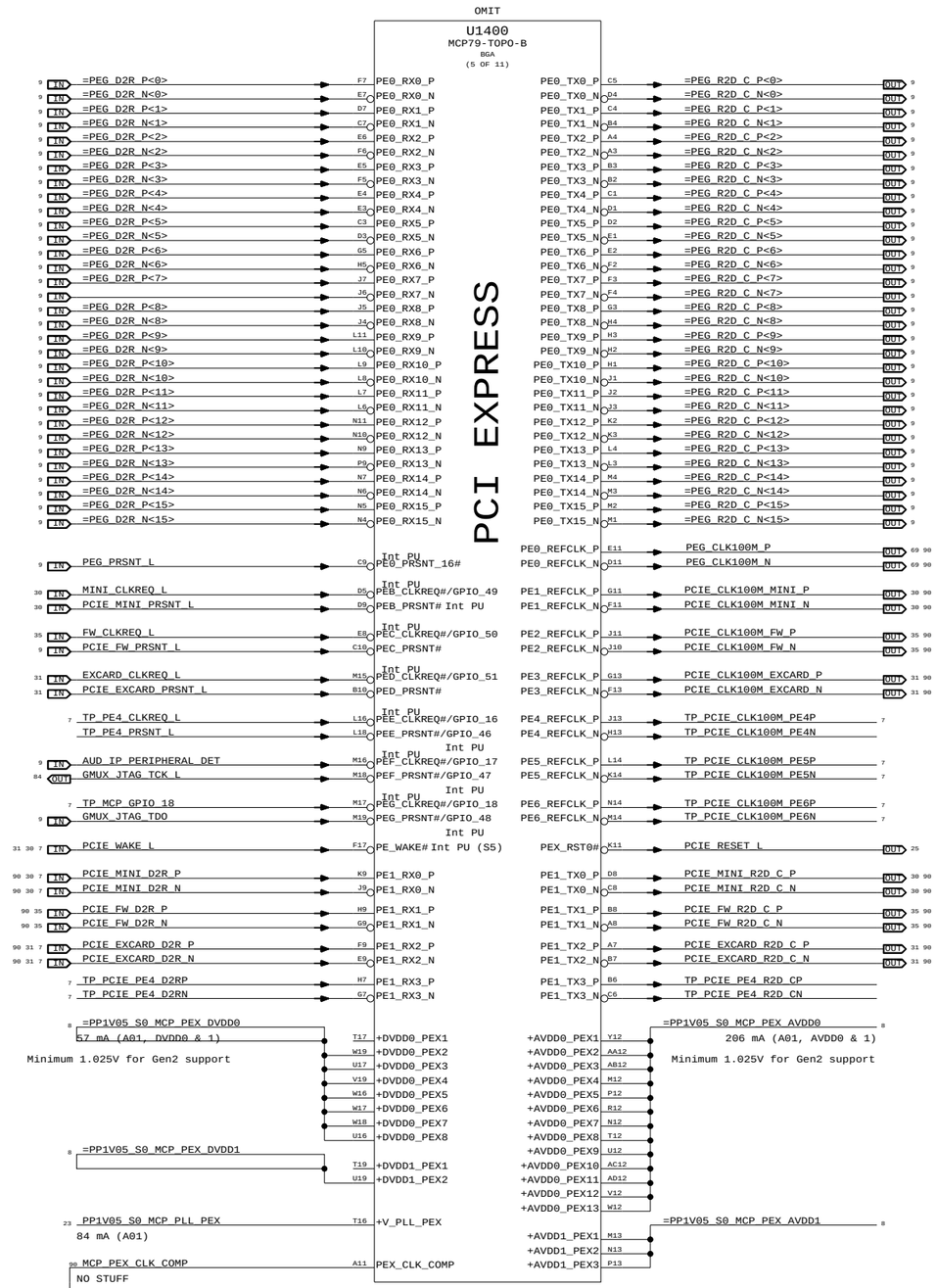
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 16 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 17 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(6 OF 11)

LAN

DACS

FLAT PANEL

=PP3V3_ENET_MCP_RMGT → +3.3V_DUAL_RMGT1 J24, +3.3V_DUAL_RMGT2 K24 — 8 18 23 — 83 mA (A01)

=PP1V05_ENET_MCP_RMGT → +V_DUAL_RMGT1 U23, +V_DUAL_RMGT2 V23 — 8 23 — 131 mA (A01)

92 32 IN	ENET_RXD<0>	C23	RGMII_RXD0
92 32 IN	ENET_RXD<1>	B23	RGMII_RXD1
92 32 IN	ENET_RXD<2>	E24	RGMII_RXD2
92 32 IN	ENET_RXD<3>	A24	RGMII_RXD3
92 32 IN	ENET_CLK125M_RXCLK	A23	RGMII_RXC/MII_RXCLK
92 32 IN	ENET_RX_CTRL	C22	RGMII_RXCTL/MII_RXDV
9 IN	=MCP_MII_RXER	F23	MII_RXER/GPIO_36
9 IN	=MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA
9 IN	=MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK
7 TP_ENET_INTR_L		J22	RGMII_INTR/GPIO_35
23 PP1V05_ENET_MCP_PLL_MAC, 5 mA (A01)		T23	+V_DUAL_MACPLL
92 MCP_MII_COMP_VDD		C27	MII_COMP_VDD
92 MCP_MII_COMP_GND		B27	MII_COMP_GND
24 TP_MCP_RGB_DAC_RSET		C39	RGB_DAC_RSET
24 TP_MCP_RGB_DAC_VREF		B38	RGB_DAC_VREF
90 24 OUT MCP_TV_DAC_RSET		E36	TV_DAC_RSET
90 24 OUT MCP_TV_DAC_VREF		A35	TV_DAC_VREF
24 IN MCP_CLK27M_XTALIN		C38	XTALIN_TV
24 OUT MCP_CLK27M_XTALOUT		D38	XTALOUT_TV
43 7 BI LPCPLUS_GPIO		E16	GPIO_6/FERR*/IGPU_GPIO_6
81 IN DP_IG_CA_DET		B15	GPIO_7/NFERR*/IGPU_GPIO_7
9 OUT LVDS_IG_BKL_PWM (See below)		G39	LCD_BKL_CTL/GPIO_57
9 OUT LVDS_IG_BKL_ON		E37	LCD_BKL_ON/GPIO_59
9 OUT LVDS_IG_PANEL_PWR		F40	LCD_PANEL_PWR/GPIO_58
9 OUT =MCP_HDMI_TXC_P		D35	HDMI_TXC_P/ML0_LANE3_P
9 OUT =MCP_HDMI_TXC_N		E35	HDMI_TXC_N/ML0_LANE3_N
9 OUT =MCP_HDMI_TXD_P<0>		G35	HDMI_TXD0_P/ML0_LANE2_P
9 OUT =MCP_HDMI_TXD_N<0>		F35	HDMI_TXD0_N/ML0_LANE2_N
9 OUT =MCP_HDMI_TXD_P<1>		F33	HDMI_TXD1_P/ML0_LANE1_P
9 OUT =MCP_HDMI_TXD_N<1>		G33	HDMI_TXD1_N/ML0_LANE1_N
9 OUT =MCP_HDMI_TXD_P<2>		J33	HDMI_TXD2_P/ML0_LANE0_P
9 OUT =MCP_HDMI_TXD_N<2>		H33	HDMI_TXD2_N/ML0_LANE0_N
90 81 OUT DP_IG_AUX_CH_P		D43	DP_AUX_CH0_P
90 81 OUT DP_IG_AUX_CH_N		C43	DP_AUX_CH0_N
9 IN =DVI_HPD_GMUX_INT (See below)		C31	HPLUG_DET2/GPIO_22
9 IN =MCP_HDMI_HPD		F31	HPLUG_DET3
24 8 =PP3V3R1V8_S0_MCP_IFP_VDD, 190 mA (A01, 1.8V)		M27	+VDD_IFPA
		M26	+VDD_IFPB
24 PP3V3_S0_MCP_VPLL, 16 mA (A01)	8 mA	M28	+V_PLL_IFPAB
	8 mA	M29	+V_PLL_HDMI
24 8 =PP1V05_S0_MCP_HDMI_VDD, 95 mA (A01)		T25	+VDD_HDMI
90 24 OUT MCP_HDMI_RSET		J31	HDMI_RSET
90 24 OUT MCP_HDMI_VPROBE		J30	HDMI_VPROBE

MII_VREF	E28	MCP_MII_VREF	23 IN
RGMII_TXD0	B24	ENET_TXD<0>	OUT 32 92
RGMII_TXD1	C24	ENET_TXD<1>	OUT 32 92
RGMII_TXD2	C25	ENET_TXD<2>	OUT 32 92
RGMII_TXD3	D25	ENET_TXD<3>	OUT 32 92
RGMII_TXC/MII_TXCLK	D24	ENET_CLK125M_TXCLK	OUT 32 92
RGMII_TXCTL/MII_TXEN	C26	ENET_TX_CTRL	OUT 32 92
RGMII_MDC	D21	ENET_MDC	OUT 32 92
RGMII_MDIO	C21	ENET_MDIO	BI 32 92
RGMII_PWRDWN/GPIO_37	G23	TP_ENET_PWRDWN_L	7
BUF_25MHZ	E23	MCP_CLK25M_BUF0_R	OUT 33 92
MII_RESET#	J23	ENET_RESET_L	OUT 32 92
+V_RGB_DAC	J32	PP3V3_S0_MCP_DAC 24, 103 mA	206 mA (A01)
+V_TV_DAC	K32	103 mA	
DDC_CLK0	B31	MCP_DDC_CLK0	
DDC_DATA0	A31	MCP_DDC_DATA0	
RGB_DAC_RED	B39	TP_MCP_RGB_RED	24
RGB_DAC_GREEN	A39	TP_MCP_RGB_GREEN	24
RGB_DAC_BLUE	B40	TP_MCP_RGB_BLUE	24
RGB_DAC_HSYNC	A40	TP_MCP_RGB_HSYNC	24
RGB_DAC_VSYNC	A41	TP_MCP_RGB_VSYNC	24
TV_DAC_RED	A36	CRT_IG_R_C_PR	OUT 24 90
TV_DAC_GREEN	B36	CRT_IG_G_Y_Y	OUT 24 90
TV_DAC_BLUE	C36	CRT_IG_B_COMP_PB	OUT 24 90
TV_DAC_HSYNC/GPIO_44	D36	CRT_IG_HSYNC	OUT 24 90
TV_DAC_VSYNC/GPIO_45	C37	CRT_IG_VSYNC	OUT 24 90
IFPA_TXC_P	B35	LVDS_IG_A_CLK_P	OUT 84 90
IFPA_TXC_N	C35	LVDS_IG_A_CLK_N	OUT 84 90
IFPA_TXD0_P	B32	LVDS_IG_A_DATA_P<0>	OUT 84 90
IFPA_TXD0_N	A32	LVDS_IG_A_DATA_N<0>	OUT 84 90
IFPA_TXD1_P	D32	LVDS_IG_A_DATA_P<1>	OUT 84 90
IFPA_TXD1_N	C32	LVDS_IG_A_DATA_N<1>	OUT 84 90
IFPA_TXD2_P	D33	LVDS_IG_A_DATA_P<2>	OUT 84 90
IFPA_TXD2_N	C33	LVDS_IG_A_DATA_N<2>	OUT 84 90
IFPA_TXD3_P	B34	LVDS_IG_A_DATA_P<3>	OUT 9 90
IFPA_TXD3_N	C34	LVDS_IG_A_DATA_N<3>	OUT 9 90
IFPB_TXC_P	L31	LVDS_IG_B_CLK_P	OUT 9 90
IFPB_TXC_N	K31	LVDS_IG_B_CLK_N	OUT 9 90
IFPB_TXD4_P	J29	LVDS_IG_B_DATA_P<0>	OUT 84 90
IFPB_TXD4_N	H29	LVDS_IG_B_DATA_N<0>	OUT 84 90
IFPB_TXD5_P	L29	LVDS_IG_B_DATA_P<1>	OUT 84 90
IFPB_TXD5_N	K29	LVDS_IG_B_DATA_N<1>	OUT 84 90
IFPB_TXD6_P	L30	LVDS_IG_B_DATA_P<2>	OUT 84 90
IFPB_TXD6_N	K30	LVDS_IG_B_DATA_N<2>	OUT 84 90
IFPB_TXD7_P	N30	LVDS_IG_B_DATA_P<3>	OUT 9 90
IFPB_TXD7_N	M30	LVDS_IG_B_DATA_N<3>	OUT 9 90
DDC_CLK2/GPIO_23	C30	LVDS_IG_DDC_CLK	OUT 81
DDC_DATA2/GPIO_24	B30	LVDS_IG_DDC_DATA	BI 81
DDC_CLK3	D31	=MCP_HDMI_DDC_CLK	OUT 9
DDC_DATA3	E31	=MCP_HDMI_DDC_DATA	BI 9
IFPAB_RSET	E32	MCP_IFPAB_RSET	OUT 24 90
IFPAB_VPROBE	G31	MCP_IFPAB_VPROBE	OUT 24 90

RGB ONLY

TV / Component
C / Pr
Y / Y
Comp / Pb

R1850 10K 5% 1/16W MF-LF 402 — 1 — 2

R1810 49.9 1% 1/16W MF-LF 402 — 23 18 8 =PP3V3_ENET_MCP_RMGT — 2

R1811 49.9 1% 1/16W MF-LF 402 — 1 — 2

R1820 47K 5% 1/16W MF-LF 402 — 20 8 =PP3V3_S5_MCP_GPIO — 2

R1860 100K 5% 1/16W MF-LF 402 — 1 — 2

R1861 100K 5% 1/16W MF-LF 402 — 1 — 2 — =PP3V3_S0_MCP_GPIO 8 19 21

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP not used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 18 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
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PCI

91 19	PCI_REQ0_L	T2	PCI_REQ0#		
91 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2		
19	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT0# R3	TP_PCI_GNT0_L 7
58 9	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT1#/FANCTL2 U10	TP_PCI_GNT1_L 7
19	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT2#/GPIO_41/RS232_DTR# R4	GMUX_JTAG_TMS 9
				PCI_GNT3#/GPIO_39/RS232_RTS# U11	GMUX_JTAG_TDI 9
				PCI_GNT4#/GPIO_53/RS232_SOUT# P3	MCP_RS232_SOUT_L 19
91 13	MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0# AA3	TP_PCI_C_BE_L<0> 7
91 13	MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1# AA6	TP_PCI_C_BE_L<1> 7
91 13	MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2# AA11	TP_PCI_C_BE_L<2> 7
91 13	MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3# W10	TP_PCI_C_BE_L<3> 7
91 13	MCP_DEBUG<4>	AB3	PCI_AD4		
91 13	MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL# AA9	TP_PCI_DEVSEL_L 7
91 13	MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME# Y4	TP_PCI_FRAME_L 7
91 13	MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY# AA10	TP_PCI_IRDY_L 7
7	TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR Y1	TP_PCI_PAR 7
7	TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD# AB9	TP_PCI_PERR_L 7
7	TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR# AA7	TP_PCI_SERR_L 7
7	TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP# Y2	TP_PCI_STOP_L 7
7	TP_PCI_AD<12>	AC11	PCI_AD12	PCI_PME#/GPIO_30 T1	PM_LATRIGGER_L 13
7	TP_PCI_AD<13>	AA1	PCI_AD13	Int PU (S5)	
7	TP_PCI_AD<14>	AA5	PCI_AD14		
7	TP_PCI_AD<15>	Y5	PCI_AD15	PCI_RESET0# R10	MEM_VTT_EN_R 25
7	TP_PCI_AD<16>	W3	PCI_AD16	PCI_RESET1# R11	TP_PCI_RESET1_L 7
7	TP_PCI_AD<17>	W6	PCI_AD17		
7	TP_PCI_AD<18>	W4	PCI_AD18		
7	TP_PCI_AD<19>	W7	PCI_AD19	PCI_CLK0 R6	TP_PCI_CLK0 7
7	TP_PCI_AD<20>	V3	PCI_AD20	PCI_CLK1 R7	TP_PCI_CLK1 7
7	TP_PCI_AD<21>	W8	PCI_AD21	PCI_CLK2 R8	91 PCI_CLK33M_MCP_R
7	TP_PCI_AD<22>	V2	PCI_AD22		
7	TP_PCI_AD<23>	W9	PCI_AD23		
7	TP_PCI_AD<24>	U3	PCI_AD24		
7	TP_PCI_AD<25>	W11	PCI_AD25		
7	TP_PCI_AD<26>	U2	PCI_AD26		
7	TP_PCI_AD<27>	U5	PCI_AD27		
7	TP_PCI_AD<28>	U1	PCI_AD28		
7	TP_PCI_AD<29>	U6	PCI_AD29		
7	TP_PCI_AD<30>	T5	PCI_AD30		
7	TP_PCI_AD<31>	U7	PCI_AD31		
7	TP_PCI_INTW_L	P2	PCI_INTW#		
7	TP_PCI_INTX_L	N3	PCI_INTX#		
7	TP_PCI_INTY_L	N2	PCI_INTY#		
7	TP_PCI_INTZ_L	N1	PCI_INTZ#		
7	TP_PCI_TRDY_L	Y3	PCI_TRDY#		

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

PCI_CLKIN R9 — 91 PCI_CLK33M_MCP

LPC

43 41 7	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	LPC_FRAME# AD4	LPC_FRAME_R_L 13 — R1960 22 5% 1/16W MF-LF 402 — LPC_FRAME_L 7 41 43 84 91
35	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU	LPC_PWRDWN#/GPIO_54/EXT_NMI# AE12	LPC_PWRDWN_L 7 41 43
7	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	LPC_RESET0# AE5	LPC_RESET_L 25 84 91
43 41 7	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	LPC_AD0 AD3	LPC_AD_R<0> R1950 22 5% 1/16W MF-LF 402 — LPC_AD<0> 7 41 43 84 91
				LPC_AD1 AD2	LPC_AD_R<1> R1951 22 5% 1/16W MF-LF 402 — LPC_AD<1> 7 41 43 84 91
				LPC_AD2 AD1	LPC_AD_R<2> R1952 22 5% 1/16W MF-LF 402 — LPC_AD<2> 7 41 43 84 91
				LPC_AD3 AD5	LPC_AD_R<3> R1953 22 5% 1/16W MF-LF 402 — LPC_AD<3> 7 41 43 84 91
				LPC_CLK0 AE9	LPC_CLK33M_SMC_R 25 91

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	Y26	GND98
U26	GND66	Y27	GND99
U39	GND67	AB18	GND100
U4	GND68	H34	GND101
U8	GND69	AB20	GND102
V16	GND70	AB21	GND103
V17	GND71	AB23	GND104
V18	GND72	AB24	GND105
V20	GND73	AB25	GND106
V22	GND74	AB26	GND107
V24	GND75	AB27	GND108
V26	GND76	AB28	GND109
V27	GND77	AB34	GND110
V28	GND78	AB37	GND111
V33	GND79	AB4	GND112
V37	GND80	AB40	GND113
V4	GND81	AC22	GND114
V40	GND82	AC36	GND115
V7	GND83	AC40	GND116
W20	GND84	AB33	GND117
W22	GND85	AC5	GND118
W24	GND86	AD16	GND119
W36	GND87	AD17	GND120
W40	GND88	AD18	GND121
W43	GND89	AD19	GND122
Y16	GND90	AD20	GND123
Y17	GND91	AD24	GND124
Y18	GND92	AD25	GND125
Y19	GND93	AD26	GND126
Y20	GND94	AD27	GND127
Y22	GND95	AD28	GND128
Y24	GND96	AD33	GND129
Y25	GND97	AD34	GND130

21 18 8 =PP3V3_S0_MCP_GPIO

19	MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
91 19	PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
91 19	PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
19	CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402
19	MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

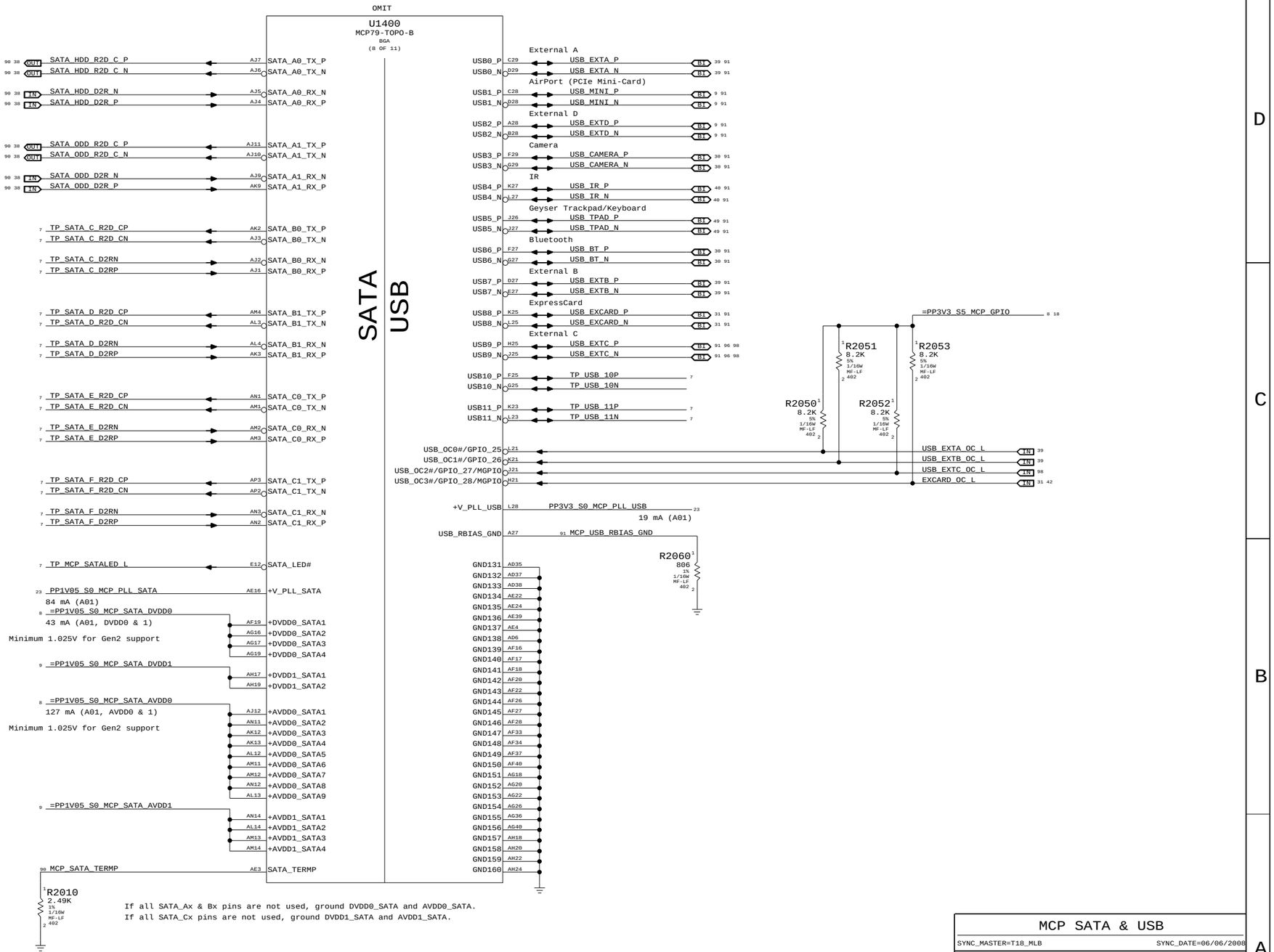
MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	19	123



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 20 OF 123	

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

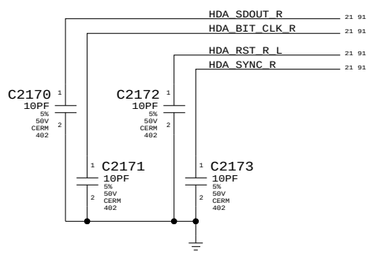
SPI Frequency Select

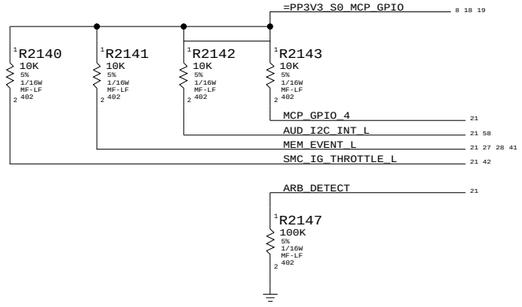
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

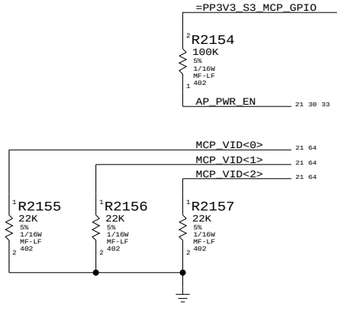
NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface







Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 21 OF 123

OMIT

U1400
MCP79-TOPO-B
BGA
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GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

45 23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59		
AG8	+VDD_CORE60		
AG9	+VDD_CORE61		
AH1	+VDD_CORE62		
AH10	+VDD_CORE63		
AH11	+VDD_CORE64		
W26	+VDD_CORE65		
AH2	+VDD_CORE66		
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AH25	+VDD_CORE69		
AH21	+VDD_CORE70	+3.3V_DUAL1	G10
AH3	+VDD_CORE71	+3.3V_DUAL2	H19
AH4	+VDD_CORE72	+3.3V_DUAL3	J20
AH5	+VDD_CORE73	+3.3V_DUAL4	K20
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
		+VDD_AUXC1	T21
		+VDD_AUXC2	U21
A20	+VBAT	+VDD_AUXC3	V21

=PP1V05_S0_MCP_FSB
8 9 14 23
1139 mA
1182 mA (A01)

=PP3V3_S0_MCP
8 21 23
450 mA (A01)

=PP3V3_S5_MCP
8 23
16 mA
266 mA (A01)

250 mA

=PP1V05_S5_MCP_VDD_AUXC
8 23
105 mA (A01)

25 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 22 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

45 22 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

8 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

8 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

22 8 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

18 8 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

22 14 9 8 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

16 8 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

22 21 8 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22 8 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21 8 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

8 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
18
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

23 18 8 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

23 18 8 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
OUT 18
C2591 0.1UF 20% 10V CERM 402

MCP 3.3V RTC Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

L2555 30-OHM-1.7A 0402

8 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
20
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 1.05V PLL Power

L2570 30-OHM-5A 0603

8 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8
206 mA (A01)

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8
127 mA (A01)

MCP 1.05V PLL Power

L2582 30-OHM-1.7A 0402

8 =PP1V05_S0_MCP_PLL_PEX_UF

C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
17
84 mA (A01)

R2580 0.2 1% 1/5W MF 402-HF

66 8 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 10% 16V X5R 603

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
14
270 mA (A01)

L2584 30-OHM-1.7A 0402

C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
20
84 mA (A01)

L2586 30-OHM-1.7A 0402

C2586 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
16
87 mA (A01)

L2588 30-OHM-1.7A 0402

C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 6.3V CERM 402-LF
C2590 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
21
37 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 25 OF 123	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18 8 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610 2.2UF 20% 6.3V CERM 402-LF

18 8 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615 4.7UF 20% 4V X5R 402
C2616 2.2UF 20% 6.3V CERM 402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE

NO STUFF
C2620 0.1UF 20% 10V CERM 402
R2620 1K 1% 1/16W MF-LF 402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE

NO STUFF
C2630 0.1UF 20% 10V CERM 402
NO STUFF
R2630 1K 1% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640 30-OHM-1.7A 0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18
16 mA (A01)

C2640 4.7UF 20% 6.3V CERM 603
C2641 2.2UF 20% 6.3V CERM 402-LF

8 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

NO STUFF
L2650 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18
206 mA (A01)

NO STUFF
C2650 2.2UF 20% 6.3V CERM 402-LF
R2651 0 5% 1/10W MF-LF 402

18 TP_MCP_RGB_RED — NC_MCP_RGB_RED
18 TP_MCP_RGB_GREEN — NC_MCP_RGB_GREEN
18 TP_MCP_RGB_BLUE — NC_MCP_RGB_BLUE
18 TP_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC
18 TP_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC
90 18 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR
90 18 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y
90 18 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB
90 18 CRT_IG_HSYNC — NC_CRT_IG_HSYNC
90 18 — NC_CRT_IG_VSYNC
18 TP_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET
18 TP_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF
90 18 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET
90 18 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF
18 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN
18 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT

(MAKE_BASE=TRUE, NO_TEST=TRUE)

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

8 =PP3V3_S0_HDCPROM

C2690 0.1UF 20% 10V CERM 402

OMIT

U2695 AT24C08 SOIC
VCC, A0, A1, A2, SDA, SCL, WP, GND

=I2C_HDCPROM_SDA — B 44
=I2C_HDCPROM_SCL — TN 44
HDCPROM_WP

R2690 10K 5% 1/16W MF-LF 402

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

MCP Graphics Support

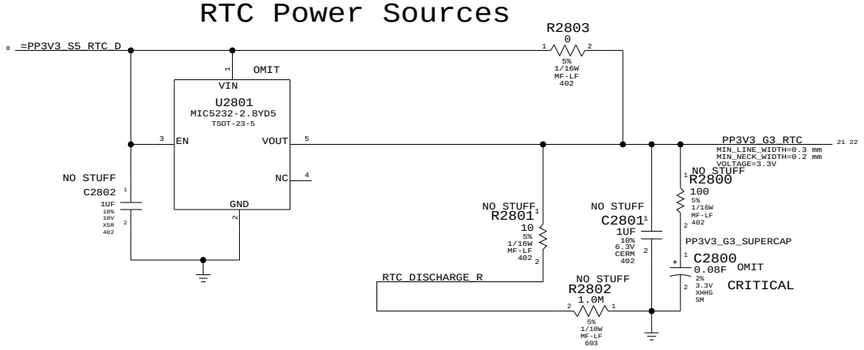
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

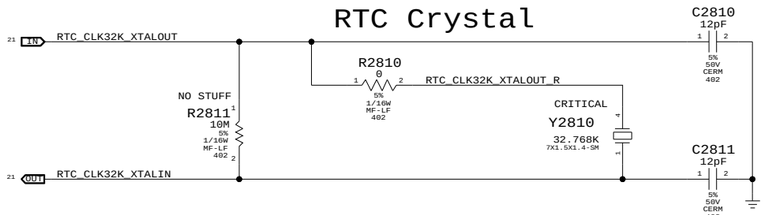
SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	26	123

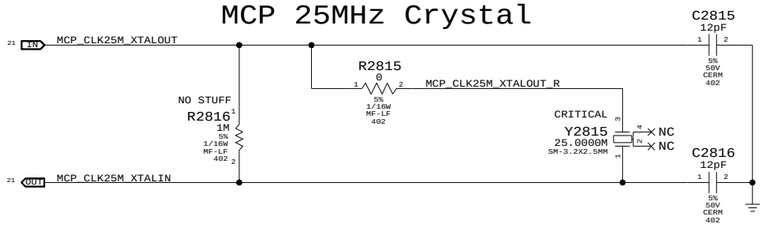
RTC Power Sources



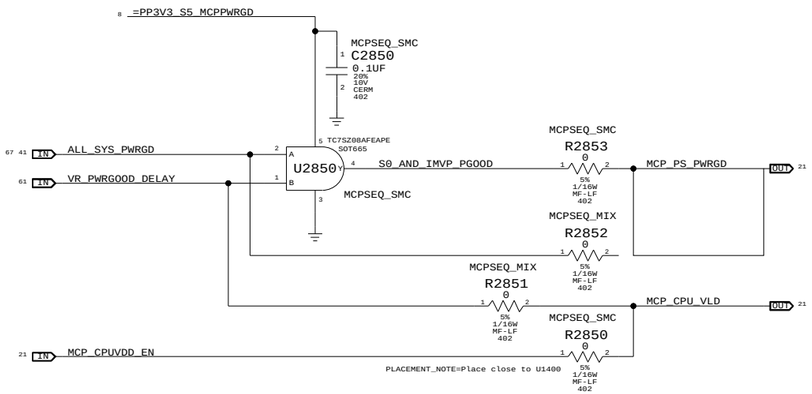
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

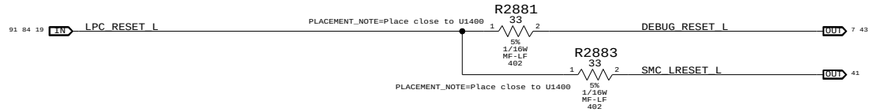
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

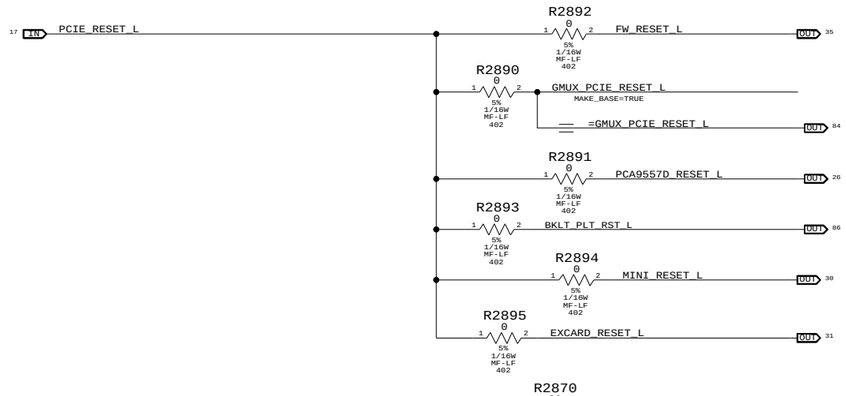
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

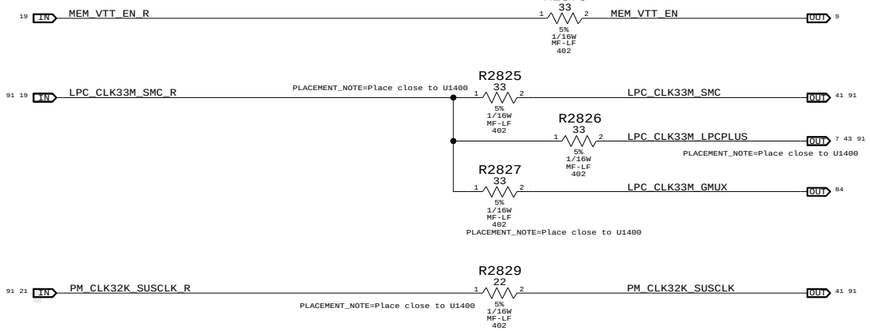
Platform Reset Connections

LPC Reset (Unbuffered)

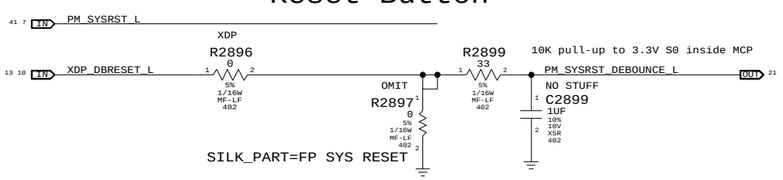


PCIE Reset (Unbuffered)





Reset Button



SB Misc		
SYNC_MASTER=M98_MLB		SYNC_DATE=05/01/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7867	01
	SCALE: NONE	SHT 28 OF 123	

Page Notes

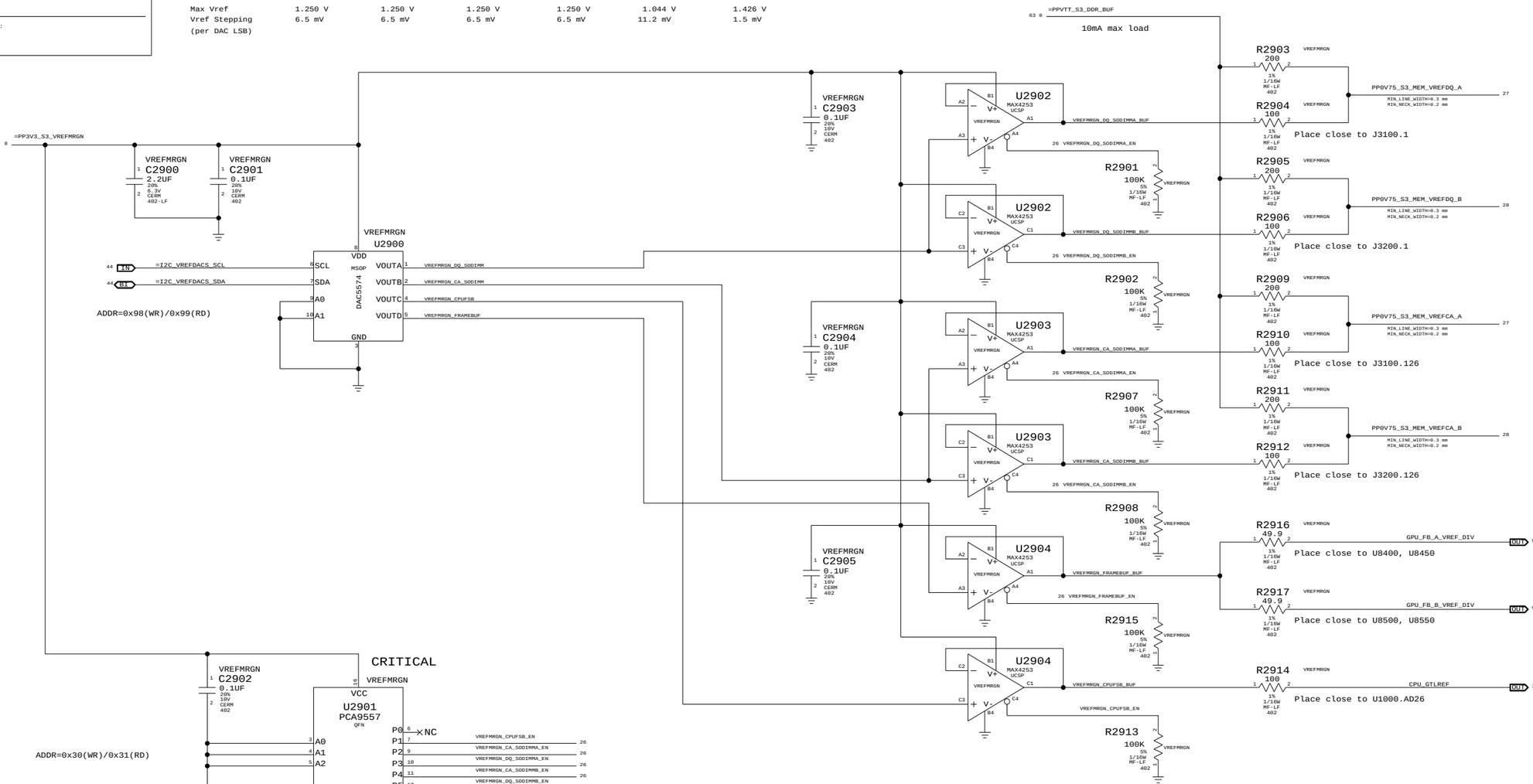
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 29 OF 123

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_A

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2) F-RT-THB

KEY

		NC	73
89 15 IN	MEM_A_CKE<0>	CKE0	73
		VDD	75
		NC	77
89 15 IN	MEM_A_BA<2>	BA2	79
		VDD	81
89 15 IN	MEM_A_A<12>	A12/BC*	83
89 15 IN	MEM_A_A<9>	A9	85
		VDD	87
89 15 IN	MEM_A_A<8>	A8	89
89 15 IN	MEM_A_A<5>	A5	91
		VDD	93
89 15 IN	MEM_A_A<3>	A3	95
89 15 IN	MEM_A_A<1>	A1	97
		VDD	99
89 15 IN	MEM_A_CLK_P<0>	CK0	101
89 15 IN	MEM_A_CLK_N<0>	CK0*	103
		VDD	105
89 15 IN	MEM_A_A<10>	A10/AP	107
89 15 IN	MEM_A_BA<0>	BA0	109
		VDD	111
89 15 IN	MEM_A_WE_L	WE*	113
89 15 IN	MEM_A_CAS_L	CAS*	115
		VDD	117
89 15 IN	MEM_A_A<13>	A13	119
89 15 IN	MEM_A_CS_L<1>	S1*	121
		VDD	123
NC		TEST	125
		VSS	127
89 15 BI	MEM_A_DQ<33>	DQ32	129
89 15 BI	MEM_A_DQ<32>	DQ33	131
		VSS	133
89 15 BI	MEM_A_DQS_N<4>	DQS4*	135
89 15 BI	MEM_A_DQS_P<4>	DQS4	137
		VSS	139
89 15 BI	MEM_A_DQ<34>	DQ34	141
89 15 BI	MEM_A_DQ<35>	DQ35	143
		VSS	145
89 15 BI	MEM_A_DQ<44>	DQ40	147
89 15 BI	MEM_A_DQ<41>	DQ41	149
		VSS	151
89 15 IN	MEM_A_DM<5>	DM5	153
		VSS	155
89 15 BI	MEM_A_DQ<45>	DQ42	157
89 15 BI	MEM_A_DQ<42>	DQ43	159
		VSS	161
89 15 BI	MEM_A_DQ<52>	DQ48	163
89 15 BI	MEM_A_DQ<51>	DQ49	165
		VSS	167
89 15 BI	MEM_A_DQS_N<6>	DQS6*	169
89 15 BI	MEM_A_DQS_P<6>	DQS6	171
		VSS	173
89 15 BI	MEM_A_DQ<55>	DQ50	175
89 15 BI	MEM_A_DQ<54>	DQ51	177
		VSS	179
89 15 BI	MEM_A_DQ<61>	DQ56	181
89 15 BI	MEM_A_DQ<60>	DQ57	183
		VSS	185
89 15 IN	MEM_A_DM<7>	DM7	187
		VSS	189
89 15 BI	MEM_A_DQ<58>	DQ58	191
89 15 BI	MEM_A_DQ<59>	DQ59	193
		VSS	195
MEM_A_SA<0>		SA0	197
8 =PPSPD_S0_MEM_A		VDDSPD	199
MEM_A_SA<1>		SA1	201
=PP0V75_S0_MEM_VTT_A 8		VTT	203

		CKE1	74
		VDD	76
		A15	78
89 15 IN	MEM_A_CKE<1>	A14	80
		VDD	82
89 15 IN	MEM_A_A<15>	A11	84
89 15 IN	MEM_A_A<14>	A7	86
		VDD	88
89 15 IN	MEM_A_A<11>	A6	90
89 15 IN	MEM_A_A<7>	A4	92
		VDD	94
89 15 IN	MEM_A_A<6>	A2	96
89 15 IN	MEM_A_A<4>	A0	98
		VDD	100
89 15 IN	MEM_A_A<2>	CK1	102
89 15 IN	MEM_A_A<0>	CK1*	104
		VDD	106
89 15 IN	MEM_A_CLK_P<1>	BA1	108
89 15 IN	MEM_A_CLK_N<1>	RAS*	110
		VDD	112
89 15 IN	MEM_A_BA<1>	S0*	114
89 15 IN	MEM_A_RAS_L	ODT0	116
		VDD	118
89 15 IN	MEM_A_CS_L<0>	ODT1	120
89 15 IN	MEM_A_ODT<0>	NC	122
		VDD	124
89 15 IN	MEM_A_ODT<1>	VREFCA	126
		VSS	128
MEM_A_DQ<36> 89 15 BI		DQ36	130
MEM_A_DQ<37> 89 15 BI		DQ37	132
		VSS	134
MEM_A_DM<4> 89 15 IN		DM4	136
		VSS	138
MEM_A_DQ<38> 89 15 BI		DQ38	140
MEM_A_DQ<39> 89 15 BI		DQ39	142
		VSS	144
MEM_A_DQ<47> 89 15 BI		DQ44	146
MEM_A_DQ<40> 89 15 BI		DQ45	148
		VSS	150
MEM_A_DQS_N<5> 89 15 BI		DQS5*	152
MEM_A_DQS_P<5> 89 15 BI		DQS5	154
		VSS	156
MEM_A_DQ<46> 89 15 BI		DQ46	158
MEM_A_DQ<43> 89 15 BI		DQ47	160
		VSS	162
MEM_A_DQ<48> 89 15 BI		DQ52	164
MEM_A_DQ<53> 89 15 BI		DQ53	166
		VSS	168
MEM_A_DM<6> 89 15 IN		DM6	170
		VSS	172
MEM_A_DQ<50> 89 15 BI		DQ54	174
MEM_A_DQ<49> 89 15 BI		DQ55	176
		VSS	178
MEM_A_DQ<57> 89 15 BI		DQ60	180
MEM_A_DQ<56> 89 15 BI		DQ61	182
		VSS	184
MEM_A_DQS_N<7> 89 15 BI		DQS7*	186
MEM_A_DQS_P<7> 89 15 BI		DQS7	188
		VSS	190
MEM_A_DQ<62> 89 15 BI		DQ62	192
MEM_A_DQ<63> 89 15 BI		DQ63	194
		VSS	196
MEM_EVENT_L OUT 21 28 41		EVENT*	198
=I2C_SODIMMA_SDA BI 44		SDA	200
=I2C_SODIMMA_SCL IN 44		SCL	202
		VTT	204

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2) F-RT-THB

CRITICAL

		VREFDQ	1
		VSS	3
MEM_A_DQ<0> 89 15 BI		DQ0	5
MEM_A_DQ<1> 89 15 BI		DQ1	7
		VSS	9
MEM_A_DM<0> 89 15 IN		DM0	11
		VSS	13
MEM_A_DQ<3> 89 15 BI		DQ2	15
MEM_A_DQ<2> 89 15 BI		DQ3	17
		VSS	19
MEM_A_DQ<9> 89 15 BI		DQ8	21
MEM_A_DQ<13> 89 15 BI		DQ9	23
		VSS	25
MEM_A_DQS_N<1> 89 15 BI		DQS1*	27
MEM_A_DQS_P<1> 89 15 BI		DQS1	29
		VSS	31
MEM_A_DQ<11> 89 15 BI		DQ10	33
MEM_A_DQ<14> 89 15 BI		DQ11	35
		VSS	37
MEM_A_DQ<16> 89 15 BI		DQ16	39
MEM_A_DQ<18> 89 15 BI		DQ17	41
		VSS	43
MEM_A_DQS_N<2> 89 15 BI		DQS2*	45
MEM_A_DQS_P<2> 89 15 BI		DQS2	47
		VSS	49
MEM_A_DQ<23> 89 15 BI		DQ18	51
MEM_A_DQ<19> 89 15 BI		DQ19	53
		VSS	55
MEM_A_DQ<24> 89 15 BI		DQ24	57
MEM_A_DQ<30> 89 15 BI		DQ25	59
		VSS	61
MEM_A_DM<3> 89 15 IN		DM3	63
		VSS	65
MEM_A_DQ<27> 89 15 BI		DQ26	67
MEM_A_DQ<25> 89 15 BI		DQ27	69
		VSS	71

		VSS	2
MEM_A_DQ<4> 89 15 BI		DQ4	4
MEM_A_DQ<5> 89 15 BI		DQ5	6
		VSS	8
MEM_A_DQS_N<0> 89 15 BI		DQS0*	10
MEM_A_DQS_P<0> 89 15 BI		DQS0	12
		VSS	14
MEM_A_DQ<6> 89 15 BI		DQ6	16
MEM_A_DQ<7> 89 15 BI		DQ7	18
		VSS	20
MEM_A_DQ<8> 89 15 BI		DQ12	22
MEM_A_DQ<12> 89 15 BI		DQ13	24
		VSS	26
MEM_A_DM<1> 89 15 IN		DM1	28
MEM_RESET_L 28 29		RESET*	30
		VSS	32
MEM_A_DQ<15> 89 15 BI		DQ14	34
MEM_A_DQ<10> 89 15 BI		DQ15	36
		VSS	38
MEM_A_DQ<21> 89 15 BI		DQ20	40
MEM_A_DQ<20> 89 15 BI		DQ21	42
		VSS	44
MEM_A_DM<2> 89 15 IN		DM2	46
		VSS	48
MEM_A_DQ<17> 89 15 BI		DQ22	50
MEM_A_DQ<22> 89 15 BI		DQ23	52
		VSS	54
MEM_A_DQ<29> 89 15 BI		DQ28	56
MEM_A_DQ<28> 89 15 BI		DQ29	58
		VSS	60
MEM_A_DQS_N<3> 89 15 BI		DQS3*	62
MEM_A_DQS_P<3> 89 15 BI		DQS3	64
		VSS	66
MEM_A_DQ<26> 89 15 BI		DQ30	68
MEM_A_DQ<31> 89 15 BI		DQ31	70
		VSS	72

KEY

516-0201

PP0V75_S3_MEM_VREFCA_A 26

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 31 OF 123	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

KEY

		73	CKE0	CKE1	74	
		75	VDD	VDD	76	
		77	NC	A15	78	MEM_B_A<15> IN 9
89 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14> IN 15 89
		81	VDD	VDD	82	
89 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11> IN 15 89
89 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7> IN 15 89
		87	VDD	VDD	88	
89 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6> IN 15 89
89 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4> IN 15 89
		93	VDD	VDD	94	
89 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2> IN 15 89
89 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0> IN 15 89
		99	VDD	VDD	100	
89 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1> IN 15 89
89 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1> IN 15 89
		105	VDD	VDD	106	
89 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1> IN 15 89
89 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L IN 15 89
		111	VDD	VDD	112	
89 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0> IN 15 89
89 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0> IN 15 89
		117	VDD	VDD	118	
89 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1> IN 15 89
89 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122	×NC
		123	VDD	VDD	124	
		125	TEST	VREFCA	126	
		127	VSS	VSS	128	
89 15 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33> BI 15 89
89 15 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36> BI 15 89
		133	VSS	VSS	134	
89 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4> IN 15 89
89 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138	
		139	VSS	DQ38	140	MEM_B_DQ<38> BI 15 89
89 15 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39> BI 15 89
89 15 BI	MEM_B_DQ<35>	143	DQ35	VSS	144	
		145	VSS	DQ44	146	MEM_B_DQ<44> BI 15 89
89 15 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45> BI 15 89
89 15 BI	MEM_B_DQ<40>	149	DQ41	VSS	150	
		151	VSS	DQS5*	152	MEM_B_DQS_N<5> BI 15 89
89 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5> BI 15 89
		155	VSS	VSS	156	
89 15 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47> BI 15 89
89 15 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46> BI 15 89
		161	VSS	VSS	162	
89 15 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48> BI 15 89
89 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54> BI 15 89
		167	VSS	VSS	168	
89 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6> IN 15 89
89 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172	
		173	VSS	DQ54	174	MEM_B_DQ<53> BI 15 89
89 15 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50> BI 15 89
89 15 BI	MEM_B_DQ<51>	177	DQ51	VSS	178	
		179	VSS	DQ60	180	MEM_B_DQ<60> BI 15 89
89 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61> BI 15 89
89 15 BI	MEM_B_DQ<57>	183	DQ57	VSS	184	
		185	VSS	DQS7*	186	MEM_B_DQS_N<7> BI 15 89
89 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7> BI 15 89
		189	VSS	VSS	190	
89 15 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58> BI 15 89
89 15 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62> BI 15 89
		195	VSS	VSS	196	
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L OUT 21 27 41
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA BI 44
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL IN 44
		203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B 8
			MTG PINS			
		205	MTG PIN	MTG PIN	206	
		207	MTG PIN	MTG PIN	208	
		209	MTG PIN	MTG PIN	210	
		211	MTG PIN	MTG PIN	212	

516s0706

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF

8 =PPSPD_S0_MEM_B

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3 CRITICAL

KEY

		1	VREFDQ	VSS	2	
		3	VSS	DQ4	4	MEM_B_DQ<4> BI 15 89
89 15 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5> BI 15 89
89 15 BI	MEM_B_DQ<1>	7	DQ1	VSS	8	
		9	VSS	DQS0*	10	MEM_B_DQS_N<0> BI 15 89
89 15 IN	MEM_B_DM<0>	11	DM0	DQS0	12	MEM_B_DQS_P<0> BI 15 89
		13	VSS	VSS	14	
89 15 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6> BI 15 89
89 15 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7> BI 15 89
		19	VSS	VSS	20	
89 15 BI	MEM_B_DQ<28>	21	DQ8	DQ12	22	MEM_B_DQ<29> BI 15 89
89 15 BI	MEM_B_DQ<24>	23	DQ9	DQ13	24	MEM_B_DQ<25> BI 15 89
		25	VSS	VSS	26	
89 15 BI	MEM_B_DQS_N<3>	27	DQS1*	DM1	28	MEM_B_DM<3> IN 15 89
89 15 BI	MEM_B_DQS_P<3>	29	DQS1	RESET*	30	MEM_RESET_L IN 27 29
		31	VSS	VSS	32	
89 15 BI	MEM_B_DQ<31>	33	DQ10	DQ14	34	MEM_B_DQ<26> BI 15 89
89 15 BI	MEM_B_DQ<30>	35	DQ11	DQ15	36	MEM_B_DQ<27> BI 15 89
		37	VSS	VSS	38	
89 15 BI	MEM_B_DQ<9>	39	DQ16	DQ20	40	MEM_B_DQ<13> BI 15 89
89 15 BI	MEM_B_DQ<8>	41	DQ17	DQ21	42	MEM_B_DQ<12> BI 15 89
		43	VSS	VSS	44	
89 15 BI	MEM_B_DQS_N<1>	45	DQS2*	DM2	46	MEM_B_DM<1> IN 15 89
89 15 BI	MEM_B_DQS_P<1>	47	DQS2	VSS	48	
		49	VSS	DQ22	50	MEM_B_DQ<14> BI 15 89
89 15 BI	MEM_B_DQ<15>	51	DQ18	DQ23	52	MEM_B_DQ<11> BI 15 89
89 15 BI	MEM_B_DQ<10>	53	DQ19	VSS	54	
		55	VSS	DQ28	56	MEM_B_DQ<20> BI 15 89
89 15 BI	MEM_B_DQ<21>	57	DQ24	DQ29	58	MEM_B_DQ<16> BI 15 89
89 15 BI	MEM_B_DQ<17>	59	DQ25	VSS	60	
		61	VSS	DQS3*	62	MEM_B_DQS_N<2> BI 15 89
89 15 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2> BI 15 89
		65	VSS	VSS	66	
89 15 BI	MEM_B_DQ<18>	67	DQ26	DQ30	68	MEM_B_DQ<19> BI 15 89
89 15 BI	MEM_B_DQ<22>	69	DQ27	DQ31	70	MEM_B_DQ<23> BI 15 89
		71	VSS	VSS	72	

516s0706

26 PP0V75_S3_MEM_VREFCA_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

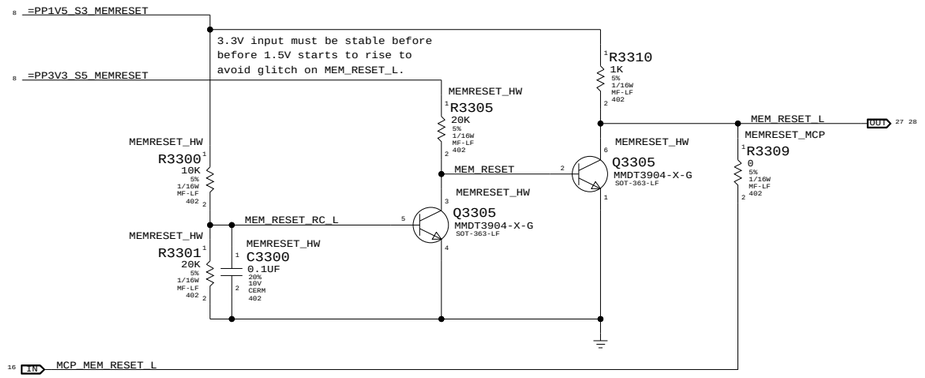
SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	32	123

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support			
SYNC_MASTER=M98_MLB		SYNC_DATE=04/01/2008	
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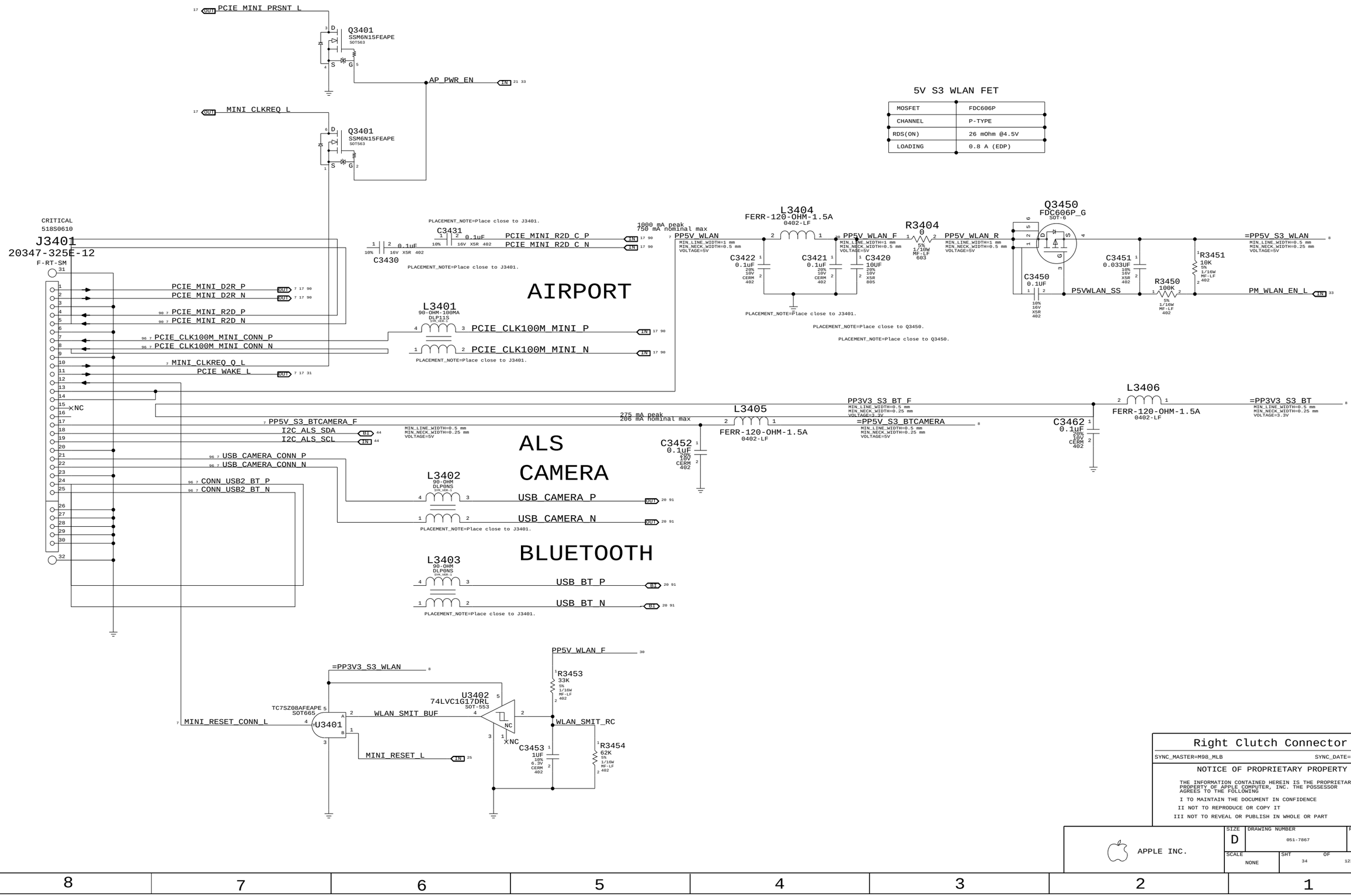
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7867	REV: 01
	SCALE: NONE	SHT: 33 OF 123	


PCIE_MINI_PRSNT_L
Q3401
SSM6N15FEAPE
SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401
SSM6N15FEAPE
SOT563
5V S3 WLAN FET
MOSFET
FDC606P
CHANNEL
P-TYPE
RDS(ON)
26 mOhm @4.5V
LOADING
0.8 A (EDP)
CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM
PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
NC
PP5V_S3_BTCAMERA_F
I2C_ALS_SDA
I2C_ALS_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N
PLACEMENT_NOTE=Place close to J3401.
C3431
0.1uF
10% 16V X5R 402
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N
C3430
0.1uF
10% 16V X5R 402
PLACEMENT_NOTE=Place close to J3401.
1000 mA peak
750 mA nominal max
PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
L3404
FERR-120-OHM-1.5A
0402-LF
PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
C3422
0.1uF
20% 10V CERM 402
C3421
0.1uF
20% 10V CERM 402
C3420
10UF
20% 10V X5R 805
PLACEMENT_NOTE=Place close to J3401.
R3404
0
5% 1/10W MF-LF 603
PP5V_WLAN_R
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
PLACEMENT_NOTE=Place close to Q3450.
Q3450
FDC606P_G
SOT-6
C3450
0.1UF
10% 16V X5R 402
P5VWLAN_SS
C3451
0.033UF
10% 16V X5R 402
R3450
100K
5% 1/16W MF-LF 402
R3451
10K
5% 1/16W MF-LF 402
=PP5V_S3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
PM_WLAN_EN_L
PLACEMENT_NOTE=Place close to Q3450.
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
PLACEMENT_NOTE=Place close to J3401.
AIRPORT
L3405
FERR-120-OHM-1.5A
0402-LF
275 mA peak
206 mA nominal max
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C3452
0.1uF
20% 16V CERM 402
L3406
FERR-120-OHM-1.5A
0402-LF
=PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
C3462
0.1uF
20% 16V CERM 402
ALS
CAMERA
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3401.
BLUETOOTH
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.
PP5V_WLAN_F
=PP3V3_S3_WLAN
R3453
33K
5% 1/16W MF-LF 402
U3402
74LVC1G17DRL
SOT-553
TC7SZ08AFEAPE
SOT665
U3401
WLAN_SMIT_BUF
WLAN_SMIT_RC
MINI_RESET_CONN_L
MINI_RESET_L
NC
C3453
1UF
10% 6.3V CERM 402
R3454
62K
5% 1/16W MF-LF 402
Right Clutch Connector
SYNC_MASTER=M98_MLB
SYNC_DATE=05/01/2008
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APPLE INC.
SIZE D
DRAWING NUMBER 051-7867
REV. 01
SCALE NONE
SHT 34 OF 123

EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

31 8 =PP3V3_S3_EXCARD
- C3530 0.1uF 20% 10V CERM 402
- C3531 10uF 20% 6.3V X5R 603

31 8 =PP1V5_S0_EXCARD
- C3534 0.1uF 20% 10V CERM 402
- C3535 10uF 20% 6.3V X5R 603

L3502
90-OHM DLP0NS SYM_VER-1
- 91 20 BI USB_EXCARD_N — 4 — 3 — USB2_EXCARD_CONN_N 7 31 96
- 91 20 BI USB_EXCARD_P — 1 — 2 — USB2_EXCARD_CONN_P 7 31 96

PLACEMENT_NOTE=Place close to J3500

L3503
90-OHM-100MA DLP11S SYM_VER-1
- 90 17 IN PCIE_CLK100M_EXCARD_N — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N 7 31 96
- 90 17 IN PCIE_CLK100M_EXCARD_P — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P 7 31 96

PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500

C3571
- 90 17 IN PCIE_EXCARD_R2D_C_N — 1 — 2 — 0.1uF — PCIE_EXCARD_R2D_N 7 31 90
- 90 17 IN PCIE_EXCARD_R2D_C_P — 1 — 2 — 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P 7 31 90

10% 16V X5R 402

C3570

PLACEMENT_NOTE=Place close to J3500

CRITICAL
J3500
502250-0627
P-ON7-SR

	29		
	26	27	
90 31 7 PCIE_EXCARD_R2D_N	24	25	PCIE_EXCARD_R2D_P 7 31 90
90 17 7 OUT PCIE_EXCARD_D2R_P	22	23	
	20	21	PCIE_EXCARD_D2R_N OUT 7 17 90
96 31 7 PCIE_CLK100M_EXCARD_CONN_N	18	19	PCIE_CLK100M_EXCARD_CONN_P 7 31 96
31 7 EXCARD_CLKREQ_CONN_L	16	17	EXCARD_CPPE_L 7 31
31 7 PP3V3_S0_EXCARD_SWITCH	14	15	PP3V3_S0_EXCARD_SWITCH 7 31
31 7 PP3V3_S3_EXCARD_SWITCH	12	13	PLT_RESET_SWITCH_L 7 31
31 7 PP1V5_S0_EXCARD_SWITCH	10	11	PCIE_WAKE_L OUT 7 17 30
44 BI =SMBUS_EXCARD_SDA	8	9	PP1V5_S0_EXCARD_SWITCH 7 31
	6	7	=SMBUS_EXCARD_SCL BI 44
31 7 EXCARD_CPUSB_L	4	5	NC
96 31 7 USB2_EXCARD_CONN_N	2	3	USB2_EXCARD_CONN_P 7 31 96
		1	
	28		

NC
NC

518S0647

OUTPUT DECOUPLING

CRITICAL
U3500
TPS2231 QFN

31 8 =PP3V3_S0_EXCARD	AUXIN	AUXOUT	15 — PP3V3_S3_EXCARD_SWITCH 7 31
31 8 =PP3V3_S0_EXCARD	2 VIN3P3	VOUT3P3	3 — PP3V3_S0_EXCARD_SWITCH 7 31
31 8 =PP1V5_S0_EXCARD	12 VIN1P5	VOUT1P5	11 — PP1V5_S0_EXCARD_SWITCH 7 31
41 IN SMC_EXCARD_PWR_EN	20 SHDN*	PERST*	8 — PLT_RESET_SWITCH_L 7 31
TP_EXCARD_STBY_L	1 STBY*	CPPE*	10 — EXCARD_CPPE_L 7 31
25 IN EXCARD_RESET_L	6 SYSRST*	CPUSB*	9 — EXCARD_CPUSB_L 7 31
42 28 IN EXCARD_OC_L	19 OC*		
NC	4 NC0	RCLKEN	18 EXCARD_RCLKEN 31
NC	5 NC1		
NC	13 NC2		
NC	14 NC3		
NC	16 NC4	THRML_PAD	21
		GND	7

R3500 0 MF-LF 402 5% 1/16W — EXCARD_SHDN_L_R

VOLTAGE=3.3V MIN_LINE_WIDTH=.3mm MIN_NECK_WIDTH=0.2mm
- C3500 0.1uF 20% 10V CERM 402
- C3503 10uF 20% 6.3V X5R 603

VOLTAGE=3.3V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
- C3501 0.1uF 10% 16V X5R 402
- C3504 10uF 20% 6.3V X5R 603

VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
- C3502 0.1uF 10% 16V X5R 402
- C3505 10uF 20% 6.3V X5R 603

31 7 EXCARD_CPPE_L — R3501 0 MF-LF 402 5% 1/16W — PCIE_EXCARD_PRSNT_L 17

31 8 =PP3V3_S3_EXCARD

31 7 EXCARD_CPUSB_L
31 7 EXCARD_CPPE_L

U3551 74HC1G00GWDG SC70-5 — SMC_EXCARD_CP OUT 41 42

C3550 0.1uF 20% 10V CERM 402

31 8 =PP3V3_S0_EXCARD

R3561 100K 1% 1/10W MF-LF 402

31 EXCARD_RCLKEN
EXCARD_CLKREQ_CONN

U3560 74HC1G00GWDG SC70-5 — EXCARD_CLKREQ_L OUT 17

31 7 EXCARD_CLKREQ_CONN_L

U3561 SN74LVC1G04YZPR BGA

C3560 0.1uF 20% 10V CERM 402

ExpressCard Connector

SYNC_MASTER=YLEE_K20 SYNC_DATE=08/22/2008

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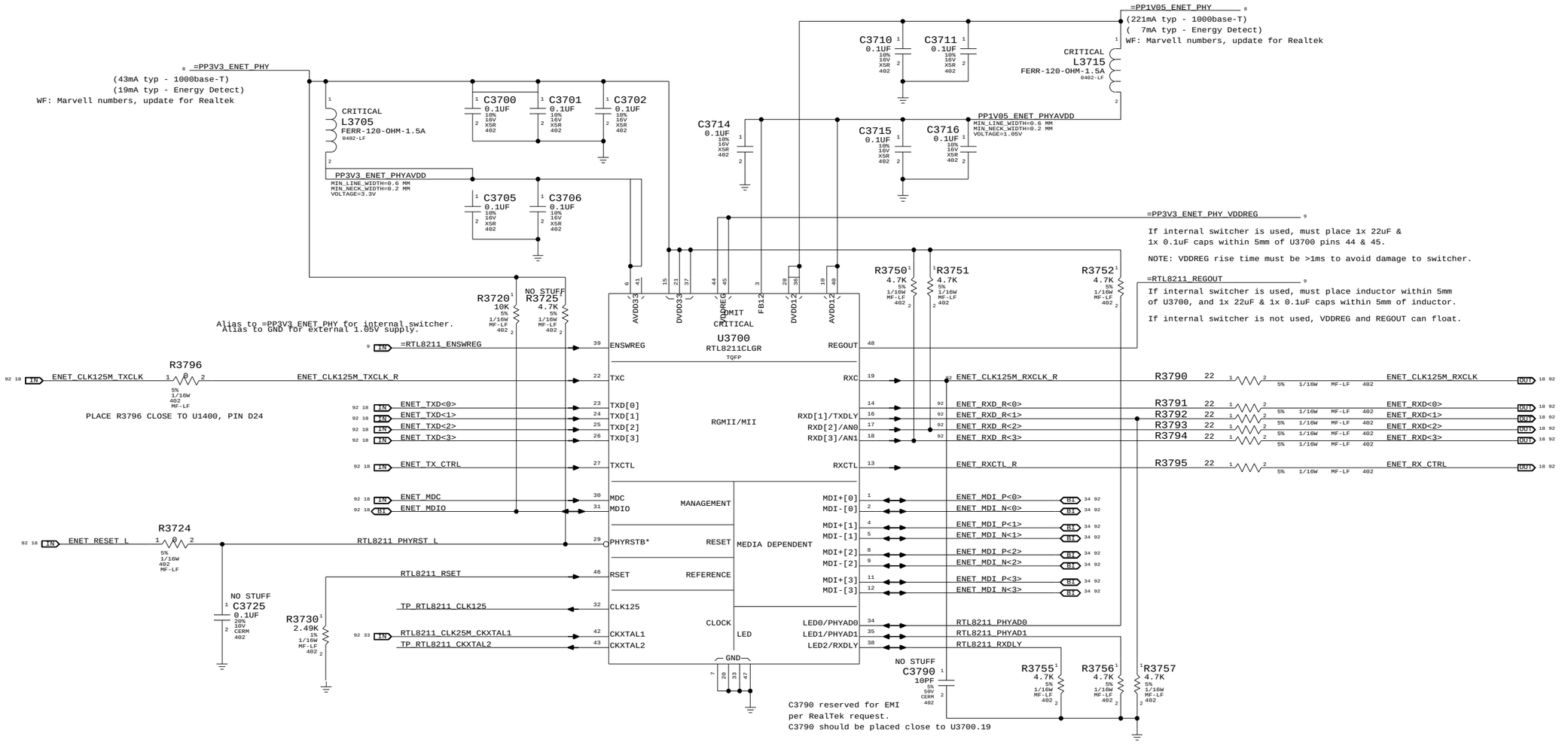
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 35 OF 123	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

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D	051-7867	01
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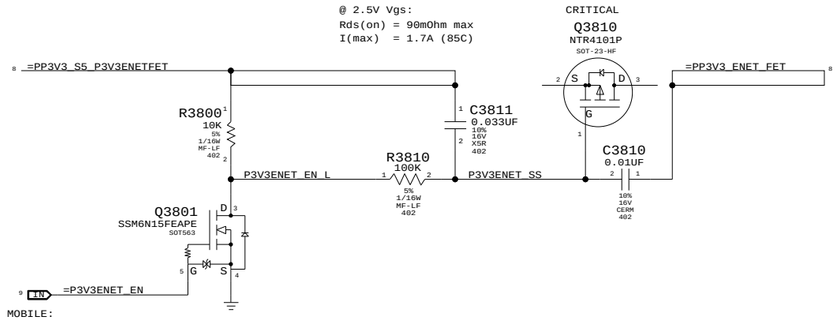
3.3V ENET FET



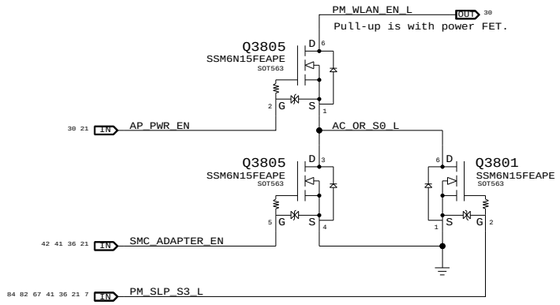
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

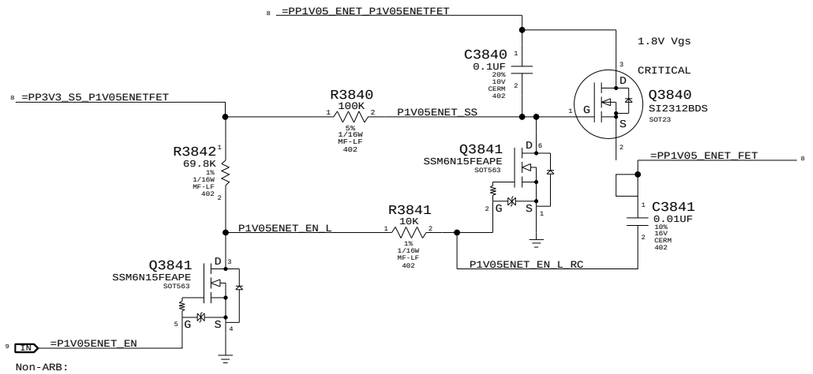
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

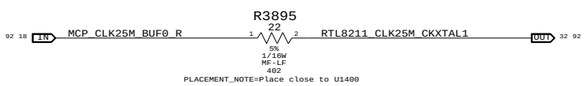


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

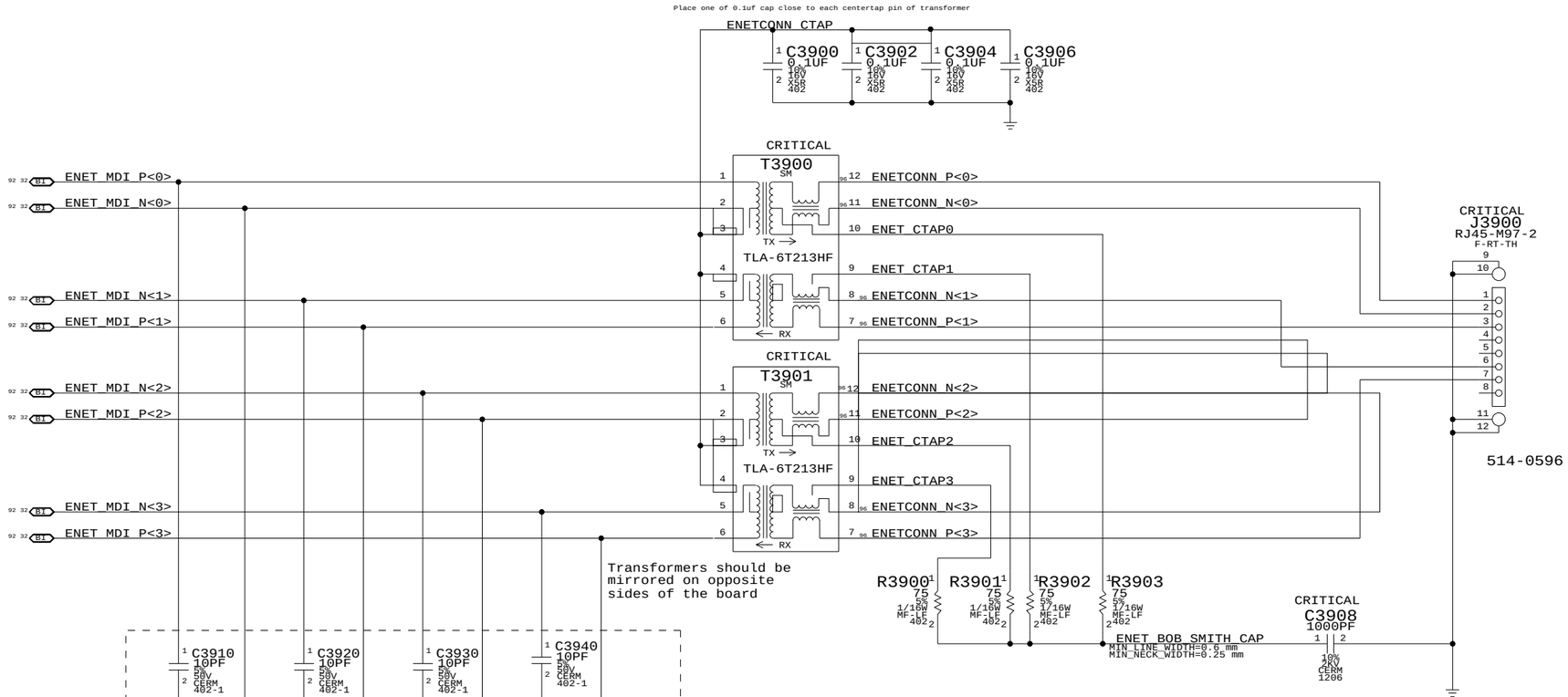
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 38 OF 123	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

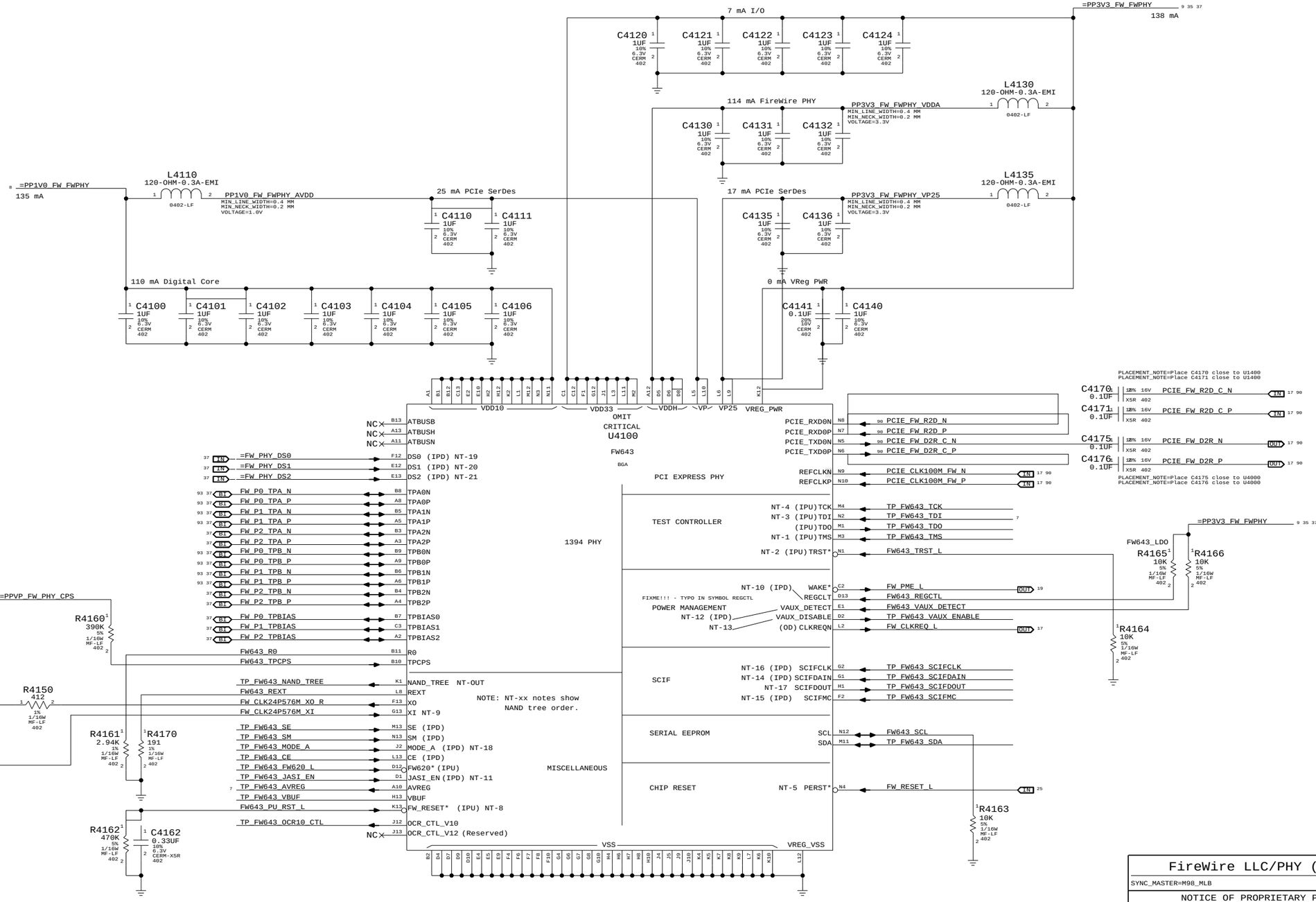


Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 39 OF 123	



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 41 OF 123	

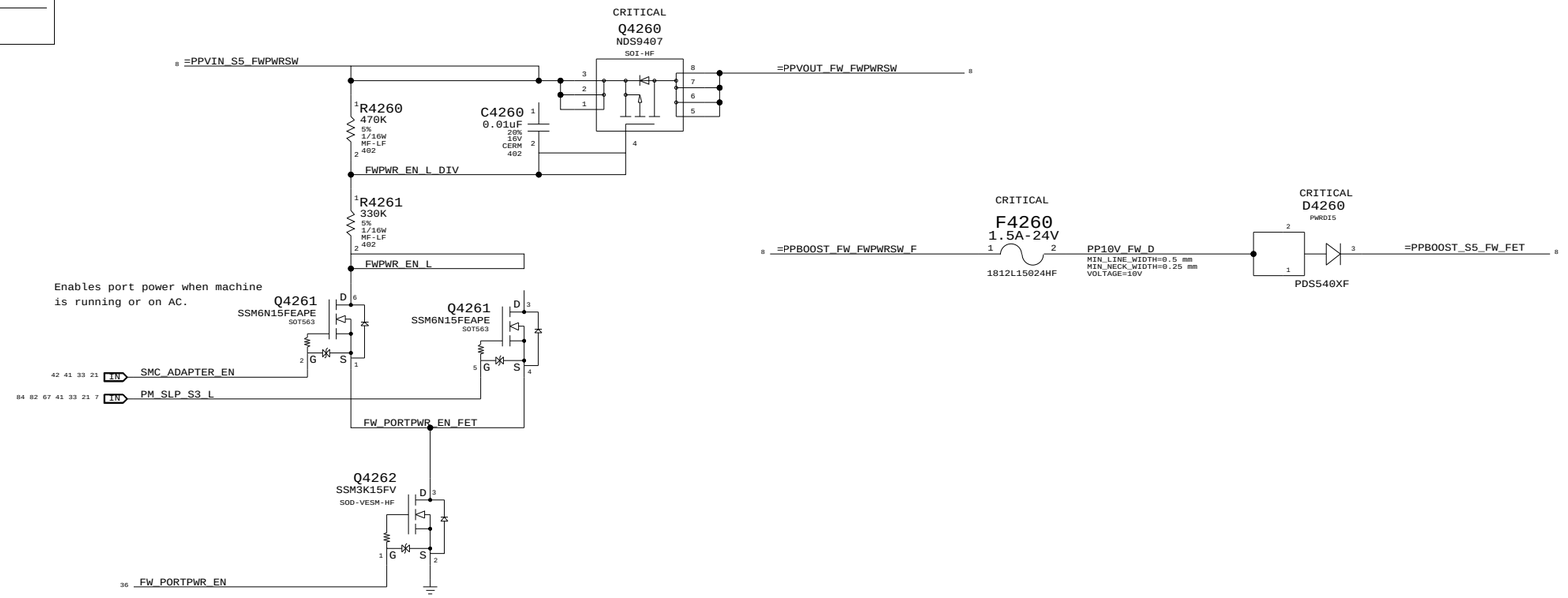
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

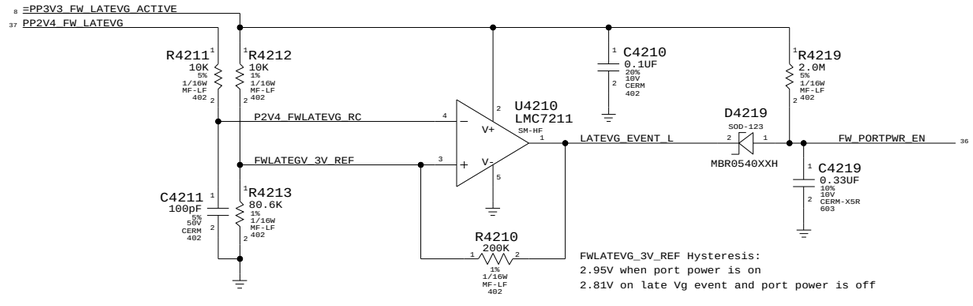
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	42	123

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

37 35 9 =PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE — =FW_PHY_DS0 35

FWPHY_DS2 MAKE_BASE=TRUE — =FW_PHY_DS2 35

FWPHY_DS1 MAKE_BASE=TRUE — =FW_PHY_DS1 35

R4381 10K 1% 1/10W MF-LF 402

35	FW_P0_TPBIAS	NC_FW0_TPBIAS	MAKE_BASE=TRUE
35	FW_P2_TPBIAS	NC_FW2_TPBIAS	MAKE_BASE=TRUE 7
93 35	FW_P0_TPA_N	NC_FW0_TPAN	MAKE_BASE=TRUE
93 35	FW_P0_TPA_P	NC_FW0_TPAP	MAKE_BASE=TRUE 7
35	FW_P2_TPA_N	NC_FW2_TPAN	MAKE_BASE=TRUE 7
35	FW_P2_TPA_P	NC_FW2_TPAP	MAKE_BASE=TRUE 7
93 35	FW_P0_TPB_N	NC_FW0_TPBN	MAKE_BASE=TRUE 7
93 35	FW_P0_TPB_P	NC_FW0_TPBP	MAKE_BASE=TRUE 7
35	FW_P2_TPB_N	NC_FW2_TPBN	MAKE_BASE=TRUE 7
35	FW_P2_TPB_P	NC_FW2_TPBP	MAKE_BASE=TRUE 7

Termination

Place close to FireWire PHY

35 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

93 35	FW_P1_TPA_P	FW_PORT1_TPA_P MAKE_BASE=TRUE 37
93 35	FW_P1_TPA_N	FW_PORT1_TPA_N MAKE_BASE=TRUE 37
93 35	FW_P1_TPB_P	FW_PORT1_TPB_P MAKE_BASE=TRUE 37
93 35	FW_P1_TPB_N	FW_PORT1_TPB_N MAKE_BASE=TRUE 37

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW (SYM-VER1)

PPVP_FW_CPS MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=10V MAKE_BASE=TRUE — =PPVP_FW_PHY_CPS 35

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

37 35 9 =PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

"Snapback" & "Late VG" Protection

37 36 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 50V X7R 402

C4310 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

37 FW_PORT1_TPB_N

37 FW_PORT1_TPB_P

37 FW_PORT1_TPA_N

37 FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

C4313 0.01uF 10% 50V X7R 402

DP4311 BAV99DW-X-G SOT-363

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Cable Power

8 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

1	TPB-	TPB(R)
9	TPB+	VP
8		
7		SC/NC
6		VG
3	TPA-	
5		
4	TPA+	TPA(R)
10		
11		CHASSIS GND
12		
13		

TPB- TPB<R> TPB+ VP NC VG TPA- TPA<R> TPA+

OUTPUT

INPUT

(FW_PORT1_BREF)

NC

(GND_FW_PORT1_VG)

FW_PORT1_AREF

514S0605

Late-VG Protection Power

8 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 36 37

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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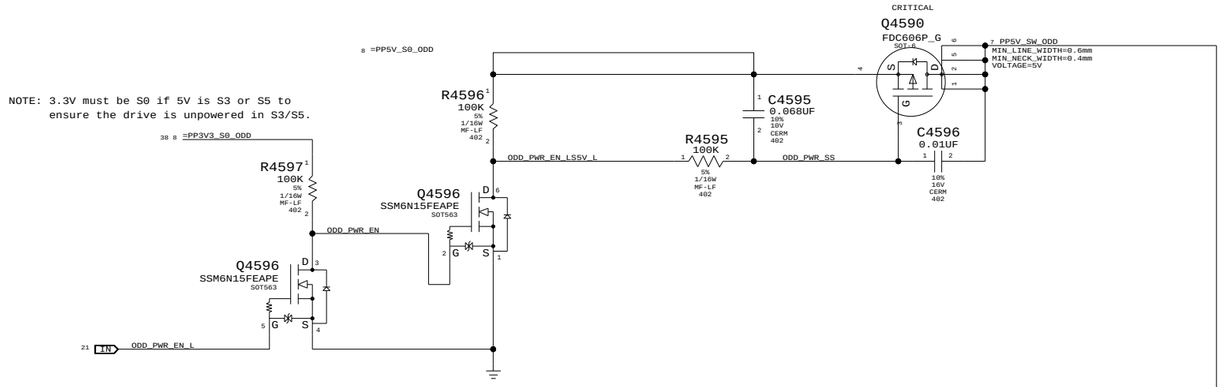
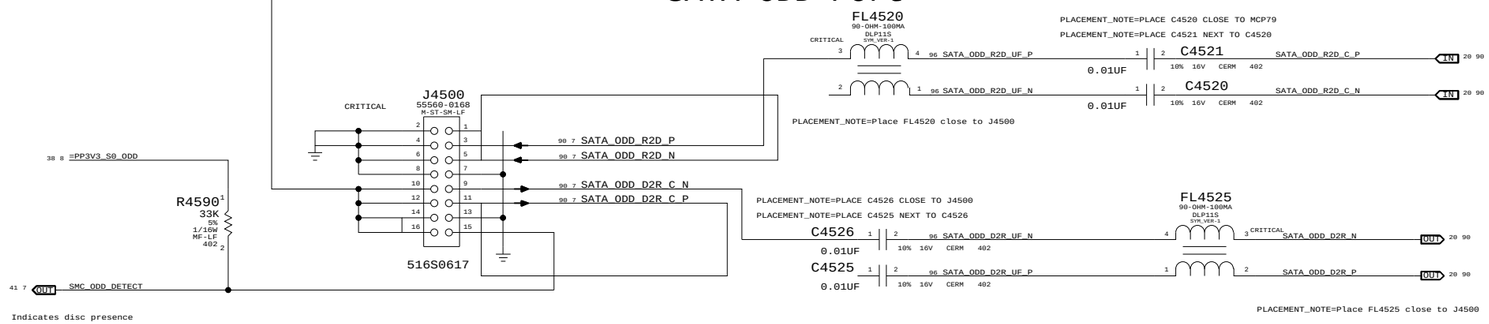
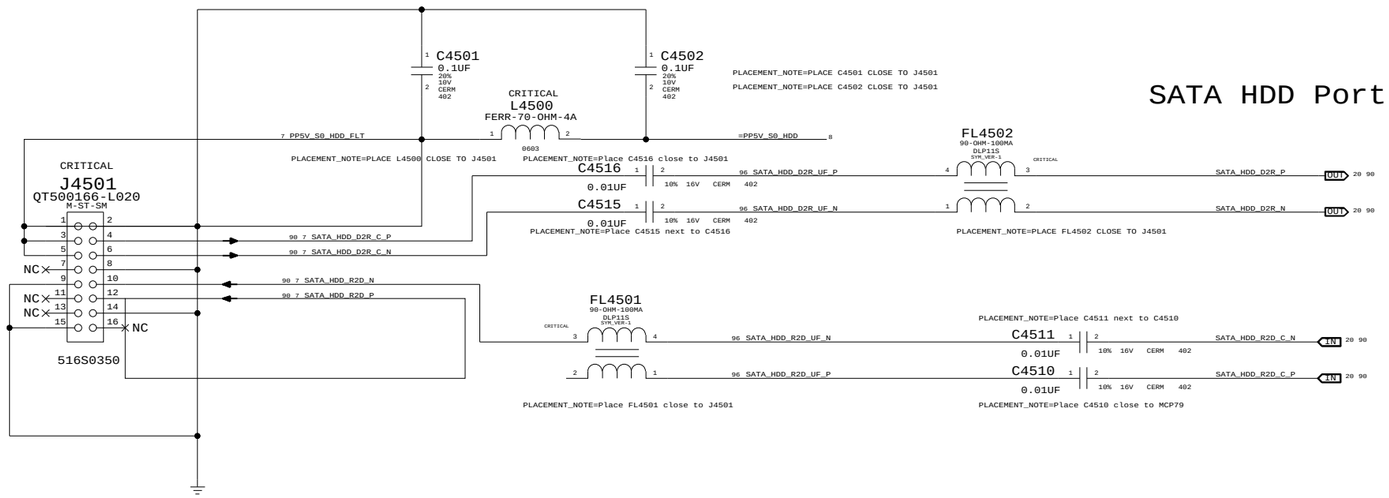
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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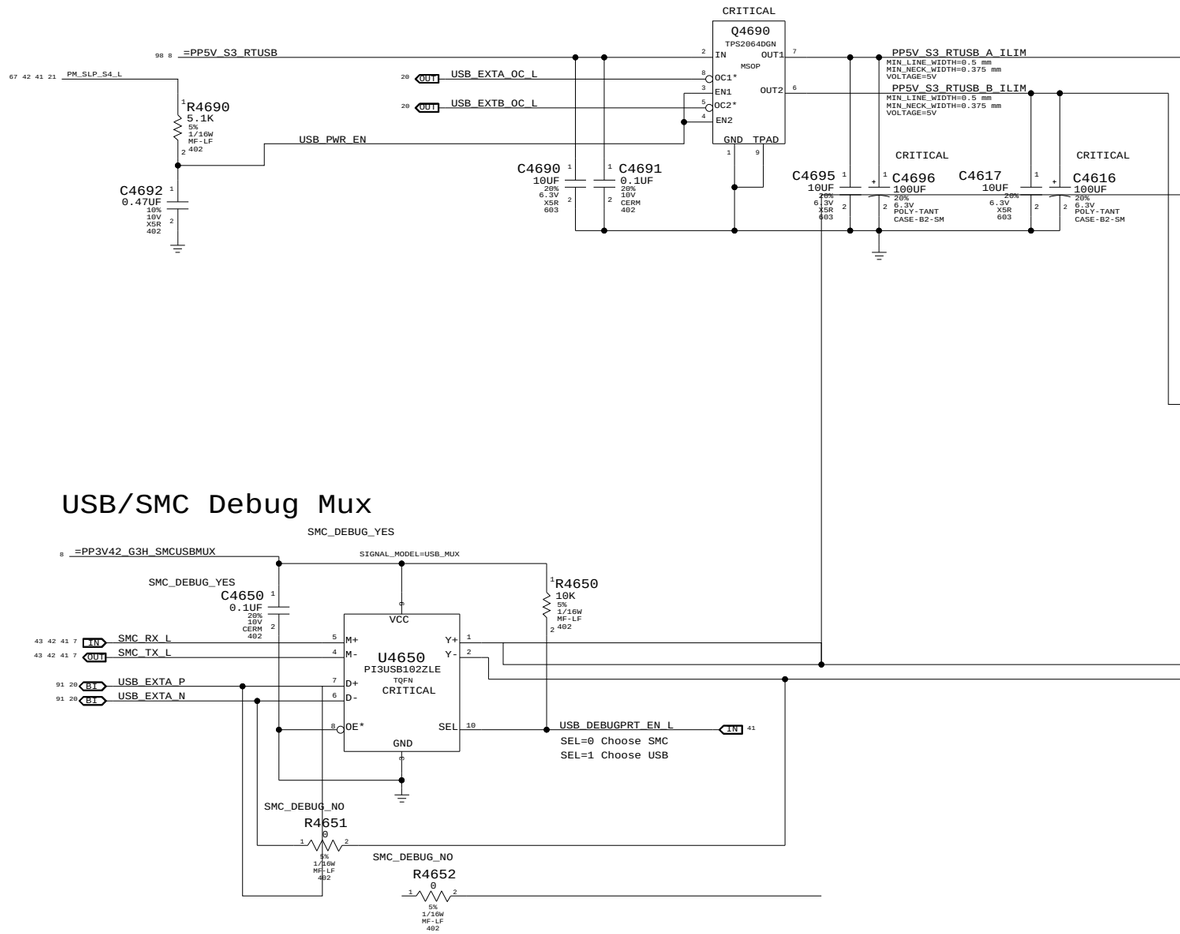
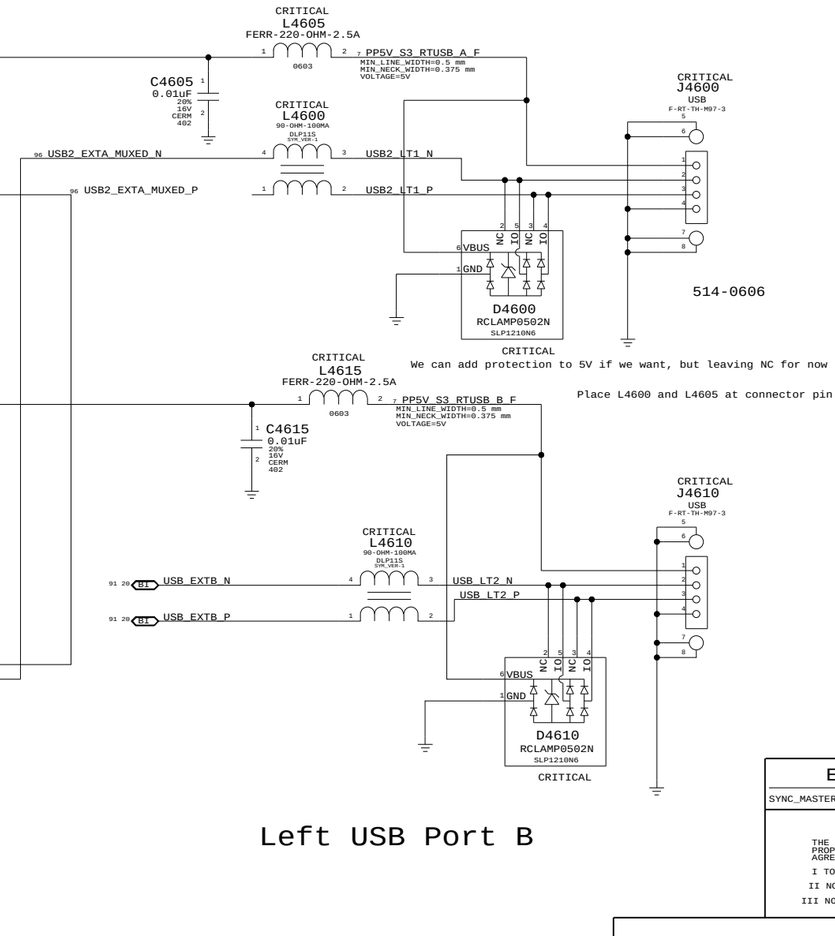
SCALE: NONE	SHT 45 OF 123	

Port Power Switch



Left USB Port A



USB/SMC Debug Mux

Left USB Port B

External USB Connectors	
SYNC_MASTER=M98_MLB	SYNC_DATE=07/14/2008

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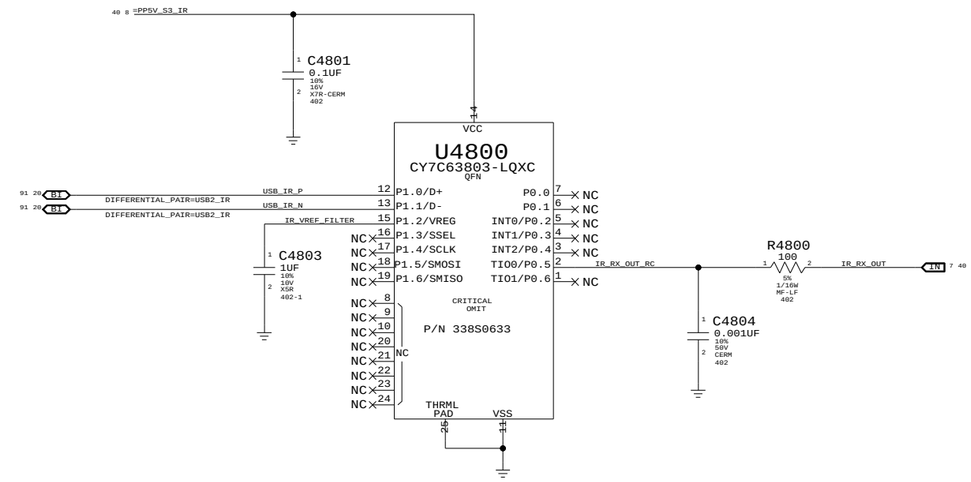

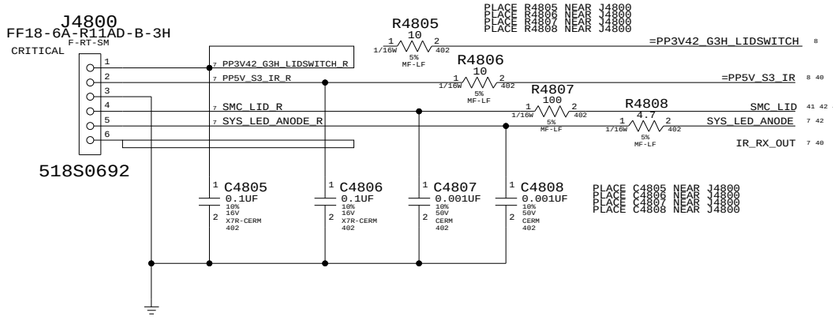

Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

APPLE INC.

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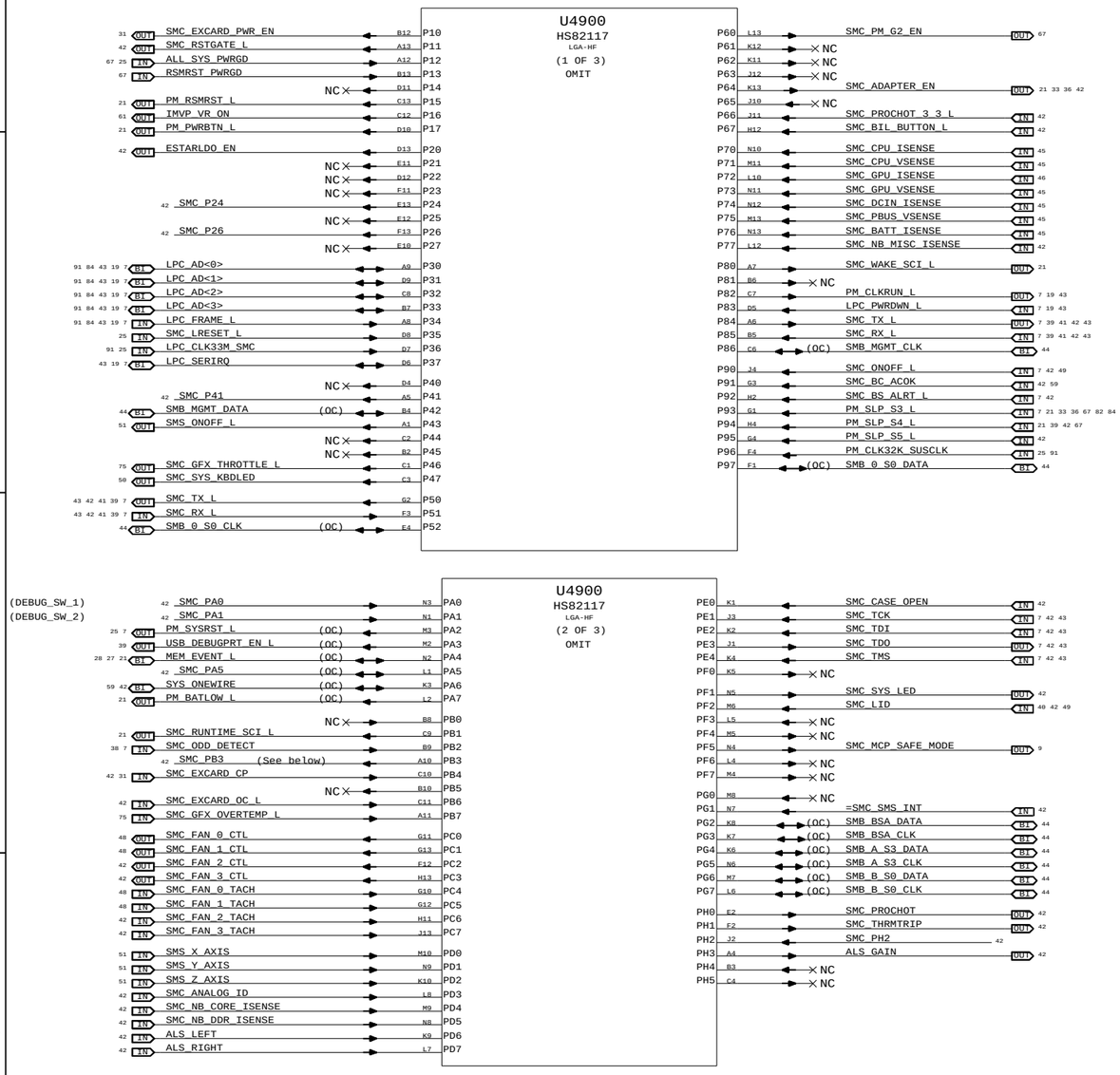
SCALE: NONE	SHT 48 OF 123	

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



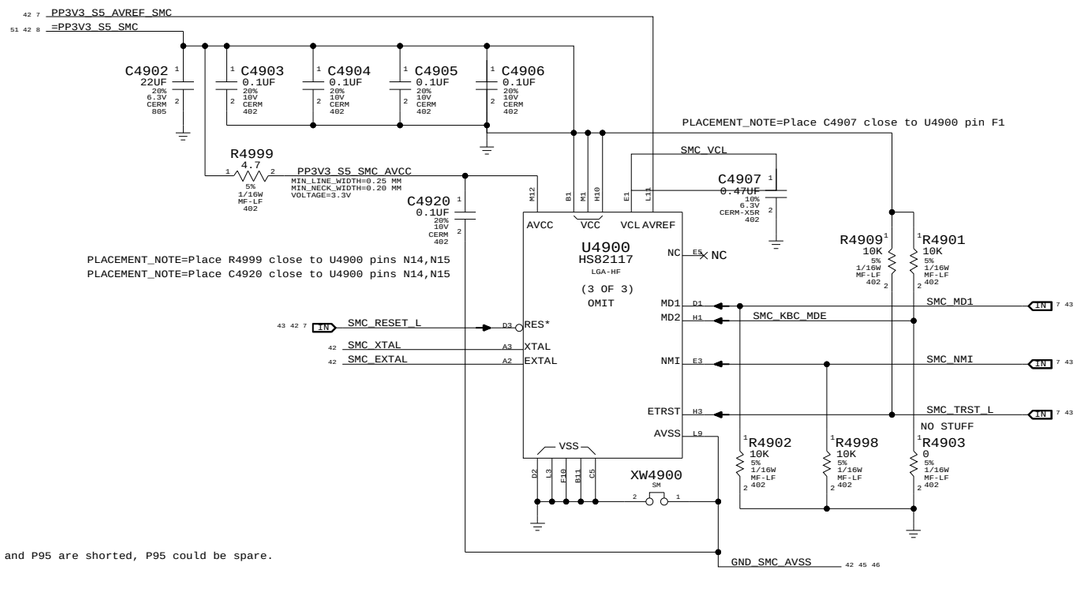
NOTE: P94 and P95 are shorted, P95 could be spare.

(DEBUG_SW_1)
(DEBUG_SW_2)

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

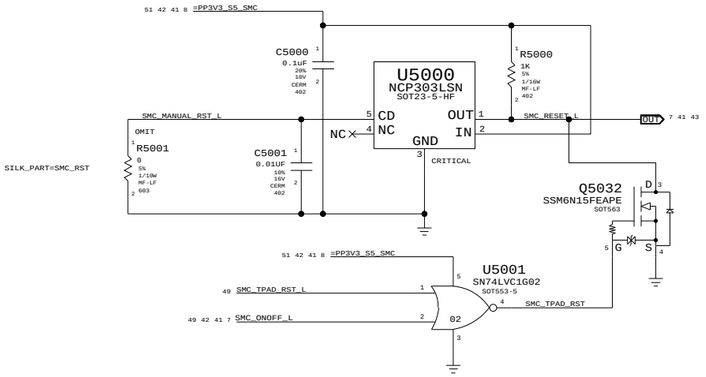
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



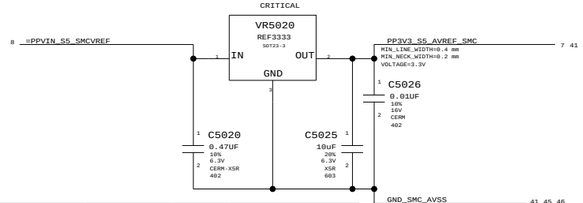
SMC		
SYNC_MASTER=T18_MLB		SYNC_DATE=06/06/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7867	01
	SCALE: NONE	SHT 49 OF 123	

SMC Reset "Button" / Brownout Detect

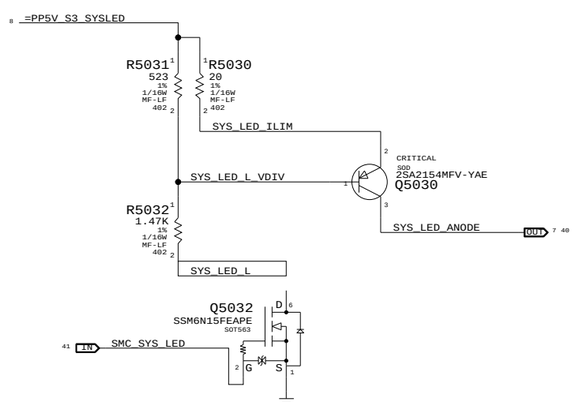


SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35351381	35351278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit



41 SMC_FAN_2_CTL — NC_SMC_FAN_2_CTL 7 (MAKE_BASE=TRUE)
41 SMC_FAN_2_TACH — NC_SMC_FAN_2_TACH 7 (MAKE_BASE=TRUE)
41 SMC_FAN_3_CTL — NC_SMC_FAN_3_CTL 7 (MAKE_BASE=TRUE)
41 SMC_FAN_3_TACH — NC_SMC_FAN_3_TACH 7 (MAKE_BASE=TRUE)

41 ESTARLDO_EN — NC_ESTARLDO_EN 7 (MAKE_BASE=TRUE)

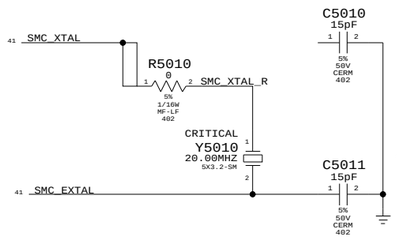
59 42 41 SMC_BC_ACOK (MAKE_BASE=TRUE) — =CHGR_ACOK 60
41 ALS_LEFT — SMC_MCP_VSENSE 45 (MAKE_BASE=TRUE)
41 ALS_RIGHT — SMC_CPU_HI_ISENSE 45 (MAKE_BASE=TRUE)
41 SMC_NB_CORE_ISENSE — SMC_MCP_CORE_ISENSE 46 (MAKE_BASE=TRUE)
41 SMC_NB_DDR_ISENSE — SMC_MCP_DDR_ISENSE 46 (MAKE_BASE=TRUE)
41 SMC_NB_MISC_ISENSE — SMC_CPU_FSB_ISENSE 46 (MAKE_BASE=TRUE)
41 SMC_ANALOG_ID — SMC_GPU_1V8_ISENSE 46 (MAKE_BASE=TRUE)

41 SMC_P24 — TP_SMC_P24 (MAKE_BASE=TRUE)
41 SMC_P26 — SMC_BMON_MUX_SEL 45 (MAKE_BASE=TRUE)
41 SMC_P41 — TP_SMC_P41 7 (MAKE_BASE=TRUE)
41 ALS_GAIN — NC_ALS_GAIN 7 (MAKE_BASE=TRUE)
41 SMC_PB3 — SMC_IG_THROTTLE_L 21 (MAKE_BASE=TRUE)
41 SMC_RSTGATE_L — TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)

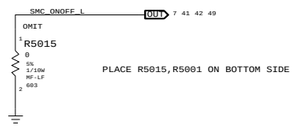
R5095 0 5% 1/16W MF-LF 402
41 OUT SMC_EXCARD_OC_L — EXCARD_OC_L IN 20 31

51 SMS_INT_L (MAKE_BASE=TRUE) — =SMC_SMS_INT 41

SMC Crystal Circuit

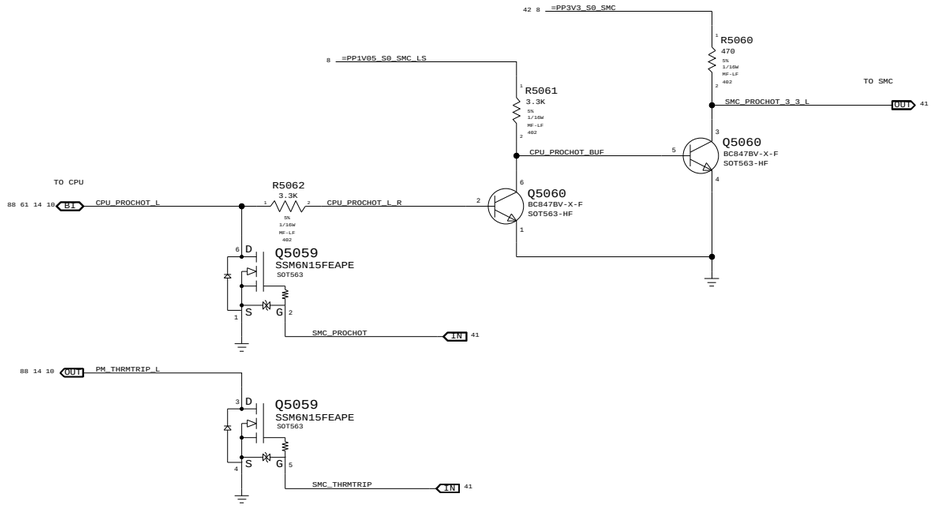


Debug Power "Button"

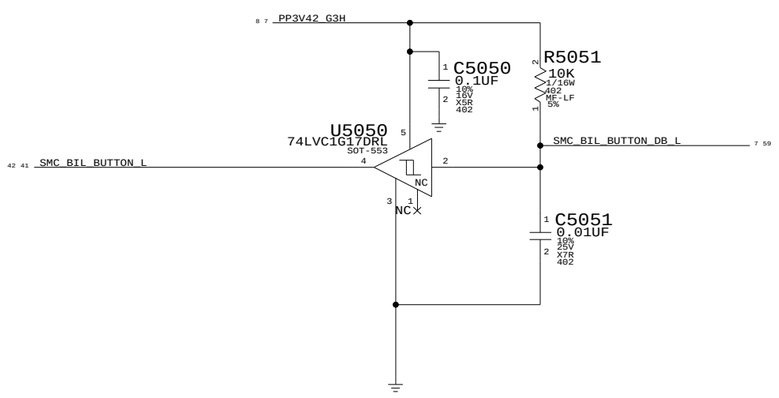


PLACE R5015,R5001 ON BOTTOM SIDE

SMC FSB to 3.3V Level Shifting



PP3V42_G3H



PP3V3_S5_SMC

41 SMC_PA0	R5091	100K	5%	1/16W	MF-LF	402	
41 SMC_PA1	R5092	100K	5%	1/16W	MF-LF	402	
49 42 41 7 SMC_ONOFF_L	R5070	10K	5%	1/16W	MF-LF	402	
49 41 40 SMC_LID	R5071	100K	5%	1/16W	MF-LF	402	
41 SMC_PH2	R5072	10K	5%	1/16W	MF-LF	402	
43 41 39 7 SMC_TX_L	R5073	10K	5%	1/16W	MF-LF	402	
43 41 39 7 SMC_RX_L	R5074	100K	5%	1/16W	MF-LF	402	
ONEWIRE_PU							
59 41 SYS_ONEWIRE	R5075	2.0K	5%	1/16W	MF-LF	402	
59 41 7 SMC_BS_ALRT_L	R5076	100K	5%	1/16W	MF-LF	402	
43 41 7 SMC_TMS	R5077	10K	5%	1/16W	MF-LF	402	
43 41 7 SMC_TDO	R5078	10K	5%	1/16W	MF-LF	402	
43 41 7 SMC_TDI	R5079	10K	5%	1/16W	MF-LF	402	
43 41 7 SMC_TCK	R5080	10K	5%	1/16W	MF-LF	402	
42 41 SMC_BIL_BUTTON_L	R5081	10K	5%	1/16W	MF-LF	402	
59 42 41 SMC_BC_ACOK	R5087	470K	5%	1/16W	MF-LF	402	

41 36 33 21 SMC_ADAPTER_EN	R5085	10K	5%	1/16W	MF-LF	402	
41 SMC_CASE_OPEN	R5086	10K	5%	1/16W	MF-LF	402	
41 31 SMC_EXCARD_CP	R5088	10K	5%	1/16W	MF-LF	402	
41 PM_SLP_S5_L	R5090	100K	5%	1/16W	MF-LF	402	
67 41 39 21 PM_SLP_S4_L							

PP3V3_S0_SMC

42 8 =PP3V3_S0_SMC
41 SMC_PA5 — R5089 10K 5% 1/16W MF-LF 402

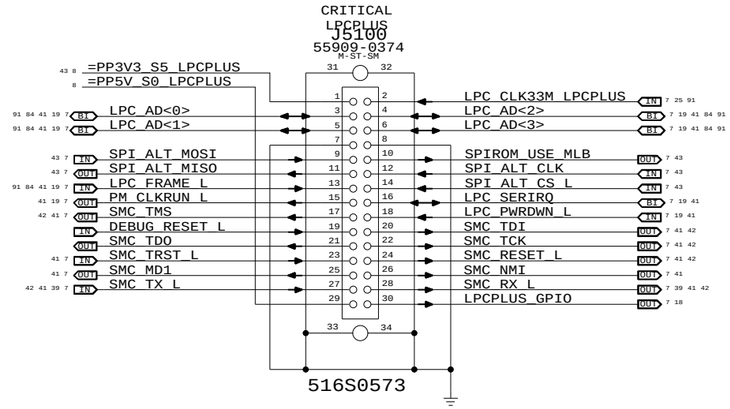
SMC Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

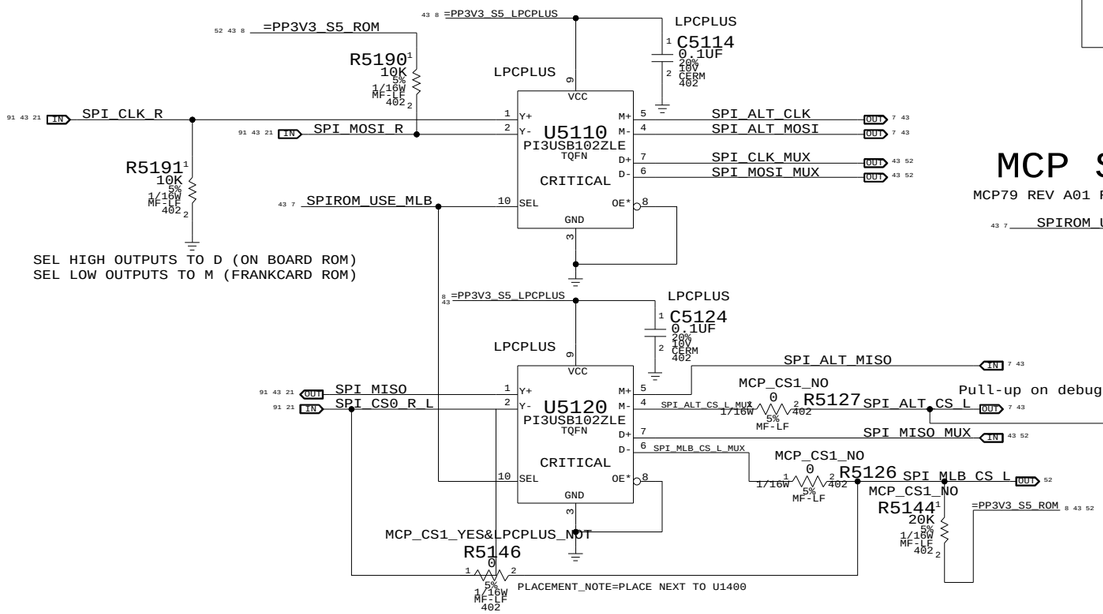
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 50 OF 123	

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

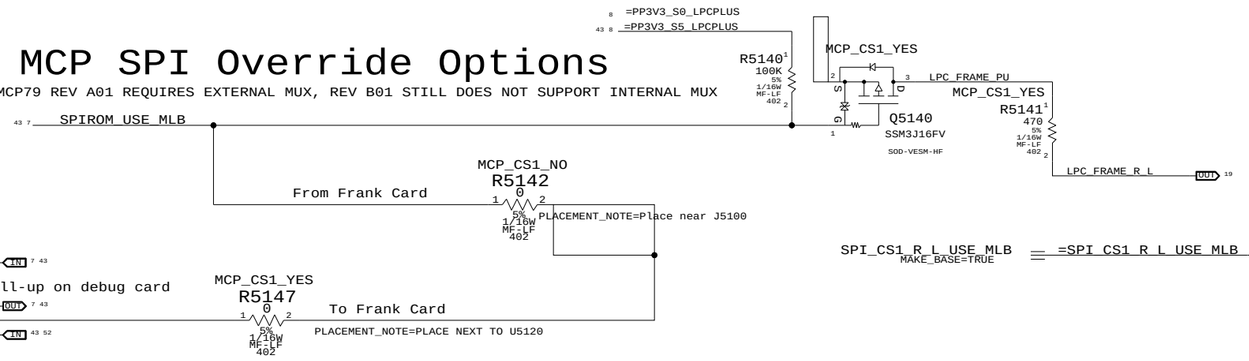


MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

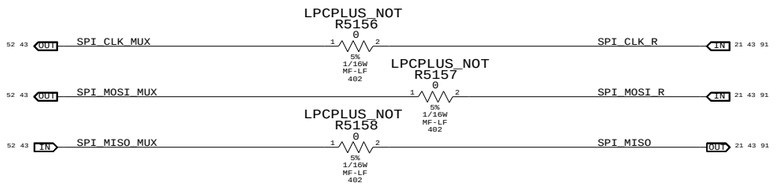
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI_CS1_R_L_USE_MLB
MAKE_BASE=TRUE
=SPI_CS1_R_L_USE_MLB

SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

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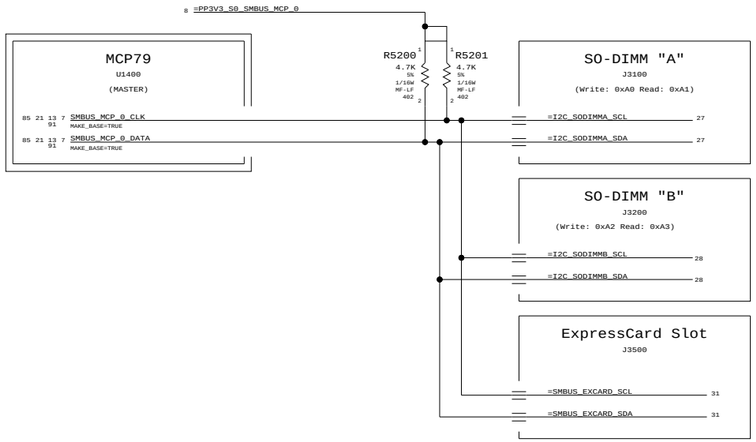
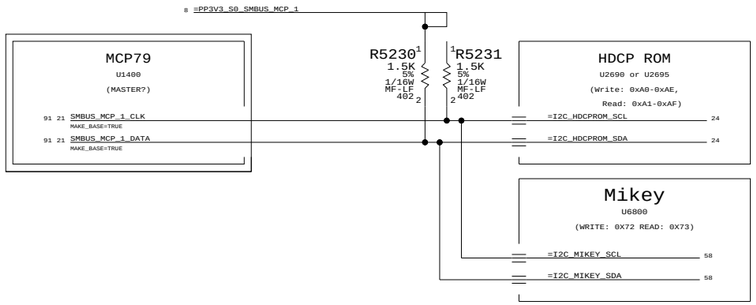
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 51 OF 123	

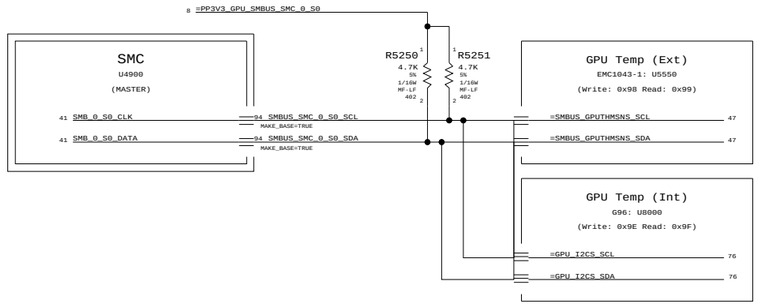
MCP79 SMBus "0" Connections



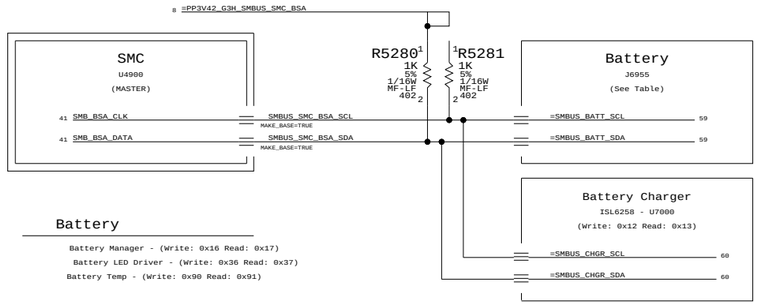
MCP79 SMBus "1" Connections



SMC "0" SMBus Connections

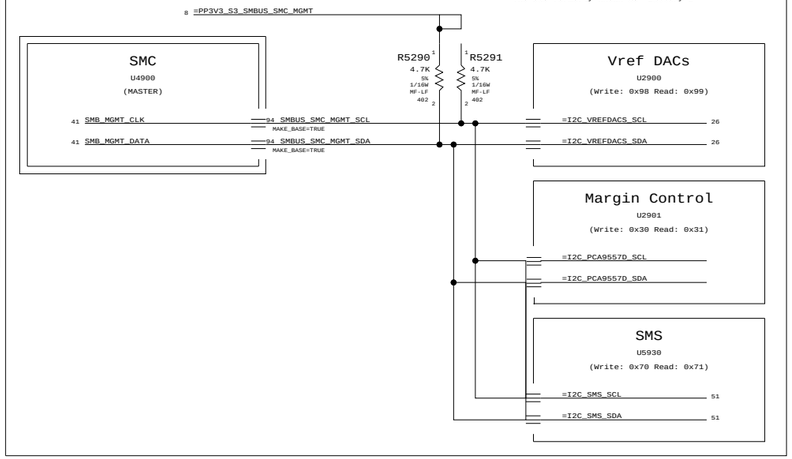


SMC "Battery A" SMBus Connections



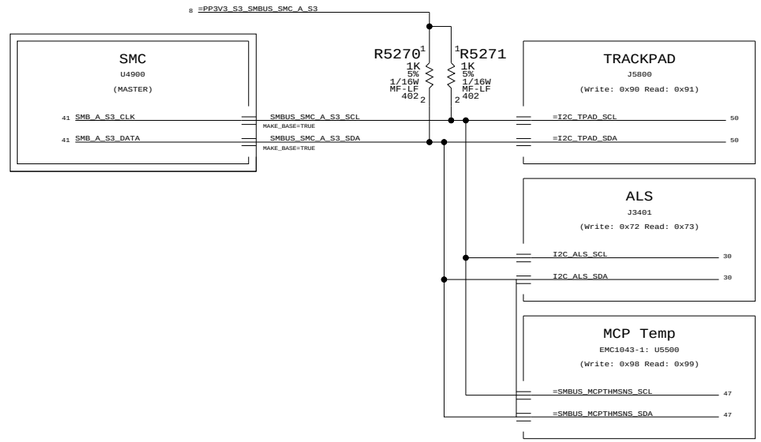
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

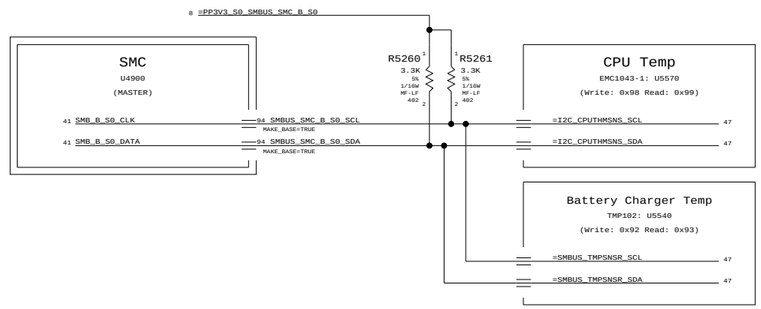


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



K20 SMBUS CONNECTIONS

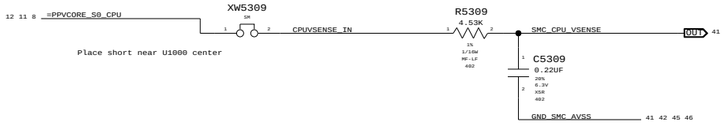
SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

APPLE INC.

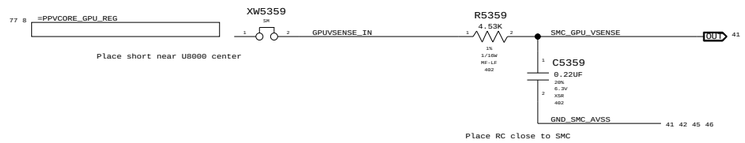
SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	52	123

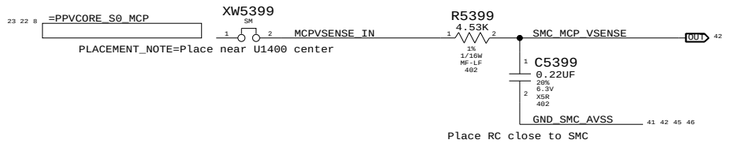
CPU Voltage Sense / Filter



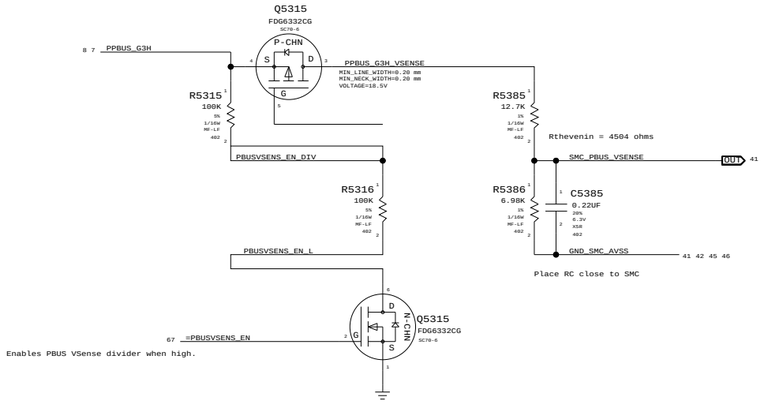
GPU Voltage Sense / Filter



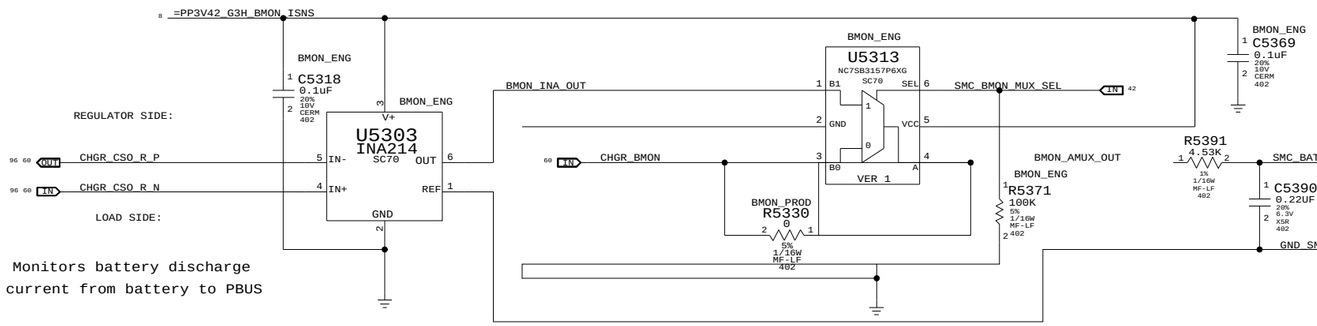
MCP Voltage Sense / Filter



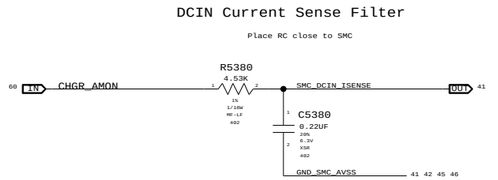
PBUS Voltage Sense & Filter



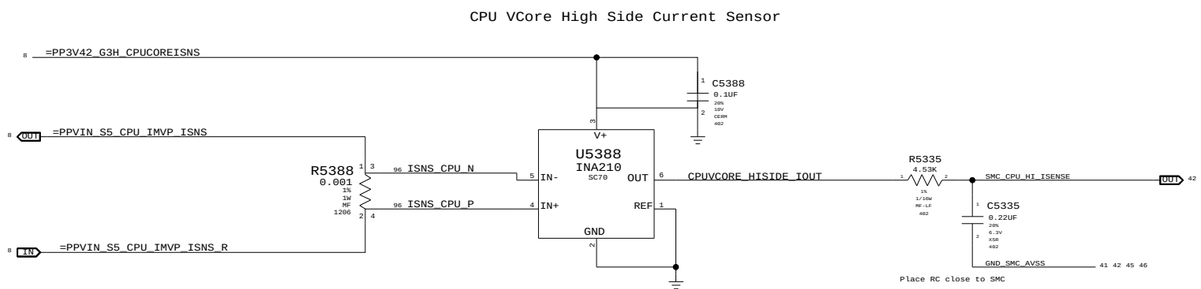
BMON Current Sense - Entire circuit must be near SMC (U4900)



DCIN Current Sense Filter

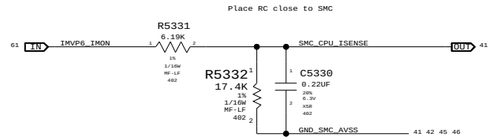


CPU VCore High Side Current Sensor



Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter



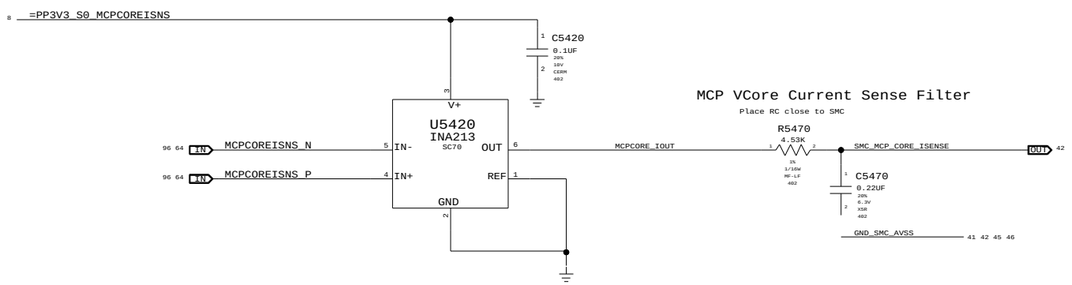
Current & Voltage Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/20/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	53	123

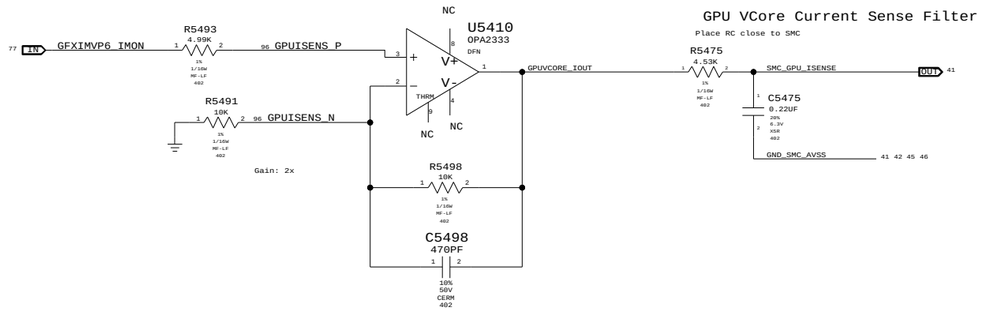
MCP VCore Current Sense



MCP VCore Current Sense Filter

Place RC close to SMC

GPU VCore Current Sense

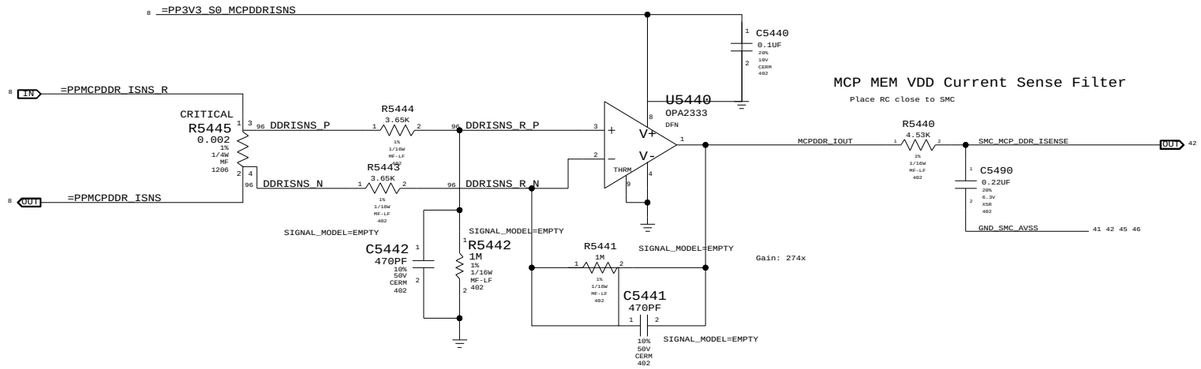


GPU VCore Current Sense Filter

Place RC close to SMC

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

MCP MEM VDD Current Sense



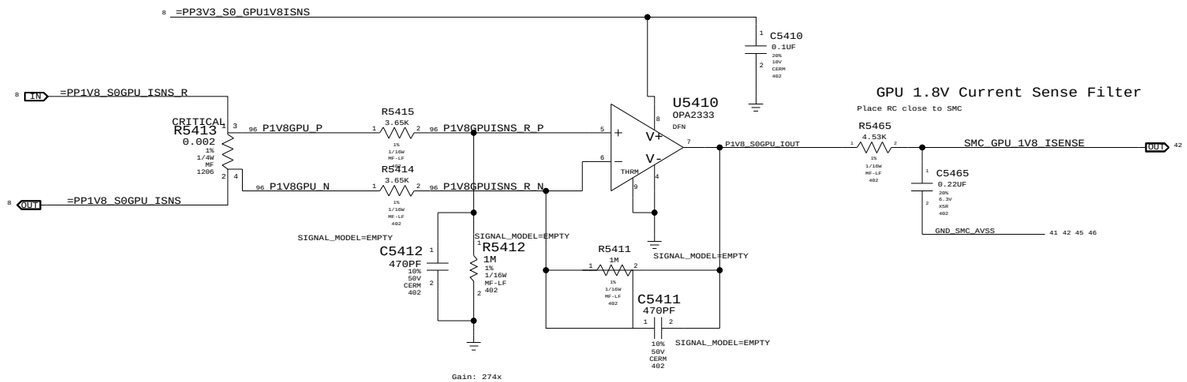
MCP MEM VDD Current Sense Filter

Place RC close to SMC

OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

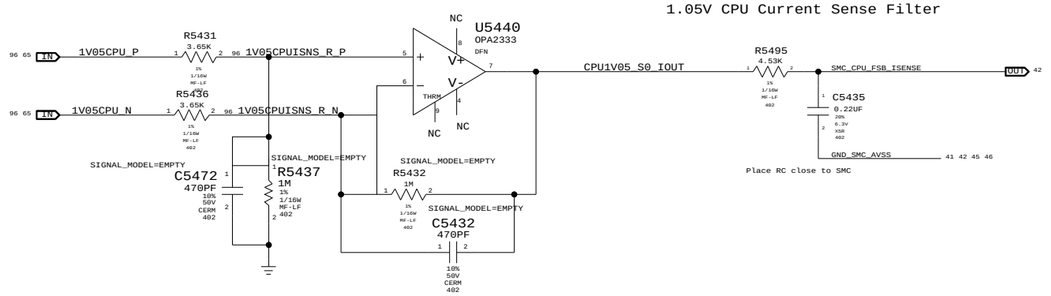
GPU 1.8V Current Sense



GPU 1.8V Current Sense Filter

Place RC close to SMC

CPU FSB 1.05V Current Sense



1.05V CPU Current Sense Filter

Place RC close to SMC

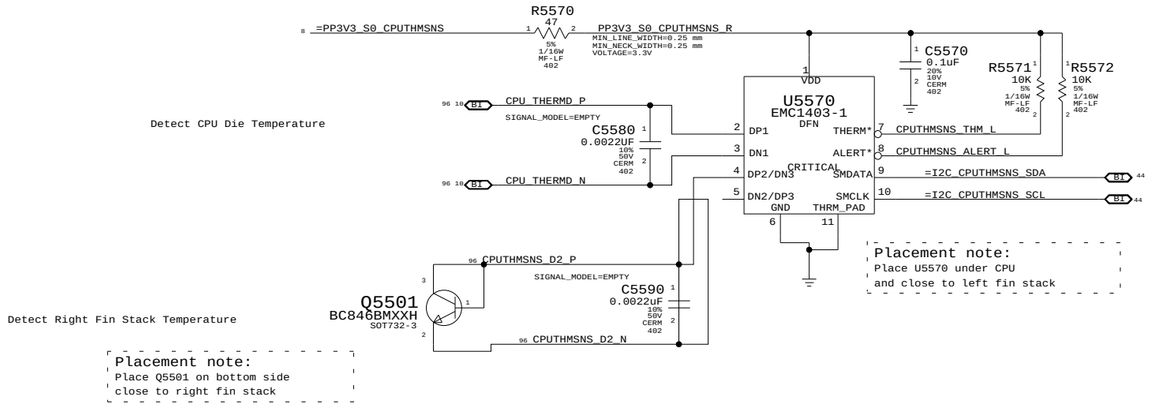
Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

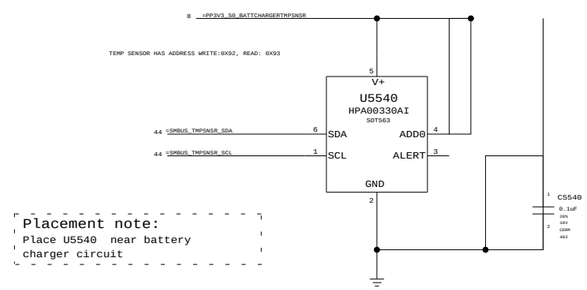
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	54	123

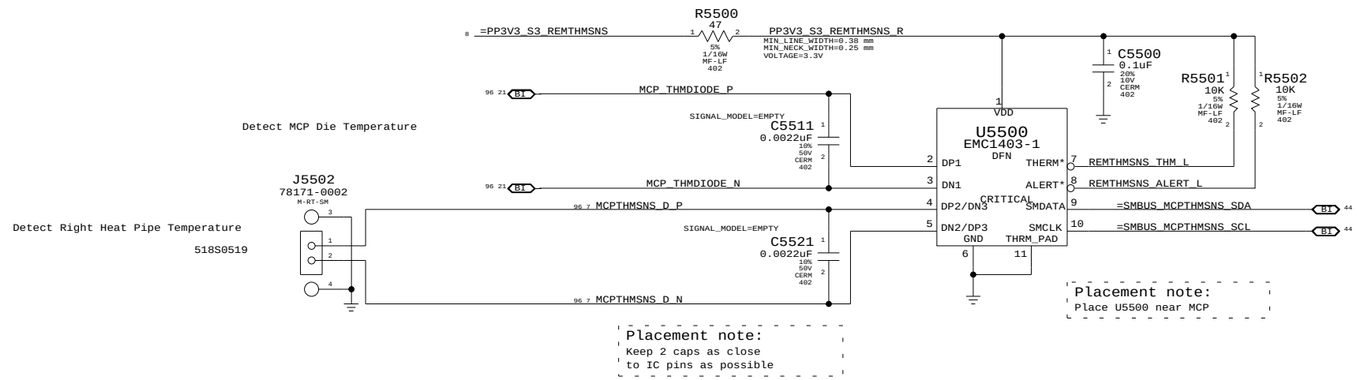
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity

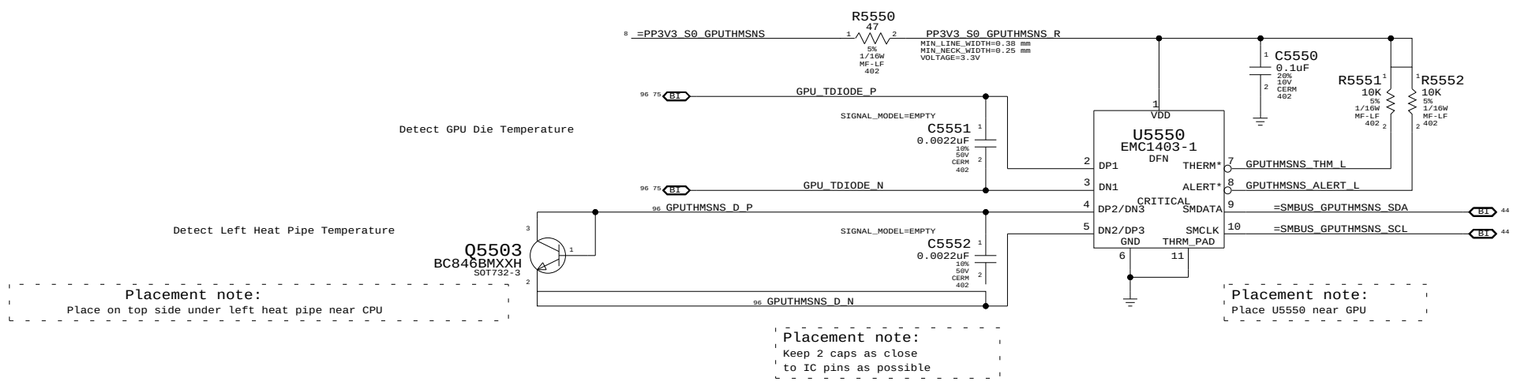


MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



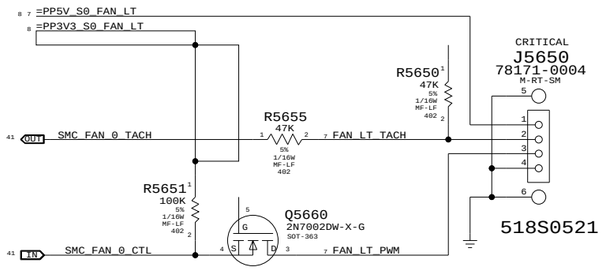
Thermal Sensors

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

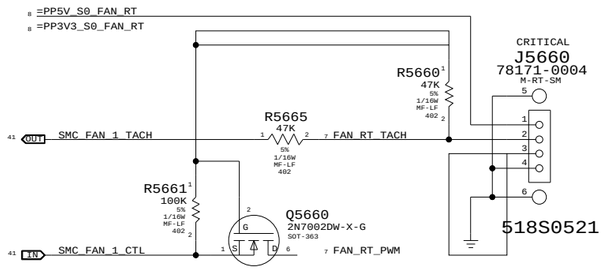
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 55 OF 123	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

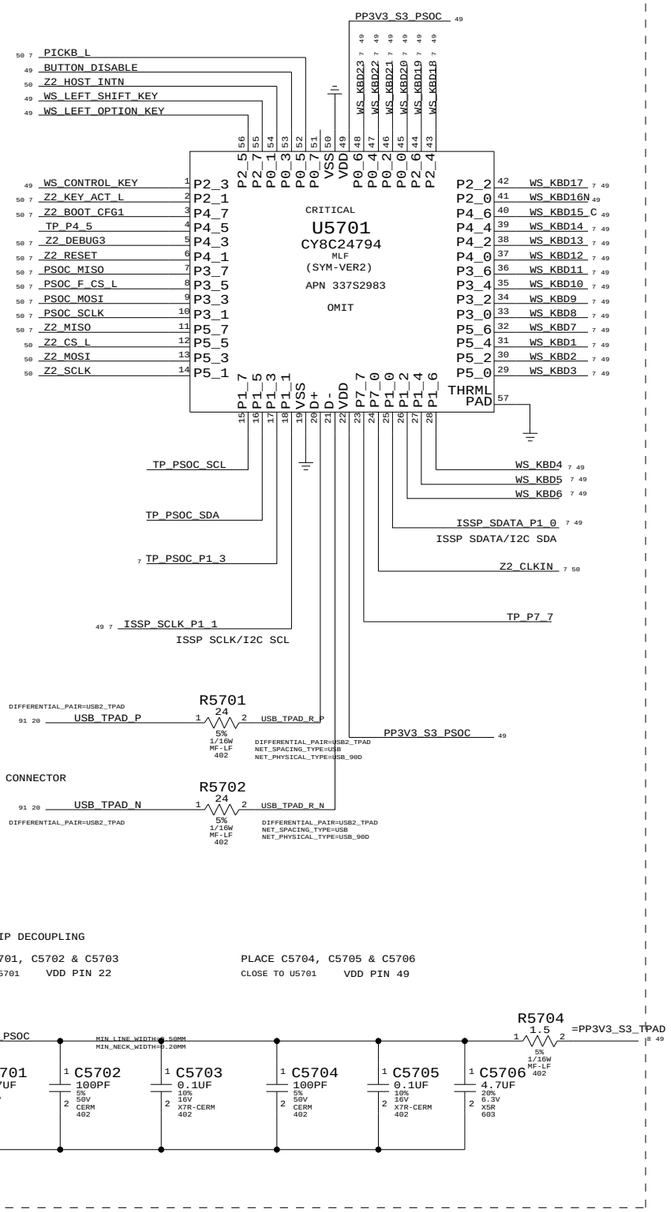
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 56 OF 123	

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

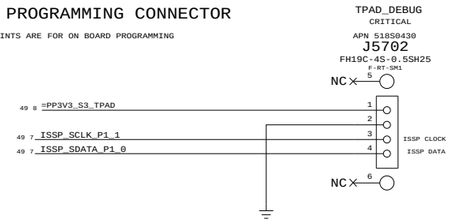
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

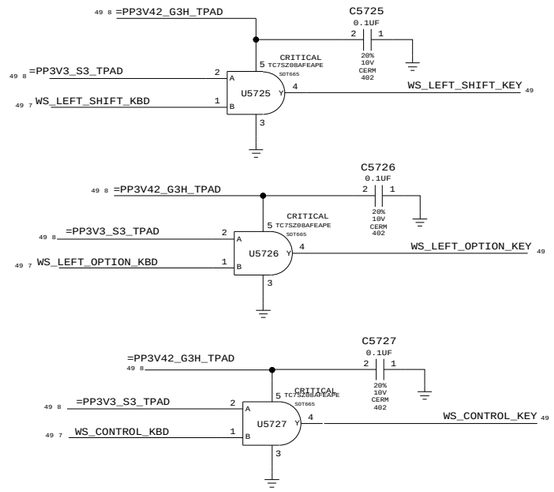
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

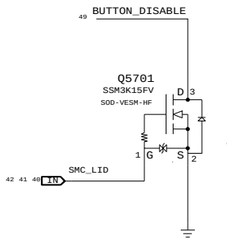
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



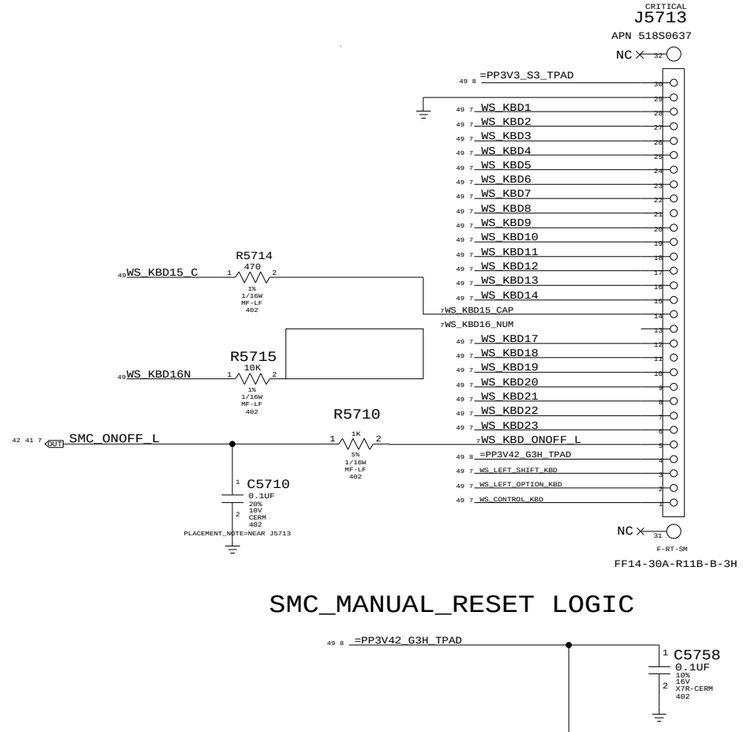
TPAD BUTTONS DISABLE



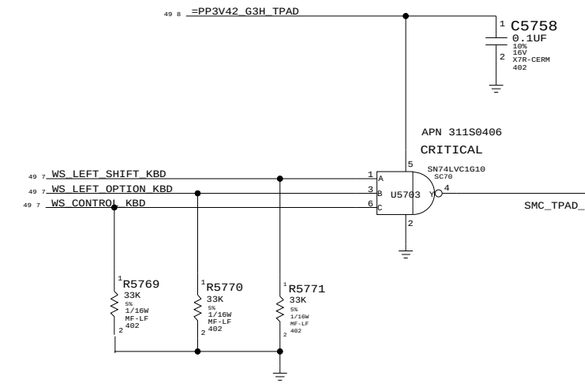
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

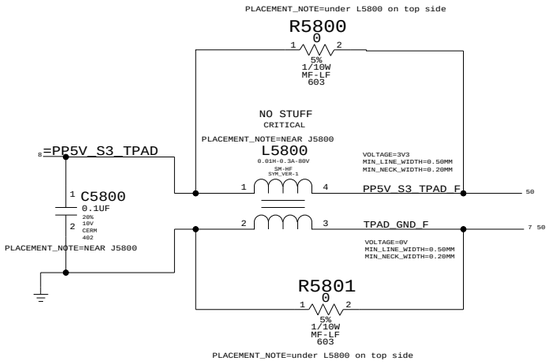
SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

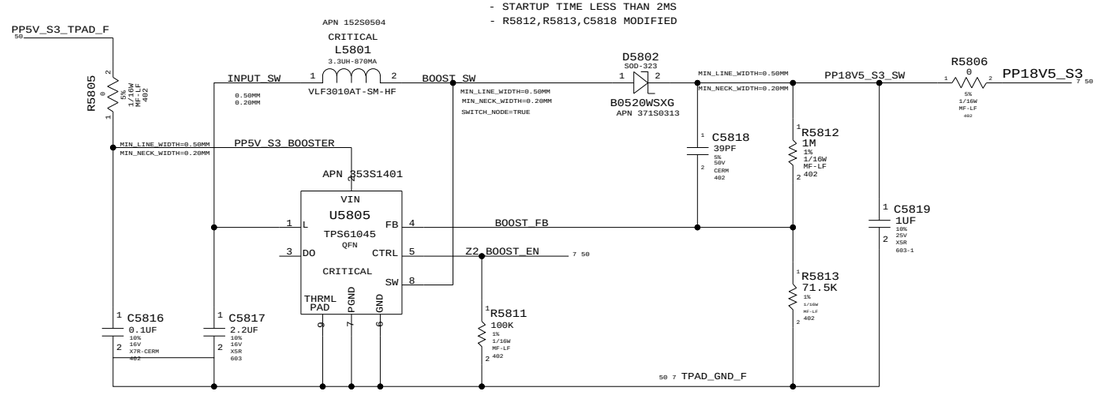
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 57 OF 123	

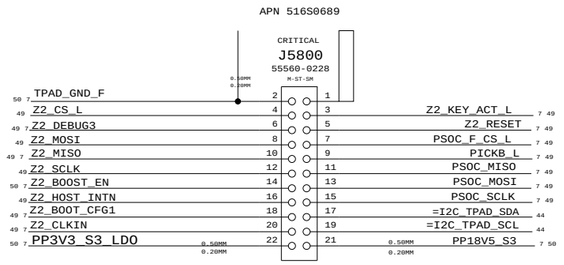
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

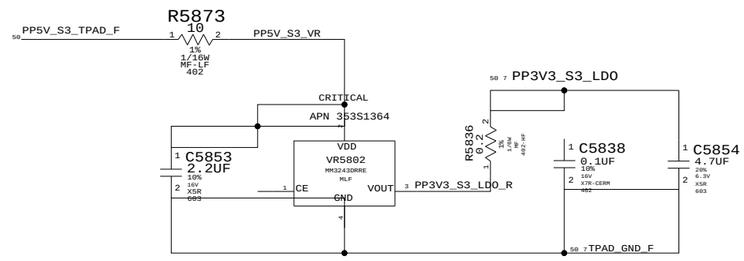




IPD FLEX CONNECTOR



3V3 LDO FOR IPD



Keyboard LED Driver

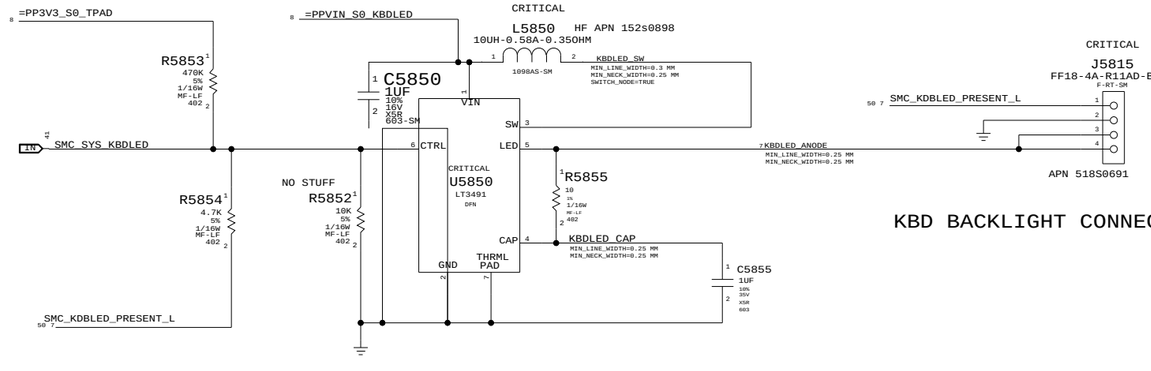
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT



KBD BACKLIGHT CONNECTOR

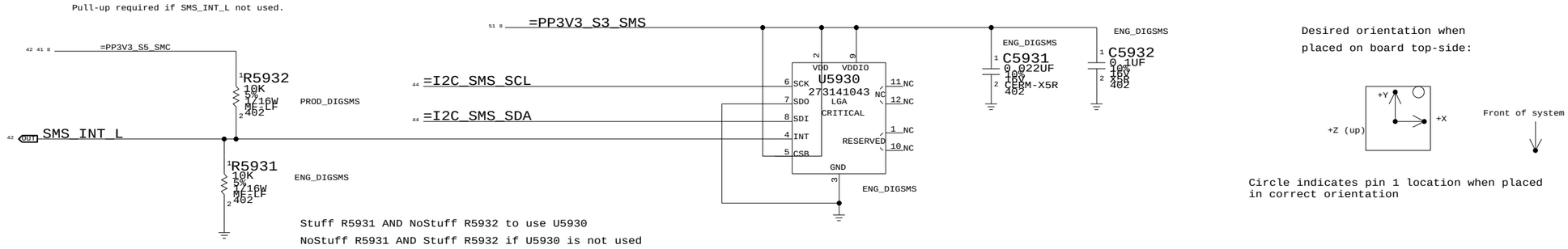
WELLSPRING 2

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

APPLE INC.

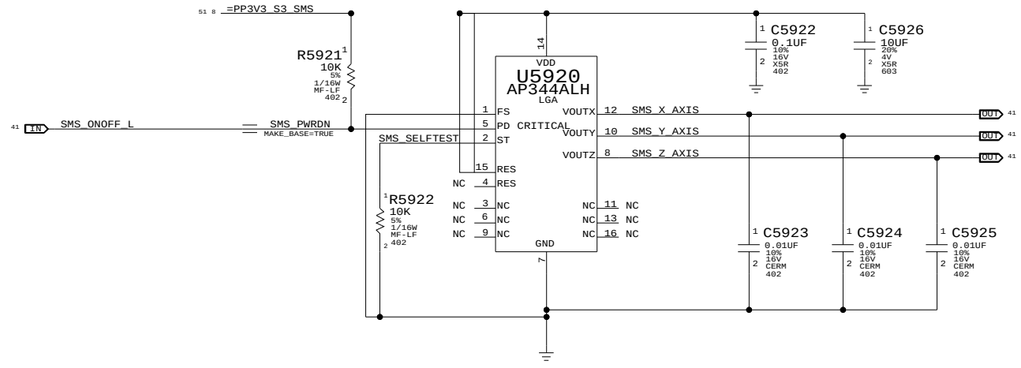
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 58 OF 123	

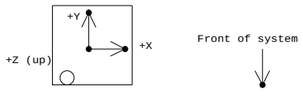
Digital SMS



Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



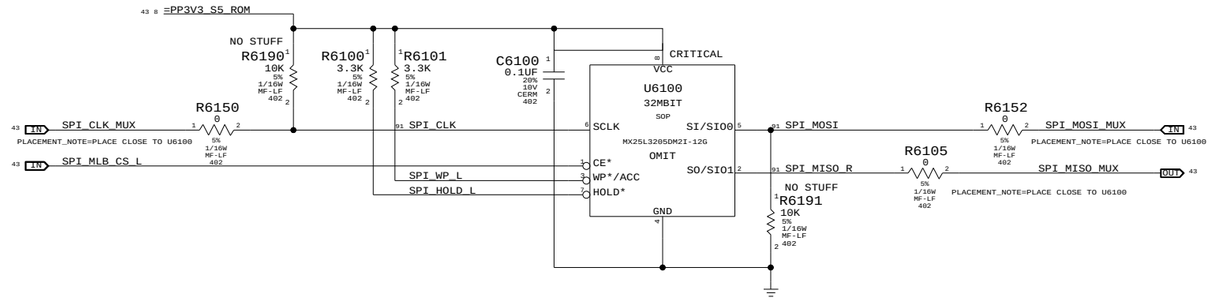


Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 59 OF 123	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

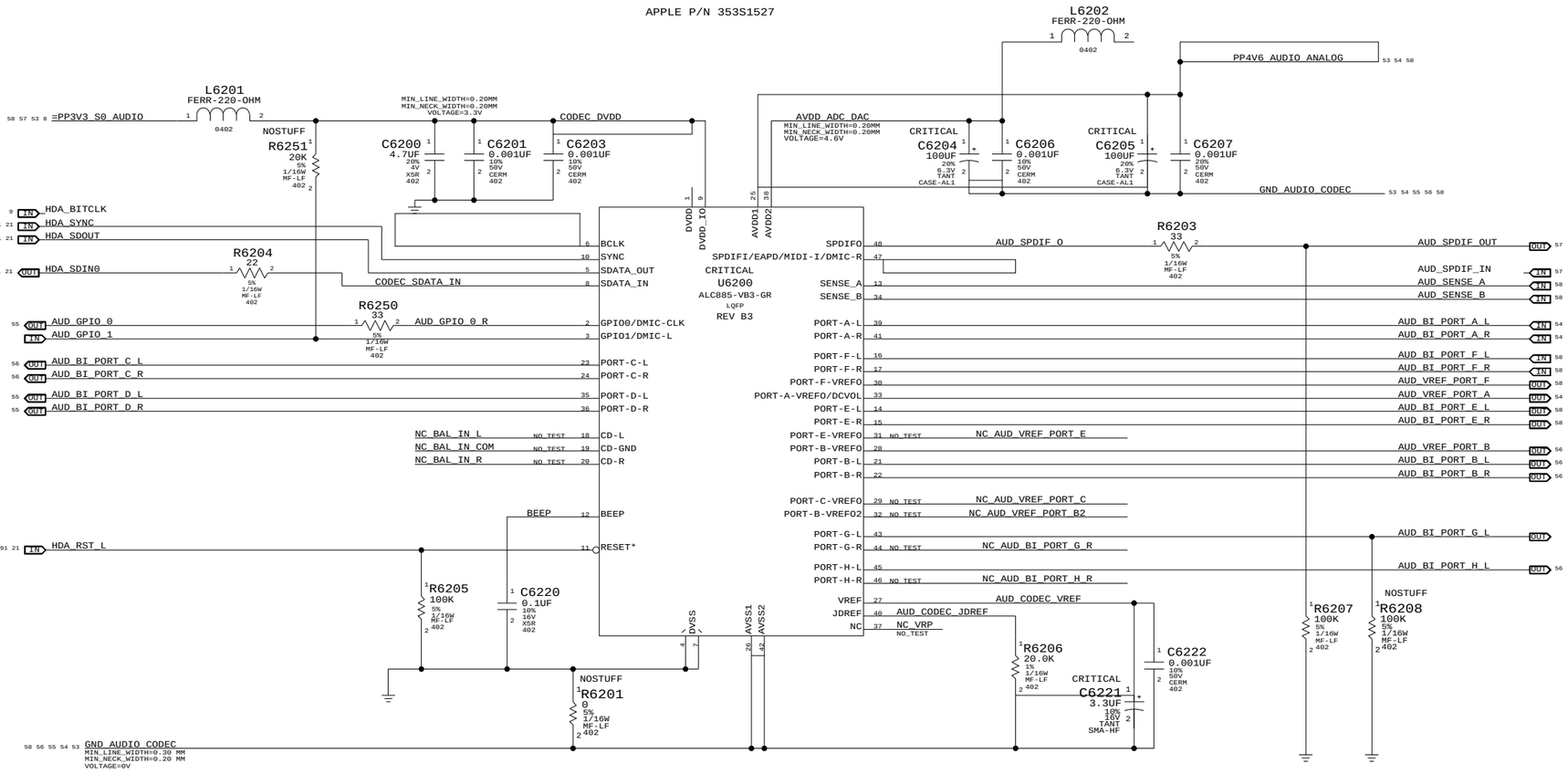
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	61	123

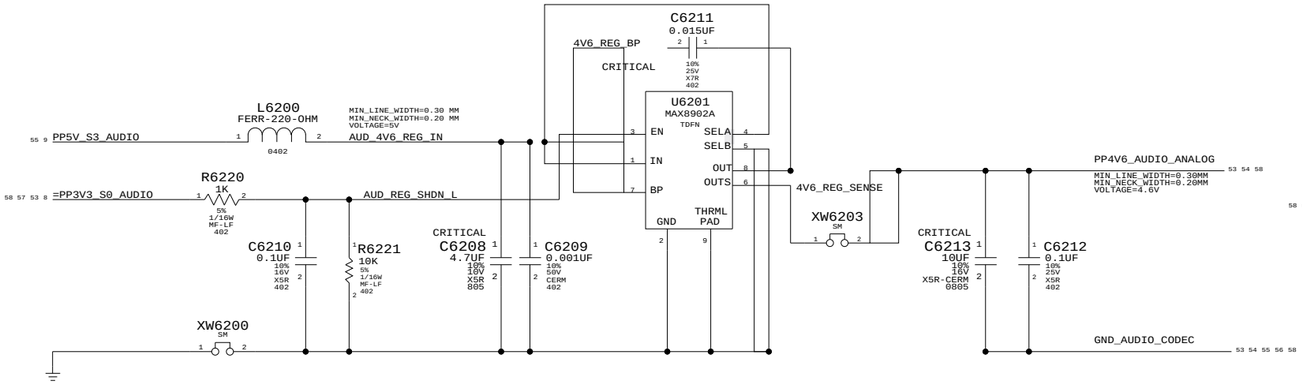
AUDIO CODEC

APPLE P/N 353S1527



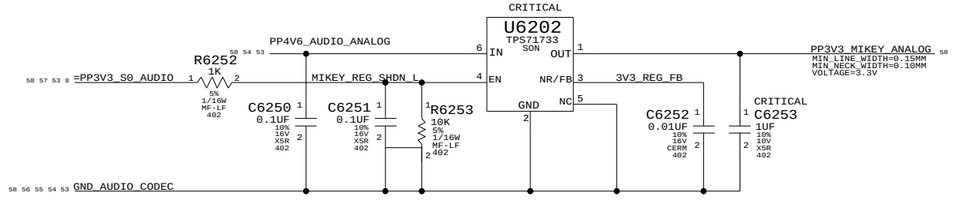
AUDIO 4.6 V REGULATOR

APPLE P/N 353S1897



MIKEY 3.3 V REGULATOR

APPLE P/N 353S1860



AUDIO:CODEC

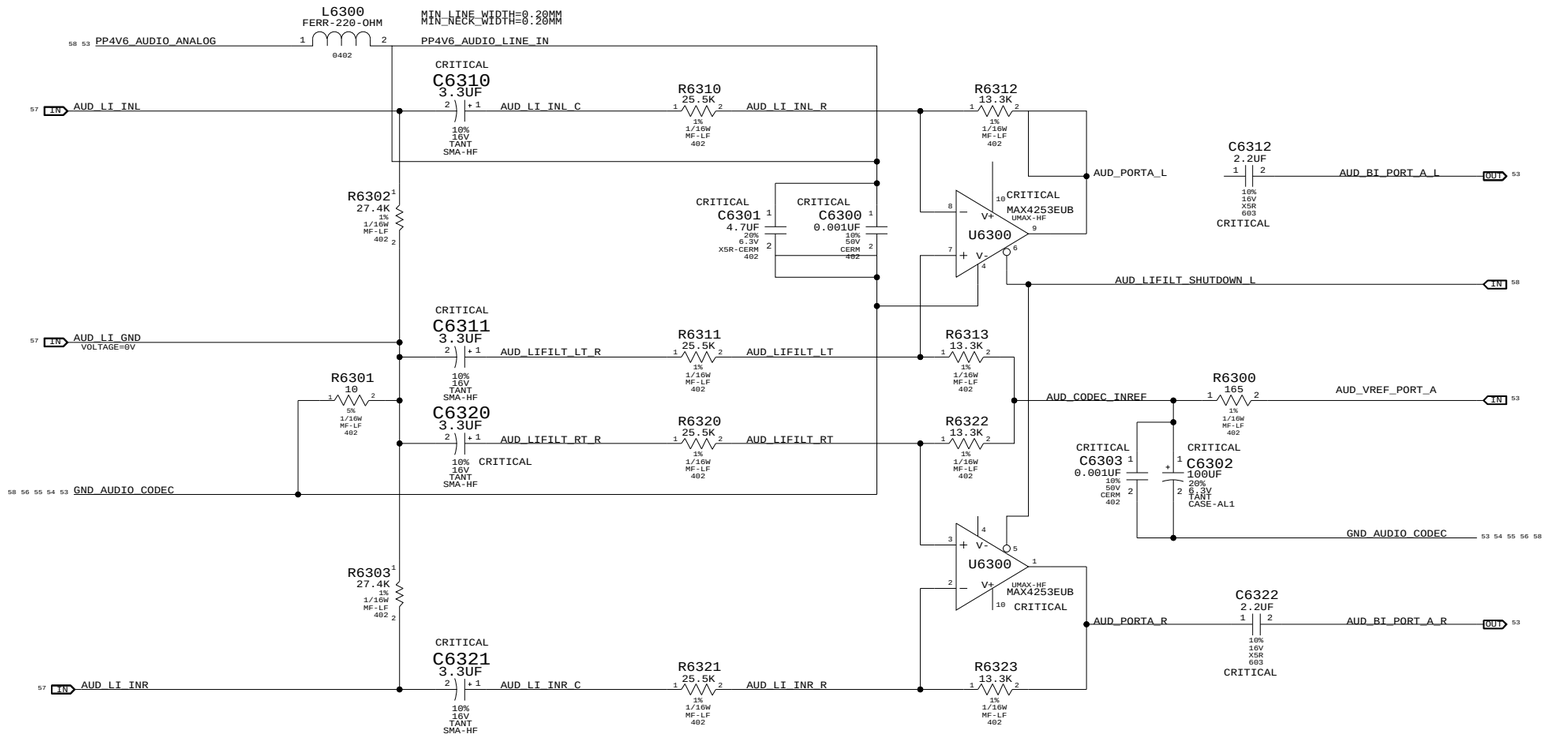
SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	62	123

Pseudo-Diff Line-In Filter
GAIN = -5.4 DB AV = 0.52
FC = 1.89 HZ



AUDIO: LINE IN

SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

APPLE INC.

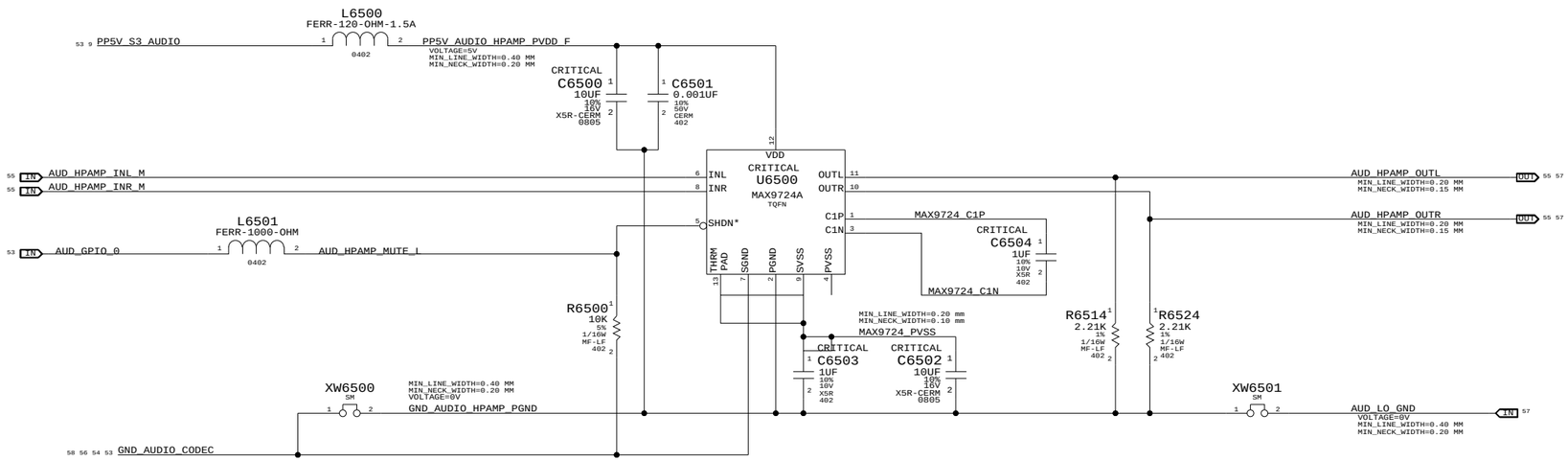
SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE

SHT 63 OF 123

Headphone Amplifier (MAX9724A)

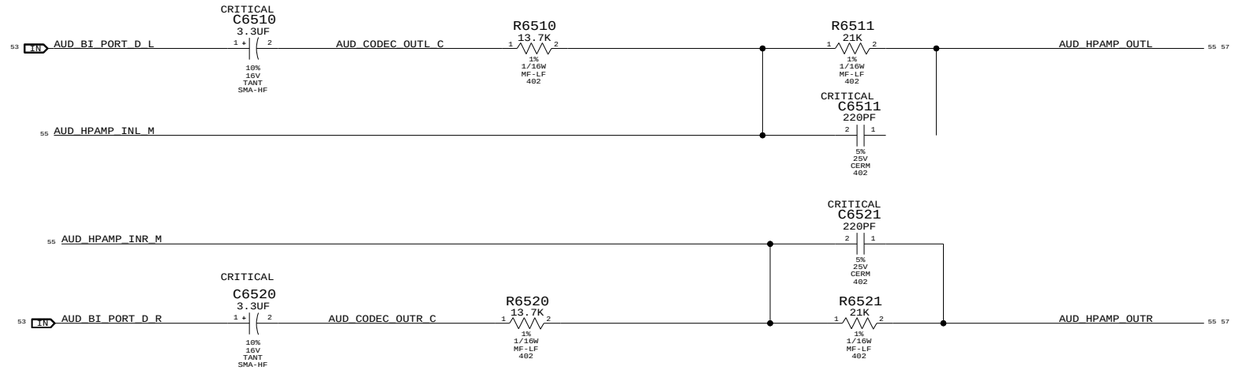
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

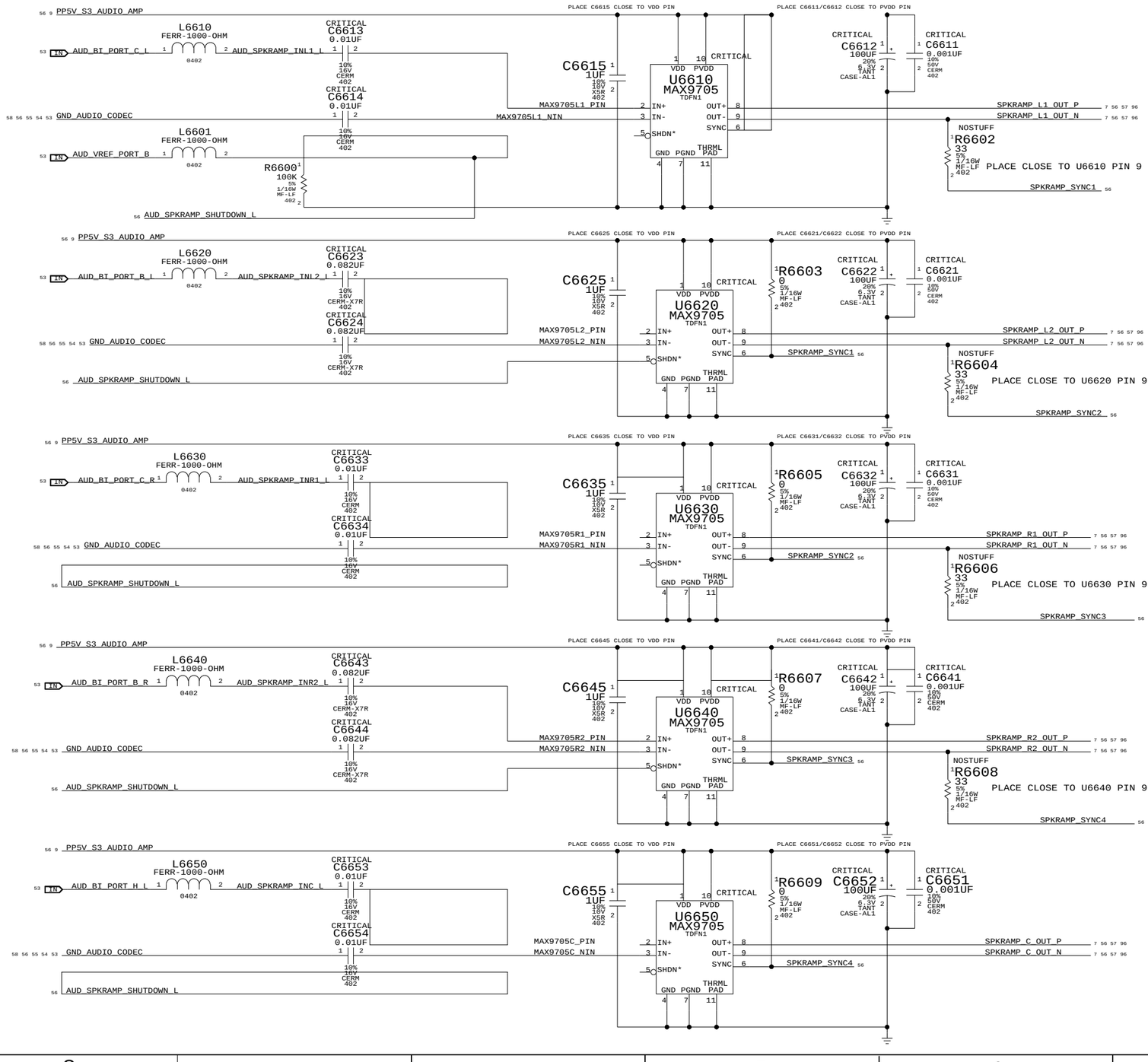
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 65 OF 123	

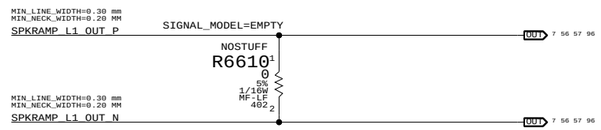
4X MONO SPEAKER AMPLIFIERS (MAX9705)

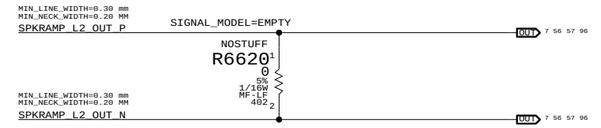
APN: 353S1595
GAIN = 12 DB

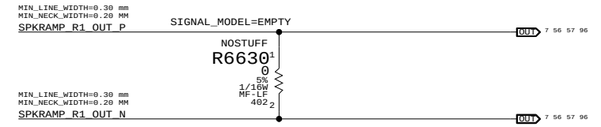
FC (SPEAKERS L1/R1/C) = ~796 HZ
FC (SPEAKERS L2/R2) = ~97 HZ

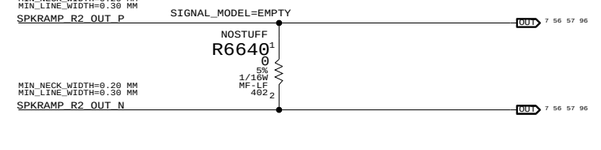


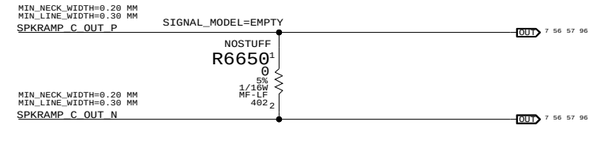
SPEAKER CHECKPOINTS











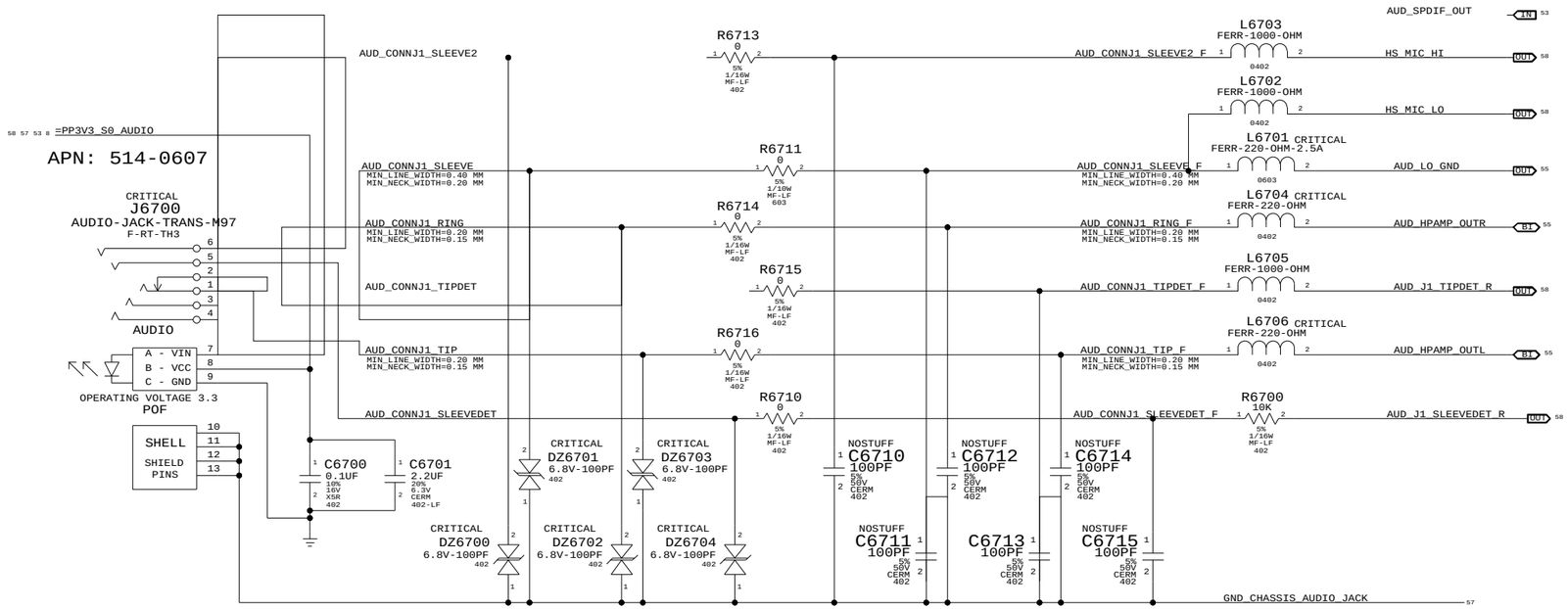
AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

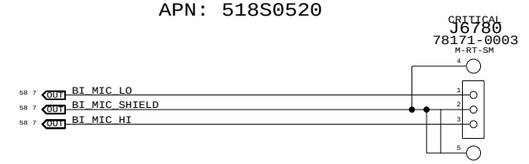
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 66 OF 123	

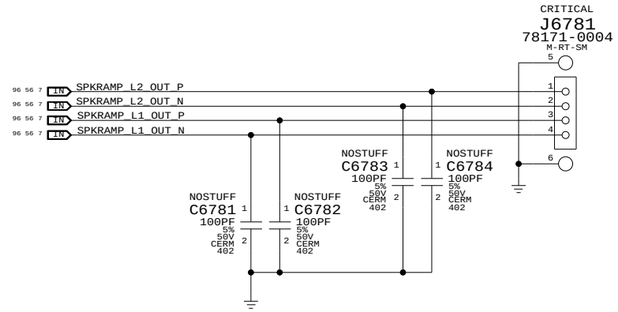
AUDIO JACK 1 LO/HP JACK, SPDIF TX



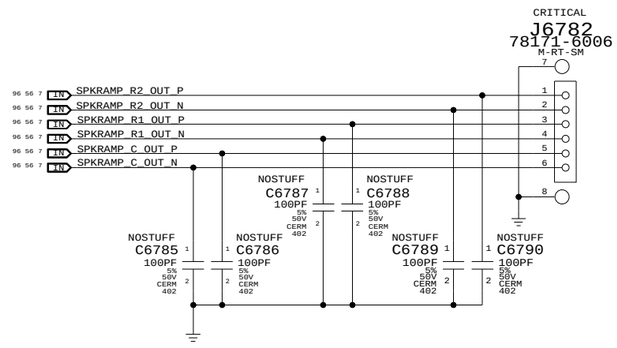
MIC CONNECTOR
APN: 518S0520



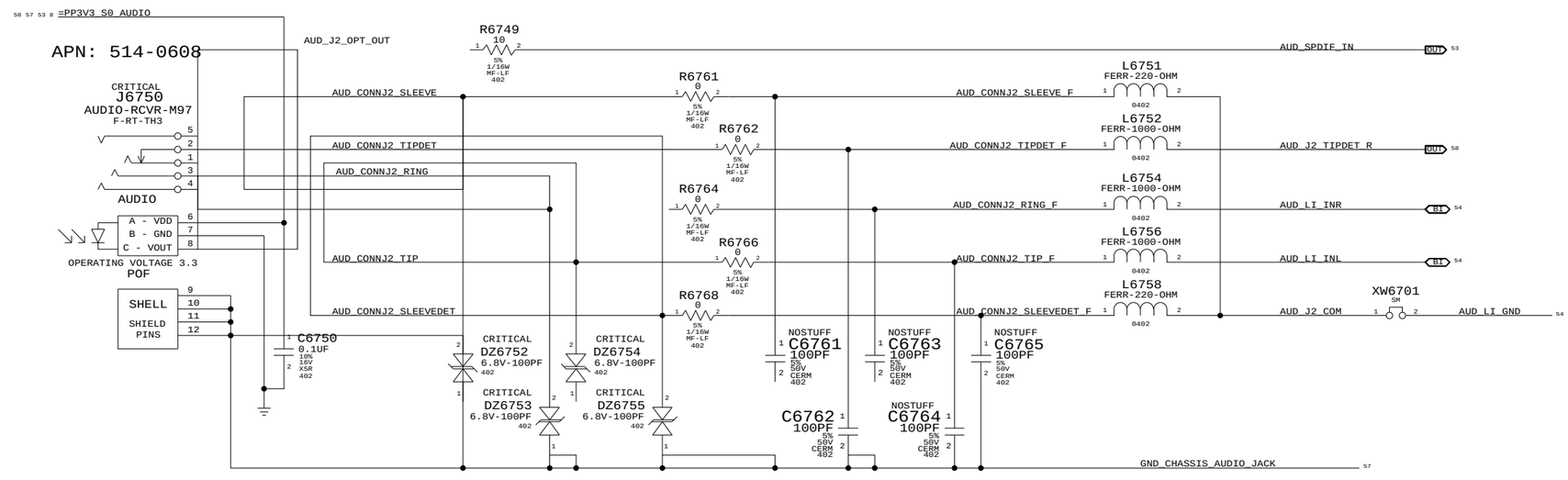
SPEAKER CONNECTORS
APN: 518S0521



APN: 518S0672



AUDIO JACK 2 LINE IN JACK, SPDIF RX



RETURN FOR HF NOISE

AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

APPLE INC.

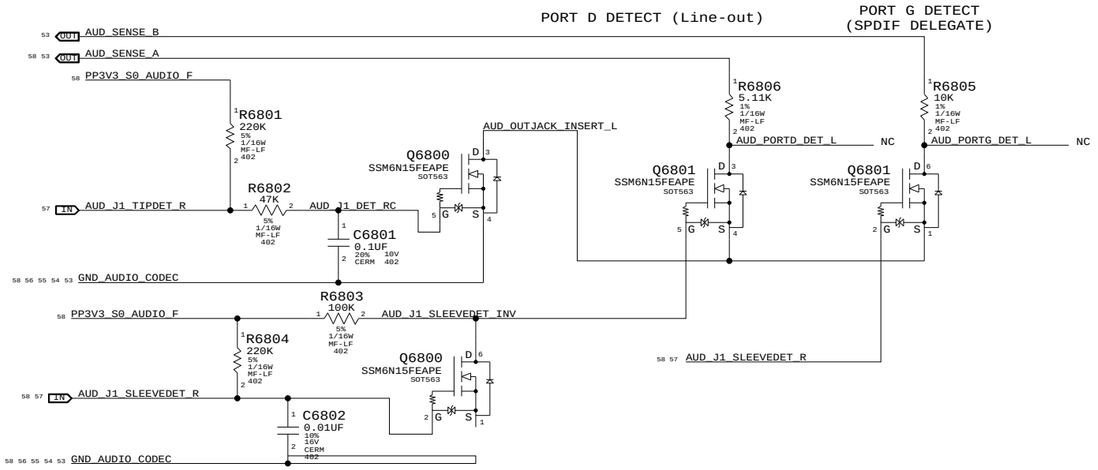
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 67 OF 123	

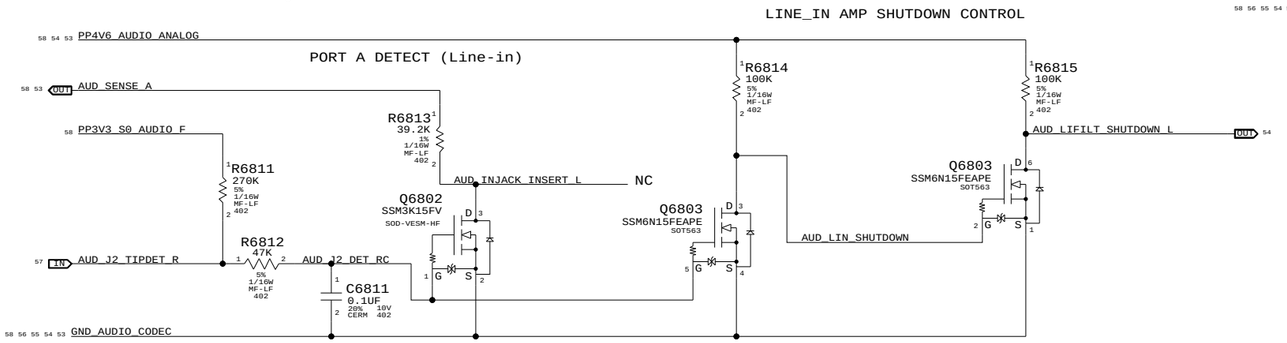
CODEC OUTPUT SIGNAL PATHS

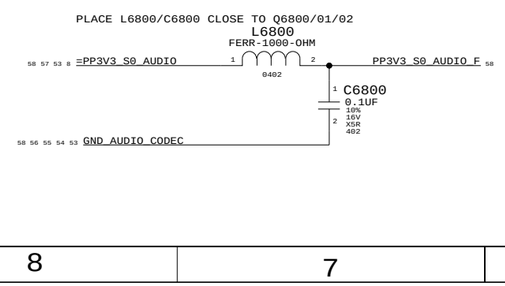
FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

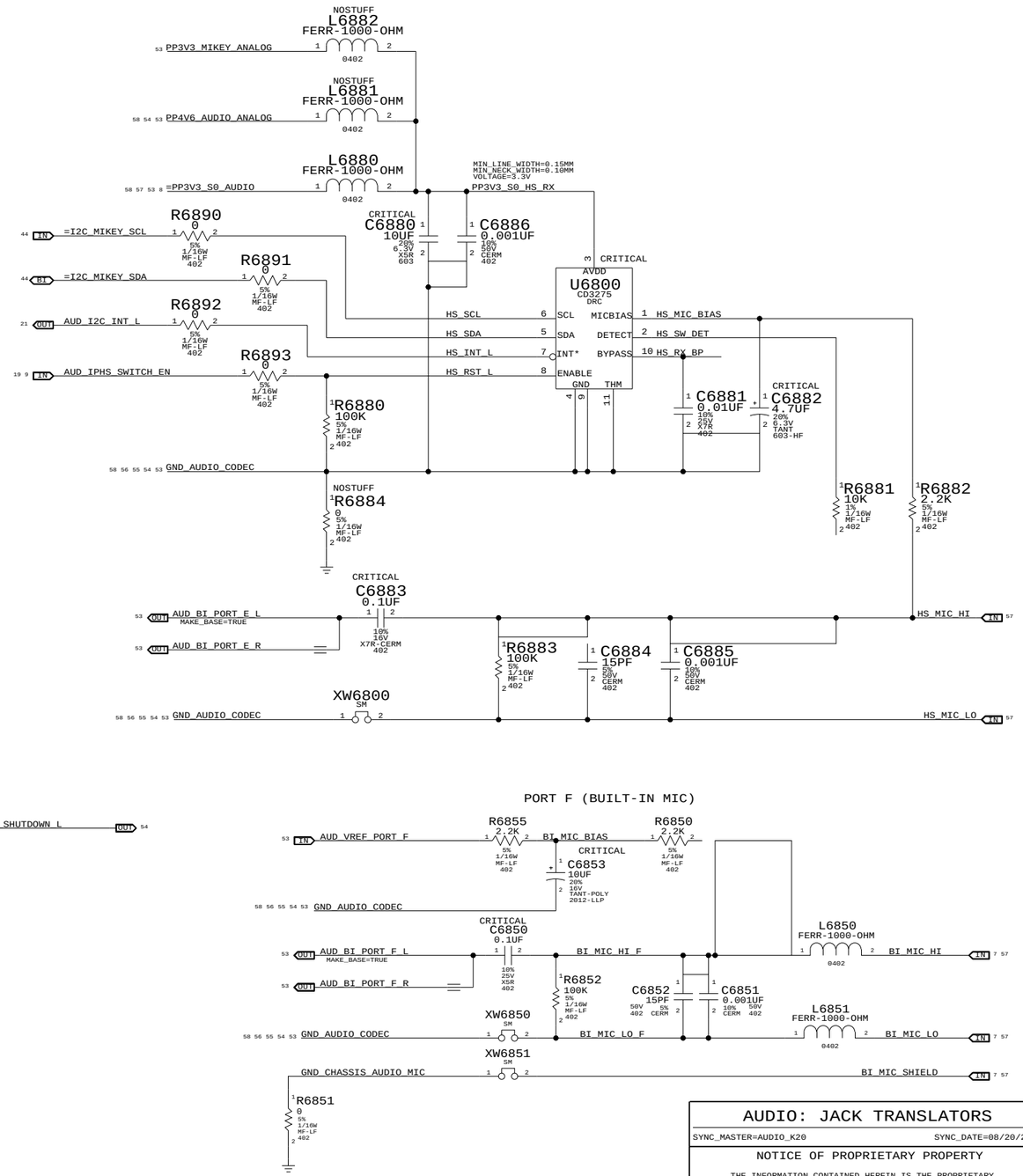
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY









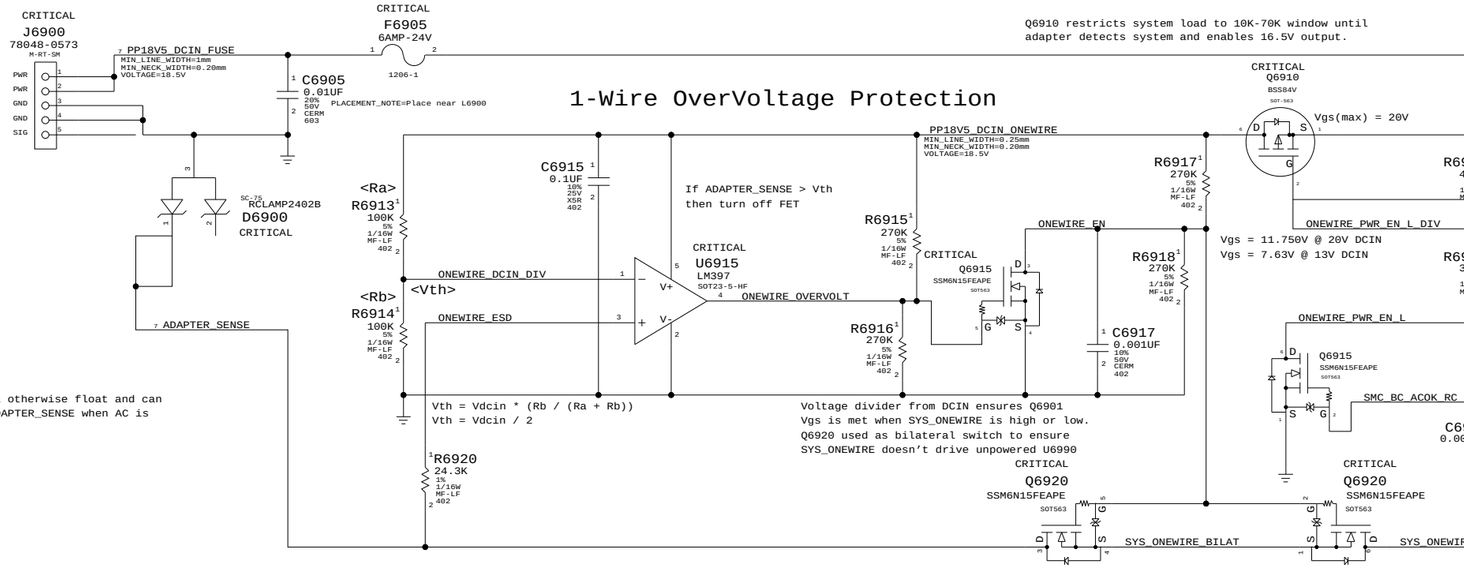
AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=08/20/2008

APPLE INC.

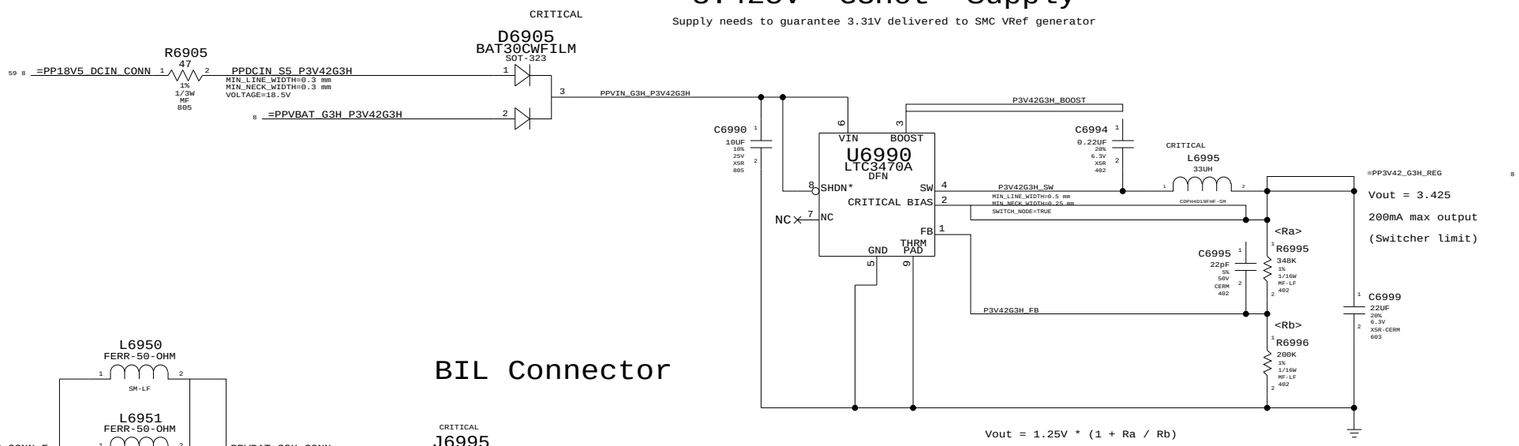
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 68 OF 123	

MagSafe DC Power Jack

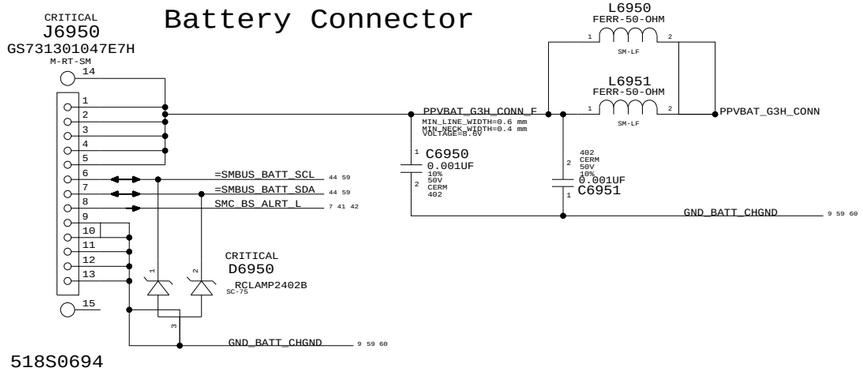


3.425V "G3Hot" Supply

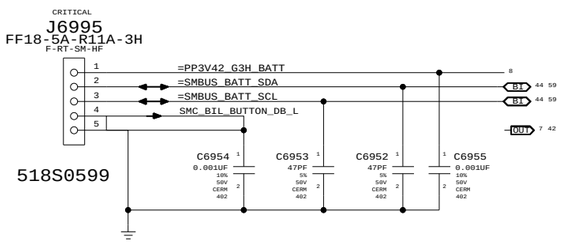
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector



BIL Connector

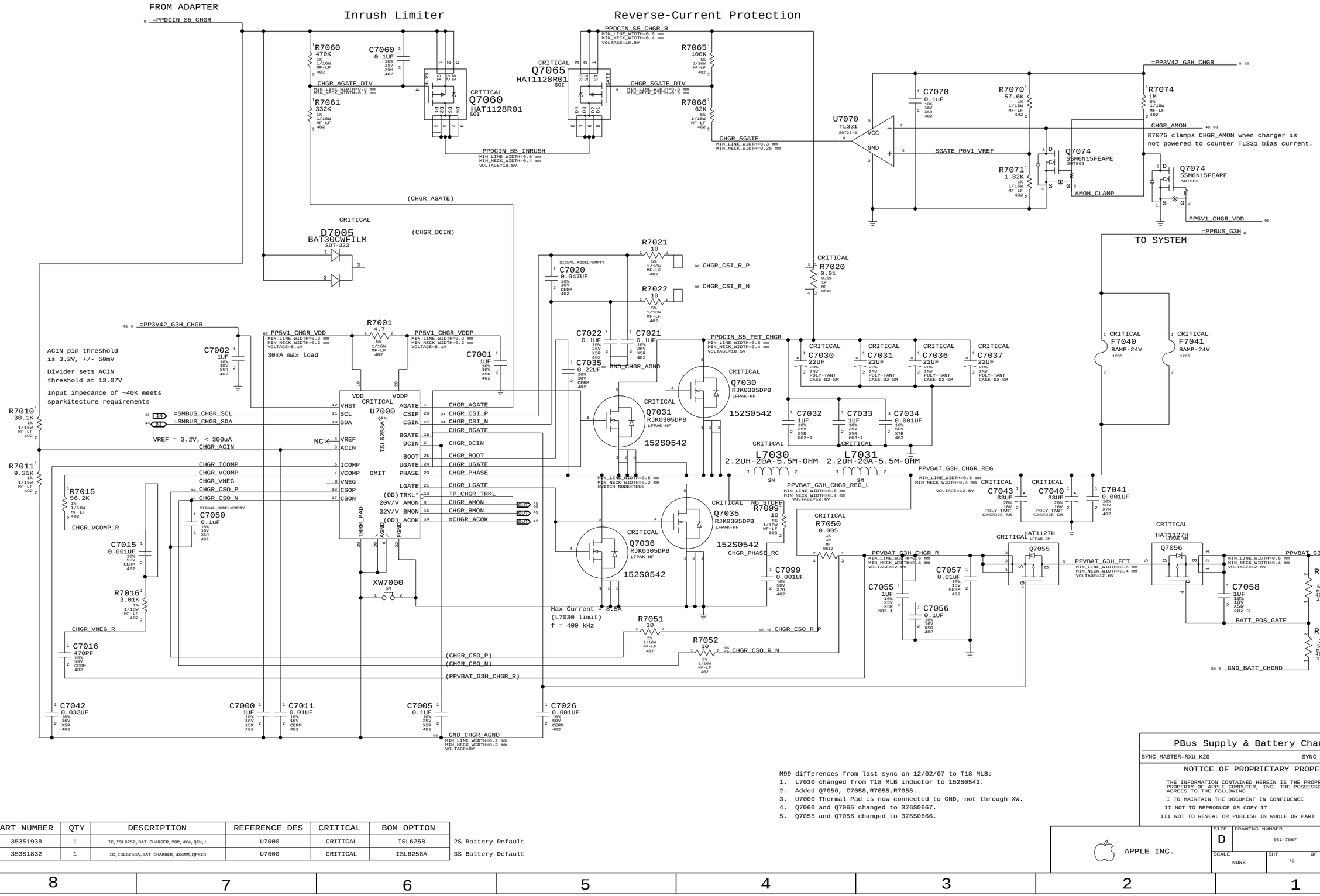


DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 69 OF 123	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

M99 differences from last sync on 12/02/07 to T18 MLB:

1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 70 OF 123	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

Place R7131 Between L7100,L7101 and CPU

NO STUFF

SIGNAL_MODEL=EMPTY

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	100R	

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	100R	

IMVP_VR_ON	IMVP_VR_ON_R			
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		

IMVP6 CPU VCore Regulator

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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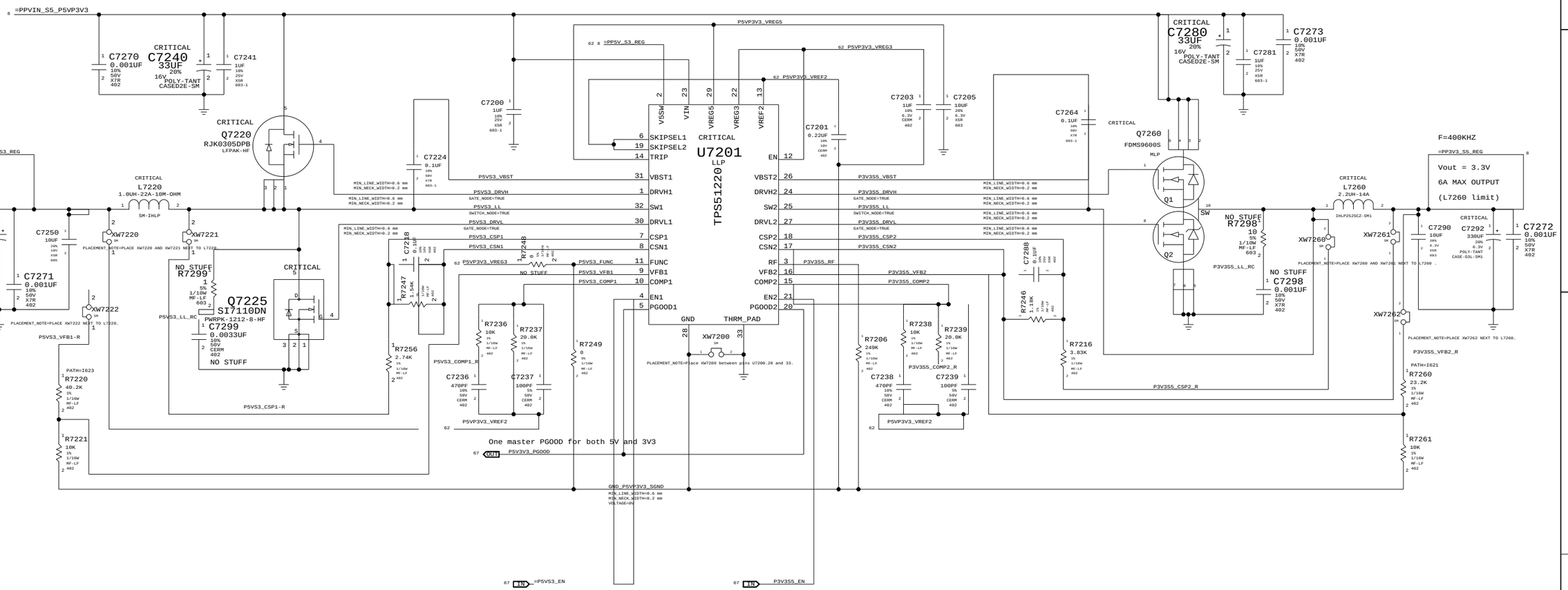
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	71	123



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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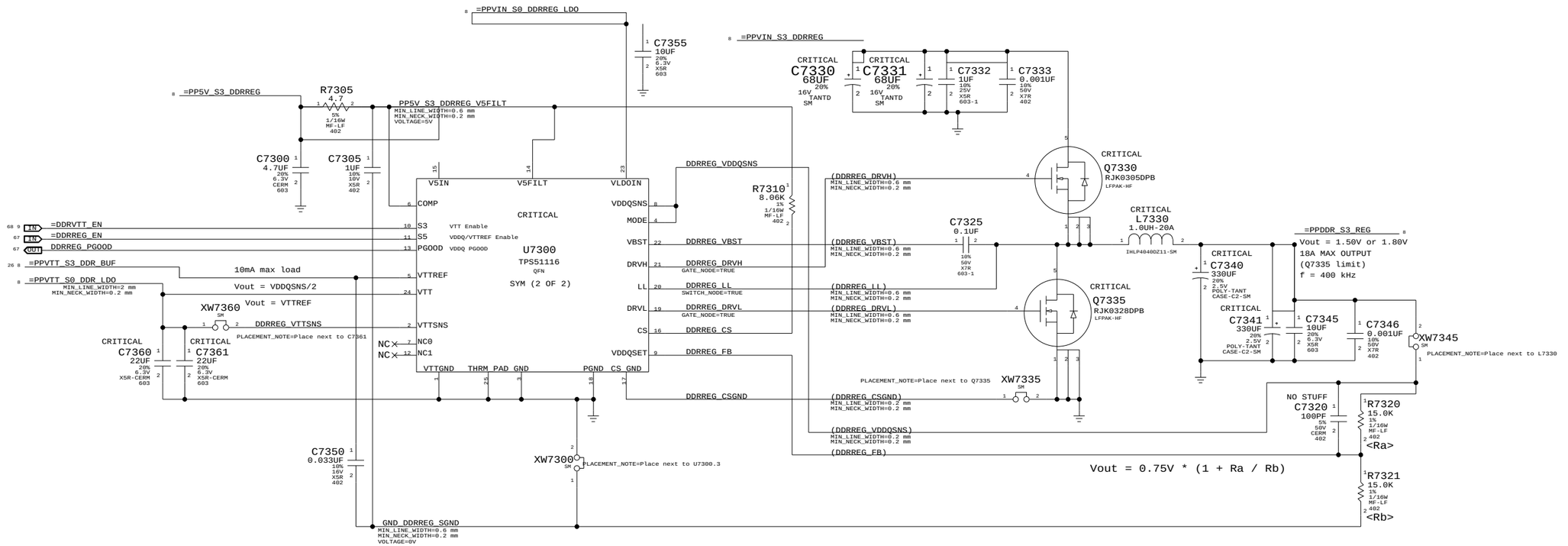
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 72 OF 123	

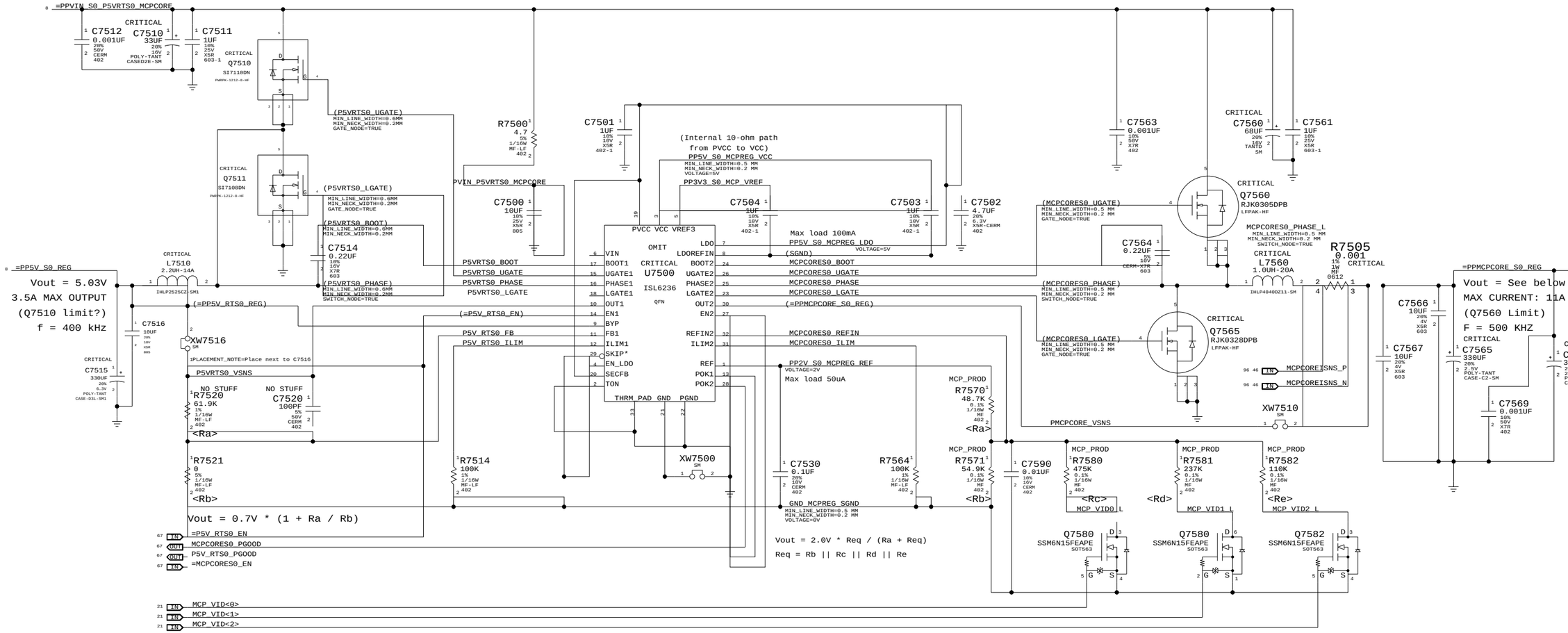


1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 73 OF 123	



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U7500	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

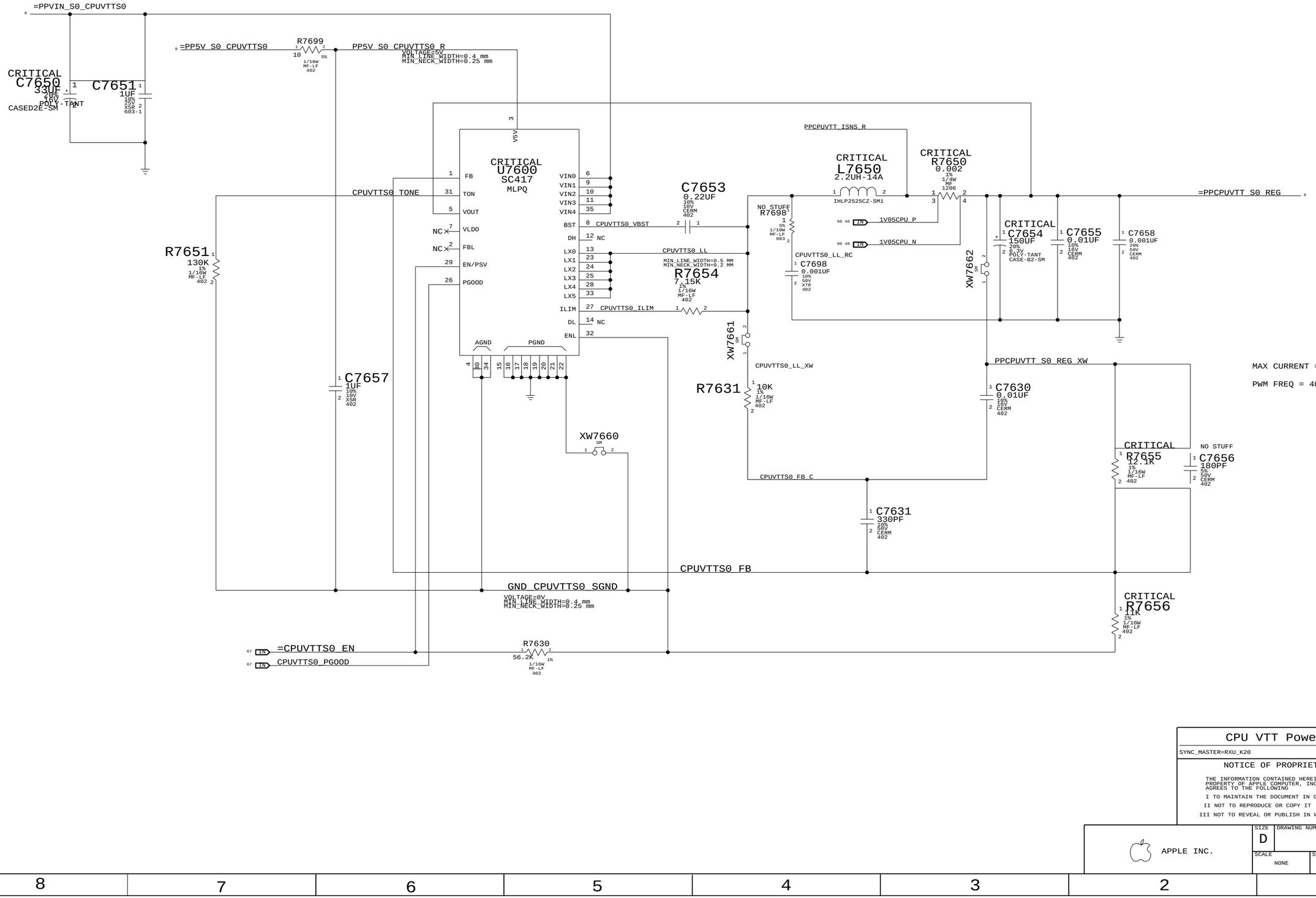
5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 75 OF 123



CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	76	123

1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature

=PP3V3_S3_P1V8S0

C7700 2.2UF 20% 6.3V CERM 402-LF

CRITICAL L7780 2.2UH-1.2A PCAA031B-SM

P1V0FW_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

C7782 10PF 5% 50V CERM 402

<Ra> R7782 187K 1% 1/16W MF-LF 402

=PP1V0_FW_REG

Vout = 1.001V
300mA max output
(Switcher limit)
f = 2.25 MHz

C7785 4.7UF 20% 4V X5R 402

<Rb> R7783 280K 1% 1/16W MF-LF 402

P1V0FW_VFB

U7700 DFN-HF CRITICAL LTC3621

VIN, SW1, SW2, VFB1, VFB2, RUN1, RUN2, THRML PAD, GND

P1V8S0_LX MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm SWITCH_NODE=TRUE

CRITICAL L7700 2.2UH-1.2A PCAA031B-SM

C7701 10PF 5% 50V CERM 402

<Ra> R7700 562K 1% 1/16W MF-LF 402

<Rb> R7701 280K 1% 1/16W MF-LF 402

=PP1V8_S0_REG

VOUT = 1.804V
0.3A max output
(Switcher limit)
F = 2.25 MHZ

C7705 4.7UF 20% 4V X5R 402

P1V8S0_VFB

=P1V8S0_EN

=PP3V3_FW_P1V0FW

Vout = 0.6V * (1 + Ra/Rb)

MCP79 PLL VLDO

=PP3V3_S0

C7740 0.1UF 20% 10V CERM 402

C7741 1UF 10% 6.3V CERM 402

U7740 LTC3025 DFN

BIAS CRITICAL, IN, SHDN*, GND, OUT, ADJ, THRML PAD

=PP1V05_S0_FET

NO STUFF
R7742 0 5% 1/16W MF-LF 402

MAX CURRENT = 300MA

=PP1V05_S0_MCP_PLL_UF

Vout = 1.052V

<Ra> R7740 66.5K 1% 1/16W MF-LF 402

<Rb> R7741 40.2K 1% 1/16W MF-LF 402

C7742 1UF 10% 6.3V CERM 402

P1V05_S0_MCP_PLL_UF_ADJ

FW BOOST POWER

=PPVIN_PFWBOOST

R7790 0.02 0.5% 1W MF 0612

PFWBOOST_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

CRITICAL L7795 4.7UH-10A PCMC063T-SM

PFWBOOST_BOOST MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C7790 10UF 10% 16V X5R 1206

CRITICAL U7790 LTC1872 SOT23-6

VIN, ITH/RUN, SENSE-, VFB, NGATE, GND

PFWBOOST_ITH, PFWBOOST_SENSE, PFWBOOST_NGATE, PFWBOOST_FB

R7797 38.3K 1% 1/16W MF-LF 402

C7797 0.0012UF 10% 50V CERM 402

PFWBOOST_ITH_R

CRITICAL D7790 D0222-SM STPS1L30MF

CRITICAL Q7790 SUD45P03-15 FDC796NG

C7795 33PF 5% 50V CERM 402

<Ra> R7795 1.00M 1% 1/4W MF-LF 1206

<Rb> R7796 86.6K 1% 1/16W MF-LF 402

C7794 1UF 10% 16V X5R 402

=PFWBOOST_REG

VOUT = 10V
?MA MAX OUTPUT
F=550KHZ?

C7799 33UF 20% 16V POLY-TANT CASED2E-SM

C7798 33UF 20% 16V POLY-TANT CASED2E-SM

VOUT = 0.8V * (1 + RA / RB)

1.8V S0 Switcher

INPUT RAIL IS 3.3V S0

=PP3V3_GPU_P1V8S0

C7760 10UF 20% 6.3V X5R 603

U7760 TPS62202 SOT23-5 CRITICAL

VI, FB, EN, GND, SW

=P1V8FB_EN

CRITICAL L7760 10UH-0.55A-330MOHM PCAA031B-SM

P1V8GPU_SW

MAX CURRENT = 300MA

=PP1V8_GPUIFPX_REG

C7762 10UF 20% 6.3V X5R 603

MCP 1.05V AUXC Supply

=PPVIN_S0_P1V05S5

C7752 1UF 10% 25V X5R 603-1

P5V_P1V05S5_V5FILT

R7751 4.7 5% 1/16W MF-LF 402

P5V_P1V05S5 MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V

C7751 4.7UF 20% 6.3V CERM 603

U7750 ISL6269 QFN CRITICAL

PVCC, VCC, VIN, FSET, EN, FCCM, PGOOD, COMP, FB, VO, UG, BOOT, PHASE, ISEN, LG, PGND, THRML PAD

C7750 2.2UF 10% 16V X5R 603

P1V05S5_DRVH GATE_NODE=TRUE

P1V05S5_VBST

P1V05S5_LL SWITCH_NODE=TRUE

P1V05S5_DRVL GATE_NODE=TRUE

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

C7770 0.22UF 10% 10V CERM 402

P1V05S5_ISEN

R7779 2.0K 1% 1/16W MF-LF 402

=PPVIN_S0_P1V05S5

C7775 1UF 10% 25V X5R 603-1

CRITICAL Q7770 SI7110DN PWRPK-1212-8-HF

CRITICAL Q7771 SI7108DN PWRPK-1212-8-HF

P1V05_S5_FSET

R7752 38.3K 1% 1/16W MF-LF 402

=P1V05S5_EN

P1V05_S5_PGOOD

C7753 0.01UF 10% 16V CERM 402

P1V05_S5_COMP

R7753 49.9K 1% 1/16W MF-LF 402

C7755 47PF 5% 50V CERM 402

P1V05S5_VFB

P1V05S5_COMP_R

C7754 470PF 10% 50V CERM 402

XW7750 SM

GND_P1V05S5_SGND MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

(P1V05S5_VFB)

(=PP1V05_S5_REG)

Vout = 0.6V * (1 + Ra / Rb)

CRITICAL L7770 2.2UH-8.0A PCMB065T-SM

PLACEMENT_NOTE=Place XW7775 next to C7775

=PP1V05_S5_MCP

Vout = 1.052V
5A max output
(L7770 limit)
f = 400 kHz

XW7775 SM

C7776 4.7UF 20% 4V X5R 402

CRITICAL C7771 330UF 20% 2.0V POLY-TANT B2-SM

P1V05S5_VSNS

<Ra> R7780 3.74K 1% 1/16W MF-LF 402

<Rb> R7781 4.42K 1% 1/16W MF-LF 402

EXPRESSCARD 1.5V_S0 SUPPLY

=PP3V3_S3_P1V5EXPS0

R7712 1 5% 1/16W MF-LF 402

CRITICAL C7710 22UF 20% 6.3V CERM 805

P1V5EXPS0_AVIN

CRITICAL L7710 2.2UH-1.2A PCAA031B-SM

=P1V5_EXP_S0_EN

CRITICAL U7710 TPS62510 BQA

AVIN, PVIN, EN, OVT, MODE, SW, FB, PG, AGND, PGND, THRM_PAD

P1V5EXPS0_SW, P1V5EXPS0_FB

C7711 0.1UF 10% 10V X5R 402

TP_P1V5_EXP_S0_PGOOD

P1V5EXPS0_SGND

C7712 22PF 5% 50V CERM 402

<Ra> R7710 150K 1% 1/16W MF-LF 402

<Rb> R7711 100K 1% 1/16W MF-LF 402

CRITICAL C7713 22UF 20% 6.3V CERM 805

=PP1V5_EXP_S0

Vout = 1.5V
MAX Current = 1.2A
FREQ = 1Mhz

XW7710 SM

VOUT = 0.6V * (1 + Ra / Rb)

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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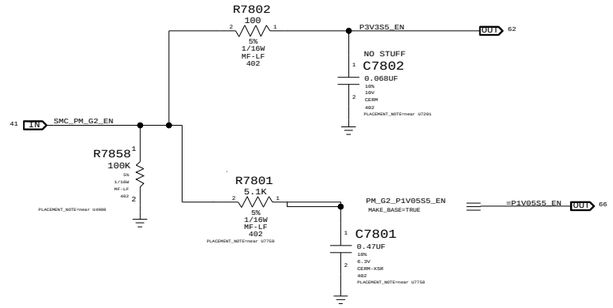
SIZE	DRAWING NUMBER	REV.
D	051-7867	01

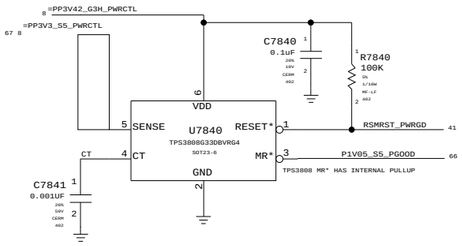
SCALE: NONE SHT 77 OF 123

3.3V 1,05V S5 ENABLE

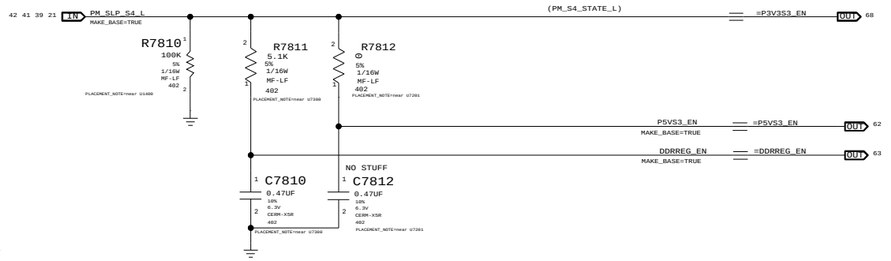


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

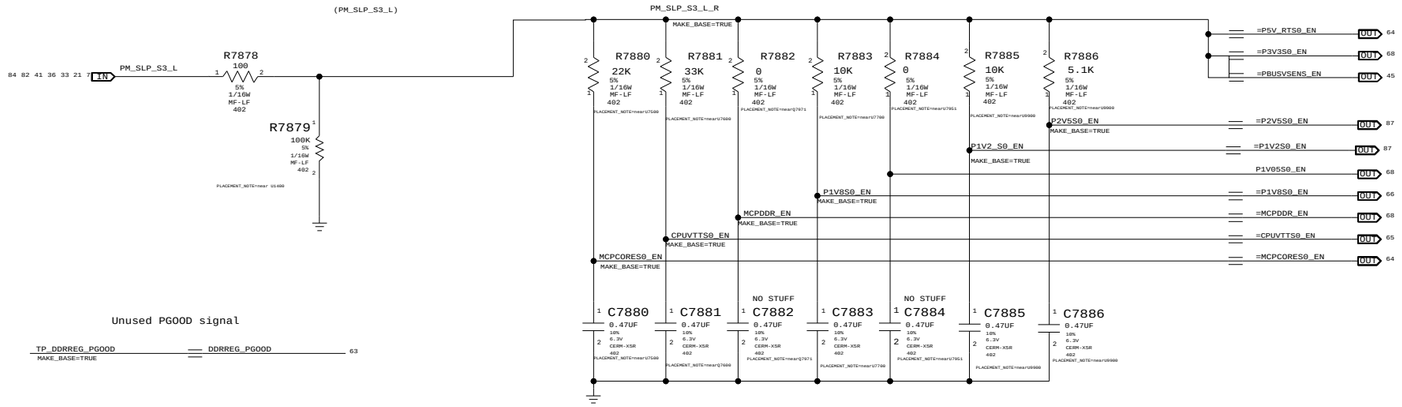
S5 rail PWRGD



3.3V,5V S3 ENABLE

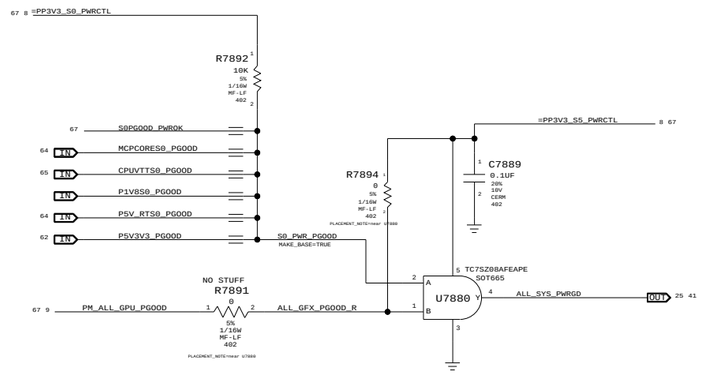


S0 ENABLE



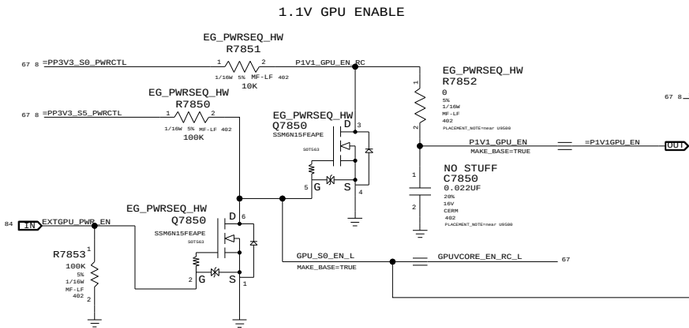
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

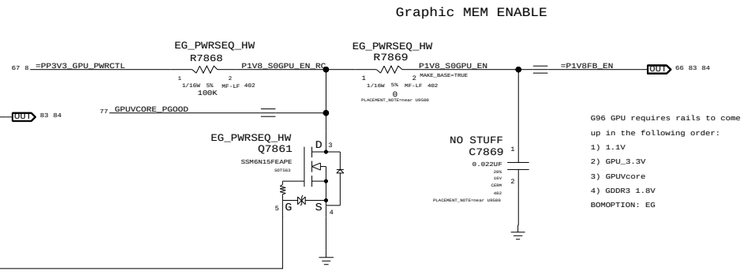


Unused PGOOD signal

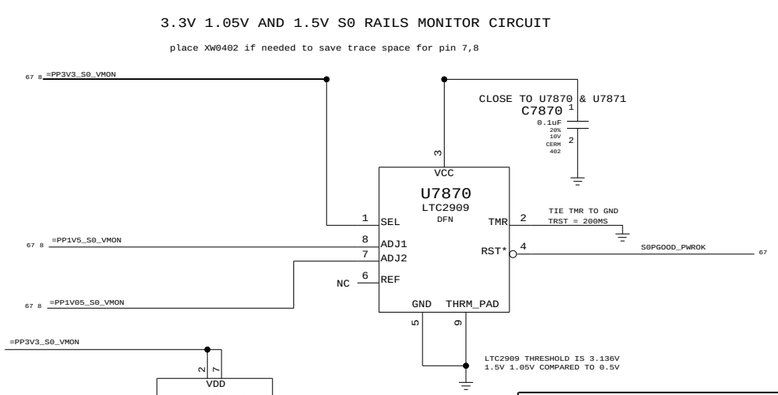
1.1V GPU ENABLE



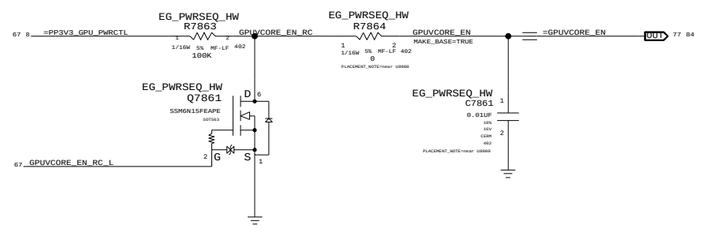
Graphic MEM ENABLE



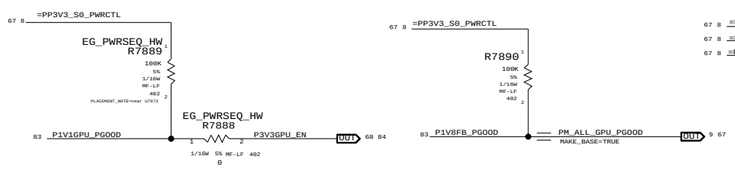
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



GPUVCORE ENABLE



EXT GPU PWRGD Pullup



Power Control		
SYNC_MASTER=YMA_K20		SYNC_DATE=09/09/2008

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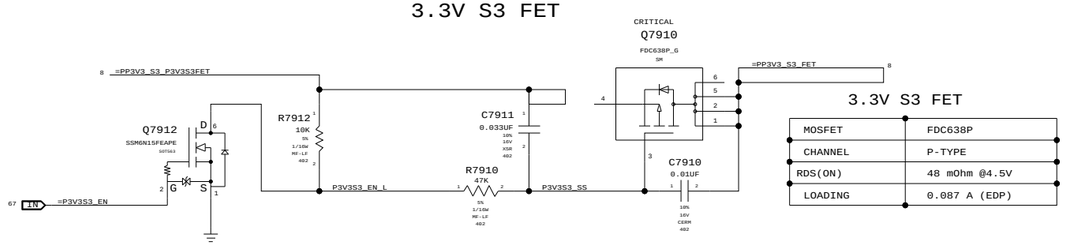
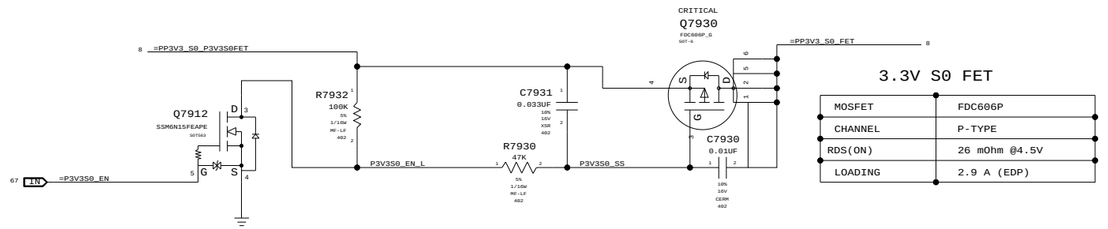
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 78 OF 123	

3.3V S3 FET



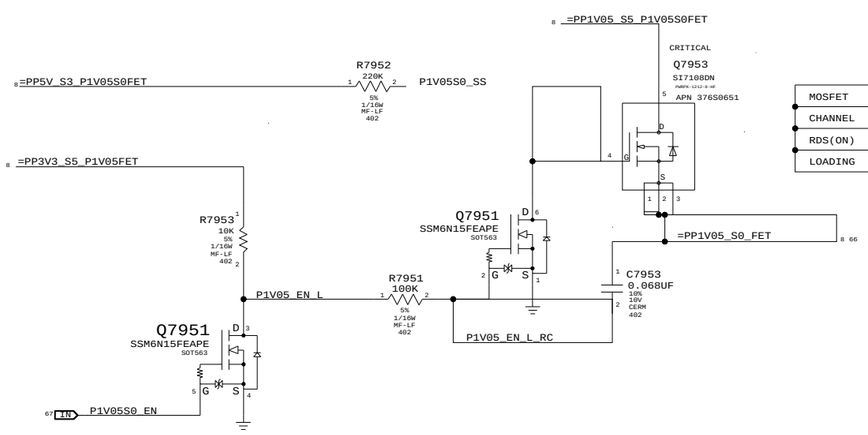
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



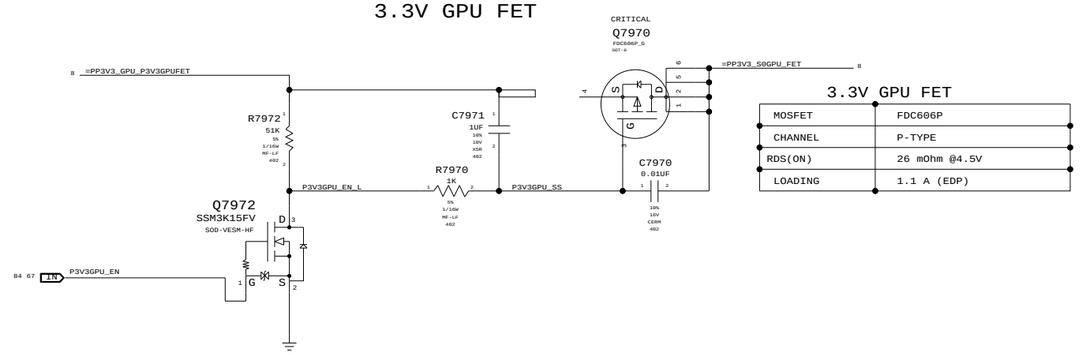
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



1.05V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

3.3V GPU FET

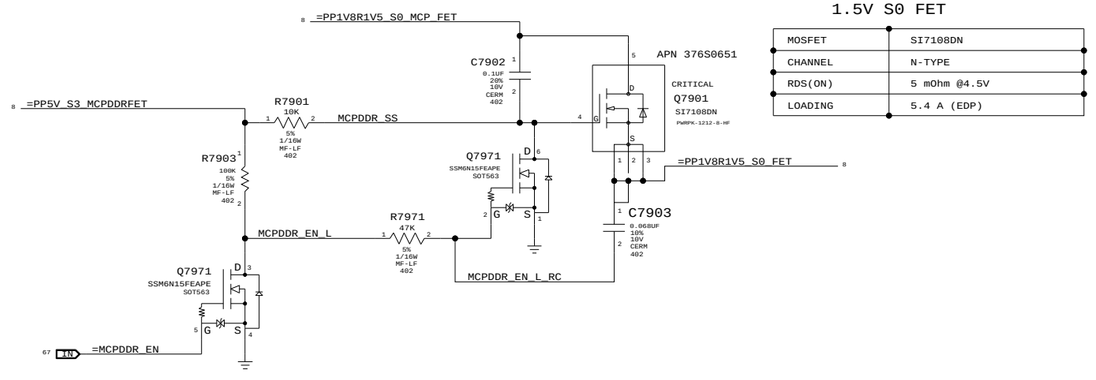


3.3V GPU FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

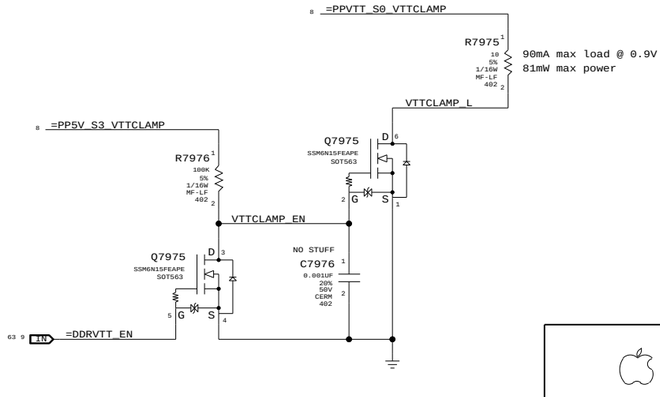
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



1.5V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

APPLE INC.

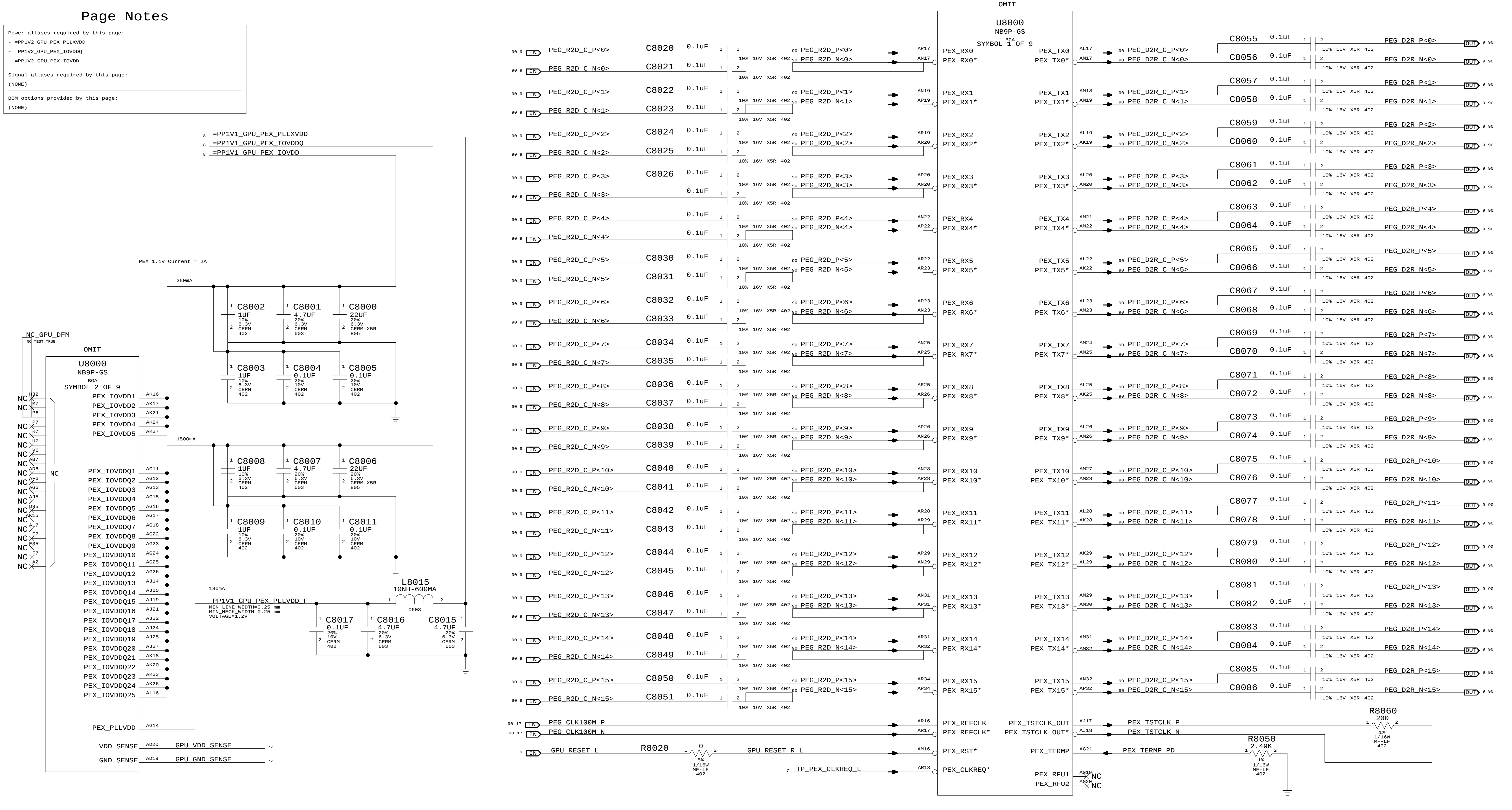
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 79 OF 123	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	80	123

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402
C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402
C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

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OMIT

L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17 — VDD

V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20 — VDD

U8000 NB9P-GS BGA SYMBOL 8 OF 9

B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16 — GND

V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30 — GND

=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

U8000 NB9P-GS BGA SYMBOL 7 OF 9

OMIT

B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16 — FBVDDQ

J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31 — FBVDDQ

NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 81 OF 123	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NB9P-GS
BGA
SYMBOL 3 OF 9

OMIT

U8000
NB9P-GS
BGA
SYMBOL 4 OF 9

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

NV G96 FRAME BUFFER I/F

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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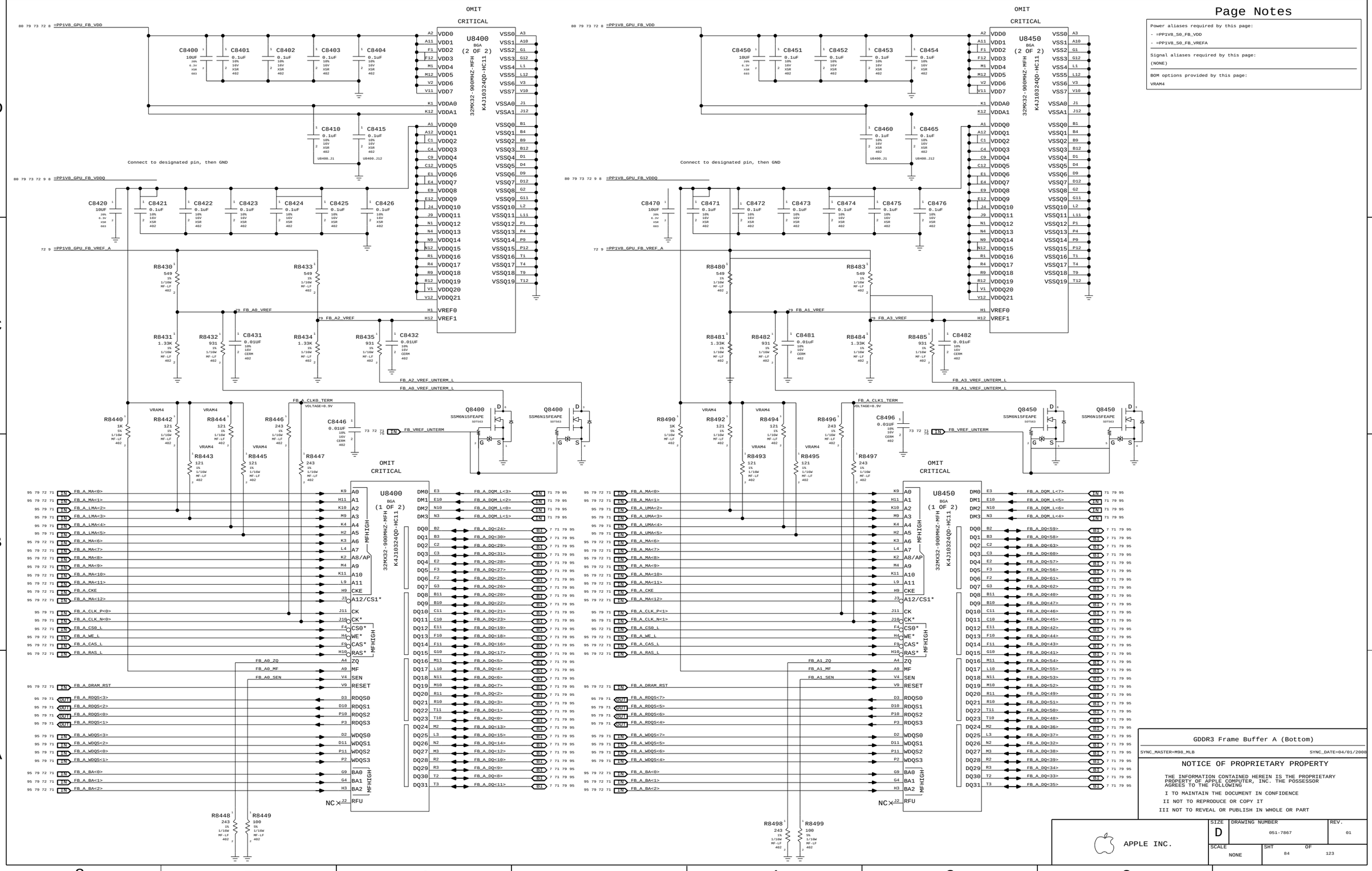
SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT: 82 OF 123	


OMIT
CRITICAL
U8400
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
U8450
(1 OF 2)
Connect to designated pin, then GND
=PP1V8_GPU_FB_VDD
=PP1V8_GPU_FB_VDDQ
=PP1V8_GPU_FB_VREF_A
FB_A_CLK0_TERM
VOLTAGE=0.9V
FB_A_CLK1_TERM
VOLTAGE=0.9V
FB_VREF_UNTERM
VRAM4
MFHIGH
Q8400
SSM6N15FEAPE
Q8450
SOT563
FB_A_MA<0>
FB_A_MA<1>
FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
FB_A_LMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_MA<12>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L
FB_A_DRAM_RST
FB_A_RDQS<3>
FB_A_RDQS<2>
FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_WDQS<3>
FB_A_WDQS<2>
FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A_DQM_L<3>
FB_A_DQM_L<2>
FB_A_DQM_L<0>
FB_A_DQM_L<1>
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FB_A_DQ<33>
FB_A_DQ<35>
FB_A0_VREF_UNTERM_L
FB_A2_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
FB_A3_VREF_UNTERM_L
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
GDDR3 Frame Buffer A (Bottom)
SYNC_MASTER=M98_MLB
SYNC_DATE=04/01/2008
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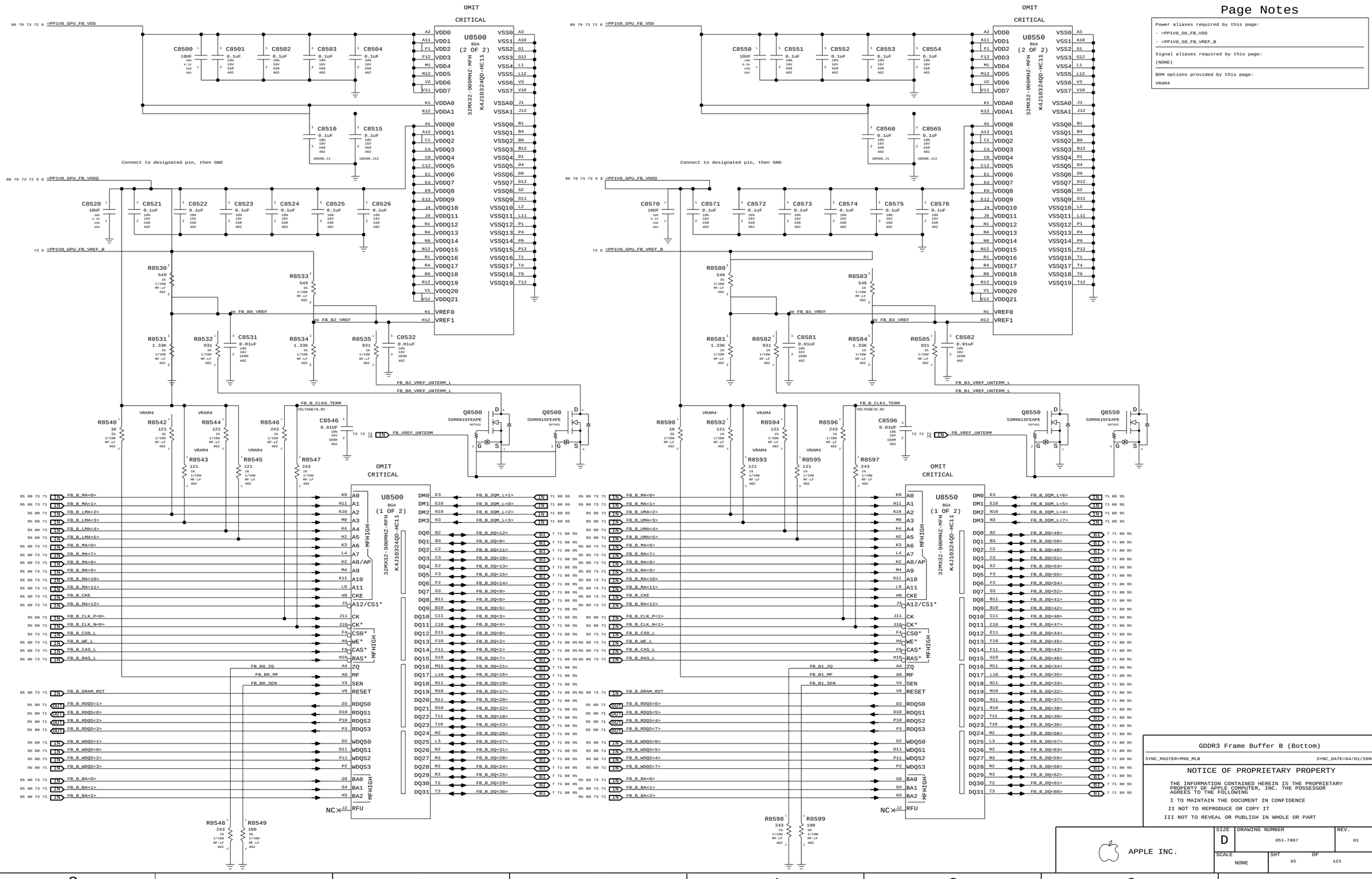
SIZE
D
DRAWING NUMBER
051-7867
REV.
01
SCALE
NONE
SHT
84
OF
123



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

GDDR3 Frame Buffer B (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 85 OF 123	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
75 74 8 6 =PP3V3_GPU_VDD33

C8690 0.022UF 10% 16V CERM-XSR 402
C8692 0.022UF 10% 16V CERM-XSR 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-XSR 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-XSR 402
C8693 0.022UF 10% 16V CERM-XSR 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-XSR 402

75 74 8 6 =PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-XSR 402
C8601 0.47UF 10% 6.3V CERM-XSR 402
C8602 0.47UF 10% 6.3V CERM-XSR 402

75 74 8 =PP3V3_GPU_MIO
75 74 8 =PP3V3_GPU_MIO
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ 74
GPU_MIOB_PD_VDDQ 74
GPU_MIOA_PU_GND 74
GPU_MIOB_PU_GND 74
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1uF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

8 =PP1V1_GPU_PLLVDD
L8630 FERR-220-OHM 0402
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

8 =PP1V1_GPU_H_PLLVDD
L8635 FERR-220-OHM 0402
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

8 =PP1V1_GPU_VID_PLLVDD
L8640 FERR-220-OHM 0402
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

J9	VDD33_1		
J10	VDD33_2		
J11	VDD33_3		
J12	VDD33_4		
J13	VDD33_5		
NC J25	RFU0		
NC J26	RFU1		
AK14	RFU0_GND		
K9	RFU1_GND		
C3	ROM_CS*	75 GPU_ROM_CS_L	
D4	ROM_SCLK	75 GPU_ROM_SCLK	
D3	ROM_SI	75 GPU_ROM_SI	
C4	ROM_SO	75 GPU_ROM_SO	
N9	STRAP_REF_3V3	GPU_STRAP_REF_3V3_PD	
M9	STRAP_REF_MIOB (IPD)	GPU_STRAP_REF_MIOB_PD	
P9	MIOA_VDDQ_1		
R9	MIOA_VDDQ_2		
T9	MIOA_VDDQ_3		
U9	MIOA_VDDQ_4		
AA9	MIOB_VDDQ_1		
AB9	MIOB_VDDQ_2		
W9	MIOB_VDDQ_3		
Y9	MIOB_VDDQ_4		
AP35	TESTMODE	GPU_TESTMODE_PD	
N5	MIOA_VREF	GPU_MIOA_VREF	
AF1	MIOB_VREF	GPU_MIOB_VREF	
U5	MIOA_CAL_PD_VDDQ	74 GPU_MIOA_PD_VDDQ	
T5	MIOA_CAL_PU_GND	74 GPU_MIOA_PU_GND	
AA7	MIOB_CAL_PD_VDDQ	74 GPU_MIOB_PD_VDDQ	
AA6	MIOB_CAL_PU_GND	74 GPU_MIOB_PU_GND	
AF9	SP_PLLVDD		
AE9	PLLVDD		
AD9	VID_PLLVDD		
B1	XTAL_IN	75 IN GPU_XTALIN	
B2	XTAL_OUT	75 OUT GPU_XTALOUT	
D1	XTAL_OUTBUFF	75 OUT GPU_XTALOUTBUFF	
D2	XTAL_SSIN	75 IN GPU_XTALSSIN	

K1	GPIO0	GPU_GPIO_0	B1 75
K2	GPIO1	GPU_GPIO_1	B1 75
K3	GPIO2	GPU_GPIO_2	B1 75
H3	GPIO3	GPU_GPIO_3	B1 75
H2	GPIO4	GPU_GPIO_4	B1 75
H1	GPIO5	GPU_GPIO_5	B1 75
H4	GPIO6	GPU_GPIO_6	B1 75
H5	GPIO7	GPU_GPIO_7	B1 75
H6	GPIO8	GPU_GPIO_8	B1 75
J7	GPIO9	GPU_GPIO_9	B1 75
K4	GPIO10	GPU_GPIO_10	B1 75
K5	GPIO11	GPU_GPIO_11	B1 75
H7	GPIO12	GPU_GPIO_12	B1 75
J4	GPIO13	GPU_GPIO_13	B1 75
J6	GPIO14	GPU_GPIO_14	B1 75
L1	GPIO15	GPU_GPIO_15	B1 75
L2	GPIO16	GPU_GPIO_16	B1 75
L4	GPIO17	GPU_GPIO_17	B1 75
M4	GPIO18	GPU_GPIO_18	B1 75
L7	GPIO19	GPU_GPIO_19	B1 75
L5	GPIO20	GPU_GPIO_20	B1 75
K6	GPIO21	GPU_GPIO_21	B1 75
L6	GPIO22	GPU_GPIO_22	B1 75
M6	GPIO23	GPU_GPIO_23	B1 75
C7	HDA_SDI	GPU_HDA_SDI	OUT 75
B7	HDA_SDO	GPU_HDA_SDO	OUT 75
A7	HDA_SYNC	GPU_HDA_SYNC	OUT 75
D7	HDA_BCLK	GPU_HDA_BCLK	OUT 75
D6	HDA_RST*	GPU_HDA_RST_L	OUT 75
A5	SPDIF	GPU_SPDIF	IN 75
A4	BUFRST*	TP_GPU_BUFRST_L	OUT 7
AP14	JTAG_TCK	GPU_JTAG_TCK	IN 6
AN14	JTAG_TDI	GPU_JTAG_TDI	IN 6
AN16	JTAG_TDO	GPU_JTAG_TDO	OUT 6
AR14	JTAG_TMS	GPU_JTAG_TMS	IN 6
AP16	JTAG_TRST*	GPU_JTAG_TRST_L	IN 6
N4	MIOA_CLKIN	GPU_MIOA_CLKIN	IN 75
R4	MIOA_CLKOUT	GPU_MIOA_CLKOUT_P	B1 75
T4	MIOA_CLKOUT*	GPU_MIOA_CLKOUT_N	B1 75
P5	MIOA_CTL3	GPU_MIOA_CTL3	B1 75
N2	MIOA_DE	GPU_MIOA_DE	B1 75
N1	MIOA_D0	GPU_MIOA_D<0>	B1 75
P4	MIOA_D1	GPU_MIOA_D<1>	B1 75
P1	MIOA_D2	GPU_MIOA_D<2>	B1 75
P2	MIOA_D3	GPU_MIOA_D<3>	B1 75
P3	MIOA_D4	GPU_MIOA_D<4>	B1 75
T3	MIOA_D5	GPU_MIOA_D<5>	B1 75
T2	MIOA_D6	GPU_MIOA_D<6>	B1 75
T1	MIOA_D7	GPU_MIOA_D<7>	B1 75
U4	MIOA_D8	GPU_MIOA_D<8>	B1 75
U1	MIOA_D9	GPU_MIOA_D<9>	B1 75
U2	MIOA_D10	GPU_MIOA_D<10>	B1 75
U3	MIOA_D11	GPU_MIOA_D<11>	B1 75
R6	MIOA_D12	GPU_MIOA_D<12>	B1 75
T6	MIOA_D13	GPU_MIOA_D<13>	B1 75
N6	MIOA_D14	GPU_MIOA_D<14>	B1 75
N3	MIOA_HSYNC	GPU_MIOA_HSYNC	B1 75
L3	MIOA_VSYNC	GPU_MIOA_VSYNC	B1 75
AE1	MIOB_CLKIN	GPU_MIOB_CLKIN	IN 75
V4	MIOB_CLKOUT	GPU_MIOB_CLKOUT_P	B1 75
W4	MIOB_CLKOUT*	GPU_MIOB_CLKOUT_N	B1 75
W3	MIOB_CTL3	GPU_MIOB_CTL3	B1 75
Y5	MIOB_DE	GPU_MIOB_DE	B1 75
Y1	MIOB_D0	GPU_MIOB_D<0>	B1 75
Y2	MIOB_D1	GPU_MIOB_D<1>	B1 75
Y3	MIOB_D2	GPU_MIOB_D<2>	B1 75
AB3	MIOB_D3	GPU_MIOB_D<3>	B1 75
AB2	MIOB_D4	GPU_MIOB_D<4>	B1 75
AB1	MIOB_D5	GPU_MIOB_D<5>	B1 75
AC4	MIOB_D6	GPU_MIOB_D<6>	B1 75
AC1	MIOB_D7	GPU_MIOB_D<7>	B1 75
AC2	MIOB_D8	GPU_MIOB_D<8>	B1 75
AC3	MIOB_D9	GPU_MIOB_D<9>	B1 75
AE3	MIOB_D10	GPU_MIOB_D<10>	B1 75
AE2	MIOB_D11	GPU_MIOB_D<11>	B1 75
U6	MIOB_D12	GPU_MIOB_D<12>	B1 75
W6	MIOB_D13	GPU_MIOB_D<13>	B1 75
Y6	MIOB_D14	GPU_MIOB_D<14>	B1 75
W5	MIOB_D15	GPU_STRAP<0>	B1 75
W7	MIOB_D16	GPU_STRAP<1>	B1 75
V7	MIOB_D17	GPU_STRAP<2>	B1 75
W1	MIOB_HSYNC	GPU_MIOB_HSYNC	B1 75
W2	MIOB_VSYNC	GPU_MIOB_VSYNC	B1 75
B5	THERMDP	GPU_THERMD_P	IN 75
B4	THERMDN	GPU_THERMD_N	OUT 75
C5	PGOOD_OUT*	TP_GPU_PGOOD_OUT_L	OUT 7

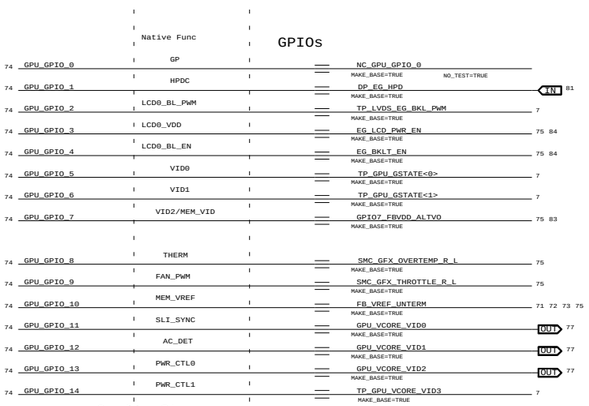
NV G96 GPIO/MIO/MISC

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

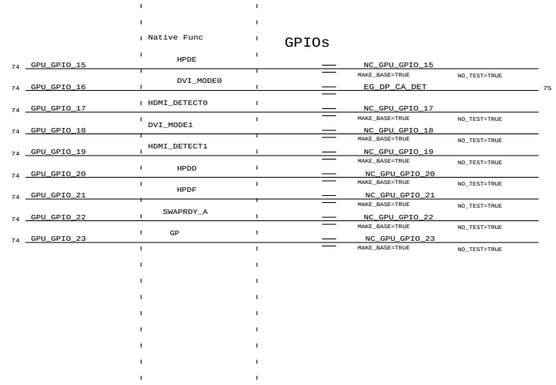
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 86 OF 123	

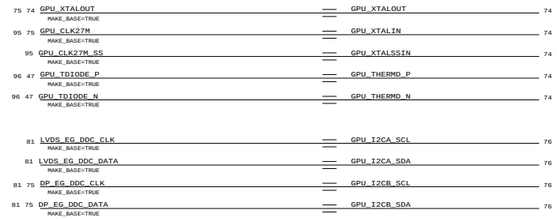
GPIOs



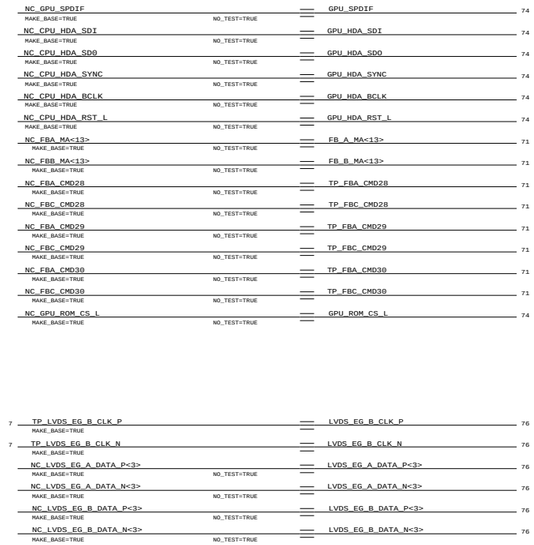
GPIOs



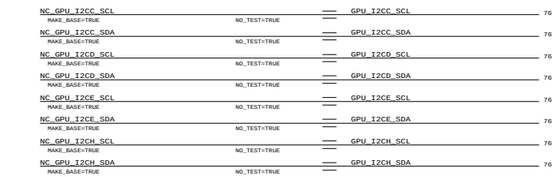
Renamed signals



Unused signals

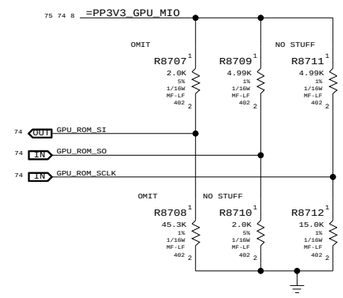


Unused I2C Buses



I2C5 ties into SMBus connection page
(I2C5 requires pullups even if not used)

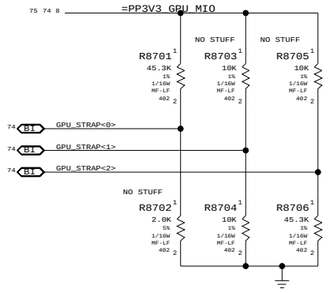
Config Straps



Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

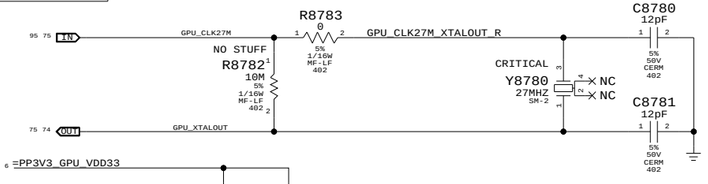
Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

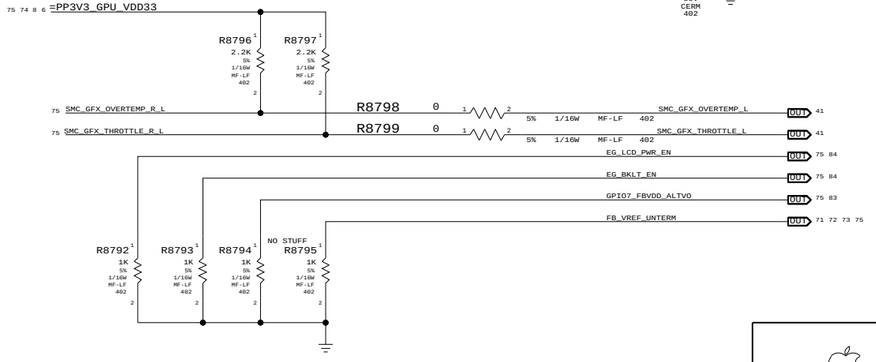
Strap S1/S2 Bit[3:0] PU/PD Rval
8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k



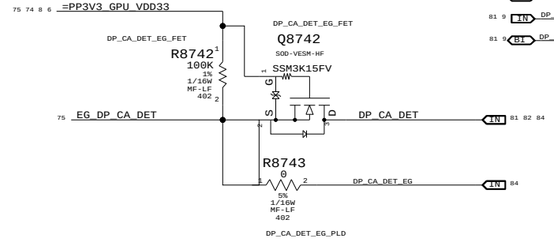
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL F1LM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES,MTL F1LM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL F1LM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL F1LM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL F1LM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL F1LM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

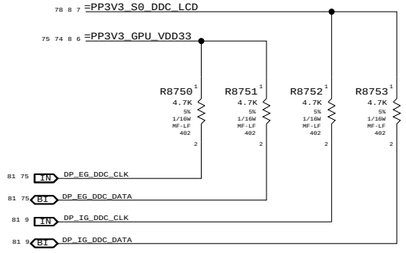
GPU 27MHz Crystal



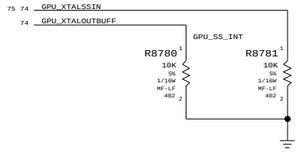


Isolation FETs for DP MUX inputs

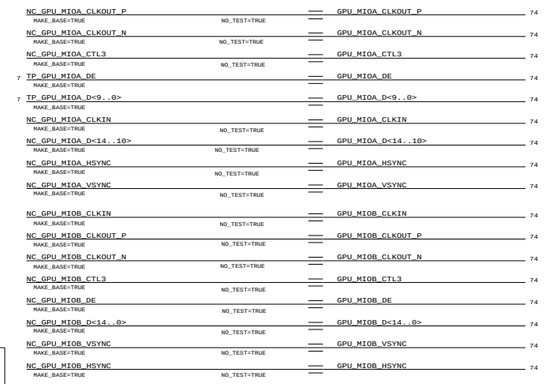




Unused Clocks



G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.



G96 GPIOs & Straps

SYNC_MASTER=M98_MLB
SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 87 OF 123	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10
PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 76
GPU_IFPCD_RSET 76
GPU_IFPAB_RSET 76
R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

L8810 FERR-220-OHM 0402
=PP1V1_GPU_IFPCD_IOVDD
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V
I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 76
PP1V8_GPU_IFPEF_PLLVDD_F 76
Power inputs must be pulled down if not used
R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD
R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
		IFPC_AUX	AP2
		IFPC_AUX*	AN3
		IFPC_L0	AM7
		IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
		IFPD_AUX	AP2 NC
		IFPD_AUX*	AN3 NC
		IFPD_L0	AR8 NC
		IFPD_L0*	AR7 NC
		IFPD_L1	AK7 NC
		IFPD_L1*	AK8 NC
		IFPD_L2	AN6 NC
		IFPD_L2*	AP5 NC
		IFPD_L3	AR5 NC
		IFPD_L3*	AR4 NC
		IFPE_AUX	AE4 NC
		IFPE_AUX*	AD4 NC
		IFPE_L0	AH6 NC
		IFPE_L0*	AH5 NC
		IFPE_L1	AH4 NC
		IFPE_L1*	AG4 NC
		IFPE_L2	AE4 NC
		IFPE_L2*	AE5 NC
		IFPE_L3	AE6 NC
		IFPE_L3*	AE5 NC
		IFPF_AUX	AF3 NC
		IFPF_AUX*	AE3 NC
		IFPF_L0	AL2 NC
		IFPF_L0*	AL3 NC
		IFPF_L1	AJ3 NC
		IFPF_L1*	AJ2 NC
		IFPF_L2	AJ1 NC
		IFPF_L2*	AK1 NC
		IFPF_L3	AK2 NC
		IFPF_L3*	AH3 NC
AJ12	DACA_VDD	DACA_RED	AM15 NC
		DACA_GREEN	AM14 NC
		DACA_BLUE	AL13 NC
AK12 NC	DACA_VREF	DACA_HSYNC	AM13 NC
AK13 NC	DACA_RSET	DACA_VSYNC	AL12 NC
AC6	DACB_VDD	DACB_RED	AA4 NC
		DACB_GREEN	AB4 NC
		DACB_BLUE	Y4 NC
AC5 NC	DACB_VREF	DACB_CSYNC	AB5 NC
AB6 NC	DACB_RSET		
AG7	DACC_VDD	DACC_RED	AK4 NC
		DACC_GREEN	AL4 NC
		DACC_BLUE	AJ4 NC
AK6 NC	DACC_VREF	DACC_HSYNC	AM1 NC
AH7 NC	DACC_RSET	DACC_VSYNC	AK3 NC

GPU_I2CA_SCL	B1	G1	I2CA_SCL
GPU_I2CA_SDA	B1	G4	I2CA_SDA
GPU_I2CC_SCL	B1	E3	I2CC_SCL
GPU_I2CC_SDA	B1	E4	I2CC_SDA
=GPU_I2CS_SCL	B1	E2	I2CS_SCL
=GPU_I2CS_SDA	B1	E1	I2CS_SDA
GPU_I2CH_SCL	B1	F6	I2CH_SCL
GPU_I2CH_SDA	B1	G6	I2CH_SDA
GPU_I2CB_SCL	B1	G3	I2CB_SCL
GPU_I2CB_SDA	B1	G2	I2CB_SDA
GPU_I2CD_SCL	B1	F4	I2CD_SCL
GPU_I2CD_SDA	B1	G5	I2CD_SDA
GPU_I2CE_SCL	B1	D5	I2CE_SCL
GPU_I2CE_SDA	B1	E5	I2CE_SDA

LVDS_EG_A_CLK_P OUT 84 95
LVDS_EG_A_CLK_N OUT 84 95
LVDS_EG_A_DATA_P<0> OUT 84 95
LVDS_EG_A_DATA_N<0> OUT 84 95
LVDS_EG_A_DATA_P<1> OUT 84 95
LVDS_EG_A_DATA_N<1> OUT 84 95
LVDS_EG_A_DATA_P<2> OUT 84 95
LVDS_EG_A_DATA_N<2> OUT 84 95
LVDS_EG_A_DATA_P<3> OUT 75
LVDS_EG_A_DATA_N<3> OUT 75
LVDS_EG_B_CLK_P OUT 75
LVDS_EG_B_CLK_N OUT 75
LVDS_EG_B_DATA_P<0> OUT 84 95
LVDS_EG_B_DATA_N<0> OUT 84 95
LVDS_EG_B_DATA_P<1> OUT 84 95
LVDS_EG_B_DATA_N<1> OUT 84 95
LVDS_EG_B_DATA_P<2> OUT 84 95
LVDS_EG_B_DATA_N<2> OUT 84 95
LVDS_EG_B_DATA_P<3> OUT 75
LVDS_EG_B_DATA_N<3> OUT 75
DP_EG_AUX_CH_P OUT 81 95
DP_EG_AUX_CH_N OUT 81 95
DP_EG_ML_P<0> OUT 81 95
DP_EG_ML_N<0> OUT 81 95
DP_EG_ML_P<1> OUT 81 95
DP_EG_ML_N<1> OUT 81 95
DP_EG_ML_P<2> OUT 81 95
DP_EG_ML_N<2> OUT 81 95
DP_EG_ML_P<3> OUT 81 95
DP_EG_ML_N<3> OUT 81 95

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402 NO STUFF

NV G96 Video Interfaces

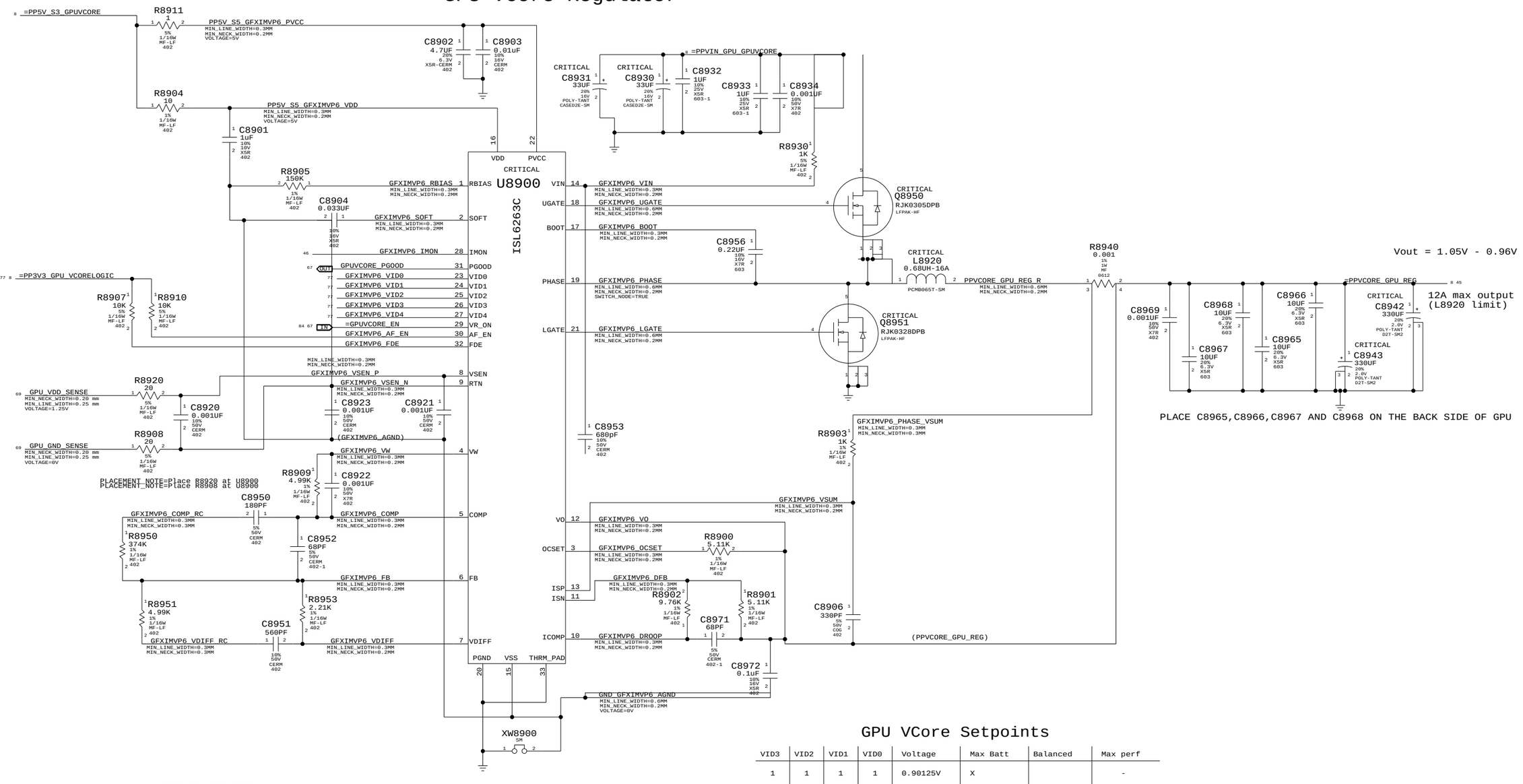
SYNC_MASTER=M99_MLB SYNC_DATE=11/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE NONE SHT 88 OF 123

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G96) CORE SUPPLY

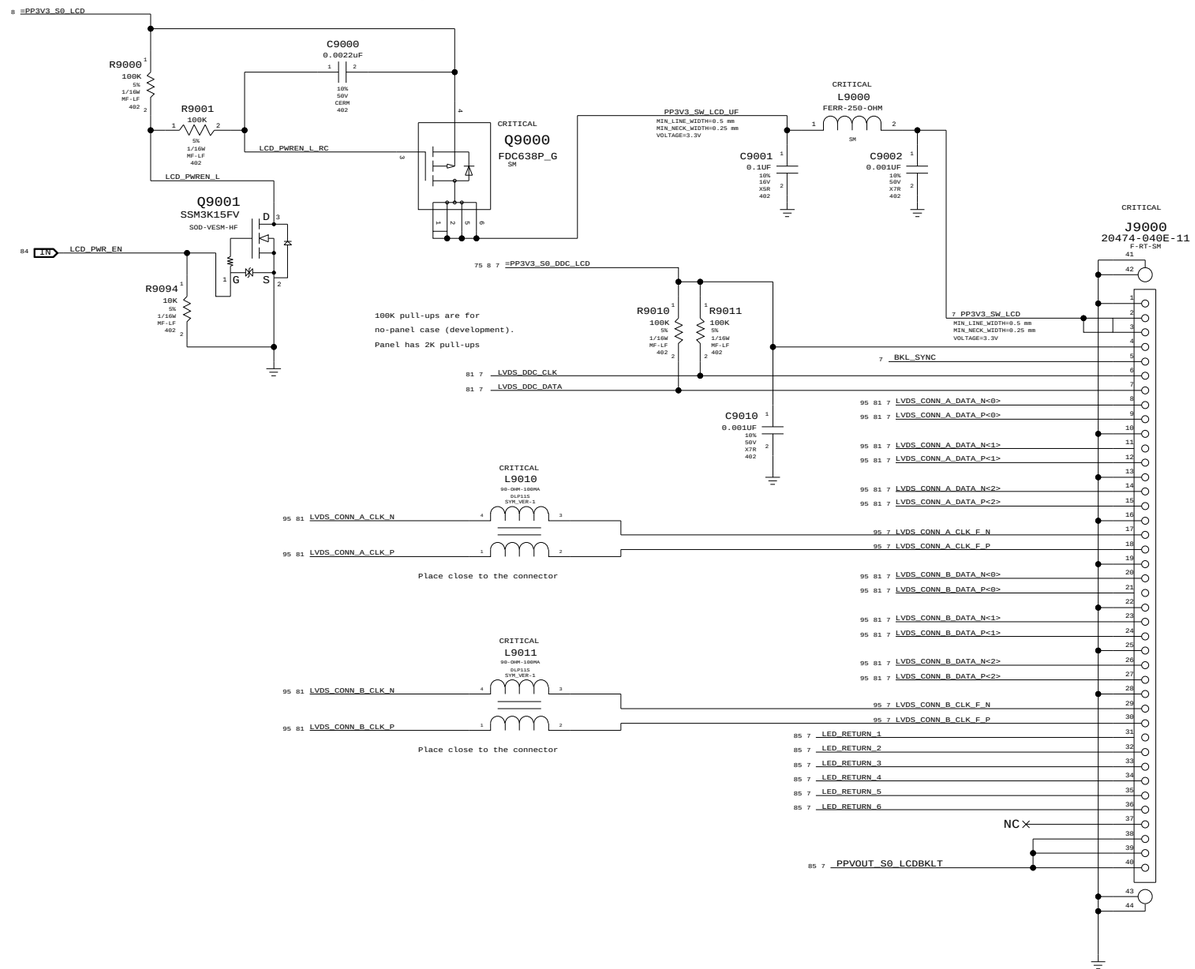
SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	89	123

LCD (LVDS) INTERFACE



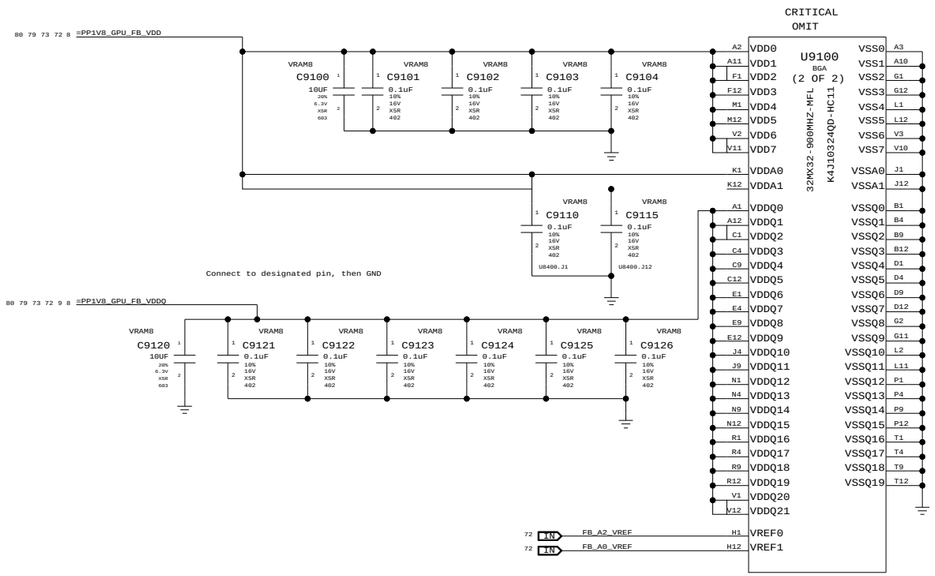
518S0651

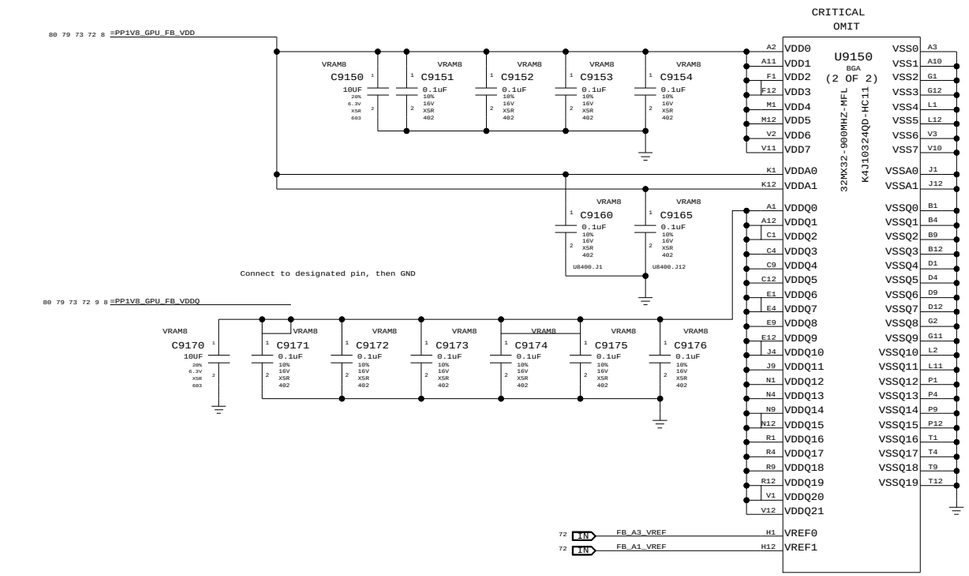
LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE	SHT	OF
NONE	90	123





Page Notes

Power aliases required by this page:

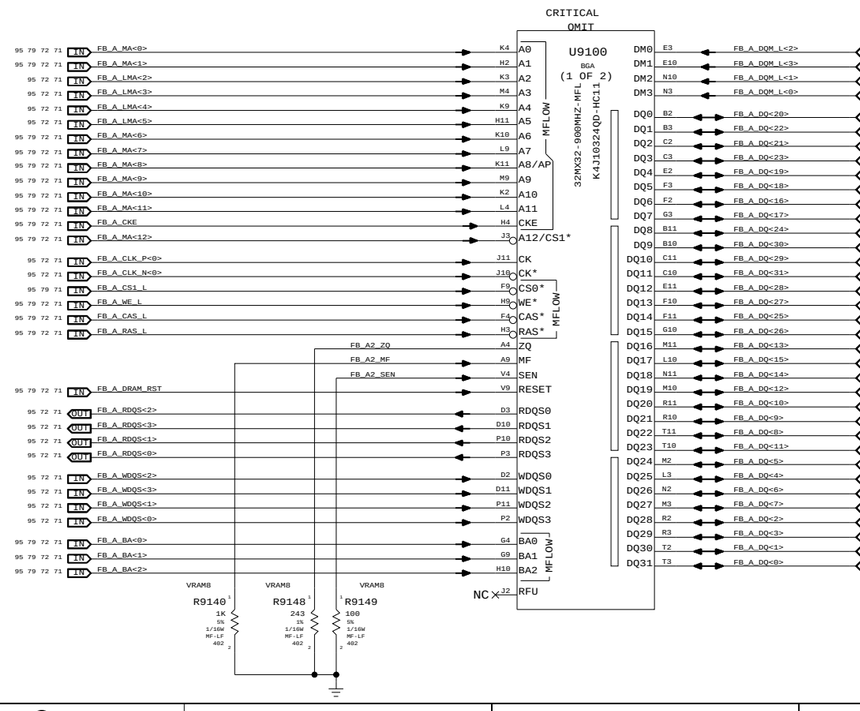
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

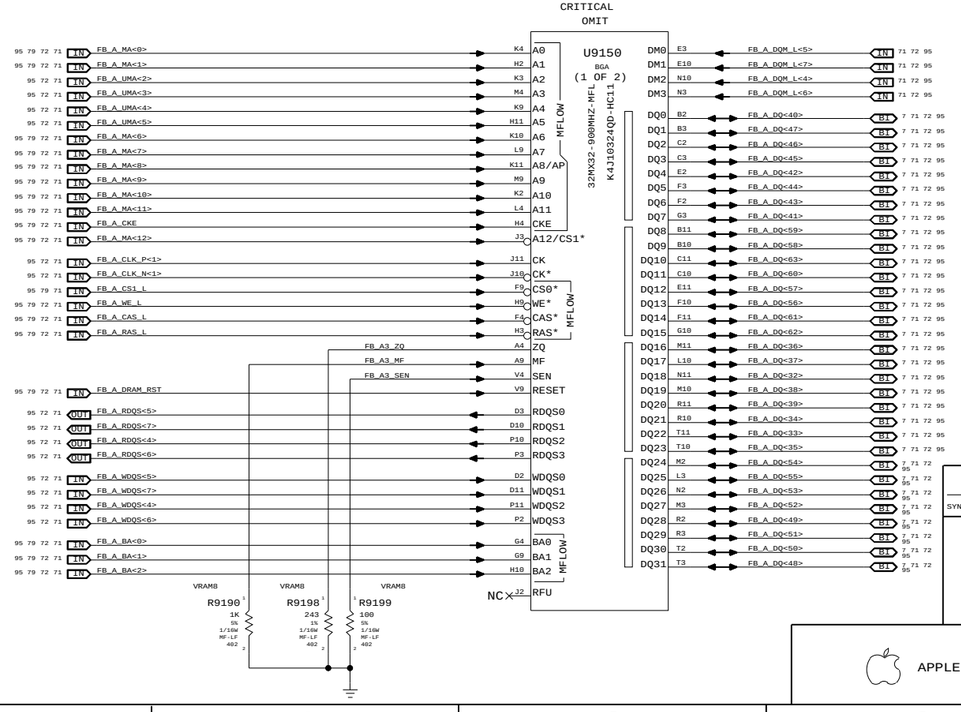
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8



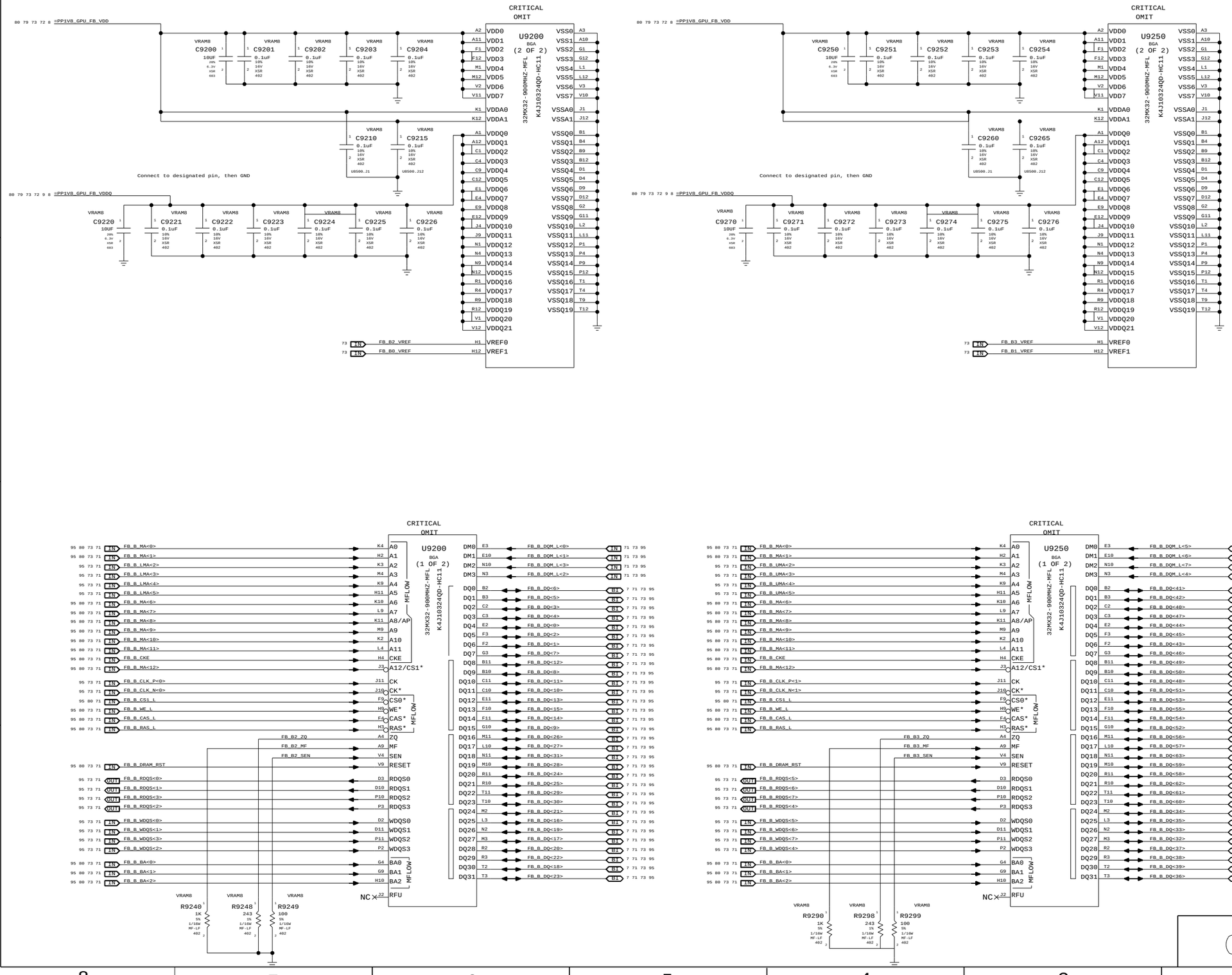


GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 91 OF 123	



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 92 OF 123	

LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9200 (All 24 resistors)

LVDS_A_CLK_P	R9320 270 1% 1/16W MF-LF 402	LVDS_CONN_A_CLK_P	R9321 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_A_CLK_N	R9322 270 1% 1/16W MF-LF 402	LVDS_CONN_A_CLK_N		
LVDS_A_DATA_P<0>	R9325 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_P<0>	R9326 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_A_DATA_N<0>	R9327 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_N<0>		
LVDS_A_DATA_P<1>	R9330 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_P<1>	R9331 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_A_DATA_N<1>	R9332 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_N<1>		
LVDS_A_DATA_P<2>	R9335 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_P<2>	R9336 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_A_DATA_N<2>	R9337 270 1% 1/16W MF-LF 402	LVDS_CONN_A_DATA_N<2>		
LVDS_B_CLK_P	R9340 270 1% 1/16W MF-LF 402	LVDS_CONN_B_CLK_P	R9341 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_B_CLK_N	R9342 270 1% 1/16W MF-LF 402	LVDS_CONN_B_CLK_N		
LVDS_B_DATA_P<0>	R9345 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_P<0>	R9346 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_B_DATA_N<0>	R9347 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_N<0>		
LVDS_B_DATA_P<1>	R9350 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_P<1>	R9351 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_B_DATA_N<1>	R9352 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_N<1>		
LVDS_B_DATA_P<2>	R9355 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_P<2>	R9356 133 1% 1/16W MF-LF 402	SIGNAL_MODEL=EMPTY
LVDS_B_DATA_N<2>	R9357 270 1% 1/16W MF-LF 402	LVDS_CONN_B_DATA_N<2>		

DisplayPort Mux

=PP3V3_S0_DPMUX

MUXGFX C9320 0.1UF 20% 10V CERM 402

MUXGFX C9321 0.1UF 20% 10V CERM 402

MUXGFX U9320 CBTL06141EE BGA CRITICAL SIGNAL_MODEL=DPMUX

VDD

DP_IG_ML_P<0>	DIN1_0+	DOUT_0+	DP_ML_P<0>
DP_IG_ML_N<0>	DIN1_0-	DOUT_0-	DP_ML_N<0>
DP_IG_ML_P<1>	DIN1_1+	DOUT_1+	DP_ML_P<1>
DP_IG_ML_N<1>	DIN1_1-	DOUT_1-	DP_ML_N<1>
DP_IG_ML_P<2>	DIN1_2+	DOUT_2+	DP_ML_P<2>
DP_IG_ML_N<2>	DIN1_2-	DOUT_2-	DP_ML_N<2>
DP_IG_ML_P<3>	DIN1_3+	DOUT_3+	DP_ML_P<3>
DP_IG_ML_N<3>	DIN1_3-	DOUT_3-	DP_ML_N<3>
DP_IG_AUX_CH_P	DAUX1+	AUX+	DP_AUX_CH_C_P
DP_IG_AUX_CH_N	DAUX1-	AUX-	DP_AUX_CH_C_N
DP_IG_DDC_CLK	DDC_CLK1		
DP_IG_DDC_DATA	DDC_DAT1		
	HPD_1		
DP_EG_ML_P<0>	DIN2_0+		
DP_EG_ML_N<0>	DIN2_0-		
DP_EG_ML_P<1>	DIN2_1+		
DP_EG_ML_N<1>	DIN2_1-		
DP_EG_ML_P<2>	DIN2_2+		
DP_EG_ML_N<2>	DIN2_2-		
DP_EG_ML_P<3>	DIN2_3+		
DP_EG_ML_N<3>	DIN2_3-		
DP_EG_AUX_CH_P	DAUX2+		
DP_EG_AUX_CH_N	DAUX2-		
DP_EG_DDC_CLK	DDC_CLK2		
DP_EG_DDC_DATA	DDC_DAT2		
	HPD_2		
DP_MUX_SEL_EG	GPU_SEL	DDC_AUX_SEL	DP_CA_DET
DP_MUX_XSD_L	XSD*	TST0	

C9330 0.1uF 10% 16V X5R 402 — DP_IG_AUX_CH_C_P

C9331 0.1uF 10% 16V X5R 402 — DP_IG_AUX_CH_C_N

C9335 0.1uF 10% 16V X5R 402 — DP_EG_AUX_CH_C_P

C9336 0.1uF 10% 16V X5R 402 — DP_EG_AUX_CH_C_N

R9306 1K 5% 1/16W MF-LF 402 — DP_IG_AUX_CH_N

R9304 100K 5% 1/16W MF-LF 402 — DP_IG_HPD

R9305 100K 5% 1/16W MF-LF 402 — DP_EG_HPD

R9301 10K 5% 1/16W MF-LF 402 — DPMUX_EN_HPD

C9301 1UF 10% 6.3V CERM-XSR 402 — DPMUX_EN_HPD

GND

=PP3V3_S0_DPMUX

DPMUX_EN_S0&DPMUX_EN_PLD

R9302 10K 1% 1/16W MF-LF 402

DPMUX_EN_PLD

R9303 0 5% 1/16W MF-LF 402 — DP_MUX_EN

DP_HOTPLUG_DET MAKE_BASE=TRUE

DP_IG_CA_DET

LO=PORT1 HI=PORT2

LO=AUX_CH HI=DDC

PLACEMENT_NOTE=Place at U9320

MUXGFX R9307 1K 5% 1/16W MF-LF 402 — HPDIN — DP_HPD_R — DP_HPD

DP_CA_DET MAKE_BASE=TRUE

LVDS DDC MUX

=PP3V3_GPU_LVDS_DDC

=PP3V3_S0_LVDSDDCMUX

R9370 20K 5% 1/16W MF-LF 402

R9371 20K 5% 1/16W MF-LF 402

C9370 0.1UF 20% 10V CERM 402

R9372 20K 5% 1/16W MF-LF 402

R9373 20K 5% 1/16W MF-LF 402

VCC U9370 QFN1 SN74LV4066A GND THRM

LVDS_DDC_SEL_EG	C1	A1	LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	C2	A2	LVDS_IG_DDC_CLK
		B2	LVDS_DDC_CLK
	C3	A3	LVDS_EG_DDC_DATA
		B3	
	C4	A4	LVDS_IG_DDC_DATA
		B4	LVDS_DDC_DATA

Muxed Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	93	123

Port Power Switch

=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
U9480 TPS2051B SOT23 (IN, EN, GND, OC*, OUT)
TP_DPPWR_OC_L
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
C9486 22UF 20% 6.3V X5R-CERM 603
R9420 100K 5% 1/16W MF-LF 402
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V

HDMI_CEC
R9425 1M 5% 1/16W MF-LF 402
DP_ML_P<3> C9414 0.1uF DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N
R9403 0 NO STUFF
R9413 0 NO STUFF
FL9403 12-OHM-100MA TCM1210-4SM
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

R9421 100K 5% 1/16W MF-LF 402

CRITICAL
J9400 DSPLYPRT-M97-2 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
		GND	1
DP_HPD	2	GND	3
DP_C_A_DET	4	ML_LANE0P	5
HDMI_CEC	6	ML_LANE0N	7
GND	8	GND	9
ML_LANE3P	10	ML_LANE1P	11
ML_LANE3N	12	ML_LANE1N	13
GND	14	GND	15
AUX_CHP	16	ML_LANE2P	17
AUX_CHN	18	ML_LANE2N	19
DP_PWR	20	RETURN	

SHIELD PINS

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

R9401 0 NO STUFF
R9431 0 NO STUFF
R9400 0 NO STUFF
R9430 0 NO STUFF
R9402 0 NO STUFF
R9432 0 NO STUFF

FL9401 12-OHM-100MA TCM1210-4SM
FL9400 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM

DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

DP_ML_C_P<0> C9410 0.1uF DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF DP_ML_N<2>

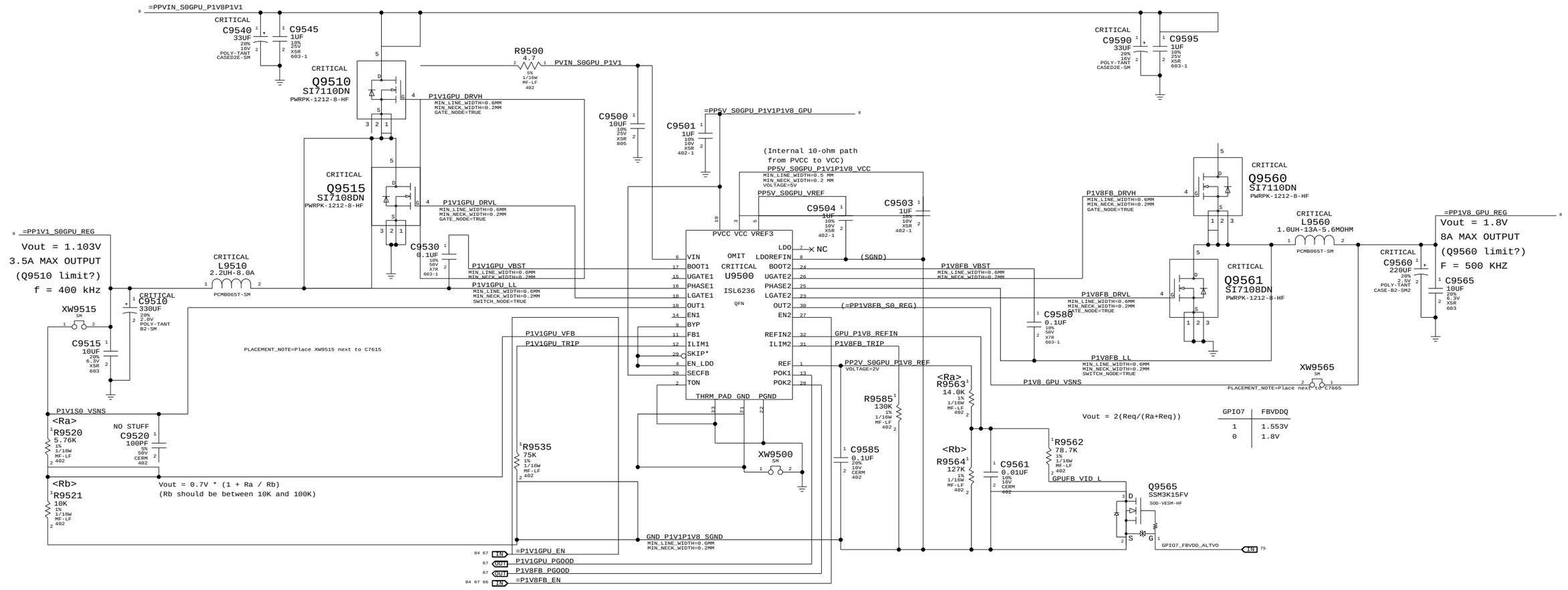
=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector

SYNC_MASTER=M98_MLB
SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 94 OF 123	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE NONE SHT 95 OF 123

GMUX CPLD

=PP3V3_S0_GMUX
C9610 0.1UF 20% 10V CERM 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9627 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402

=PP2V5_S0_GMUX
C9611 0.1UF 20% 10V CERM 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

=PP1V2_S0_GMUX
C9600 4.7UF 20% 4V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

=PP3V3_S0_GMUX
R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402
NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402
NO STUFF R9647 10K 1% 1/16W MF-LF 402

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9621 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9620 FERR-220-OHM 0402
C9630 0.1UF 20% 10V CERM 402

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO0 B5
VCCIO1 B7
VCCIO2 A12
VCCIO3 C14
VCCIO4 F13
VCCIO5 M12
VCCIO6 M9
VCCIO7 M3
VCCJ N5
ULC_VCCPLL M1
LRC_VCCPLL C3
F2
K12
A4
P11

OMIT
CRITICAL
U9600
XP28
CSBGA-HF

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	IN
JTAG_GMUX_TDO	K13	TDO	OUT
JTAG_GMUX_TMS	L12	TMS	IN
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB2A	OUT
LCD_BKLT_PWM	N2	PB2B	OUT
LVDS_DDC_SEL_EG	P4	PB14A	OUT
LVDS_DDC_SEL_IG	N4	PB14B	OUT
DP_MUX_EN	N3	PB15A (do)	OUT
DP_MUX_SEL_EG	M4	PB15B	OUT
EG_RESET_L	P5	PB16A	OUT
EG_RAIL1_EN	M5	PB16B	OUT
EG_RAIL2_EN	P6	PB17A	OUT
EG_RAIL3_EN	M6	PB17B	OUT
EG_RAIL4_EN	P7	PB18A	OUT
EG_CLKREQ_OUT_L	M7	PB18B (do)	OUT
DP_CA_DET_EG	N7	PB19A	OUT
LCD_PWR_EN	N8	PB19B	OUT
LPC_AD<0>	P9	PB20A	BI
LPC_AD<1>	N9	PB20B	BI
LPC_AD<2>	P10	PB30A	BI
LPC_AD<3>	M10	PB30B	BI
LPC_FRAME_L	P12	PB31A	BI
LPC_RESET_L	P13	PB31B	BI
LPC_CLK33M_GMUX	N12	PB32A	IN
GMUX_INT	P14	PB32B	OUT
LVDS_IG_B_DATA_P<2>	B1	PL2A	IN
LVDS_IG_B_DATA_N<2>	B2	PL2B	IN
TP_GMUX_PL10A	C2	PL10A	
TP_GMUX_PL10B	D3	PL10B	
LVDS_IG_A_DATA_P<0>	D1	PL11A	IN
LVDS_IG_A_DATA_N<0>	E1	PL11B	IN
LVDS_IG_A_DATA_P<1>	D2	PL12A	IN
LVDS_IG_A_DATA_N<1>	E3	PL12B	IN
LVDS_IG_A_DATA_P<2>	F1	PL13A	IN
LVDS_IG_A_DATA_N<2>	G1	PL13B	IN
LVDS_IG_B_DATA_P<0>	F3	PL14A	IN
LVDS_IG_B_DATA_N<0>	G2	PL14B	IN
LVDS_IG_B_DATA_P<1>	H2	PL15A	IN
LVDS_IG_B_DATA_N<1>	G3	PL15B	IN
LVDS_IG_A_CLK_P	H1	PL16A	IN
LVDS_IG_A_CLK_N	H3	PL16B	IN
LVDS_MUX_SEL_EG	L1	PL18A	OUT
TP_GMUX_PL18B_VSYNC	L3	PL18B	
=GMUX_PCIE_RESET_L	K3	PL19A	IN
GMUX_PM_SLP_S3_L	L2	PL19B	IN
ALL_EG_PGOOD	N1	PL32A	IN
EG_CLKREQ_IN_L	P1	PL32B	IN

BANK5 BANK4 BANK7 BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1 B8 C6 F12 G13 E13 M14 N10 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PT2A	A2	LVDS_B_DATA_P<0>	OUT
PT2B	A3	LVDS_B_DATA_N<0>	OUT
PT3A	A1	LVDS_B_DATA_P<1>	OUT
PT3B	B3	LVDS_B_DATA_N<1>	OUT
PT4A	C5	LVDS_B_DATA_P<2>	OUT
PT4B	A5	LVDS_B_DATA_N<2>	OUT
PT14A	B6	EG_PWRSEQ_EN	IN
PT14B	C7	GMUX_DEBUG_RESET_L	IN
PT15A	A6	LVDS_A_CLK_P	OUT
PT15B	A7	LVDS_A_CLK_N	OUT
PT16A	C8	LVDS_B_CLK_P	OUT
PT16B	C9	LVDS_B_CLK_N	OUT
PT17A	A8	LVDS_A_DATA_P<0>	OUT
PT17B	B9	LVDS_A_DATA_N<0>	OUT
PT18A	A9	LVDS_A_DATA_P<1>	OUT
PT18B	C10	LVDS_A_DATA_N<1>	OUT
PT19A	B10	LVDS_A_DATA_P<2>	OUT
PT19B	A10	LVDS_A_DATA_N<2>	OUT
PT20A	A11	TP_GMUX_PT20A	
PT20B	B12	TP_GMUX_PT20B	
PT32A	B13	TP_GMUX_PT32A	
PT32B	A13	TP_GMUX_PT32B	
PR2A	A14	DP_CA_DET	IN
PR2B	B14	DP_HOTPLUG_DET	IN
PR10A	D12	LVDS_EG_A_DATA_P<0>	IN
PR10B	D13	LVDS_EG_A_DATA_N<0>	IN
PR11A	D14	LVDS_EG_A_DATA_P<1>	IN
PR11B	E14	LVDS_EG_A_DATA_N<1>	IN
PR12A	E12	LVDS_EG_A_DATA_P<2>	IN
PR12B	F12	LVDS_EG_A_DATA_N<2>	IN
PR13A	F14	LVDS_EG_B_DATA_P<0>	IN
PR13B	G14	LVDS_EG_B_DATA_N<0>	IN
PR14A	G12	LVDS_EG_B_DATA_P<1>	IN
PR14B	G13	LVDS_EG_B_DATA_N<1>	IN
PR15A	H13	LVDS_EG_B_DATA_P<2>	IN
PR15B	H12	LVDS_EG_B_DATA_N<2>	IN
PR16A	H14	LVDS_EG_A_CLK_P	IN
PR16B	J12	LVDS_EG_A_CLK_N	IN
PR18A	L14	IG_LCD_PWR_EN	IN
PR18B	M13	EG_LCD_PWR_EN	IN
PR30A	N14	IG_BKLT_EN	IN
PR30B	N13	EG_BKLT_EN	IN

BANK0 BANK1 BANK2 BANK3

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650	100		LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100		LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100		LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100		LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100		LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100		LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100		LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100		LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100		LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100		LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100		LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100		LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100		LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100		LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX
GMUX_DEBUG_RESET_L R9680 1K
JTAG_GMUX_TCK R9690 4.7K
EG_CLKREQ_OUT_L R9695 10K
All: 5% 1/16W MF-LF 402

NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K
LVDS_DDC_SEL_IG	R9682	10K
LVDS_DDC_SEL_EG	R9683	10K

All: 5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF
EG_RESET_L R9691 100K
GMUX_INT R9692 20K
LCD_BKLT_PWM R9693 100K
EG_CLKREQ_IN_L R9694 100K
All: 5% 1/16W MF-LF 402

EG_PWRSEQ_HW R9630 0
EG_PWRSEQ_GMUX R9631 0
EG_PWRSEQ_GMUX R9632 0
EG_PWRSEQ_GMUX R9633 0
EG_PWRSEQ_GMUX R9634 0
All: 5% 1/16W MF-LF 402

EG_RAIL1_EN → EXTGPU_PWR_EN OUT 67
EG_PWRSEQ_GMUX → =P1V1GPU_EN OUT 67 83
EG_RAIL2_EN → P3V3GPU_EN OUT 67 68
EG_PWRSEQ_GMUX → GPUVCORE_EN OUT 67 77
EG_RAIL3_EN
EG_PWRSEQ_GMUX → =P1V8FB_EN OUT 66 67 83
EG_RAIL4_EN

The MAKE BASE properties for these signals are on the POWER CONTROL page.

EG_PWRSEQ_GMUX R9671 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9672 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9673 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9674 4.7K 5% 1/16W MF-LF 402
NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

PM_SLP_S3_L Isolation

=PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
PM_SLP_S3_L (IN) → GMUX_PM_SLP_S3_L
MAKE_BASE=TRUE
EG_PWRSEQ_EN

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L

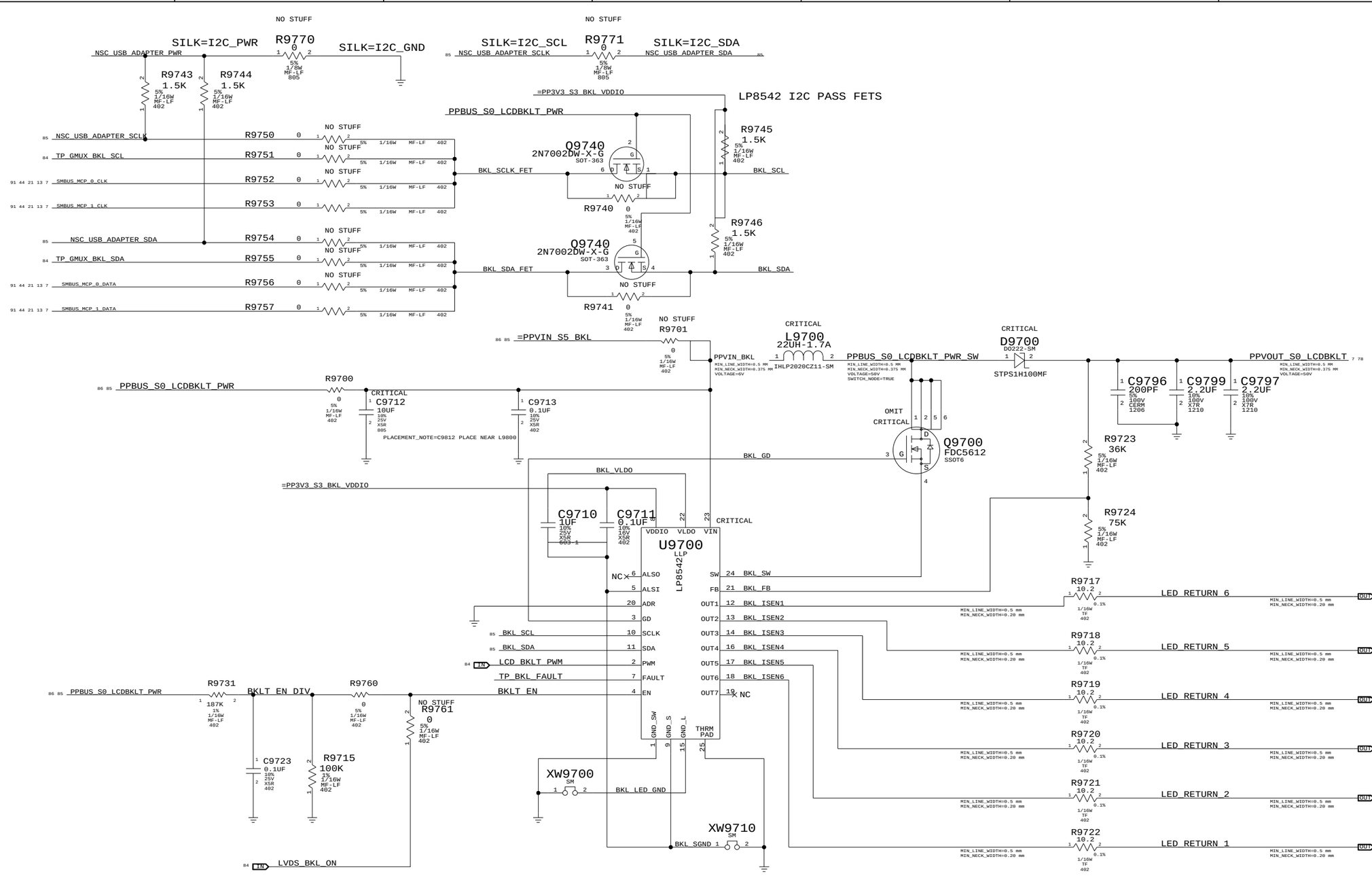
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2354	1	IC,CPLD,LATTICE,132CSBGA,K20	U9600	CRITICAL	GMUX_PROG

Graphics MUX (GMUX)

SYNC_MASTER=T18_MXMGMUX SYNC_DATE=02/13/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 96 OF 123	



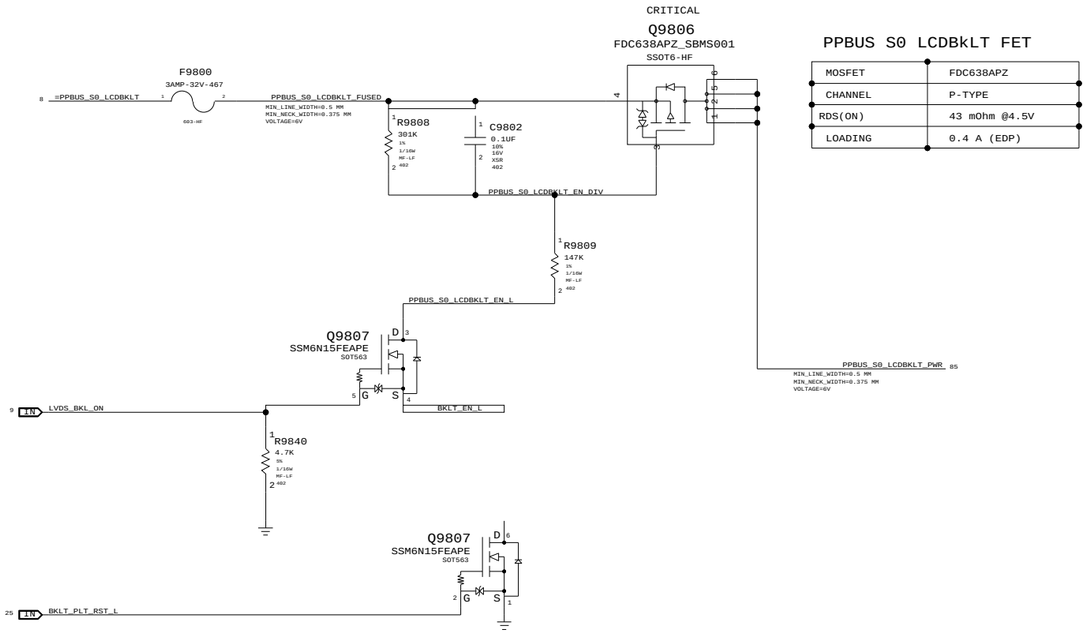
LCD BACKLIGHT DRIVER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0747	1	XSTR,FET,N-CH,60V,3.6A,0.128OHM,TSOP-6,L	Q9700	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=NA

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 97 OF 123	



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

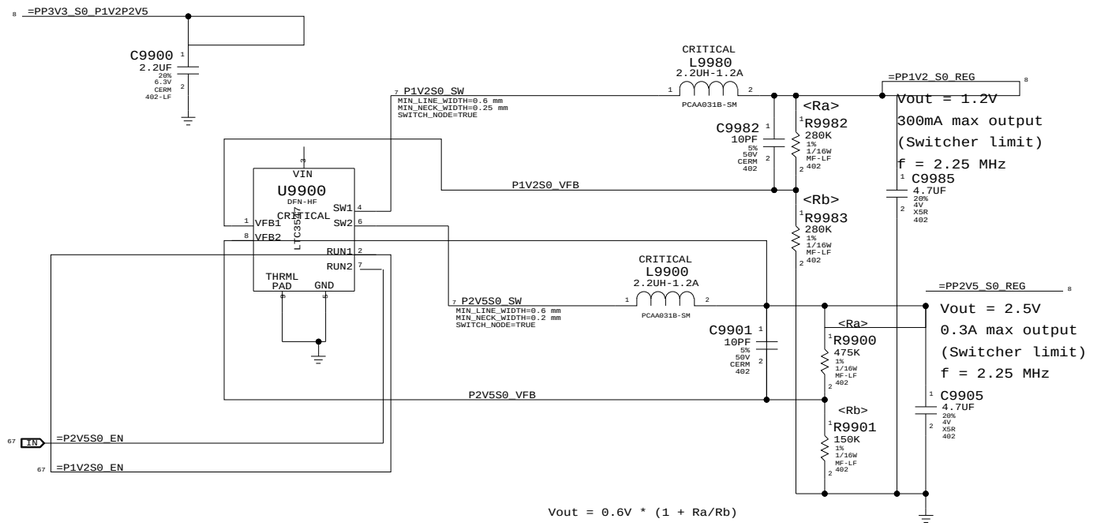
LCD Backlight Support

SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 98 OF 123	

2.5V/1.2V S0 Switcher



Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	99	123

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT: 100 OF: 123

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3		MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4		MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5		MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6		MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7		MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0		MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT: 101 OF 123

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	69
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 24
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D	SATA	SATA_HDD_R2D_N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 102 OF 123

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P 20 39
	USB_90D	USB	USB_EXTA_N 20 39
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 9 20
	USB_90D	USB	USB_MINI_N 9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 20
	USB_90D	USB	USB_EXTD_N 9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20 30
	USB_90D	USB	USB_CAMERA_N 20 30
USB_BT	USB_90D	USB	USB_BT_P 20 30
	USB_90D	USB	USB_BT_N 20 30
USB_TPAD	USB_90D	USB	USB_TPAD_P 20 49
	USB_90D	USB	USB_TPAD_N 20 49
USB_IR	USB_90D	USB	USB_IR_P 20 40
	USB_90D	USB	USB_IR_N 20 40
USB_EXTB	USB_90D	USB	USB_EXTB_P 20 39
	USB_90D	USB	USB_EXTB_N 20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 20 31
	USB_90D	USB	USB_EXCARD_N 20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P 20 96 98
	USB_90D	USB	USB_EXTC_N 20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 7 13 21 44 85
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 7 13 21 44 85
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 9 21
	HDA_55S	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21 53
	HDA_55S	HDA	HDA_SYNC_R 21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_RST_L 21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21 53
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21 53
	HDA_55S	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 25 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 21 43
	SPI_55S	SPI	SPI_CLK 52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 21 43
	SPI_55S	SPI	SPI_MOSI 52
SPI_MISO	SPI_55S	SPI	SPI_MISO 21 43
	SPI_55S	SPI	SPI_MISO_R 52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 21 43
	SPI_55S	SPI	SPI_CS0_L

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 103 OF 123

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE NONE SHT 104 OF 123

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 35 37
FW_P0_TPA_N 35 37
FW_P0_TPB_P 35 37
FW_P0_TPB_N 35 37
FW_P1_TPA_P 35 37
FW_P1_TPA_N 35 37
FW_P1_TPB_P 35 37
FW_P1_TPB_N 35 37

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	105	123

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
	1TO1_DIFFPAIR		CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
	1TO1_DIFFPAIR		CHGR_CSO_N	60

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE	SHT	OF
NONE	106	123

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R5SSE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	81 84
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	**DP_ML_P<3..0>**	81 82
	DP_100D	DISPLAYPORT	**DP_ML_N<3..0>**	81 82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_MA<12..6>	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_BA<2..0>	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_RAS_L	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_CAS_L	71 72 79
FB_AB_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_A_WE_L	71 72 79
FB_AB_CMD_FO	GDDR3_40R5SSE	GDDR3_CMD	FB_A_CKE	71 72 79
FB_AB_CS0	GDDR3_40R5SSE	GDDR3_CMD	FB_A_CS0_L	71 72
FB_AB_CMD_FO	GDDR3_40R5SSE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	71 72 79
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	71 72 79
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	71 72 79
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	71 72 79
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	71 72 79
	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
U200 FB_AB_CS1	GDDR3_40R5SSE	GDDR3_CMD	FB_A_CS1_L	71 79

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	75
CK505_CLK27MSS	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	75
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_P<3..0>**	76 81
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_N<3..0>**	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	76 81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_MA<12..6>	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_BA<2..0>	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_RAS_L	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_CAS_L	71 73 80
FB_CD_CMD	GDDR3_40R5SSE	GDDR3_CMD	FB_B_WE_L	71 73 80
FB_CD_CMD_FO	GDDR3_40R5SSE	GDDR3_CMD	FB_B_CKE	71 73 80
FB_CD_CS0	GDDR3_40R5SSE	GDDR3_CMD	FB_B_CS0_L	71 73
FB_CD_CMD_FO	GDDR3_40R5SSE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
U200 FB_CD_CS1	GDDR3_40R5SSE	GDDR3_CMD	FB_B_CS1_L	71 80

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

SCALE: NONE SHT 107 OF 123

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
U145	SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
U145	SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
U144	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
U142	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
U143	SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
U140	SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
U141	SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
U139	SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 47
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 47
GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 75
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
	SENSE_1TO1_55S	SENSE	GPUISENS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
	SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
		GND	GND	
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8 9 66 85
		SB_POWER	PP1V5_S0	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_WE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
U130	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
U131	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
U138	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
U136	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
U137	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
U135	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	39
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	39
(USB_EXTA)	USB_90D	USB	USB2_LT1_P	7 39
(USB_EXTA)	USB_90D	USB	USB2_LT1_N	7 39
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 30
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 30
	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
	USB_90D	USB	USB_LT2_P	7 39
	USB_90D	USB	USB_LT2_N	7 39
	USB_90D	USB	USB2_EXCARD_CONN_P	7 31
	USB_90D	USB	USB2_EXCARD_CONN_N	7 31
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
	PCIE_90D	PCIE	PCIE_FC_D2R_N	
	PCIE_90D	PCIE	PCIE_FC_R2D_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_N	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_C_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_C_OUT_N	7 56 57
	USB_90D	USB	USB_EXTC_P	20 91 98
	USB_90D	USB	USB_EXTC_N	20 91 98
	USB_90D	USB	USB_LT3_P	7 98
	USB_90D	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 108 OF 123	

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR		Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

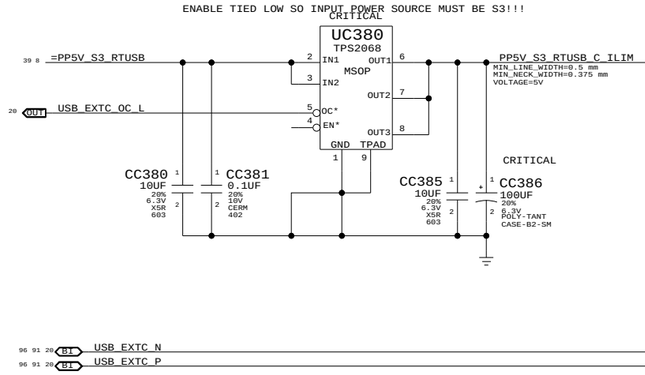
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01

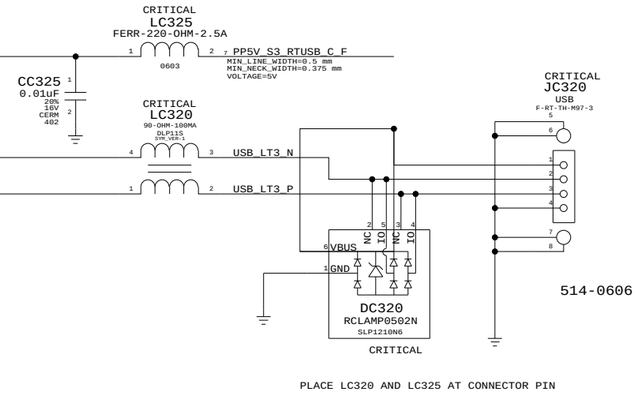
SCALE NONE SHT 109 OF 123

Port Power Switch

ENABLE TIED LOW SO INPUT POWER SOURCE MUST BE S3!!!



LEFT USB PORT C



PLACE LC320 AND LC325 AT CONNECTOR PIN

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7867	01
SCALE: NONE	SHT 123 OF 123	