1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
### K19 BOM Groups

<table>
<thead>
<tr>
<th>BOM NAME</th>
<th>BOM OPTIONS</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REF DES</th>
<th>CRITICAL</th>
<th>BOM OPTIONS</th>
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<tbody>
<tr>
<td>K19 MLB DEVELOPMENT</td>
<td>085-0736 K19 MLB DEVELOPMENT</td>
<td>630-9969 PCBA, 3.06GHZ, 512SAM_VRAM, HB_AUDIO, K19</td>
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<tr>
<td>K19 MLB DEVELOPMENT</td>
<td>085-0736 K19 MLB DEVELOPMENT</td>
<td>630-9968 PCBA, 2.80GHZ, 512HYN_VRAM, HB_AUDIO, K19</td>
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<tr>
<td>K19 MLB DEVELOPMENT</td>
<td>085-0736 K19 MLB DEVELOPMENT</td>
<td>630-9966 PCBA, 2.66GHZ, 256HYN_VRAM, HB_AUDIO, K19</td>
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</table>

### Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE ALT</th>
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<th>BOM OPTION</th>
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<tbody>
<tr>
<td>501-3635</td>
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<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
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<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
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### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
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<th>BOM OPTION</th>
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<tbody>
<tr>
<td>333S0506</td>
<td>1</td>
<td>IC, SGRAM, GDDR3, 16Mx32, 1000MHZ, 136 FBGA</td>
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<tr>
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<tr>
<td>337S3761</td>
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<td>CRITICAL U1000</td>
<td></td>
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<tr>
<td>338S0554</td>
<td>1</td>
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<tr>
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</table>

### Development BOM

<table>
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<th>REFERENCE ALT</th>
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<th>BOM OPTION</th>
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<tr>
<td>501-3635</td>
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<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
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<tr>
<td>501-3635</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
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</tr>
<tr>
<td>501-3635</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

If you have any further questions or need assistance, feel free to reach out. Thank you for considering our products.
Current numbers from Merom for Santa Rosa EMTS, doc #22221.

8 7 6 5 4 3 2 1
8 7 6 5 4 3 2 1

AB18
AB17
AB15
AB14
AB12
AB10
AA18
AA17
AA15
AA12
AA10

A18
AB9
F20
F18
F17
F15
F14
F12
F10

E18
E17
E15
E13
E12
E10
D15
D12
D10

C10
AA7
E20
D18
D17
C18
C15
C13
C12

B20
B18
B17
B15
B14
B12
B10
A20
A17
A15
A13
A12

F7
E9
E7
D9
C9
B9
B7
A9
A7

VCC
U1000
PENRYN
OMIT
VSSSENSE
VCCSENSE
VCCP
VID6
VID5
VID4
VID3
VID2
VID1

CPU Power & Ground

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CPU Power & Ground

SIZE
SCALE
DRAWING NUMBER
SHEET OF
REV.

APPLE INC.
CPU VCORE HF AND BULK DECOUPLING

- 1x 10uF, 1x 0.01uF

CPU VCORE HF AND BULK DECOUPLING

- 4x 330uF, 20x 22uF 0805

VCCP (CPU I/O) DECOUPLING

- 1x 470uF, 6x 0.1uF 0402

VCCA (CPU AVdd) DECOUPLING

- 6.3V20% X5R-CERM 22UF
- 2.5V20% D2T POLY 470UF

CRITICAL
- WF: Consider sharing bulk cap with NB Vtt?

VCCP (CPU I/O) DECOUPLING

- 6.3V20% X5R-CERM 22UF
- 2.0V20% D2T-SM2POLY-TANT 330UF

CRITICAL
- PLACEMENT_NOTE=Place in CPU center cavity.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XP-TS03 adapter board to support CPU XDP debugging.

MCP79-specific pinout

Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Minimum 1.025V for Gen2 support

8 7 6 5 4 3 2 1

OUT
IN

127 mA (A01, AVDD0 & 1)
84 mA (A01)
43 mA (A01, DVDD0 & 1)

402 MF-LF 1/16W 402 5%
8.2K MF-LF 1/16W 402 1%

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.
If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for results in earlier ROMSIP and MCP FSB I/O interface initialization.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections,
DDR3 RESET Support

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

- 3.3V is used because MEM_RESET must be high before 1.6V starts to rise to avoid glitch on MEM_RESET_L.
- 5% MF-LF 1/16W 100K
- 5% MF-LF 10K
- 20% CERM 0.1UF
- 5% MF-LF 12
- 5% MF-LF 1K
- 5% MF-LF 1K
- 5% MF-LF 16
- 5% MF-LF 1K
WLAN Enable Generation

**NOTE:** S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

---

**1.05V ENET FET**

---

**RTL8211 25MHz Clock**

**NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
Place one of 0.1uf cap close to each centertap pin of transformer

Transformers should be mirrored on opposite sides of the board

Placement_Note: Place on MDI lines so there are no stubs all 8 caps.

Ethernet Connector
Termination

Place close to FireWire PHY

Cable Power

Late-VG Protection Power
ODD Power Control

SATA ODD Port

SATA HDD Port

SATA Connectors
We can add protection to 5V if we want, but leaving NC for now.

Place L4600 and L4605 at connector pin.

Port Power Switch

Left USB Port A

Left USB Port B

USB/SMC Debug Mux

External USB Connectors

Min Neck Width = 0.375 mm
Min Line Width = 0.5 mm
Voltage = 5V

SYNC_MASTER = M98_MLB
SYNC_DATE = 11/14/2008

Min Neck Width = 0.375 mm
Min Line Width = 0.5 mm
Voltage = 3.3V

PM_SLP_S4_L
USB_PWR_EN
PP3V42_G3H
USB_EXTB_OC_L
USB_DEBUGPRT_EN_L
USB2_EXTA_MUXED_P
USB2_EXTA_MUXED_N
USB_LT2_N
USB_LT2_P
USB_EXTB_OC_L
USB_EXTA_OC_L
USB_EXTA_OC_L
USB_EXTB_P
USB_EXTB_OC_L
USB_EXTA_O
NOTE: Unused pins have "SMC.Pin" names. Unused pins designated as outputs can be left floating, those designated as inputs require pull-ups.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

NOTE: P84 and P85 are shorted, P85 could be spare.
Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

0.1uF 10V MF1206 1%0.5W

Place RC close to SMC

4.53K 1%1/16W MF-LF402

SMC_MCP_VSENSE
0.22UF 20% X5R 6.3V2

C5399

CPU VCore High Side Current Sensor

1%1/16W

BMON_ENG

SC70

MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.20 mm
Analog SMS

R5921 pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC.

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.

Sudden Motion Sensor (SMS)

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APPLE INC.
Any of the 4 frequencies can be selected with R5190 and R5191.
25 MHz is selected with R5190 and R5191.
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 Hz.
VIN = 2Vrms, CODEC VIN = 1.21 Vrms

AUD_LI_R_DIV

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

AUD_LI_P_L

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

AUD_LI_GND

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

AUD_LI_R

GND_AUDIO_CODEC

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

AUD_LI_L

www.vinafix.vn
CODEC OUTPUT SIGNAL PATHS

CODEC INPUT SIGNAL PATHS

PORT A DETECT [HEADPHONES]  PORT B DETECT [SPDIF DELEGATE]

PORT B LEFT [HEADSET MIC]

PORT B RIGHT [BUILT-IN MIC]

PORT C DETECT [LINE-IN]
[Diagram of a power supply schematic]

MCP 1.05V S0 (AUX) SUPPLY

VOUT = 0.8V * (1 + RA / RB)

VOUT = 1.05V

Max Current = 0.5A

Misc Power Supplies
Page Notes

- PP3V3_GPU_IFPCD_IOVDD
- PP1V8_GPU_IFPX
- 2K
- 1/16W
- 1%

Page Notes

- R8851
- 1K
- 1%

Page Notes

- PP1V8_GPU_IFPEF_PLLVDD_F
- PP1V1_GPU_IFPEF_IOVDD_F
- 1
- R8851
- 1K
- 1%

Page Notes

- GPU_IFPAB_RSET
- GPU_IFPEF_RSET
- 8 71 73 76 83
- PP1V1_S0GPU_REG
- 8 78
- 78
- 78

Page Notes

- FERR-220-OHM
- L8815
- L8805
- L8800
- 0402
- 0402
- 0402

Page Notes

- C8810
- C8805
- C8800
- 21
- 4.7UF
- 2
- 2
- 2

Page Notes

- CERM
- CERM
- 6.3V
- 20%

Page Notes

- 160mA peak
- ?mA peak per diff pair
- Place at AJ8
- Place at AG9

Page Notes

- www.vinafix.vn
- C8816
- C8811
- C8801

Page Notes

- I2CS must be pulled up if not used.
- I2CS addr fixed at 0x9E,0x9F

Page Notes

- VOLTAGE=1.8V
- MIN_LINE_WIDTH=0.3 mm

Page Notes

- 10V
- 20%

Page Notes

- VOLTAGE=1.1V
- MIN_NECK_WIDTH=0.1 mm

Page Notes

- NC
- NC
- NC
- NC
- NC
- NC

Page Notes

- GPAK_I2CE_SCL
- GPAK_I2CH_SCL
- GPAK_I2CD_SCL
- GPAK_I2CS_SCL
- GPAK_I2CA_SCL
- GPAK_I2CC_SCL
- GPAK_I2CS_SCL
- GPAK_I2CC_SCL

Page Notes

- BI
- BI
- BI
- BI
- BI
- BI

Page Notes

- DACC_VSYNC
- DACB_CSYNC
- DACA_VSYNC
- DACB_VDD
- DACB_RED
- DACA_VREF

Page Notes

- IFPEF_PLLVDD
- IFPCD_RSET
- IFPAB_PLLVDD
- IFPE_IOVDD
- IFPD_IOVDD
- IFPC_IOVDD

Page Notes

- IFPF_L2*
- IFPF_AUX
- IFPE_L3*
- IFPE_L2*
- IFPE_L1*
- IFPD_L3*
- IFPD_L2*
- IFPD_L1*
- IFPC_L3*
- IFPC_L2*
- IFPC_L1*
- IFPC_L0*

Page Notes

- AG9
- AG10
- AJ8
- AA4
- AK4

Page Notes

- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
- OUT
1.8V/1.2V S0 SWITCHER

Vout = 0.6V * (1 + Ra/Rb)

f = 2.25 MHz

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)

0.6A max output

(Switcher limit)
Most CPU signals with impedance requirements are 55-ohm single-ended.

Intel Design Guide recommends FSB signals be routed only on internal layers.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

Signals within each 4x group should be matched within 5 ps of strobe.

FSB 4X signals / groups shown in signal table on right.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.
### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Area_Type</th>
<th>Spacing_Rule_Set</th>
<th>Net_Spacing_Type1</th>
<th>Net_Spacing_Type2</th>
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</thead>
<tbody>
<tr>
<td>MEM_CTRL2MEM</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_CLK</td>
<td>MEM_CLK2MEM</td>
</tr>
<tr>
<td>MEM_DATA2MEM</td>
<td>MEM_DATA2MEM</td>
<td>MEM_CLK</td>
<td>MEM_CLK2MEM</td>
</tr>
<tr>
<td>MEM_CMD2MEM</td>
<td>MEM_CMD2MEM</td>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
</tr>
<tr>
<td>MEM_CMD</td>
<td>MEM_CMD</td>
<td>MEM_CMD2CMD</td>
<td>MEM_CMD2MEM</td>
</tr>
<tr>
<td>MEM_CMD2MEM</td>
<td>MEM_CMD2MEM</td>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
</tr>
</tbody>
</table>

### Memory Bus Constraints

- **MEM_CTRL2CTRL**: 2:1_SPACING
- **MEM_DATA2MEM**: 3:1_SPACING
- **MEM_CMD2MEM**: 3:1_SPACING

### Diagrams

- Electrical Components: MEM_B_DQS_P<5> - MEM_B_DQ<55..48>
- Electrical Components: MEM_B_DQS_P<4> - MEM_B_DQ<39..32>
- Electrical Components: MEM_B_DQS_P<3> - MEM_B_DQ<23..16>
- Electrical Components: MEM_B_DQS_P<2> - MEM_B_DQ<15..8>
- Electrical Components: MEM_B_DQS_P<1> - MEM_B_DQ<7..0>
- Electrical Components: MEM_B_DQS_N<5> - MEM_B_DQ<55..48>
- Electrical Components: MEM_B_DQS_N<4> - MEM_B_DQ<39..32>
- Electrical Components: MEM_B_DQS_N<3> - MEM_B_DQ<23..16>
- Electrical Components: MEM_B_DQS_N<2> - MEM_B_DQ<15..8>
- Electrical Components: MEM_B_DQS_N<1> - MEM_B_DQ<7..0>
- Electrical Components: MEM_B_DQS_N<0> - MEM_B_DQ<1..0>
- Electrical Components: MEM_B_DM<7> - MEM_B_DQ<55..48>
- Electrical Components: MEM_B_DM<6> - MEM_B_DQ<39..32>
- Electrical Components: MEM_B_DM<5> - MEM_B_DQ<23..16>
- Electrical Components: MEM_B_DM<4> - MEM_B_DQ<15..8>
- Electrical Components: MEM_B_DM<3> - MEM_B_DQ<7..0>
- Electrical Components: MEM_B_DM<2> - MEM_B_DQ<1..0>
- Electrical Components: MEM_B_DM<1> - MEM_B_DQ<0..0>
- Electrical Components: MEM_B_DM<0> - MEM_B_DQ<0..0>

### Area Type Spacing

- **Area Type**: MEM_DATA
  - **Spacing Rule Set**: MEM_DATA2MEM
  - **Net Spacing Type 1**: MEM_DATA
  - **Net Spacing Type 2**: MEM_CLK

- **Area Type**: MEM_CLK
  - **Spacing Rule Set**: MEM_CLK2MEM
  - **Net Spacing Type 1**: MEM_CLK
  - **Net Spacing Type 2**: MEM_CLK2MEM

### Table Spacing Assignment

- **Table Spacing Assignment**
  - **Area Type**: MEM_CTRL
  - **Spacing Rule Set**: MEM_CTRL2MEM
  - **Net Spacing Type 1**: MEM_CTRL
  - **Net Spacing Type 2**: MEM_CTRL2MEM

- **Table Spacing Assignment**
  - **Area Type**: MEM_CTRL
  - **Spacing Rule Set**: MEM_CTRL2MEM
  - **Net Spacing Type 1**: MEM_CTRL
  - **Net Spacing Type 2**: MEM_CTRL2MEM

### Table Physical Rule

- **Table Physical Rule**
  - **Area Type**: MEM_CTRL
  - **Spacing Rule Set**: MEM_CTRL2MEM
  - **Net Spacing Type 1**: MEM_CTRL
  - **Net Spacing Type 2**: MEM_CTRL2MEM

### Table Electrical Constraint

- **Table Electrical Constraint**
  - **Area Type**: MEM_CTRL
  - **Spacing Rule Set**: MEM_CTRL2MEM
  - **Net Spacing Type 1**: MEM_CTRL
  - **Net Spacing Type 2**: MEM_CTRL2MEM

### Table Source

- **Source**: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4
- **Source**: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2
- **Source**: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
### SATA Interface Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

- **Max length of LVDS/DisplayPort/TMDS traces:** 12 inches.
- **LVDS intra-pair matching:** should be 5 mils. Pairs should be within 100 mils of clock length.

### Digital Video Signal Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

- **75-ohm from output of three-pole filter to connector (if possible).**
- **37.5-ohm from MCP to first termination resistor.**
- **CRT signal single-ended impedance:** varies by location:
  - PCI-Express: MCP_DAC_COMP * ?=2:1_SPACING
  - PCIE_90D: ?=3X_DIELECTRIC

### Analog Video Signal Constraints

- **Line-to-line spacing:** varies by location:
  - SATA: TOP,BOTTOM =3x_DIELECTRIC
  - CRT: 50 MIL

### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>8 MIL</td>
<td>20 MIL</td>
<td>100_OHM_DIFF</td>
<td>90_OHM_DIFF</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>8 MIL</td>
<td>20 MIL</td>
<td>100_OHM_DIFF</td>
<td>90_OHM_DIFF</td>
</tr>
</tbody>
</table>

### Table: Spacing Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
<th>Physical Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>CRT_2CLK 50 MIL</td>
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### PHY Constraints

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<th>Max Neck Length</th>
<th>Diff Pair Prim Gap</th>
<th>Diff Pair Neck Gap</th>
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<tr>
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<td>7.5 mil</td>
<td>Standard</td>
<td>100 ohm</td>
<td>100 ohm</td>
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**ENET**

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<th>Diff Pair Prim Gap</th>
<th>Diff Pair Neck Gap</th>
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<tr>
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<td>Standard</td>
<td>100 ohm</td>
<td>100 ohm</td>
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**Source:** MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

**88E1116R (Ethernet PHY) Constraints**

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<td>ENET_MDI_P&lt;3..0&gt;</td>
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<tr>
<td></td>
<td>ENET_RXD&lt;3..0&gt;</td>
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<tr>
<td></td>
<td>ENET_CLK125M_RXCLK</td>
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<tr>
<td></td>
<td>ENET_RXD&lt;0&gt;</td>
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<tr>
<td></td>
<td>ENET_RXD_STRAP</td>
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<td>ENET_RX_CTRL</td>
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<tr>
<td></td>
<td>ENET_TXD&lt;3..0&gt;</td>
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<td>ENET_INTR_L</td>
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**MCP RGMII (Ethernet) Constraints**

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<td>ENET_RX_CTRL</td>
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**MCP MII_COMP**

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**MCP_BUF0_CLK**

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**Source:** MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4
### FireWire Interface Constraints

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### FireWire Net Properties

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<th>X Min</th>
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### SD Card Interface Constraints

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<th>Y Margin</th>
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### FireWire Constraints

- **Sync Master**: MUX
- **Sync Date**: 02/18/2008
- **FW TP**: 110_OHM_DIFF
- **SD_55S**: =STANDARD
- **SD_INTERFACE**: FW_110D, FW_PORT1_TPA, FW_PORT1_TPB, NC_FW0_TPBN, NC_FW0_TPBP, NC_FW0_TPAP

---

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### SMC SMBus Net Properties

<table>
<thead>
<tr>
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<th>Constraint Set</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
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<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>SMC_BSA_SDA</td>
<td>0.1 mm</td>
<td>7.42 mm</td>
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<tr>
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<td>SMC_MGMT_SCL</td>
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<td>7.42 mm</td>
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<tr>
<td>SMBUS_SMC_B_SA_SCL</td>
<td>SMC_BSA_SCL</td>
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<td>7.42 mm</td>
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<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>SMC_0_SCL</td>
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<td>7.42 mm</td>
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<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
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### SMBus Charger Net Properties

<table>
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<th>Constraint Set</th>
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<td>SMC_B_SA_SCL</td>
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### SMC Constraints

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- **Not to reveal or publish in whole or part.**
- **To maintain the document in confidence.**
### Memory Constraint Relaxations

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### Graphics SATA Constraint Relaxations

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<th>Net Spacing Type 2</th>
<th>Layer</th>
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### Project Specific Constraints

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*Forma power-referenced memory signals (1394, 1394v, SATA) to non-power on 1394, 1394v & 1394v (non-referenced planes).*
## PCB Board-specific Spacing & Physical Constraints

### Table: Physical Rule Item

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### Table: Spacing Rule Item

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<td>MEM_CLK</td>
<td>BGA_P1MM</td>
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<td>BGA_P3MM</td>
<td>FSB_DSTB</td>
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### Table: Spacing Assignment Item

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<tr>
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<td>MEM_CLK</td>
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<td>BGA_P2MM</td>
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<tr>
<td>FSB_DSTB</td>
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### Note
100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.