K24 MLB SCHEMATIC

PVT RELEASE

5/6/2009
## K24 BOARD STACK–UP

### Top
- **SIGNAL**
- **SIGNAL (High Speed)**
- **GROUND**
- **SIGNAL (High Speed)**
- **POWER**
- **GROUND**
- **SIGNAL (High Speed)**
- **SIGNAL (High Speed)**
- **GROUND**
- **SIGNAL**

### Bottom
- **SIGNAL**

## Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1000</td>
<td>1</td>
<td>SIGNAL</td>
<td>12010</td>
<td>CRITICAL</td>
<td>BOM_0000</td>
</tr>
<tr>
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## Programmable Parts

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## Alternate Parts

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## DEVELOPMENT BOM

<table>
<thead>
<tr>
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**BOM Variants**

<table>
<thead>
<tr>
<th>BOM GROUP</th>
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<th>BOM OPTIONS</th>
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<td>BOM Groups</td>
<td>BOM Group</td>
<td>BOM Options</td>
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</table>

**Alternate Parts**

- **LOCKED BOOTROM APN IS 341S2443**
- **QTY**
- **DESCRIPTION**

## Bar Code Labels / E2E #'s

<table>
<thead>
<tr>
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**MCP_0000:**
- **CRITICAL**
- **DRAWING NUMBER**
- **SHT**
- **NONE**
- **REV.**
- **CRITICAL**

---

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TOKO AS ALTERNATE

**REFERENCES DES**

**DESCRIPTION**

- **REFERENCE DES**
- **DESCRIPTION**

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SYNC_MASTER = M97_MLB

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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CHANGE C1240-C1243 AND C1260 FROM 128S0241 (9 MILLI-OHM) TO 128S0231 (6 MILLI-OHM)

REMOVE NO STUFF CAPS C1220 TO C1231

SYNC FROM T18

D2T-SM

D2T-SM

CPU Decoupling

SYNC_DATE=03/31/2008

4X 330UF. 20X 22UF 0805

VCCP (CPU I/O) DECOUPLING

VCCA (CPU AVdd) DECOUPLING

2X 330UF, 6x 0.1uF 0402

VCCP (CPU I/O) DECOUPLING

4X 330UF. 20X 22UF 0805

CPU VCore HF and Bulk Decoupling

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

PLACE inside socket cavity on secondary side.

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PLACE inside socket cavity on secondary side.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout. Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.

DP_IG_AUX_CH_P/N = MCP_HDMI_DDC_DATA

MCP Signal

8 TMDS_IG_DDC_CLK

8 TMDS_IG_TXD_P/N<2>

Dual-channel TMDS: Power +VDD_IFPx at 3.3V
LVDS:              Power +VDD_IFPx at 1.8V

22B6
22A5
17D3
7B5
229
78C
72C8
72B7
229
78C
72C8
72B7

Alias to HPLUG_DET2 for other systems.

Alias to DVI_HPD for systems using IFP for DVI.

pull-ups (~10K to 3.3V S0). To ensure pins are low
In MCP79 these pins have undocumented internal

OUT
OUT
OUT
OUT
OUT
OUT
OUT
OUT
OUT
OUT
IN
IN
IN
IN

95 mA (A01)
16 mA (A01)
190 mA (A01, 1.8V)

MCP_IFPAB_RSET

MCP_HDMI_RSET

=PP1V05_S0_MCP_HDMI_VDD

=PP3V3R1V8_S0_MCP_IFP_VDD

=PP3V3_S0_MCP_GPIO

MCP_HDMI_VDD

HPLUG_DET2/GPIO_22

DP_AUX_CH0_P

HDMI_TXD2_N/ML0_LANE0_N

HDMI_TXD2_P/ML0_LANE0_P

HDMI_TXD1_N/ML0_LANE1_N

HDMI_TXD0_N/ML0_LANE2_N

HDMI_TXC_P/ML0_LANE3_P

HDMI_VPROBE

+VDD_HDMI

+V_PLL_IFPAB

R1820

ME-LF

1/16W

MF-LF

5%

APPLE INC.

Okay to float XTALIN_TV and XTALOUT_TV.

Okay to float DDC_CLK0/DDC_DATA0 pull-ups still required.

Okay to float all RGB_DAC signals.

May be necessary to ground or raise LVDS and TMDS.
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

- REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672
- REMOVE HDCP ROMS
- CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
- SYNC FROM T18
- MCP Graphics Support

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.

Required zero ohm resistors when no VREF margining circuit stuffed

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<th>NOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>25A5</td>
<td>2</td>
<td>VREFMRGN_CPUFSB_BUF</td>
<td>CRITICAL</td>
<td>UCSP</td>
</tr>
<tr>
<td>25A5</td>
<td>2</td>
<td>VREFMRGN_CA_SODIMMA_BUF</td>
<td>CRITICAL</td>
<td>UCSP</td>
</tr>
<tr>
<td>25A5</td>
<td>2</td>
<td>VREFMRGN_DQ_SODIMMA_BUF</td>
<td>CRITICAL</td>
<td>UCSP</td>
</tr>
<tr>
<td>25A5</td>
<td>2</td>
<td>VREFMRGN_CA_SODIMMB_BUF</td>
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Revision A

87 6 5 4 3 2 1

APPLE INC.

5%
1/16W MF-LF 402

1K
R3310

5%
402 1/16W MF-LF

10K
R3300

5%
402 MF-LF

21
R3305

5%
402 MF-LF

C3300

1/16W MF-LF

10V
0.1UF 20%
CERM 402

402

5%
402 MF-LF

R3301

7D3
7A3

SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008

MCP_MEM_RESET_L = PP1V5_S3_MEMRESET
MEM_RESET_RC_L = PP3V3_S5_MEMRESET
MEM_RESET_L = MCP79_RESET

DDR3 Support

051-7898 4.7.0

DMB53D0UDW SOT-363 Q3305

28 81

MCP79 does not meet DDR3 spec power-up reset timing requirement.

DDDR3 RESET Support
WLAN Enable Generation

```
3.3V ENET FET

WLAN = (S3 && AP_PWR_EN) && (AC || S0)
```

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

```
I(max) = 1.7A (85C)
Rds(on) = 90mOhm max
@ 2.5V Vgs:
3.3V ENET FET
1.05V ENET FET
```

MOBILE:

```
RTL8211 25MHz Clock

= P1V05ENET_EN. Nets separated on
Recommend aliasing PM_SLP_RMGT_L and ARB for alternate power options.

= P3V3ENET_EN. Nets separated on
Recommend aliasing PM_SLP_RMGT_L and ARB for alternate power options.
```

Pull-up is with power FET.

```
R3800 = 1/16W 5% 100K
```

```
C3811 = 0.033UF
C3810 = 0.01UF
C3840 = 0.1UF
C3841 = 0.01UF
```

```
MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
```

```
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
```

```
Ethernet & AirPort Support
```

```
SMC_ADAPTER_EN
PM_SLP_S3_L
PM_WLAN_EN_L
AC_OR_S0_L
SMC_ADAPTER_EN
PM_SLP_S3_L
PM_WLAN_EN_L
AC_OR_S0_L
```

```
Q3801
SSM6N15FEAPE
SOT563
Q3810
NTR4101P
SOT-23-HF
```

```
C3810
16V
0.01UF
```

```
C3811
16V
0.033UF
```

```
C3840
CERM
0.1UF
```

```
C3841
CERM
0.01UF
```

```
Q3805
SSM6N15FEAPE
SOT563
```

```
Q3841
SSM6N15FEAPE
SOT563
```

```
R3800
MF-LF
1% 1/16W 69.8K
```

```
Q3840
MF-LF
1% 1/16W 10K
```

```
R3841
MF-LF
1% 1/16W 402 10K
```

```
R3841
MF-LF
402 10K
```

```
R3842
MF-LF
1% 1/16W 10K
```

```
R3895
MF-LF
1/16W 100K
```

```
Q3805
SSM6N15FEAPE
SOT563
```

```
Q3841
SSM6N15FEAPE
SOT563
```

```
R3800
```

```
R3895
```

```
C3840
```

```
C3841
```

```
C3810
```

```
C3811
```

```
Q3805
```

```
Q3841
```

```
Q3840
```

```
Q3801
```

```
Q3810
```

```
Q3841
```

```
Q3840
```

```
Q3801
```

```
Q3810
```

```
Q3841
```

```
Q3840
```

```
R3801
```

```
C3810
```

```
C3811
```

```
R3810
```

```
R3895
```

```
Q3805
```

```
Q3841
```

```
R3841
```

```
R3895
```

```
Q3805
```

```
Q3841
```

```
R3841
```

```
R3895
```

```
Q3805
```

```
Q3841
```

```
R3841
```

```
R3895
```
ETHERNET CONNECTOR

ENET_CONN CTAP

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

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402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%

CRITICAL

2

1

402-1

10PF

50V

CERM

5%
**PLACEMENT_NOTE**

- Place C4503 close to J4501
- Place C4526 close to J4500
- Place FL4520 close to J4500
- Place C4515 next to C4516
- Place C4516 close to J4501
- Place FL4502 close to J4501
- Place FL4525 close to J4500
- Place C4521 next to C4520
- Place C4520 close to MCP79
- Place C4510 close to MCP79
- Place C4511 next to C4510

**SATA HDD/IR/SIL**

**ODD Power Control**

**NOTE:** 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

**SYNC_DATE=12/04/2008**

**SYNC_MASTER=K19_MLB**

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**SYMBOLIC VERIFICATION:**

- ODD_PWR_EN_L
- SATA_ODD_D2R_C_P
- SATA_ODD_D2R_UF_P
- SATA_ODD_R2D_UF_P
- SATA_HDD_D2R_P
- SATA_HDD_D2R_UF_P
- SATA_HDD_R2D_P
- SATA_HDD_R2D_UF_P

**SCALE:**

- 37
- 33
- 30
- 28
- 25
- 22
- 20
- 18
- 16
- 14
- 12
- 10
- 8
- 6
- 4
- 2

**SIZE:**

- 4.7.0

**DRAWING NUMBER:**

- 051-7898

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We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

External USB Connectors

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SYNC_DATE=01/18/2008

SYNC_MASTER=YUAN.MA
those designated as inputs require pull-ups.

Otherwise, TP/NC okay (was ISENSE_CAL_EN)

PLACEMENT NOTE=PLACE R4999 CLOSE TO U4900 PINS M12

PLACEMENT NOTE=PLACE C4920 CLOSE TO U4900 PINS M12

VOLTAGE=3.3V MIN

NECK WIDTH=0.20 MM

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SYNC_DATE=06/26/2008

APPENDIX A

B
CPU Voltage Sense / Filter

- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000

MCP Voltage Sense / Filter

- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000

PBUS VOLTAGE SENSE ENABLE & FILTER

- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000
- PLACE EXPERIMENTAL SAMPLE CLOSE TO U1000

VOLTAGE SENSING

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APPLE INC. 2008
MCP VCore Current Sense Filter

CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)

WAB92

MCP MEM VDD Current Sense

DC-IN (AMON) CURRENT SENSE

PLACCE U5403 AND C5418 NEAR R7008

NOTE: MONITORING CURRENT FROM BATTERY TO PCI (BATTERY DISCHARGE) ACROSS R7008

INA213 has gain of 50V/V

For engineering, stuff U5313 and unstuff R5330
Place RC close to SMC

For production, stuff R5330 and unstuff U5313
Place RC close to SMC

BMON PROD

SYNC_DATE=12/17/2008

SYNC_MASTER=YUNWU

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APPLE INC.
CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

REPLACED 518S0521 WITH 518S0519
TRISTATE SMC_SYS_KBDLED:
To detect Keyboard backlight, SMC will
LOW = keyboard backlight present
HIGH = keyboard backlight not present

KEYBOARD BACKLIGHT DRIVING AND DETECTION

BOOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- LOAD LINE REGULATION
- RIPPLE TO MEET ERS (MAX 20%)
- DROOP LINE REGULATION
- POWER CONSUMPTION
- RIPPLE TO MEET ERS (MAX 20%)

BOOSTER DESIGN CONSIDERATION:
- R5812, R5813, C5818 MODIFIED
  - STARTUP TIME LESS THAN 2MS
  - RIPPLE TO MEET ERS
  - DROOP LINE REGULATION
  - POWER CONSUMPTION

3V3 LDO FOR IPD

To detect Keyboard backlight, SMC will
LOW = keyboard backlight present
HIGH = keyboard backlight not present

WELLSPRING 2

APPLE INC.
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.

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APPLE INC.
MCPT79 SPI Frequency Select

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>42 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>25 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- 25MHz is selected with R6190 and R6191.
- Any of the 4 frequencies can be selected with R6190, R6191, R5190, and R5191.
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
CODEC RSH = 10.56K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
PC HP = 3.6 HZ
PC LP = 43KHz
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

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AUDIO: LINE INPUT FILTER

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

APPLE INC.
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

AV_PB = -1V/V, FC_LPF = 35.2KHZ

MAX9724 GAIN/FILTER COMPONENTS
APN: 353S1637

SYNC_DATE=02/03/2009
SYNC_MASTER=AUDIO
AUDIO: HEADPHONE FILTER

APPENDIX B: AUDIO FILTERS

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appleinc
1.5V/0.75V (DDR3) POWER SUPPLY

\[ VOUT = 0.75V \times \left(1 + \frac{RA}{RB}\right) \]

**ROUTING NOTE:**
- PUT 6 VIAS UNDER THE THERMAL PAD
- USE KEVIN CONNECTION.
- Q7321 PIN1, 2, 3
  - CONNECT CS_GND TO

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**SYNC_DATE: 01/31/2008**
**SYNC_MASTER: RAYMOND**

**MAX CURRENT = 12A**
**PWM FREQ. = 400 KHZ**
**PUT ONE BULK CAP NEXT TO THE LOAD**

**STATE | PM_SLP_S4_L | PM_SLP_S3_L | PP1V5_S3 | PP0V75_S0**
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>HIGH</td>
<td>HIGH</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>S3</td>
<td>HIGH</td>
<td>LOW</td>
<td>1.5V</td>
<td>0.0V</td>
</tr>
<tr>
<td>S5/G3HOT</td>
<td>LOW</td>
<td>LOW</td>
<td>0.0V</td>
<td>0.0V</td>
</tr>
</tbody>
</table>

**1.5V/0.75V DDR3 SUPPLY**

**SCALE | SIZE | REV. | DRAWING NUMBER**
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
<td>B</td>
<td>A</td>
</tr>
</tbody>
</table>

**NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

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**II AGREES TO THE FOLLOWING**

**III NOTICE OF PROPRIETARY PROPERTY**
VOUT = 1.062V
F = 320 KHZ
8A max output

Vout = 0.75V * (1 + Ra / Rb)

PLACEMENT_NOTE = Place XW7665 next to L7620

C7660
1
330UF
20%
TANT
CASE-B2-SM

C7661
402
20%
16V
33UF
TANT
CASE-D2E-SM

C7665
402
8.45K
1%
1/16W

R7670
MF-LF
1%
1/16W
20.0K

R7671
MF-LF
1%
1/16W

X5R
1
603-1
10%
25V

C7695
1UF
1
2
CASED2E-SM
POLY-TANT

C7630
CRITICAL
20%
16V
33UF
X7R
0.1UF
10%
50V

C7603
2
4.7UF
10%
1
2
C7604
603
X5R-CERM
6.3V

C7601
10%
66C1
66A5
1/16W
1%
MF-LF

R7604
1
8.87K
1/16W

R7601
1
8.87K
1/16W

R7603
MF-LF
1%
1/16W
200K

X5R
1
603-1
10%
25V

C7660
1
2
330UF
20%
2.5V
TANT
CASE-B2-SM

Q7620
MLP
1
4
9
7
8
10
3
FDMS9600S

L7620
2.2US-8.0A

CPUVTTS0_VBST
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

CPUVTTS0_VFB
DIDT=TRUE

CPUVTTS0_VSNS
DIDT=TRUE

CPUVTTS0_VOUT
DIDT=TRUE

CPUVTTS0_TRIP
MIN_NECK_WIDTH=0.2MM
GATE_NODE=TRUE

CPUVTTS0_LL
SWITCH_NODE=TRUE
DIDT=TRUE

CPUVTTS0_DRVH
GATE_NODE=TRUE
DIDT=TRUE

CPUVTTS0_DRVL
GATE_NODE=TRUE
DIDT=TRUE

CPU VT(1.05V) SUPPLY

SYNC_DATE=02/08/2008
SYNC_MASTER=RAYMOND
1.8V S0 SWITCHER

VOUT = 0.8V * (1 + RA / RB)

1.05V S0 PLL LDO

VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY

MISC POWER SUPPLIES

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DRAWING NUMBER

MIN. LINE WIDTH
VOLTAGE
MIN. NECK WIDTH
MCP79 DDRVTT FET

MCP79 DDRVTT FET is used to provide a 1.5V S0 FET.

ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP WILL EXIT SELF-REFRESH PREMATURELY.

UNTIL AFTER RAIL TURNS BACK ON OR DIMMS BEFORE RAIL IS TURNED OFF, AND REMAINS LOW MUST GUARANTEE MEM_CKE SIGNALS ARE LOW IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE

nVIDIA RECOMMENDS UNPOWERING DURING SLEEP.

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT (1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)
CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

343x478 34x298 34x121 34x586
681x478 535x478 827x478 974x478

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REV. A

SYNC_DATE=04/04/2008

SYNC_MASTER=NMARTIN

PP3V3_S5_LCD=PP3V3_S0_LCD

LVDS_IG_PANEL_PWR

LED_Return_6

LED_Return_5

LED_Return_4

LED_Return_3

LED_Return_2

LED_Return_1

PPVOUT_S0_LCDBKLT

LVDS_IG_A_DATA_N<1>

LVDS_IG_A_DATA_N<2>

LVDS_IG_A_DATA_P<2>

LVDS_IG_A_DATA_P<0>

MIN_NECK_WIDTH=0.20 MM

MIN_LINE_WIDTH=0.30 MM

VOLTAGE=3.3V

PP3V3_LCDVDD_SW_F

PP3V3_S0_LCD_F

LVDS_IG_A_CLK_P

LVDS_IG_A_CLK_N

LVDS_IG_DDC_CLK

LVDS_IG_DDC_DATA

TP_BKL_SYNC

MIN_NECK_WIDTH=0.20 MM

PP3V3_LCDVDD_SW

VOLTAGE=3.3V

MIN_LINE_WIDTH=0.30 MM

LVDS Connector:518S0650
Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up on the MLB).
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MCP has internal 10K pull-up for these signals.

PVDS 20 LCDSALT FET

<table>
<thead>
<tr>
<th>NAME</th>
<th>PACKAGE</th>
<th>SN</th>
<th>VOLTAGE</th>
<th>MIN_NECK_WIDTH</th>
<th>MIN_LINE_WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC638APZ_SBMS001</td>
<td>SSOT6-HF</td>
<td>1 2 5 6</td>
<td>12.6V</td>
<td>0.25 mm</td>
<td>0.4 mm</td>
</tr>
<tr>
<td>FDC638APZ_SBMS001</td>
<td>SSOT6-HF</td>
<td>3 4 5 6</td>
<td>12.6V</td>
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</tr>
</tbody>
</table>

SYNC_DATE=06/30/2008

MCP has internal 10K pull-up for these signals.

PVDS 20 LCDSALT FET

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<tr>
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SYNC_DATE=06/30/2008

MCP has internal 10K pull-up for these signals.

PVDS 20 LCDSALT FET

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<td>FDC638APZ_SBMS001</td>
<td>SSOT6-HF</td>
<td>3 4 5 6</td>
<td>12.6V</td>
<td>0.25 mm</td>
<td>0.4 mm</td>
</tr>
</tbody>
</table>

SYNC_DATE=06/30/2008
**FSB (Front-Side Bus) Constraints**

**CPU Signal Constraints**

- Source: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4
- CPU Signal Constraints
  - Note: Intel Design Guide allows closer spacing if signal lengths can be shortened.
  - Intel Design Guide recommends FSB signals be routed only on internal layers.
  - Design Guide recommends each strobe/signal group is routed on the same layer.
  - Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.
  - Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.
  - Signals within each 2x group should be matched within 20 ps. ADSTB#s should be matched +/- 300 ps.
  - DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
  - Signals within each 4x group should be matched within 5 ps of strobe.
  - FSB 4X signals / groups shown in signal table on right.
  - All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

**FSB 1X Signals**

- (CPU_VCCSENSE)
- (CPU_VCCSENSE)
- (CPU_8MIL)
- (CPU_AGTL)
- (CPU_COMP)
- CPU_GTLREF
- (CPU_DPRSTP_L)
- FSB_CLK_MCP_N
- FSB_CLK_ITP_N
- FSB_CLK_ITP_P

**FSB Clock Constraints**

- Source: MCP79 Interface DG (DG-03328-001_v01), Section 2.7
- FSB Clock Constraints
  - Source: MCP79 Interface DG (DG-03328-001_v01), Section 2.7

**CPU / FSB Net Properties**

**PHYSICAL_RULE_SET**

**SPACING_RULE_SET**

**CPU_GTLREF**

**CPU_27P4S**

**CPU_8MIL**

**CPU_AGTL**

**FSB_DATA**

**MCP_50S**

**CPU_50S**

**CPU_ITP**

**LINE-TO-LINE SPACING**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_RULE_HEAD**

**LINE-TO-LINE SPACING**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_RULE_HEAD**

**LINE-TO-LINE SPACING**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_RULE_HEAD**

**LINE-TO-LINE SPACING**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_RULE_HEAD**

**LINE-TO-LINE SPACING**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**CORE PHOTO**
**Memory Bus Constraints**

<table>
<thead>
<tr>
<th>Memory Bus Constraint</th>
<th>X</th>
<th>Y</th>
<th>Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
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</thead>
<tbody>
<tr>
<td>NET_SPACINGTYPE1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NET_SPACINGTYPE2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Memory Data</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Memory Control</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Memory DQS</td>
<td></td>
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</table>

**Memory Net Properties**

<table>
<thead>
<tr>
<th>Memory Net</th>
<th>Property</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_A_DQ</td>
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</tr>
<tr>
<td>MEM_B_DQ</td>
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<td></td>
</tr>
<tr>
<td>MEM_A_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS</td>
<td></td>
<td></td>
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<tr>
<td>MEM_B_DQS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CMD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CMD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
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<tr>
<td>MEM_B_CNTL</td>
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</tbody>
</table>

**Memory Bus Spacing Group Assignments**

<table>
<thead>
<tr>
<th>Memory Bus Spacing Group</th>
<th>X</th>
<th>Y</th>
<th>Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
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</thead>
<tbody>
<tr>
<td>NET_SPACINGTYPE1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NET_SPACINGTYPE2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Memory Constraints**

**Notice of Proprietary Property**

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**Memory Bus Constraints**

- **AD/BA/cmd signals should be matched within 5 ps of CLK pairs.**
- **No DQS to clock matching requirement.**
- **DQ signals should be matched within 5 ps of associated DQS pair.**

**DDR3**

- **DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.**

**DDR2**

- Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Memory Bus Spacing Group</th>
<th>X</th>
<th>Y</th>
<th>Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
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</thead>
<tbody>
<tr>
<td>NET_SPACINGTYPE1</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NET_SPACINGTYPE2</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SPACING_RULE_SET**

- **AREA_TYPE**
  - **MINIMUM LINE WIDTH**
  - **MAXIMUM NECK LENGTH**
  - **DIFFPAIR NECK GAP**
  - **MINIMUM NECK WIDTH**
  - **5 MIL**
  - **7 MIL**
  - **2:1_SPACING**
  - **4:1_SPACING**
  - **70_OHM_DIFF**
  - **40_OHM_SE**
  - **STANDARD**

**Memory Bus Spacing Group Assignments**

- **PHYSICAL_RULE_SET**
- **TABLE_SPACING_RULE_HEAD**
  - **TABLE_SPACING_ASSIGNMENT_ITEM**
- **MEMORY BUS ASSIGNMENT**

---

**NET_TYPE**

- **NET_TYPE**
- **NET_SPACINGTYPE1**
- **NET_SPACINGTYPE2**

---

**Memory Net Properties**

- **ELECTRICAL_CONSTRAINT_SET**
  - **MEMORY Net Properties**
  - **MEMORY Net Properties**
  - **MEMORY Net Properties**
  - **MEMORY Net Properties**
  - **MEMORY Net Properties**
  - **MEMORY Net Properties**

---

**Memory Constraints**

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### SATA Interface Constraints

*SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.*

- DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
- DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
- LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

### PCI-Express

#### PHYSICAL_RULE_SET

- **LINE-TO-LINE SPACING**
  - =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF
  - =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF
  - =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD

- **MINIMUM NECK WIDTH**
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  - =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF

- **MAXIMUM NECK LENGTH**
  - TOP,BOTTOM TOP,BOTTOM TOP,BOTTOM TOP,BOTTOM TOP,BOTTOM TOP,BOTTOM

- **MINIMUM LINE WIDTH**
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  - =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF

### Digital Video Signal Constraints

#### LAYER

- **LINE-TO-LINE SPACING**
  - ALLOW ROUTE =3x_DIELECTRIC

- **MINIMUM NECK WIDTH**

- **MAXIMUM NECK LENGTH**

### MCP Constraints 1

*NOT TO REVEAL OR PUBLISH IN WHOLE OR PART*
### PCI Bus Constraints

| Source: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14. |

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### Notation

- **ENET_MDI** = 100_OHM_DIFF
- **ENET_MII_55S** = 55_OHM_SE
- **ENET_MII** = STANDAR
- **ENET_MII_55S** = STANDAR
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**FireWire Interface Constraints**

**FireWire Net Properties**

**SD Card Interface Constraints**

**SD Card Net Properties**

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**FireWire Constraints**

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Apple Inc.
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<td></td>
</tr>
<tr>
<td>B14</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>0.126 MM</td>
<td>0.090 MM</td>
<td></td>
</tr>
<tr>
<td>B15</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>DEFAULT</td>
<td>0.100 MM</td>
<td></td>
</tr>
<tr>
<td>B16</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>0.076 MM</td>
<td>0.090 MM</td>
<td></td>
</tr>
<tr>
<td>B17</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>0.090 MM</td>
<td>0.076 MM</td>
<td></td>
</tr>
<tr>
<td>B18</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>0.100 MM</td>
<td>0.100 MM</td>
<td></td>
</tr>
<tr>
<td>B19</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>Top, Bottom</td>
<td>DEFAULT</td>
<td>0.076 MM</td>
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</tbody>
</table>

### SPACING RULE SET

<table>
<thead>
<tr>
<th>Table</th>
<th>Rule</th>
<th>Description</th>
<th>Level</th>
<th>Value</th>
<th>Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>LINE-TO-LINE SPACING</td>
<td>Top, Bottom</td>
<td>4X_DIELECTRIC</td>
<td>0.252 MM</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>LINE-TO-LINE SPACING</td>
<td>Top, Bottom</td>
<td>3X_DIELECTRIC</td>
<td>0.126 MM</td>
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</tr>
<tr>
<td>C3</td>
<td>LINE-TO-LINE SPACING</td>
<td>Top, Bottom</td>
<td>0.210 MM</td>
<td>0.25 MM</td>
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</tr>
<tr>
<td>C4</td>
<td>LINE-TO-LINE SPACING</td>
<td>Top, Bottom</td>
<td>DEFAULT</td>
<td>0 MM</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>LINE-TO-LINE SPACING</td>
<td>Top, Bottom</td>
<td>0.252 MM</td>
<td>0.25 MM</td>
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</tbody>
</table>

### BOARD LAYERS

<table>
<thead>
<tr>
<th>Layer</th>
<th>Allow Route</th>
<th>Minimum Line Width</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>Y</td>
<td>0.222 MM</td>
<td>0.091 MM</td>
<td>30 MM</td>
<td>0.330 MM</td>
<td>0.230 MM</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>Y</td>
<td>0.222 MM</td>
<td>0.091 MM</td>
<td>30 MM</td>
<td>0.330 MM</td>
<td>0.230 MM</td>
</tr>
</tbody>
</table>