M97A MLB SCHEMATIC
REFERENCED FROM T18
03/11/2009

**POST-RAMP**

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### Revision History

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### M97 BOARD STACK-UP

**Top**
- SIGNAL
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- POWER
- GROUND
- POWER
- GROUND

**Bottom**
- SIGNAL
Revision History

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.
1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)

From XDP connector

U1000 CPU

To XDP connector and/or level translator

From XDP connector or via level translator

U1400 MCP

XDP connector
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC FROM T18

CPU Power & Ground


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CPU Power & Ground

DRAWING NUMBER

SHT OF

REV.

APPLE INC.
Change C1240-C1243 and C1260 from 128S0241 (9 milli-ohm) to 128S0231 (6 milli-ohm).

Remove C1244 & C1245.

Remove no stuff caps C1220 to C1231.

Sync from T18.

CPU VCore HF and Bulk Decoupling:

CPU Decoupling

Sync from T18.

Remove no stuff caps C1220 to C1231.

Remove C1244 & C1245.

Change C1240-C1243 and C1260 from 128S0241 (9 milli-ohm) to 128S0231 (6 milli-ohm).
SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN

MCP79-specific pinout

SYNC_DATE=12/12/2007
SYNC_MASTER=T18_MLB

PLACEMENT_NOTE=Place close to CPU to minimize stub.

CRITICAL 6-1747769-0
F-ST-SM
9 8 7 6 5 4 3 2 1

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP PCIe Interfaces

SIZE

SYNC_DATE=04/04/2008

SYNC_MASTER=T18_MLB

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Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

(11 OF 11)
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.

MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

SMC_MCP_SAFE_MODE = PP3V3_S5_MCP_A01

JTAG_MCP_TMS
JTAG_MCP_TDI
SMC_RUNTIME_SCI_L
PM_PWRBTN_L
MAKE_BASE=TRUE
MCP_LID_L
PM_BATLOW_L
SMC_WAKE_SCI_L
PM_SYSRST_DEBOUNCE_L
PM_LATRIGGER_L
TP_MCP_LID_L
PCIE_WAKE_L

R2430
SMD_0805_0.015
R2429
SMD_0805_0.015
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

- **HDCP ROM**: contains the necessary information to enable HDCP (Highbandwidth Digital Content Protection) support.

- **SYNC FROM T18**: indicates the source of the sync signal.

- **REMOVE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT**: removes the crystal circuit because the device does not support TV output.

- **REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672**: disconnects the DAC terminations.

- **NO STUFF PP3V3_S0_MCP_DAC**: removes the PP3V3_S0_MCP_DAC rail components.

- **CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC**: changes the component values.

- **SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007**: sets the sync master and date.

- **VPDNeCK_WIDTH=0.2 MM**: sets the minimum neck width.

- **MIN_LINE_WIDTH=0.4 MM**: sets the minimum line width.

- **VOLTAGE=3.3V**: sets the voltage level.

- **=PP3V3_S0_HDCPROM**: connects the PP3V3_S0_HDCPROM rail.

- **=PP1V05_S0_MCP_HDMI_VDD**: connects the PP1V05_S0_MCP_HDMI_VDD rail.

- **=PP3V3R1V8_S0_MCP_IFP_VDD**: connects the PP3V3R1V8_S0_MCP_IFP_VDD rail.

- **=I2C_HDCPROM_SDA**: connects the I2C_HDCPROM_SDA line.

- **=I2C_HDCPROM_SCL**: connects the I2C_HDCPROM_SCL line.

- **HDCPROM_WP**: connects the HDCPROM_WP line.

- **MCP_HDMI_VPROBE**: connects the MCP_HDMI_VPROBE line.

- **MCP_HDMI_RSET**: connects the MCP_HDMI_RSET line.

- **MCP_IFPAB_RSET**: connects the MCP_IFPAB_RSET line.

- **MCP_IFPAB_VPROBE**: connects the MCP_IFPAB_VPROBE line.

- **MIN_LINE_WIDTH=0.4 MM**: sets the minimum line width again.

- **VOLTAGE=3.3V**: sets the voltage level again.

- **MIN_NECK_WIDTH=0.2 MM**: sets the minimum neck width again.

- **PP3V3_S0_MCP_DAC_UF**: connects the PP3V3_S0_MCP_DAC_UF rail.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail.

- **PP3V3_S0_MCP_DAC_UF**: connects the PP3V3_S0_MCP_DAC_UF rail.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail again.

- **MCP IFPAB RSET**: connects the MCP_IFPAB_RSET line again.

- **MCP IFPAB VPROBE**: connects the MCP_IFPAB_VPROBE line again.

- **MCP_HDMI_RSET**: connects the MCP_HDMI_RSET line again.

- **MCP_HDMI_VPROBE**: connects the MCP_HDMI_VPROBE line again.

- **MIN_LINE_WIDTH=0.4 MM**: sets the minimum line width again.

- **VOLTAGE=3.3V**: sets the voltage level again.

- **MIN_NECK_WIDTH=0.2 MM**: sets the minimum neck width again.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail again.

- **PP3V3_S0_MCP_DAC_UF**: connects the PP3V3_S0_MCP_DAC_UF rail again.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail again.

- **MCP IFPAB RSET**: connects the MCP_IFPAB_RSET line again.

- **MCP IFPAB VPROBE**: connects the MCP_IFPAB_VPROBE line again.

- **MCP_HDMI_RSET**: connects the MCP_HDMI_RSET line again.

- **MCP_HDMI_VPROBE**: connects the MCP_HDMI_VPROBE line again.

- **MIN_LINE_WIDTH=0.4 MM**: sets the minimum line width again.

- **VOLTAGE=3.3V**: sets the voltage level again.

- **MIN_NECK_WIDTH=0.2 MM**: sets the minimum neck width again.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail again.

- **PP3V3_S0_MCP_DAC_UF**: connects the PP3V3_S0_MCP_DAC_UF rail again.

- **PP3V3_S0_MCP_VPLL_UF**: connects the PP3V3_S0_MCP_VPLL_UF rail again.

- **MCP IFPAB RSET**: connects the MCP_IFPAB_RSET line again.

- **MCP IFPAB VPROBE**: connects the MCP_IFPAB_VPROBE line again.

- **MCP_HDMI_RSET**: connects the MCP_HDMI_RSET line again.

- **MCP_HDMI_VPROBE**: connects the MCP_HDMI_VPROBE line again.
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for results in earlier ROMSIP and MCP FSB I/O interface initialization.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections,
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.

Required zero ohm resistors when no VREF margining circuit stuffed:

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<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>NON OPTION</th>
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<td>29B3</td>
<td>CERM 402</td>
<td>10V</td>
<td>20%</td>
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<tr>
<td>28B3</td>
<td>VCC</td>
<td></td>
<td></td>
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<tr>
<td>29A1</td>
<td>VDD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29A2</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29D5</td>
<td>VOUTASCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27B3</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27B4</td>
<td>VCC</td>
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<td></td>
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<tr>
<td>27B5</td>
<td>VOUTASCL</td>
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<tr>
<td>27B6</td>
<td>CPU_GTLREF</td>
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<tr>
<td>27B7</td>
<td>CPU_GTLREF</td>
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</table>
MCP79 cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

DDR3 RESET Support

Before 1.5V starts to rise to 3.3V input must be stable before MCP79 can control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

MMDT3904-X-G

CERM
0.1UF
MEMRESET_HW

1/16W MF-LF 402
R3310

10V
C3300

20%
5%
10K
MEMRESET_HW

1/16W MF-LF 402
R3300

MEMRESET_MCP

MMDT3904-X-G

Q3305

28C2 29C2

5%
20K
MEMRESET_HW

1/16W MF-LF 402
R3301

MEMRESET_HW

SOT-363-LF

MMDT3904-X-G

Q3305

28C2 29C2

5%
20K
MEMRESET_HW

1/16W MF-LF 402
R3305

MMDT3904-X-G

Q3305

28C2 29C2

5%
20K
MEMRESET_HW

1/16W MF-LF 402
R3309

MEMRESET_HW
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VENICE CONNECTOR

SYNC_DATE=03/13/2008
SYNC_MASTER=YITE

VENICE CONNECTOR

051-7918 C
WLAN Enable Generation

"WLAN" = (S3 && AP_PWR_EN) && (AC || S0)

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

3.3V ENET FET

Ethernet & AirPort Support

051-7918 C

SYNC_MASTER=SUMA
SYNC_DATE=07/01/2008

1.05V ENET FET

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock. Use clock in alternate ENET rail if present.
Design must ensure P1V05 is powered whenever ENET rail is, or use separate crystal.

CRITICAL
NOTE: 3.3V must be IO if 5V is S3 or S5 to ensure the drive is powered in S3/S5.

PLACEMENT_NOTE=PLACE C4516 close to J4501
PLACEMENT_NOTE=PLACE C4515 next to C4516

PLACEMENT_NOTE=PLACE FL4501 close to J4501

CRITICAL

PLACEMENT_NOTE=PLACE C4501 close to J4501
PLACEMENT_NOTE=PLACE C4502 close to J4501

PLACEMENT_NOTE=PLACE FL4502 close to J4501

CRITICAL

PLACEMENT_NOTE=PLACE FL4520 close to J4500

CRITICAL

PLACEMENT_NOTE=PLACE C4521 next to C4520
PLACEMENT_NOTE=PLACE C4520 close to MCP79

PLACEMENT_NOTE=PLACE C4511 next to C4510
PLACEMENT_NOTE=PLACE C4510 close to MCP79
NOTE: Ground pins have "NOC,Pin" names. Ground pins designed as outputs can be left floating. 
Unused outputs can be left unpopulated.

Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC_PB3:

BI

OUT

IN

ALS_RIGHT

SMC_NB_DDR_ISENSE

SMC_NB_CORE_ISENSE

SMS_Z_AXIS

SMS_Y_AXIS

SMC_FAN_3_TACH

SMC_FAN_1_TACH

SMC_FAN_3_CTL

SMC_FAN_2_CTL

SMC_FAN_1_CTL

SMC_EXCARD_CP

PM_BATLOW_L

SMC_SYS_KBDLED

SMC_GFX_THROTTLE_L

SMB_MGMT_DATA

LPC_SERIRQ

LPC_CLK33M_SMC

LPC_FRAME_L

LPC_AD<2>

LPC_AD<1>

LPC_AD<0>

ESTARLDO_EN

PM_PWRBTN_L

ALL_SYS_PWRGD

SMC_EXCARD_PWR_EN

SMC_ODD_DETECT

SMC_TX_L

SMB_A_S3_DATA

SMB_BSA_CLK

SMC_TMS

SMC_LID

PM_SLP_S5_L

PM_SLP_S3_L

SMB_MGMT_CLK

SMC_RX_L

SMC_TX_L

SMC_PBUS_VSENSE

SMC_DCIN_ISENSE

SMC_GPU_VSENSE

SMC_CPU_VSENSE

SMC_CPU_ISENSE

SMC_ADAPTER_EN

SMC_PM_G2_EN

PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15

NOTE: Pins D11 and D5 are shared. D5 could be spared.

NOTE: One interrupt can be active high or low, narrow not accordingly. If one interrupt is not used, pull up to GND each.
**CPU Voltage Sense / Filter**

- R5309
- CS509
- Place RC close to SMC

**MCP Voltage Sense / Filter**

- R5329
- CS509
- Place RC close to SMC

**PBUS VOLTAGE SENSE ENABLE & FILTER**

- R5315
- CS516
- Place RC close to SMC

---

**VOLTAGE SENSING**

- MIN LINE WIDTH: 0.20 mm
- MIN NECK WIDTH: 0.20 mm
- PPBUS_G3HRS5_VSENSE: VOLTAGE = 18.5V

---

**PLACEMENT_NOTE**

- Place near U1400 center
- Place near U1000 center
CPU T-Diode Thermal Sensor

DETECT CPU DIE TEMPERATURE
DETECT HEAT PIPE TEMPERATURE
DETECT FIN-STACK TEMPERATURE

REPLACED 518S0521 WITH 518S0519

MCP T-Diode Thermal Sensor

DETECT MCP DIE TEMPERATURE
DETECT MCP PROXIMITY TEMPERATURE
DETECT CPU PROXIMITY TEMPERATURE

REPLACED 518S0521 WITH 518S0519
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DRAWING NUMBER

SHEET OF

SIZE

D

5V DC TACH MOTOR CONTROL

GND

518S0521

NC

402 MF-LF 5% 1/16W

47K

R5665

47K 1/16W MF-LF 402

2

1

R5660

100K 402 MF-LF 1/16W 5%

2

1

R5661

SOD-VESM-HF

Q5660

SSM3K15FV

J5601

M-RT-SM

78171-0004

CRITICAL

4 3 2 1

6 5

8 7 6 5 4 3 2 1

SYNC_DATE=01/18/2008 SYNC_MASTER=CHANGZHANG

SMC_FAN_0_TACH FAN_RT_TACH SMC_FAN_0_CTL

=PP3V3_S0_FAN_RT =PP5V_S0_FAN_RT =PP3V3_S0_FAN_RT =PP5V_S0_FAN_RT

FAN_RT_PWM 39A8 7D7 39B8 8C5 8D5 7D7

APPLE INC.
BOoster +18.5VDC FOR sEnsORS

BOOSTER DESIGN CONSIDERATION:
- Power Consumption
- Short-Circuit Protection
- Double as Reset Pin
- ISO-7854 AND CARD OPTION
- SMD, BumpLESS

TRIPLE SMC_SYS_KBDLED:
To detect Keyboard backlight, SMC will

LOW = keyboard backlight present
HIGH = keyboard backlight not present

MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

KEYBOARD BACKLIGHT DRIVING AND DETECTION

To detect Keyboard backlight, SMC will

Z2_BOOST_EN
Z2_DEBUG3
Z2_CS_L
Z2_RESET
PSOC_F_CS_L
PSOC_SCLK
PSOC_MOSI
PSOC_MISO
Z2_KEY_ACT_L
Z2_HOST_INTN
Z2_CLKIN

KBD BACKLIGHT CONNECTOR

IPD FLEX CONNECTOR

PP5V_S3_TPAD
PP5V_S3_VR
PP18V5_S3_SW
PP18V5_S3

MIKEY RECEIVER CKT

PLACE R6301, R6305, R6306, R6307, AND R6308 OUTSIDE AUDIO SECTION TO CONSERVE AUDIO AREA

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<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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<td>R6301</td>
<td>2.2UF 16V X5R</td>
<td>1</td>
<td>CRITICAL MIKEY</td>
</tr>
<tr>
<td>R6302</td>
<td>NOSTUFF 0402</td>
<td>1</td>
<td>L6300</td>
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<td>R6303</td>
<td>2.2K 5% 1/16W</td>
<td>1</td>
<td>MF-LF MIKEY</td>
</tr>
<tr>
<td>R6304</td>
<td>1K 5% 1/16W</td>
<td>1</td>
<td>MF-LF MIKEY</td>
</tr>
<tr>
<td>R6305</td>
<td>100K 5% 1/16W</td>
<td>1</td>
<td>MF-LF MIKEY</td>
</tr>
<tr>
<td>R6306</td>
<td>5% 1/16W SENTRY</td>
<td>1</td>
<td>L6301</td>
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<td>R6307</td>
<td>NOSTUFF 0402</td>
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<td>L6301</td>
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<td>R6308</td>
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AUDI0: MIKEY
SYNC_MASTER=FULL
SYNC_DATE=07/03/2008

APPLE INC.
5V_RT/3.3V POWER SUPPLY

PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

VOUT = (2 * RA / RB) + 2
VOUT = (2 * RC / RD) + 2

C7290
10UF
603
X5R
20%

Place XW7201 between Pin 15 and Pin 25 of U7200.

ROUTING NOTE:

Place XW7202 between Pin 1 and Pin 2 of C7292.

C7292
150UF
CRITICAL
CASE-B2-SMPOLY-TANT
6.3V
20%

64D1
IN
=PP5VRT_S0_REG

PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

C7280
33UF
POLY-TANT
CASED2E-SM

5V_RT/3.3V POWER SUPPLY

C7260
402
X5R
16V10%

XW7203
XW7204
XW7205

5VRT_S0_VFB_XW7203
5VRT_S0_VFB
5VRT_S0_VO1
5VRT_S0_LL
5VRT_S0_DRVH
5VRT_S0_DRVH
5VRT_S0_BST
5VRT_S0_ENTRIP

Q7261
Q7260

MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6 MM

PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

C7270
1UF
603-1
25V10%

6.3V
CASE-B2-SMPOLY-TANT

CRITICAL

L7260
CRITICAL
PWRPK-1212-8-HF

45A5
2
1

SYNC_MASTER=RAYMOND
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1.5V/0.75V (DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

MAX CURRENT = 12A
PWM FREQ. = 400 KHZ

SYNC_MASTER = RAYMOND
SYNC_DATE = 01/31/2008

1.5V/0.75V DDR3 SUPPLY
**IMVP6 CPU VCore Regulator**

**IMVP6_PHASE1**
- R7412
- C7426

**IMVP6_PHASE2**
- R7418
- C7434

**IMVP6_PHASE3**
- R7423
- C7419

**IMVP6_PHASE4**
- R7422
- C7418

**IMVP6_PHASE5**
- R7421
- C7417

**NOTICE OF PROPRIETARY PROPERTY**
- UTILS DATE: 10/12/2006
- UTILS SIZE: 051-7918
- UTILS SCALE: 1:1

**REV.**
- D

**DRAWING NUMBER**
- D

**MIN. MECHANICAL CLEARANCE**
- 0.25 MM

**MIN. NECK WIDTH**
- 0.25 MM

**MIN. LINE WIDTH**
- 0.25 MM

**MAX. CURRENT**
- 44 A

**PWM FREQ. = 300 KHZ**

**LOAD LINE SLOPE = -2.1 mV/A**

**CPU PROCHOT_L**
- CPU_VID<3>
- CPU_VID<0>
- CPU_VID<1>
- CPU_VID<2>

**STUFF**
- MF-LF
- R7412

**NOT NOTE:**
- C7432, C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.
CPUVTT POWER SUPPLY

Place XW7600 between Pin 7 and Pin 15 of U7600.

Vout = 1.052V

Place XW7601 by C7660.

Vout = 0.75V * (1 + Ra / Rb)

F = 400 KHZ
1.8V S0 SWITCHER

MCP 1.05V_S5 AUXC SUPPLY

\[ \text{VOUT} = 0.6V \times (1 + \frac{R_a}{R_b}) \]

MCP 790 new AS1 requires higher voltage

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MISC POWER SUPPLIES

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</table>

APPLE INC.
### 3.3V S3 FET

#### Critical Components

- **Q7901**: P3V3S0_EN
- **Q7902**: P3V3S0_EN
- **Q7903**: P3V3S3_EN
- **Q7904**: P3V3S3_EN

#### Schematic Details

- **R7900**: 100K
- **C7900**: 0.01UF
- **C7901**: 0.01UF
- **C7902**: 0.1UF
- **C7903**: 0.068UF
- **C7904**: 0.001UF

### 3.3V S0 FET

#### Critical Components

- **Q7910**: 1.05V S0 FET
- **Q7911**: 1.05V S0 FET
- **Q7912**: 1.05V S0 FET

#### Schematic Details

- **R7910**: 10K
- **C7910**: 0.01UF
- **C7911**: 0.01UF
- **C7912**: 0.1UF
- **C7913**: 0.001UF

### 1.05V S0 FET

#### Critical Components

- **Q7915**: 1.05V S0 FET
- **Q7916**: 1.05V S0 FET
- **Q7917**: 1.05V S0 FET

#### Schematic Details

- **R7916**: 10K
- **C7916**: 0.01UF
- **C7917**: 0.01UF
- **C7918**: 0.1UF
- **C7919**: 0.001UF

### MCP79 DDRVT FET

- **MCP79 DDR FET**

#### Components

- **R7901**: 10K
- **C7902**: 0.068UF
- **C7903**: 0.001UF

#### Notes

This section details the circuitry and components used in the MPP79 DDR FET, including capacitor and resistor specifications. The diagram highlights critical connections and components, with attention to signal integrity and power distribution. The circuit is designed for high efficiency and reliability in DDR memory systems, ensuring optimal performance and stability under various operating conditions.
Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB).
Some signals require 27.4-ohm single-ended impedance.

**CPU Signal Constraints**

Signaling within each group should be matched within 5 ps of group.

FSB 1X signals shown in signal table on right.

Signals within each group should be matched within 20 ps.  ADTSB#s should be matched +/- 300 ps.

FSB 2X signals / groups shown in signal table on right.

DSTB# complementary pairs are spaced normally and are MCL routed as different pairs.

FSB 4X signals / groups shown in signal table on right.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

**CPU / FSB Net Properties**

**CPU/FSB Constraints**

**MCP FSB Comp Signal Constraints**

**FSB Clock Constraints**

**MCP FSB Interface**
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

Digital Video Signal Constraints

PCI-Express

*SATA_100D_HDD
*SATA_100D
*DP_100D
*CLK_PCIE_100D

LVDS_100D LVDS
=3x_DIELECTRIC*DISPLAYPORT

PCIE_90D PCIE
=4X_DIELECTRIC*PCIE

SATA_100D SATA
=SATA_TERMP
=3x_DIELECTRIC*LVDS

PCIE_MINI_R2D_C_N PCIE_MINI_R2D_C_P
=90_OHM_DIFF

TO LINE-TO-LINE SPACING

PCIE_CLK100M_MINI_CONN_P PCIE_CLK100M_MINI_CONN_N
=100_OHM_DIFF

PCIE_FC_R2D_C_P PCIE_FC_R2D_C_N
=100_OHM_DIFF

PCIE_FC_R2D_P PCIE_FC_R2D_N
=100_OHM_DIFF

MCP_HDMI_VPROBE MCP_DV_COMP
=100_OHM_DIFF

DP_ML_P<3..0> DP_ML_C_N<3..0>
=100_OHM_DIFF_HDD

PCIE_MINI_D2R_N PCIE_MINI_D2R_P
=90_OHM_DIFF

PCIE_FC_R2D_C_N PCIE_FC_R2D_P
=90_OHM_DIFF

PCIE_90D PCIE
=90_OHM_DIFF

SATA_HDD_D2R_UF_C_P SATA_HDD_D2R_UF_N
=STANDARD

SATA_HDD_D2R_P SATA_HDD_D2R_N
=STANDARD

SATA_HDD_D2R_P SATA_HDD_D2R_N
=STANDARD20 MIL 20 MIL

MCP_PEX_COMP MCP_PEX_CLK_COMP
=100_OHM_DIFF

MCP_PEX_COMP MCP_PEX_CLK_COMP
=100_OHM_DIFF

MCP_PEX_COMP MCP_PEX_CLK_COMP
=100_OHM_DIFF

MCP_PEX_COMP MCP_PEX_CLK_COMP
=100_OHM_DIFF
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### M97 SPECIAL CONSTRAINTS

The special constraints include:
- M97_MLB
- STANDARD
- 0.1 MM
- DIFFPAIR
- M97_SENSOR_NET_PROPERTIES

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**Scale**

The scale of the drawing is 1:1.
### M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

#### ISL3, ISL4, ISL9, ISL10

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#### SIZE

- **Scale:**
  - **NONE**

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### M97 RULE DEFINITIONS

#### Version

- **ALLEGRO (MIL or MM) BOARD UNITS BOARD LAYERS BOARD AREAS**

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