

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# M97A MLB SCHEMATIC

REFERENCED FROM T18

03/11/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
C		681298	PRODUCTION RELEASED		
				DATE	DATE
				03/11/09	?

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21	MCP HDA & MISC	T18_MLB	06/26/2008
22	MCP Power & Ground	T18_MLB	04/04/2008
23	MCP79 A01 Silicon Support	T18_MLB	03/08/2008
24	MCP Standard Decoupling	T18_MLB	04/04/2008
25	MCP Graphics Support	T18_MLB	12/12/2007
26	SB Misc	RAYMOND	04/05/2008
27	FSB/DDR3 Vref Margining	BEN	03/31/2008
28	DDR3 SO-DIMM Connector A	BEN	06/30/2008
29	DDR3 SO-DIMM Connector B	BEN	05/09/2008
30	DDR3 Support	T18_MLB	04/04/2008
31	Right Clutch Connector	YITE	04/22/2008
32	VENICE CONNECTOR	YITE	03/13/2008
33	Ethernet PHY (RTL8211CL)	SUMA	05/23/2008
34	Ethernet & AirPort Support	SUMA	07/01/2008
35	ETHERNET CONNECTOR	SUMA	04/04/2008

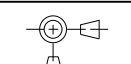
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60	IMVP6 CPU VCore Regulator	RAYMOND	01/31/2008
61	MCP VCore Regulator	RAYMOND	01/31/2008
62	CPU VTT(1.05V) SUPPLY	RAYMOND	02/08/2008
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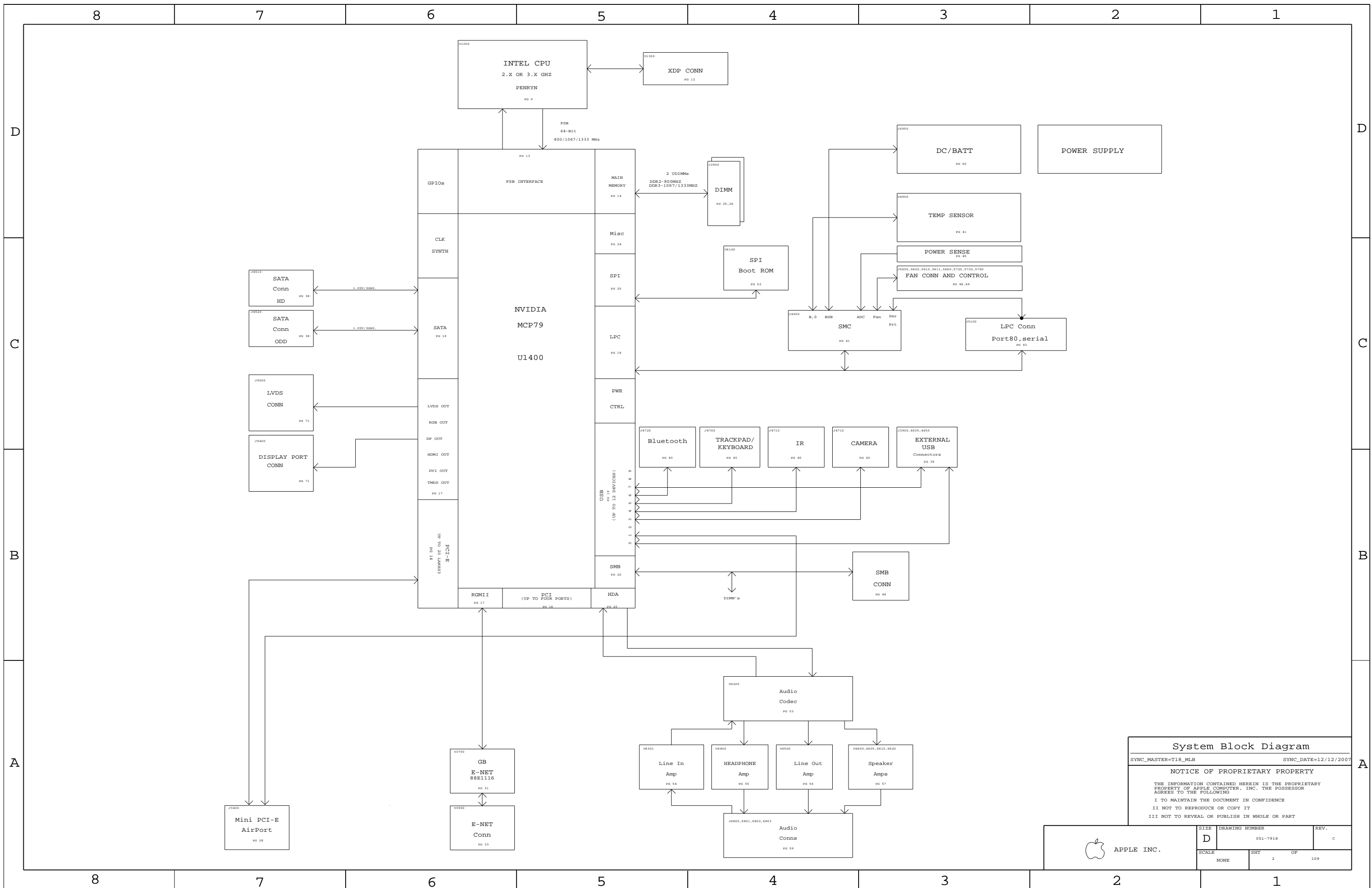
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## POST-RAMP

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7918	1	SCHEM, MLB, M97A	SCH	CRITICAL	
820-2327	1	PCBF, MLB, M97	PCB	CRITICAL	

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XX :	_____	DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
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**System Block Diagram**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9937	PCBA,MLB,BETTER,M97A	M97A_COMMON,CPU_2_0GHZ,EEE_6KM
630-9938	PCBA,MLB,BEST,M97A	M97A_COMMON,CPU_2_4GHZ,EEE_6KN,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6KM]	CRITICAL	EEE_6KM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6KN]	CRITICAL	EEE_6KN

BOM Groups

BOM GROUP	BOM OPTIONS
M97A_COMMON	COMMON,ALTERNATE,M97A_MCP,M97A_MISC,M97A_DEBUG_PROD,M97A_PROGPARTS
M97A_MCP	MCP_B02,MCP_PROD,MEMRESET_HW,MEMRESET_MCP,BOOT_MODE_USER,MCPSEQ_SMC,MCP_CS1_NO
M97A_MISC	ONEWIRE_PU,BKLT_PLL_NOT,DP_ESD,PROD_BMON,MIKEY
M97A_PROGPARTS	BOOTROM_PROD,SMC_PROD,IR_PROD,WELLSPRING_PROD
M97A_DEBUG_ENG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TFAD_DEBUG
M97A_DEBUG_PVT	SMC_DEBUG_YES,XDP,LPCPLUS,NO_VREFMRGN
M97A_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3693	1	PDC,SLOBE,FREQ.2.0,25W,1066,RO,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3680	1	PDC,SLBAN,FREQ.2.4,25W,1066,RO,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0635	1	IC,GMCP,MCP979,35X35MM,BGA1437,B02	U1400	CRITICAL	MCP_B02

Programmable Parts

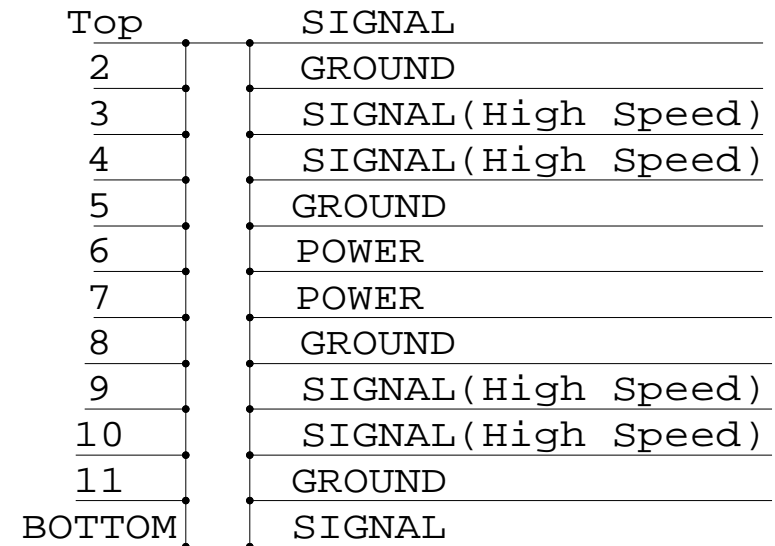
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HP	U4900	CRITICAL	SMC_BLANK
341S2444	1	IC,SMC,M97A	U4900	CRITICAL	SMC_PROD
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2440	1	IC,PRGRM,EPI BOOTROM,UNLOCK,M97A	U6100	CRITICAL	BOOTROM_PROD
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97A	U4800	CRITICAL	IR_PROD
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLP,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC,WELLSPRING CONTROLLER,M97A	U5701	CRITICAL	WELLSPRING_PROD

LOCKED M97A BOOTROM IS 341S2442

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S1381	353S1912		ALL	INTERTEC 284002 AS ALTERNATE
337S3646	337S3693		ALL	NO CPU AS ALTERNATE FOR 80 CPU
337S3639	337S3680		ALL	NO CPU AS ALTERNATE FOR 80 CPU
341S2287	341S2444		ALL	M97 SMC AS ALTERNATE
341S2285	341S2440		ALL	M97 BOOTROM AS ALTERNATE

# M97 BOARD STACK-UP



**BOM Configuration**

SYNC\_MASTER=M97\_MLB

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Revision History

BOM CHANGES FROM M97:

- REMOVE U5850, L5850, R5854, R5855, C5850, C5855, J5815 ON BETTER BOM.
- STUFF R5932
- CHANGE R6302 FROM 10K(114S315) TO 1K(114S0218).
- STUFF L6300
- NOSTUFF L6301
- UPDATE CPU APNS TO R0 STEPPING
- UPDATE 630 NUMBERS AND SEE CODES AND 051 NUMBER.
- UPDATE 341 NUMBERS FOR SMC AND BOOTROM.
- CHANGE U3700 FROM 3880570 TO 3880594, REALTEK PHY WITH ALDPS FIXED.
- ADD MOLEX SODIMM CONNECTORS AS ALTERNATE TO 00HM(116S0004).
- CHANGE R9711-R9722 FROM 10 OHM(105S198) TO 00HM(116S0004).
- CHANGE R9730 FROM 0.1OHM(114S0538) TO 00HM(116S0004).
- CHANGE J3900 FROM 514-0596 TO 514-0636
- CHANGE J4600 AND J4610 FROM 514-0606 TO 514-0638.
- CHANGE J9400 FROM 514-0610 TO 514-0637
- ADD INTERSIL 13160002(1333S1381) AS ALTERNATE FOR TI REF3333(353S1912).

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SYNC\_MASTER=M97\_MLB


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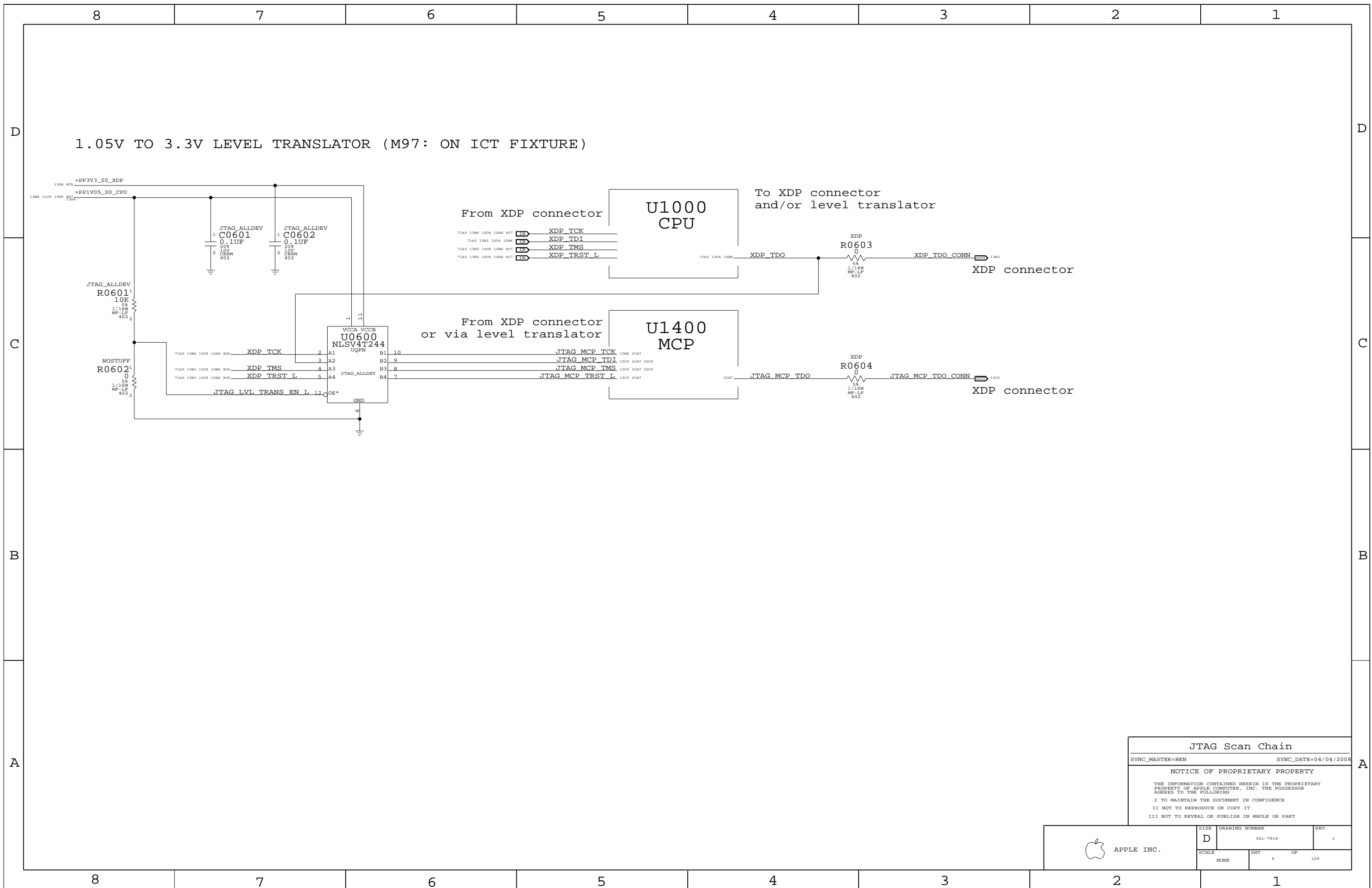
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**JTAG Scan Chain**

SYNC\_MASTER=BEN SYNC\_DATE=04/04/2008

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NONE	6		

# Functional Test Points

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## Fan Connectors

1880 TRUE PP5VRT S0 (NEED 3 TP) 703 805  
 1885 TRUE FAN RT PWM 4684  
 1815 TRUE FAN RT TACH 4604  
 (NEED TO ADD 3 GND TP)

## MIC FUNC\_TEST

1931 TRUE MIC HI CONN 5481 5402  
 1935 TRUE MIC LO CONN 5481 5402  
 1939 TRUE MIC SHLD CONN 5402 5546

## SPEAKER FUNC\_TEST

1990 TRUE SPKRAMP L N OUT 5382 5402  
 1920 TRUE SPKRAMP L P OUT 5382 5402  
 1925 TRUE SPKRAMP R N OUT 5303 5402  
 1928 TRUE SPKRAMP R P OUT 5303 5402  
 1932 TRUE SPKRAMP SUB N OUT 5382 5402  
 1933 TRUE SPKRAMP SUB P OUT 5302 5402

## THERMAL FUNC\_TEST

1926 TRUE MCPTHMSNS D2 P 4585 7703  
 1927 TRUE MCPTHMSNS D2 N 4585 7703

## LVDS FUNC\_TEST

1925 TRUE PP3V3 LCDVDD SW F 703 6602  
 1926 TRUE PP3V3 S0 LCD F 6603  
 1927 TRUE PPVOUT S0 LCDBKLT 703 6602 6983 6901  
 1928 TRUE LVDS IG DDC CLK 1883 6602  
 1929 TRUE LVDS IG DDC DATA 1883 6602  
 1930 TRUE LVDS IG A DATA N<0> 1883 6602 7383  
 1931 TRUE LVDS IG A DATA P<0> 1883 6602 7383  
 1932 TRUE LVDS IG A DATA N<1> 1883 6602 7383  
 1933 TRUE LVDS IG A DATA P<1> 1883 6602 7383  
 1934 TRUE LVDS IG A DATA N<2> 1883 6602 7383  
 1935 TRUE LVDS IG A DATA P<2> 1883 6602 7383  
 1936 TRUE LVDS IG A CLK F N 6602 7383  
 1937 TRUE LVDS IG A CLK F P 6602 7383  
 1938 TRUE LED RETURN 1 6683 6901  
 1939 TRUE LED RETURN 2 6683 6901  
 1940 TRUE LED RETURN 3 6683 6901  
 1941 TRUE LED RETURN 4 6683 6901  
 1942 TRUE LED RETURN 5 6683 6901  
 1943 TRUE LED RETURN 6 6683 6901  
 (NEED TO ADD 5 GND TP)

## SATA ODD CONN

1924 TRUE PP5V SW ODD (NEED 4 TP) 703 3603  
 1925 TRUE SMC ODD DETECT 3687 3988  
 1926 TRUE SATA ODD D2R C P 3685 73A3  
 1927 TRUE SATA ODD D2R C N 3685 73A3  
 1928 TRUE SATA ODD R2D P 3605 73A3  
 1929 TRUE SATA ODD R2D N 705 3605 73A3  
 (NEED TO ADD 4 GND TP)

## DC POWER CONN

1930 TRUE PP18V5 DCIN FUSE (NEED 3 TP) 5606  
 1931 TRUE ADAPTER SENSE 5607  
 (NEED TO ADD 4 GND TP)

## BATT POWER CONN

1930 TRUE PPVBAT G3H CONN F (NEED 3 TP) 56A8  
 1931 TRUE GND BATT CONN (NEED 3 TP) 56A8  
 1932 TRUE SMBUS SMC BSA\_SCL 7A7 4205 76D3  
 1933 TRUE SMBUS SMC BSA\_SCL 7A7 787 4205 76D3  
 1934 TRUE SMC BS ALRT L 3905 4082 56A8

## BATT SIGNAL CONN

1930 TRUE PP3V42 G3H (NEED 3 TP) 785 703 805  
 1931 TRUE SMBUS SMC BSA\_SCL 7A7 787 4205 76D3  
 1932 TRUE SMBUS SMC BSA\_SCL 7A7 787 4205 76D3  
 1933 TRUE SMC BIL BUTTON DB L 56A5  
 (NEED TO ADD 3 GND TP)

## FRONT FLEX CONN

1930 TRUE PP3V42 G3H LIDSWITCH\_R 3886  
 1931 TRUE PP5V S3 IR\_R 3886  
 1932 TRUE IR\_RX\_OUT 3884 3904  
 1933 TRUE SMC LID\_R 3886  
 1934 TRUE SYS\_LED ANODE\_R 3886  
 (NEED TO ADD 2 GND TP)

## RIGHT CLUTCH CONN

1930 TRUE PP5V S3 BTCAMERA\_F 3107  
 1931 TRUE PCIE MINI D2R P 1786 3107 73D3  
 1932 TRUE PCIE MINI D2R N 1786 3107 73D3  
 1933 TRUE PCIE MINI R2D P 3107 73D3  
 1934 TRUE PCIE MINI R2D N 3107 73D3  
 1935 TRUE PCIE CLK100M MINI CONN P 3107 73D3  
 1936 TRUE PCIE CLK100M MINI CONN N 3107 73D3  
 1937 TRUE USB CAMERA CONN P 3187 74C3  
 1938 TRUE USB CAMERA CONN N 3187 74C3  
 1939 TRUE PP5V WLAN 703 3105  
 1940 TRUE PCIE WAKE L 1786 3105 3107  
 1941 TRUE SMBUS SMC A S3\_SCL 785 4202 76D3  
 1942 TRUE SMBUS SMC A S3\_SDA 785 4202 76D3  
 1943 TRUE CONN USB2\_BT\_P 3187 74C3  
 1944 TRUE CONN USB2\_BT\_N 3187 7483  
 1945 TRUE MINI\_CLKREQ\_O\_L 3107  
 1946 TRUE MINI\_RESET\_CONN\_L 31A7  
 (NEED TO ADD 3 GND TP)

## SATA HDD CONN

1930 TRUE PP5V S0 HDD FLT (NEED 4 TP) 703 3687  
 1931 TRUE SATA HDD R2D P 36A7 73A3  
 1932 TRUE SATA HDD R2D N 36A7 73A3  
 1933 TRUE SATA HDD D2R\_C\_P 36A7 73A3  
 1934 TRUE SATA HDD D2R\_C\_N 36A7 73A3  
 1935 TRUE SATA ODD R2D\_N 707 3605 73A3  
 (NEED TO ADD 4 GND TP)

## IPD\_FLEX\_CONN

1930 TRUE PP3V3 S3 LDO 703 4884 4803  
 1931 TRUE PP18V5 S3 703 4801 4803  
 1932 TRUE TPAD\_GND\_F 4884 4803 4804 4807  
 1933 TRUE Z2\_CS\_L 4708 4803  
 1934 TRUE Z2\_DEBUG3 4708 4803  
 1935 TRUE Z2\_MOSI 4708 4803  
 1936 TRUE Z2\_MISO 4708 4803  
 1937 TRUE Z2\_SCLK 4708 4803  
 1938 TRUE Z2\_BOOST\_EN 4803 4805  
 1939 TRUE Z2\_HOST\_INTN 4708 4803  
 1940 TRUE Z2\_BOOT\_CFG1 4708 4803  
 1941 TRUE Z2\_CLKIN 4708 4803  
 1942 TRUE Z2\_KEY\_ACT\_L 4708 4801  
 1943 TRUE Z2\_RESET 4708 4801  
 1944 TRUE PSOC\_MISO 4708 4801  
 1945 TRUE PSOC\_MOSI 4708 4801  
 1946 TRUE PSOC\_SCLK 4708 4801  
 1947 TRUE SMBUS\_SMC\_A\_S3\_SDA 705 4202 76D3  
 1948 TRUE SMBUS\_SMC\_A\_S3\_SCL 705 4202 76D3  
 1949 TRUE PSOC\_F\_CS\_L 4708 4801  
 1950 TRUE PICKB\_L 4708 4801

## KEYBOARD CONN

1930 TRUE PP3V3 S3 703 803  
 1931 TRUE PP3V42 G3H 7A7 703 805  
 1932 TRUE WS\_KBD1 4706 4702  
 1933 TRUE WS\_KBD2 4706 4702  
 1934 TRUE WS\_KBD3 4706 4702  
 1935 TRUE WS\_KBD4 4706 4702  
 1936 TRUE WS\_KBD5 4706 4702  
 1937 TRUE WS\_KBD6 4706 4702  
 1938 TRUE WS\_KBD7 4706 4702  
 1939 TRUE WS\_KBD8 4706 4702  
 1940 TRUE WS\_KBD9 4706 4702  
 1941 TRUE WS\_KBD10 4706 4702  
 1942 TRUE WS\_KBD11 4706 4702  
 1943 TRUE WS\_KBD12 4706 4702  
 1944 TRUE WS\_KBD13 4706 4702  
 1945 TRUE WS\_KBD14 4702 4706  
 1946 TRUE WS\_KBD15\_CAP 4702  
 1947 TRUE WS\_KBD16\_NUM 4702  
 1948 TRUE WS\_KBD17 4702 4706  
 1949 TRUE WS\_KBD18 4702 4707  
 1950 TRUE WS\_KBD19 4702 4707  
 1951 TRUE WS\_KBD20 4702 4707  
 1952 TRUE WS\_KBD21 4702 4707  
 1953 TRUE WS\_KBD22 4702 4707  
 1954 TRUE WS\_KBD23 4702 4707  
 1955 TRUE WS\_KBD\_ONOFF\_L 4702  
 1956 TRUE WS\_LEFT\_SHIFT\_KBD 4783 4785 4702  
 1957 TRUE WS\_LEFT\_OPTION\_KBD 4783 4785 4702  
 1958 TRUE WS\_CONTROL\_KBD 4783 4785 4702  
 (NEED TO ADD 1 GND TP)

## KBD BACKLIGHT CONN

1930 TRUE KBDLED\_ANODE 48A6  
 (NEED TO ADD 2 GND TP)

## DEBUG VOLTAGE

1930 TRUE PPVCORE\_S0\_CPU 807  
 1931 TRUE PPCPUVTT\_S0 807  
 1932 TRUE PPVCORE\_S0\_MCP 807  
 1933 TRUE PP0V75\_S0 807  
 1934 TRUE PP1V05\_S0 807  
 1935 TRUE PP1V5\_S0 887  
 1936 TRUE PP1V8\_S0 887  
 1937 TRUE PP5VRT\_S0 707 805  
 1938 TRUE PP3V3\_S0 805  
 1939 TRUE PP1V5\_S3 805  
 1940 TRUE PP3V3\_S3 785 803  
 1941 TRUE PP5VLT\_S3 803  
 1942 TRUE PP1V1R1V05\_S5 883  
 1943 TRUE PP3V3\_S5 883  
 1944 TRUE PP3V42\_G3H 7A7 785 801  
 1945 TRUE PPBUS\_G3H 801  
 1946 TRUE PP3V3\_ENET\_PHY 881  
 1947 TRUE PP1V2R1V05\_ENET 881  
 1948 TRUE PP3V3\_G3\_RTC 2108 22A5 26D4  
 1949 TRUE PP5V\_WLAN 705 3105  
 1950 TRUE PP5V\_SW\_ODD 787 36D3  
 1951 TRUE PP5V\_S0\_HDD\_FLT 705 3687  
 1952 TRUE PP3V3\_S5\_AVREF\_SMC 3904 4006  
 1953 TRUE PP18V5\_S3 705 4801 4803  
 1954 TRUE PP3V3\_S3\_LDO 705 4884 4803  
 1955 TRUE PP3V3\_LCDVDD\_SW\_F 707 6602  
 1956 TRUE PPVOUT\_S0\_LCDBKLT 707 6682 6983 6901  
 1957 TRUE BKL\_VREF\_4V9 6986 6988 6904 6908  
 1958 TRUE PP4V6\_AUDIO\_ANALOG 51A3 51D3 52D6  
 1959 TRUE SMC\_PM\_G2\_EN 3905 6408  
 1960 TRUE PM\_SLP\_S4\_L 2103 3905 40A2 6408  
 1961 TRUE PM\_SLP\_S3\_L 2103 3487 3905 41A5 6405 68D8  
 (NEED TO ADD 4 GND TP)

## FUNC TEST

SYNC\_MASTER=M97\_MLB

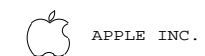
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	7	109

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7

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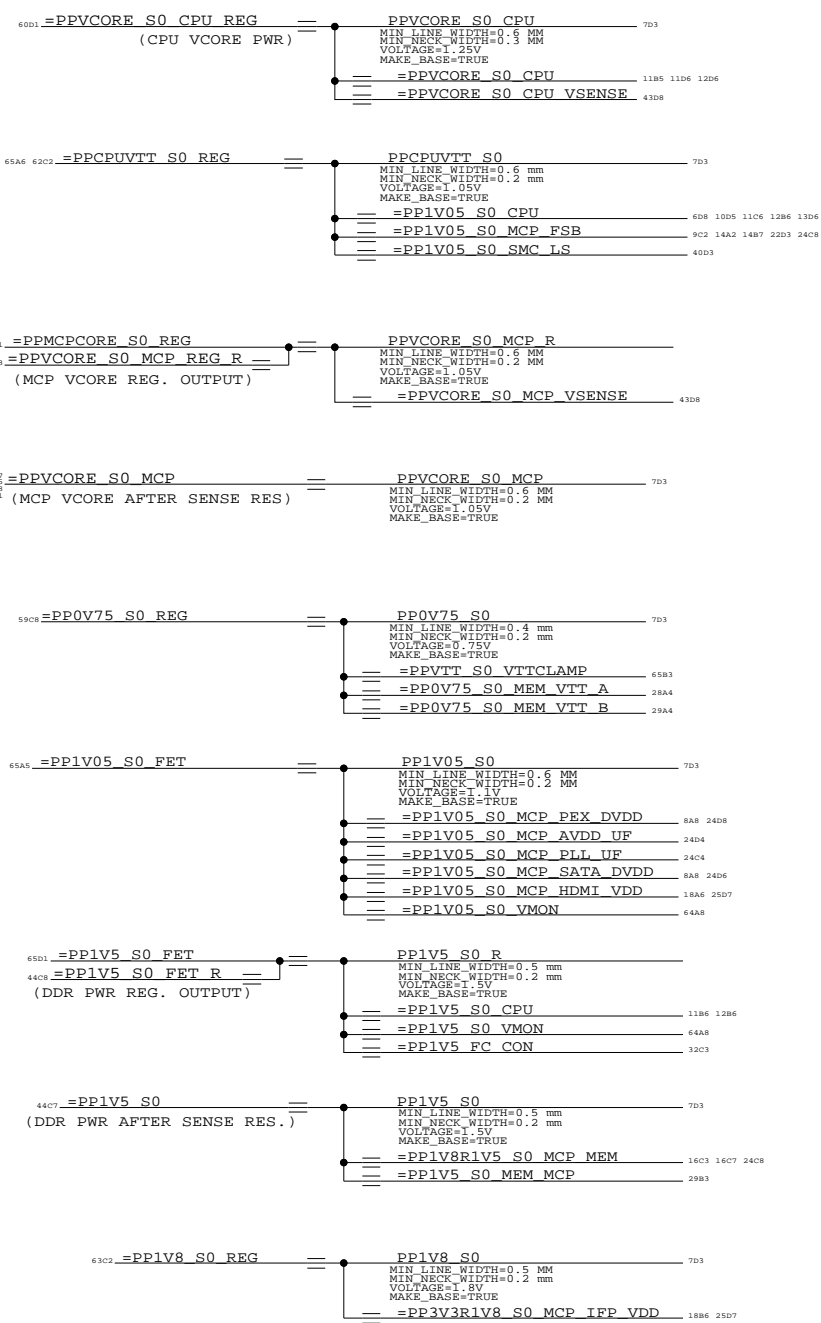
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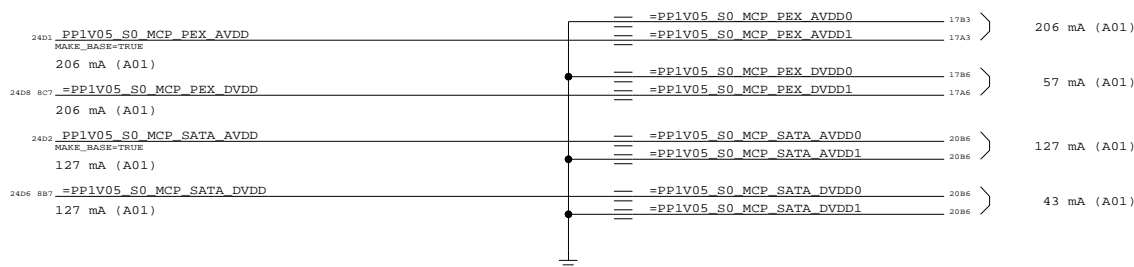
2

1

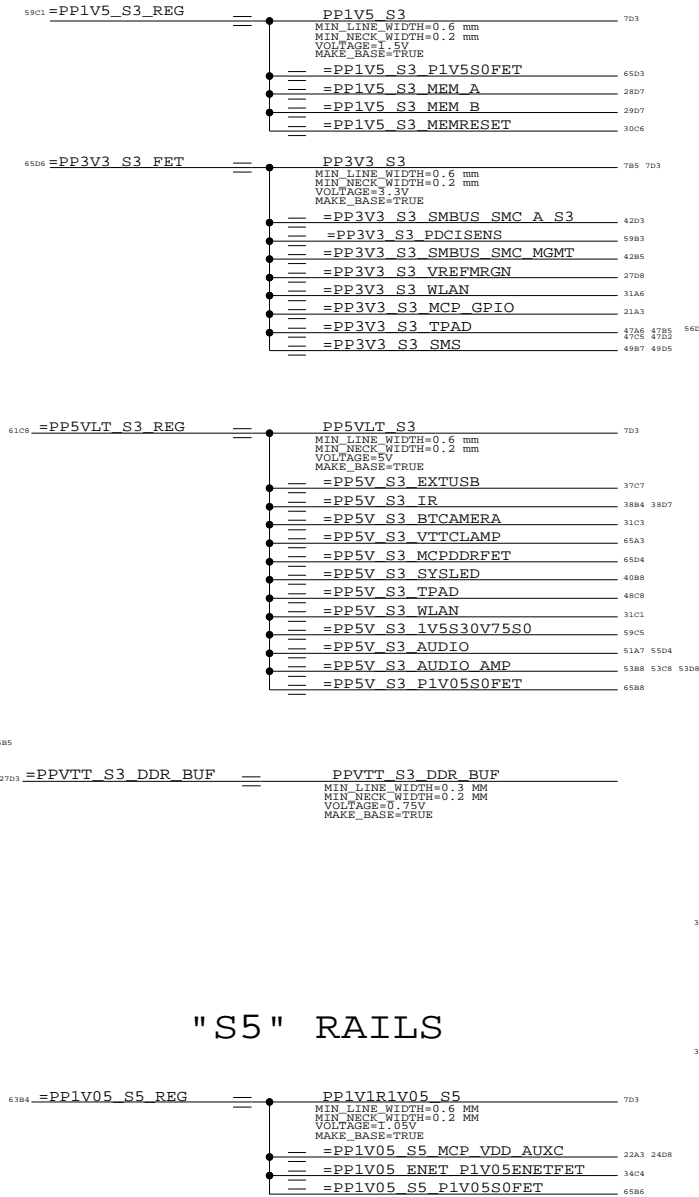
## "S0,S0M" RAILS



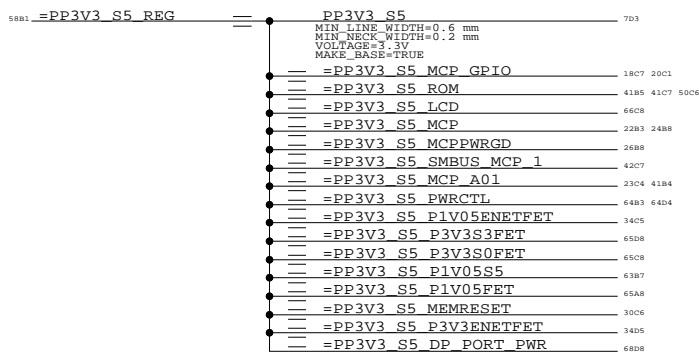
## PEX & SATA AVDD/DVDD aliases



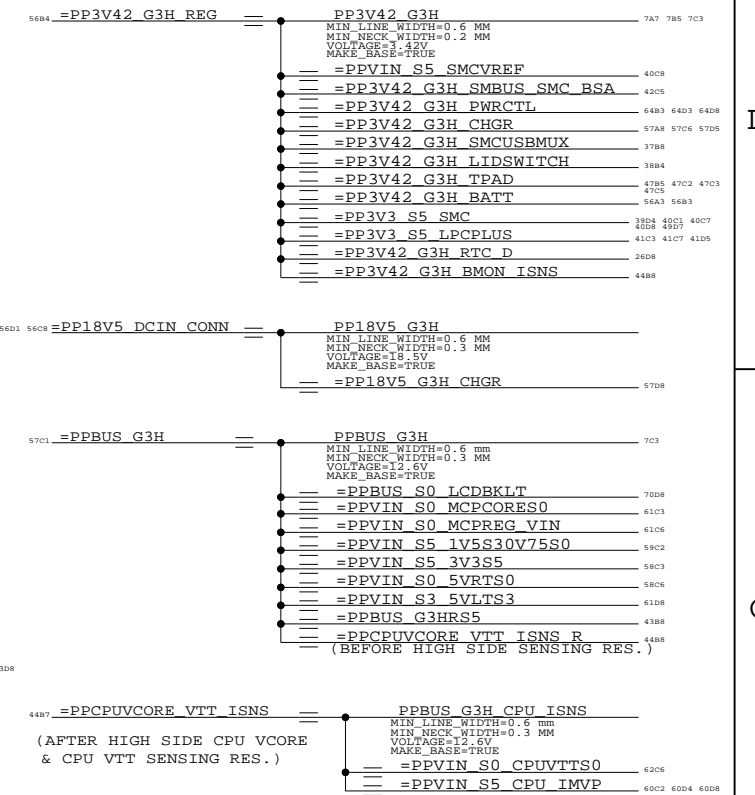
## "S3" RAILS



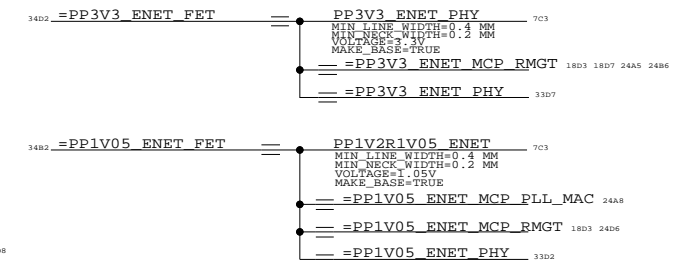
## "S5" RAILS



## "G3H" RAILS



## "ENET" RAILS

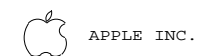


## Power Aliases

SYNC\_MASTER=BEN

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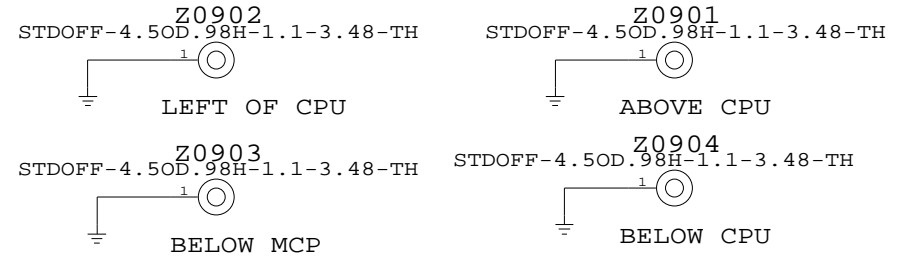
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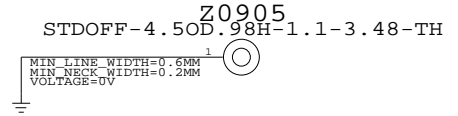
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SCALE	SHT	OF
NONE	8	109



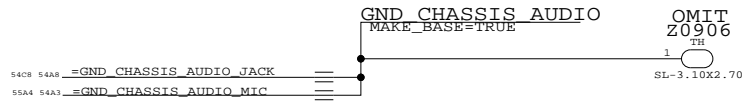
### HEATSINK STANDOFFS



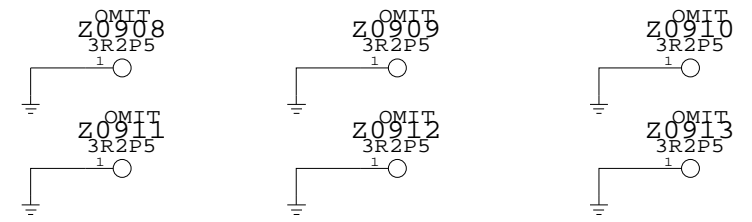
### FAN STANDOFF



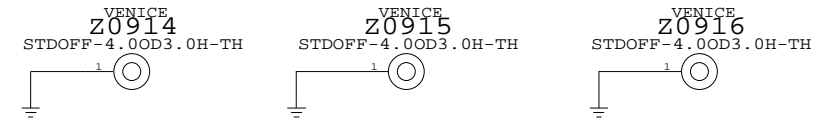
### AUDIO CHASSIS GND



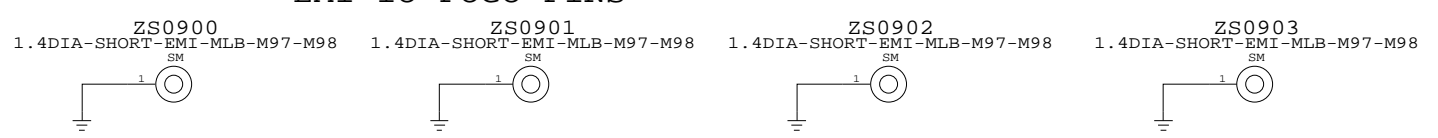
### MLB MOUNTING SCREW HOLES



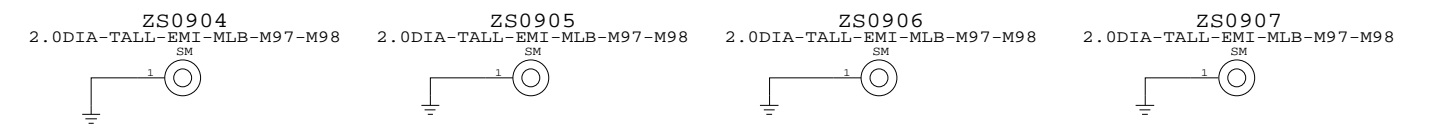
### VENICE BOARD STANDOFFS



### EMI IO POGO PINS



### EMI POGO PINS



### PCI-E ALIASES

UNUSED GPU LANES			
1706	=PEG D2R N<15:0>	==	NC PEG D2R N<15:0>
1706	=PEG D2R P<15:0>	==	NC PEG D2R P<15:0>
1703	=PEG R2D C N<15:0>	==	NC PEG R2D C N<15:0>
1703	=PEG R2D C P<15:0>	==	NC PEG R2D C P<15:0>
1706	PEG PRSNT L	==	TP PEG PRSNT L
1703	PEG CLK100M P	==	TP PEG CLK100M P
1703	PEG CLK100M N	==	TP PEG CLK100M N
UNUSED FW LANE			
1786	PCIE FW D2R P	==	TP PCIE FW D2R P
1786	PCIE FW D2R N	==	TP PCIE FW D2R N
1783	PCIE FW R2D C P	==	TP PCIE FW R2D C P
1783	PCIE FW R2D C N	==	TP PCIE FW R2D C N
1706	PCIE FW PRSNT L	==	TP PCIE FW PRSNT L
1706	FW CLKREQ L	==	TP FW CLKREQ L
1703	PCIE CLK100M FW P	==	TP PCIE CLK100M FW P
1703	PCIE CLK100M FW N	==	TP PCIE CLK100M FW N
UNUSED EXPRESS CARD LANE			
1784	PCIE EXCARD D2R P	==	TP PCIE EXCARD D2R P
1784	PCIE EXCARD D2R N	==	TP PCIE EXCARD D2R N
1783	PCIE EXCARD R2D C P	==	TP PCIE EXCARD R2D C P
1783	PCIE EXCARD R2D C N	==	TP PCIE EXCARD R2D C N
1706	PCIE EXCARD PRSNT L	==	TP PCIE EXCARD PRSNT L
1706	EXCARD CLKREQ L	==	TP EXCARD CLKREQ L
1703	PCIE CLK100M EXCARD P	==	TP PCIE CLK100M EXCARD P
1703	PCIE CLK100M EXCARD N	==	TP PCIE CLK100M EXCARD N

AIRPORT CARD PRESENT SIGNAL (WRONG ALIAS, REMOVE AT NEXT BOARD SPIN)

FOR VENICE CARD			
1706	TP PE4 CLKREQ L	==	FC CLKREQ L
1706	TP PE4 PRSNT L	==	FC PRSNT L
1703	TP PCIE CLK100M PE4P	==	PCIE CLK100M FC P
1703	TP PCIE CLK100M PE4N	==	PCIE CLK100M FC N
1786	TP PCIE PE4 D2RP	==	PCIE FC D2R P
1786	TP PCIE PE4 D2RN	==	PCIE FC D2R N
1783	TP PCIE PE4 R2D CP	==	PCIE FC R2D C P
1783	TP PCIE PE4 R2D CN	==	PCIE FC R2D C N

### USB ALIASES

UNUSED USB PORTS			
2003	USB EXTC P	==	TP USB EXTC P
2003	USB EXTC N	==	TP USB EXTC N
2003	USB EXTD P	==	TP USB EXTD P
2003	USB EXTD N	==	TP USB EXTD N
2003	USB EXCARD P	==	TP USB EXCARD P
2003	USB EXCARD N	==	TP USB EXCARD N
2003	USB MINI P	==	TP USB MINI P
2003	USB MINI N	==	TP USB MINI N

### DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE			
1806	MCP TV DAC RSET	==	NC MCP TV DAC RSET
1806	MCP TV DAC VREF	==	NC MCP TV DAC VREF
1806	MCP CLK27M XTALIN	==	NC MCP CLK27M XTALIN
1806	MCP CLK27M XTALOUT	==	NC MCP CLK27M XTALOUT
1803	CRT IG R C PR	==	NC CRT IG R C PR
1803	CRT IG G Y Y	==	NC CRT IG G Y Y
1803	CRT IG B COMP PB	==	NC CRT IG B COMP PB
1803	CRT IG HSYNC	==	NC CRT IG HSYNC
1803	CRT IG VSYNC	==	NC CRT IG VSYNC

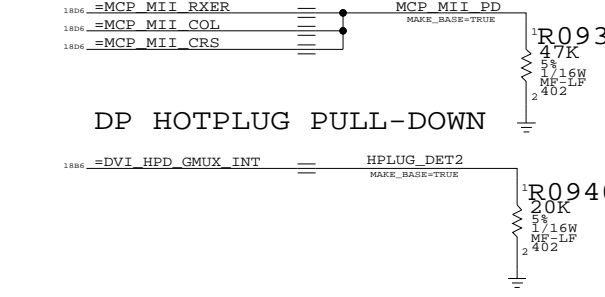
### LVDS ALIASES

UNUSED LVDS SIGNALS			
1883	LVDS IG A DATA P<3>	==	NC LVDS IG A DATA P3
1883	LVDS IG A DATA N<3>	==	NC LVDS IG A DATA N3
1883	LVDS IG B CLK P	==	NC LVDS IG B CLK P
1883	LVDS IG B CLK N	==	NC LVDS IG B CLK N
1883	LVDS IG B DATA P<3:0>	==	NC LVDS IG B DATA P<3:0>
1883	LVDS IG B DATA N<3:0>	==	NC LVDS IG B DATA N<3:0>

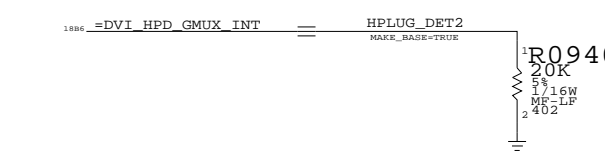
### MISC MCP79 ALIASES

1486	CPU PECCI MCP	==	TP CPU PECCI MCP
1987	FW PME L	==	TP FW PME L
1786	GMUX JTAG TCK L	==	TP GMUX JTAG TCK L
1786	GMUX JTAG TDO	==	TP GMUX JTAG TDO
1904	GMUX JTAG TDI	==	TP GMUX JTAG TDI
1904	GMUX JTAG TMS	==	TP GMUX JTAG TMS

### LAN ALIASES



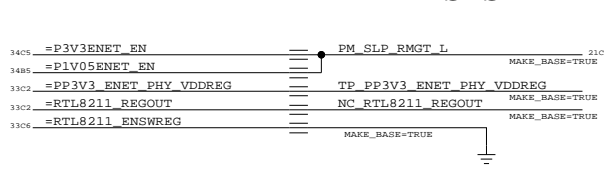
### DP HOTPLUG PULL-DOWN



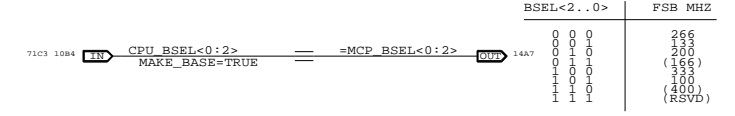
### SO-DIMM ALIASES

UNUSED ADDRESS PINS			
2805	MEM A A<15>	==	TP MEM A A15
2905	MEM B A<15>	==	TP MEM B A15

### ETHERNET ALIASES

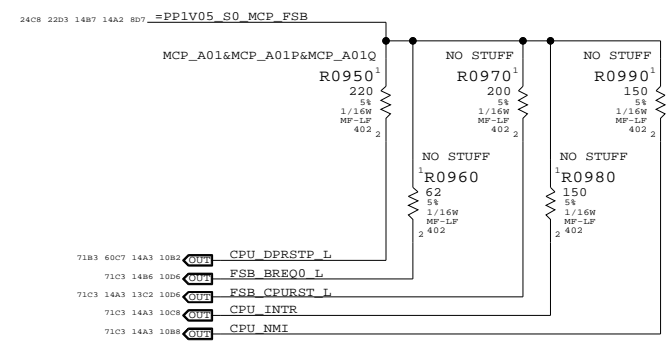


### CPU FSB FREQUENCY STRAPS



### Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA. If found to be necessary, will move to page14.csa



### SIGNAL ALIAS

SYNC\_MASTER=M97\_MLB

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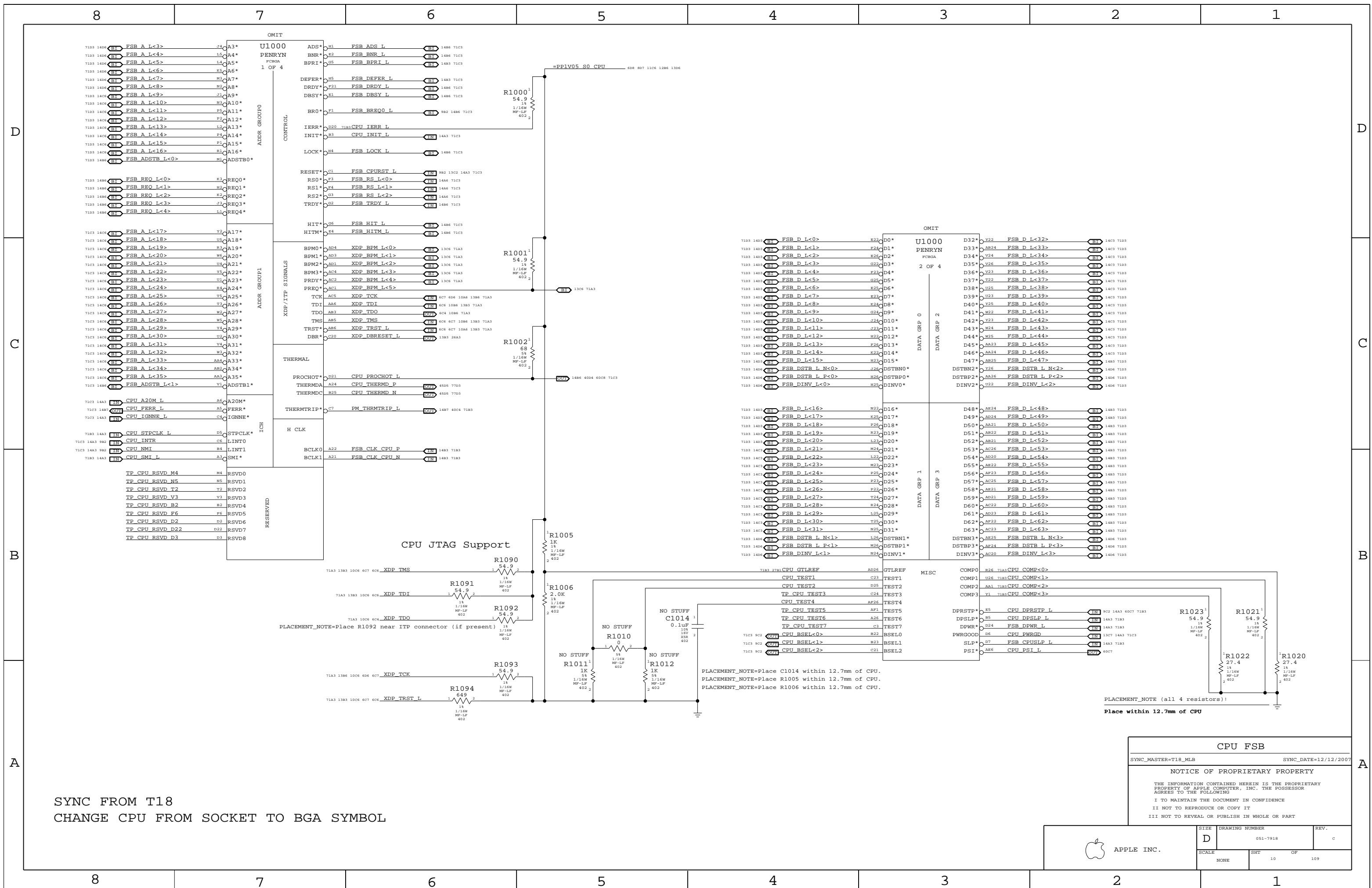
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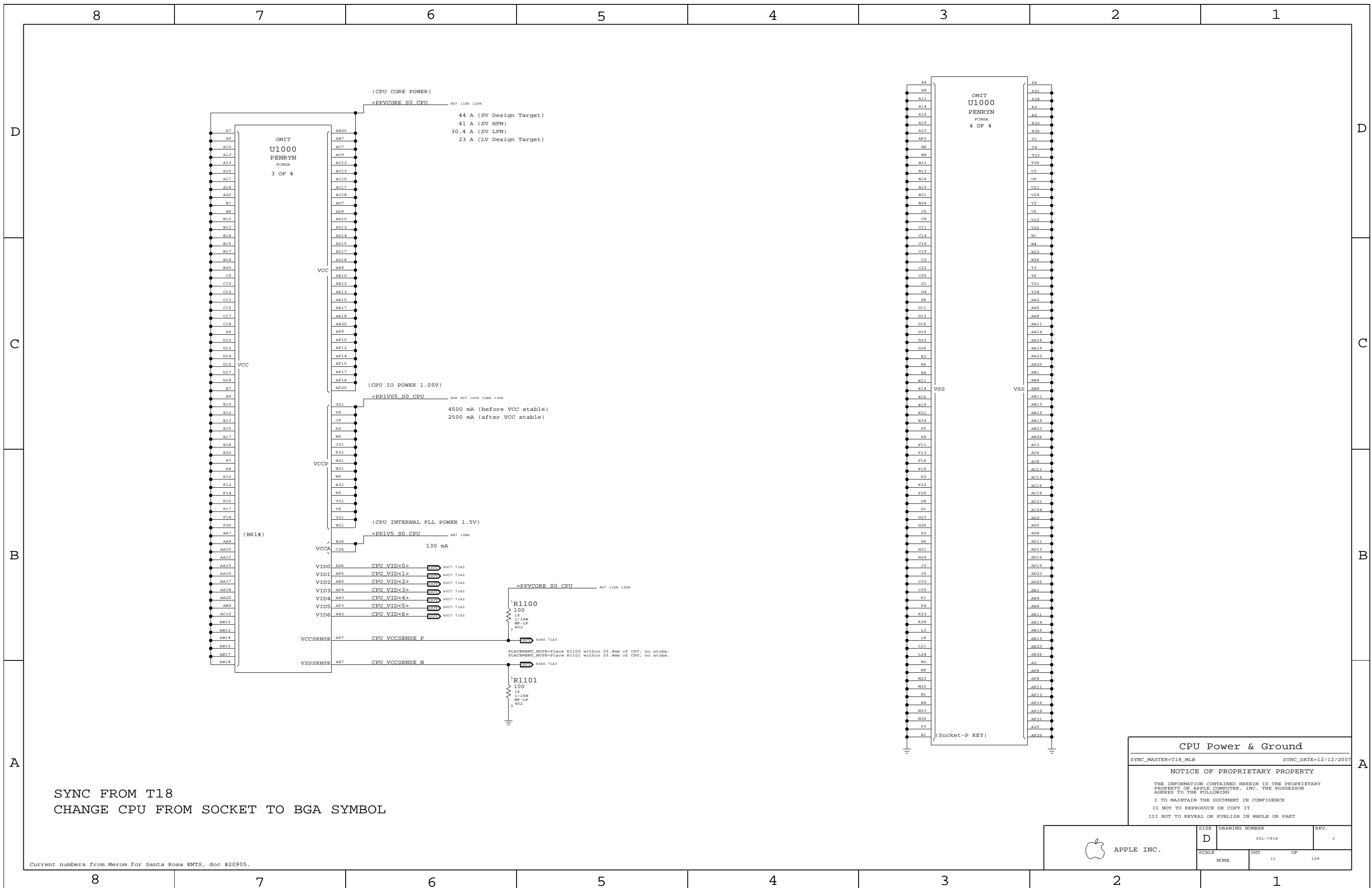
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	9	109



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

**CPU FSB**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007  
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SCALE	NONE	SHT	OF 109



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

**CPU Power & Ground**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007

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SCALE	SHT	OF	REV.
NONE	11	109	

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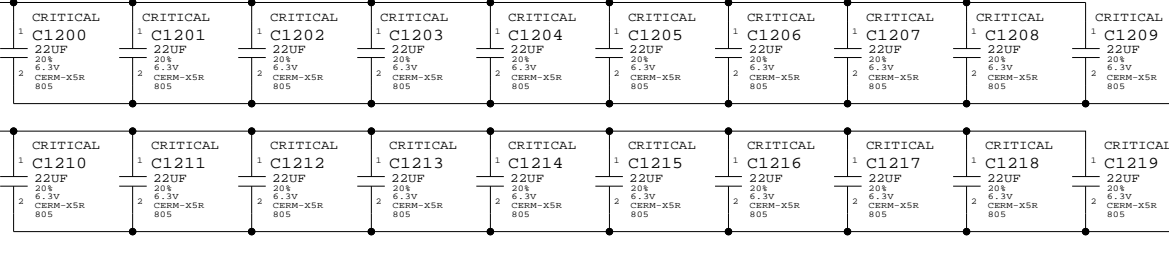
### CPU VCore HF and Bulk Decoupling

4X 330UF, 20X 22UF 0805

1106 1185 807=PPVCORE\_S0\_CPU

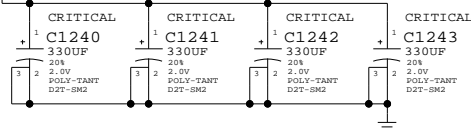
PLACEMENT\_NOTE (C1200-C1219):

Place inside socket cavity on secondary side.



PLACEMENT\_NOTE (C1240-C1243):

Place on secondary side.

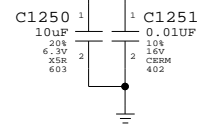


### VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

1186 807=PP1V5\_S0\_CPU

PLACEMENT\_NOTE=Place C1281 near CPU pin B26.

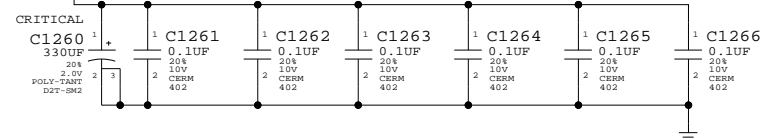


### VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

1106 1106 1005 807 608=PP1V05\_S0\_CPU

PLACEMENT\_NOTE=Place C1260 between CPU & NB.



SYNC FROM T18  
 REMOVE NO STUFF CAPS C1220 TO C1231  
 REMOVE C1244 & C1245  
 CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

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### CPU Decoupling

SYNC\_MASTER=RAYMOND

SYNC\_DATE=03/31/2008

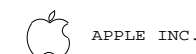
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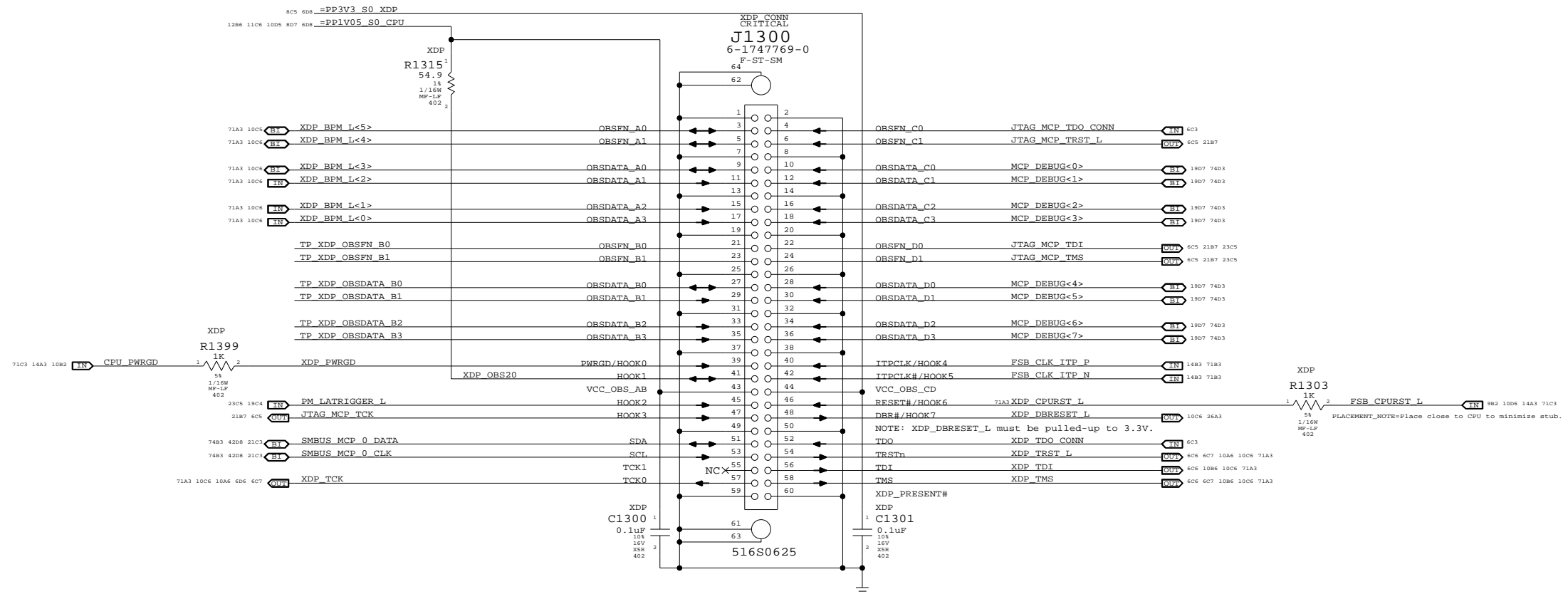
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NONE	12	109

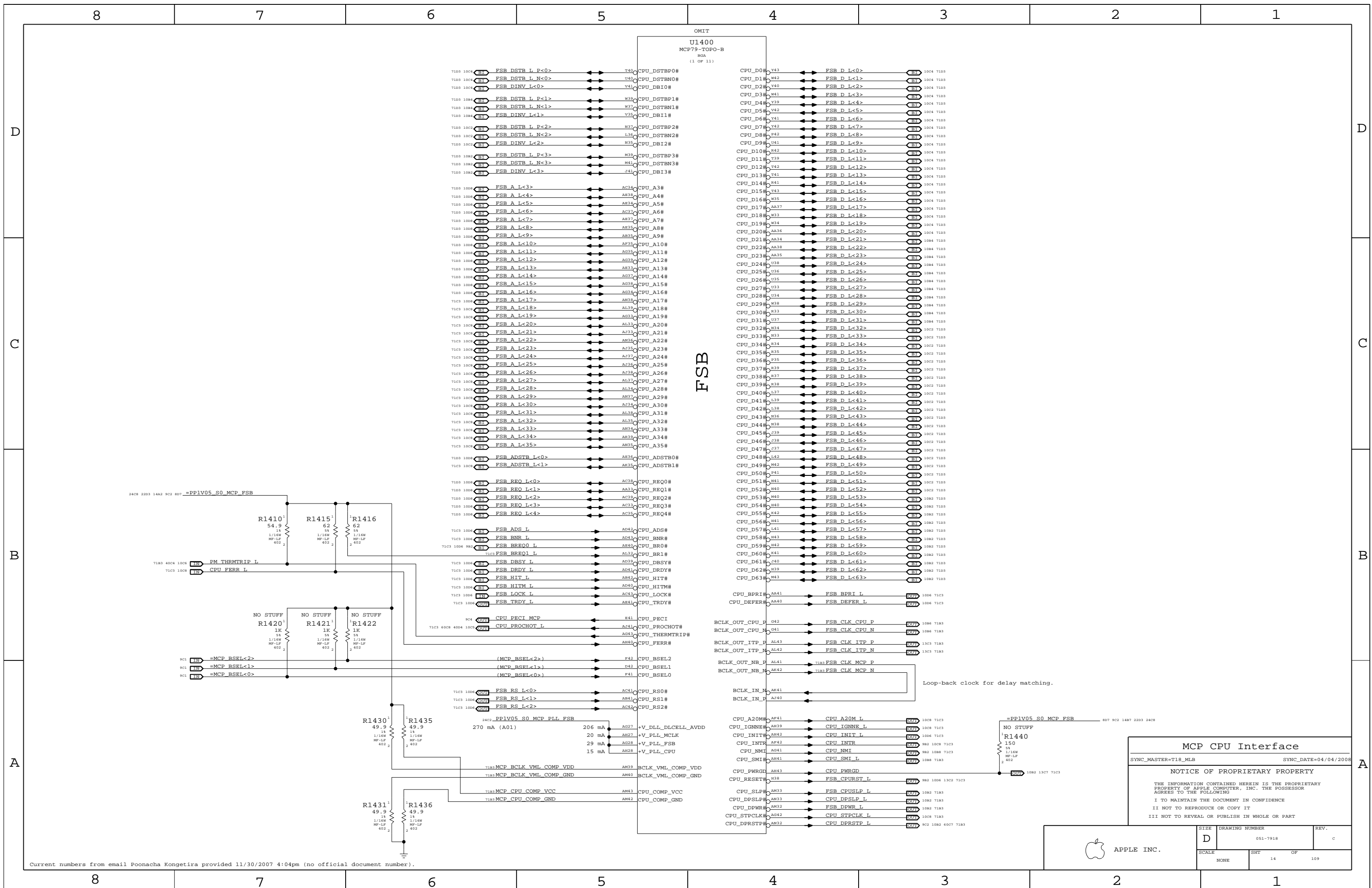
### MCP79-specific pinout



SYNC FROM T18  
 CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625  
 RENAME JTAG\_MCP\_TDO TO JTAG\_MCP\_TDO\_CONN  
 RENAME XDP\_TDO TO XDP\_TDO\_CONN

eXtended Debug Port (XDP)  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007  
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	SCALE NONE	SHEETS 13	OF 109



U1400  
MCP79-TOPO-B  
BGA  
(1 OF 11)

7103 1004	FSB DSTB L P<0>	T10	CPU_DSTBP0#
7103 1004	FSB DSTB L N<0>	U40	CPU_DSTBN0#
7103 1004	FSB DINV L<0>	V41	CPU_DBI0#
7103 1084	FSB DSTB L P<1>	W39	CPU_DSTBP1#
7103 1084	FSB DSTB L N<1>	W17	CPU_DSTBN1#
7103 1084	FSB DINV L<1>	V15	CPU_DBI1#
7103 1002	FSB DSTB L P<2>	N37	CPU_DSTBP2#
7103 1002	FSB DSTB L N<2>	L16	CPU_DSTBN2#
7103 1002	FSB DINV L<2>	W15	CPU_DBI2#
7103 1082	FSB DSTB L P<3>	M39	CPU_DSTBP3#
7103 1082	FSB DSTB L N<3>	M41	CPU_DSTBN3#
7103 1082	FSB DINV L<3>	J41	CPU_DBI3#
7103 1008	FSB A L<3>	AC34	CPU_A3#
7103 1008	FSB A L<4>	AE18	CPU_A4#
7103 1008	FSB A L<5>	AE14	CPU_A5#
7103 1008	FSB A L<6>	AC17	CPU_A6#
7103 1008	FSB A L<7>	AE37	CPU_A7#
7103 1008	FSB A L<8>	AE35	CPU_A8#
7103 1008	FSB A L<9>	AE15	CPU_A9#
7103 1008	FSB A L<10>	AE16	CPU_A10#
7103 1008	FSB A L<11>	AG15	CPU_A11#
7103 1008	FSB A L<12>	AG19	CPU_A12#
7103 1008	FSB A L<13>	AE33	CPU_A13#
7103 1008	FSB A L<14>	AG37	CPU_A14#
7103 1008	FSB A L<15>	AG18	CPU_A15#
7103 1008	FSB A L<16>	AG14	CPU_A16#
7103 1008	FSB A L<17>	AE18	CPU_A17#
7103 1008	FSB A L<18>	AL39	CPU_A18#
7103 1008	FSB A L<19>	AG33	CPU_A19#
7103 1008	FSB A L<20>	AL33	CPU_A20#
7103 1008	FSB A L<21>	AL33	CPU_A21#
7103 1008	FSB A L<22>	AL16	CPU_A22#
7103 1008	FSB A L<23>	AJ35	CPU_A23#
7103 1008	FSB A L<24>	AJ37	CPU_A24#
7103 1008	FSB A L<25>	AJ36	CPU_A25#
7103 1008	FSB A L<26>	AJ18	CPU_A26#
7103 1008	FSB A L<27>	AL37	CPU_A27#
7103 1008	FSB A L<28>	AL34	CPU_A28#
7103 1008	FSB A L<29>	AN37	CPU_A29#
7103 1008	FSB A L<30>	AJ34	CPU_A30#
7103 1008	FSB A L<31>	AL18	CPU_A31#
7103 1008	FSB A L<32>	AL15	CPU_A32#
7103 1008	FSB A L<33>	AN14	CPU_A33#
7103 1008	FSB A L<34>	AN14	CPU_A34#
7103 1008	FSB A L<35>	AN35	CPU_A35#
7103 1008	FSB ADSTB L<0>	AE16	CPU_ADSTB0#
7103 1008	FSB ADSTB L<1>	AE15	CPU_ADSTB1#
7103 1008	FSB REQ L<0>	AC18	CPU_REQ0#
7103 1008	FSB REQ L<1>	AA33	CPU_REQ1#
7103 1008	FSB REQ L<2>	AC19	CPU_REQ2#
7103 1008	FSB REQ L<3>	AC13	CPU_REQ3#
7103 1008	FSB REQ L<4>	AC35	CPU_REQ4#
7103 1004	FSB ADS L	AD42	CPU_ADS#
7103 1004	FSB BNR L	AD43	CPU_BNR#
7103 1004	FSB BREQ0 L	AE40	CPU_BR0#
7103 1004	FSB BREQ1 L	AE42	CPU_BR1#
7103 1004	FSB DBSY L	AD39	CPU_DBSY#
7103 1004	FSB DRDY L	AD41	CPU_DRDY#
7103 1004	FSB HIT L	AD42	CPU_HIT#
7103 1004	FSB HITM L	AD40	CPU_HITM#
7103 1004	FSB LOCK L	AC43	CPU_LOCK#
7103 1004	FSB TRDY L	AE41	CPU_TRDY#
804	CPU PECCI MCP	K41	CPU_PECCI
7103 4008 4004 1004	CPU PROCHOT L	AJ41	CPU_PROCHOT#
		AG43	CPU_THERMTRIP#
		AM40	CPU_FERR#
	(MCP_BSEL<2>)	F42	CPU_BSEL2
	(MCP_BSEL<1>)	D42	CPU_BSEL1
	(MCP_BSEL<0>)	F41	CPU_BSEL0
7103 1004	FSB RS L<0>	AC41	CPU_RS0#
7103 1004	FSB RS L<1>	AM41	CPU_RS1#
7103 1004	FSB RS L<2>	AC42	CPU_RS2#
2403	PP1V05_S0 MCP PLL FSB		
	270 mA (A01)	AG27	+V_DLL_DLCELL_AVDD
	206 mA	AM27	+V_PLL_MCLK
	29 mA	AG28	+V_PLL_FSB
	15 mA	AM28	+V_PLL_CPU
7103	MCP BCLK VML COMP VDD	AM39	BCLK_VML_COMP_VDD
7103	MCP BCLK VML COMP GND	AM40	BCLK_VML_COMP_GND
7103	MCP CPU COMP VCC	AM43	CPU_COMP_VCC
7103	MCP CPU COMP GND	AM42	CPU_COMP_GND

FSB

Loop-back clock for delay matching.

**MCP CPU Interface**

SYNC\_MASTER=TI8\_MLB      SYNC\_DATE=04/04/2008

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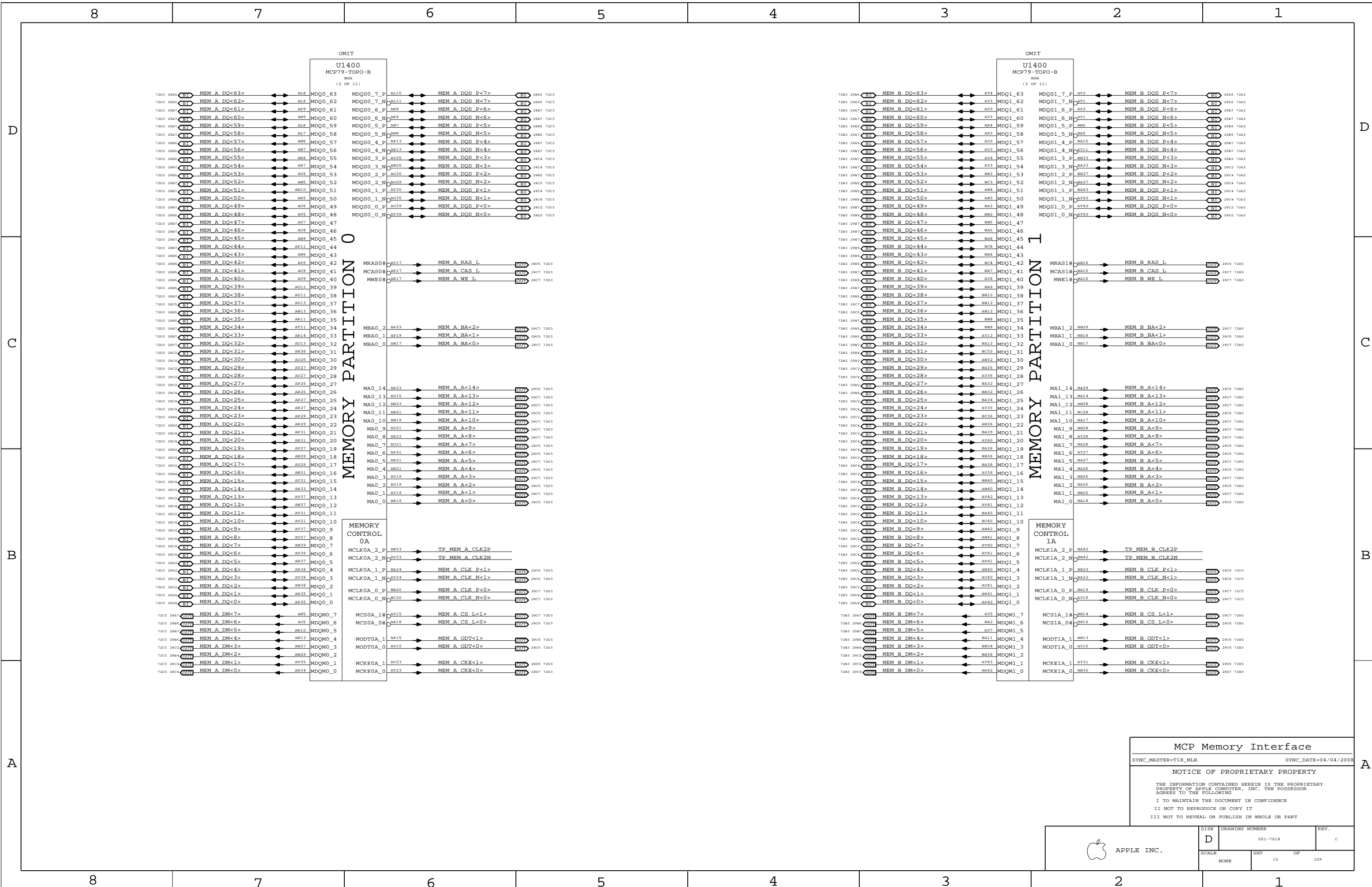
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NONE	14		

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**MCP Memory Interface**

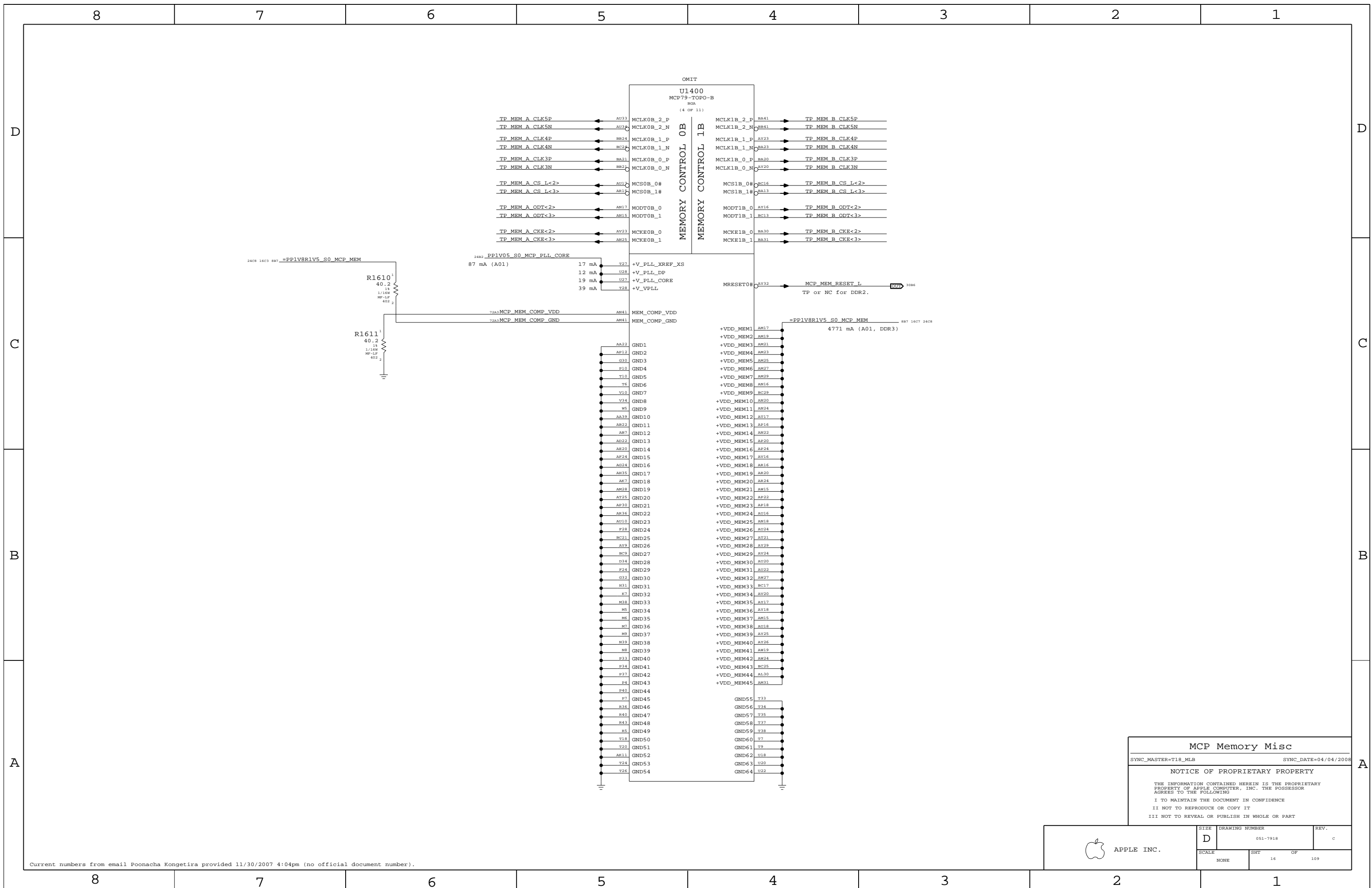
SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHEET 15	OF 109



**MCP Memory Misc**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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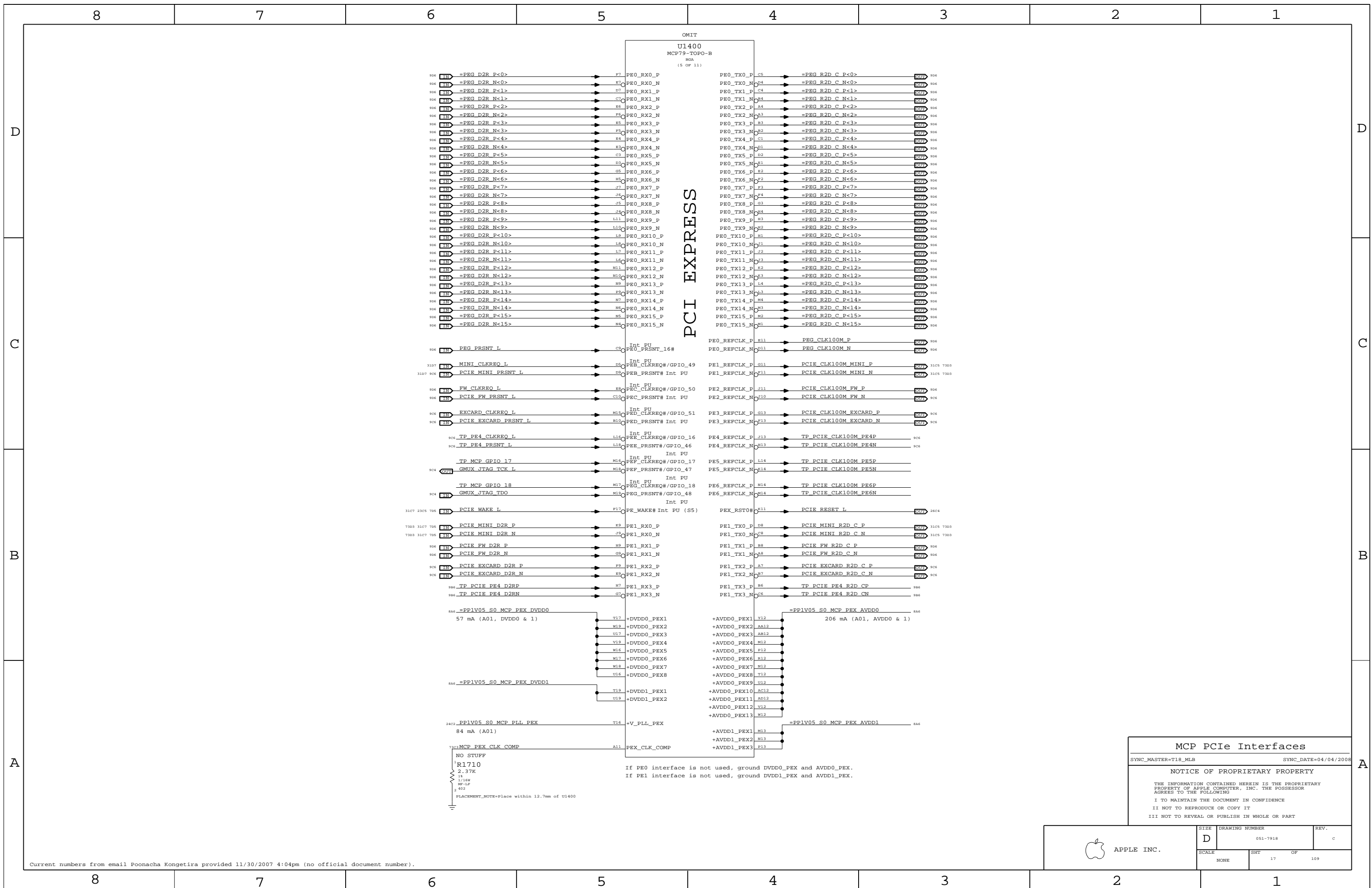
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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7918	REV. c
	SCALE NONE	SHEETS 16	OF 109

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**MCP PCIe Interfaces**

SYNC\_MASTER=TI8\_MLB      SYNC\_DATE=04/04/2008

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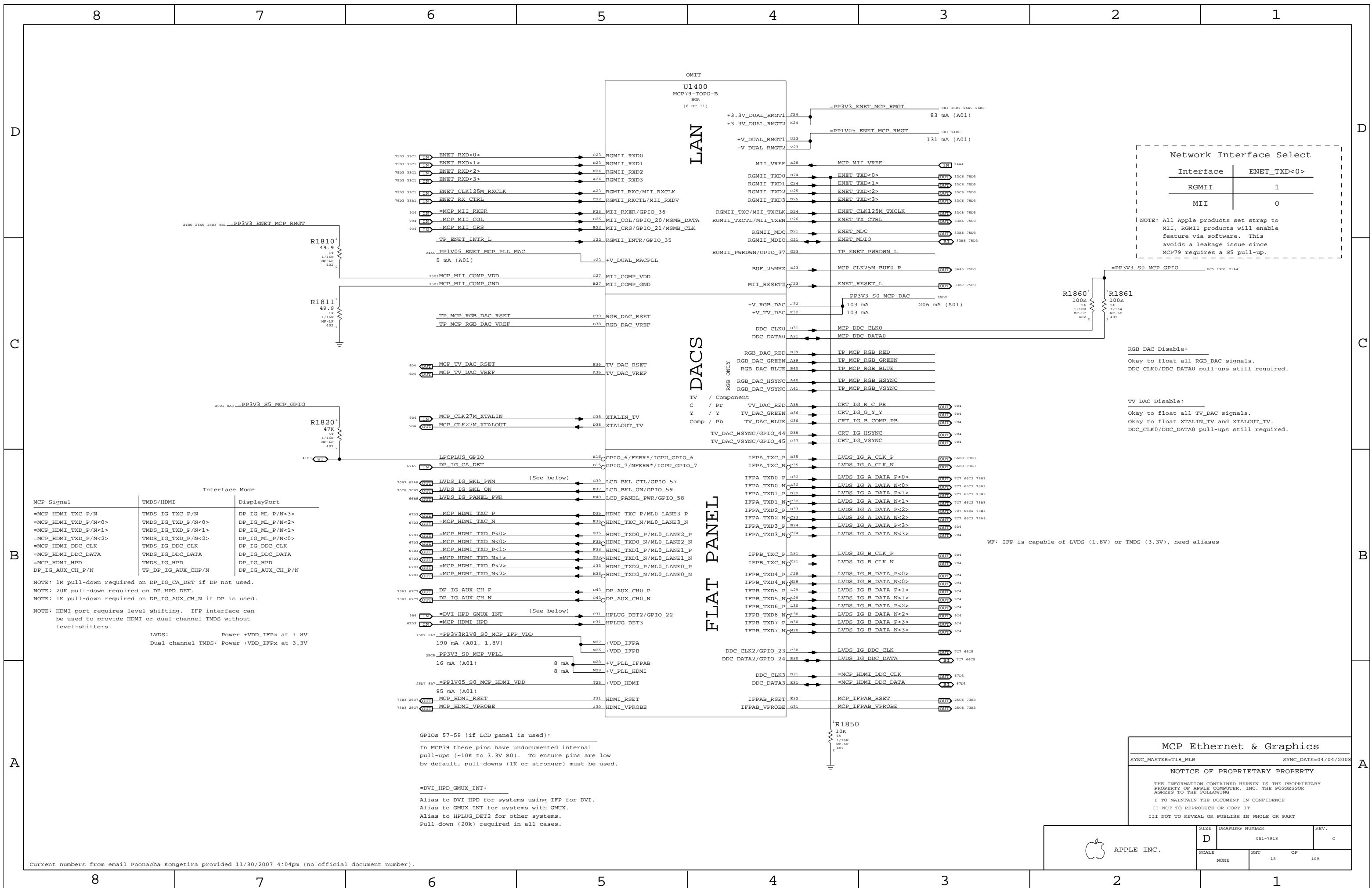
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	D	051-7918	C
SCALE	SHT	OF	109
NONE	17		

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Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: \_\_\_\_\_  
 Okay to float all RGB\_DAC signals.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable: \_\_\_\_\_  
 Okay to float all TV\_DAC signals.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

MCP Signal	Interface Mode	
	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
 NOTE: 20K pull-down required on DP\_HPD\_DET.  
 NOTE: 1K pull-down required on DP\_IG\_AUX\_CH\_N if DP is used.  
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD\_IPFx at 1.8V  
 Dual-channel TMDS: Power +VDD\_IPFx at 3.3V

GPIOs 57-59 (if LCD panel is used):  
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI\_HPD\_GMUX\_INT:  
 Alias to DVI\_HPD for systems using IFP for DVI.  
 Alias to GMUX\_INT for systems with GMUX.  
 Alias to HPLUG\_DET2 for other systems.  
 Pull-down (20k) required in all cases.

**MCP Ethernet & Graphics**

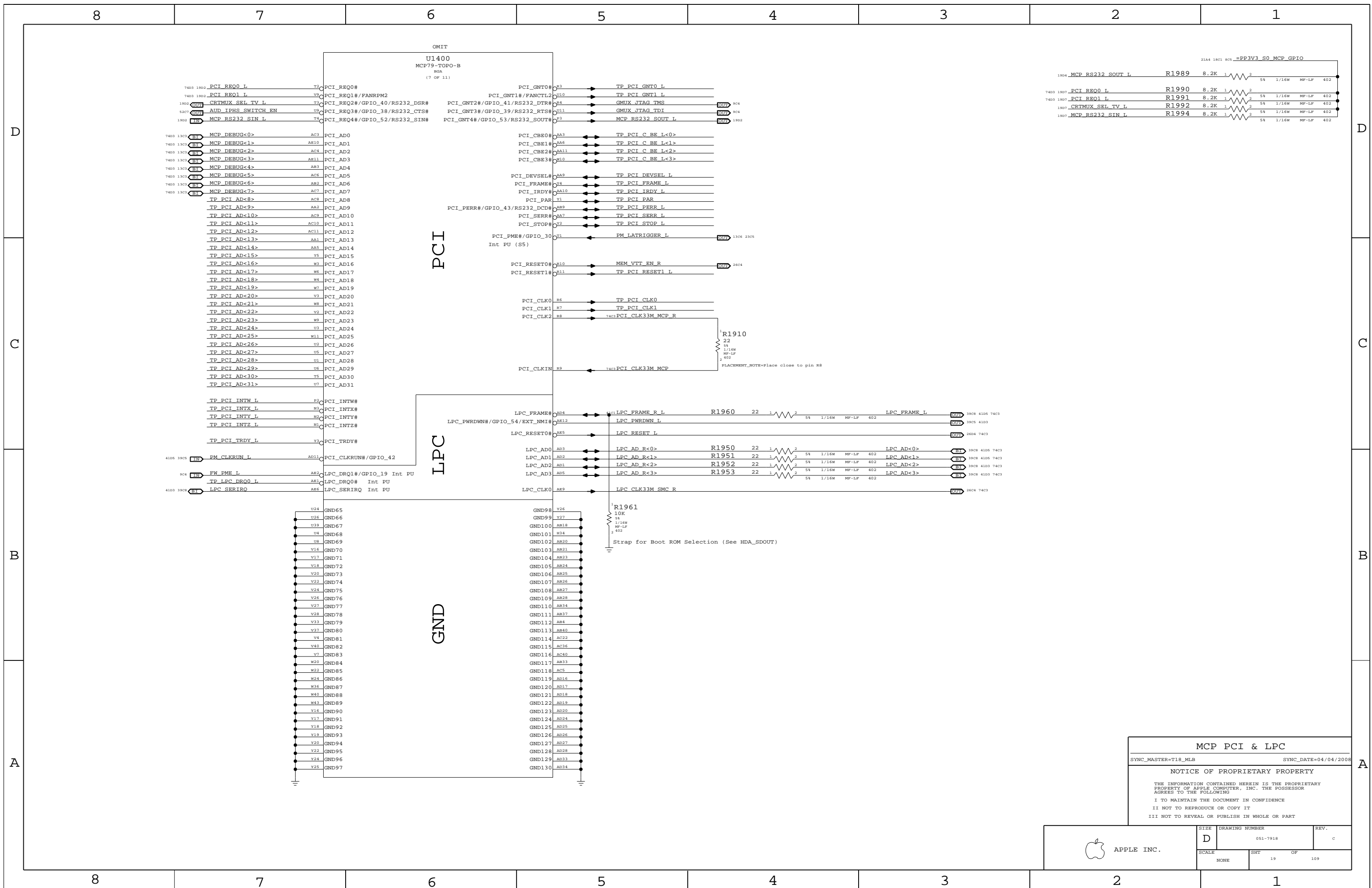
SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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	D	051-7918	C
SCALE	SHT	OF	109
NONE	18		



**MCP PCI & LPC**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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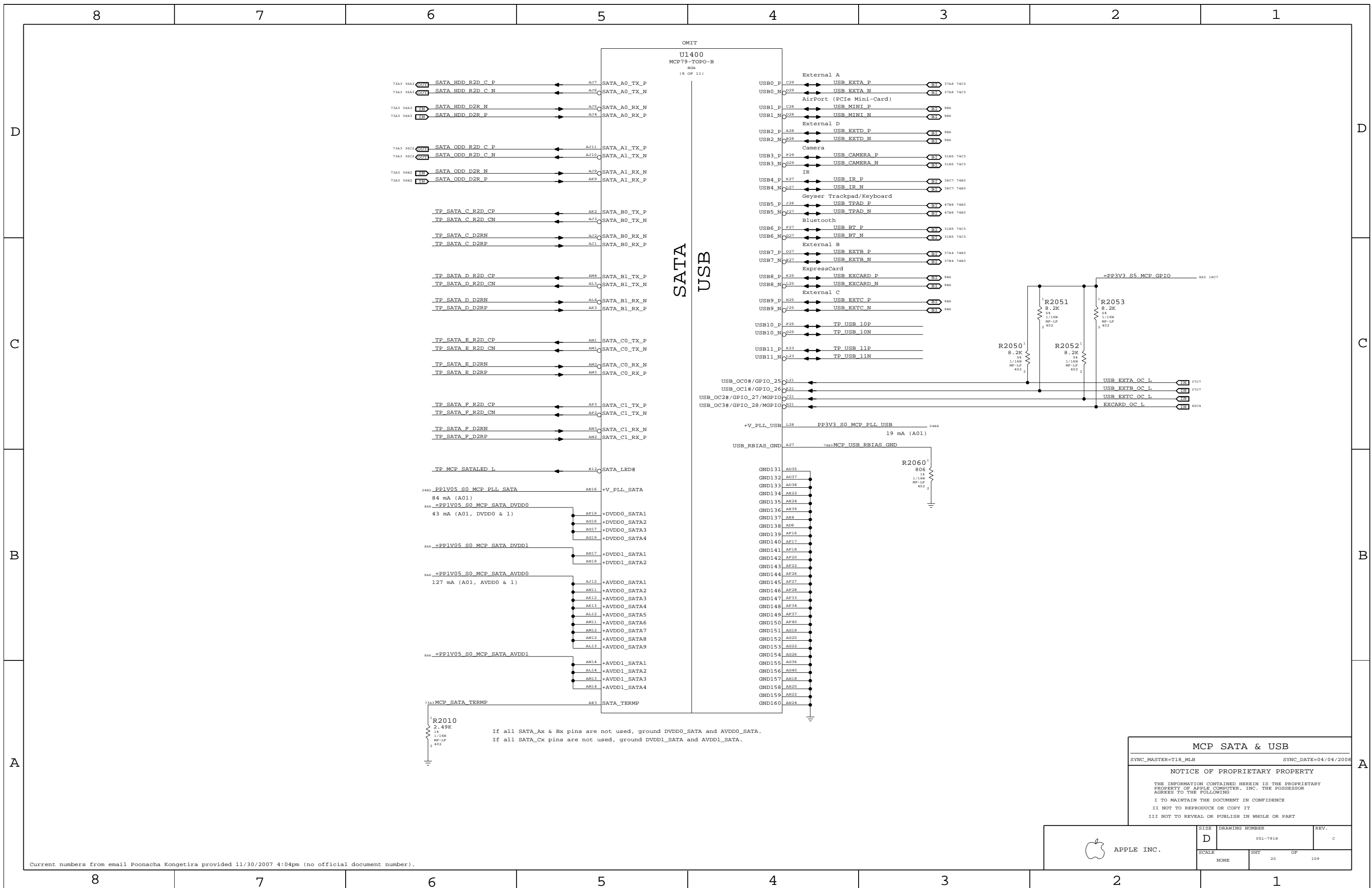
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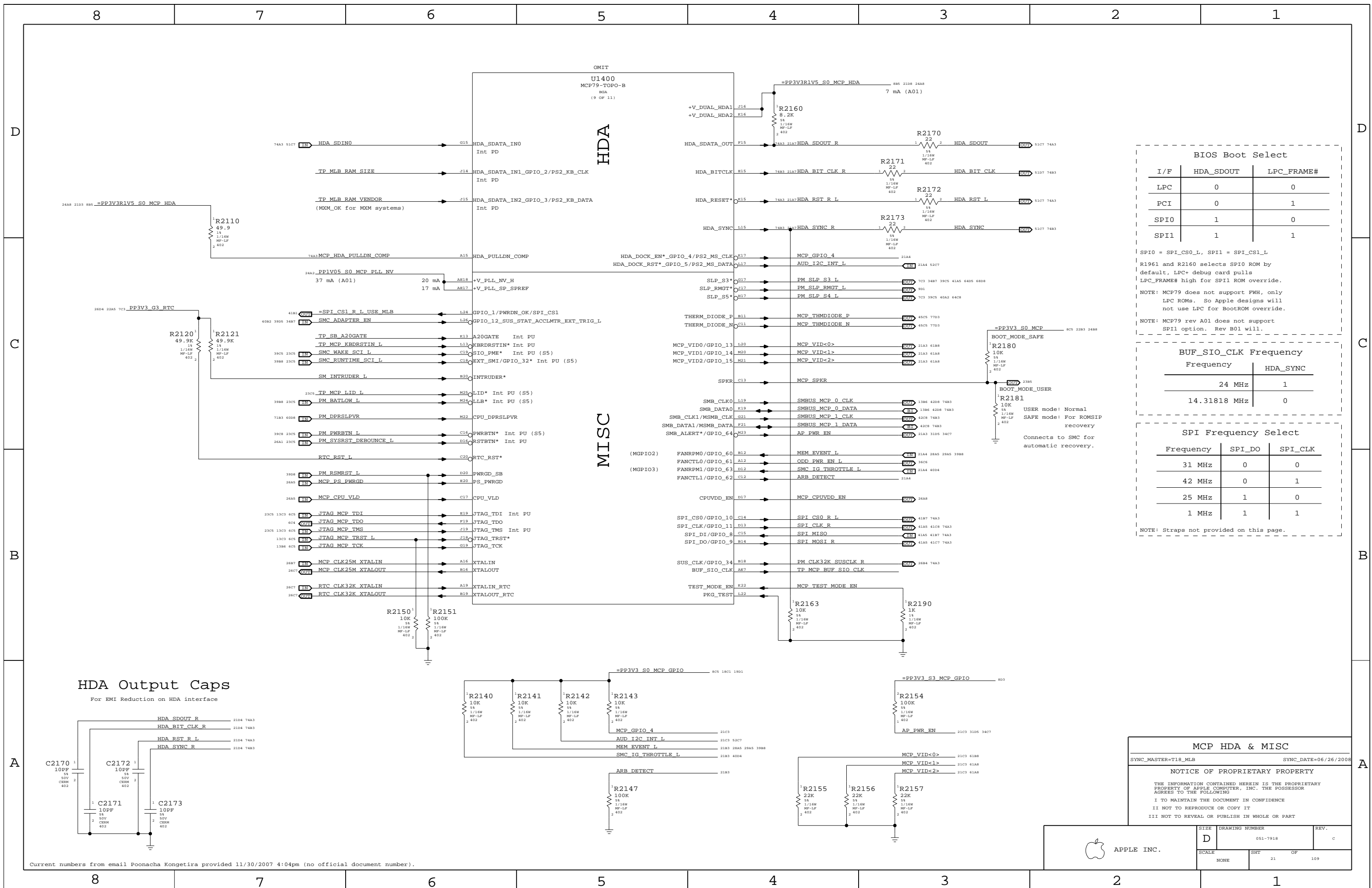
APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHEET 19	OF 109



If all SATA\_Ax & Bx pins are not used, ground DVDD0\_SATA and AVDD0\_SATA.  
 If all SATA\_Cx pins are not used, ground DVDD1\_SATA and AVDD1\_SATA.

**MCP SATA & USB**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	20		



BIOS Boot Select

I/F	HDA_SDOUR	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L  
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.  
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.  
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF\_SIO\_CLK Frequency

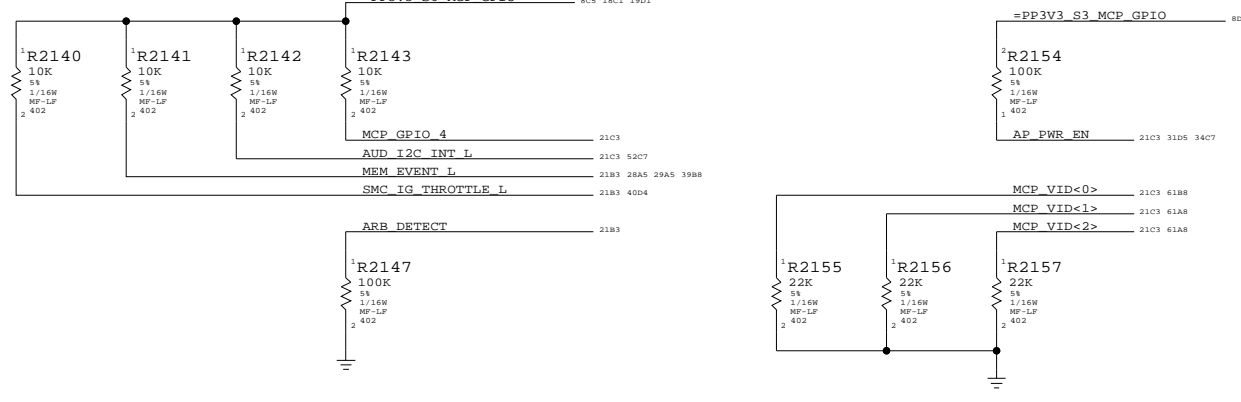
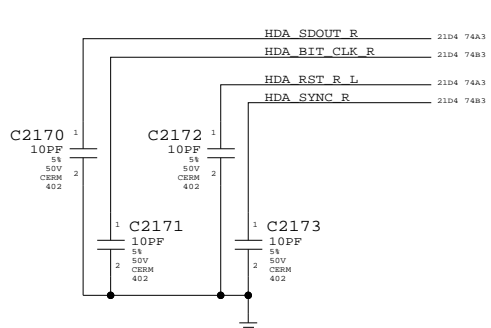
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

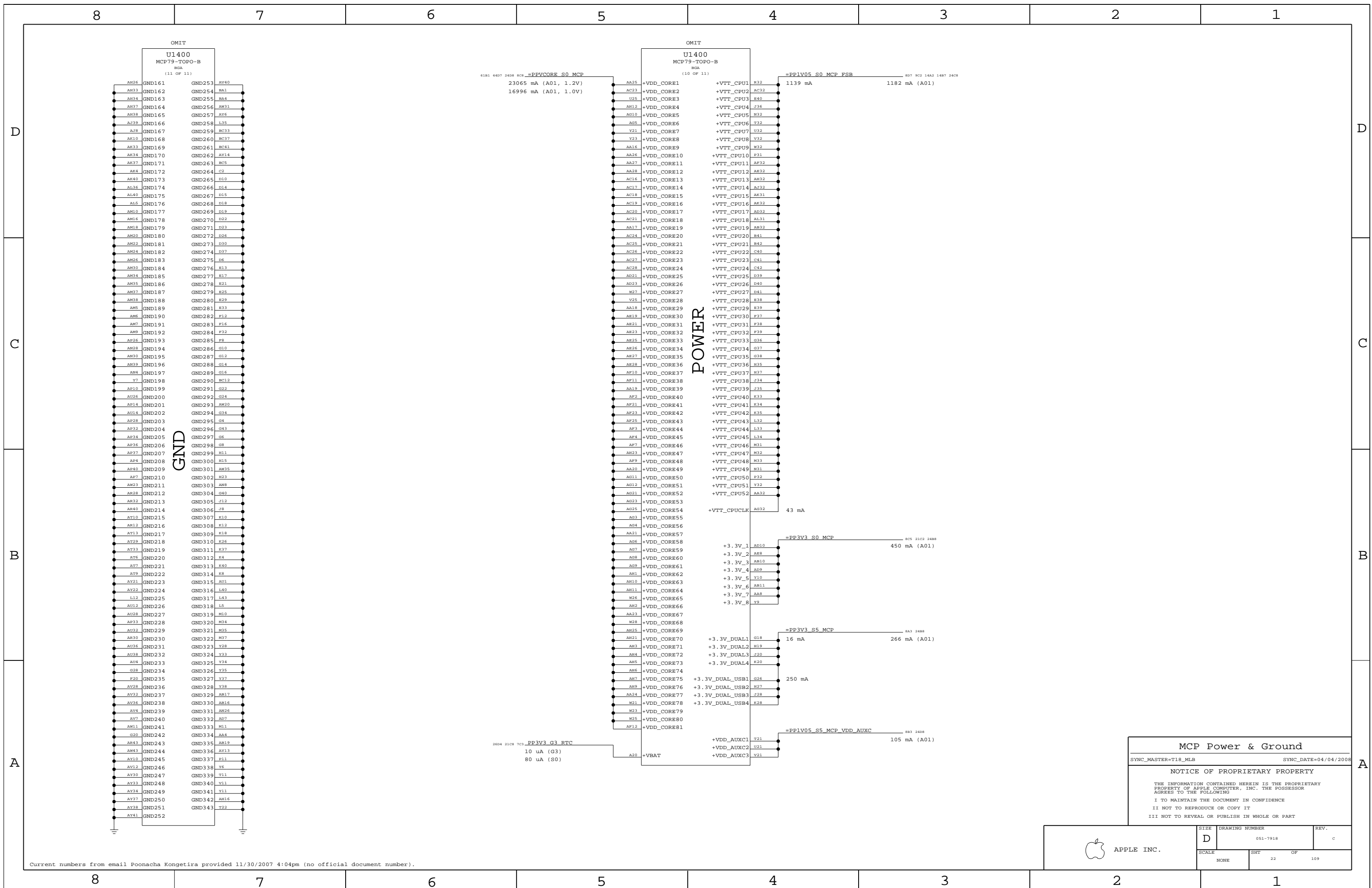
HDA Output Caps  
 For EMI Reduction on HDA interface



MCP HDA & MISC  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=06/26/2008  
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APPLE INC.  
 DRAWING NUMBER: 051-7918  
 SCALE: NONE  
 SHEET: 21 OF 109

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MCP Power & Ground

SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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	D	051-7918	c
SCALE	SHT	OF	REV.
NONE	22	109	

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8

7

6

5

4

3

2

1

D

D

C

C

B

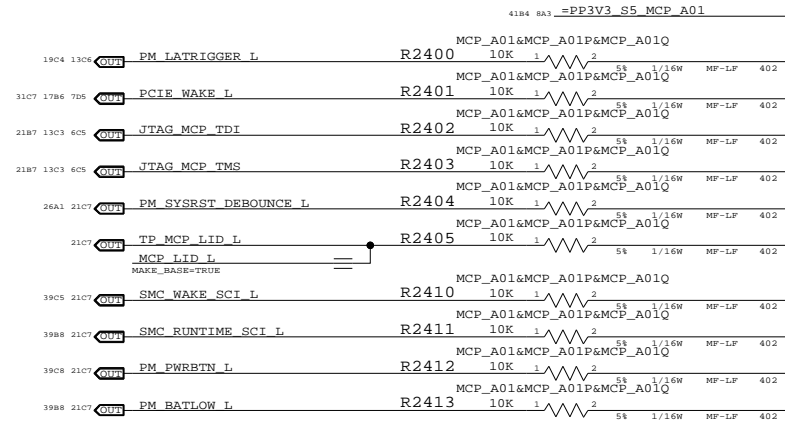
B

A

A

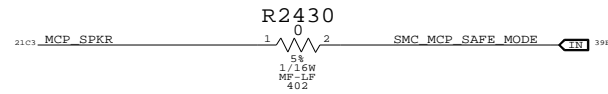
### 3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



### MCP\_SAFE\_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345



#### MCP79 A01 Silicon Support

SYNC\_MASTER=T18\_MLB SYNC\_DATE=03/08/2008

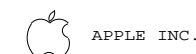
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	24	109

8

7

6

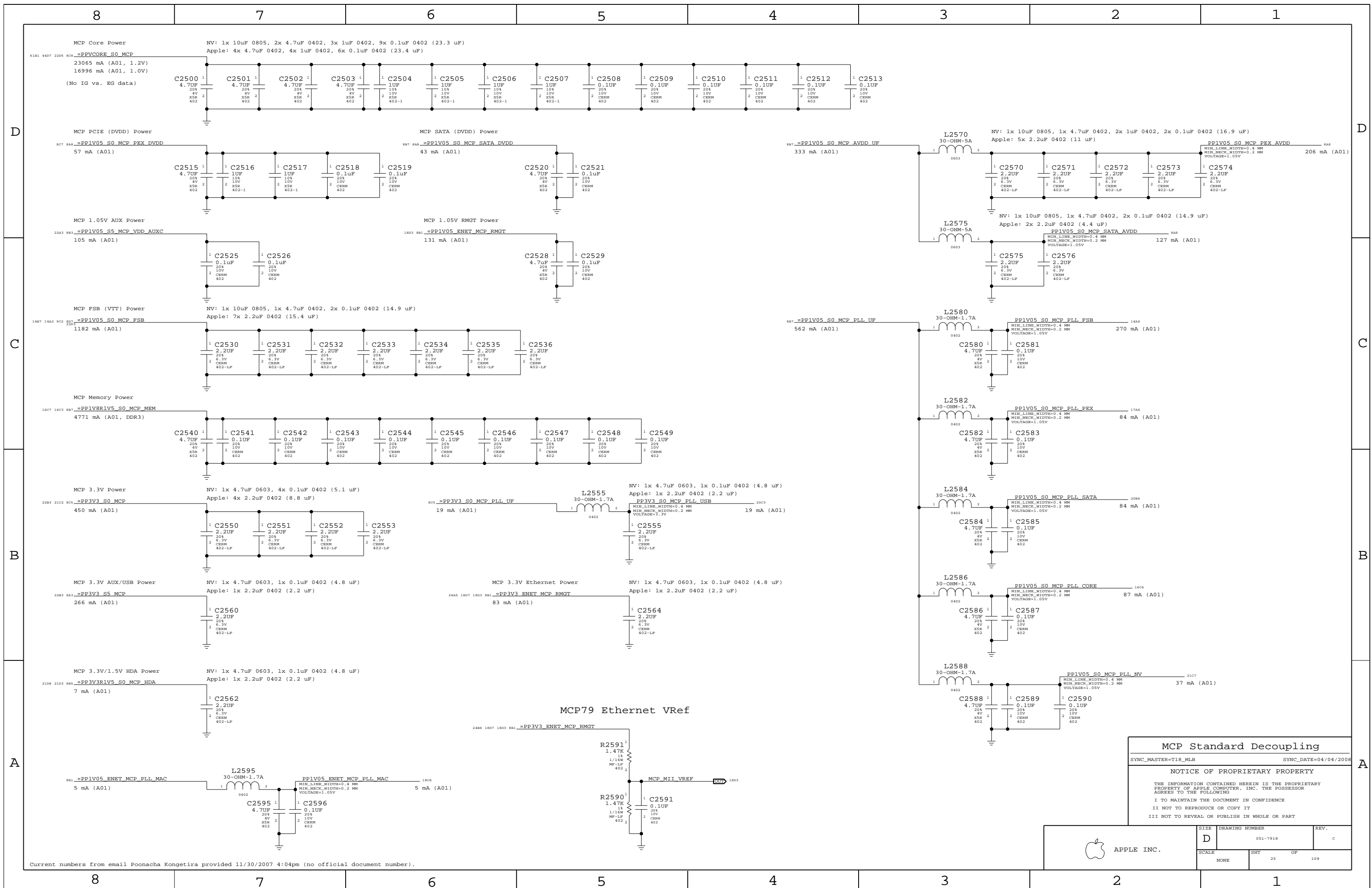
5

4

3

2

1



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**MCP Standard Decoupling**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008  
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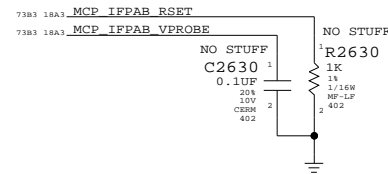
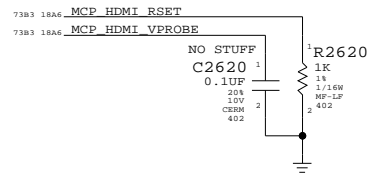
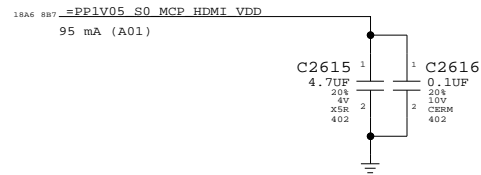
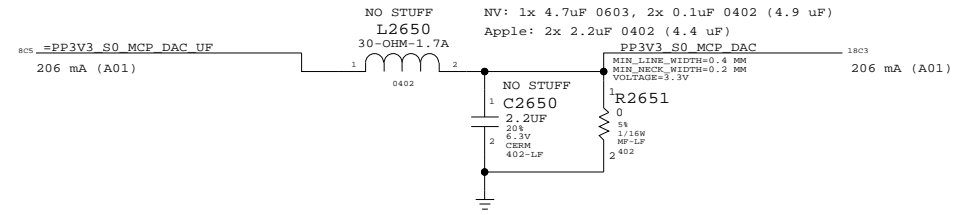
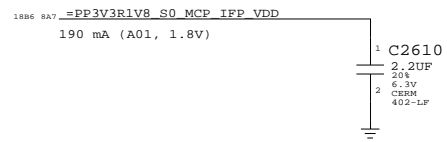
SCALE	DRAWING NUMBER		REV.
	D	051-7918	
NONE	SHT	OF	109



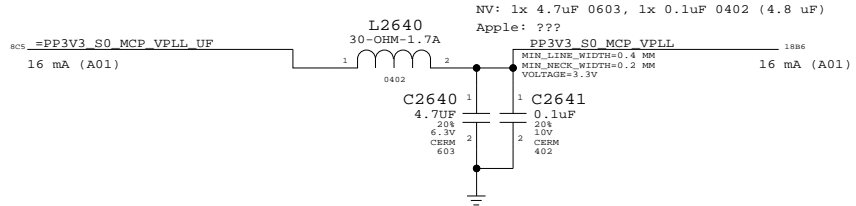


WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
 Apple: 1x 2.2uF 0402 (2.2 uF)

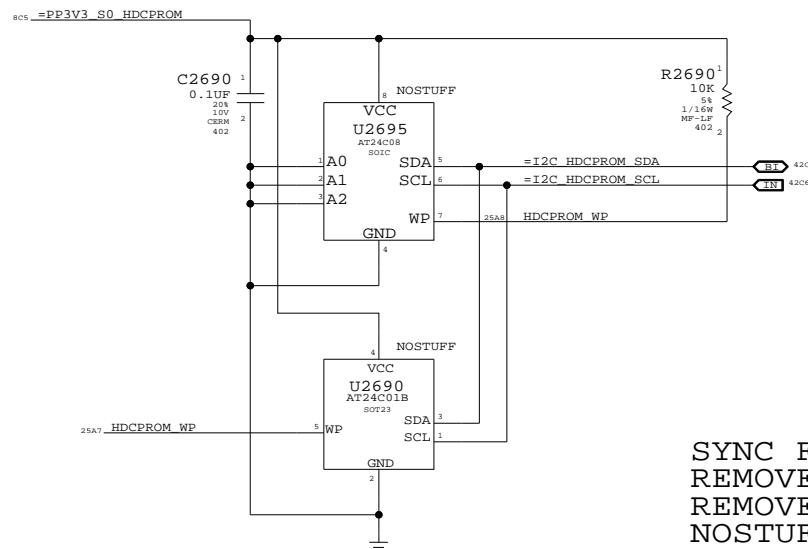


WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



### HDCP ROM

WF: Open question on which package option(s) nVidia can support.



SYNC FROM T18  
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT  
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672  
 NOSTUFF PP3V3\_S0\_MCP\_DAC RAIL COMPONENTS (L2650 AND C2650)  
 CHANGE C2651 TO R2651 TO GND PP3V3\_S0\_MCP\_DAC

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### MCP Graphics Support

SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007

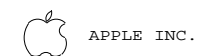
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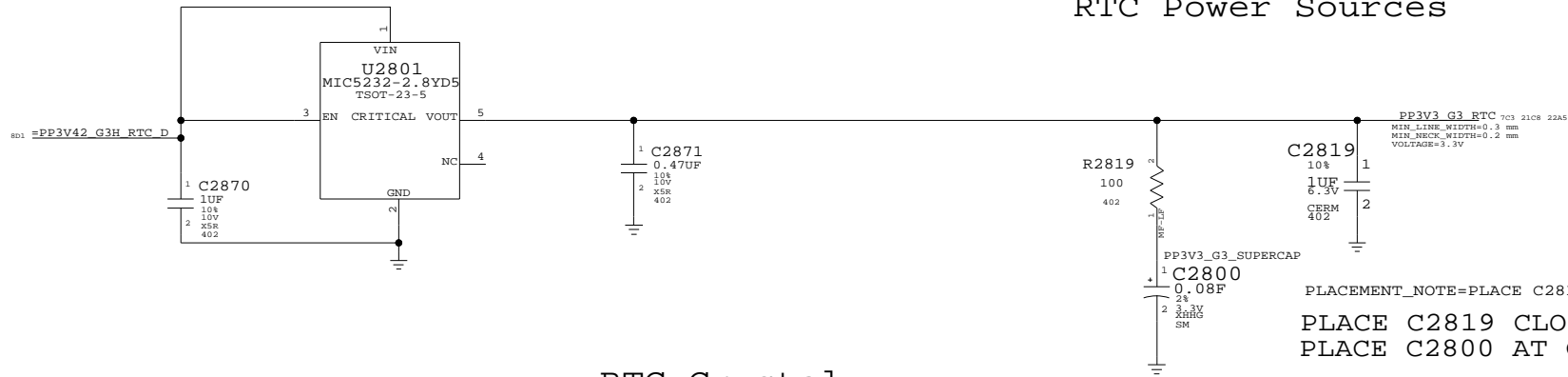
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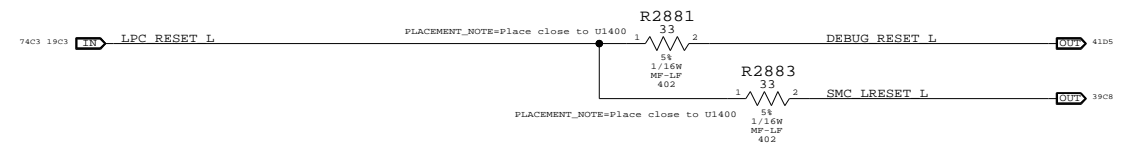
SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	26	109

### RTC Power Sources

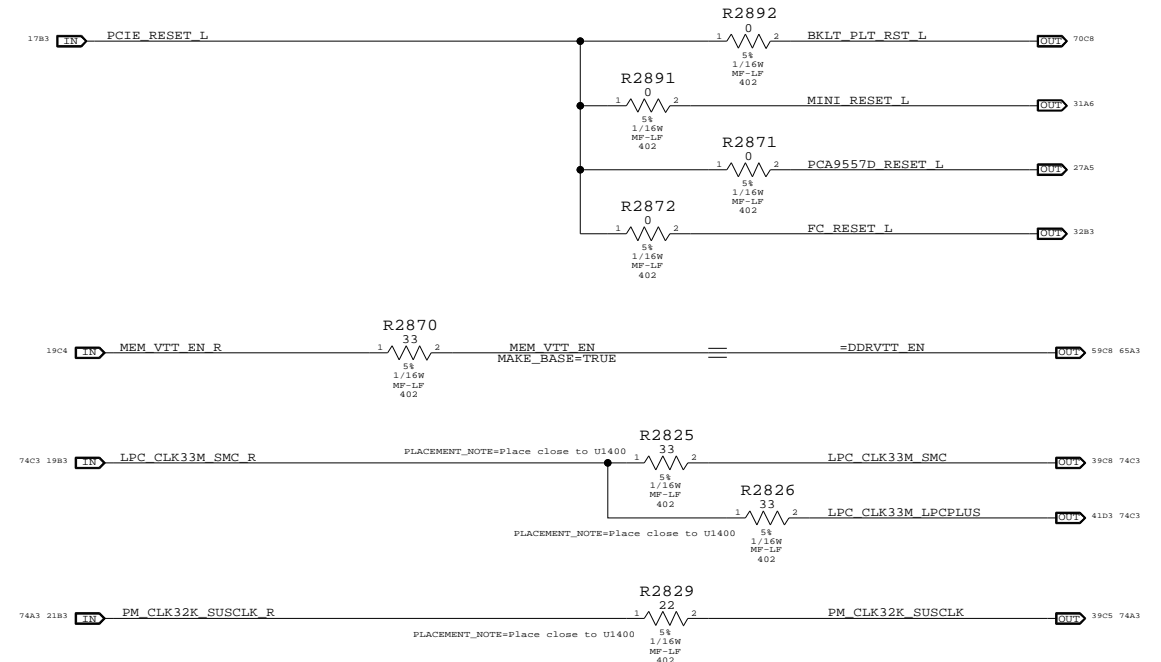


### Platform Reset Connections

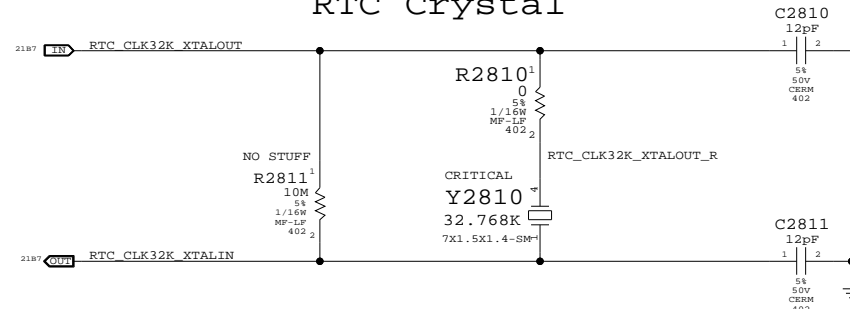
#### LPC Reset (Unbuffered)



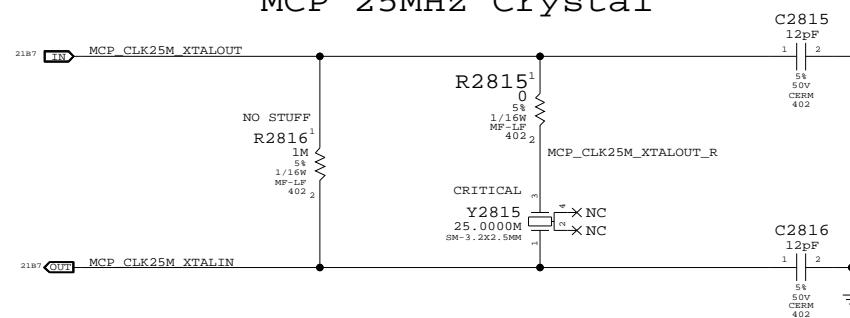
#### PCIE Reset (Unbuffered)



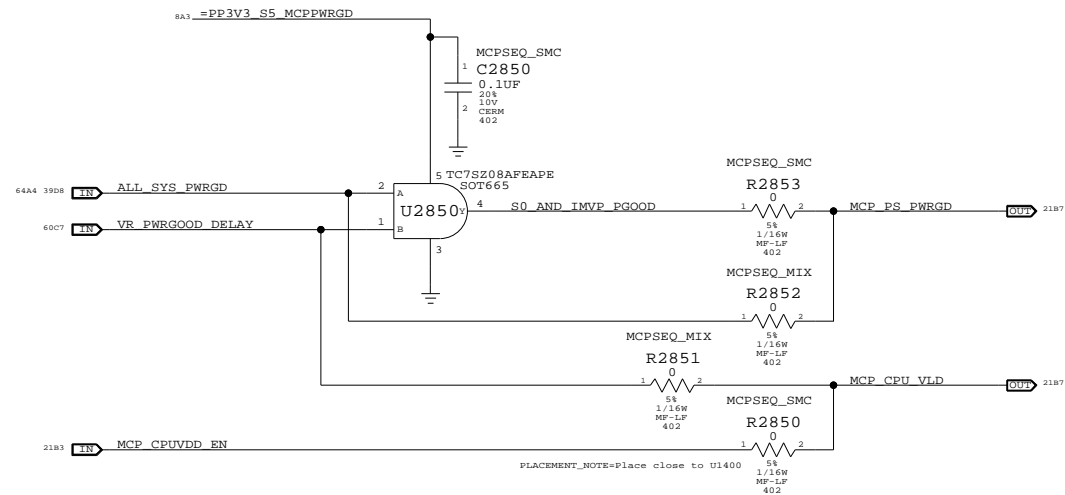
### RTC Crystal



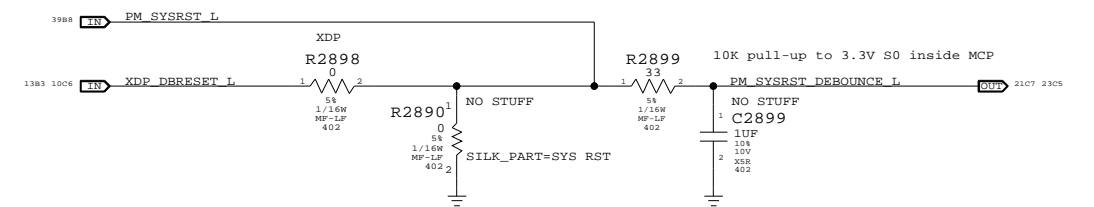
### MCP 25MHz Crystal



### MCP S0 PWRGD & CPU\_VLD



### Reset Button

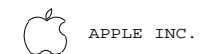


#### SB Misc

SYNC\_MASTER=RAYMOND SYNC\_DATE=04/05/2008

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SCALE	SHT	OF
NONE	28	109

MCPSEQ\_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.  
 MCPSEQ\_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.  
 SMC 99ms delay from ALL\_SYS\_PWRGD to IMVP\_VR\_ON plus IMVP6 delay for VR\_PWRGD\_DELAY should guarantee CPU\_VLD does not go high before CPUVDD\_EN (which is 40-100ms after PS\_PWRGD assertion).  
 NOTE: If CPU\_VLD deasserts during S0 MCP79 will take system to S5 immediately.

SYNC FROM T18  
 CHANGE RESET BUTTON TO RESET PADS  
 REMOVE UNUSED PCIE RESET SIGNALS  
 REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
 CHANGE RTC COIN CELL TO LDO & SUPERCAP  
 ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

# Page Notes

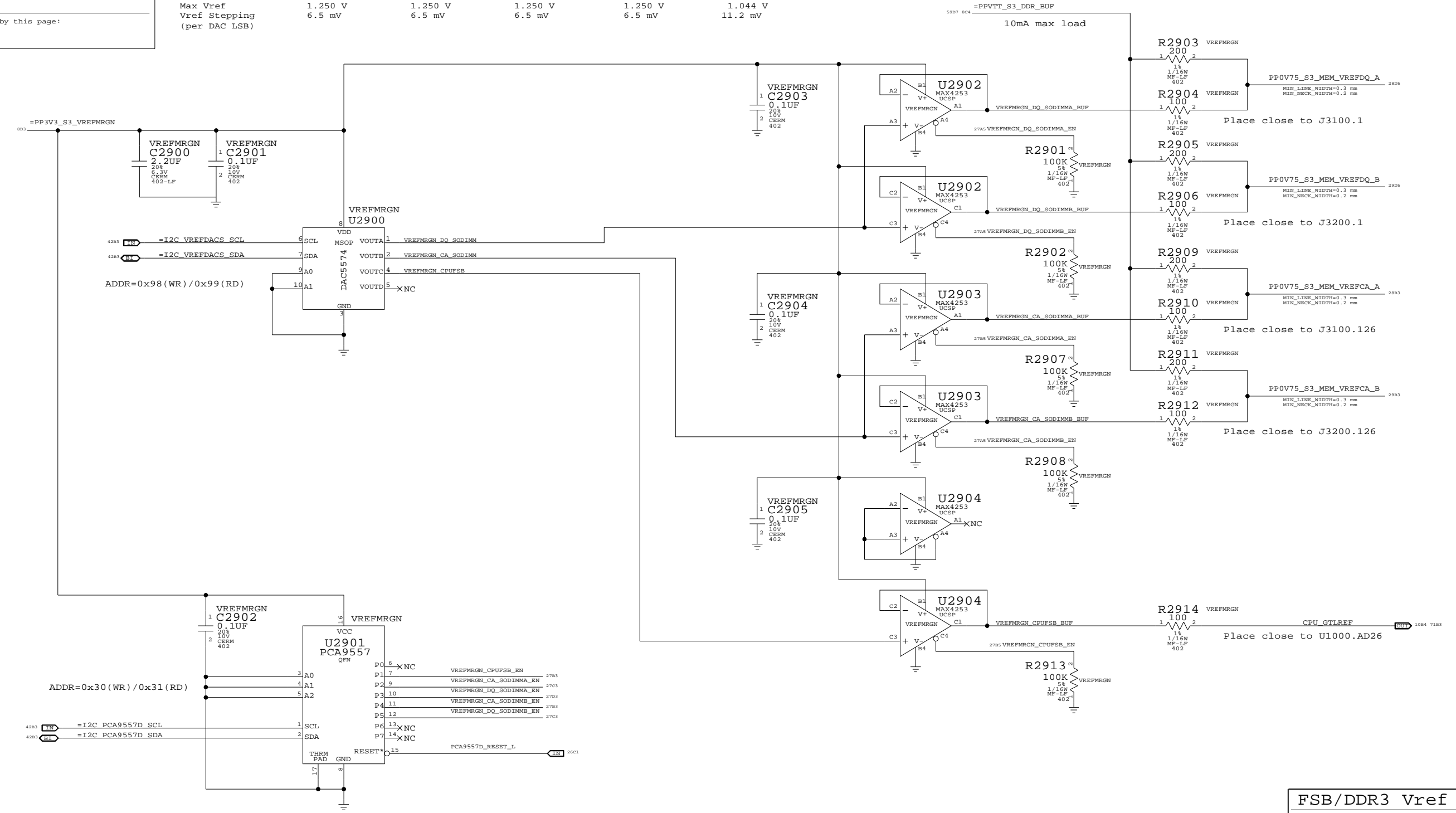
Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PP3V3\_S5\_VREFMRGN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMRGN  
 NO\_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2911	CRITICAL	NO_VREFMRGN

## FSB/DDR3 Vref Margining

SYNC\_MASTER=BEN SYNC\_DATE=03/31/2008

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D	051-7918	c
SCALE	SHT	OF
NONE	29	109

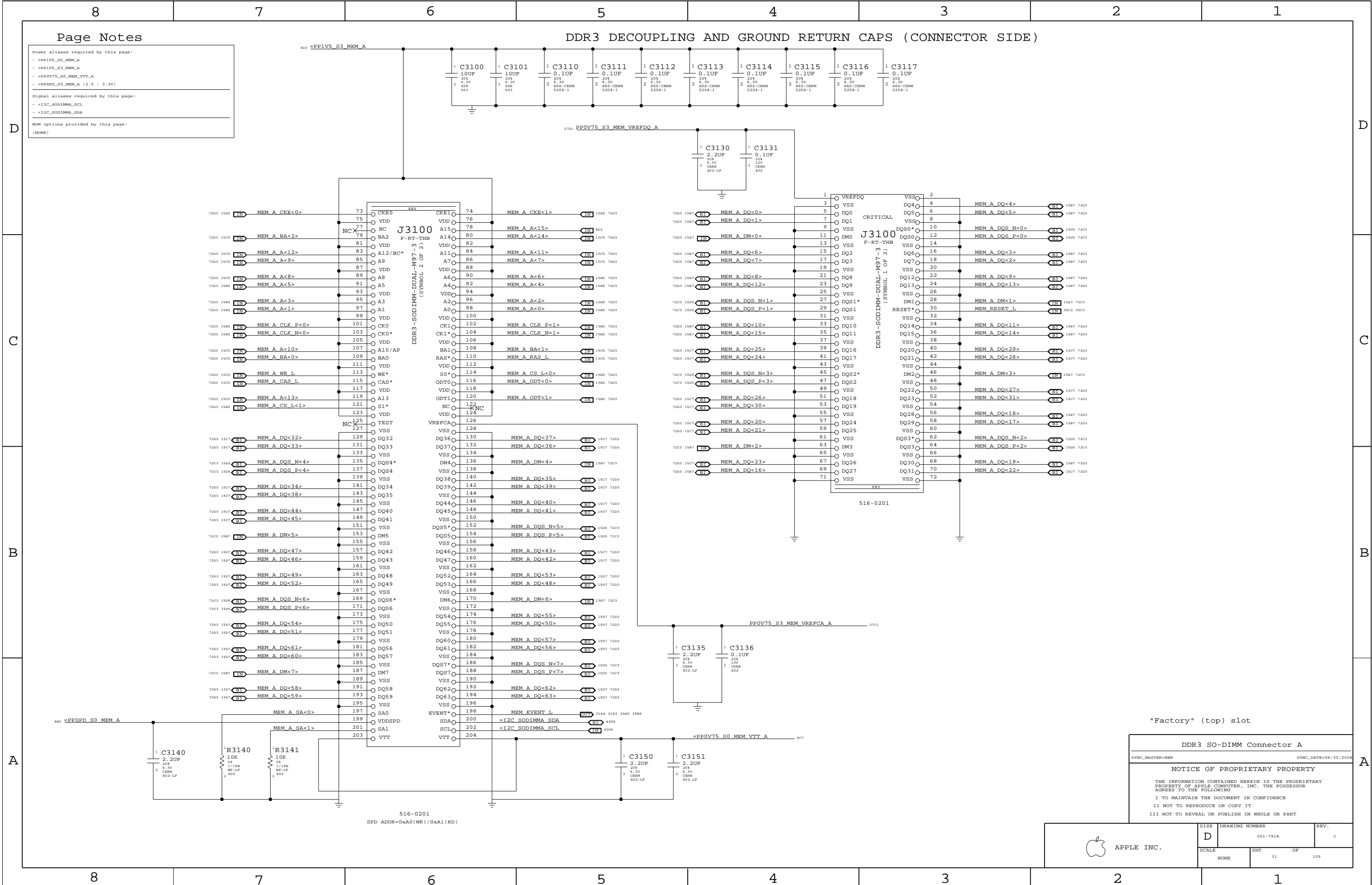
Page Notes

Power aliases required by this page:  
 - =PP1V5\_S0\_MEM\_A  
 - =PP1V5\_S3\_MEM\_A  
 - =PP0V75\_S0\_MEM\_VTT\_A  
 - =PPSPD\_S0\_MEM\_A (2.5 - 3.3V)

Signal aliases required by this page:  
 - =I2C\_SODIMMA\_SCL  
 - =I2C\_SODIMMA\_SDA

BOM options provided by this page:  
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC\_MASTER=BN SYNC\_DATE=06/30/2008

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	D	051-7918	C
SCALE	SHT	OF	109
NONE	31		

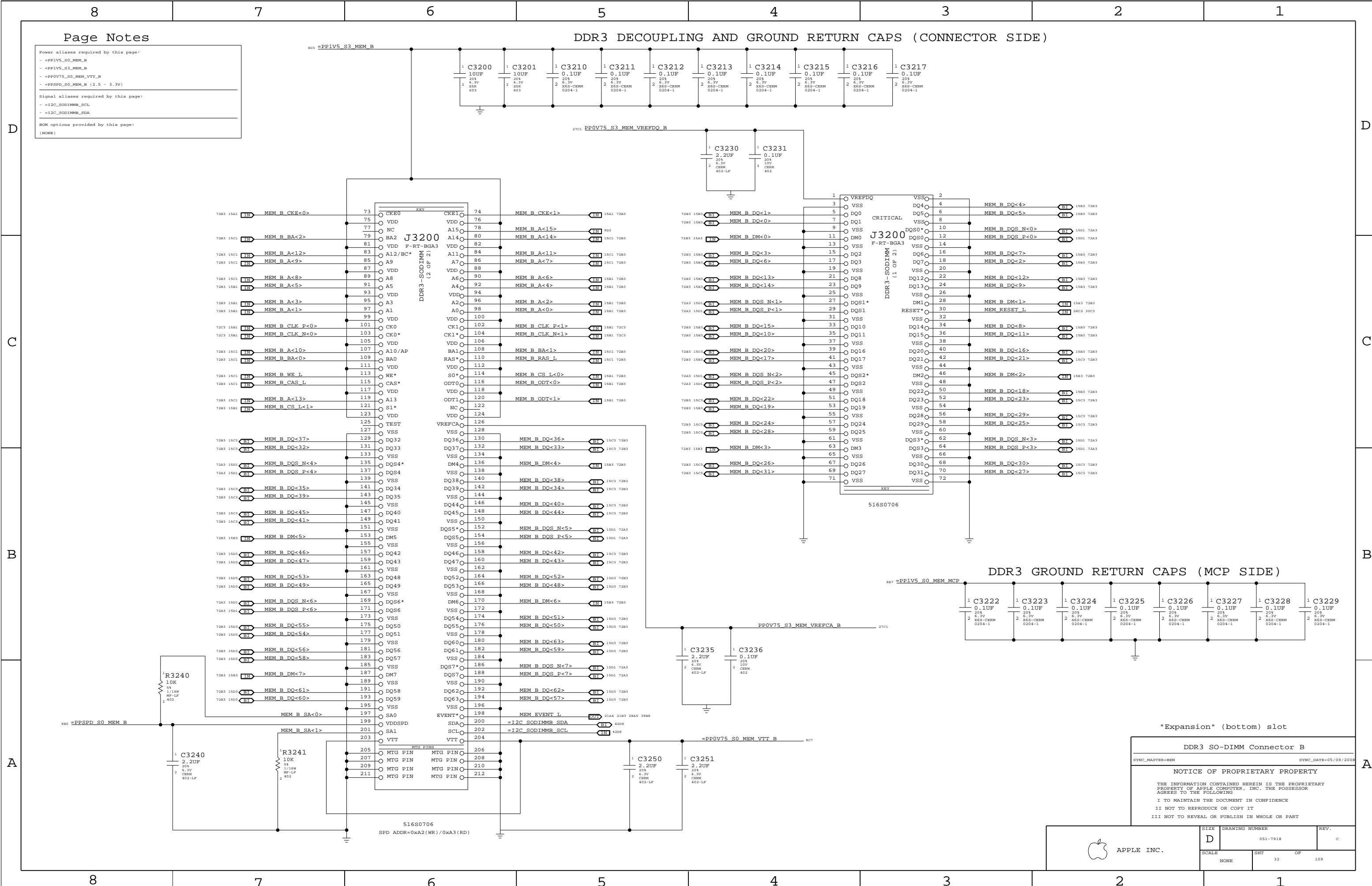
Page Notes

Power aliases required by this page:  
 - =PP1V5\_S0\_MEM\_B  
 - =PP1V5\_S3\_MEM\_B  
 - =PP0V75\_S0\_MEM\_VTT\_B  
 - =PPSPD\_S0\_MEM\_B (2.5 - 3.3V)

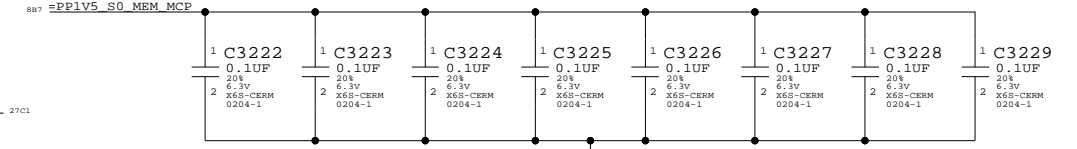
Signal aliases required by this page:  
 - =I2C\_SODIMMB\_SCL  
 - =I2C\_SODIMMB\_SDA

BOM options provided by this page:  
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC\_MASTER=BNB SYNC\_DATE=05/09/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	NONE	SHT	OF 109
		32	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

4

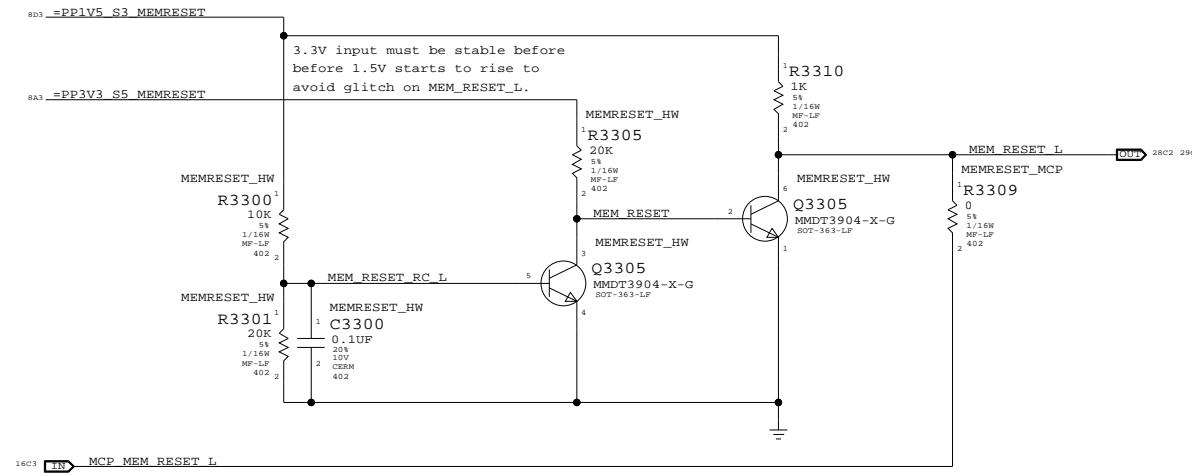
3

2

1

### DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



**DDR3 Support**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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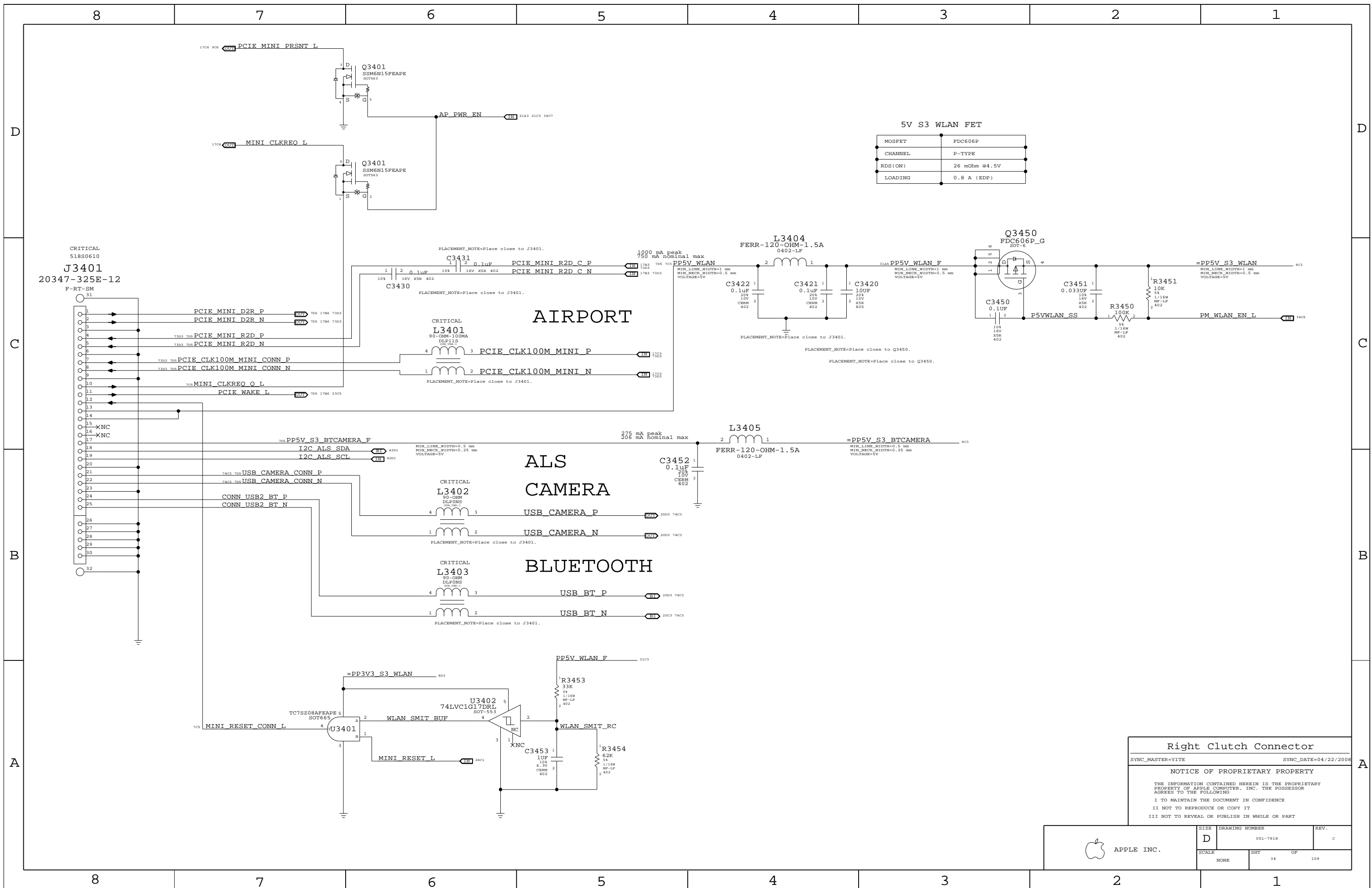
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	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	33	1	109



**Right Clutch Connector**

SYNC\_MASTER=YITE      SYNC\_DATE=04/22/2008

**NOTICE OF PROPRIETARY PROPERTY**

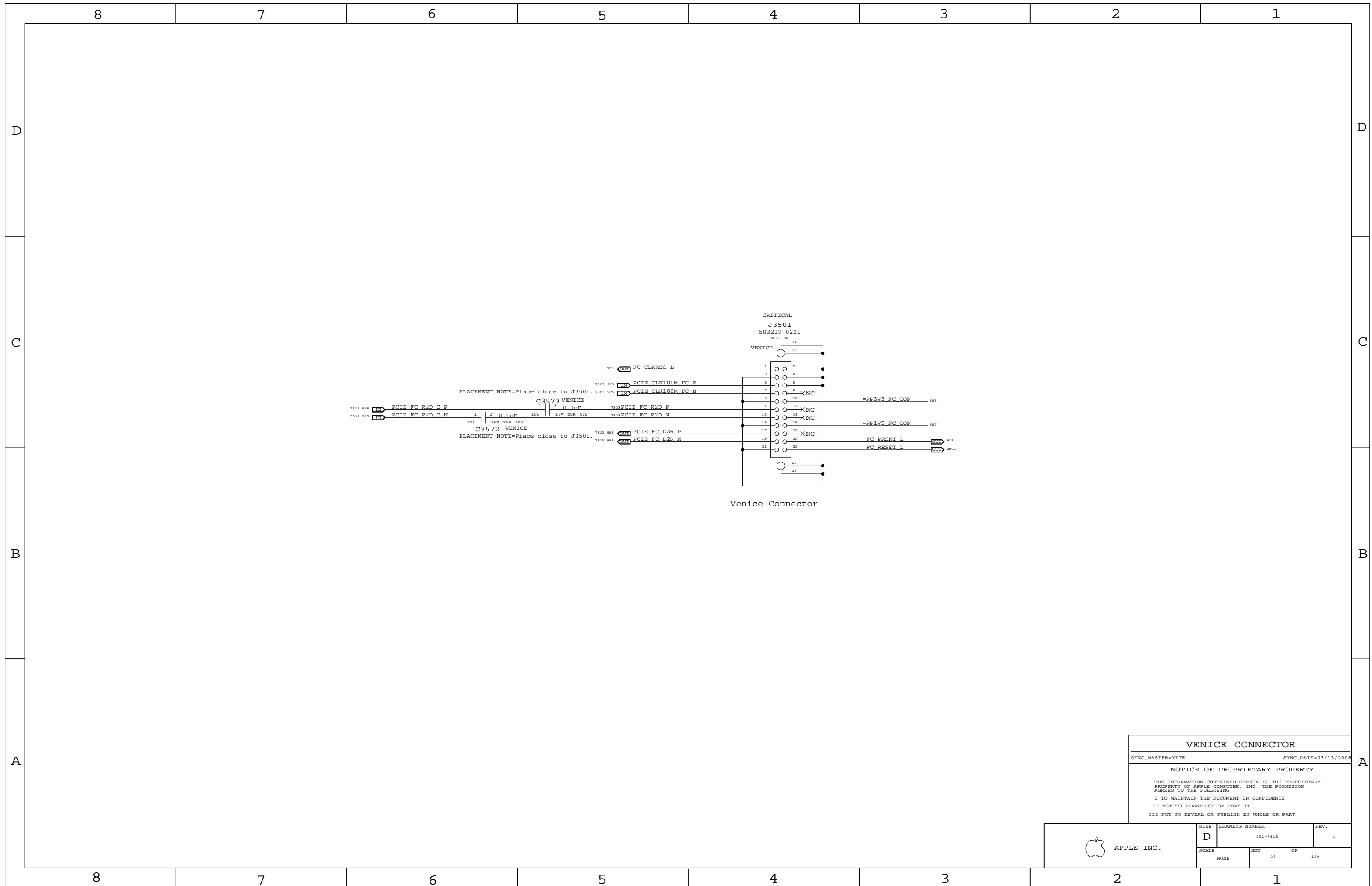
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	34		



**VENICE CONNECTOR**

SYNC\_MASTER=YITE SYNC\_DATE=03/13/2008

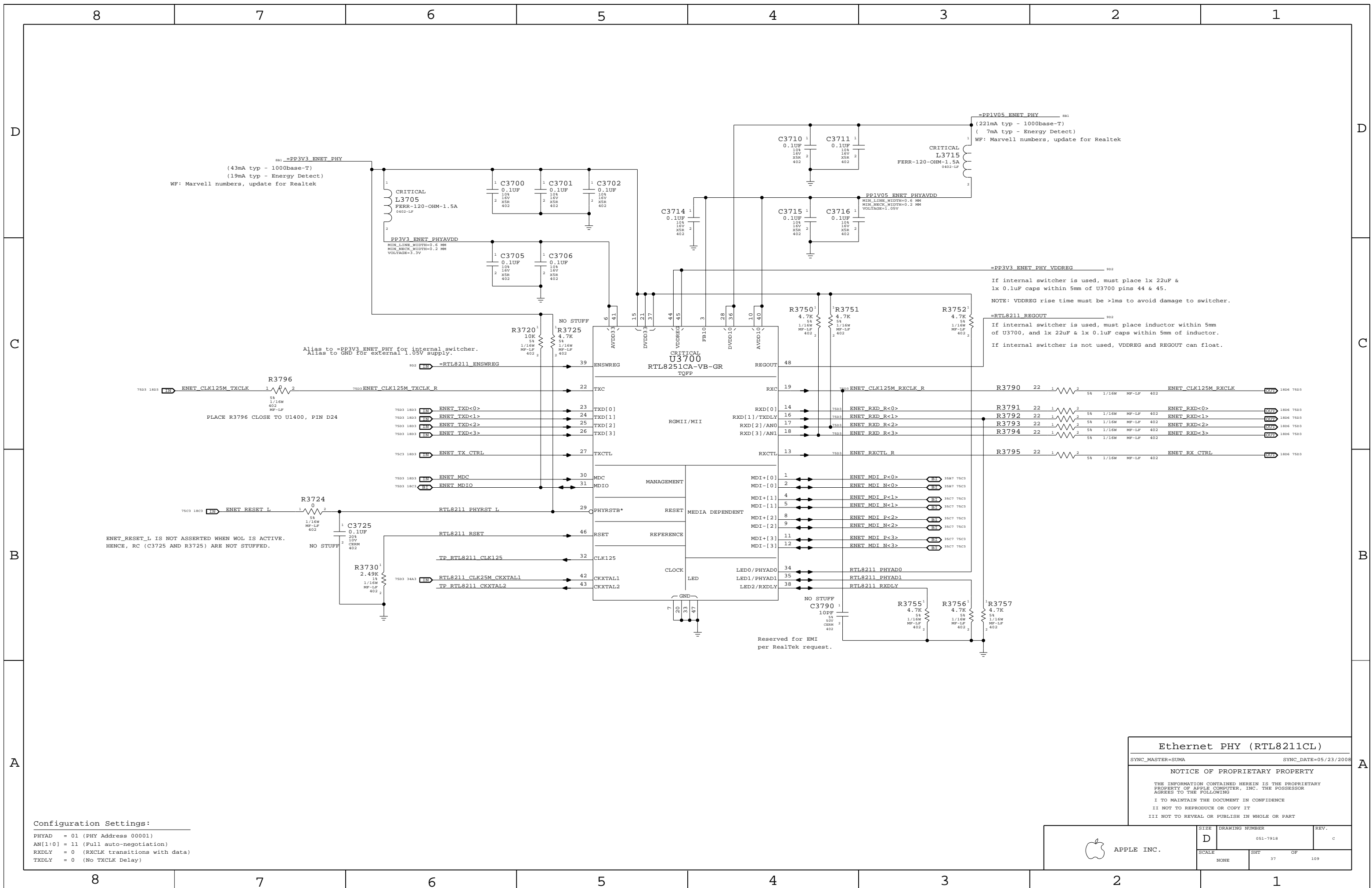
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	<b>SIZE</b> D	<b>DRAWING NUMBER</b> 051-7918	<b>REV.</b> c
	<b>SCALE</b> NONE	<b>SHT</b> 35	<b>OF</b> 109





=PP3V3\_ENET\_PHY  
 (43mA typ - 1000base-T)  
 (19mA typ - Energy Detect)  
 WF: Marvell numbers, update for Realtek

=PP1V05\_ENET\_PHY  
 (221mA typ - 1000base-T)  
 (7mA typ - Energy Detect)  
 WF: Marvell numbers, update for Realtek

Alias to =PP3V3\_ENET\_PHY for internal switcher.  
 Alias to GND for external 1.05V supply.

=PP3V3\_ENET\_PHY\_VDDREG  
 If internal switcher is used, must place 1x 22uF &  
 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.  
 NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211\_REGOUT  
 If internal switcher is used, must place inductor within 5mm  
 of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.  
 If internal switcher is not used, VDDREG and REGOUT can float.

PLACE R3796 CLOSE TO U1400, PIN D24

ENET\_RESET\_L IS NOT ASSERTED WHEN WOL IS ACTIVE.  
 HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

Reserved for EMI  
 per Realtek request.

**Configuration Settings:**  
 PHYAD = 01 (PHY Address 00001)  
 AN[1:0] = 11 (Full auto-negotiation)  
 RXDLY = 0 (RXCLK transitions with data)  
 TXDLY = 0 (No TXCLK Delay)

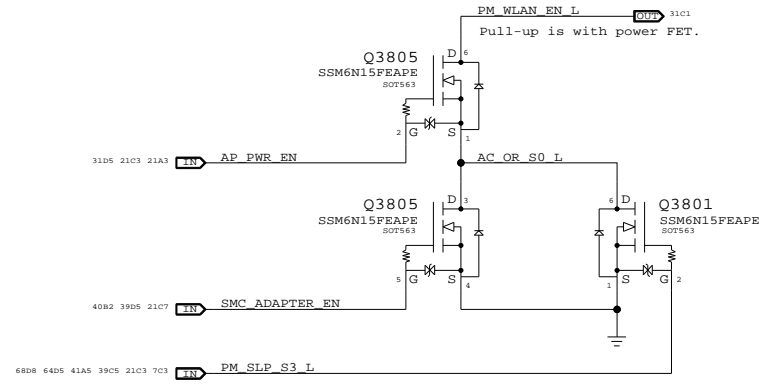
**Ethernet PHY (RTL8211CL)**  
 SYNC\_MASTER=SUMA SYNC\_DATE=05/23/2008  
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	SIZE <b>D</b>	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHEET 37	OF 109

### WLAN Enable Generation

"WLAN" = ("S3" && "AP\_PWR\_EN" && ("AC" || "S0"))

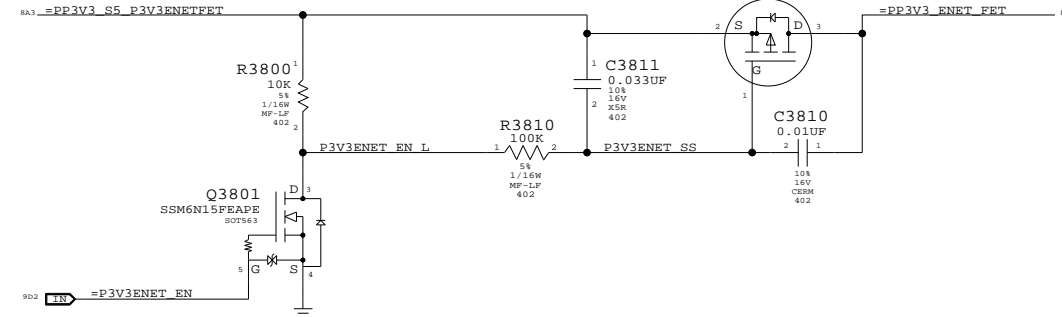
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



### 3.3V ENET FET

@ 2.5V Vgs:  
 Rds(on) = 90mOhm max  
 I(max) = 1.7A (85C)

CRITICAL  
 Q3810  
 NTR4101P  
 SOT-23-NP

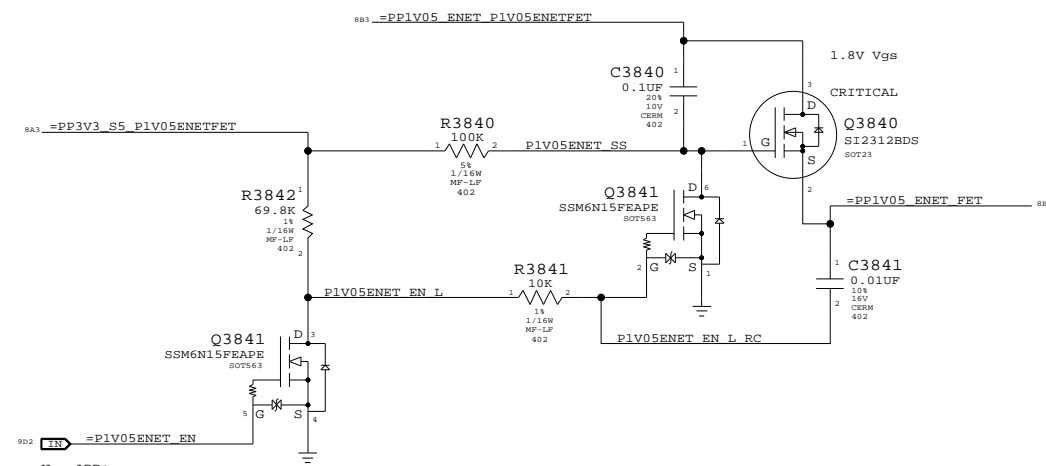


MOBILE:  
 Recommend aliasing PM\_SLP\_RMGT\_L and =P3V3ENET\_EN. Nets separated on ARB for alternate power options.

### 1.05V ENET FET

1.8V Vgs

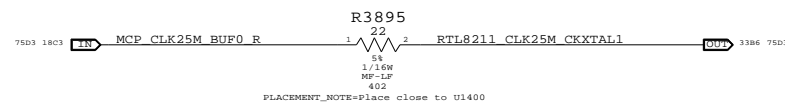
CRITICAL



Non-ARB:  
 Recommend aliasing PM\_SLP\_RMGT\_L and =P1V05ENET\_EN. Nets separated on ARB for alternate power options.

### RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



### Ethernet & AirPort Support

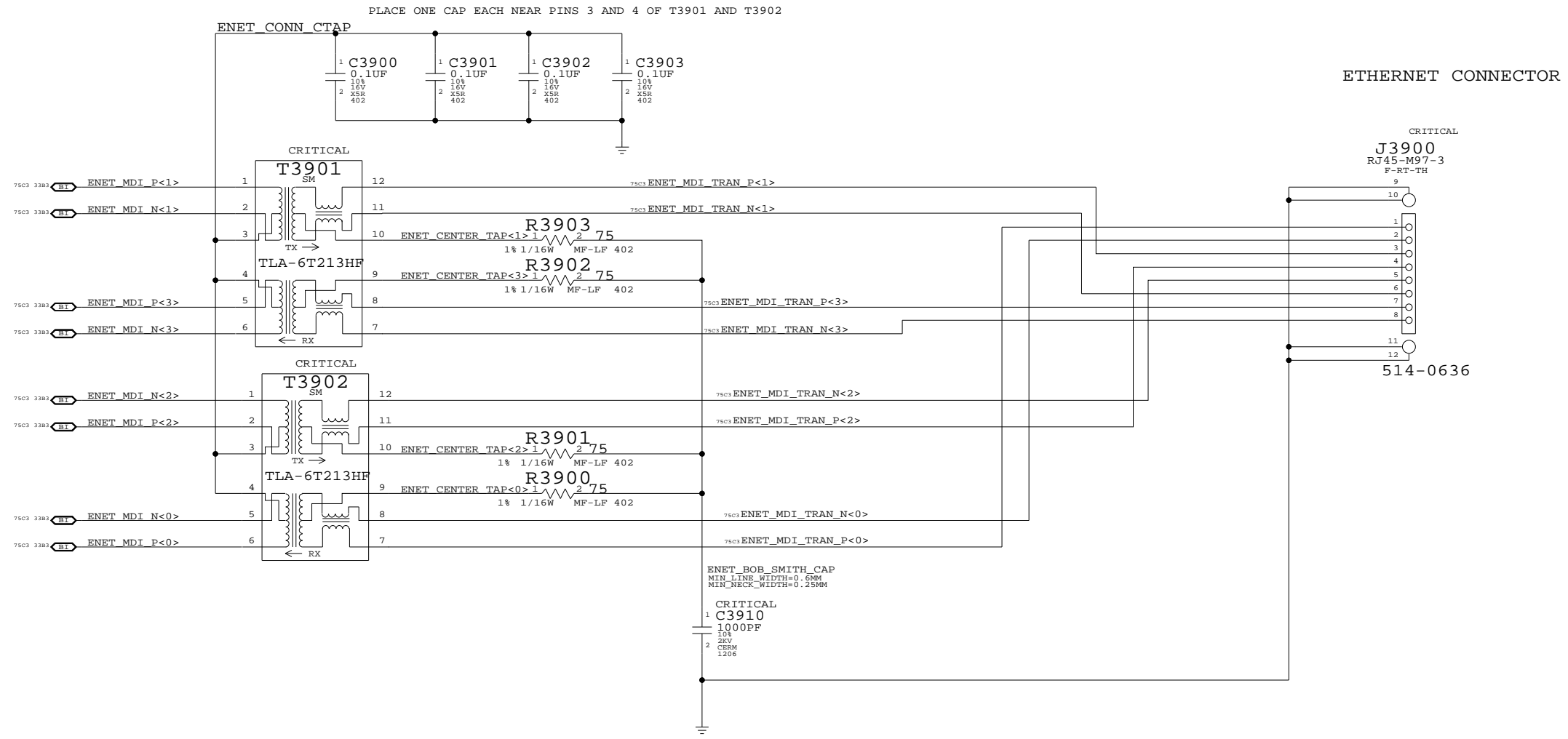
SYNC\_MASTER=SUMA SYNC\_DATE=07/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	38	109



**ETHERNET CONNECTOR**

SYNC\_MASTER=SUMA SYNC\_DATE=04/04/2008

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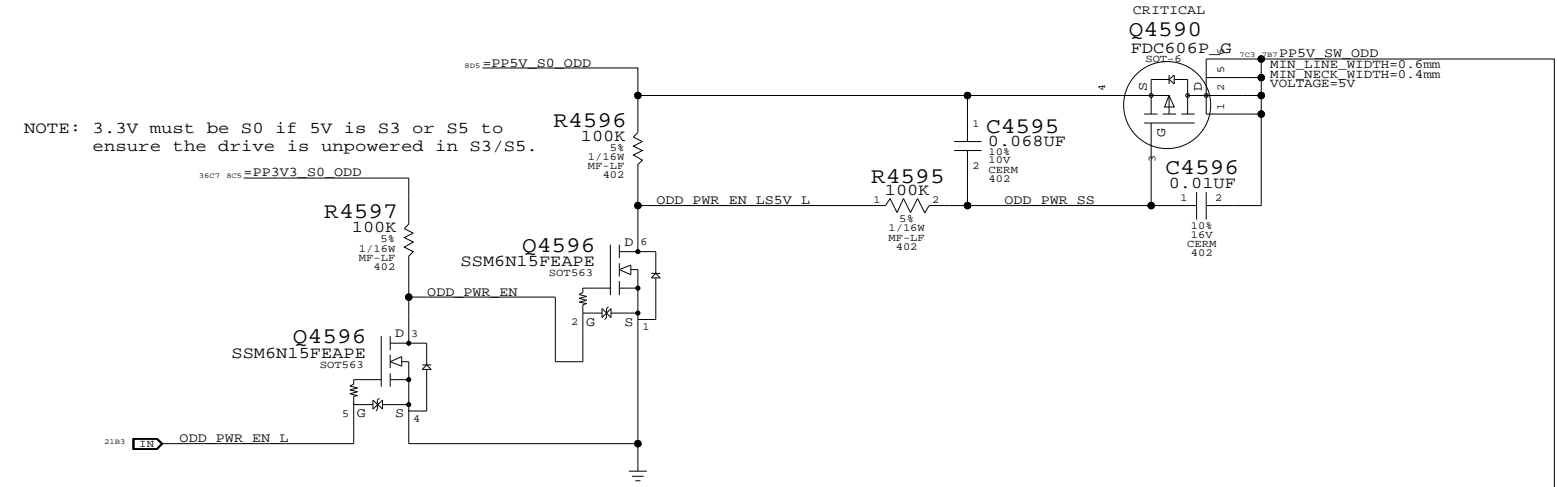
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

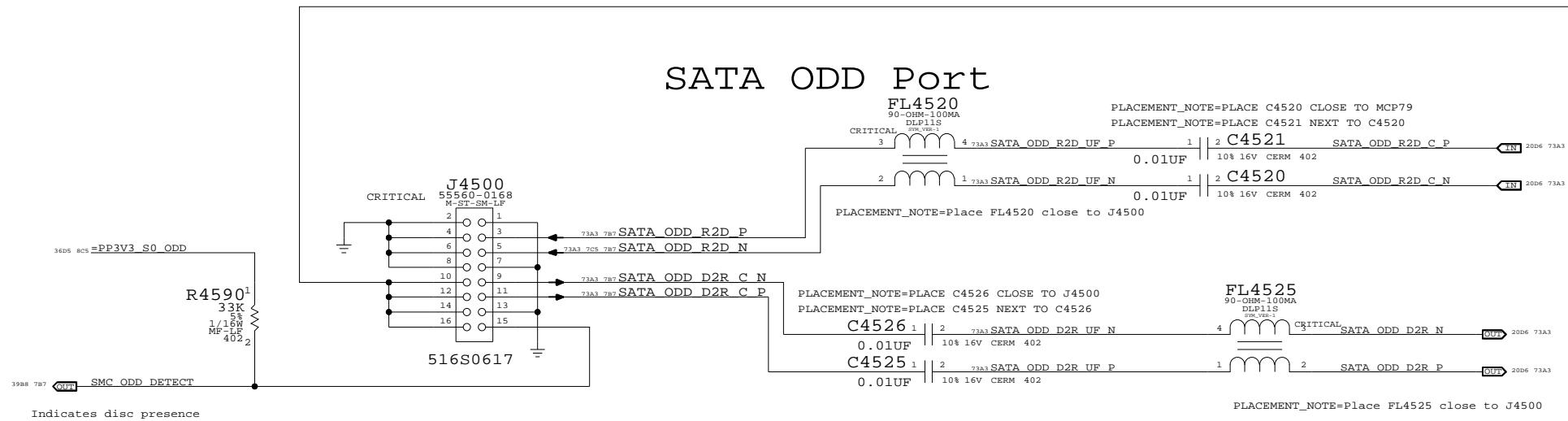
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE <b>D</b>	DRAWING NUMBER 051-7918	REV. c
	SCALE NONE	SHT 39	OF 109

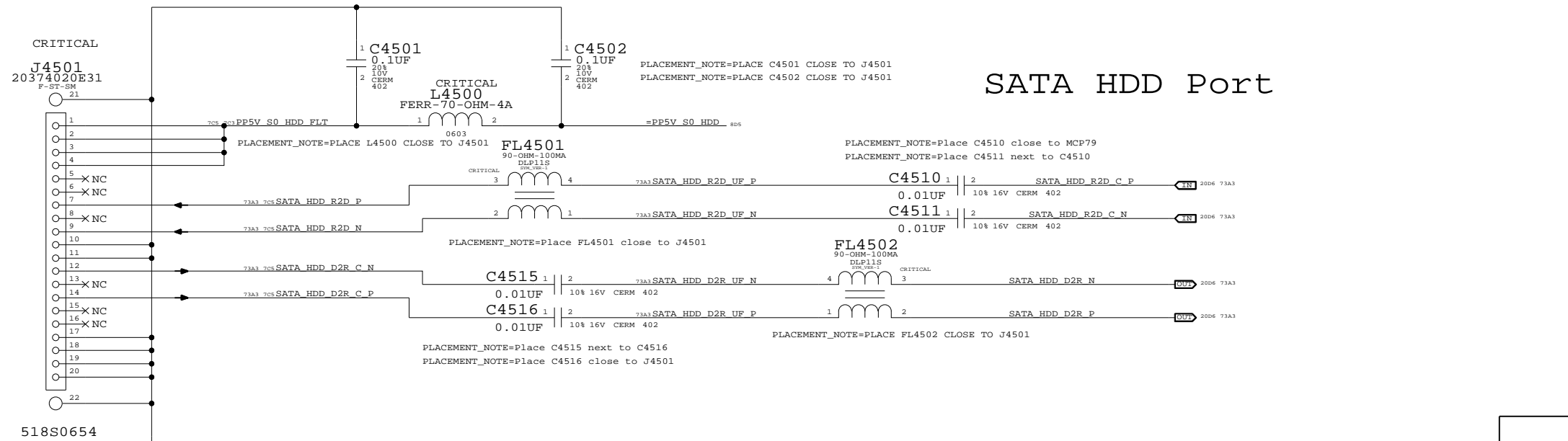
### ODD Power Control



### SATA ODD Port



### SATA HDD Port



**SATA Connectors**  
 SYNC\_MASTER=CHANGZHANG SYNC\_DATE=04/14/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	REV.
NONE	45	109	

D

D

C

C

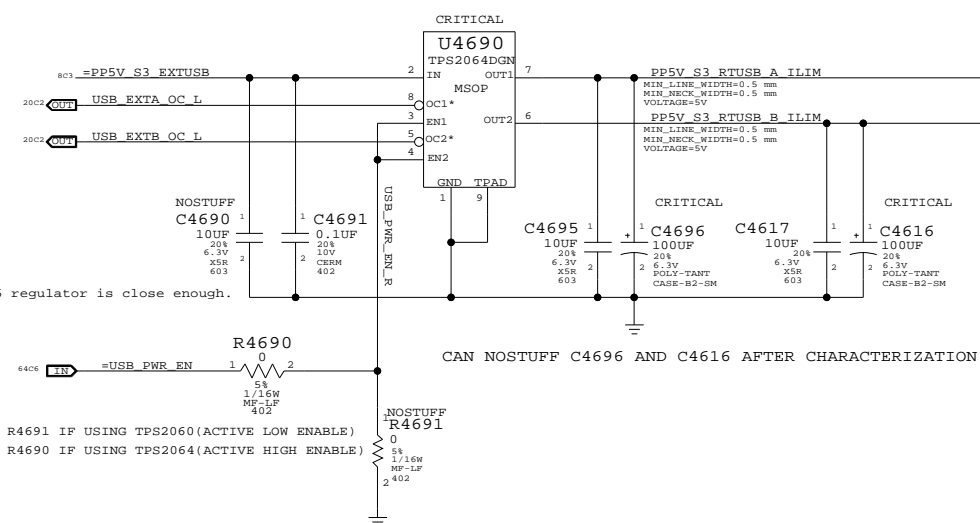
B

B

A

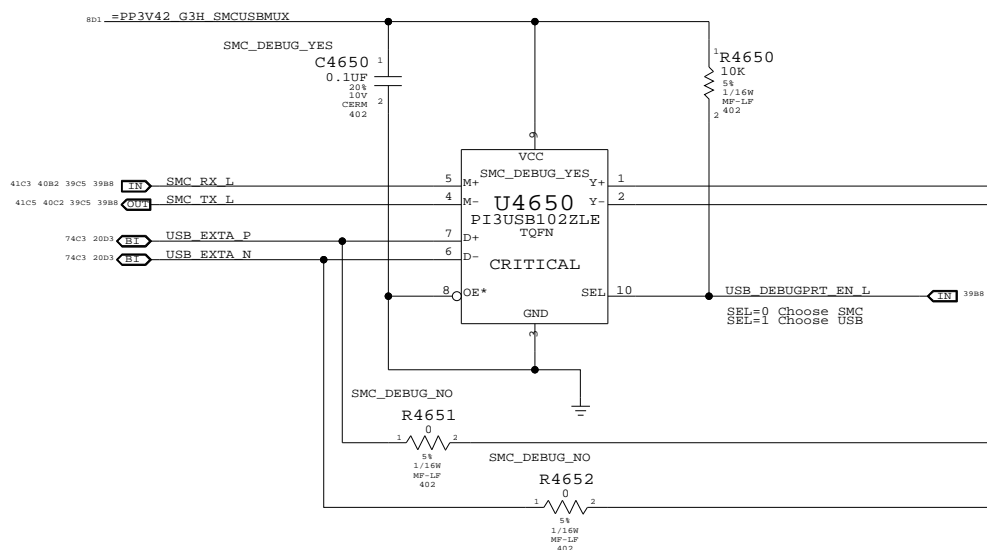
A

### Port Power Switch

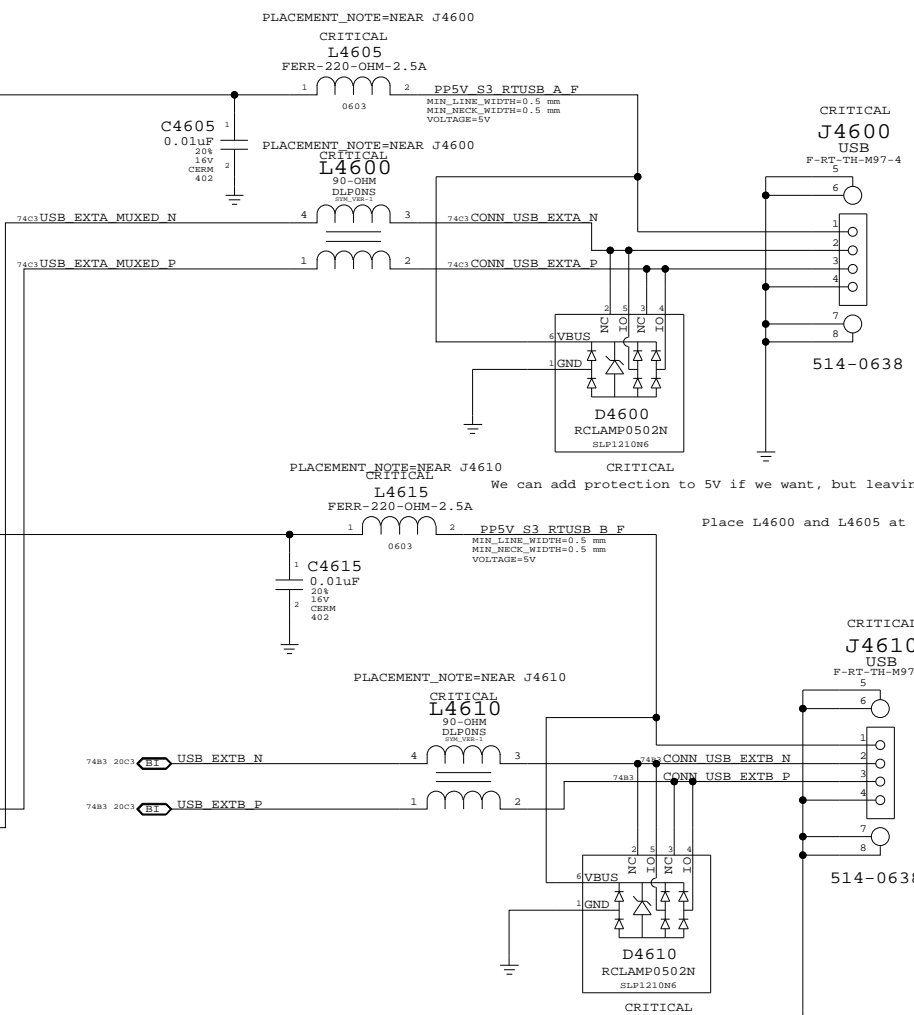


We can remove C4690 later if the output cap of the 5V\_S5 regulator is close enough.

### USB/SMC Debug Mux



### USB PORT A (FRONT PORT)



### USB PORT B (BACK PORT)

**External USB Connectors**

SYNC\_MASTER=YUAN.MA SYNC\_DATE=01/18/2008

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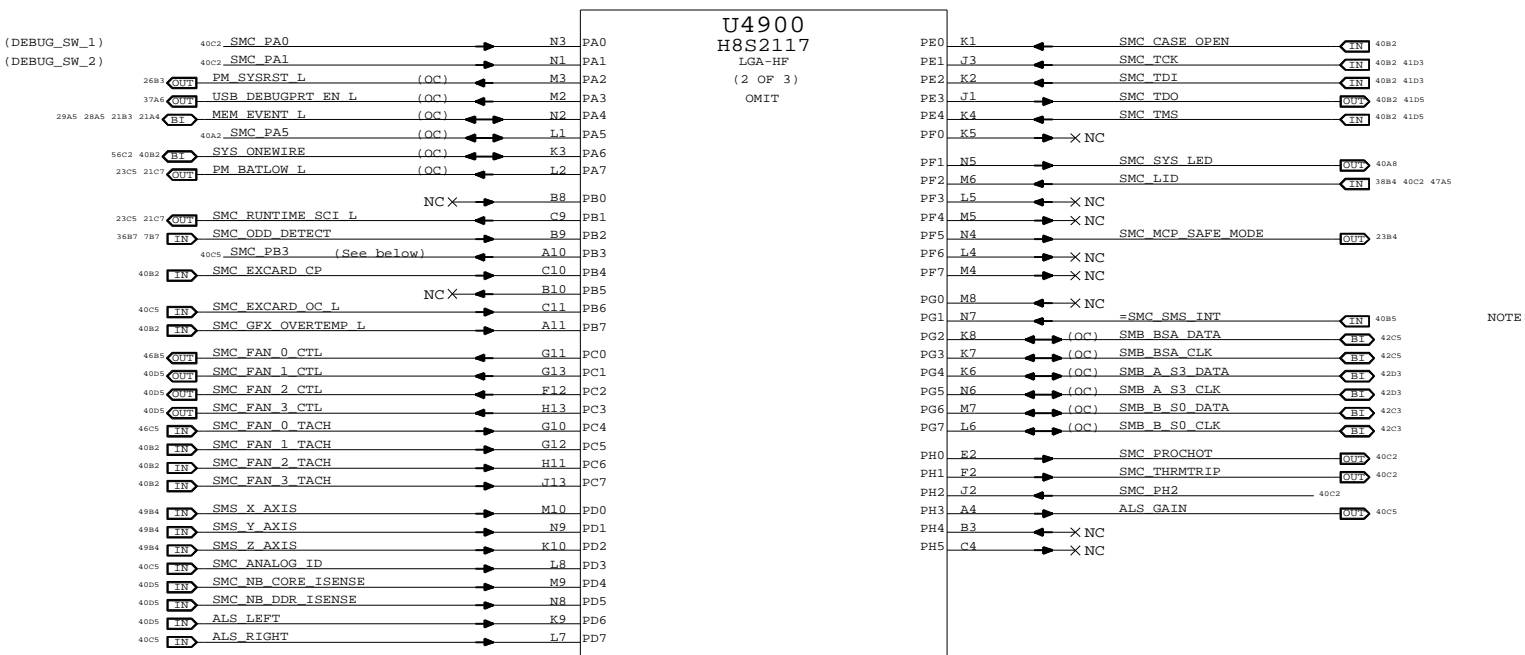
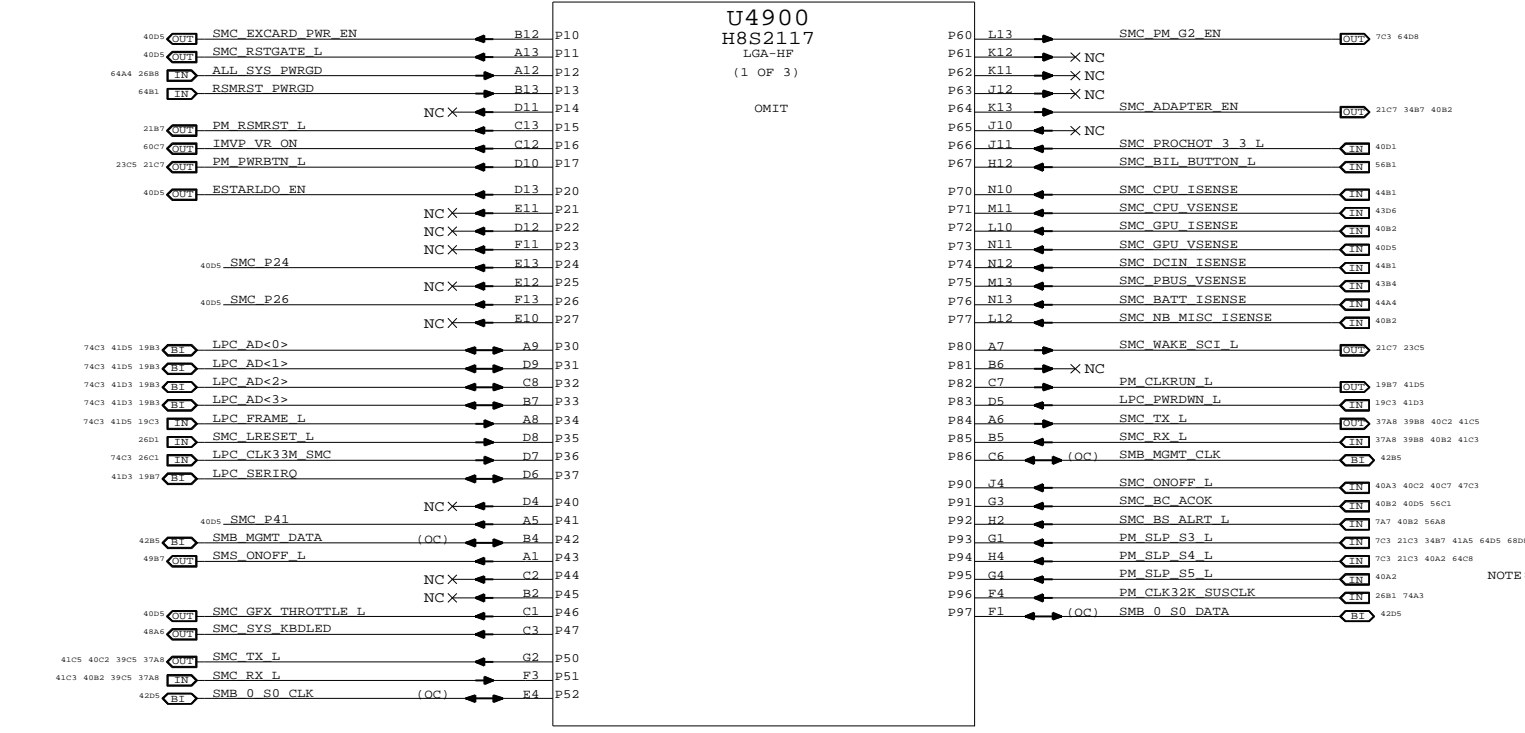
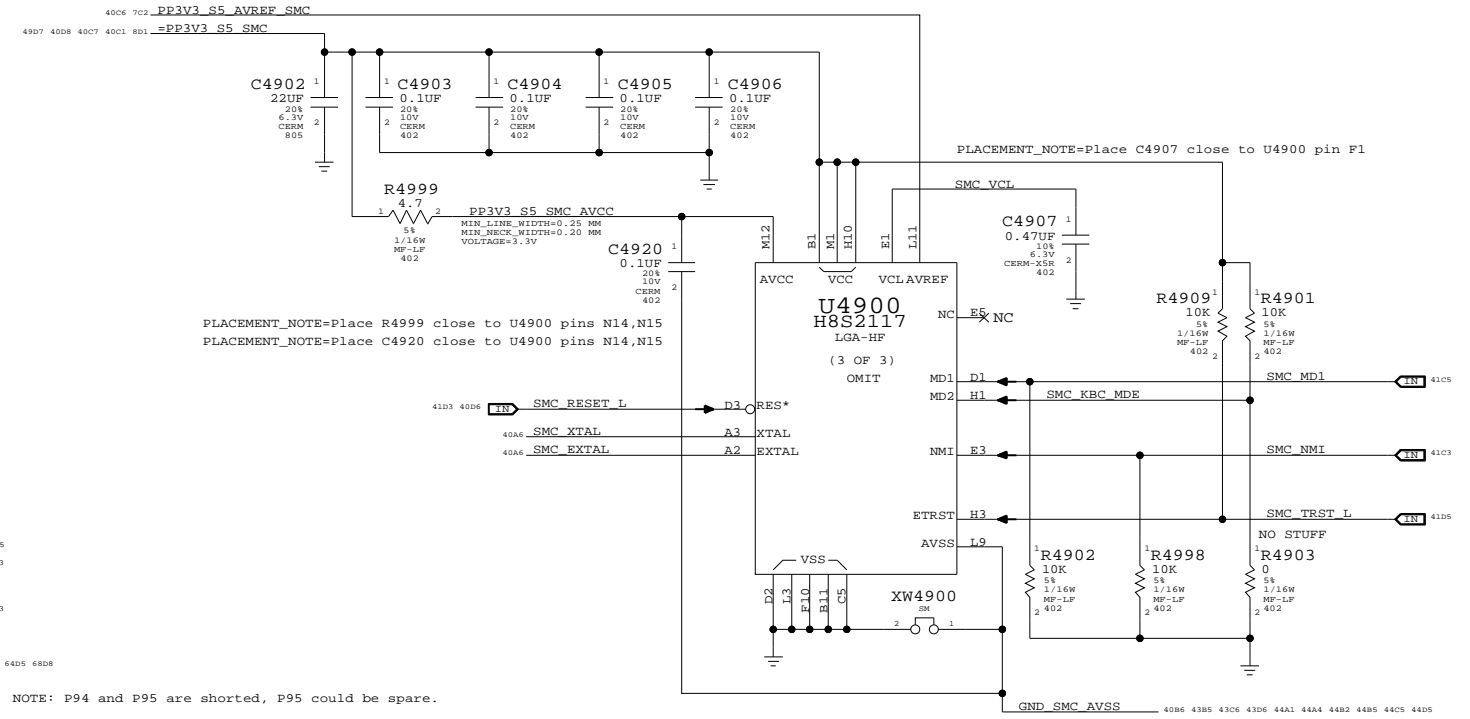
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	46		



NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

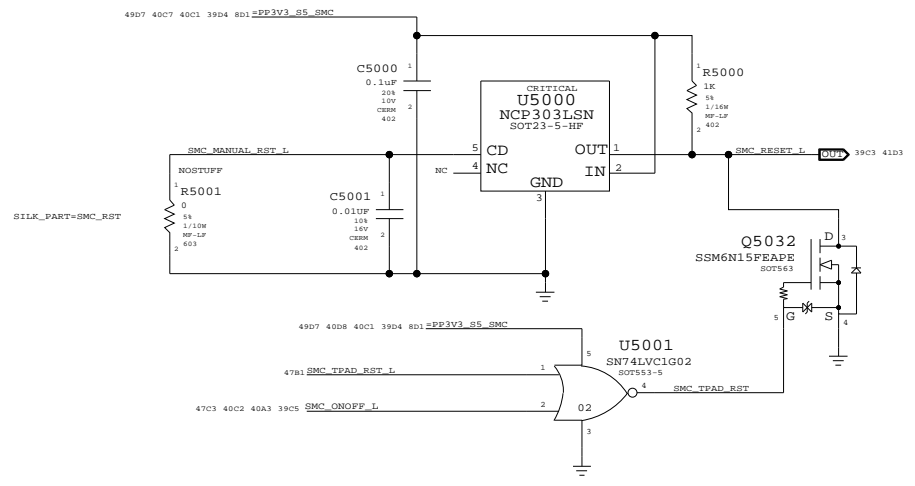


SMC\_PB3:  
 SMC\_IG\_THROTTLE\_L for MG systems.  
 Otherwise, TP/NC okay (was ISENSE\_CAL\_EN)

SMC  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=06/26/2008  
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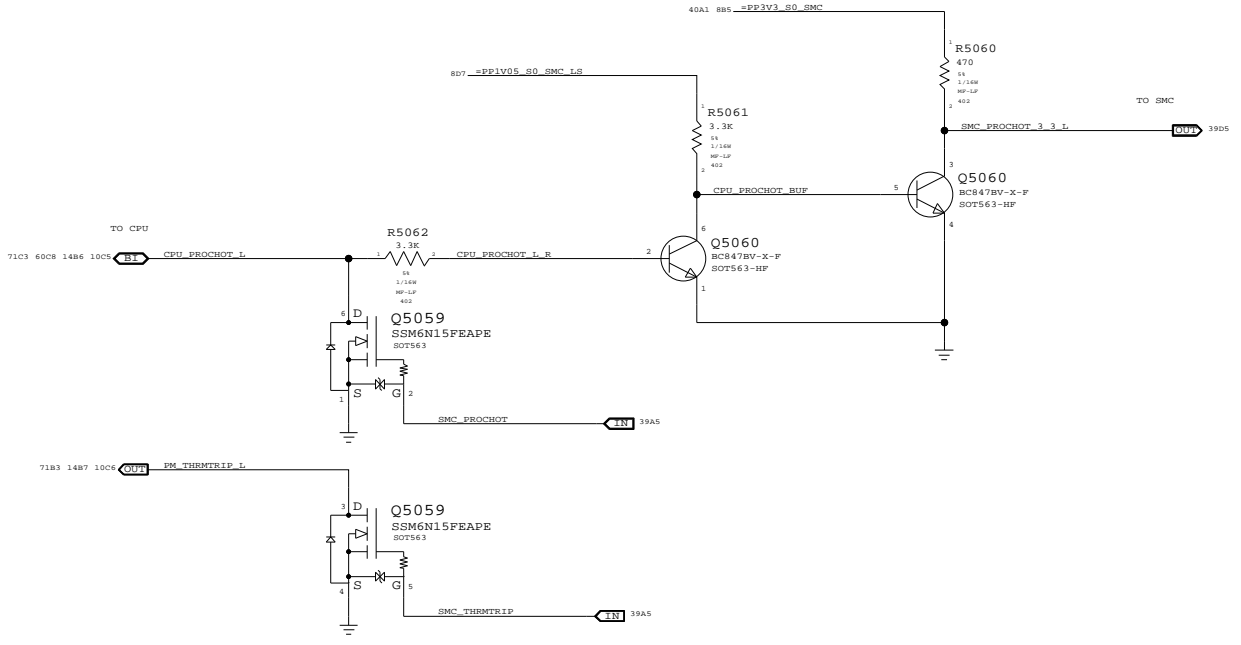
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	49		

SMC Reset "Button" / Brownout Detect

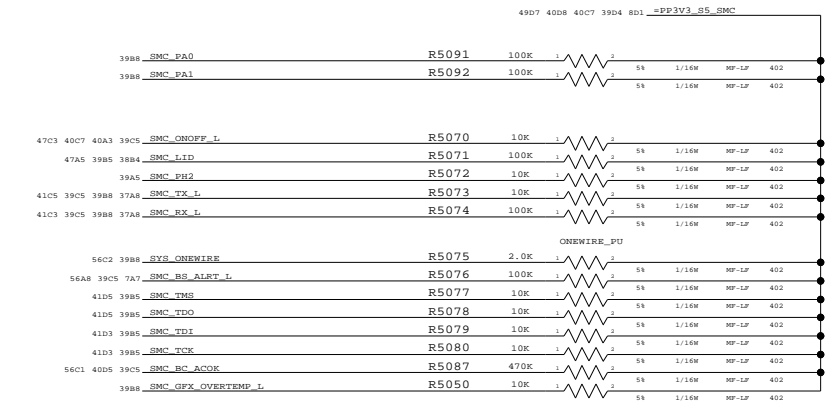
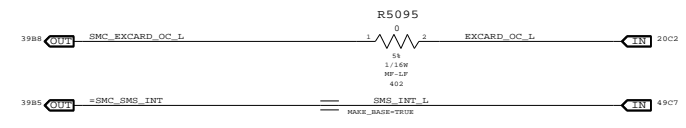
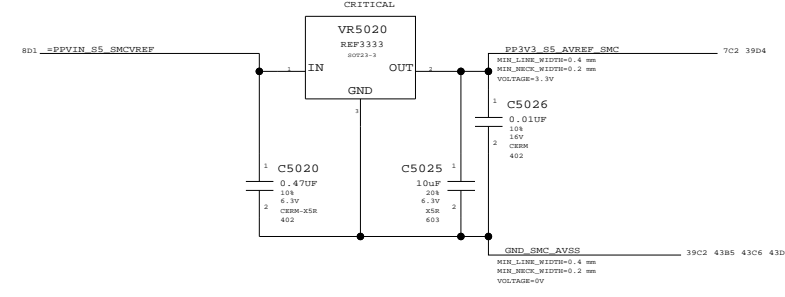


39A8	SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE	
39A8	SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
39A8	SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
39C8	SMC_GPU_THROTTLE_L	SMC_GPU_THROTTLE_L	MAKE_BASE=TRUE	21A4 21B3
39C8	ESTARLDO_EN	NC_ESTARLDO_EN	MAKE_BASE=TRUE	
56C1 40B2 39C5	SMC_BC_ACOK	=CHGR_ACOK	MAKE_BASE=TRUE	57C5
39C8	SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
39C8	SMC_P26	SMC_RMON_MUX_SEL	MAKE_BASE=TRUE	44A5
39C8	SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
39A8	SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	44D5
39A8	SMC_NB_DDR_ISENSE	SMC_MCP_DDR_ISENSE	MAKE_BASE=TRUE	44C5
39A8	ALS_LEFT	SMC_CPU_FSB_ISENSE	MAKE_BASE=TRUE	44B5
39C5	SMC_GPU_VSENSE	SMC_MCP_VSENSE	MAKE_BASE=TRUE	43D6
39D8	SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
39D8	SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
39B8	SMC_PB3	NC_SMC_PB3	MAKE_BASE=TRUE	
39A5	ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	
39A8	SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE	
39A8	ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE	

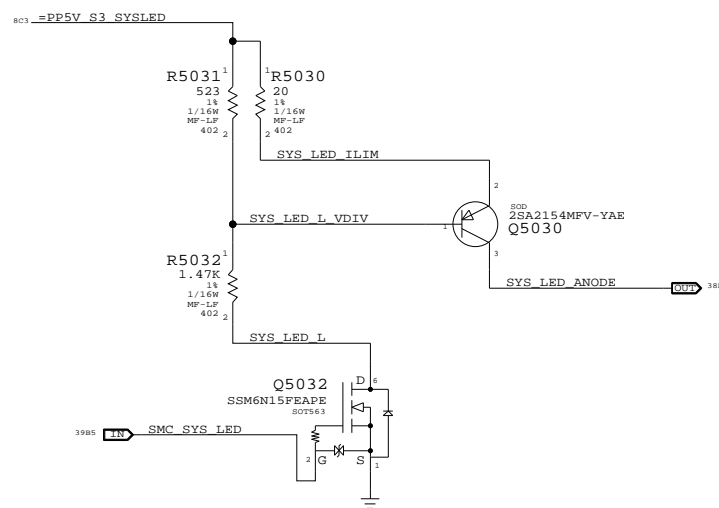
SMC FSB to 3.3V Level Shifting



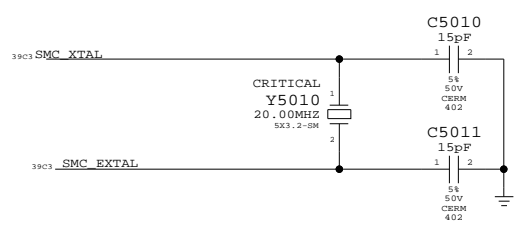
SMC AVREF Supply



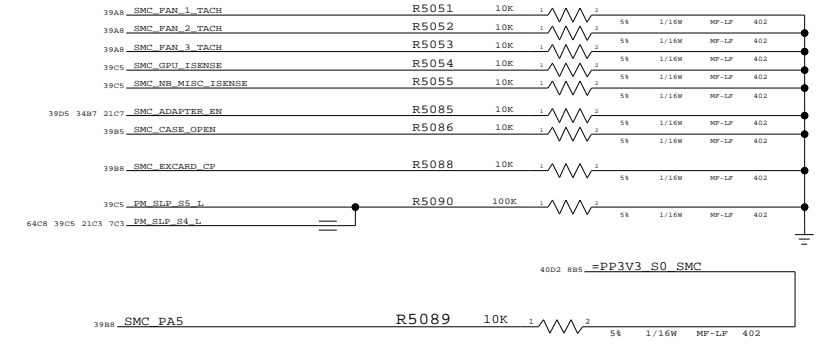
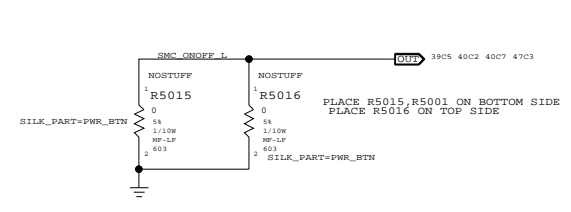
System (Sleep) LED Circuit



SMC Crystal Circuit



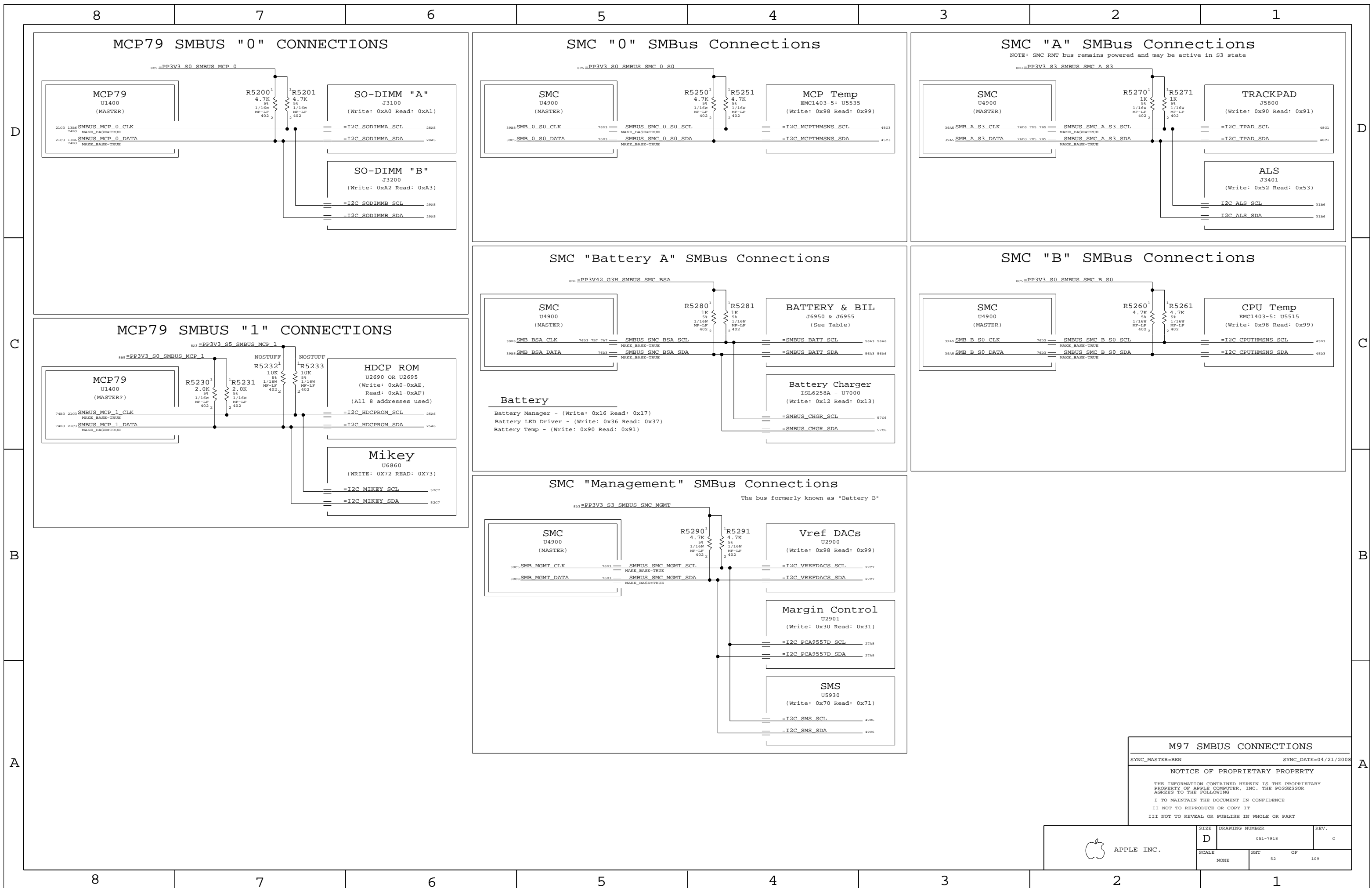
Debug Power "Button"



SMC Support  
 SYNC\_MASTER=YUAN.MA SYNC\_DATE=05/28/2008  
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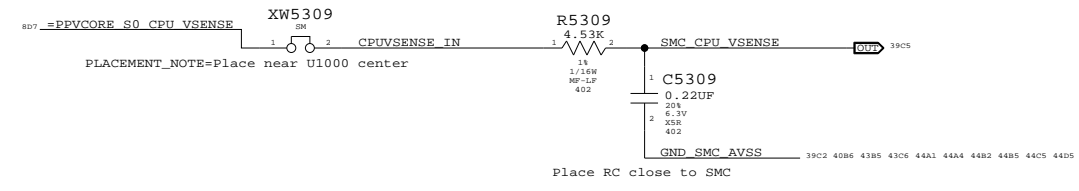




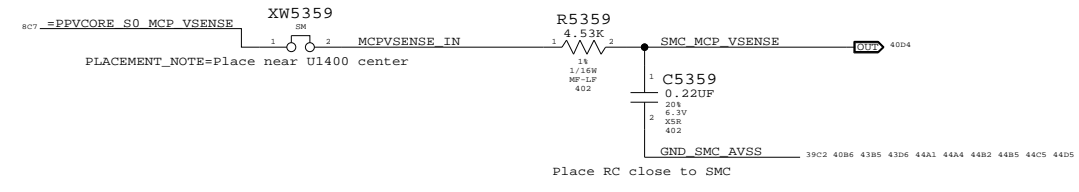
**M97 SMBUS CONNECTIONS**  
 SYNC\_MASTER=BEN SYNC\_DATE=04/21/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	52		

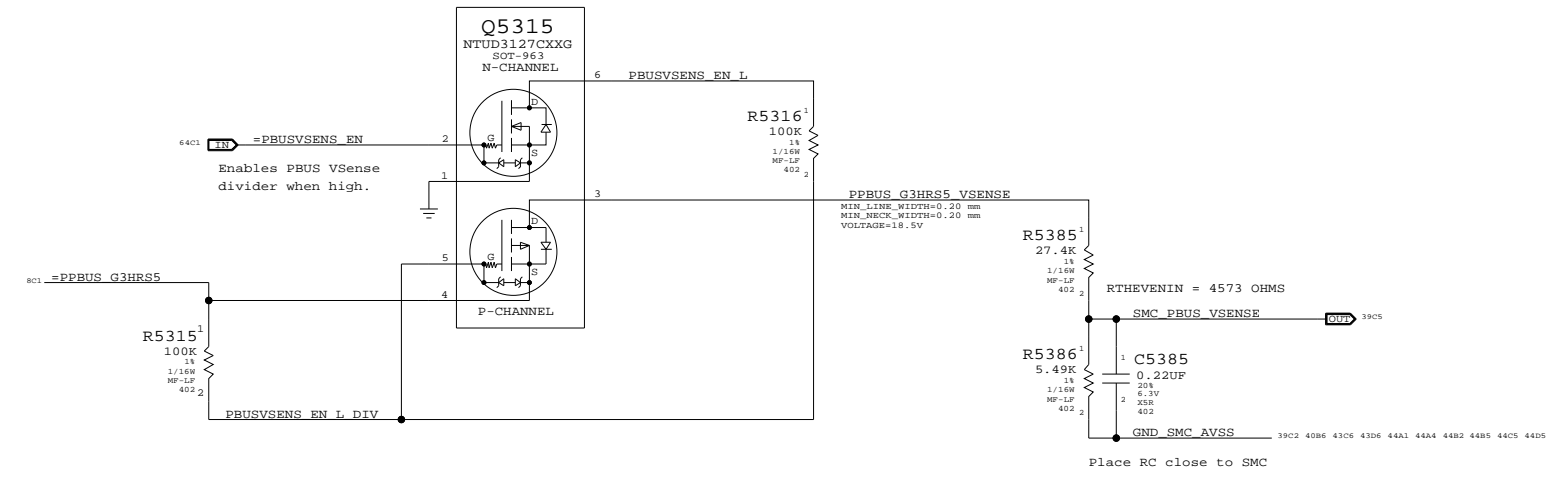
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



VOLTAGE SENSING

SYNC\_MASTER=YUNWU SYNC\_DATE=02/04/2008

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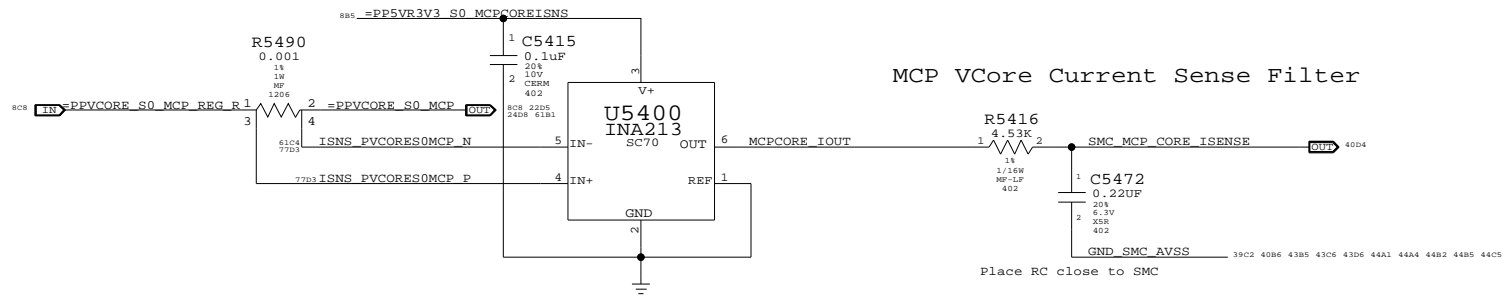
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	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	53		

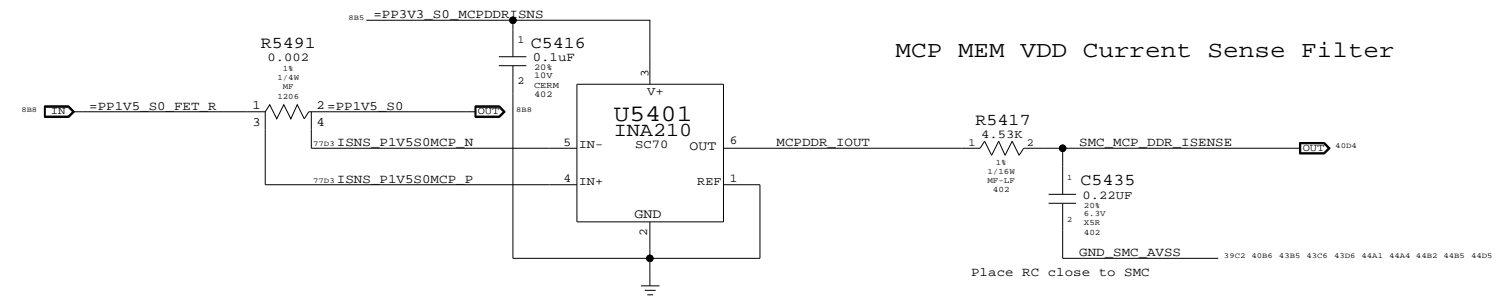
MCP VCore Current Sense



MCP VCore Current Sense Filter

Place RC close to SMC

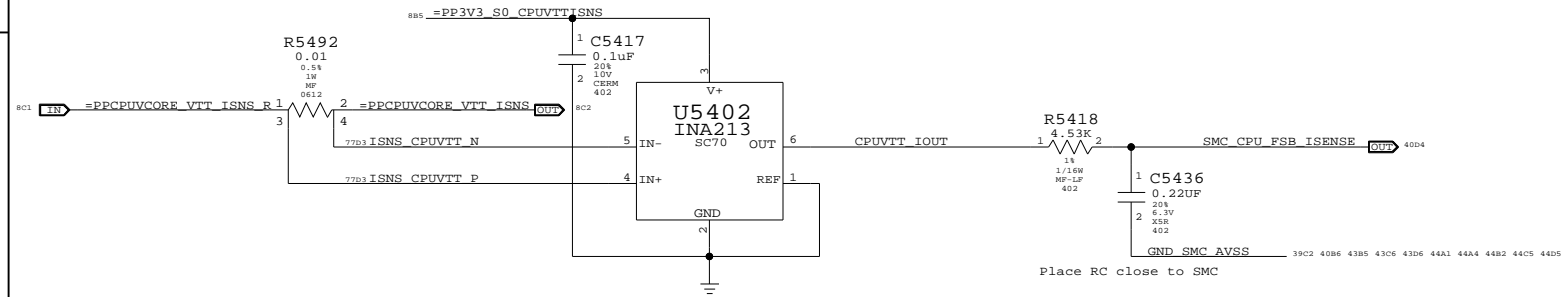
MCP MEM VDD Current Sense



MCP MEM VDD Current Sense Filter

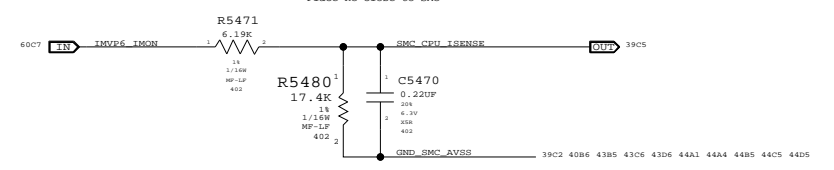
Place RC close to SMC

CPU 1.05V AND CPU VCore HIGH SIDE CURRENT SENSE



Place RC close to SMC

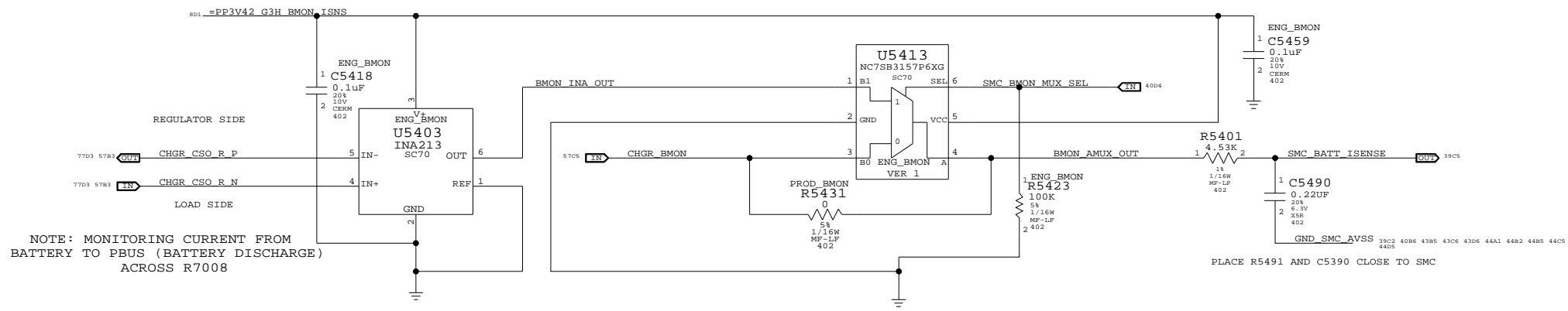
CPU VCore Load Side Current Sense / Filter



Place RC close to SMC

BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)



PLACE R5491 AND C5390 CLOSE TO SMC

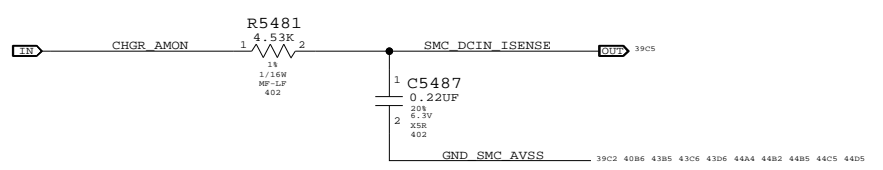
NOTE: MONITORING CURRENT FROM BATTERY TO PBUS (BATTERY DISCHARGE) ACROSS R7008

INA213 has gain of 50V/V

PLACE U5403 AND C5418 NEAR R7008

For engineering, stuff U5313 and unstuff R5330  
For production, stuff R5330 and unstuff U5313

DC-IN (AMON) CURRENT SENSE



**Current Sensing**

SYNC\_MASTER=YUNWU SYNC\_DATE=04/07/2008

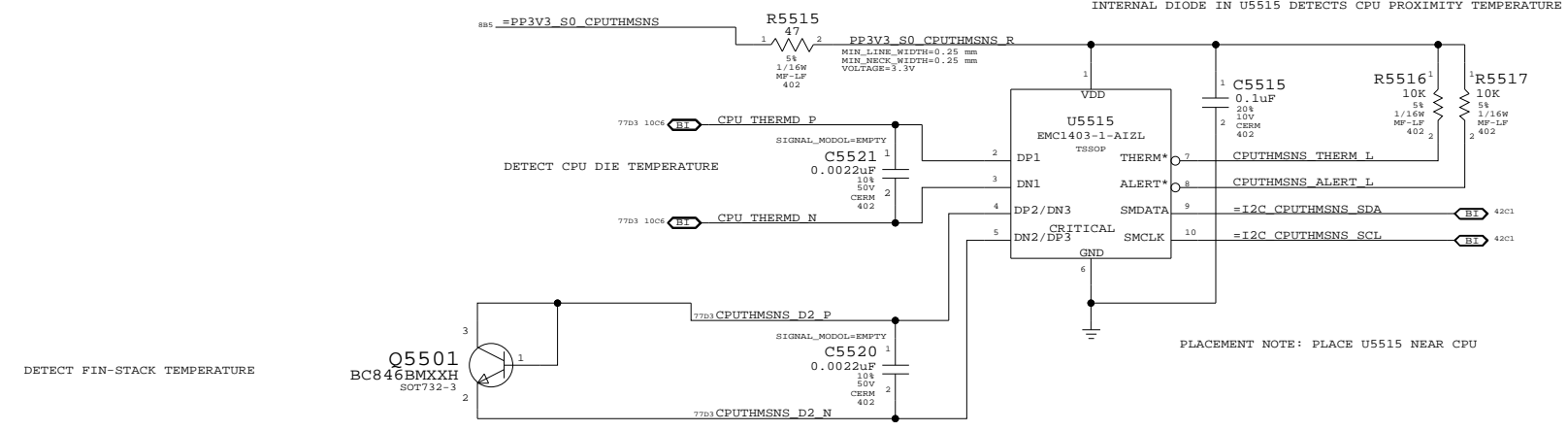
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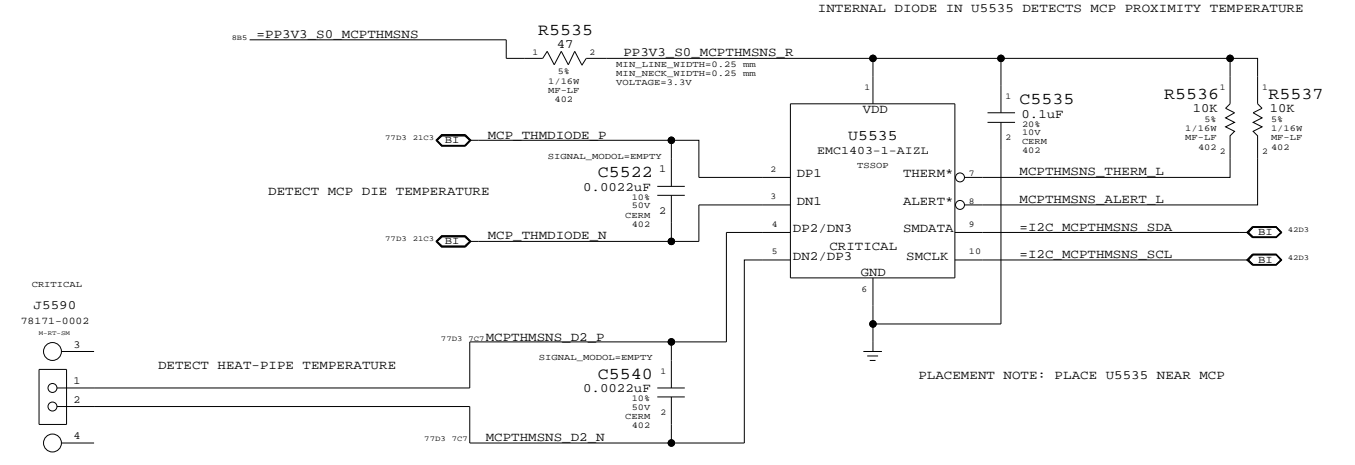
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
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	DRAWING NUMBER		REV.
	051-7918		c
SCALE		SHT	OF
NONE		54	109

### CPU T-Diode Thermal Sensor



### MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

**Thermal Sensors**

SYNC\_MASTER=YUNWU SYNC\_DATE=03/20/2008

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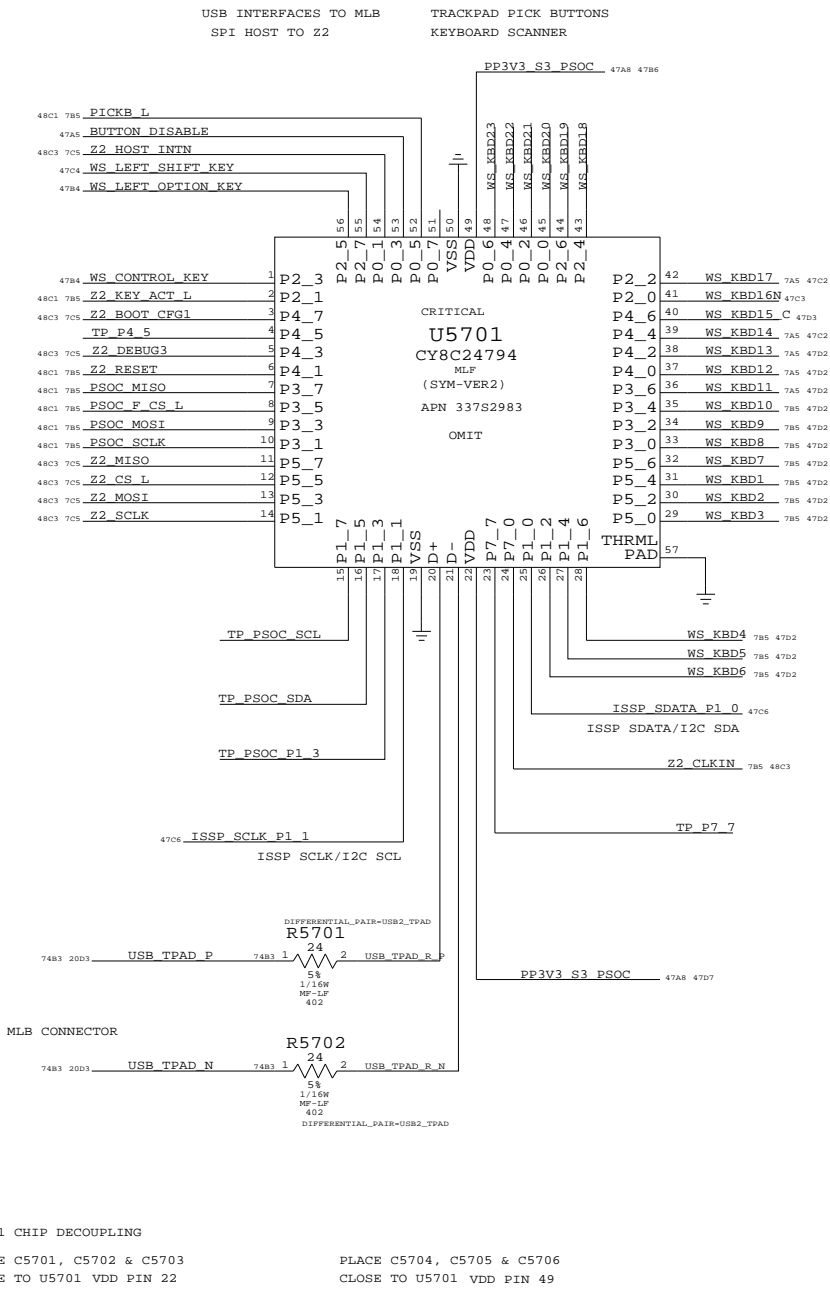
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	55		



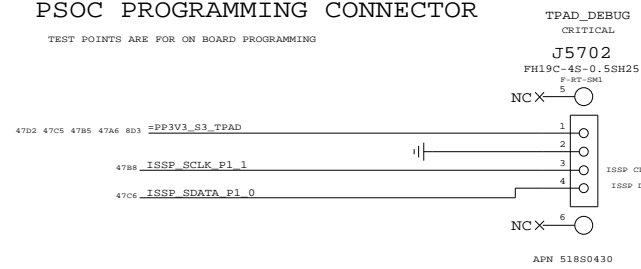
### PSOC USB CONTROLLER



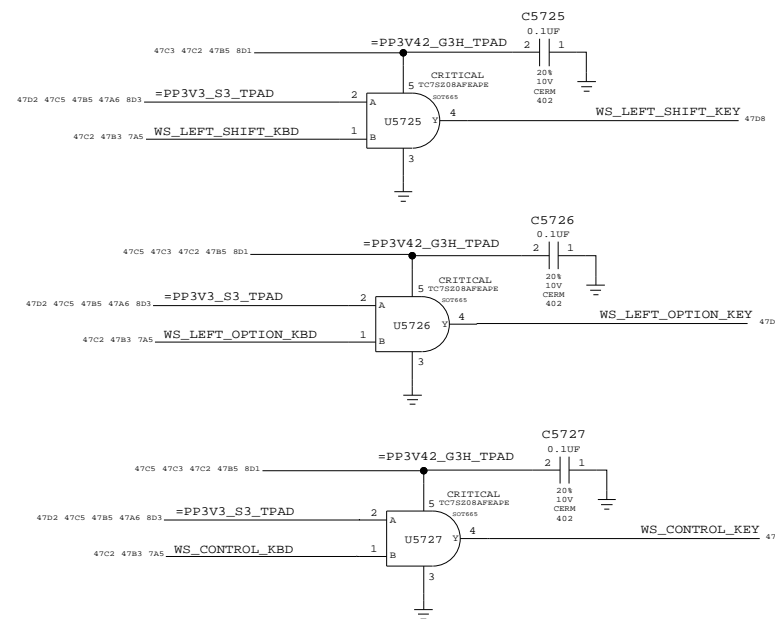
IC	PIN NAME	CURRENT	R_SMS	V_SMS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	16.32E-3 W
PSOC	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V	96E-6 W 294E-6 W
1.8V BOOSTER	VIN	49A (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

### PSOC PROGRAMMING CONNECTOR

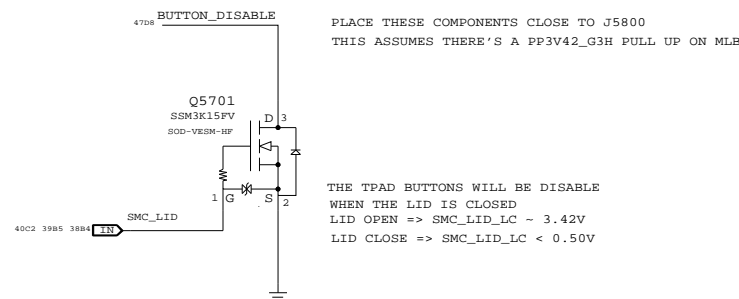
TEST POINTS ARE FOR ON BOARD PROGRAMMING



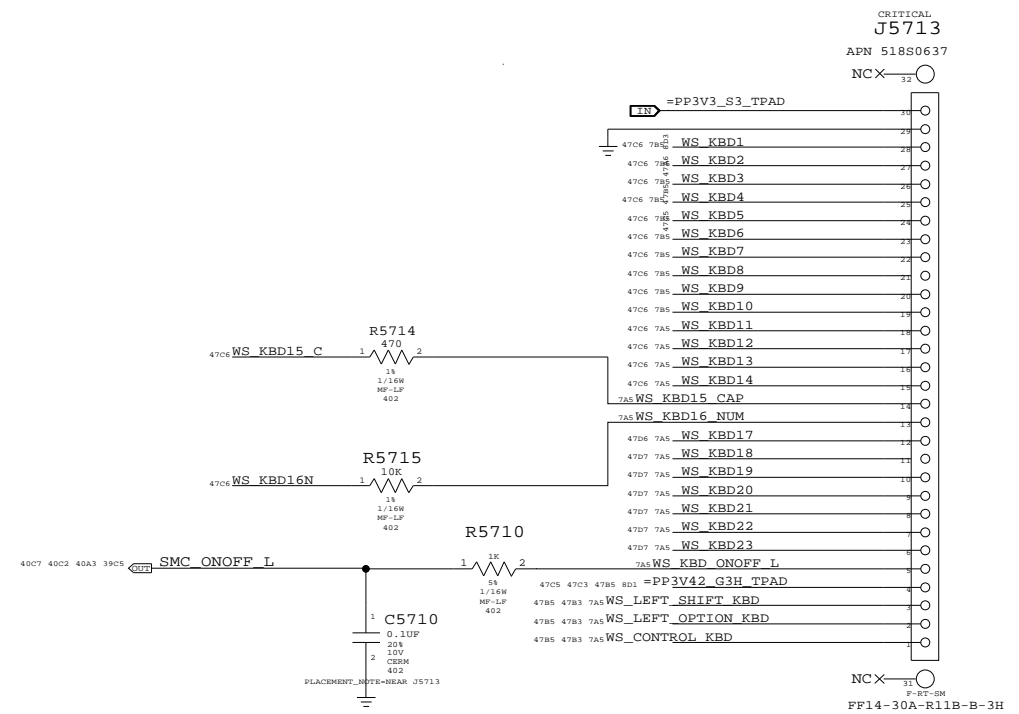
### ISOLATION CIRCUIT



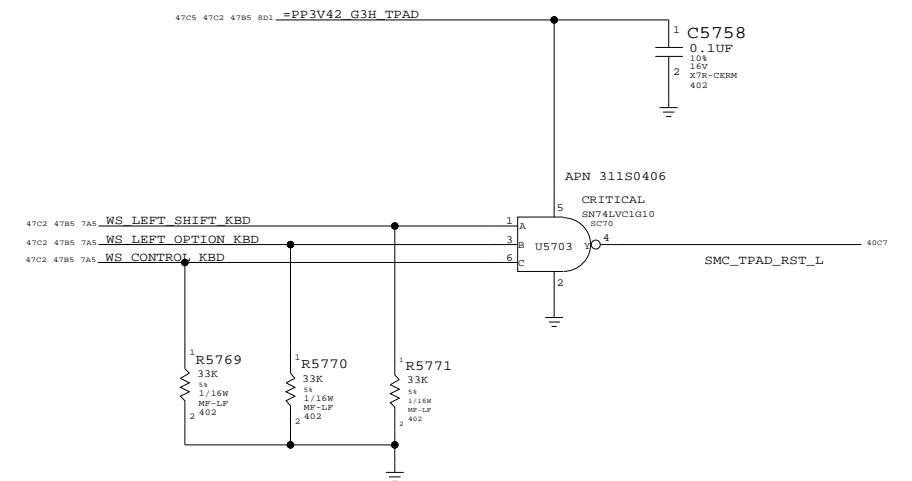
### TPAD BUTTONS DISABLE



### KEYBOARD CONNECTOR



### SMC\_MANUAL\_RESET LOGIC



### WELLSPRING 1

SYNC\_MASTER=YUAN.MA SYNC\_DATE=04/22/2008

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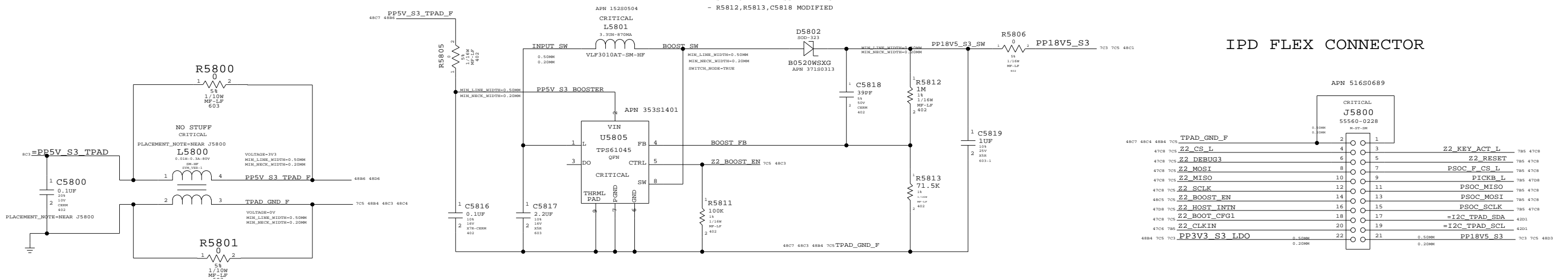


SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	57	109

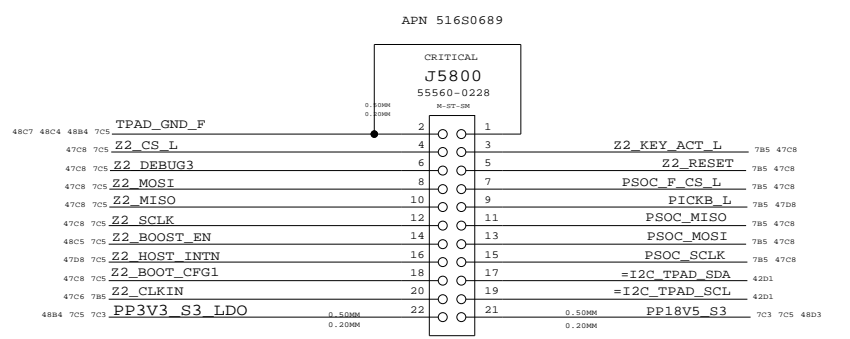
### BOOSTER +18.5VDC FOR SENSORS

#### BOOSTER DESIGN CONSIDERATION:

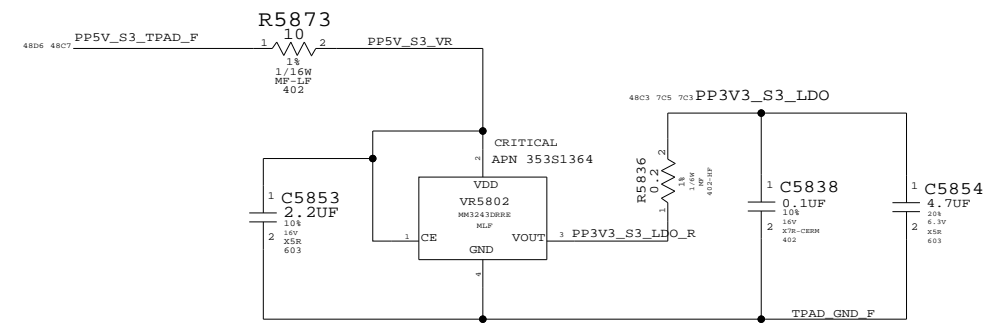
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



### IPD FLEX CONNECTOR

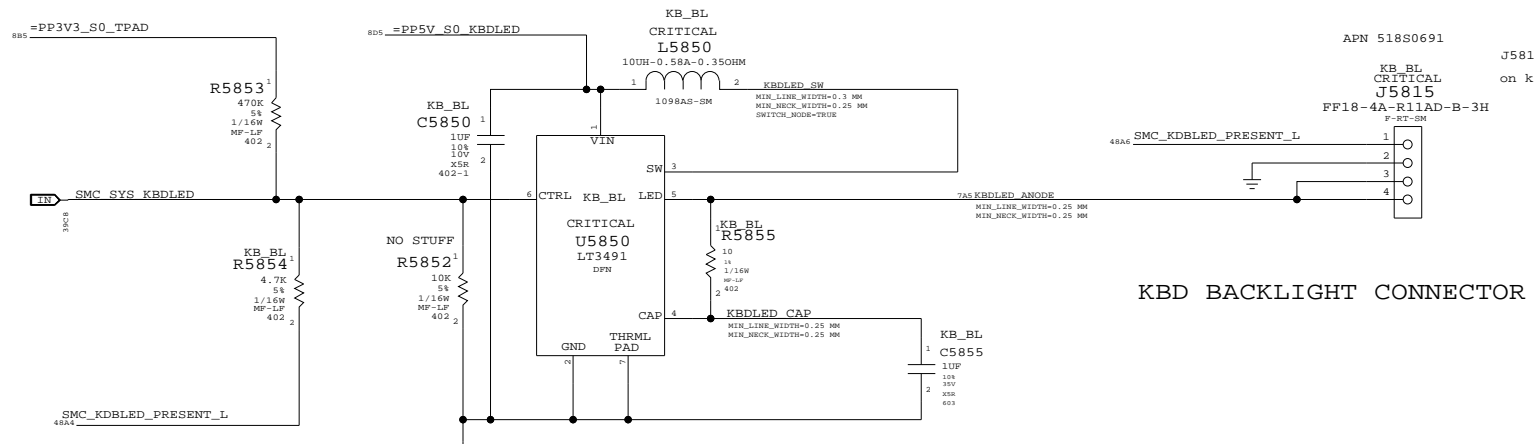


### 3V3 LDO FOR IPD



### KEYBOARD BACKLIGHT DRIVING AND DETECTION

To detect Keyboard backlight, SMC will tristate SMC\_SYS\_KBDLED:  
 LOW = keyboard backlight present  
 HIGH = keyboard backlight not present  
 BOM OPTION: KBDLED\_YES  
 TURNED ON FOR BEST MLB CONFIG  
 R5853 ALWAYS PRESENT



### KBD BACKLIGHT CONNECTOR

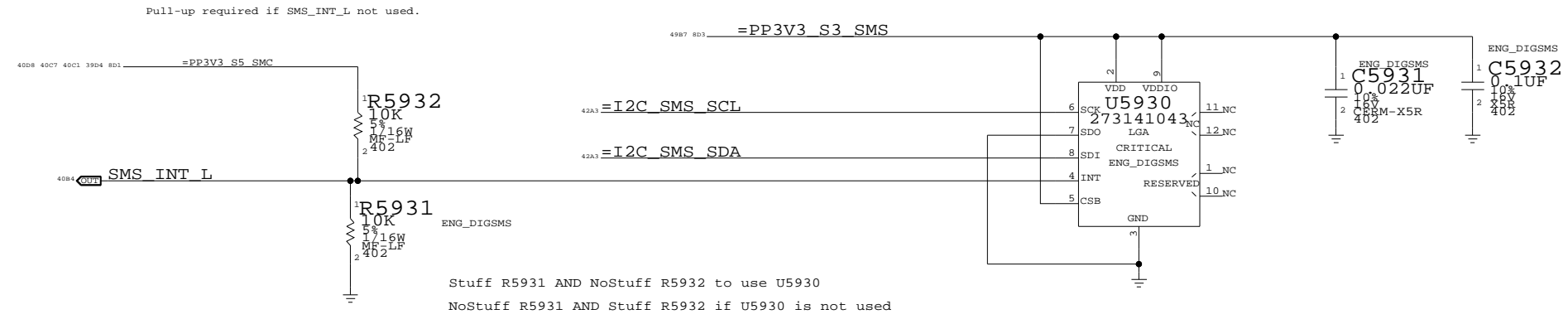
J5815 pin 1 is grounded on keyboard backlight flex

**WELLSPRING 2**  
 SYNC\_MASTER=YUAN.MA SYNC\_DATE=05/09/2008  
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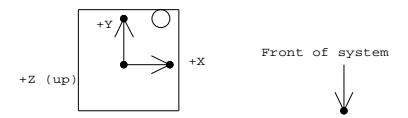
APPLE INC. DRAWING NUMBER: 051-7918 REV. C  
 SCALE: NONE SHEET: 58 OF 109



## Digital SMS

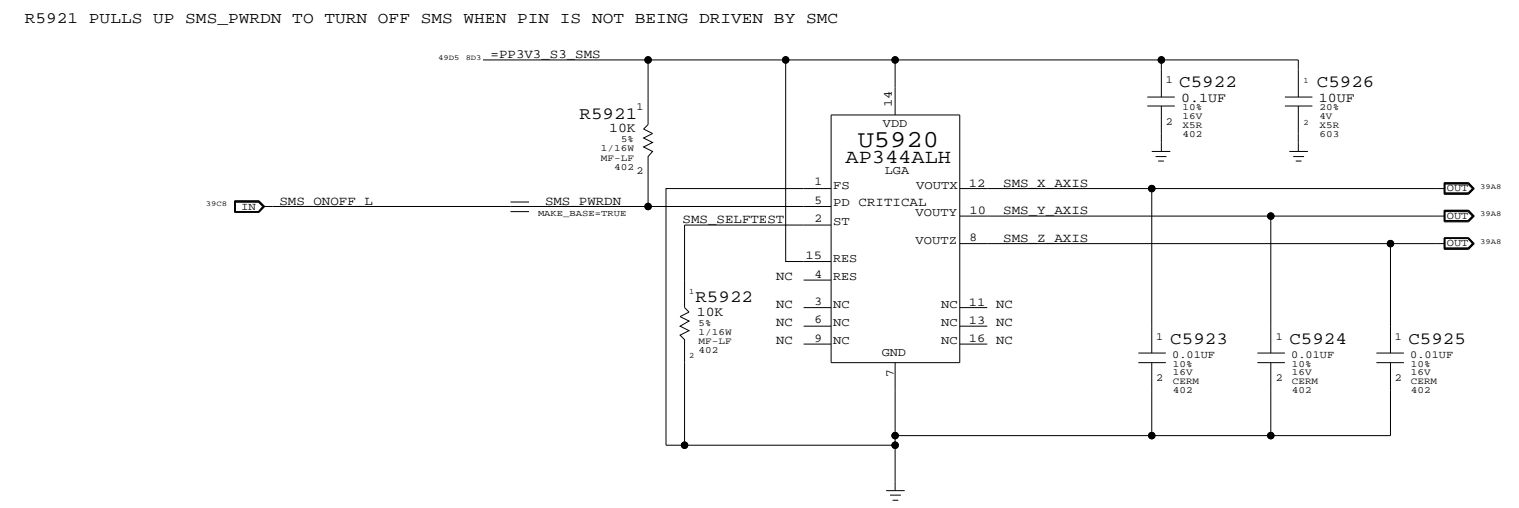


Desired orientation when placed on board top-side:

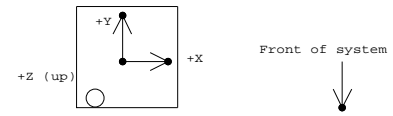


Circle indicates pin 1 location when placed in correct orientation

## Analog SMS



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

**SMS**

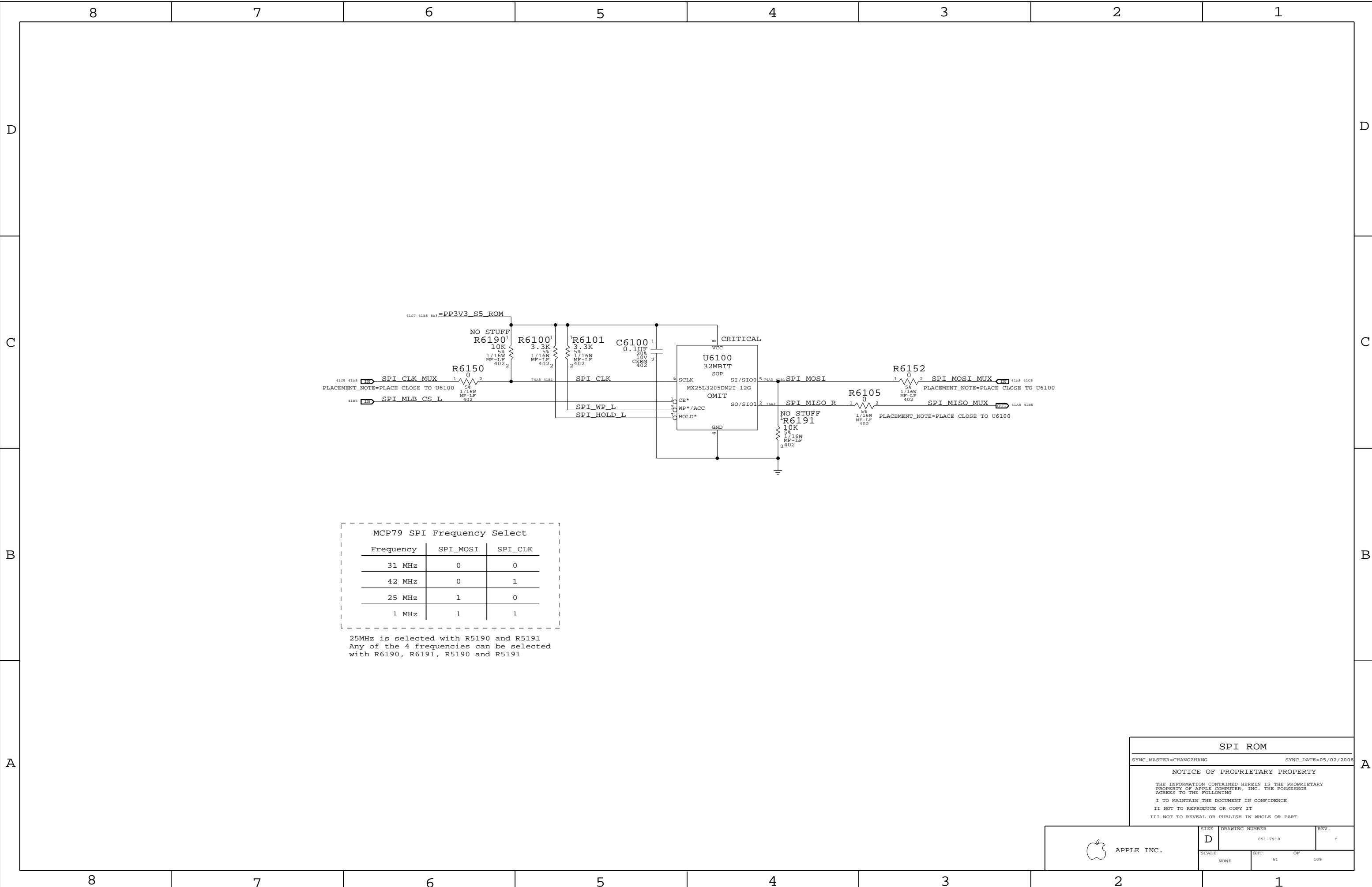
SYNC\_MASTER=YUNWU      SYNC\_DATE=06/26/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	59		



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191  
 Any of the 4 frequencies can be selected  
 with R6190, R6191, R5190 and R5191

**SPI ROM**

SYNC\_MASTER=CHANGZHANG      SYNC\_DATE=05/02/2008

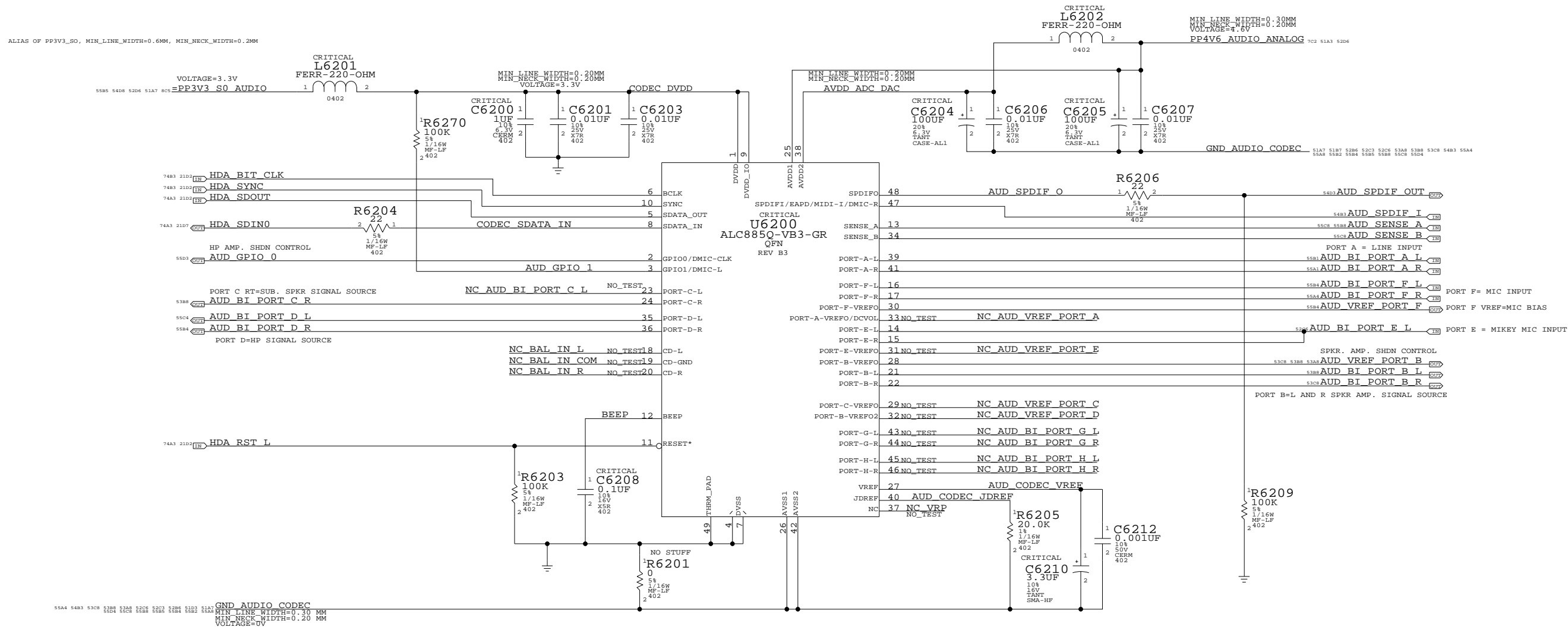
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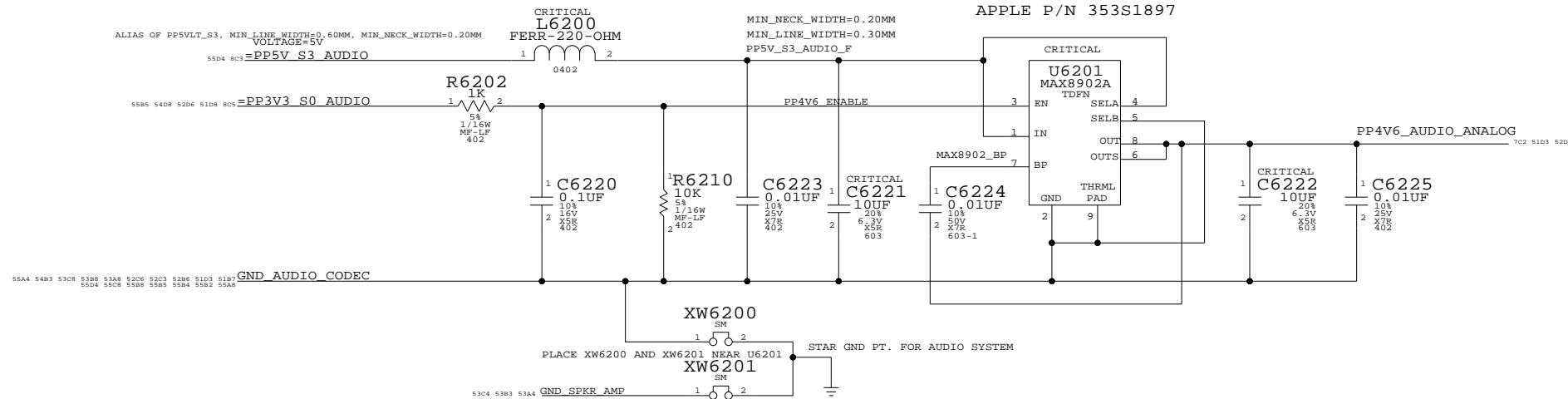
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
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	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	REV.
NONE	61	109	

**AUDIO CODEC**  
APPLE P/N 353S1538



**AUDIO 4.6V REGULATOR**  
APPLE P/N 353S1897



**AUDIO: CODEC**

SYNC\_MASTER=AUDIO SYNC\_DATE=07/01/2008

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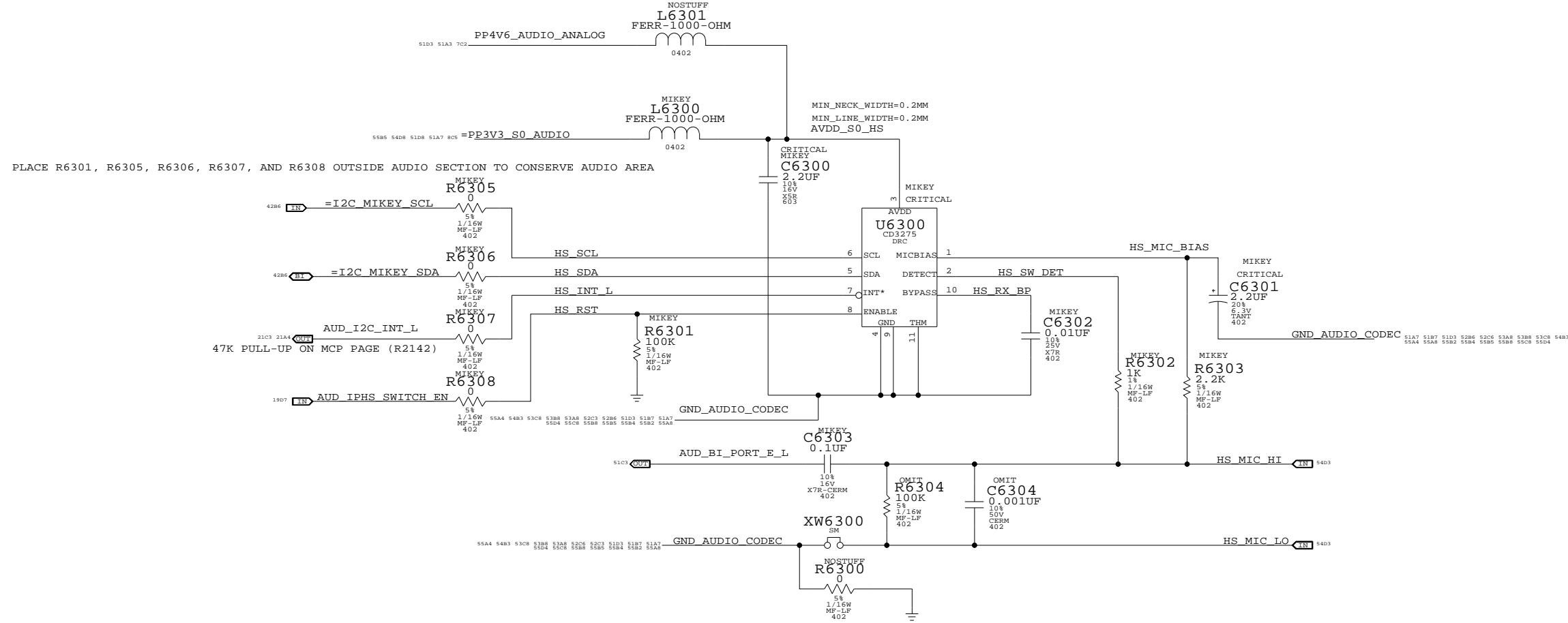
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	62		

# MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	0.001UF 50V 10% 0402 CAP	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

## AUDIO: MIKEY

SYNC\_MASTER=AUDIO SYNC\_DATE=07/03/2008

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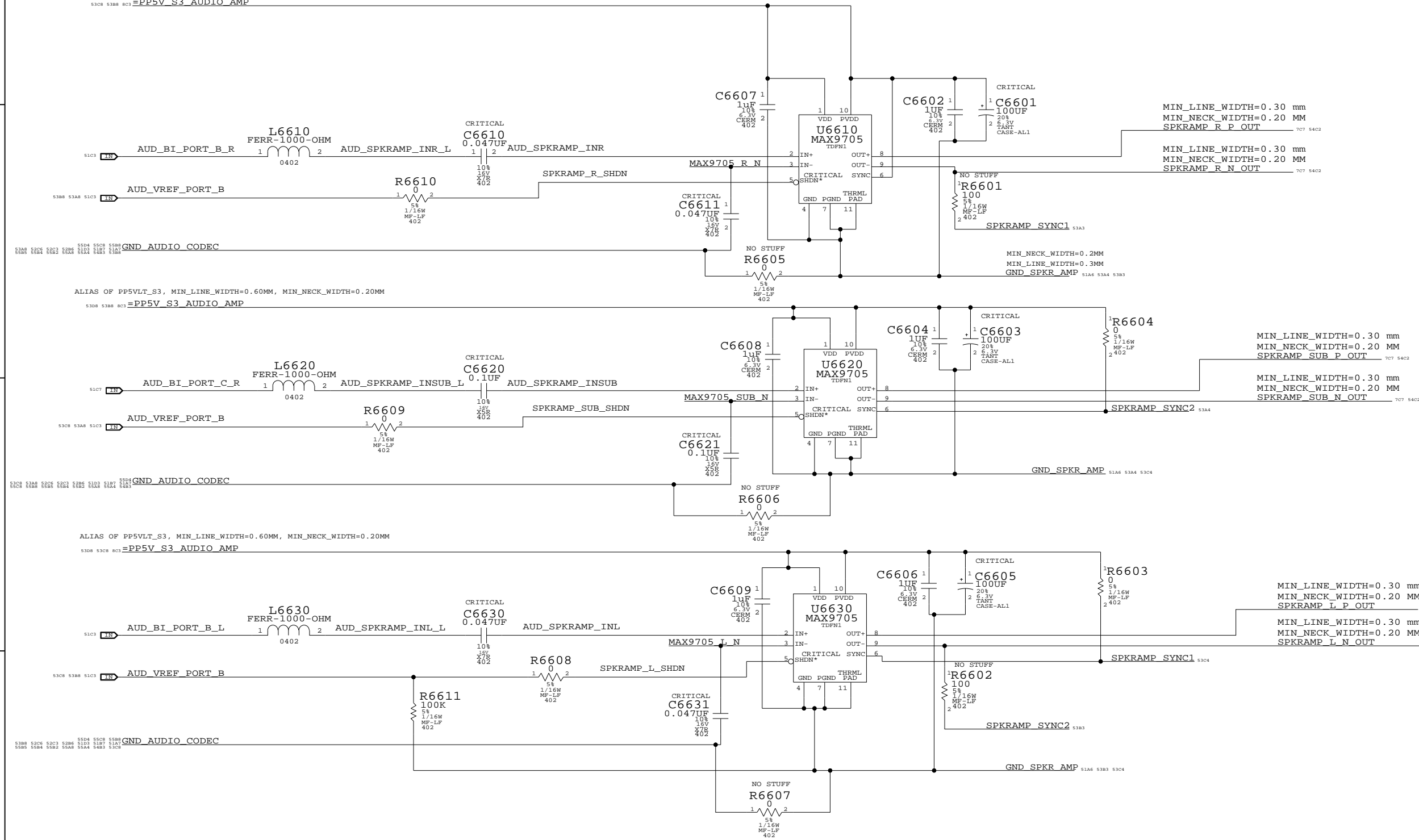


SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	63	109

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ  
 SUB 80 HZ < FC < 132 HZ  
 GAIN 12DB

ALIAS OF PP5VLT\_S3, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM  
 VOLTAGE=5V  
 5308 5388 RC1=PP5V\_S3\_AUDIO\_AMP



MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_R\_P\_OUT 707 5402

MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_R\_N\_OUT 707 5402

MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_SUB\_P\_OUT 707 5402

MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_SUB\_N\_OUT 707 5402

MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_L\_P\_OUT 707 5402

MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 MM  
 SPKRAMP\_L\_N\_OUT 707 5402

**AUDIO: SPEAKER AMP**  
 SYNC\_MASTER=AUDIO SYNC\_DATE=07/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	66		

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

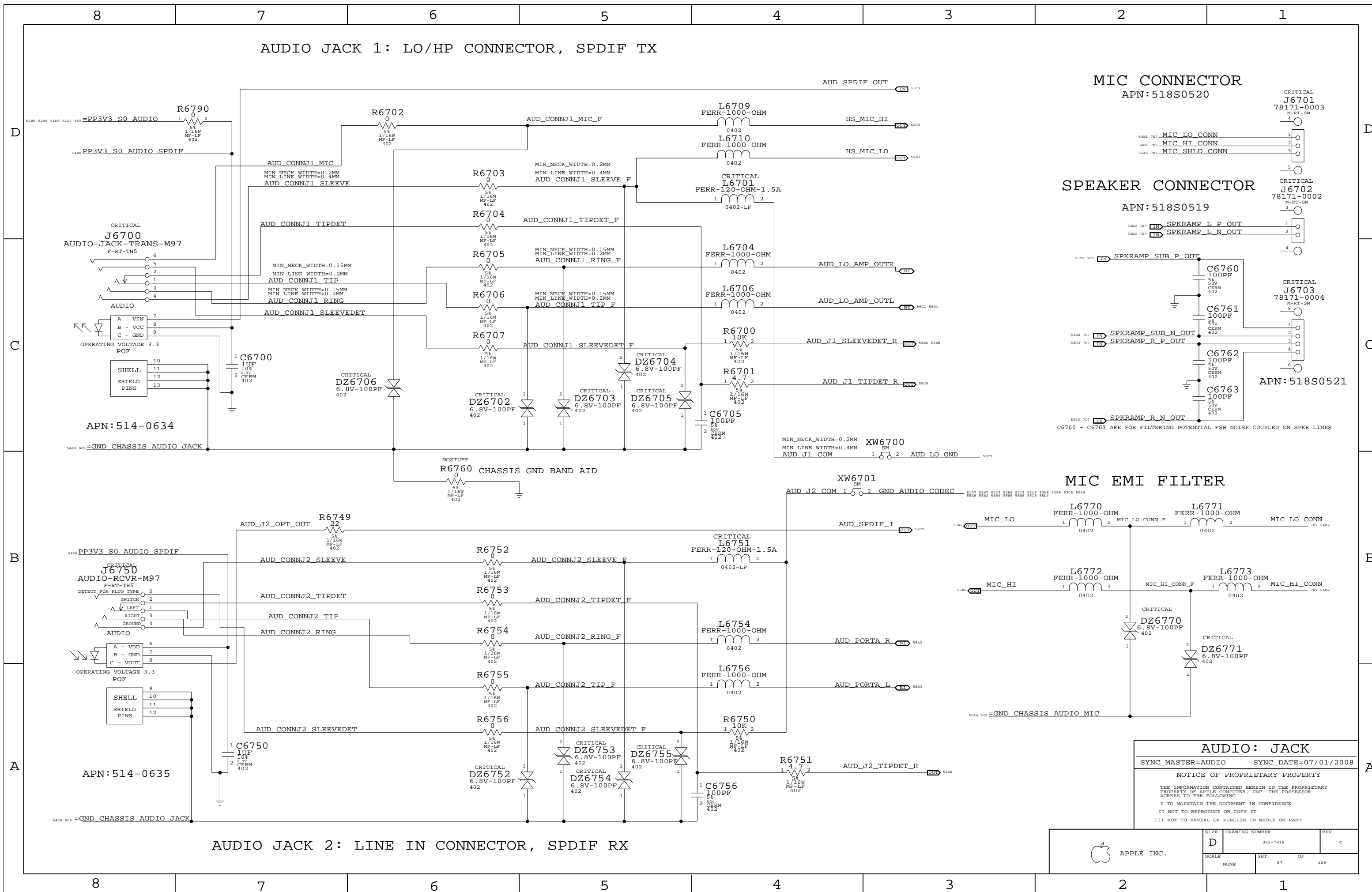
MIC CONNECTOR  
APN: 518S0520

SPEAKER CONNECTOR  
APN: 518S0519

MIC EMI FILTER

AUDIO: JACK

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



SYNC\_MASTER=AUDIO SYNC\_DATE=07/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	67		

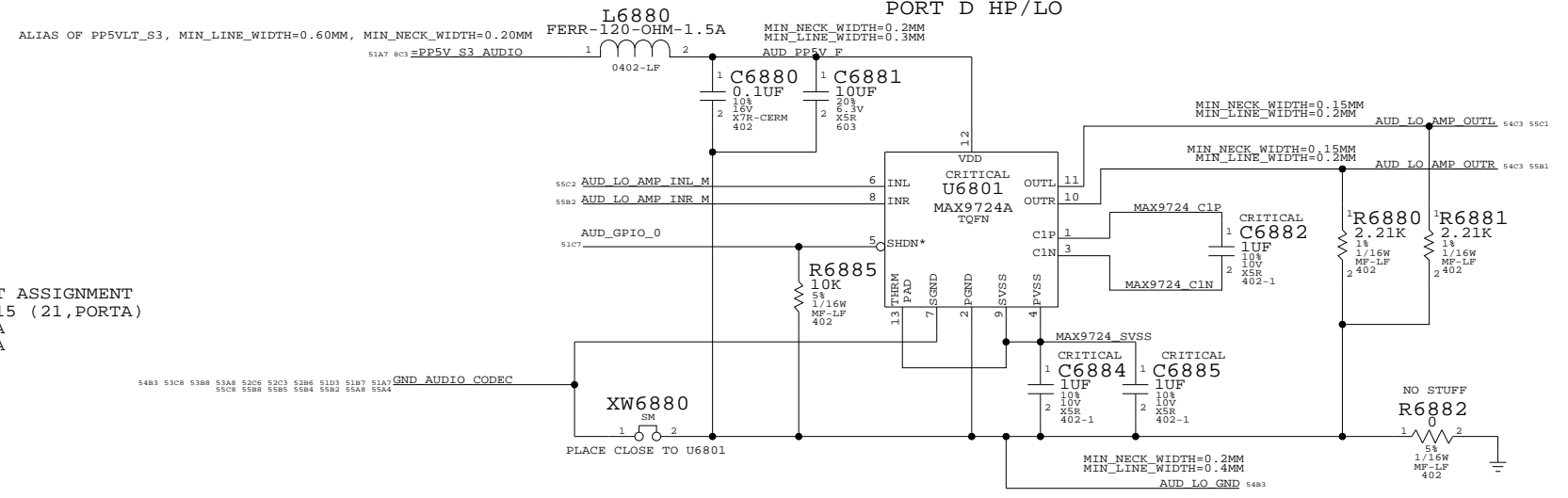
HP/LO AMP  
APN: 353S1637  
PORT D HP/LO

CODEC OUTPUT SIGNAL PATHS

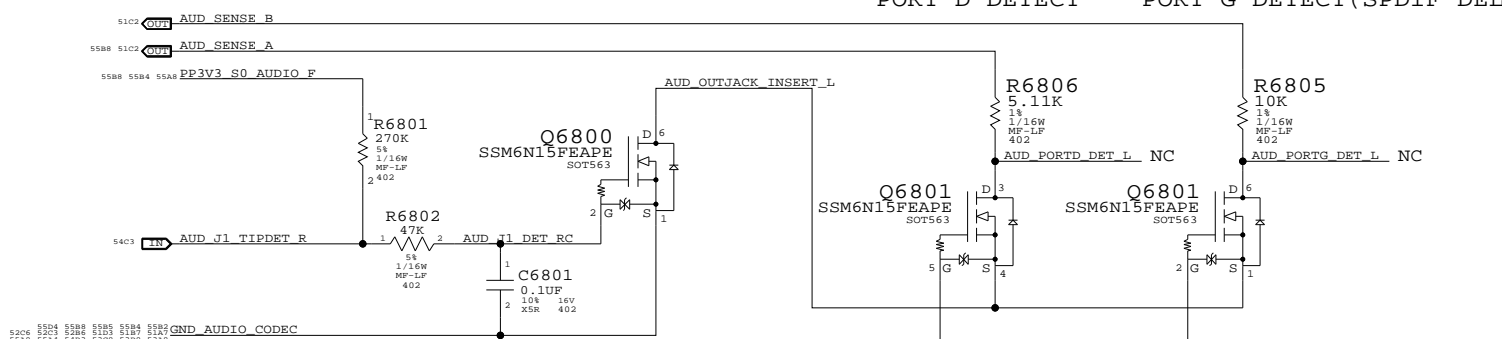
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0C (12)	0X02 (2)	0X14 (20,PORTD)	GPIO 0	0X14 (20,PORTD)
SAT SPKRS	0X0D (13)	0X03 (3)	0X18 (24,PORTB)	VREF_B(100%)	N/A
SUB SPKR	0X0F (15)	0X05 (5)	0X1A (26,PORTC)	VREF_B(100%)	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X16 (22, PORTG)

CODEC INPUT SIGNAL PATHS

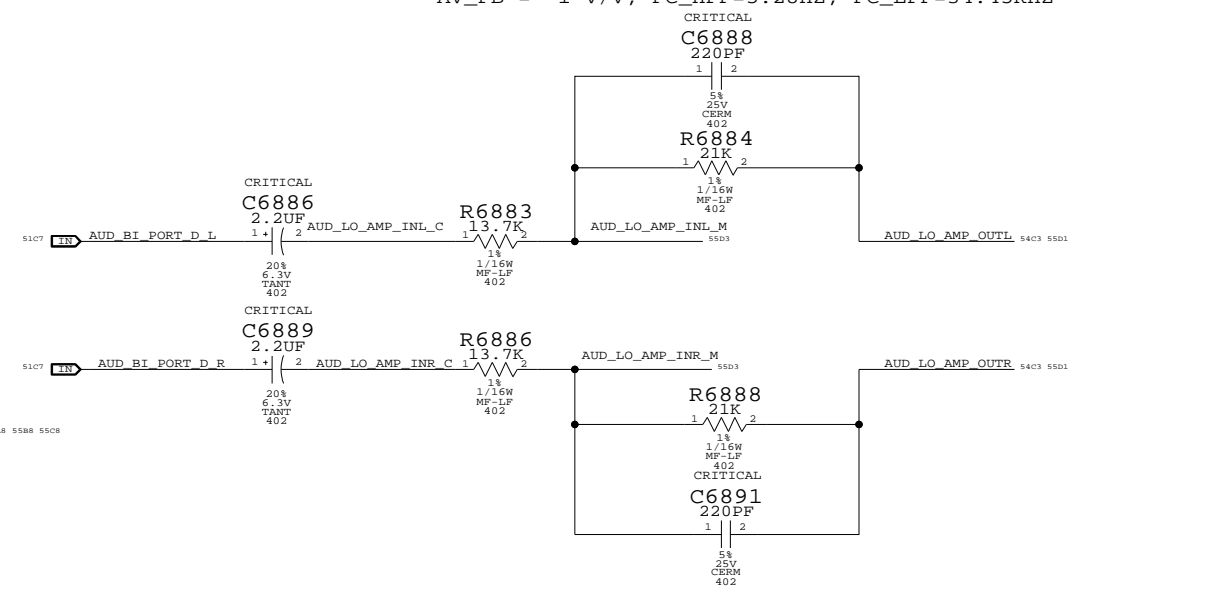
FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X15 (21,PORTA)	N/A	0X15 (21,PORTA)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X19 (25,PORTF)	VREF_F (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A



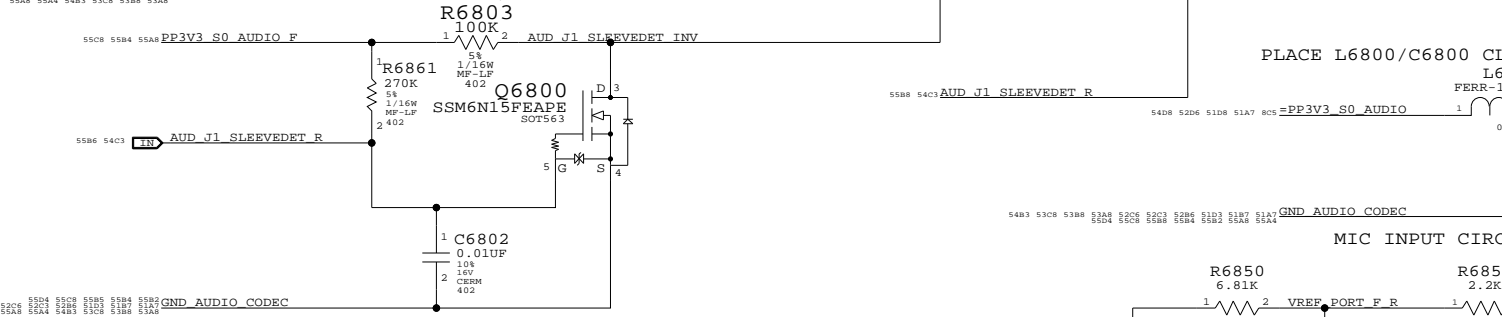
PORT D DETECT PORT G DETECT (SPDIF DELEGATE)



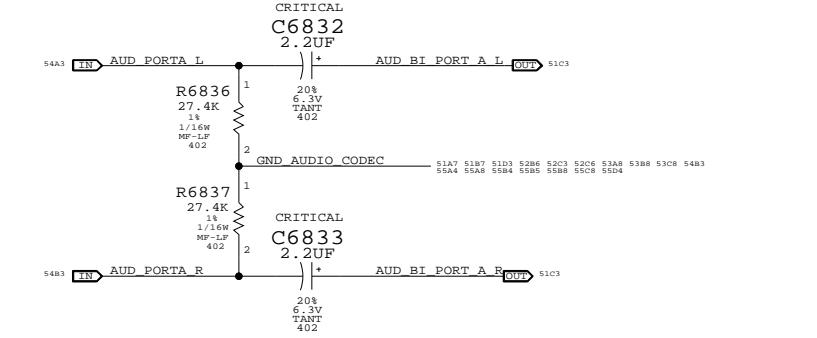
MAX9724 GAIN/FILTER COMPONENTS  
AV\_PB = -1 V/V, FC\_HPF=5.28HZ, FC\_LPF=34.45KHZ



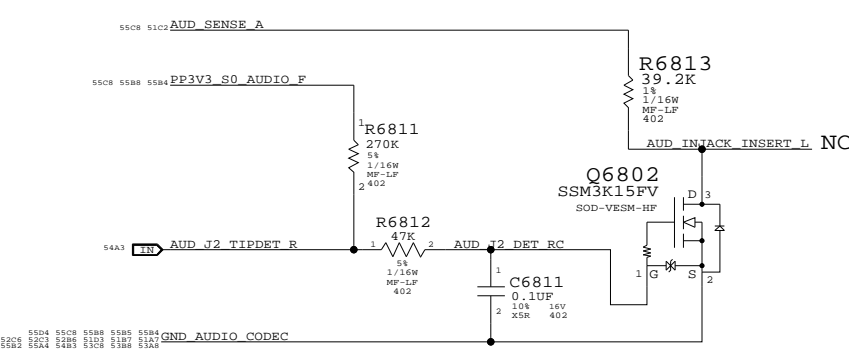
PLACE L6800/C6800 CLOSE TO Q6800



PORT A LI



LINE-IN (PORT A) DETECT



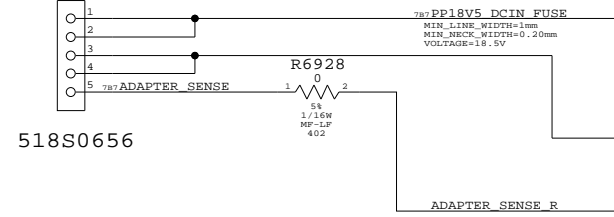
**AUDIO: JACK TRANSLATORS**  
SYNC\_MASTER=AUDIO SYNC\_DATE=07/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	68		

# MagSafe DC Power Jack

CRITICAL  
J6900  
78048-0573  
M-RT-SM



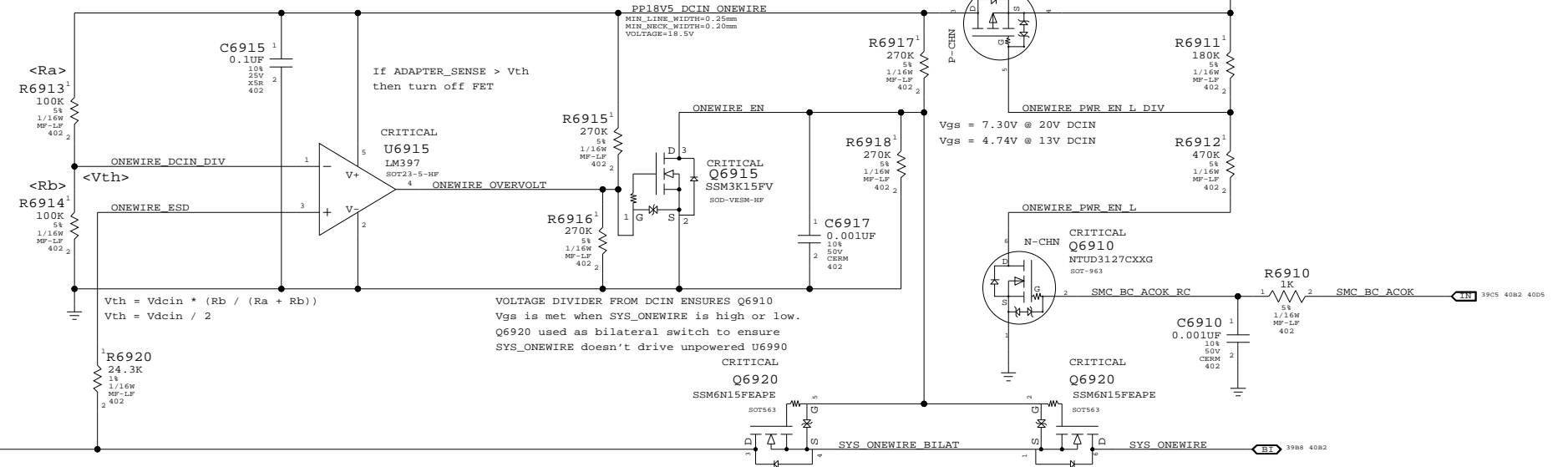
518S0656

CRITICAL  
F6905  
6AMP-24V

1206-1

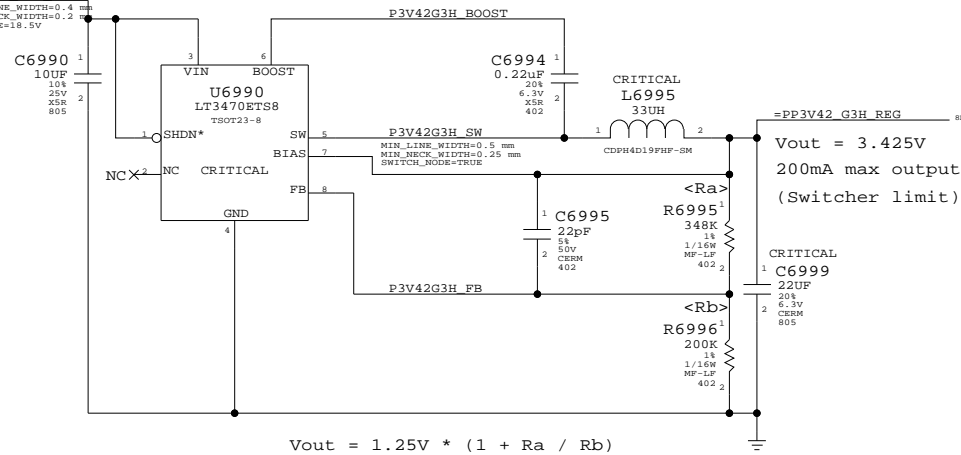
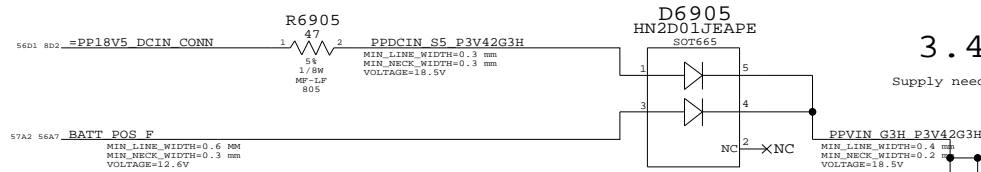
Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

## 1-Wire OverVoltage Protection

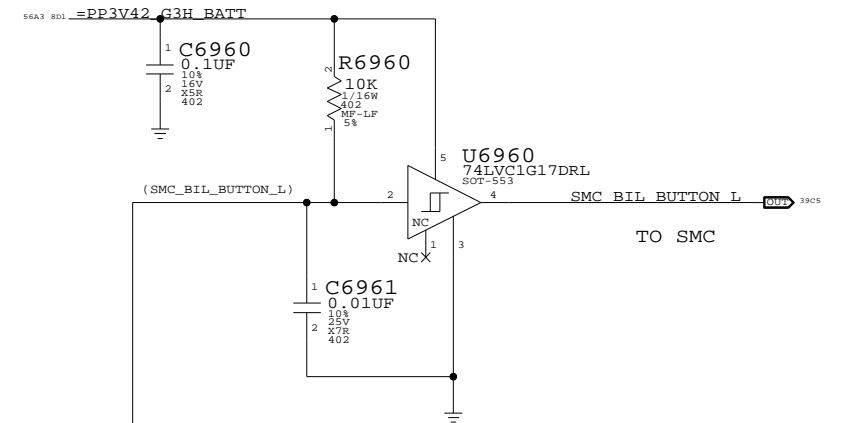


## 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

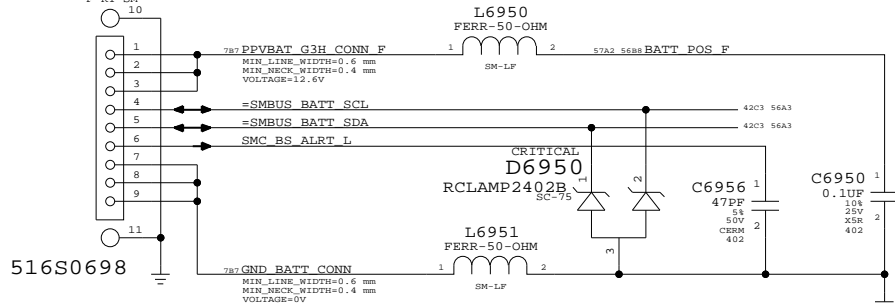


## BIL BUTTON DEBOUNCE CIRCUIT



## BATTERY POWER CONNECTOR

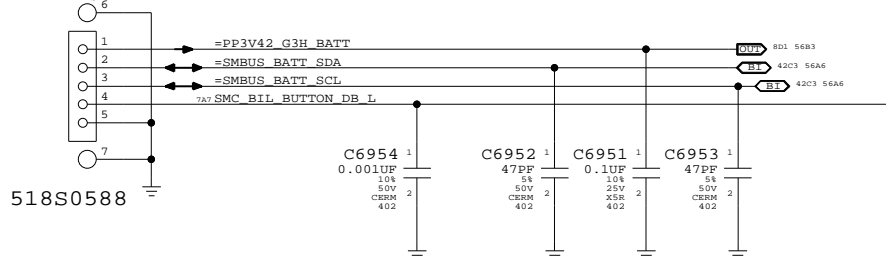
CRITICAL  
J6950  
BAT-M98  
F-RT-SM



516S0698

## BATTERY SIGNAL CONNECTOR

CRITICAL  
J6955  
78171-0005  
M-RT-SM



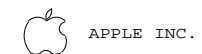
518S0588

### DC-In & Battery Connectors

SYNC\_MASTER=JACK SYNC\_DATE=03/13/2008

#### NOTICE OF PROPRIETARY PROPERTY

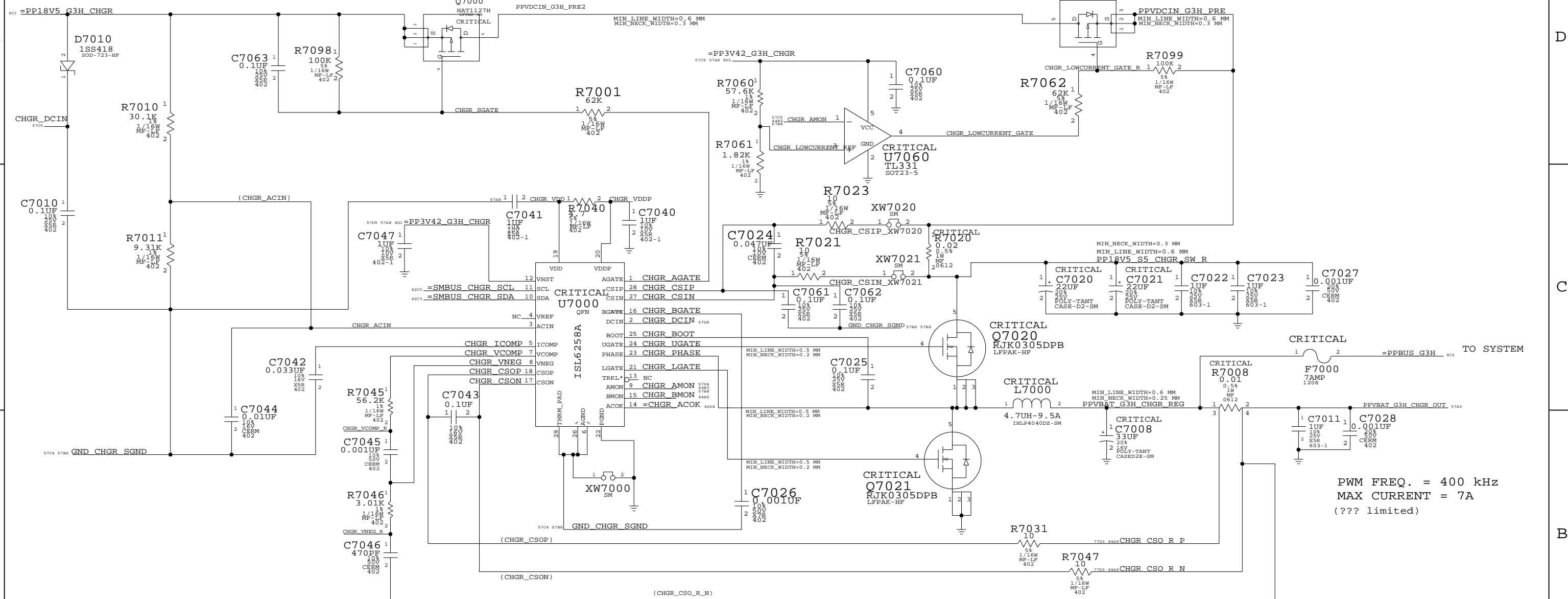
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SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	69	109



# PBUS SUPPLY / BATTERY CHARGER



PWM FREQ. = 400 kHz  
MAX CURRENT = 7A  
(??? limited)

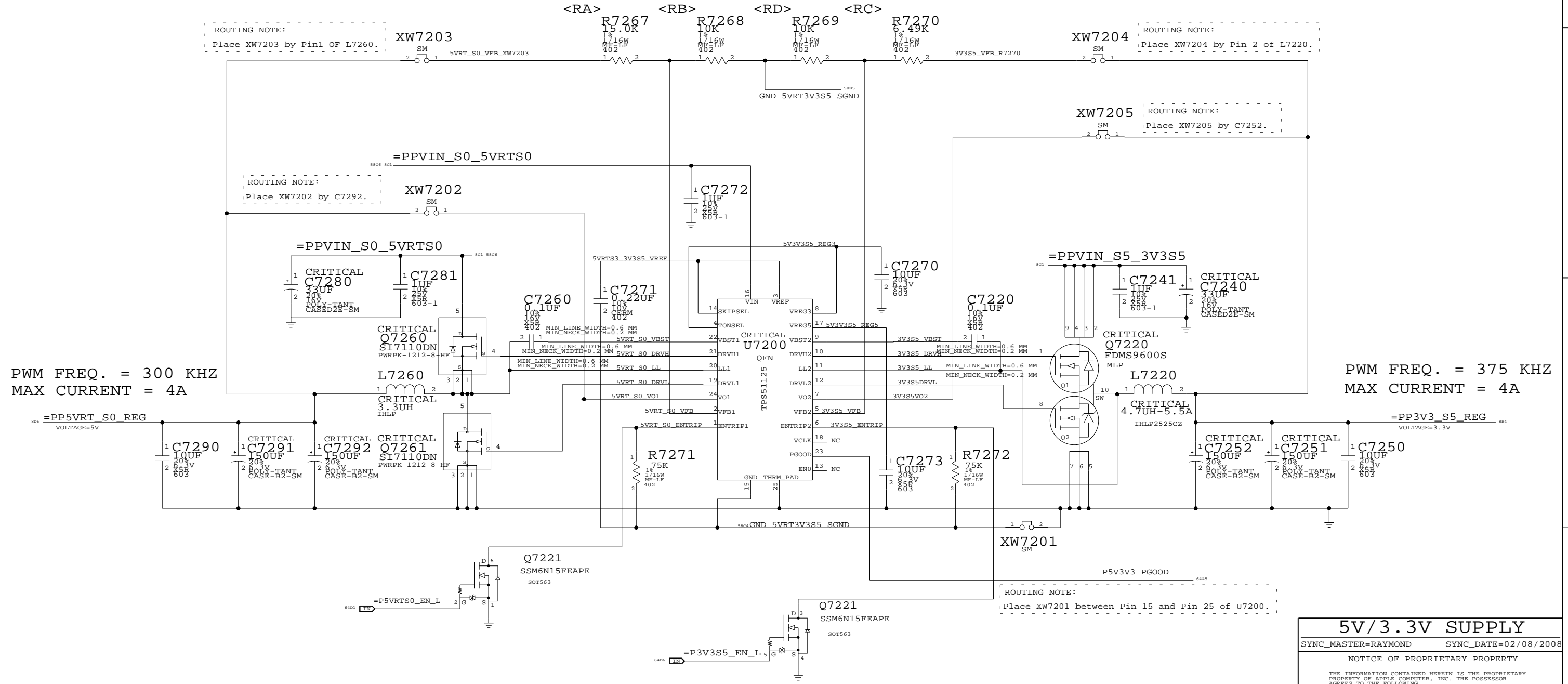
**PBUS Supply/Battery Charger**  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=01/31/2008  
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHEET 70	OF 109

# 5V\_RT/3.3V POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

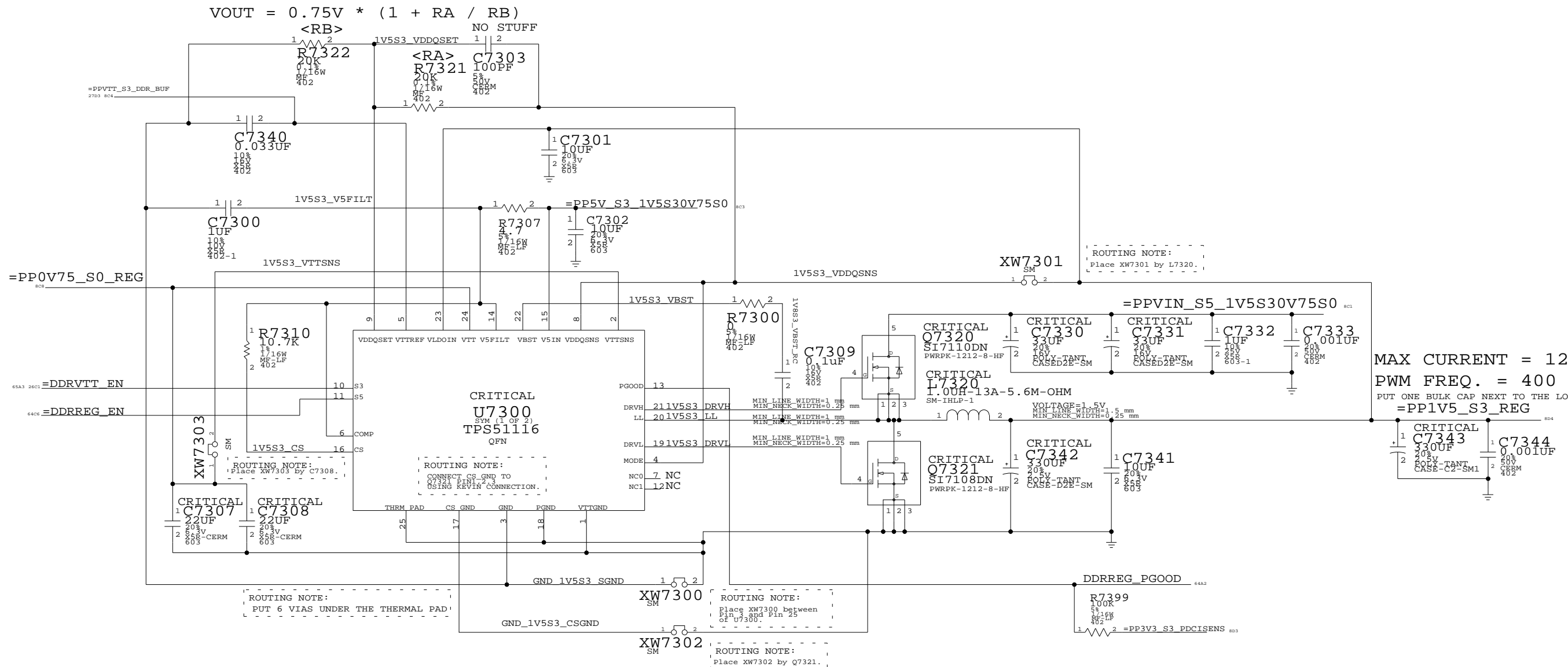
$$V_{OUT} = (2 * R_C / R_D) + 2$$



**5V/3.3V SUPPLY**  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=02/08/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	72		

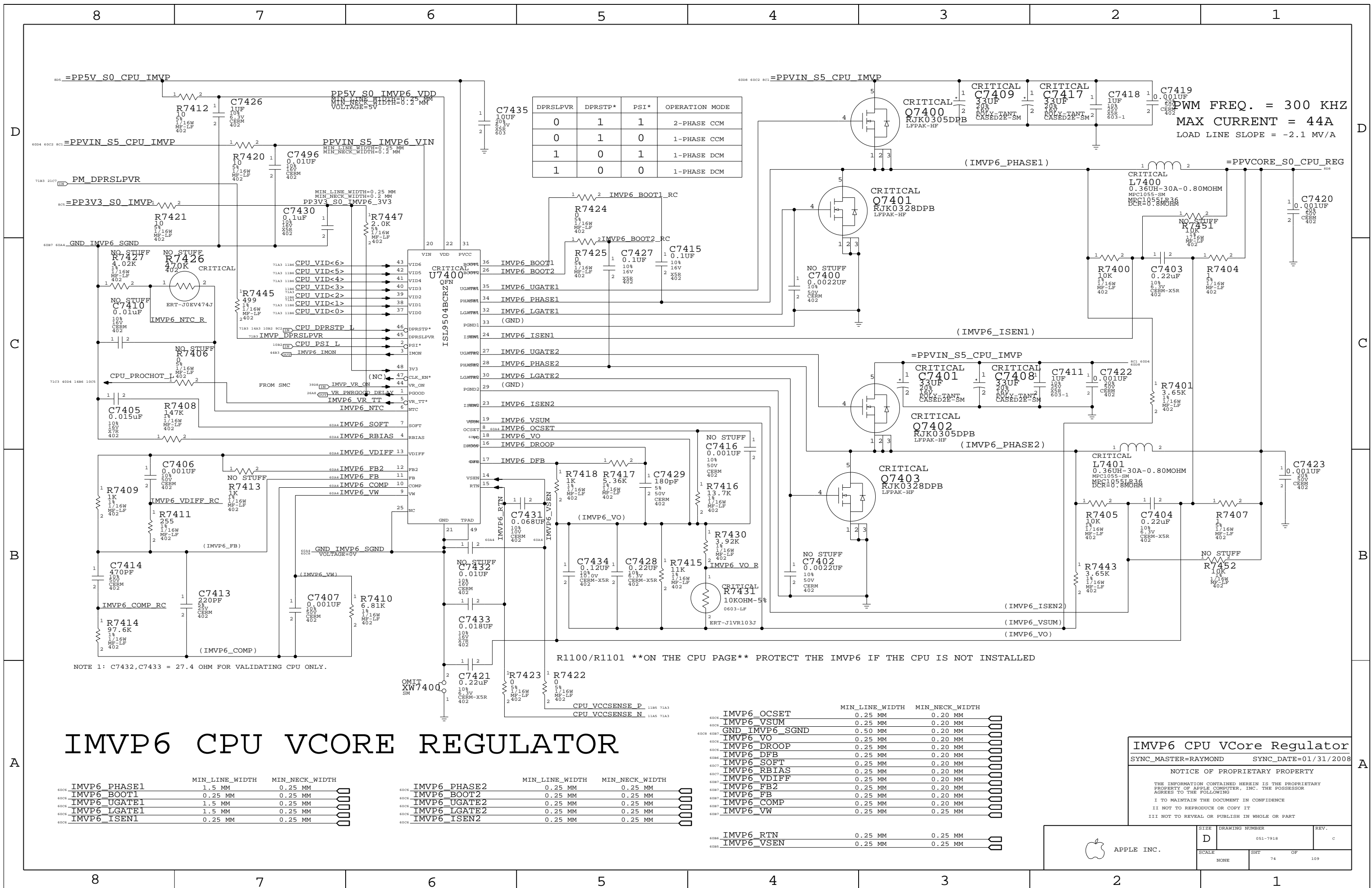
# 1.5V/0.75V (DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

**1.5V/0.75V DDR3 SUPPLY**  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=01/31/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	73		



DPRSPLVVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ  
 MAX CURRENT = 44A  
 LOAD LINE SLOPE = -2.1 MV/A

R1100/R1101 \*\*ON THE CPU PAGE\*\* PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6 PHASE1	1.5 MM	0.25 MM
IMVP6 BOOT1	0.25 MM	0.25 MM
IMVP6 UGATE1	1.5 MM	0.25 MM
IMVP6 LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6 PHASE2	0.25 MM	0.25 MM
IMVP6 BOOT2	0.25 MM	0.25 MM
IMVP6 UGATE2	0.25 MM	0.25 MM
IMVP6 LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

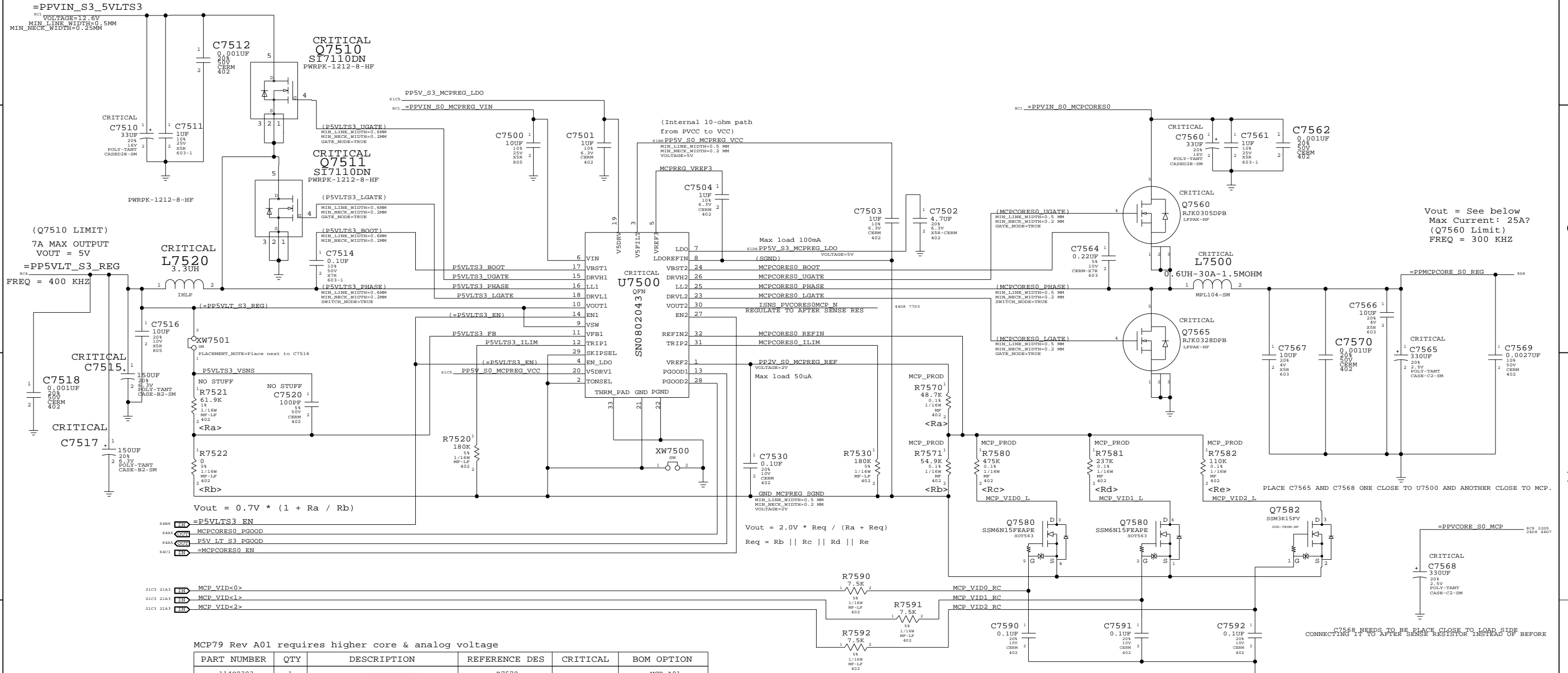
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=01/31/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHEET	OF	
NONE	74	109	

# MCP VCORE / 5V\_S3 LEFT REGULATOR



(Q7510 LIMIT)  
7A MAX OUTPUT  
VOUT = 5V  
FREQ = 400 KHZ

$$V_{out} = 0.7V * (1 + R_a / R_b)$$

$$V_{out} = 2.0V * R_{eq} / (R_a + R_{eq})$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

Vout = See below  
Max Current: 25A?  
(Q7560 Limit)  
FREQ = 300 KHZ

- 6486 **EN** =P5VLT3\_EN
- 6485 **PGOOD** =MCPCORESO\_PGOOD
- 6484 **PGOOD** =P5V LT S3\_PGOOD
- 6481 **EN** =MCPCORESO\_EN
- 21C3 21A3 **VID<0>**
- 21C3 21A3 **VID<1>**
- 21C3 21A3 **VID<2>**

MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES.MTL.FILM,1/16W,49.9K,1,0402,SMD,LP	R7570		MCP_A01
114S0401	1	RES.MTL.FILM,1/16W,78.7K,1,0402,SMD,LP	R7571		MCP_A01
114S0484	1	RES.MTL.FILM,1/16W,849K,1,0402,SMD,LP	R7580		MCP_A01
114S0454	1	RES.MTL.FILM,1/16W,274K,1,0402,SMD,LP	R7581		MCP_A01
114S0423	1	RES.MTL.FILM,1/16W,133K,1,0402,SMD,LP	R7582		MCP_A01
114S0373	1	RES.MTL.FILM,1/16W,40.2K,1,0402,SMD,LP	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES.MTL.FILM,1/16W,84.5K,1,0402,SMD,LP	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES.MTL.FILM,1/16W,301K,1,0402,SMD,LP	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES.MTL.FILM,1/16W,237K,1,0402,SMD,LP	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES.MTL.FILM,1/16W,100K,1,0402,SMD,LP	R7582		MCP_A01P&MCP_A01Q

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:  
 Added C7568 bulk cap on output.  
 Tied TON to REF.  
 Changed Q7510 to 376S0674.  
 C7500 changed to 138S0638.  
 L7560 changed from T18 MLB inductor to 152S0782.  
 Changed Q7565 to 376S0637.  
 Changed R7514 to 280K, R7564 to 180K.

**MCP VCORE REGULATOR**

SYNC\_MASTER=RAYMOND SYNC\_DATE=01/31/2008

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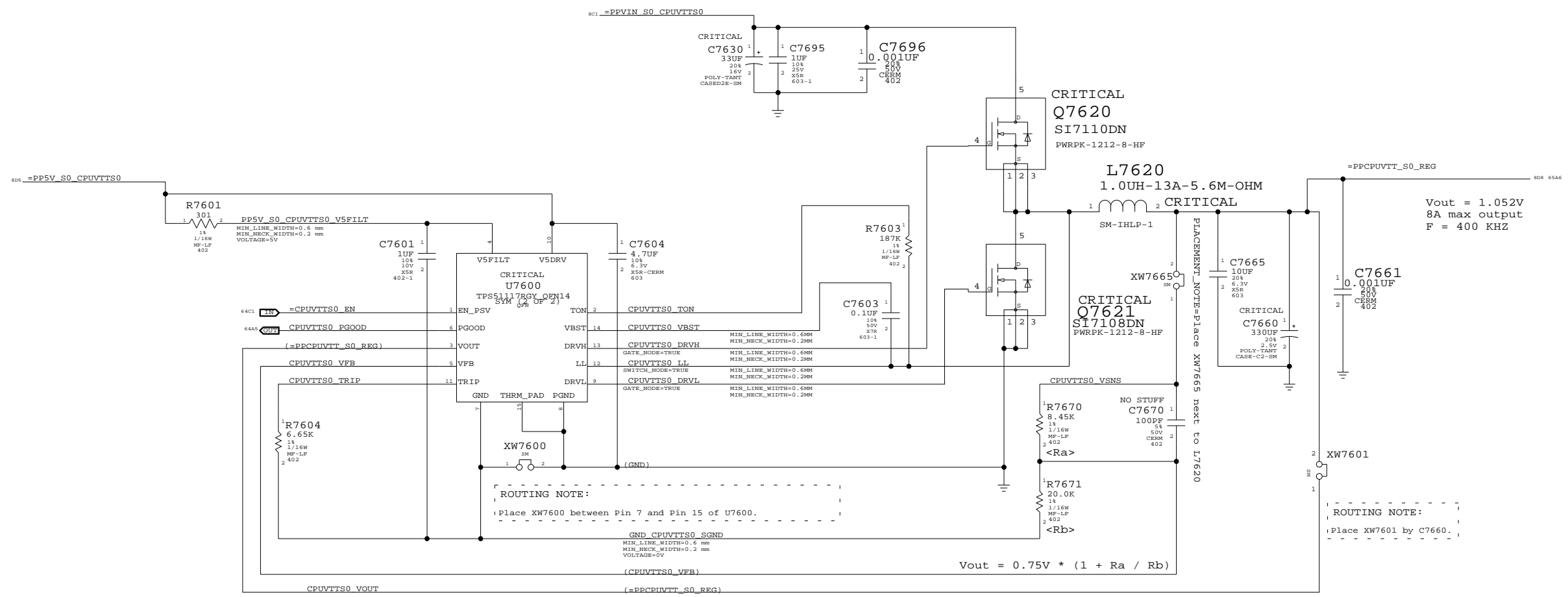
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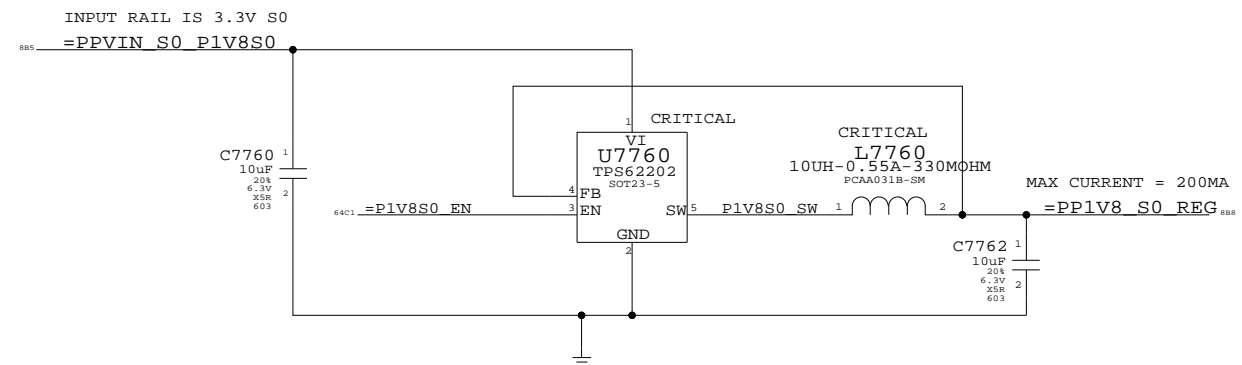
# CPUVTT POWER SUPPLY



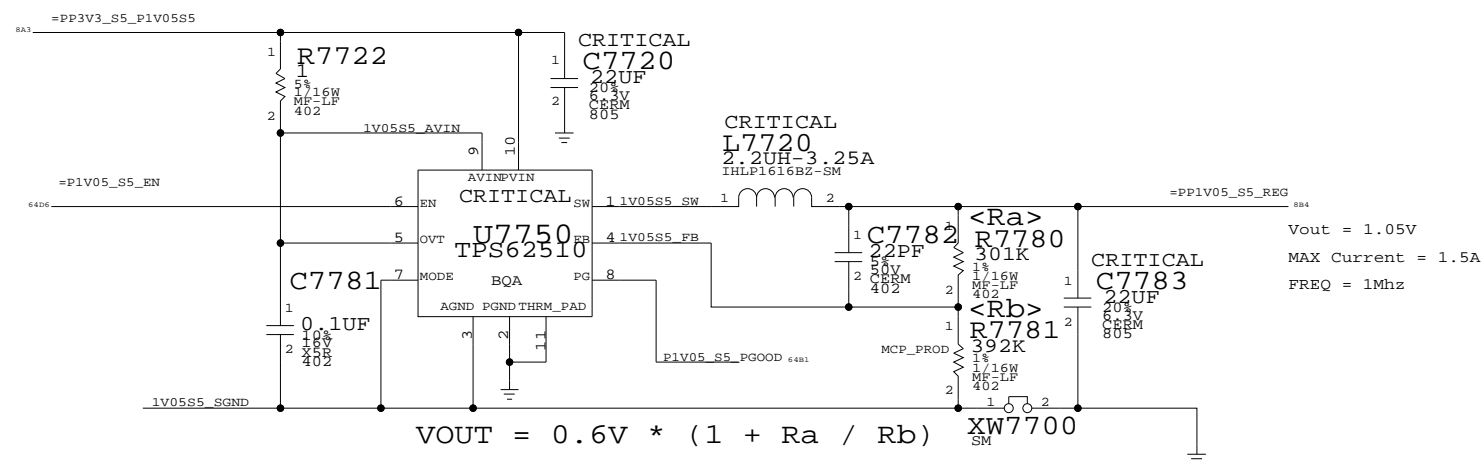
**CPU VTT(1.05V) SUPPLY**  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=02/08/2008  
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	D	051-7918	c
SCALE	SHT	OF	109
NONE	76		

# 1.8V S0 SWITCHER



## MCP 1.05V\_S5 AUXC SUPPLY



MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781		MCP_A01&MCP_A01P&MCP_A01Q

VOUT = 1.102V

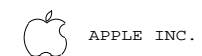
### MISC POWER SUPPLIES

SYNC\_MASTER=RAYMOND SYNC\_DATE=01/23/2008

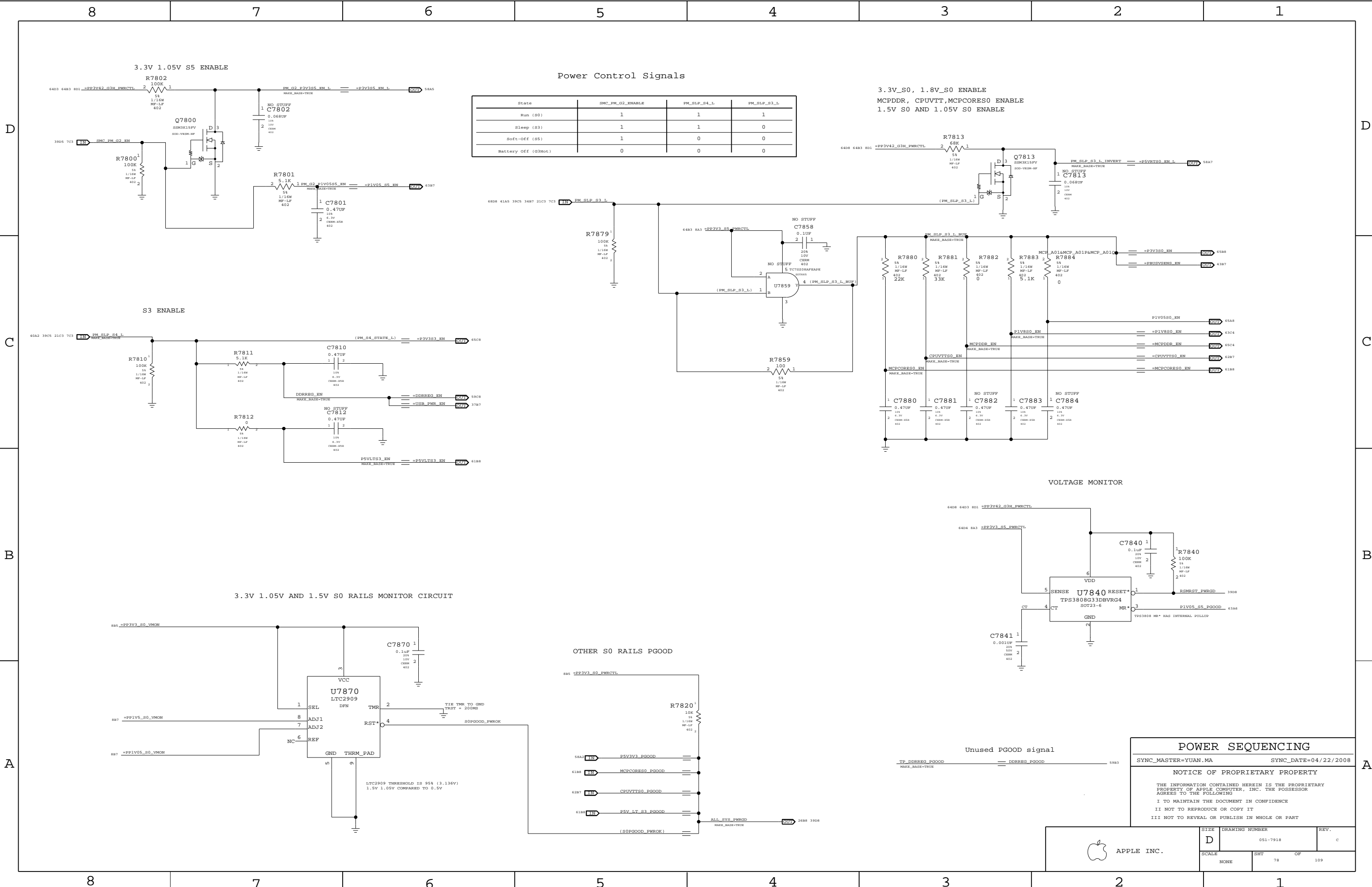
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SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	77	109



Power Control Signals

State	S5C_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.3V\_S0, 1.8V\_S0 ENABLE  
MCPDDR, CPUVTT, MCPCORES0 ENABLE  
1.5V S0 AND 1.05V S0 ENABLE

3.3V 1.05V S5 ENABLE

S3 ENABLE

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

OTHER S0 RAILS PGOOD

VOLTAGE MONITOR

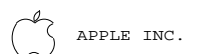
Unused PGOOD signal

POWER SEQUENCING

SYNC\_MASTER=YUAN.MA SYNC\_DATE=04/22/2008

NOTICE OF PROPRIETARY PROPERTY

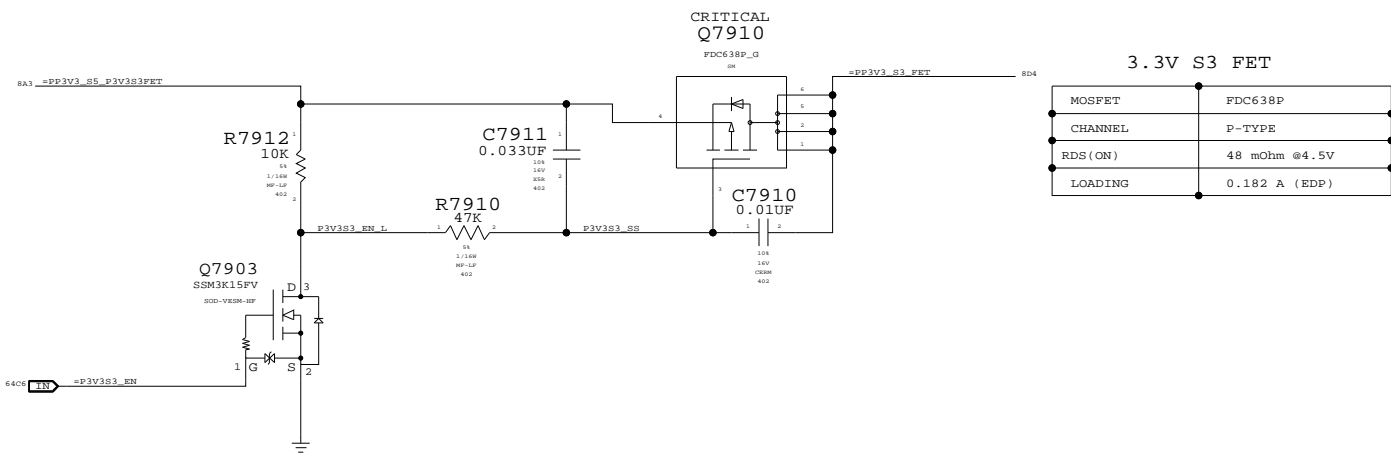
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SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	78	109

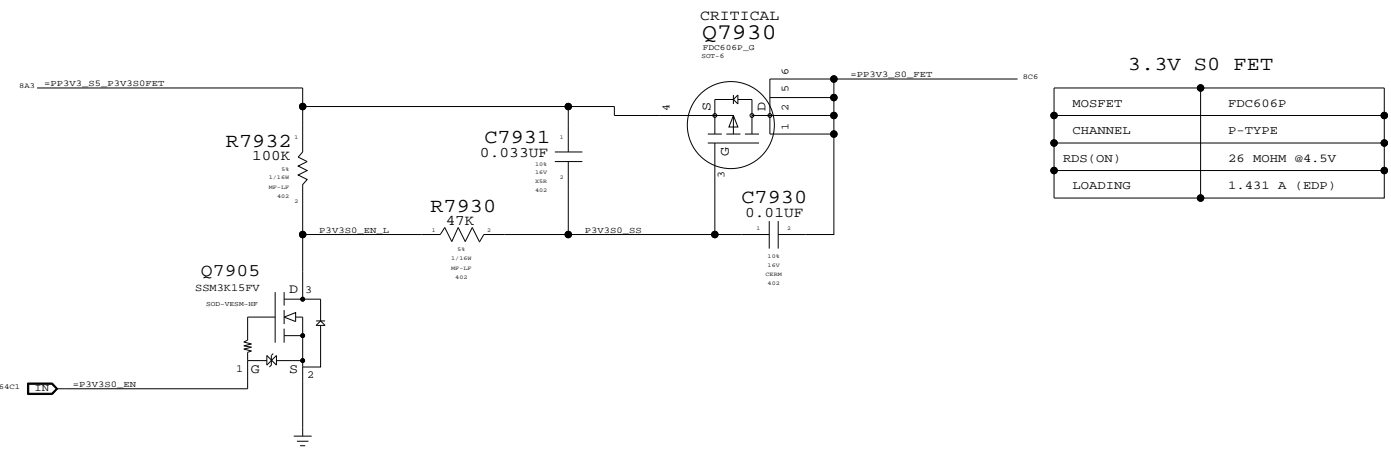


3.3V S3 FET



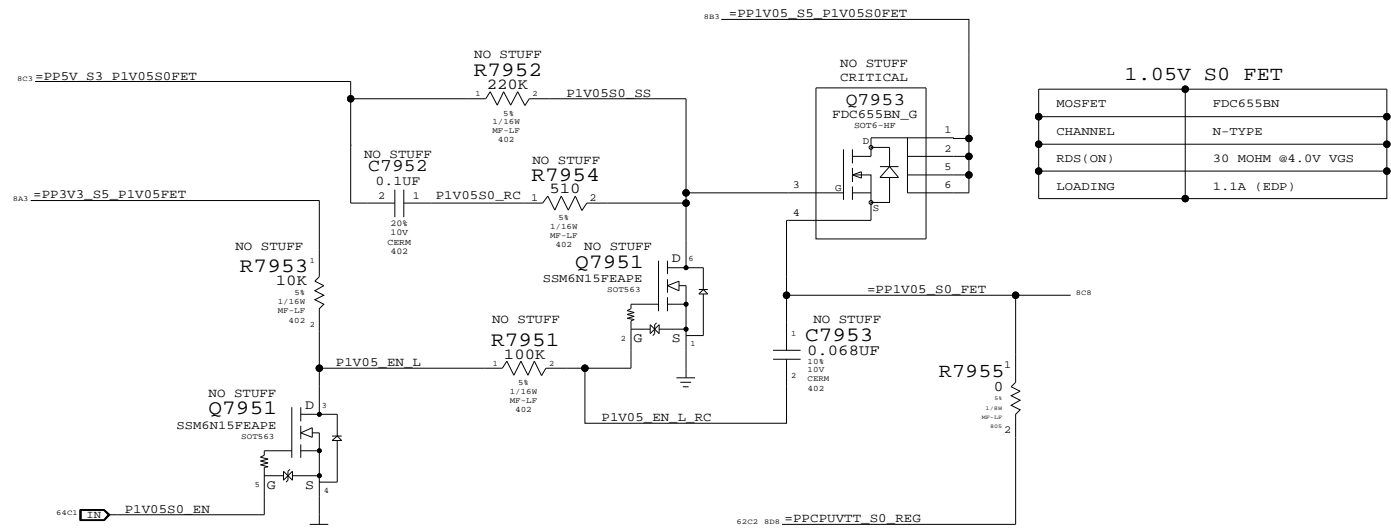
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

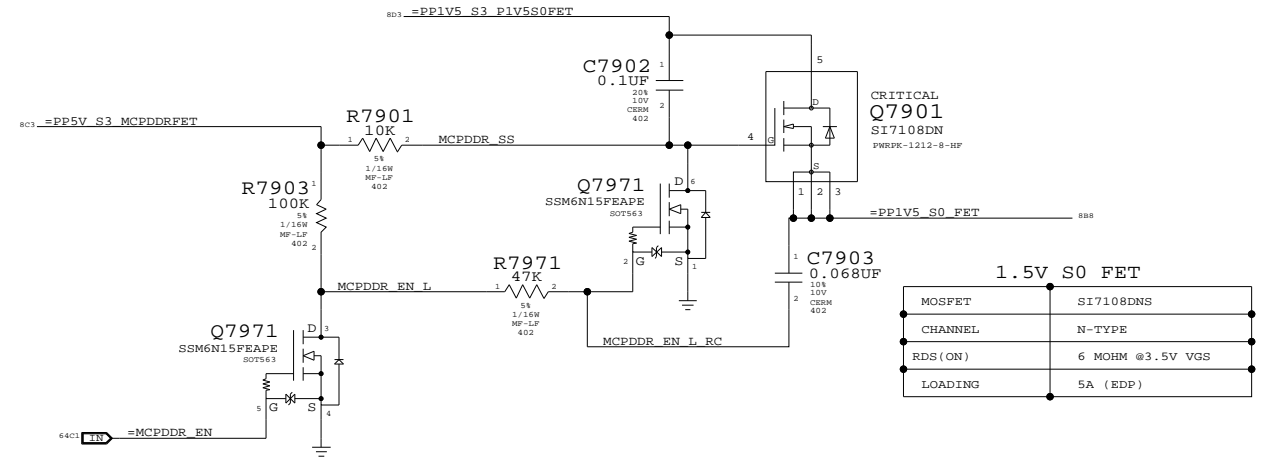
1.05V S0 FET



1.05V S0 FET	
MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

1.5V S0 FET

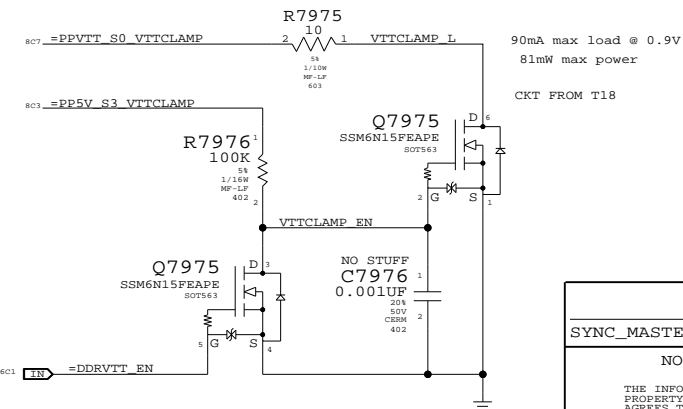
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



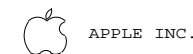
90mA max load @ 0.9V  
81mW max power  
CKT FROM T18

POWER FETS

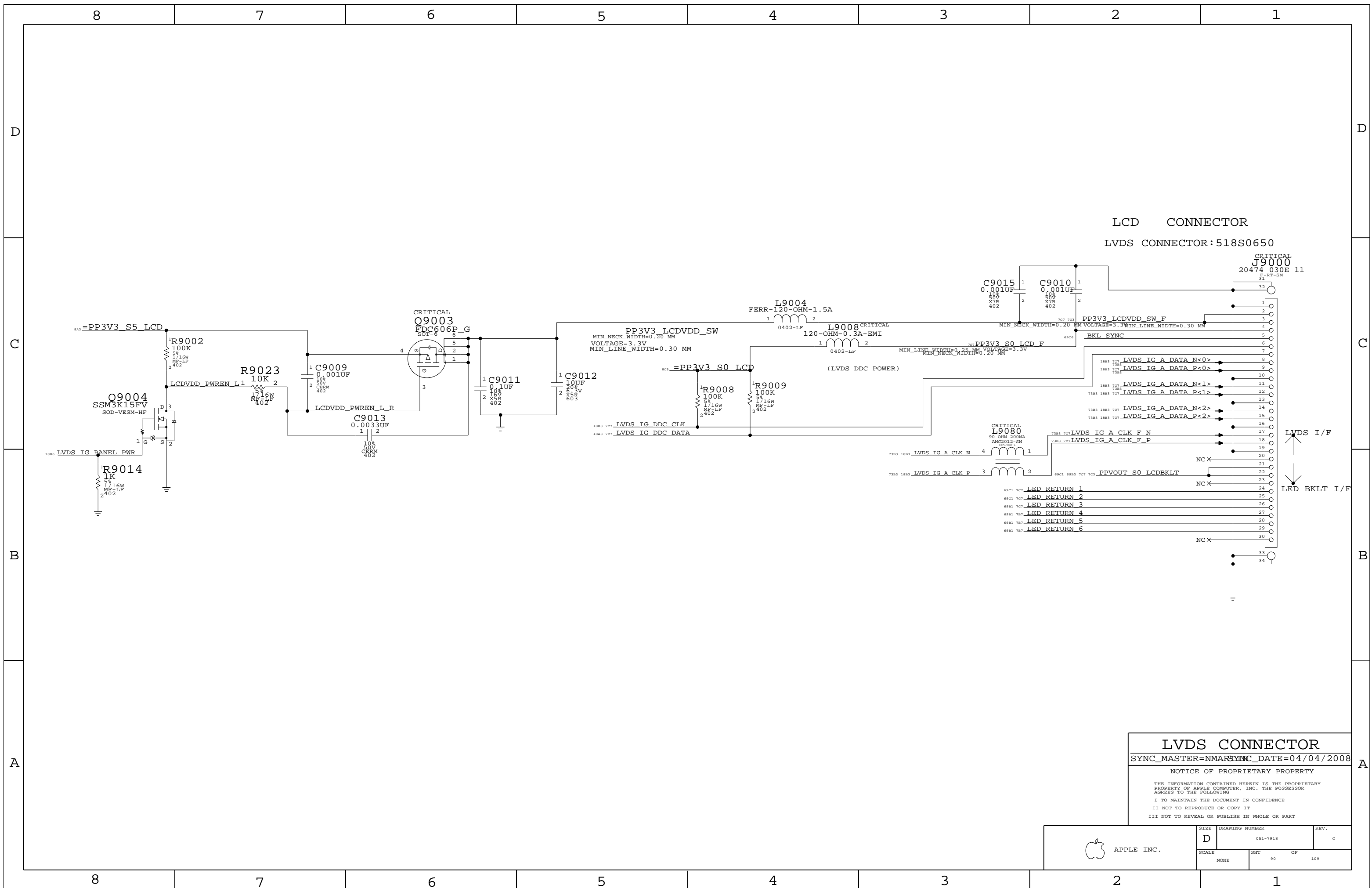
SYNC\_MASTER=YUAN.MA SYNC\_DATE=04/04/2008

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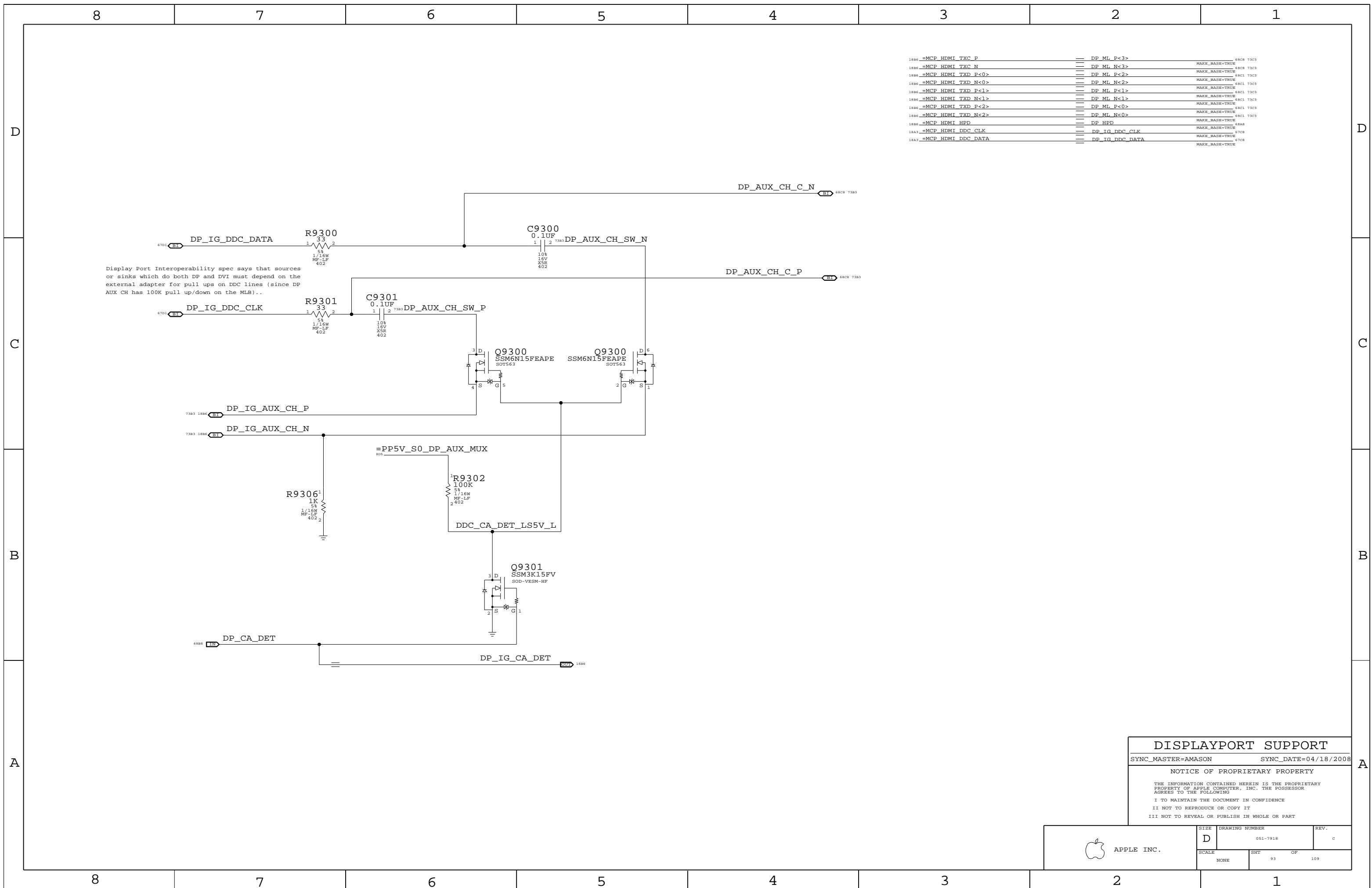
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	79	109



LCD CONNECTOR  
LVDS CONNECTOR: 518S0650

**LVDS CONNECTOR**  
 SYNC\_MASTER=NMARSYMC DATE=04/04/2008  
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	D	051-7918	c
SCALE	SHT	OF	109
NONE	90		

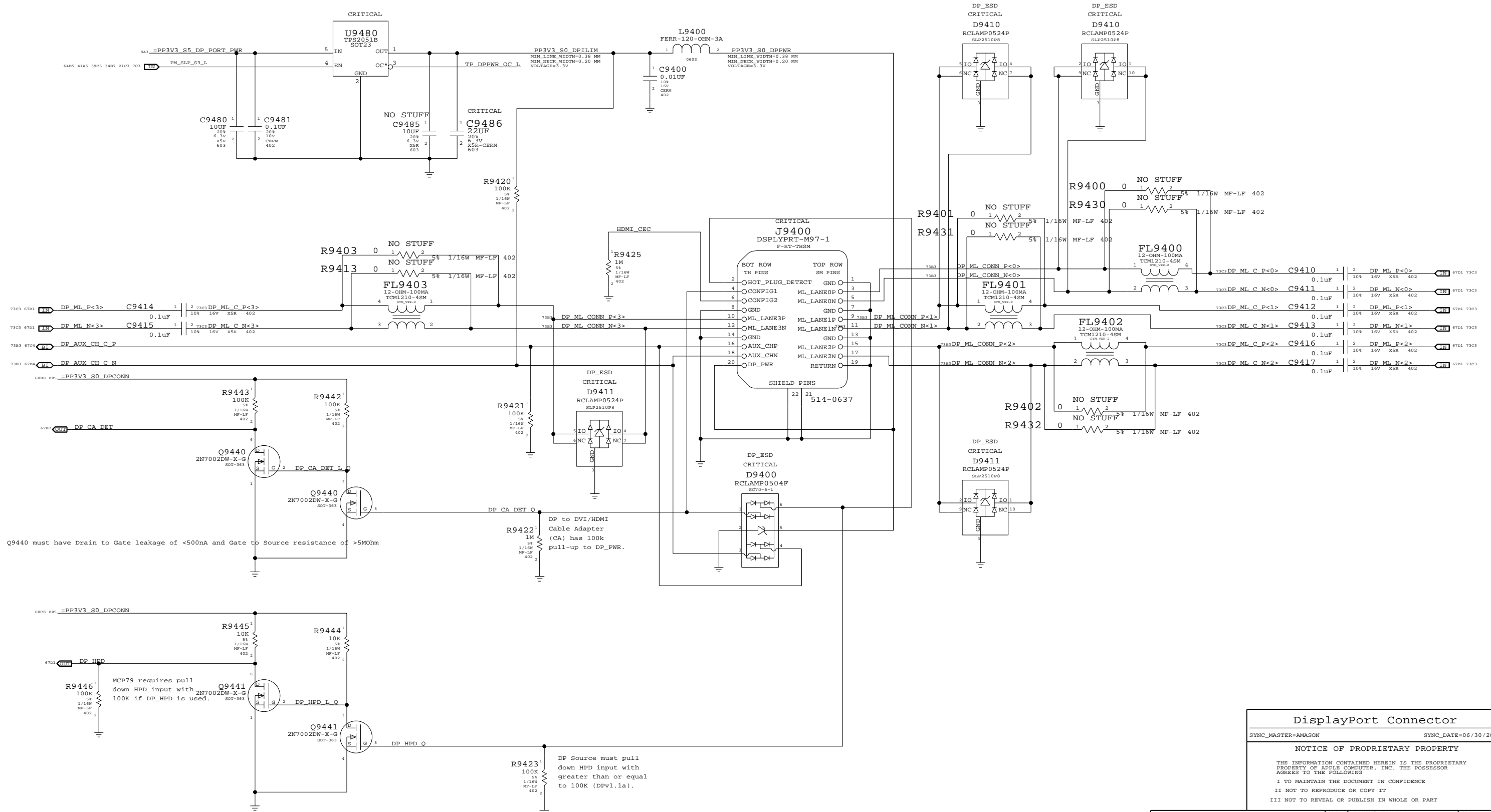


1886	=MCP_HDMI_TXC_P	DP_ML_P<3>	68C8_73C3
1886	=MCP_HDMI_TXC_N	DP_ML_N<3>	MAKE_BASE=TRUE 68C8_73C3
1886	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_P<2>	DP_ML_P<0>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<2>	DP_ML_N<0>	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_HPD	DP_HPD	MAKE_BASE=TRUE 68A8
18A1	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	MAKE_BASE=TRUE 67C8
18A1	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE 67C8

**DISPLAYPORT SUPPORT**  
 SYNC\_MASTER=AMASON SYNC\_DATE=04/18/2008  
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	109
NONE	93		

# Port Power Switch



**DisplayPort Connector**

SYNC\_MASTER=AMASON      SYNC\_DATE=06/30/2008

**NOTICE OF PROPRIETARY PROPERTY**

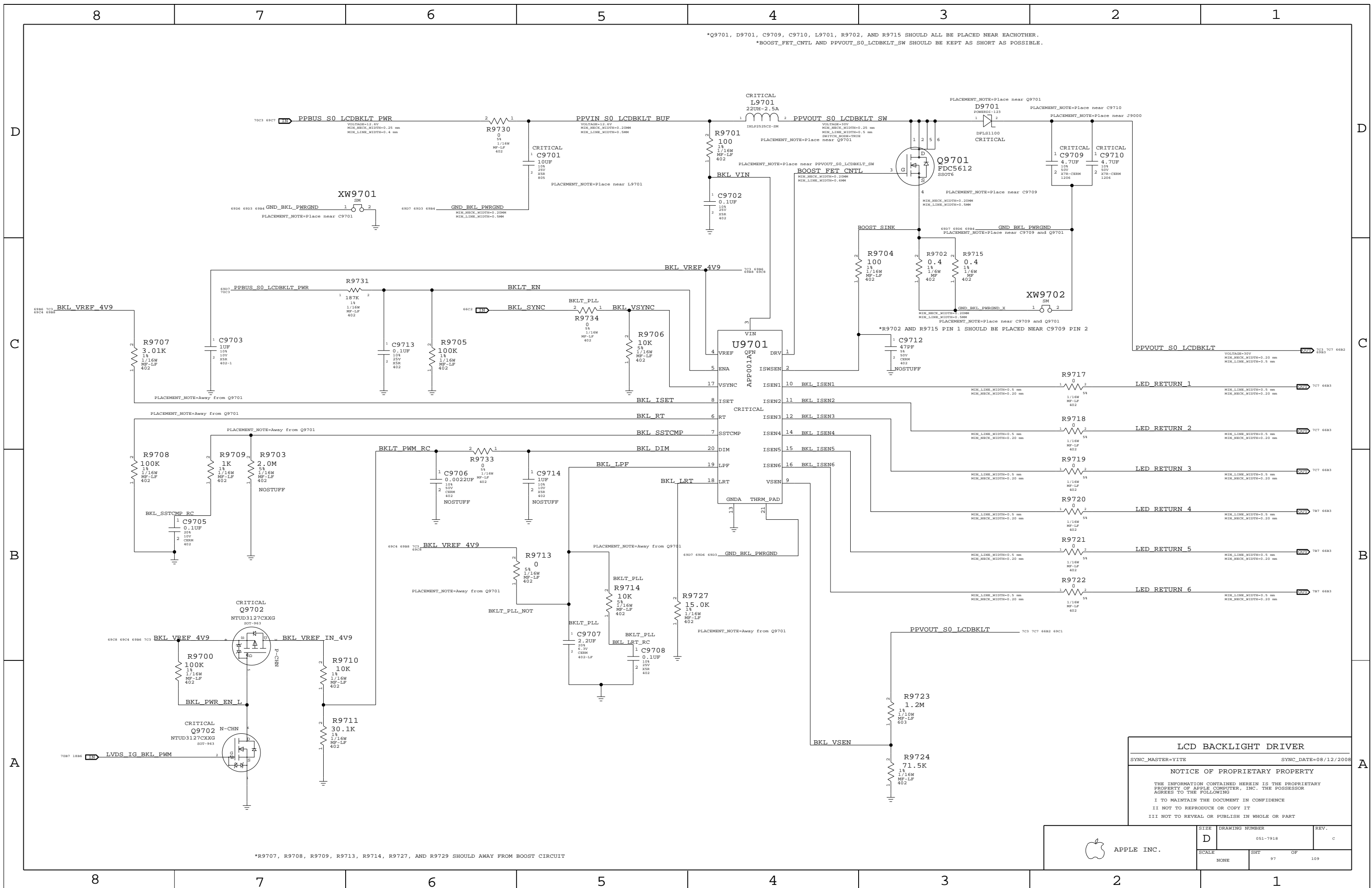
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	DRAWING NUMBER		REV.
	D	051-7918	C
SCALE		SHT	OF
NONE		94	109

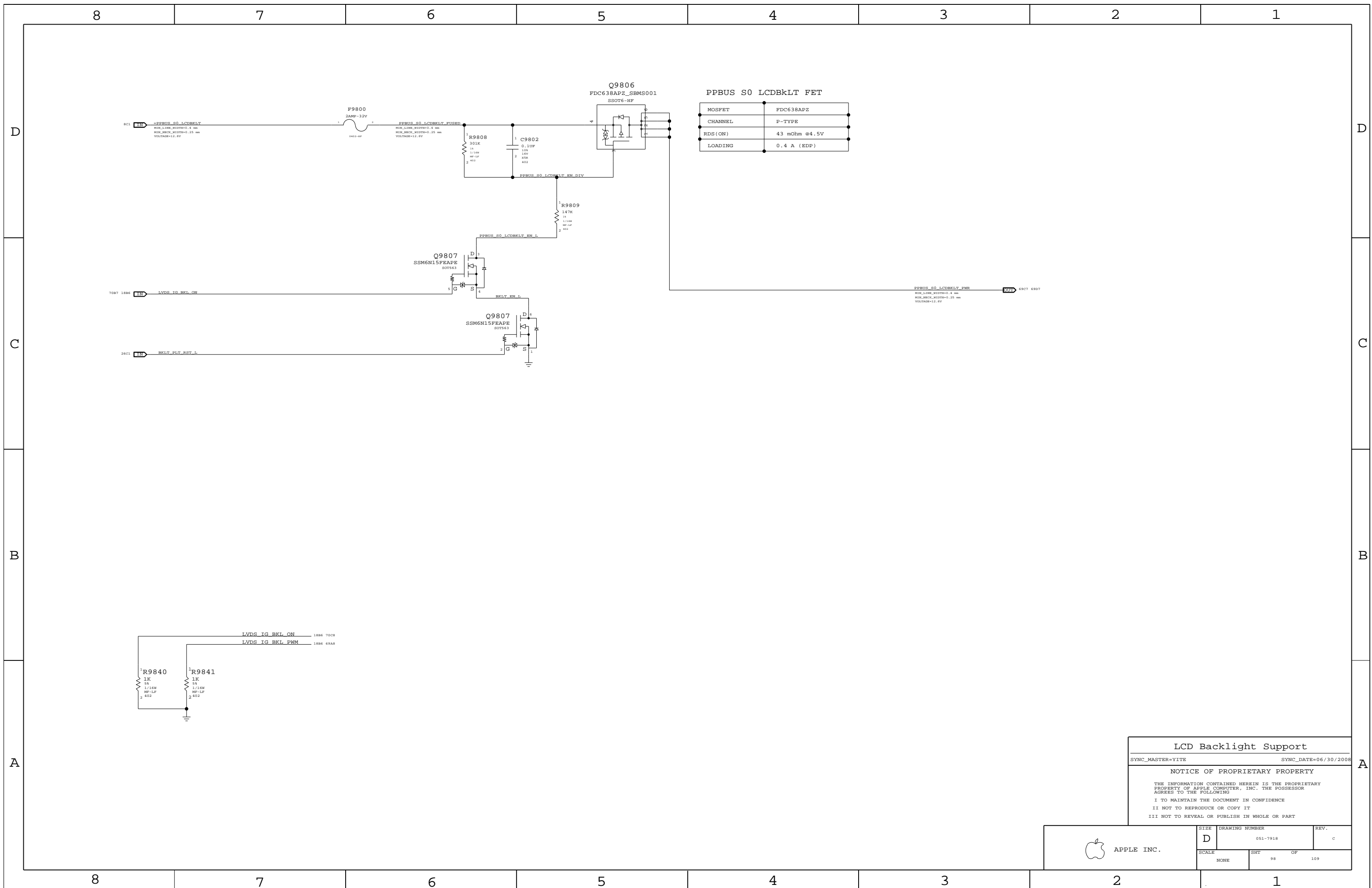


\*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.  
 \*BOOST\_FET\_CNTL AND PPVOUT\_S0\_LCDBKLT\_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

**LCD BACKLIGHT DRIVER**  
 SYNC\_MASTER=VITE SYNC\_DATE=08/12/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	109
NONE	97		

\*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT



**LCD Backlight Support**

SYNC\_MASTER=VITE SYNC\_DATE=06/30/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	SHT	OF	REV.
NONE	98	109	

FSB (Front-Side Bus) Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include FSB\_50S and FSB\_DSTB\_50S.

Table with 8 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT, SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include FSB\_DATA, FSB\_DSTB, FSB\_ADDR, FSB\_ADSTB, and FSB\_1X.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right. Signals within each 4x group should be matched within 5 ps of strobe. DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

FSB 2X signals / groups shown in signal table on right. Signals within each 2x group should be matched within 20 ps. ADSTB#s should be matched +/- 300 ps. Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right. Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include CPU\_50S and CPU\_27P4S.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Table with 8 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT, SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include CPU\_AGTL, CPU\_8MIL, CPU\_COMP, CPU\_GTLREF, CPU\_ITP, and CPU\_VCCSENSE.

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes MCP\_50S.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes MCP\_FSB\_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes CLK\_FSB\_100D.

Table with 8 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT, SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes CLK\_FSB.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

Large table listing electrical constraint sets, physical properties, and spacing for various signal groups like FSB 4X, FSB 2X, and FSB 1X. Includes columns for ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, SPACING, and NET\_NAME.

CPU/FSB Constraints

SYNC\_MASTER=T18\_MLB SYNC\_DATE=01/04/2008

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APPLE INC.

Table with 3 columns: DRAWING NUMBER, SCALE, SHEET OF. Values: 051-7918, NONE, 100 OF 109.

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.  
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.  
 All DQS pairs should be matched within 100 ps of clocks.  
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.  
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.  
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).  
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.  
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps  
 No DQS to clock matching requirement.  
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.  
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.  
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).  
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3  
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

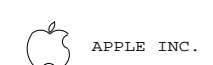
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MEM_A_CLK	MEM_70D_VDD	MEM_CLK		MEM A CLK P<5..0> 1585 2805 2807
MEM_A_CLK	MEM_70D_VDD	MEM_CLK		MEM A CLK N<5..0> 1585 2805 2807
MEM_A_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM A CKE<3..0> 1585 2805 2807
MEM_A_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM A CS L<3..0> 1585 2805 2807
MEM_A_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM A ODT<3..0> 1585 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM A A<14..0> 1585 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM A BA<2..0> 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM A RAS L 1505 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM A CAS L 1505 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM A WE L 1505 2807
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA		MEM A DQ<7..0> 1587 2802 2804 2802 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA		MEM A DQ<15..8> 1587 2802 2804
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA		MEM A DQ<23..16> 1587 1507 2882 2884 2802 2804
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA		MEM A DQ<31..24> 1507 2802 2804
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA		MEM A DQ<39..32> 1507 2885 2887 2805 2807
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA		MEM A DQ<47..40> 1507 1507 2885 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA		MEM A DQ<55..48> 1507 2885 2887
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA		MEM A DQ<63..56> 1507 2885 2887 2885 2887
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA		MEM A DM<0> 1587 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA		MEM A DM<1> 1587 2802
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA		MEM A DM<2> 1587 2884
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA		MEM A DM<3> 1587 2802
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA		MEM A DM<4> 1587 2885
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA		MEM A DM<5> 1587 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA		MEM A DM<6> 1587 2885
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA		MEM A DM<7> 1587 2887
MEM_A_DQS0	MEM_70D	MEM_DQS		MEM A DQS P<0> 1505 2802
MEM_A_DQS0	MEM_70D	MEM_DQS		MEM A DQS N<0> 1505 2802
MEM_A_DQS1	MEM_70D	MEM_DQS		MEM A DQS P<1> 1505 2804
MEM_A_DQS1	MEM_70D	MEM_DQS		MEM A DQS N<1> 1505 2804
MEM_A_DQS2	MEM_70D	MEM_DQS		MEM A DQS P<2> 1505 2882
MEM_A_DQS2	MEM_70D	MEM_DQS		MEM A DQS N<2> 1505 2802
MEM_A_DQS3	MEM_70D	MEM_DQS		MEM A DQS P<3> 1505 2804
MEM_A_DQS3	MEM_70D	MEM_DQS		MEM A DQS N<3> 1505 2804
MEM_A_DQS4	MEM_70D	MEM_DQS		MEM A DQS P<4> 1505 2887
MEM_A_DQS4	MEM_70D	MEM_DQS		MEM A DQS N<4> 1505 2887
MEM_A_DQS5	MEM_70D	MEM_DQS		MEM A DQS P<5> 1505 2885
MEM_A_DQS5	MEM_70D	MEM_DQS		MEM A DQS N<5> 1505 2885
MEM_A_DQS6	MEM_70D	MEM_DQS		MEM A DQS P<6> 1505 2887
MEM_A_DQS6	MEM_70D	MEM_DQS		MEM A DQS N<6> 1505 2887
MEM_A_DQS7	MEM_70D	MEM_DQS		MEM A DQS P<7> 1505 2885
MEM_A_DQS7	MEM_70D	MEM_DQS		MEM A DQS N<7> 1505 2885
MEM_B_CLK	MEM_70D_VDD	MEM_CLK		MEM B CLK P<5..0> 1581 2905 2907
MEM_B_CLK	MEM_70D_VDD	MEM_CLK		MEM B CLK N<5..0> 1581 2905 2907
MEM_B_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM B CKE<3..0> 1581 2905 2907
MEM_B_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM B CS L<3..0> 1581 2905 2907
MEM_B_CNTR1	MEM_40S_VDD	MEM_CTRL		MEM B ODT<3..0> 1581 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM B A<14..0> 1581 1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM B BA<2..0> 1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM B RAS L 1501 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM B CAS L 1501 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM B WE L 1501 2907
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA		MEM B DQ<7..0> 1583 2902 2904 2902 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA		MEM B DQ<15..8> 1583 2902 2904
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA		MEM B DQ<23..16> 1583 1503 2902 2904
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA		MEM B DQ<31..24> 1503 2982 2984 2902 2904
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA		MEM B DQ<39..32> 1503 2985 2987 2905 2907
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA		MEM B DQ<47..40> 1503 1503 2985 2987
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA		MEM B DQ<55..48> 1503 2985 2987
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA		MEM B DQ<63..56> 1503 2985 2987 2985 2987
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA		MEM B DM<0> 1583 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA		MEM B DM<1> 1583 2902
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA		MEM B DM<2> 1583 2902
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA		MEM B DM<3> 1583 2984
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA		MEM B DM<4> 1583 2985
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA		MEM B DM<5> 1583 2987
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA		MEM B DM<6> 1583 2985
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA		MEM B DM<7> 1583 2987
MEM_B_DQS0	MEM_70D	MEM_DQS		MEM B DQS P<0> 1501 2902
MEM_B_DQS0	MEM_70D	MEM_DQS		MEM B DQS N<0> 1501 2902
MEM_B_DQS1	MEM_70D	MEM_DQS		MEM B DQS P<1> 1501 2904
MEM_B_DQS1	MEM_70D	MEM_DQS		MEM B DQS N<1> 1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS		MEM B DQS P<2> 1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS		MEM B DQS N<2> 1501 2904
MEM_B_DQS3	MEM_70D	MEM_DQS		MEM B DQS P<3> 1501 2982
MEM_B_DQS3	MEM_70D	MEM_DQS		MEM B DQS N<3> 1501 2902
MEM_B_DQS4	MEM_70D	MEM_DQS		MEM B DQS P<4> 1501 2987
MEM_B_DQS4	MEM_70D	MEM_DQS		MEM B DQS N<4> 1501 2987
MEM_B_DQS5	MEM_70D	MEM_DQS		MEM B DQS P<5> 1501 2985
MEM_B_DQS5	MEM_70D	MEM_DQS		MEM B DQS N<5> 1501 2985
MEM_B_DQS6	MEM_70D	MEM_DQS		MEM B DQS P<6> 1501 2987
MEM_B_DQS6	MEM_70D	MEM_DQS		MEM B DQS N<6> 1501 2987
MEM_B_DQS7	MEM_70D	MEM_DQS		MEM B DQS P<7> 1501 2985
MEM_B_DQS7	MEM_70D	MEM_DQS		MEM B DQS N<7> 1501 2985
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP		MCP MEM COMP VDD 1606
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP		MCP MEM COMP GND 1606

Memory Constraints

SYNC\_MASTER=T18\_MLB SYNC\_DATE=01/04/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	101	109



PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?
CLK_PCI_E	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
PCI_E_90D	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_P	706 3107	
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_N	706 3107	
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_C_P	1783 3105	
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_C_N	1783 3105	
	PCI_E_90D	PCI_E	PCI_E_MINI_D2R_P	706 1786 3107	
	PCI_E_90D	PCI_E	PCI_E_MINI_D2R_N	706 1786 3107	
	PCI_E_90D	PCI_E	PCI_E_FC_R2D_P	3205	
	PCI_E_90D	PCI_E	PCI_E_FC_R2D_N	3205	
	PCI_E_90D	PCI_E	PCI_E_FC_R2D_C_P	986 3206	
	PCI_E_90D	PCI_E	PCI_E_FC_R2D_C_N	986 3206	
	PCI_E_90D	PCI_E	PCI_E_FC_D2R_P	986 3205	
	PCI_E_90D	PCI_E	PCI_E_FC_D2R_N	986 3205	
CLK_PCI_E_100D	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_P	1703 3105	
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_N	1703 3105	
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_CONN_P	706 3107	
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_CONN_N	706 3107	
MCP_PEX_CLK_COMP	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_FC_P	905 3205	
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_FC_N	905 3205	
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6		
DP_100D	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P		
	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N		
	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>		
	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>		
	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	6701 6801 6808	
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	6802 6807	
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	6701 6801 6808	
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	6802 6807	
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	1886 6707	
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	1886 6707	
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	6706	
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	6705	
MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	DP_AUX_CH_C_P	6704 6808	
	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	DP_AUX_CH_C_N	6704 6808	
	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	DP_AUX_CH_C_P	6704 6808	
	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	DP_AUX_CH_C_N	6704 6808	
	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	MCP_HDMI_RSET	18A6 2507	
	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	MCP_HDMI_VPROBE	18A6 2507	
	LVDS_100D	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	1883 6683
		LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	707 6602
		LVDS_100D	LVDS	LVDS_IG_A_CLK_N	1883 6683
		LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	707 6602
		LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	707 1883 6602
		LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	707 1883 6602
DP_ML		DP_ML	DISPLAYPORT	DP_ML_CONN_P<3..0>	6803 6804 6805
		DP_ML	DISPLAYPORT	DP_ML_CONN_N<3..0>	6803 6804 6805
MCP_IPFAB_VPROBE	MCP_IPFAB_VPROBE	MCP_IPFAB_VPROBE	MCP_IPFAB_RSET	18A3 2506	
	MCP_IPFAB_VPROBE	MCP_IPFAB_VPROBE	MCP_IPFAB_VPROBE	18A3 2506	
SATA_100D_HDD	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	2006 36A3	
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	2006 36A3	
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	705 36A7	
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	705 36A7	
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	36A5	
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	36A5	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	2006 36A3	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	2006 36A3	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	705 36A7	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	705 36A7	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P	36A5	
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N	36A5	
	SATA_100D_HDD	SATA	SATA_ODD_R2D_C_P	2006 36C2	
	SATA_100D_HDD	SATA	SATA_ODD_R2D_C_N	2006 36C2	
	SATA_100D_HDD	SATA	SATA_ODD_R2D_P	787 3605	
	SATA_100D_HDD	SATA	SATA_ODD_R2D_N	787 3605 3605	
SATA_100D	SATA_100D	SATA	SATA_ODD_R2D_UF_P	3604	
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	3604	
	SATA_100D	SATA	SATA_ODD_D2R_P	2006 36B2	
	SATA_100D	SATA	SATA_ODD_D2R_N	2006 36B2	
	SATA_100D	SATA	SATA_ODD_D2R_C_P	787 36B5	
	SATA_100D	SATA	SATA_ODD_D2R_C_N	787 36B5	
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	36B4	
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	36B4	
MCP_SATA_TERM	SATA_TERM	MCP_SATA_TERM	20A6		

**MCP Constraints 1**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=01/04/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE	SHT	OF	
NONE	102	109	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAIS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

HDA Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MCP_DEBUG	SPT_55S	SPT		MCP_DEBUG<7..0> 1303 1907
PCI_AD	PCI_55S	PCI		PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI		PCI_AD<24>
PCI_AD	PCI_55S	PCI		PCI_AD<31..25>
PCI_AD	PCI_55S	PCI		PCI_PAR
PCI_C_BE_L	PCI_55S	PCI		PCI_C_BE_L<3..0>
PCI_CNTRL	PCI_55S	PCI		PCI_IRDY_L
PCI_CNTRL	PCI_55S	PCI		PCI_DEVSEL_L
PCI_CNTRL	PCI_55S	PCI		PCI_PERR_L
PCI_CNTRL	PCI_55S	PCI		PCI_SERR_L
PCI_CNTRL	PCI_55S	PCI		PCI_STOP_L
PCI_CNTRL	PCI_55S	PCI		PCI_TRDY_L
PCI_CNTRL	PCI_55S	PCI		PCI_FRAME_L
PCI_BE00_I	PCI_55S	PCI		PCI_BE00_I
PCI_BE00_I	PCI_55S	PCI		PCI_BE00_I
PCI_BE01_I	PCI_55S	PCI		PCI_BE01_I
PCI_CNTRL_I	PCI_55S	PCI		PCI_CNTRL_I
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_I
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_I
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_I
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_I
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI		PCI_CLK33M MCP_R 1905
	CLK_PCI_55S	CLK_PCI		PCI_CLK33M MCP 1905
LPC_AD	LPC_55S	LPC		LPC_AD<3..0> 1983 3908 41D3 41D5
LPC_FRAME_I	LPC_55S	LPC		LPC_FRAME_I 1903 3908 41D5
LPC_RESET_I	LPC_55S	LPC		LPC_RESET_I 1903 2604
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC		LPC_CLK33M SMC_R 1983 2604
	CLK_LPC_55S	CLK_LPC		LPC_CLK33M SMC 2601 3908
	CLK_LPC_55S	CLK_LPC		LPC_CLK33M LPCPLUS 2681 41D3
USB_EXTN	USB_90D	USB		USB_EXTN_P 2003 3748
	USB_90D	USB		USB_EXTN_N 2003 3748
	USB_90D	USB		USB_EXTN_MUXED_P 3704
	USB_90D	USB		USB_EXTN_MUXED_N 3704
	USB_90D	USB		CONN_USB_EXTN_P 3703
	USB_90D	USB		CONN_USB_EXTN_N 3703
USB_CAMERA	USB_90D	USB		USB_CAMERA_P 2003 3185
	USB_90D	USB		USB_CAMERA_N 2003 3185
	USB_90D	USB		USB_CAMERA_CONN_P 705 3187
	USB_90D	USB		USB_CAMERA_CONN_N 705 3187
USB_BT	USB_90D	USB		USB_BT_P 2003 3188
	USB_90D	USB		USB_BT_N 2003 3188
	USB_90D	USB		CONN_USB2_BT_P 705 3187
	USB_90D	USB		CONN_USB2_BT_N 705 3187
USB_TPAD	USB_90D	USB		USB_TPAD_P 2003 4788
	USB_90D	USB		USB_TPAD_N 2003 4788
	USB_90D	USB		USB_TPAD_R_P 4787
	USB_90D	USB		USB_TPAD_R_N 4787
USB_IR	USB_90D	USB		USB_IR_P 2003 3807
	USB_90D	USB		USB_IR_N 2003 3807
USB_EXTB	USB_90D	USB		USB_EXTB_P 2003 3784
	USB_90D	USB		USB_EXTB_N 2003 3784
	USB_90D	USB		CONN_USB_EXTB_P 3783
	USB_90D	USB		CONN_USB_EXTB_N 3783
MCP_USB_RBIAIS	MCP_USB_RBIAIS			MCP_USB_RBIAIS_GND 2004
SMBUS_MCP_0_CLK	SMB_55S	SMB		SMBUS_MCP_0_CLK 1386 2103 4208
SMBUS_MCP_0_DATA	SMB_55S	SMB		SMBUS_MCP_0_DATA 1386 2103 4208
SMBUS_MCP_1_CLK	SMB_55S	SMB		SMBUS_MCP_1_CLK 2103 4208
SMBUS_MCP_1_DATA	SMB_55S	SMB		SMBUS_MCP_1_DATA 2103 4208
HDA_BIT_CLK	HDA_55S	HDA		HDA_BIT_CLK 2102 5107
	HDA_55S	HDA		HDA_BIT_CLK_R 21A7 21D4
HDA_SYNC	HDA_55S	HDA		HDA_SYNC 2102 5107
	HDA_55S	HDA		HDA_SYNC_R 21A7 21D4
HDA_RST_I	HDA_55S	HDA		HDA_RST_R_L 21A7 21D4
	HDA_55S	HDA		HDA_RST_L 2102 5107
HDA_SDIN0	HDA_55S	HDA		HDA_SDIN0 2107 5107
	HDA_55S	HDA		HDA_SDIN_CODEC 2102 5107
HDA_SDOUT	HDA_55S	HDA		HDA_SDOUT 21A7 21D4
	HDA_55S	HDA		HDA_SDOUT_R 21A7 21D4
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP			MCP_HDA_PULLDN_COMP 2107
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW		PM_CLK32K_SUSCLK_R 2183 2684
	CLK_SLOW_55S	CLK_SLOW		PM_CLK32K_SUSCLK 2681 3905
SPT_CLK	SPT_55S	SPT		SPI_CLK_R 2183 41A5 4108
	SPT_55S	SPT		SPI_CLK 4181 5005
	SPT_55S	SPT		SPI_ALT_CLK 4105 41D3
SPT_MOSI	SPT_55S	SPT		SPI_MOSI_R 2183 41A5 4107
	SPT_55S	SPT		SPI_MOSI 4181 5004
SPT_MISO	SPT_55S	SPT		SPI_MISO 2183 41A5 4187
	SPT_55S	SPT		SPI_MISO_R 5004
	SPT_55S	SPT		SPI_ALT_MISO 4185 41D5
SPT_CS0	SPT_55S	SPT		SPI_CS0_R_L 2183 4187
	SPT_55S	SPT		SPI_CS0_L
	SPT_55S	SPT		SPI_CS1_R_L
	SPT_55S	SPT		SPI_CS1_R_L_USE_MLB 4182

**MCP Constraints 2**

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	NONE	103	109

MCP RGMI (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

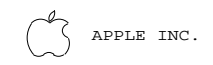
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	1806
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	1806
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	1803 3445
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	3386 3443
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	1803 3386
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	1803 3386
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	3304
ENET_RXCTL_R	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	1806 3301
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	3304
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	1806 3301
ENET_RXD_STEAR	ENET_MII_55S	ENET_MII	ENET_RXD<3..3>	1806 3301
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	1806 3381
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	3384
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	3306
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	1803 3308
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	1803 3306
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..3>	1803 3306
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	1803 3386
ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	1803 3387
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	3383 3587 3507
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	3383 3587 3507
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	3584 3504 3505
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	3584 3504 3505

Ethernet Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 55G	SMB	SMBUS_SMC_A_S3_SCL	785 7D5 42D2
SMBUS_SMC_A_S3_SDA	SMB 55G	SMB	SMBUS_SMC_A_S3_SDA	785 7D5 42D2
SMBUS_SMC_B_S0_SCL	SMB 55G	SMB	SMBUS_SMC_B_S0_SCL	42C2
SMBUS_SMC_B_S0_SDA	SMB 55G	SMB	SMBUS_SMC_B_S0_SDA	42C2
SMBUS_SMC_O_S0_SCL	SMB 55G	SMB	SMBUS_SMC_O_S0_SCL	42D5
SMBUS_SMC_O_S0_SDA	SMB 55G	SMB	SMBUS_SMC_O_S0_SDA	42D5
SMBUS_SMC_BSA_SCL	SMB 55G	SMB	SMBUS_SMC_BSA_SCL	7A7 7B7 42C5
SMBUS_SMC_BSA_SDA	SMB 55G	SMB	SMBUS_SMC_BSA_SDA	42C5
SMBUS_SMC_MGMT_SCL	SMB 55G	SMB	SMBUS_SMC_MGMT_SCL	42B5
SMBUS_SMC_MGMT_SDA	SMB 55G	SMB	SMBUS_SMC_MGMT_SDA	42B5

### SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	
			CHGR_CSI_N	
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	
			CHGR_CSO_N	

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**SMC Constraints**

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NONE	106	109	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

M97 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DIFFPAIR	CHGR_CSO_R_P		44A8	57B3
DIFFPAIR	CHGR_CSO_R_N		44A8	57B3
DIFFPAIR	CPUTHMSNS_D2_P		45C5	
DIFFPAIR	CPUTHMSNS_D2_N		45C5	
DIFFPAIR	CPU_THERMD_P		10C6	45D5
DIFFPAIR	CPU_THERMD_N		10C6	45D5
DIFFPAIR	ISNS_CPUVTT_P		44B7	
DIFFPAIR	ISNS_CPUVTT_N		44B7	
DIFFPAIR	ISNS_P1VSSOMCP_P		44C7	
DIFFPAIR	ISNS_P1VSSOMCP_N		44C7	
DIFFPAIR	ISNS_PVCORESOMCP_P		44D8	
DIFFPAIR	ISNS_PVCORESOMCP_N		44D8	61C4
DIFFPAIR	MCP_THMSNS_D2_P		7C7	45B5
DIFFPAIR	MCP_THMSNS_D2_N		7C7	45B5
DIFFPAIR	MCP_THMDIODE_P		21C3	45C5
DIFFPAIR	MCP_THMDIODE_N		21C3	45C5

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M97 SPECIAL CONSTRAINTS

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NONE	107	109

M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA_P1MM				MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM				
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM				
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27F4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM				
27F4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM	
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM	
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM	
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM	
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

M97 RULE DEFINITIONS

SYNC\_MASTER=M97\_MLB

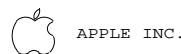
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