GINSU (K51A)

REFERENCE FROM T18

LAST MODIFIED=Thu Feb 19 13:16:29 2009

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

ALL CAPACITANCE VALUES ARE IN MICROFARADS.
### BOM Variants

<table>
<thead>
<tr>
<th>BOM NUMBER</th>
<th>BOM NAME</th>
<th>BOM OPTIONS</th>
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</thead>
<tbody>
<tr>
<td>639-0017</td>
<td>BOM, 0.017</td>
<td>639-0017</td>
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<tr>
<td>639-0016</td>
<td>BOM, 0.016</td>
<td>639-0016</td>
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<tr>
<td>639-0013</td>
<td>BOM, 0.013</td>
<td>639-0013</td>
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<tr>
<td>639-0020</td>
<td>BOM, 0.020</td>
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<tr>
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<td>BOM, 0.019</td>
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<td>BOM, 0.018</td>
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<td>BOM, 0.4701</td>
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<tr>
<td>639-0014</td>
<td>BOM, 0.014</td>
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### BOM GROUPS

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<thead>
<tr>
<th>BOARD STACK-UP</th>
<th>SIGNAL</th>
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<tbody>
<tr>
<td>TOP</td>
<td>2</td>
<td>GROUND</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>SIGNAL</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>POWER</td>
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<tr>
<td></td>
<td>5</td>
<td>POWER</td>
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<td>6</td>
<td>SIGNAL</td>
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<td></td>
<td>7</td>
<td>GROUND</td>
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### COMMON

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<tr>
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<th>REFERENCE DESIGNATOR(S)</th>
<th>ALTERNATES</th>
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<tbody>
<tr>
<td></td>
<td>CPU</td>
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</tr>
<tr>
<td></td>
<td>X50A, X51A</td>
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<td></td>
<td>PCB, SCHEM, MLB, K51A</td>
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<td>PCBA, MLB, K51A</td>
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<td>Intel Sock-P, BGA, 26X26-479</td>
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<td></td>
<td>EFI ROM, K50A/K51A/K50E</td>
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<td>MLB LABEL, 48.0X4.8</td>
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<td>PCB, FAB, IO ALIGNMENT, K50/K51</td>
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<td>IC, FW643-06, 1394B, REV-E</td>
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</table>

### K50A PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
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</thead>
<tbody>
<tr>
<td>152-0101</td>
<td></td>
</tr>
<tr>
<td>152-0102</td>
<td></td>
</tr>
<tr>
<td>152-0103</td>
<td></td>
</tr>
<tr>
<td>152-0104</td>
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### K51A PARTS

<table>
<thead>
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<th>ALTERNATE FOR</th>
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<tbody>
<tr>
<td>152-0101</td>
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<tr>
<td>152-0102</td>
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<tr>
<td>152-0103</td>
<td></td>
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<td>152-0104</td>
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### ALTERNATES

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
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---

**Scale and Size:**

- Scale: 1:1
- Size: D0
MCP79-specific pinout

1. **TP_XDP_OBSFN_B1**
   - XDP_BPM_L<1>
   - XDP_BPM_L<4>
   - XDP_BPM_L<0>
   - XDP_TMS
   - XDP_TDO
   - XDP_TCK
   - XDP_TDI
   - XDP_DEBUG<1>
   - XDP_DEBUG<0>
   - XDP_DEBUG<7>
   - XDP_DEBUG<6>
   - XDP_DEBUG<5>
   - XDP_DEBUG<4>
   - XDP_DEBUG<3>
   - SMBUS_MCP_0_CLK
   - SMBUS_MCP_0_DATA

2. **TP_XDP_OBSDATA_B1**
   - XDP_BPM_L<2>
   - XDP_BPM_L<3>
   - XDP_BPM_L<5>
   - XDP_PWRGD
   - TP_XDP_OBSDATA_B3
   - TP_XDP_OBSDATA_B2
   - TP_XDP_OBSDATA_B0

3. **JTAG_MCP_TDI**
   - XDP_CPURST_L
   - XDP_DBRESET_L
   - XDP_CPURST_L
   - XDP_BPM_L<6>
   - JTAG_MCP_TRST_L
   - JTAG_MCP_TMS
   - JTAG_MCP_TCK
   - JTAG_MCP_TDO

4. **SMBUS_MCP_0_CLK**
   - FSB_CLK_ITP_P
   - FSB_CLK_ITP_N

5. **CPU_PWRGD**
   - FS0_CPURST_L
   - XDP_TRST_L
   - XDP_BPM_L<7>

6. **MCP_DEBUG<0>-<7>**

7. **eXtended Debug Port (XDP)**

---

**Sync Date:** 01/07/2009

**Apple Inc.**

---

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Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

=PP1V8R1V5_S0_MCP_MEM

R1611
40.2
MF-LF
1/16W
R1610
402
1%
2
1
2

16C7 25C8 30B7 30C7

8B8
8B8
8C8
8B8
8B8
8B8
8A8
8A8
8A8
8A8
8A8
8A8

4771 mA (A01, DDR3)

www.vinafix.vn
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.

If PE1 interface is not used, ground DVDD0_PEX and AVDD0_PEX.

www.vinafix.vn
CPU FSB Frequency Straps

NOTE: () values not supported by MCP79.

Merom/Penryn do not officially support FSB1, but it’s not clear whether FSB1 interface is present or not. T12 used pin F6.

Extra FSB Pull-ups
Exist in MM but not Intel designs. Here for CYA.

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If found to be necessary, will move to page14.png

APPENDIX A

Scale REV.

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WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
16 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>
CAPS TO COUPLE MCP 1V5_S0_MEM AND DIMMS 1V5_S3

CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM A (FURTHER FROM MCP)

CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM B (CLOSER TO MCP)

EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

www.vinafix.vn
 DDR3 RESET Support

DDTR support cannot control this signal directly, since it must be high in sleep and MCP MEM rails are not powered in sleep.

1. VDD must be stable before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

- R3310: 5% 1/16W MF-LF 1K
- C3300: CERM 20% 0.1UF
- R3300: 5% 1/16W MF-LF 10K
- R3309: 5% 1/16W MF-LF 0
- R3305: 5% 1/16W MF-LF 20K
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

1.05V ENET FET

NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY

RTL8211 25MHz Clock

NOTE: MCX79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
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NOTE: DELTA RECOMMENDS CENTER-TAP BE FLOATING WHEN USING REALTEK PHY.

NOTE: BOB SMITH TERMINATION FOR EMC INVESTIGATION.

ALSO AVAILABLE 157S0057 - 12 CORE

ENET_MCT_BS
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.4 MM

ENET_TCT

ENET_MDI_T_N<0>
ENET_MDI_T_P<2>
ENET_MDI_T_N<2>
ENET_MDI_T_P<3>
ENET_MDI_T_N<3>

ENET_MDI_T_P<0>
ENET_MDI_T_P<1>
ENET_MDI_T_N<1>
ENET_MDI_T_P<0>
ENET_MDI_T_P<1>
ENET_MDI_T_N<2>

ENET_MDI_T_N<3>
ENET_MDI_P<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

ENET_MDI_P<3>
ENET_MCT1

ENET_MDI_T_P<2>
ENET_MDI_T_P<0>

ENET_MDI_T_N<1>

ENET_MCT3

ENET_MCT4

ENET_MCT2

ENET_MCT1

ENET_MCT2

ENET_MDI_T_P<3>

ENET_MDI_P<3>

ENET_MDI_N<0>
ENET_MDI_P<0>

ENET_MDI_T_N<0>
ENET_MDI_T_P<2>
ENET_MDI_T_N<2>

ETHERNET CONNECTOR

www.vinafix.vn
FW643 1.0V GENERATION

Termination
Place close to Firewire PHY

1394 PHY DATA/STROBE OPTIONS

2ND & 3RD TPA/TPB PAIR UNUSED

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

NOTE: Q4200 COLLECTOR CONNECT TO CAPS WITH 0.4 SQ-IN HEAT SINK

NOTE: MULTIPLE VIAS TO DGND

MIN_NECK_WIDTH=0.08MM
VOLTAGE=1.86V

MIN_NECK_WIDTH=0.1MM
MIN_LINE_WIDTH=0.6MM
MAX_NECK_LENGTH=3MM

www.vinafix.vn

Apple Inc.
12 VOLTS 7 WATTS MAX PER PORT

"Snapback" & "Late VG" Protection

ESD Rail

PORT 0 1394B

VOLTAGE=3.3V MIN_NECK_WIDTH=0.25 mm MIN_LINE_WIDTH=0.38 mm

PP3V3_FW_ESD

FERR-250-OHM

C4300

0.01UF

603-1 X7R

50V 10%

L4300

SM

402

1W MF

5% CRITICAL

PPVP_FW_PHY_CPS_FET

=PPVP_FW_PHY_CPS

=PP3V3_FW_PHY

FIREWIRE CONNECTOR

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APPLE INC.

9350 S. De Anza Blvd.

CA 95070 USA

(650) 444-9000

www.apple.com

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FIREWIRE CONNECTOR
SATA PORT A0 FOR HDD

SATA PORT A1 FOR SLIMLINE ODD

SATA Activity LED

SATA Connectors

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DRAWING NUMBER

SHT OF SIZE

518S0553

SB has internal 15K pull-downs on both sides of the pin.

Both sides of the pin.

K37L (BLUETOOTH) CONNECTOR

Ir receiver

USB_BT_N = PP3V3_S3_BT

USB_BT_P = PP5V_S3_BT

USB_IR_L_P = PP5V_S3_BNDI

USB_IR_L_N = PP5V_S3_BNDI

USB_CAMERA_P = PP5V_S3_BNDI

USB_CAMERA_L_P = PP5V_S3_BNDI

USB_CAMERA_L_N = PP5V_S3_BNDI

USB_IR_P = PP5V_S3_BNDI

USB_IR_N = PP5V_S3_BNDI

Internal USB Connections

MIN_LINE_WIDTH=0.6MM

MIN_NECK_WIDTH=0.2MM

VOLTAGE=5V

PP5V_S3_BNDI_IR

MIN_LINE_WIDTH=0.6MM

MIN_NECK_WIDTH=0.2MM

VOLTAGE=5V

USB_BT_N

USB_BT_P

USB_CAMERA_L_P

USB_CAMERA_L_N

USB_IR_L_N

USB_IR_P

USB_IR_N

20D3

103C3

103C3

103C3

103B3

7B8

20D3

103C3

47D5

7B8

20C3

103C3

7B8

20D3

103C3

6D3

7B8

20D3

103C3

47D8

103C3

6C3

47B4

103C3

6C3

47B6

www.vinafix.vn
NOTE: Unused pins have "SMC_Pxx" names.

Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC_P24:

If SMS interrupt is not used, pull up to SMC rail.

MIN_NECK_WIDTH=0.20 MM

NO STUFF

www.vinafix.vn
REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

REMOTE THERMAL SENSORS

HEATSINKS, AMBIENT, PANEL AND DISKS

DIGITAL LCD TEMP SENSOR

CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor
NOTE: MCP79 only issue 'READ' (0x03) commands

SST25VF016B max speed for READ command is 25MHz.
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PSAR = 14.73A
AVG = 8.33A

Vout = 0.75V * (1 + Ra / Rb)

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

CRITICAL
EN 1.05V S0 and 3.3V S5 rails

**INPUT POWER OF 12V_S0**

- **X5R-CERM 10UF**
- **C7621 POLY 16V 20%**
- **10.0K R7663**
- **25V 5.23K**
- **MF 402 1/16W 603**
- **MF-LF 1/10W 603 402 1%**
- **3V3REG_VCC**
- **3V3S5_OUT**
- **3V3S5_ILIM**
- **3V3_BOOT2**
- **C7689 X7R-CERM 6.3V 20% 3V3_BOOT2_R**
- **C7675 X5R 10%**
- **C7683 X5R 10%**
- **3.7V VOLTAGE=5V**

**INPUT POWER OF 12V_S5**

- **PPVIN_S0_P1V05S0**
- **POWER BUDGET**
- **16V 10%**
- **6D6**
- **6.7A MAX OUTPUT (R7614 LIMIT)**
- **10UF C7616 0.1UF CERM 16V 20%**
- **1.5UH-12A CRITICAL**
- **1V05_SNUBBER MIN_LINE_WIDTH=0.4MM**
- **0.1UF 603 16V**
- **Vout = 0.7V * (1 + Ra / Rb) =1V05S0_EN**
- **Q1 (R7663 LIMIT)**
- **10.0K 25V 5.23K 9 MF 402 1/16W 603**
- **MF-LF 1/10W 603 402 1%**
- **P1V05S0_PHASE P1V05S0_UGATE**
- **LGATE1 LGATE2 OUT1 OUT2**
- **27 AFTER LDO OUT**
- **22 BOOT2**
- **C7689 X7R-CERM 6.3V 20% 3V3_BOOT2_R**
- **C7675 X5R 10%**
- **C7683 X5R 10%**
- **200K MF-LF 5%**
- **16V 10%**
- **2**
- **CRITICAL**
- **K50/K51 805-1 76**
- **SYNC_DATE=01/07/2009**
- **PP3V3_S5_REG**
- **1**
- **EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER EN_R (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO REGS ON POWER IS ENABLED AS SOON AS LDO OUTPUT IS GOOD**
- **EN1 (1.05_S0) CONTROLLED SEPARATELY**

---

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER EN_R (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO REGS ON POWER IS ENABLED AS SOON AS LDO OUTPUT IS GOOD

EN1 (1.05_S0) CONTROLLED SEPARATELY
MCP ONLY 1.8V_S0 POWER SUPPLY

VOUT = 0.5 * (1 + RA/RB)

MAX CURRENT = 300MA
VOUT = 1.8V

SYNC_MASTER=K50
SYNC_DATE=01/07/2009

MIN_NECK_WIDTH=0.1MM
SWITCHNODE
MIN_LINE_WIDTH=0.3MM
1V8_SW
1V8S0_EN
108D3
6A4
6C6 7D3

APPLE INC.
www.vinafix.vn
PLACE THESE CAPACITORS AT LEAST 1 INCH AWAY FROM DP CONNECTOR
### MCP FSB COMP Signal Constraints

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

**MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-Ohm SINGLE-ENDED.**

**SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2

*Design Guide recommends each strobe/signal group is routed on the same layer. Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.*

*Signals within each 4x group should be matched within 5 ps of strobe. All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.*

### FSB (Front-Side Bus) Constraints

**PHYSICAL_RULE_SET**

- **SPACING_RULE_SET**
  - **CPU_GTLREF**
  - **CPU_AGTL**
  - **MCP_50S**
  - **CPU_50S**

**LAYER**

- **LINE-TO-LINE SPACING** on layer?
  - **ALLOW ROUTE**
    - 27P4_OHM_SE
    - 100_OHM_DIFF
  - **MINIMUM LINE WIDTH**
    - 0.6 MM
    - 0.2 MM
  - **MINIMUM LINE WIDTH**
    - 50_OHM_SE
  - **WEIGHT**
  - **TABLE_SPACING_RULE_ITEM**
  - **TABLE_SPACING_RULE_HEAD**
  - **TABLE_PHYSICAL_RULE_HEAD**
  - **TABLE_PHYSICAL_RULE_ITEM**

**FSB_ADSTB**

- **TABLE_SPACING_RULE_ITEM**
  - **TABLE_SPACING_RULE_HEAD**
  - **TABLE_PHYSICAL_RULE_ITEM**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_RULE_HEAD**

**TABLE_PHYSICAL_RULE_HEAD**

**TABLE_PHYSICAL_RULE_ITEM**

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Source</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### MCP MEM COMP Signal Constraints

- **DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.**
- **All memory signals maximum length is 1.005 ps.** CLK minimum length is 594 ps (lengths include substrate).
- **A/BA/cmd signals should be matched within 5 ps of CLK pairs.** No DQS to clock matching requirement.

### DDR3:
- **All memory signals maximum length is 1.005 ps.** CLK minimum length is 594 ps (lengths include substrate).
- **A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.**
- **CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.**
- **DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.**

### DDR2:
- **All memory signals maximum length is 1.005 ps.** CLK minimum length is 594 ps (lengths include substrate).
- **A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.**
- **CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.**
- **DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.**

### Memory Net Properties

### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Space</th>
<th>Max Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CTRL</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
</tr>
<tr>
<td>MEM_CLK</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
</tr>
<tr>
<td>MEM_DQS</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
<td>70_OHM_DIFF</td>
<td>40_OHM_SE</td>
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</tbody>
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<table>
<thead>
<tr>
<th>Signal</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Space</th>
<th>Max Space</th>
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</thead>
<tbody>
<tr>
<td>MEM_CTRL2CTRL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA2MEM</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>MEM_70D</td>
<td></td>
<td></td>
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<tr>
<td>MEM_40S</td>
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### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Group Name</th>
<th>Min Space</th>
<th>Max Space</th>
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</thead>
<tbody>
<tr>
<td>MEM_CTRL2CTRL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA2MEM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_70D</td>
<td></td>
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</tr>
<tr>
<td>MEM_40S</td>
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<td></td>
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</tbody>
</table>

### MCP MEM COMP Signal Constraints

- **Use 140_OHM_DIFF for connections to other components.**
### HD Audio Interface Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line-to-line spacing</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum line width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum neck width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Maximum neck length</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
</tbody>
</table>

### USB 2.0 Interface Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Min. Spacing</th>
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<tbody>
<tr>
<td>Line-to-line spacing</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum line width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum neck width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Maximum neck length</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
</tbody>
</table>

### PCI Bus Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
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</thead>
<tbody>
<tr>
<td>Line-to-line spacing</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum line width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum neck width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Maximum neck length</td>
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### EMbus Interface Constraints

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
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</thead>
<tbody>
<tr>
<td>Line-to-line spacing</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum line width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Minimum neck width</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
</tr>
<tr>
<td>Maximum neck length</td>
<td>0.2 mm</td>
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</tbody>
</table>

### MCP Constraints 2

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.
Digital Video Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

---

PHYSICAL_RULE_SET

SPACING_RULE_SET

DISPLAYPORT

MCP_DV_COMP

LVDS_100D

WEIGHT

TABLE_SPACING_RULE_ITEM

TABLE_SPACING_RULE_HEAD

LINE-TO-LINE SPACING

ON LAYER?

=100_OHM_DIFF

=100_OHM_DIFF

=3x_DIELECTRIC

=3x_DIELECTRIC

Y

76

WEIGHT

TABLE_SPACING_RULE_ITEM

TABLE_SPACING_RULE_ITEM

TABLE_PHYSICAL_RULE_ITEM

TABLE_PHYSICAL_RULE_ITEM

TABLE_PHYSICAL_RULE_HEAD

DIFFPAIR NECK GAP

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=STANDARD

=STANDARD

=STANDARD

=STANDARD

=STANDARD

MAXIMUM NECK LENGTH

TOP,BOTTOM

TOP,BOTTOM

TOP,BOTTOM

TOP,BOTTOM

LINE-TO-LINE SPACING

=4x_DIELECTRIC

=4x_DIELECTRIC

=4x_DIELECTRIC

=4x_DIELECTRIC

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

MINIMUM LINE WIDTH

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

MINIMUM NECK WIDTH

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF

=100_OHM_DIFF
PCI, LPC, HDA, SPI, RGMII, SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

Constraints are based on MCP79 Design Guide DG-03328-001_V06

PCi, LPC, SPI, HDA, SMBUS, SPI, RGMII, SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

**K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS**

### PHYSICAL RULE SET

<table>
<thead>
<tr>
<th>Layer</th>
<th>Width</th>
<th>Minimum Neck Width</th>
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<th>Comment</th>
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<tbody>
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<td>0.075</td>
<td>0.085</td>
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<tr>
<td>B</td>
<td>0.085</td>
<td>0.075</td>
<td>0.085</td>
<td>*</td>
</tr>
<tr>
<td>C</td>
<td>0.085</td>
<td>0.075</td>
<td>0.085</td>
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<td>D</td>
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<td>0.075</td>
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**CONSTRAINTS FOR BGA AREA**

<table>
<thead>
<tr>
<th>BGA_P1MM</th>
<th>0.3 MM</th>
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<th>0.1 MM</th>
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<tbody>
<tr>
<td>BGA_P2MM</td>
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<td>0.1 MM</td>
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**TABLE PHYSICAL RULES**

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<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
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</thead>
<tbody>
<tr>
<td>PHYSICAL RULE SET</td>
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<td>0.85 MM</td>
<td>0.081 MM</td>
</tr>
<tr>
<td>DEFAULT</td>
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<td>0.081 MM</td>
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**TABLE BOARD INFO**

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<thead>
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<tr>
<td>A</td>
<td>ALLEGRO</td>
<td>D</td>
<td>3</td>
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