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Power Block Diagram

SYNC_DATE=08/23/2006  
SYNC_MASTER=(T9_MLB)

REV.  

APPLE COMPUTER INC.  

D  051-7221  14-8-0

D  051-7221  14-8-0

SCALE  

NONE
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Power Block Diagram

SYNC_MASTER=N/A  SYNC_DATE=N/A

051-7225 14.0.0

Apple Computer Inc.
### BOM Variants

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference</th>
<th>CRITICAL</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>

### M75 BOM Groups

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<tr>
<th>BOM Group</th>
<th>Description</th>
<th>Reference</th>
<th>CRITICAL</th>
<th>BOM Options</th>
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</thead>
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### Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>Bar Code</th>
<th>Description</th>
<th>Reference</th>
<th>CRITICAL</th>
<th>BOM Options</th>
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<tbody>
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</table>

### Module Parts

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<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference</th>
<th>CRITICAL</th>
<th>BOM Options</th>
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<tbody>
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### BOM Configuration

<table>
<thead>
<tr>
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<th>Reference</th>
<th>CRITICAL</th>
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</table>
**DVT (cont'd)**

12.6.0: Thermal Sensors: Added B5150/B5154 in case low pass filter is needed for KHC1033

12.5.0: Power Control: Corrected alias connections for D3/5/6/7/8 signals

12.4.0: Thermal Sensors: Added thermal sensor to connector for right chassis gap

12.3.0: Thermal Sensors: Updated B3/9/11 configurations

12.2.0: Thermal Sensors: Updated B5/B031/B032/11 to 0.6B

12.1.0: Thermal Sensors: Updated B8/B031/B032/11 to 0.6B

12.0.0: Thermal Sensors: Updated B7/B031/B032/11 to 0.6B

8.1.0: Thermal Sensors: Updated B4/B031/B032/11 to 0.6B

8.0.0: Thermal Sensors: Updated B3/B031/B032/11 to 0.6B

6.1.0: Thermal Sensors: Updated B2/B031/B032/11 to 0.6B

4.1.0: Thermal Sensors: Updated B1/B031/B032/11 to 0.6B

2.1.0: Thermal Sensors: Updated B0/B031/B032/11 to 0.6B

**EVT**

01/04/07 -- Clock Termination: Removed NO STOP properly from RS04

01/04/07 -- Clock Termination: Corrected CR (termination added cap and removed connection to VCC5)

01/04/07 -- GP2 FR: Added VREF support for unterminated memory mode (added FETs and pulled up 8B)

01/04/07 -- GP2 FR: Added VREF support for unterminated memory mode (added 2FETs and pulled up 8B)

01/04/07 -- Power Supplies: Moved 5% power supply feedback connection from R741 to R743

01/04/07 -- Power Supplies: Added VREG_25V to CP4922 from 8B (layout improvements)

01/04/07 -- Power Supplies: Added VREG_24V to CP4922 from 8B (layout improvements)

01/04/07 -- Power Supplies: Added VREG_24V to CP4922 from 8B (layout improvements)

01/04/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)

01/04/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request

01/03/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)

01/03/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)

01/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines

01/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)

02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)

02/28/07 -- Left Clutch IC: Updated both 1-FET connectors to new KPM (part update for shell plating)

02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)

02/26/07 -- Thermal Sensors: Updated B3/9/11 to 0.6B

02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates

02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)

02/25/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)

02/24/07 -- Power Supplies: Corrected FB CLK termination (added cap and removed connection to VDDQ)

02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)

02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)

02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup

02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup

01/28/07 -- Clock Conn: Reconnected IDD power FET gate control circuitry to properly implement soft start (added one wire)

01/29/07 -- SN Decoupling: Removed filtering for PIVVS_32.fullName=AP_B to enable PIVVS_32 connections at SN

01/29/07 -- SN Decoupling: Changed resistor about reference designation from R932 to R932-V

01/25/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)

01/25/07 -- SB GPIOs: Added pass FET for page25.csa to TBD in T9_MLB to get pullup updates

01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0

01/24/07 -- Power Sequencing: Added 8B to create RC delay for 1.5 and 1.05V S0 rails

01/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

01/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup

01/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup

01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)

01/18/07 -- Power Sequencing: Added 8B to create RC delay for 1.5 and 1.05V S0 rails

01/17/07 -- BOM: Added Hynix BOM configurations

01/17/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONs to GPU straps)

01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs

01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support

01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0

01/17/07 -- Power Sequencing: Changed to Rev C of TI FireWire MCM (APN: 338S0435)

01/17/07 -- IMVP: Updated BOMOPTIONs and values for ISL9504B

01/17/07 -- Power Sequencing: Changed to Rev C of TI FireWire MCM (APN: 338S0435)

01/17/07 -- Power Sequencing: Changed to Rev C of TI FireWire MCM (APN: 338S0435)

01/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)

01/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel

01/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering

01/15/07 -- NV (HPI, LSP_FB_H, FVFX) changed to single pin nets to prevent LSP glitches per Intel

01/15/07 -- Yukos Power Control: Crystal caps changed to 18pF (rdar://5945834) and (rdar://5945835)

12.7.0: Thermal Sensors: Added reflow sensor to EMC1033 to indicate device should be on 03 call

12.6.0: Temperature Sensors: Added reflow sensor to EMC1033 to indicate device should be on 03 call

12.5.0: Power Control: Corrected alias connections for D3/5/6/7/8 signals

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2.1.0: Thermal Sensors: Updated B0/B031/B032/11 to 0.6B

**Revision History**

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**SCALE**

**D**

**B**

**C**

**A**
CPUTHMSNS can not be supported due to layout constraints

### Thermal Diode Connectors
- LPC+ Debug Connector
  - LPC+ Debug Connector
  - LPC+ Debug Connector
- Left I/O Power Connector
  - Left I/O Power Connector

### Battery Digital Connector
- Battery Digital Connector
  - Battery Digital Connector

### System Validation TPs
- System Validation TPs
  - System Validation TPs

### Left ALS Connector
- Left ALS Connector
  - Left ALS Connector

### Fan Connectors
- Fan Connectors
  - Fan Connectors

### Left Clutch Barrel Connector
- Left Clutch Barrel Connector
  - Left Clutch Barrel Connector

### Other Func Test Points
- Other Func Test Points
  - Other Func Test Points

### CPU FSB NO_TESTSs
- CPU FSB NO_TESTSs
  - CPU FSB NO_TESTSs

### NB NO_TESTSs
- NB NO_TESTSs
  - NB NO_TESTSs

### GPU NO_TESTSs
- GPU NO_TESTSs
  - GPU NO_TESTSs

### ICT Test Points

### Functional Test Points

**NOTE:** 10 additional GND test points are called out separately in these notes.
Current numbers from Merom for Santa Rosa EMTs, doc #22221.

Current Voltage:
- 1.05V (CPU IO POWER)
- 1.5V (CPU INTERNAL PLL POWER)

Standard Voltage:
- 4.0 A (Enhanced Deeper Sleep)
- 6.0 A (Deep Sleep SuperLFM)
- 8.0 A (Deep Sleep HFM)
- 9.4 A (Enhanced Deeper Sleep)
- 11.5 A (Deeper Sleep)
- 16.0 A (Deep Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 27.4 A (Sleep HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 25.5 A (SuperLFM)
- 30.4 A (LFM)
- 44.0 A (Design Target)

Low Voltage:
- 2500 mA (after VCC stable)
- 4500 mA (before VCC stable)

Ultra Low Voltage:
- 130 mA
- 9.4 A (Enhanced Deeper Sleep)
- 11.5 A (Deeper Sleep)
- 16.0 A (Deep Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 27.4 A (Sleep HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 25.5 A (SuperLFM)
- 30.4 A (LFM)
- 44.0 A (Design Target)

CPU Power & Ground

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12345678

12345678

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0651 adapter board to support CPU, VM & SW debugging.
**CRT Disable / TV-Out Enable**

Tie VCC \_TV\_L and VCCA\_L to GND.

If SDVO is used, VCCA\_SDVO must remain powered with proper decoupling. Otherwise, tie VCCA\_L to GND.

**Follow instructions for LVDS and CRT & TV-Out Disable above.**

---

**Internal Graphics Disable**

Can tie the following rails to GND:

- CRT & TV-Out Disable
- rails must be filtered except for VCCA\_CRT.

- CRT & TV-Out Disable
- All CRT/TV-Out rails must be powered.
  All rails must be filtered except for VCCA\_CRT.

**TV-Out Signal Usage:**

- For CRT and TV-Out only
- Component: DAC\_B & DAC\_D
- Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs can share filtering with VCCA\_CRT.

- CRT & TV-Out Disable
- tie VCCA\_CRT and VCC\_CRT to GND. Must power all TV-Out rails. VCCA\_CRT and VCC\_CRT must share filtering with VCCA\_CRT.

- CRT Disable / TV-Out Disable
- tie VCCA\_CRT to GND. Must power all TV-Out rails. VCCA\_CRT must remain powered, but can omit filtering components. Unused DAC outputs can share filtering with VCCA\_CRT.

**Note:**

- SR DG says to tie LVDS\_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5077926.

- If SDVO is used, VCC\_D must remain powered with proper decoupling. Otherwise, SDVO must remain powered with proper decoupling.

---

**NB PEG / Video Interfaces**

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- Apple Computer, Inc.
- 1-4-3-4
- 1992

---

**REV.**

- A
- B
- C
- D
Crestline Thermal Diode Pins

Mainly for investigation, if not used, alias these nets directly to GND.

NOTE: TDB = _N
NOTE: TDE = _P
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
RTC Power Sources

- Coin-Cell Connector
- SB RTC Crystal
- VRMPWRGD Inverter
- PWROK Circuit
- CPU VCore ForcePSI

Platform Reset Connections

- Unbuffered
- Mixed GFX GPU Reset Support
- PCI Reset Connections

NOTES:
- R2800 and R2805 form the double-fault protection for RTC battery.
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MAKE_BASE=TRUE
- NB_RESET_L
- ENET_RESET_L
- CRITICAL
- NB_RESET_L
- NB_RESET_L

This part is never stuffed, it provides a set of pads on the board to short or to inhibit a reset button.

This delay ensures that GPU clocks and clocks are still running.

This ensures that GPU is put into reset while chip is still powered and clocks are still running.
"Factory" (thru-hole) slot
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
**FireWire PHY Config Straps**

- Configured PHY for...
  - 2-port Portable Power Class (1394B)
  - Port "A" Data-Stroke only (1394A)
  - Port "B" Bilingual (1394B)

**Termination**

Place close to FireWire PHY

- If FireWire TPA/TPB pairs are NOT appropriate connectors and/or to FireWire TPA/TPB pairs to their necessary aliases to map the signal aliases required by this page:
  - =GND_CHASSIS_FW_EMI_R
  - =GND_CHASSIS_FW_PORT1
  - =GND_CHASSIS_FW_PORT0U
  - =PP3V3_FW_LATEVG
  - =PPVP_FW_PORT1

**Power aliases required by this page:**

- R4390 should be 390 Ohms max for a 3.3V rail and should be biased to 2.4V for margin to at least 2.1V for FW signal integrity.
- PP2V4_FW_LATEVG needs to be biased 85mV for viability. If not available, 1.2V must be used.

**Note:** Trace PPVP_FW_PORT1 must handle up to 5A current and should be 120mV for viability. APEF needs to be isolated from all local grounds per 1394B spec.

When a bilingual device is connected to a data-only device, there is no DC path between them to avoid ground offset issues.

APEF should be hard-connected to logic ground for speed signaling and detection detection currents per 1394B VI.13.
NOTE: Unused pins have “SMC_Pxx” names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

NOTE: Unused pins have “SMC_Pxx” names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
LPC+ Connector  
FWH_INIT_L Generation

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**PLACEMENT NOTE:** Place Q5190 close to R5190 to minimize CPU_INIT_L stub.

**SYNC_DATE:** 03/19/2007

**SYNC_MASTER:** M76_MLB

**A:** 47 88

**D:** 051-1223 16-0-0

**CRITICAL**
CPU Voltage Sense / Filter

Place short near IMVP6 center

NB GFX Current Sense Filter

Place RC close to SMC

GPU Voltage Sense / Filter

Place short near U1000 center

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

PBUS Voltage Sense & Filter

Place RC close to SMC

NB Core Current Sense Filter

Place RC close to SMC

CPU Current Sense Filter

Place RC close to SMC

DCIN Current Sense Filter

Place RC close to SMC

Battery (PBUS) Current Sense Filter

Place RC close to SMC

GPU Current Sense Filter

Place RC close to SMC

NB 1.8V Current Sense Filter

Place RC close to SMC

SO/GPU 1.25V Current Sense Filter

Place RC close to SMC

CPUVCORE_ISENSE_CAL

Current & Voltage Sensing
**Placement note:**

**CRITICAL**

**J5520**

**J5510**

**NO STUFF**

**18PF**

**CERM402 50V 5%**

**518S0487**

**GPU/Heat Pipe & Bottom Case Skin Thermal Sensor**

**GPU Die Thermal Sensor**

**No Stuff**

**10K 5%**

**MF-LF 1/16W**

**402**

**CERM**

**50V 10%**

**402CERM50V 10%**

**0.0022uF**

**0.1uF**

**402X5R**

**R5500**

**5% 1/16W**

**R5550**

**SMBUS_SMC_B_S0_SDA**

**SMBUS_SMC_0_S0_SCL**

**SMBUS_SMC_A_S3_SDA**

**SMBUS_SMC_A_S3_SCL**

**SMDATA**

**SMCLK**

**U5500**

**U5570**

**U5550**

**402MF-LF**

**1/16W 5%**

**1/16W 1%**

**10K**

**402**

**CERM 10V 20%**

**402CERM 10V 20%**

**0.1UF**

**SCLK**

**THM**

**THM***

**SDATA**

**BI**

**D**

**D-**

**D+**

**SYNC_MASTER=(MASTER)**

**SYNC_DATE=(MASTER)**

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I2C addresses:
- ADDR low -> 0x30, 0x32
- ADDR high -> 0x31, 0x33
- Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
- Package Top
- Desired orientation when placed on board bottom-side:
- Top-through View

Sudden Motion Sensor (SMS)
C6100
1 2
402
0.1UF 10V 20%
CERM

R6101
1 2
402
3.3K MF-LF 5% 1/16W

R6100
1 2
402
3.3K MF-LF 5% 1/16W

R6114
1 2
402
1/16W 5%
MF-LF

PLACEMENT_NOTE=Place R6114 within 12.7mm of U6100

U6100
1
7
6
5

CRITICAL
16MBIT
SOI
SST25VF016B

R6190
1 2
402
15
1/16W 5%
MF-LF

PLACEMENT_NOTE=Place R6190 within 12.7mm of U2300

R6191
1 2
402
15
1/16W 5%
MF-LF

PLACEMENT_NOTE=Place R6191 within 12.7mm of U2300

R6193
1 2
402
15
1/16W 5%
MF-LF

PLACEMENT_NOTE=Place R6193 within 12.7mm of U2300

SPI BootROM
55 88
14.0.0051-7225
SYNC_DATE=03/16/2007
SYNC_MASTER=T9_NOME
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J6900

CRITICAL
M-RT-SM
87438-0663

J6950

CRITICAL
SM04B-ACH
M-RT-SM

DZ6951

NO STUFF
8V-100PF
402

DZ6950

NO STUFF
8V-100PF
402

R6950

10
402MF-LF1/16W
5%

PPBUS_G3H
74
63 62 61 60 59 58 57 49 40 8
7

SYNC_DATE=09/09/2006
SYNC_MASTER=(M59_SYNC)

PBus-In & Battery Connectors

A
B
C
D

Left I/O Power Connector

Battery Connector (Digital Signals)
Vout = 0.75V \times (1 + \frac{Ra}{Rb})

Vout = 1.2496V

8A max output (L74107 limit)

Vout = 1.055V

10A max output (L74607 limit)
Vout = 1.50V
8A max output
(L7620 limit)

Vout = 0.75V * (1 + Ra / Rb)

SCW (2 OF 2)
Power Control Signals

3.425V "G3Hot" Supply

Supply needs to guarantee 3.12V delivered to SMU Vref generator.

State

Run (S0)  Sleep (S3)  S3/4 Delay
0  1  0
1  0  0

Battery off Circuit

SHAPE

3.425V G3Hot Supply & Power Control

LTC2900 Typical threshold is 93.5% (6.45V, 3.084V, 1.685V, 1.12V)

Other S0 Rails PWRGD Circuit

Does not include SMU rails

46 77 51 28

0.22μF 16V 20%

CRITICAL 10K 1/16W

CPU/MEM 0.1μF CERM

Vout = 3.425V

20mA max output

(Switcher limit)

173K 1/16W 5%

Vout = 1.25V * (1 + Ra / Rb)

NOTE: 0.9V/2.5V is not checked!
Signal aliases required by this page:
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_PLLVDD
- =PP3V3_GPU_VDD33

Component values provided by this page:
R8622 1
R8620 1/16W 1%
C8633 402MF-LF
C8640 4.7UF 1%
C8636 603CERM 6.3V 20%
R8617 1
R8616 1/16W 5%
C8641 0.1uF X5R

Apple Computer Inc.
PGOOD Monitor for GPU Rails

LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit

LTC2900 typical threshold is 94.56 (3.3V0, 3.3V1, 3.3V2, 1.120)

Fast wake condition is worst case. ICHx can create an X duration of 1 sec clock (12 ms). If mux select is on core well and N/O gate is implemented, glitch filter or other PGOOD assertion time is required. PGOOD assert will vary at end of 50 ms timer. If mux select on resume well, then observed PGOOD will not change during 50 ms transition and ICHx will honor whatever PGOOD delay is provided.

GPU_power rails have come up and are valid (which should be before platform reset assertion). Could be eliminated if GPIO moved to resume well.

Current select Conditioning

GPU LVDS I/F

LVDS Data Mux Power Supply

Panel/Backlight Control Mux

GPU DDC Pass FETs
Left ALS Connector

White colored version of 51820469

SATA HDD & IR & SIL Flex Connector

NOTE: DATA_A/Q nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.
Most CPU signals with impedance requirements are 55-ohm single-ended.

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

Design Guide recommends each strobe/signal group is routed on the same layer.

DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Min Spacing</th>
<th>Max Spacing</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
<th>Differential Neck Width</th>
<th>Differential Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_DSTB_L</td>
<td>1:1</td>
<td>2:1</td>
<td>27 mils</td>
<td>27 mils</td>
<td>27 mils</td>
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<tr>
<td>FSB_COMMON</td>
<td>3:1</td>
<td></td>
<td>27 mils</td>
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<td>FSB_DATA</td>
<td>3:1</td>
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</table>

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

### CPU / FSB Net Properties

<table>
<thead>
<tr>
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<th>Min Spacing</th>
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<th>Min Neck Width</th>
<th>Max Neck Length</th>
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<td>27 mils</td>
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<td>27 mils</td>
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</table>

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DS, Rev 0.9 (#20517), Sections 4.2 & 4.3
**PCI-Express / DMI Bus Constraints**

**Video Signal Constraints**

**NB Constraints**

Video Signal Constraints

---

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

---

PCI-Express / DMI Bus Constraints
Memory Net Properties

<table>
<thead>
<tr>
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<th>SPACING</th>
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</thead>
<tbody>
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<td>MEM_A_DQS_P&lt;6&gt;</td>
<td>MEM_A_DQ&lt;63..56&gt;</td>
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<tr>
<td>MEM_A_DQS_P&lt;5&gt;</td>
<td>MEM_A_DQS_P&lt;4&gt;</td>
</tr>
<tr>
<td>MEM_A_DQS_P&lt;3&gt;</td>
<td>MEM_A_DQS_P&lt;2&gt;</td>
</tr>
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<td>MEM_A_DM&lt;0&gt;</td>
<td>MEM_A_DQ&lt;39..32&gt;</td>
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<td>MEM_A_DQ&lt;31..24&gt;</td>
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</table>
**Disk Interface Constraints**

**USB 2.0 Interface Constraints**

**HD Audio Interface Constraints**

**Internal Interface Constraints**

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.13.2, 10.7 & 10.9

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.17

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.9.1

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.12.2
### Clock Signal Properties

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<td>10</td>
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<tr>
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<td>55</td>
<td>10</td>
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### Clock Net Properties

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<th>Width</th>
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### Clock & BMC Constraints

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</table>

**Notice of Proprietary Property**

Rev. 1.0 (#21112), Sections 14.1 - 14.6
Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

SIM Card Constraints

SIM Card Constraints
# M75 Board-Specific Spacing & Physical Constraints

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<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>TOP</td>
<td>0.100 mm</td>
<td>0.200 mm</td>
<td>0.100 mm</td>
<td>0.200 mm</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>0.100 mm</td>
<td>0.200 mm</td>
<td>0.100 mm</td>
<td>0.200 mm</td>
</tr>
</tbody>
</table>

**Notes:**
- Min. Neck Width and Max. Neck Length are specified in mm.
- Diff PAIR Primary Gap and Neck Gap are also specified in mm.

---

# M75 Rule Definitions

**Note:** Rule violations in different layers may lead to non-compliance with specifications.

## Physical Rules

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
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<tr>
<td>PHYSICAL_RULE</td>
<td>Specifies physical design rules.</td>
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</table>

## Spacing Rules

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<td>Specifies spacing rules.</td>
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</table>

## Area Types

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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>AREA_TYPE</td>
<td>Specifies area types.</td>
</tr>
</tbody>
</table>

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**Important:**
- Violations of specified rules can lead to non-compliance with standards.
- Compliance with specifications is mandatory for successful board design.