

P611:MXM-III, G3-128, 256/512MB, 128-bit, 8/16Mx32 DDR-3 LVDS, DVI_A, DVI_B, TV_OUT, VGA

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HISTORY:

A00: INITIAL VERSION

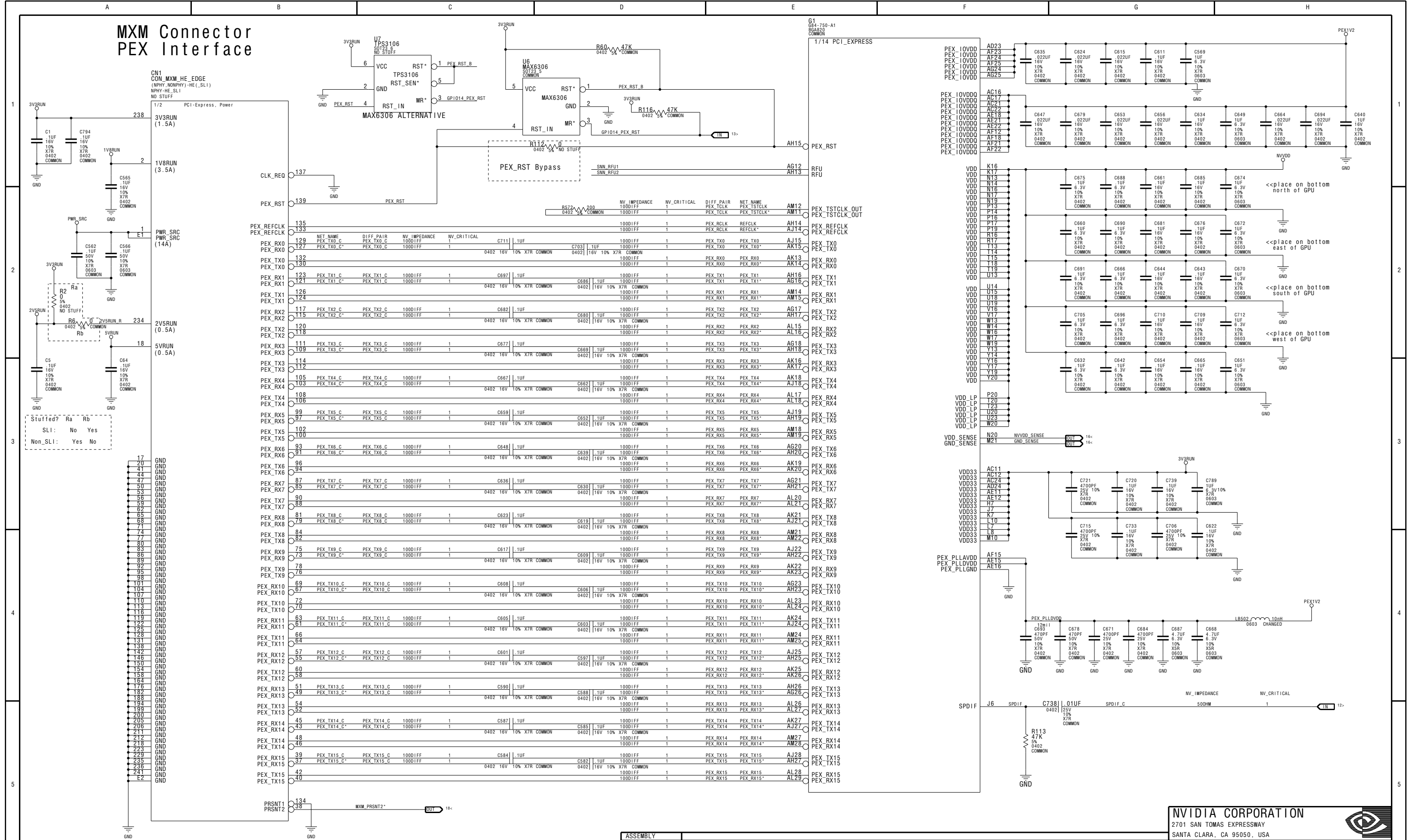
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B	BASE	600-10611-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	0001	600-10611-0001-000	NB8E-SE/G84-750 with HDCP Kit, 512MB, 8pcs 16Mx32 GDDR3 (1Mb Vbios ROM)
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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MXM Connector PEX Interface



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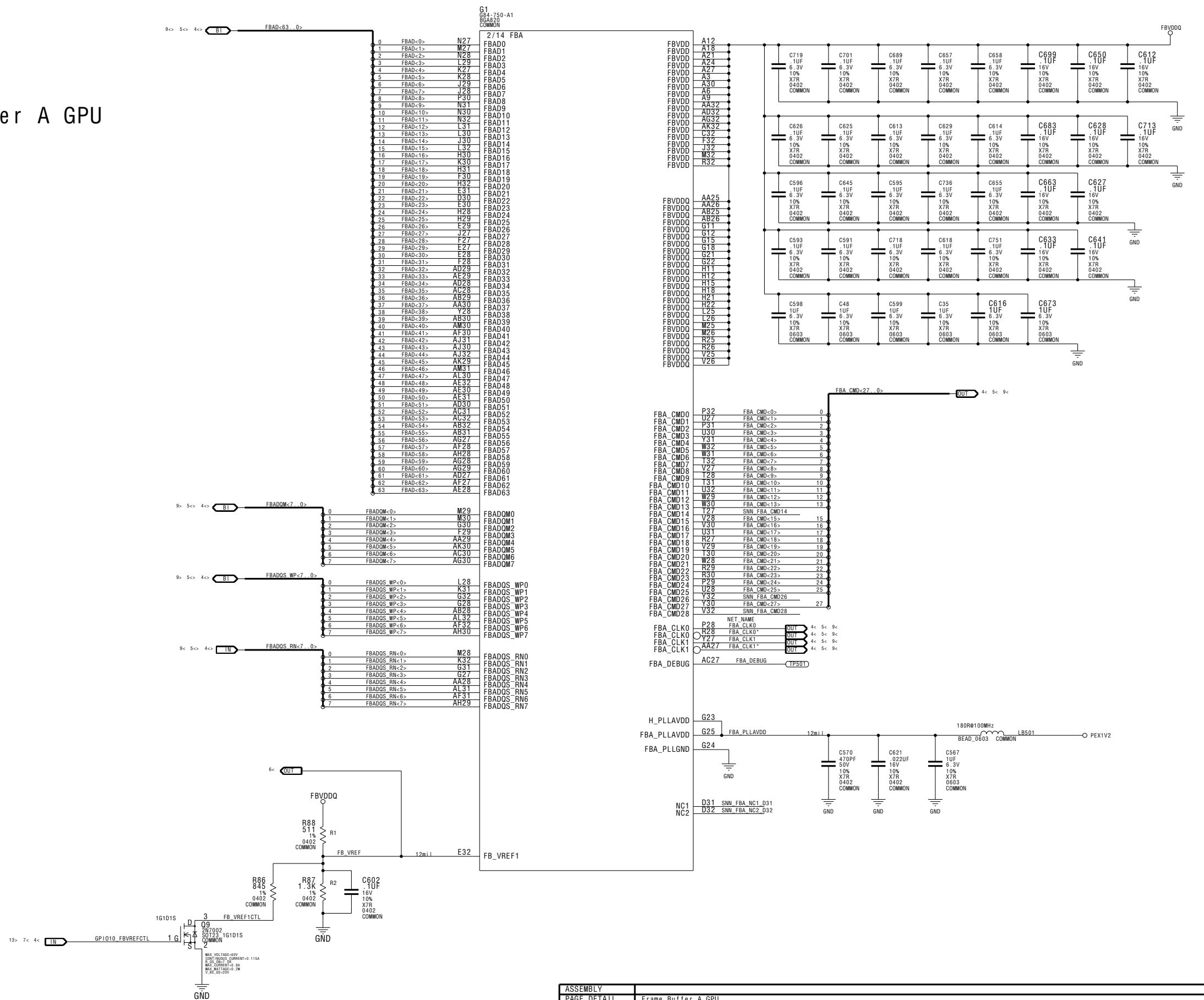


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ASSEMBLY
PAGE DETAIL
PCI EXPRESS Interface

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Frame Buffer A GPU



ASSEMBLY		Frame Buffer A GPU	
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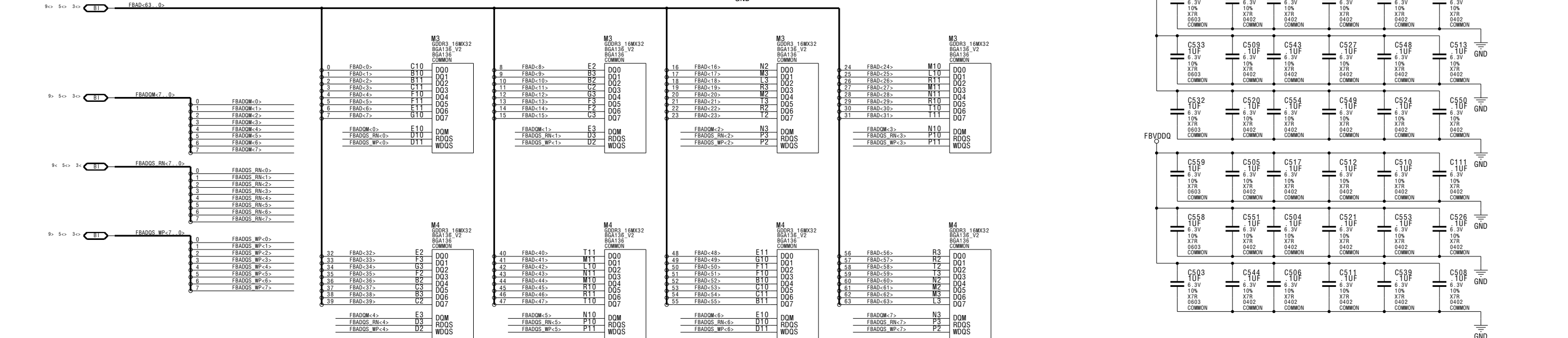
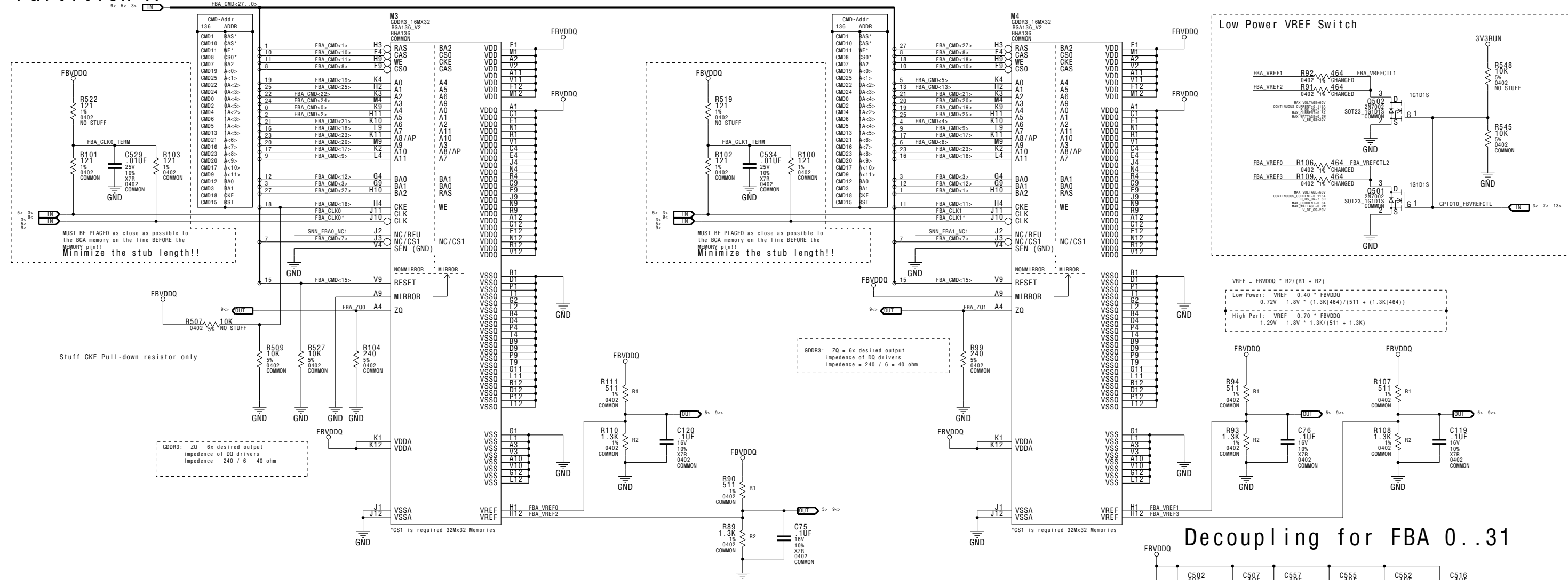
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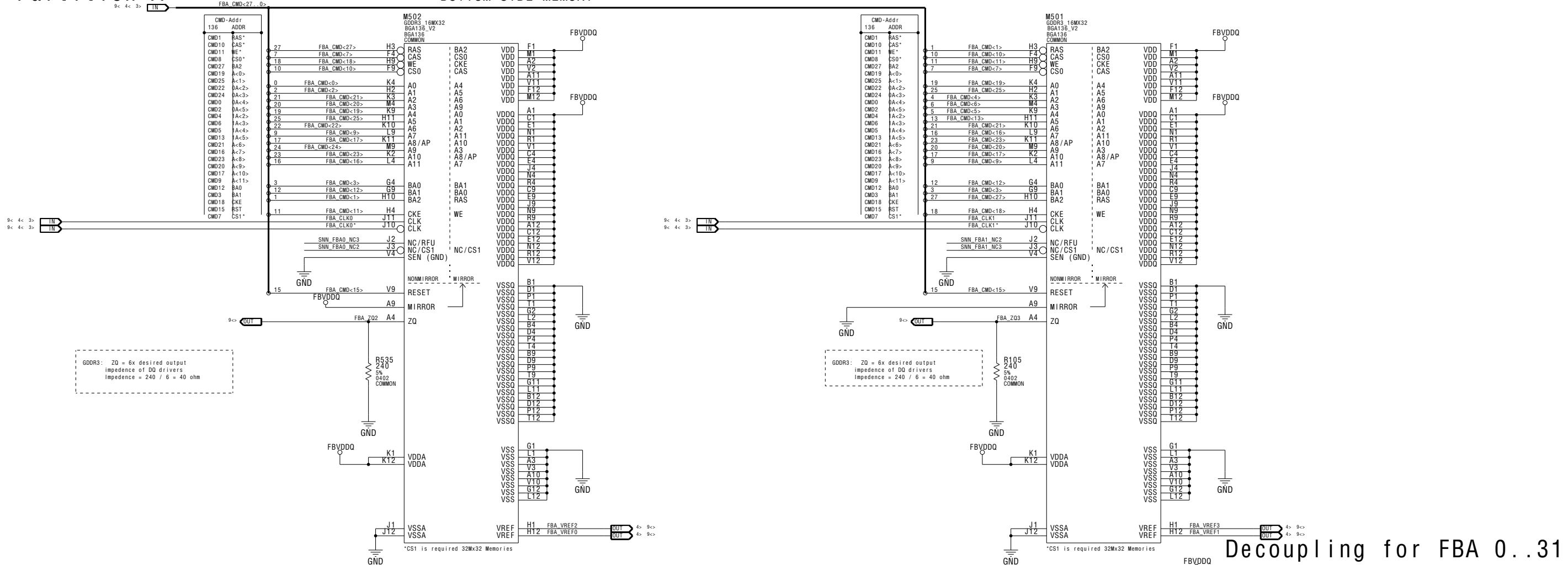
FB Partition A

Topside memory

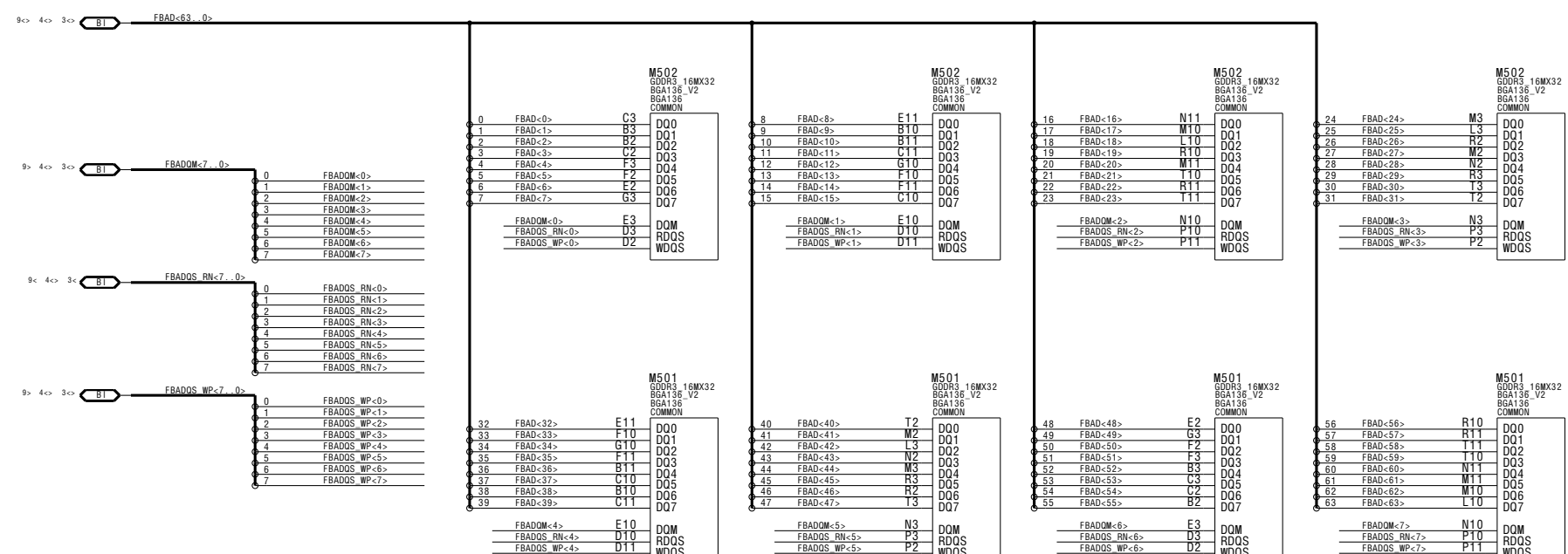
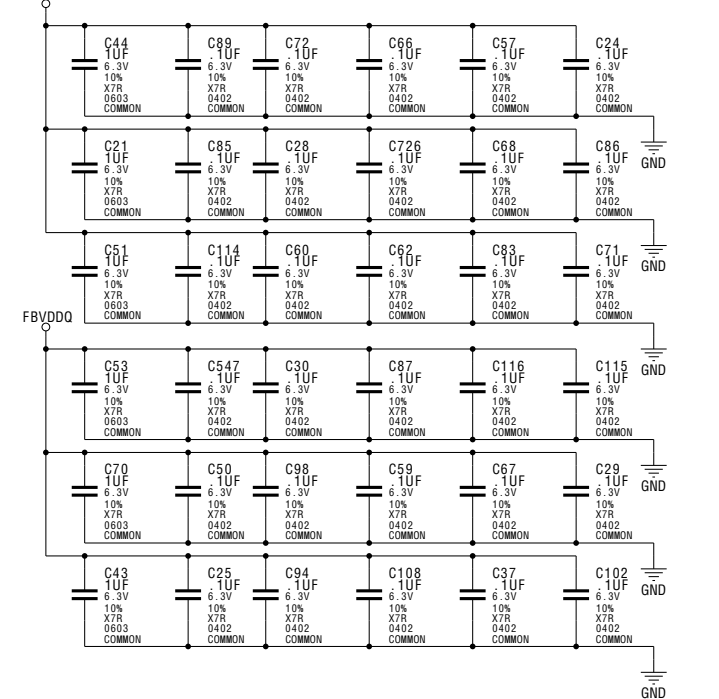


FB Partition A

BOTTOM SIDE MEMORY



Decoupling for FBA 0..31

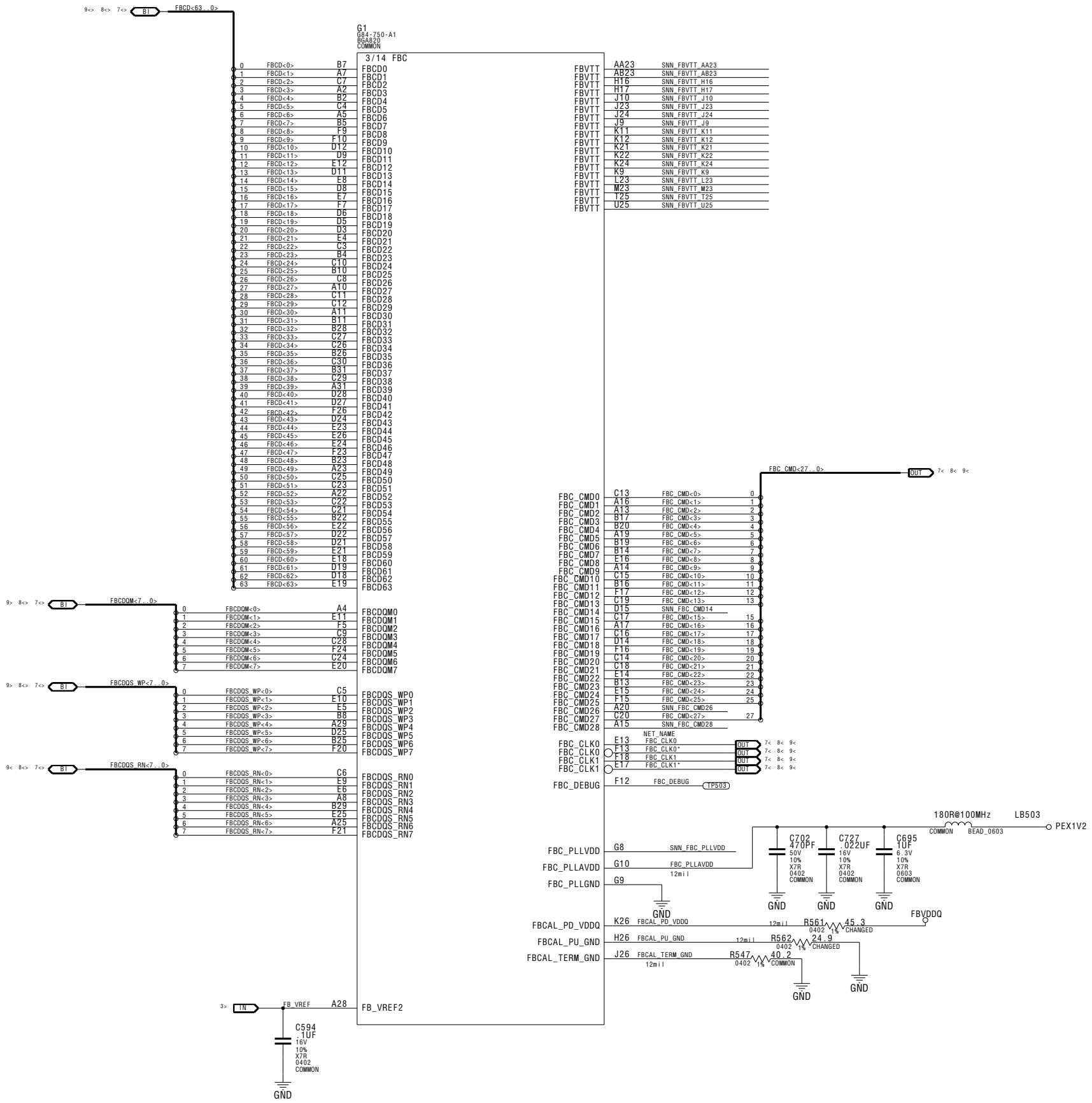


ASSEMBLY PAGE DETAIL Frame Buffer A Memories Rank1

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Frame Buffer C GPU



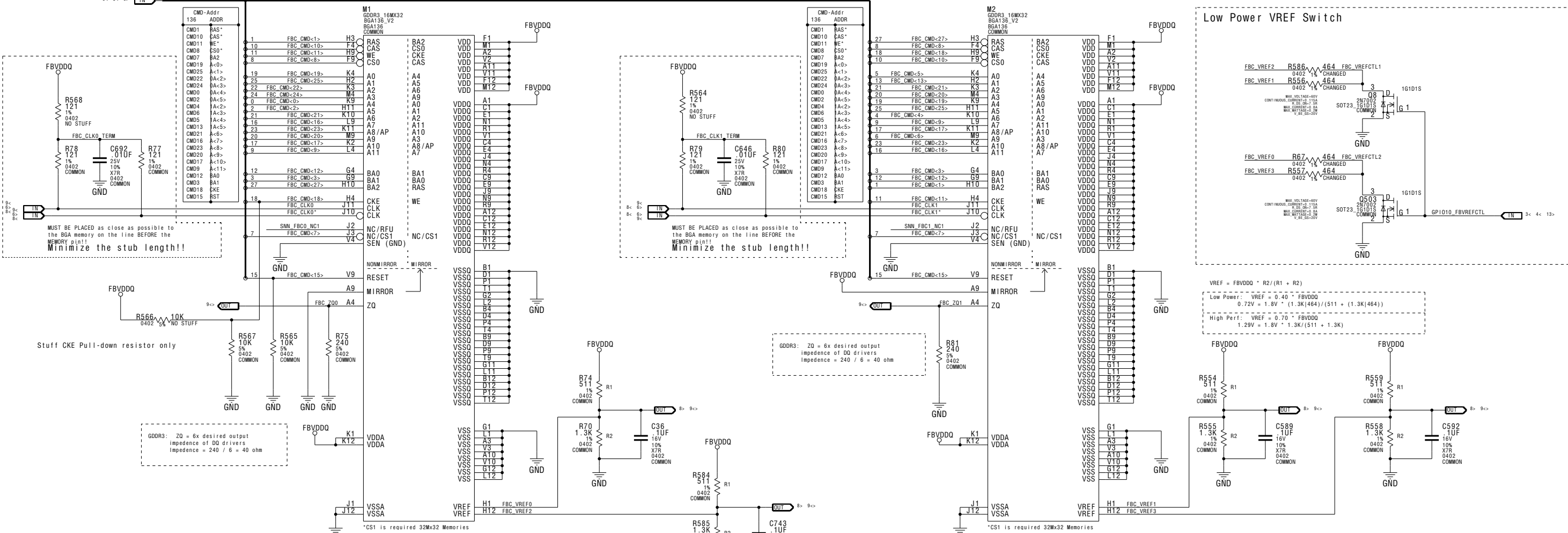
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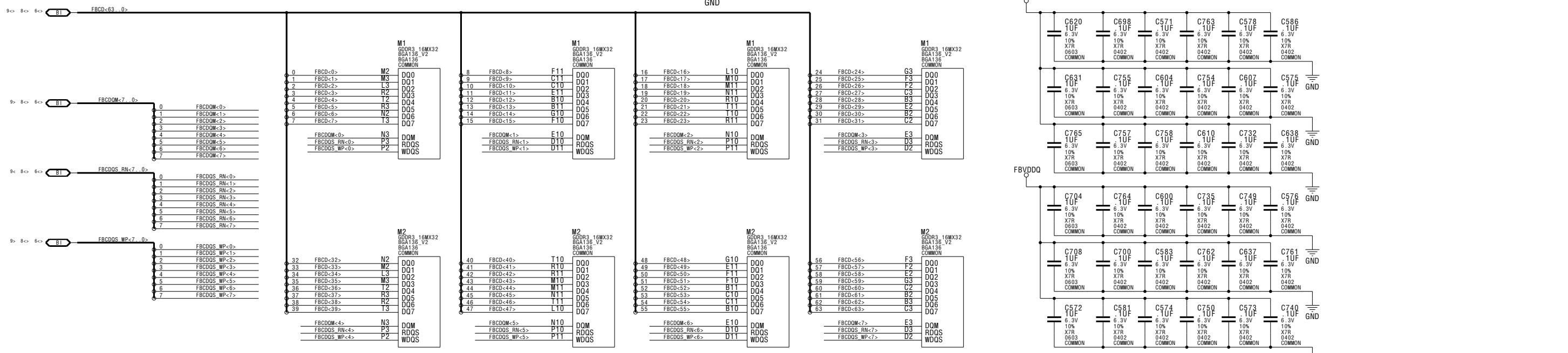
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FB Partition C

Topside memory



Decoupling for FBC 0..31



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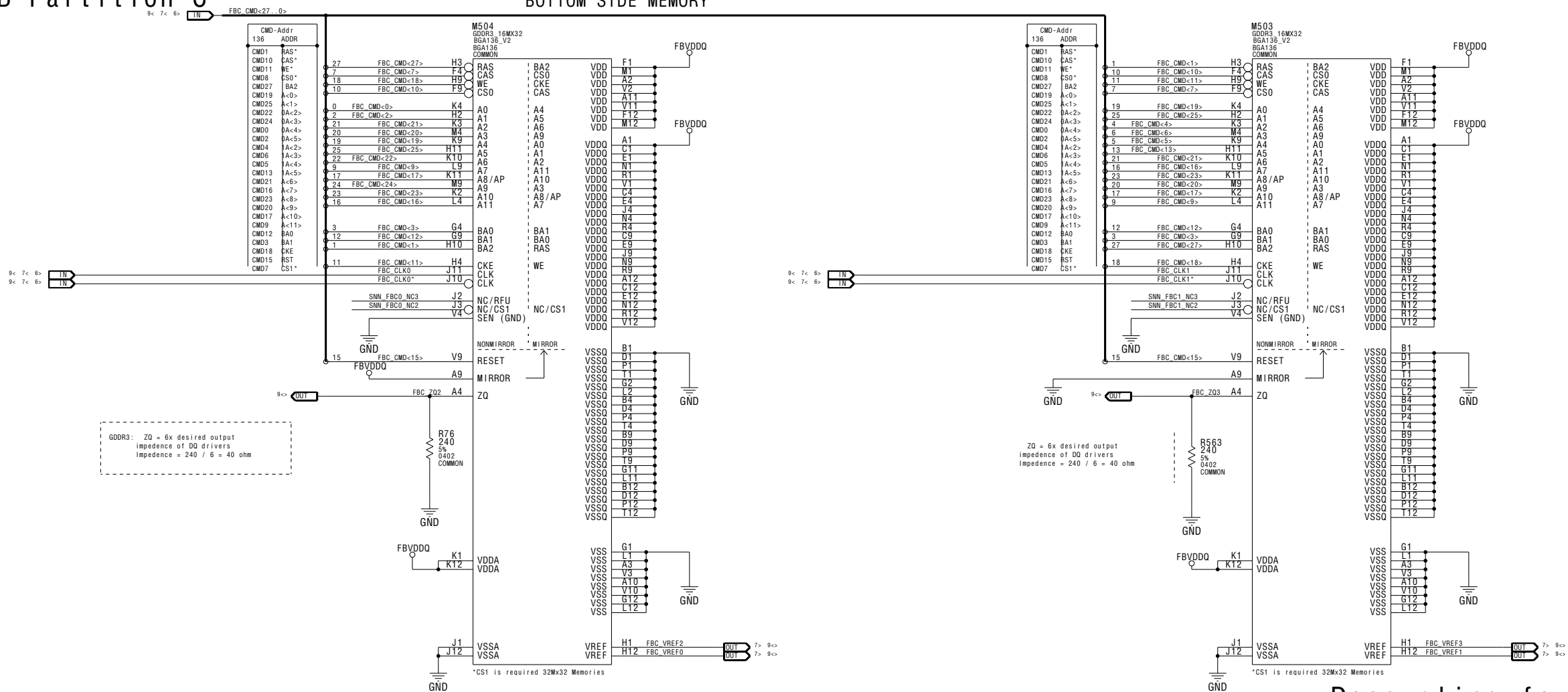
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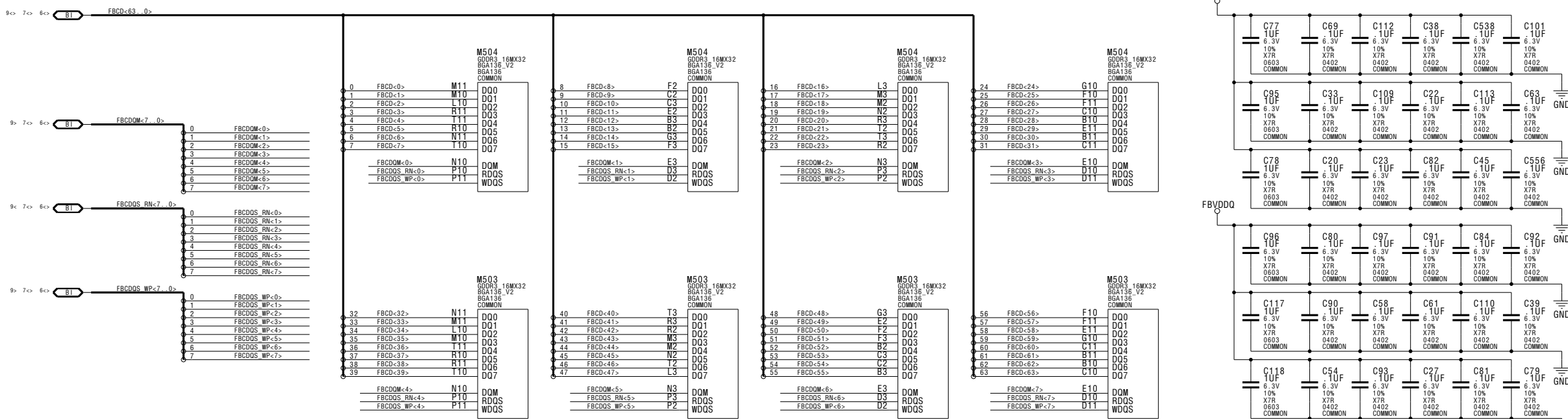
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FB Partition C

BOTTOM SIDE MEMORY



Decoupling for FBC 0..31



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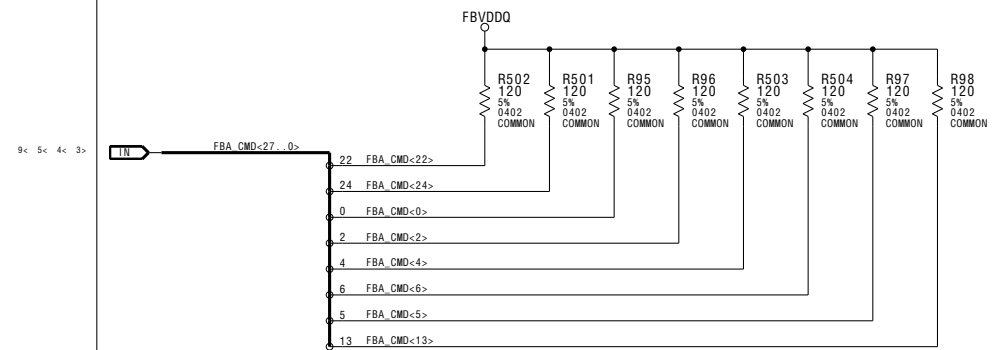
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FrameBuffer Net Rules

NET RULES for FrameBuffer A

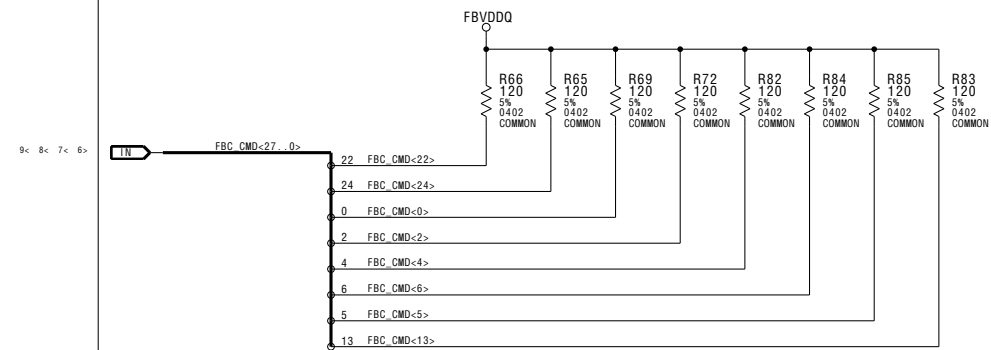
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1
FBA_CMD<27..0>	1	560HM	
FBA<DS> WP<7..0>	1	400HM	
FBA<DS> RN<7..0>	1	400HM	
FBA<DS> R<7..0>	1	400HM	
FBA<DS> B<3..0>	1	400HM	



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.47V	0.02A	12MIL
FBA_VREF1	1.47V	0.02A	12MIL
FBA_VREF2	1.47V	0.02A	12MIL
FBA_VREF3	1.47V	0.02A	12MIL
FBA_Z00	1.47V	0.02A	12MIL
FBA_Z01	1.47V	0.02A	12MIL
FBA_Z02	1.47V	0.02A	12MIL
FBA_Z03	1.47V	0.02A	12MIL

NET RULES for FrameBuffer C

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80DIFF	FBC_CLK0
FBC_CLK0*	1	80DIFF	FBC_CLK0
FBC_CLK1	1	80DIFF	FBC_CLK1
FBC_CLK1*	1	80DIFF	FBC_CLK1
FBC_CMD<27..0>	1	560HM	
FBC<DS> WP<7..0>	1	400HM	
FBC<DS> RN<7..0>	1	400HM	
FBC<DS> R<7..0>	1	400HM	
FBC<DS> B<3..0>	1	400HM	

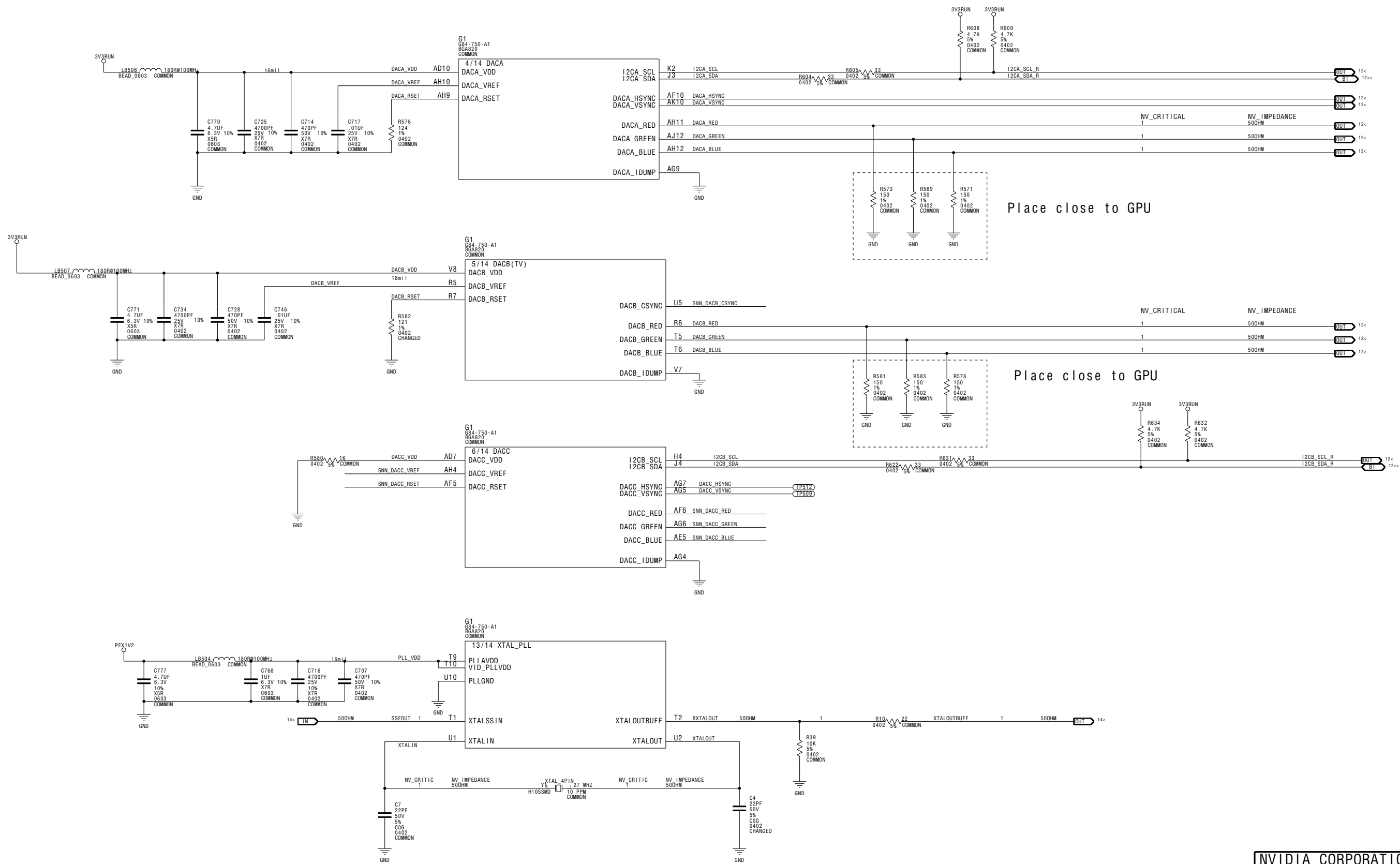


NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBC_VREF0	1.47V	0.02A	12MIL
FBC_VREF1	1.47V	0.02A	12MIL
FBC_VREF2	1.47V	0.02A	12MIL
FBC_VREF3	1.47V	0.02A	12MIL
FBC_Z00	1.47V	0.02A	12MIL
FBC_Z01	1.47V	0.02A	12MIL
FBC_Z02	1.47V	0.02A	12MIL
FBC_Z03	1.47V	0.02A	12MIL

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DACs, Clockgeneration



Place close to GPU

Place close to GPU

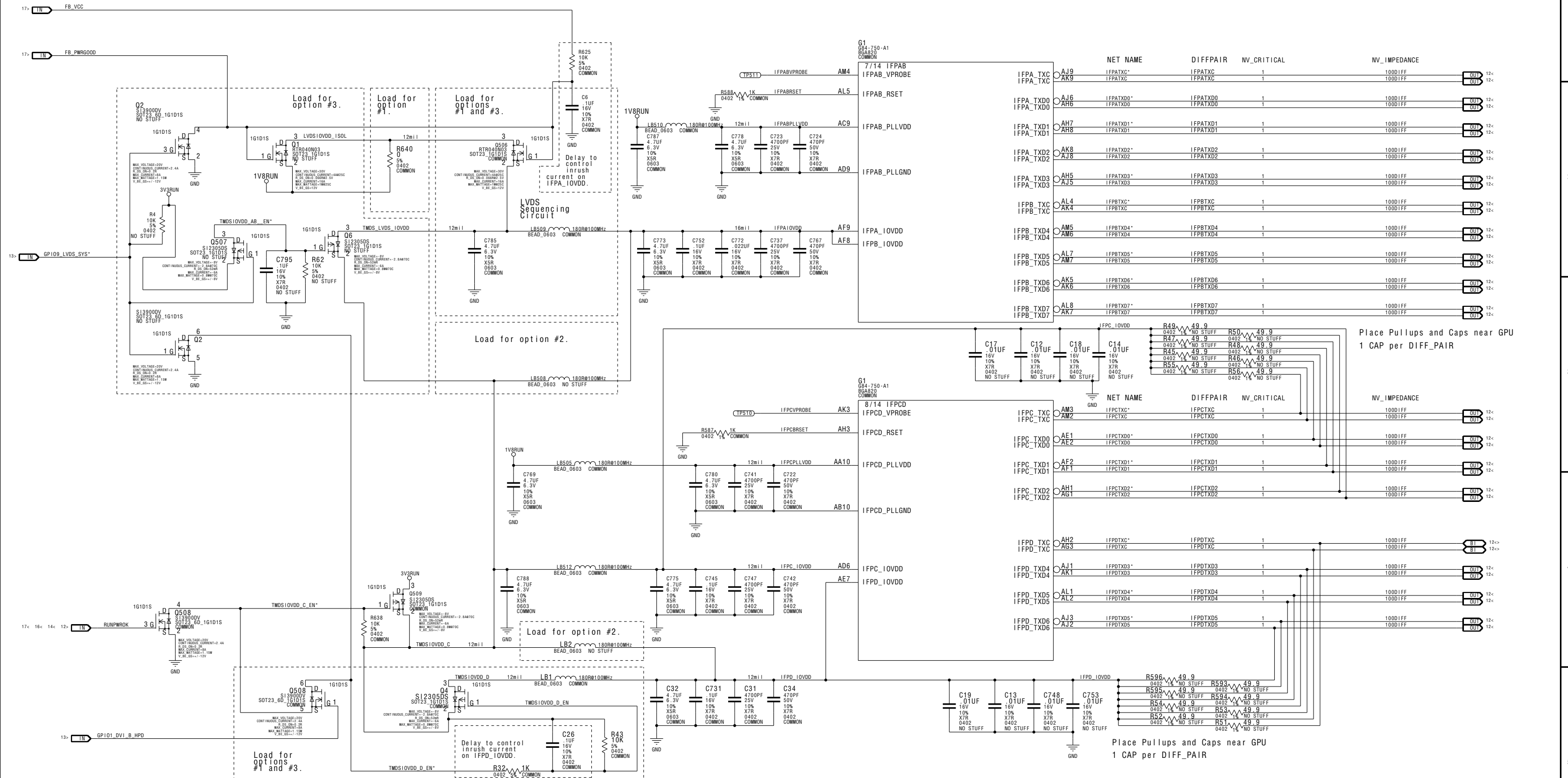
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LVDS / TMDS Interface

Loading options for IFPAB outputs

- Option #1) IFPAB outputs to LVDS only.
- Option #2) IFPAB outputs to DVI-C only.
- Option #3) Controlled with GP109, IFPAB dynamically outputs to LVDS or DVI-C.



NET NAME	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TXC	IFPATXC*	1	100DIFF
IFPA_TXC	IFPATXC	1	100DIFF
IFPA_TXD0	IFPATXD0*	1	100DIFF
IFPA_TXD0	IFPATXD0	1	100DIFF
IFPA_TXD1	IFPATXD1*	1	100DIFF
IFPA_TXD1	IFPATXD1	1	100DIFF
IFPA_TXD2	IFPATXD2*	1	100DIFF
IFPA_TXD2	IFPATXD2	1	100DIFF
IFPA_TXD3	IFPATXD3*	1	100DIFF
IFPA_TXD3	IFPATXD3	1	100DIFF
IFPB_TXC	IFPBTXC*	1	100DIFF
IFPB_TXC	IFPBTXC	1	100DIFF
IFPB_TXD4	IFPBTXD4*	1	100DIFF
IFPB_TXD4	IFPBTXD4	1	100DIFF
IFPB_TXD5	IFPBTXD5*	1	100DIFF
IFPB_TXD5	IFPBTXD5	1	100DIFF
IFPB_TXD6	IFPBTXD6*	1	100DIFF
IFPB_TXD6	IFPBTXD6	1	100DIFF
IFPB_TXD7	IFPBTXD7*	1	100DIFF
IFPB_TXD7	IFPBTXD7	1	100DIFF

Place Pullups and Caps near GPU
1 CAP per DIFF_PAIR

NET NAME	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPC_TXC	IFPCTXC*	1	100DIFF
IFPC_TXC	IFPCTXC	1	100DIFF
IFPC_TXD0	IFPCTXD0*	1	100DIFF
IFPC_TXD0	IFPCTXD0	1	100DIFF
IFPC_TXD1	IFPCTXD1*	1	100DIFF
IFPC_TXD1	IFPCTXD1	1	100DIFF
IFPC_TXD2	IFPCTXD2*	1	100DIFF
IFPC_TXD2	IFPCTXD2	1	100DIFF
IFPD_TXC	IFPDTXC*	1	100DIFF
IFPD_TXC	IFPDTXC	1	100DIFF
IFPD_TXD4	IFPDTXD3*	1	100DIFF
IFPD_TXD4	IFPDTXD3	1	100DIFF
IFPD_TXD5	IFPDTXD4*	1	100DIFF
IFPD_TXD5	IFPDTXD4	1	100DIFF
IFPD_TXD6	IFPDTXD5*	1	100DIFF
IFPD_TXD6	IFPDTXD5	1	100DIFF

Place Pullups and Caps near GPU
1 CAP per DIFF_PAIR

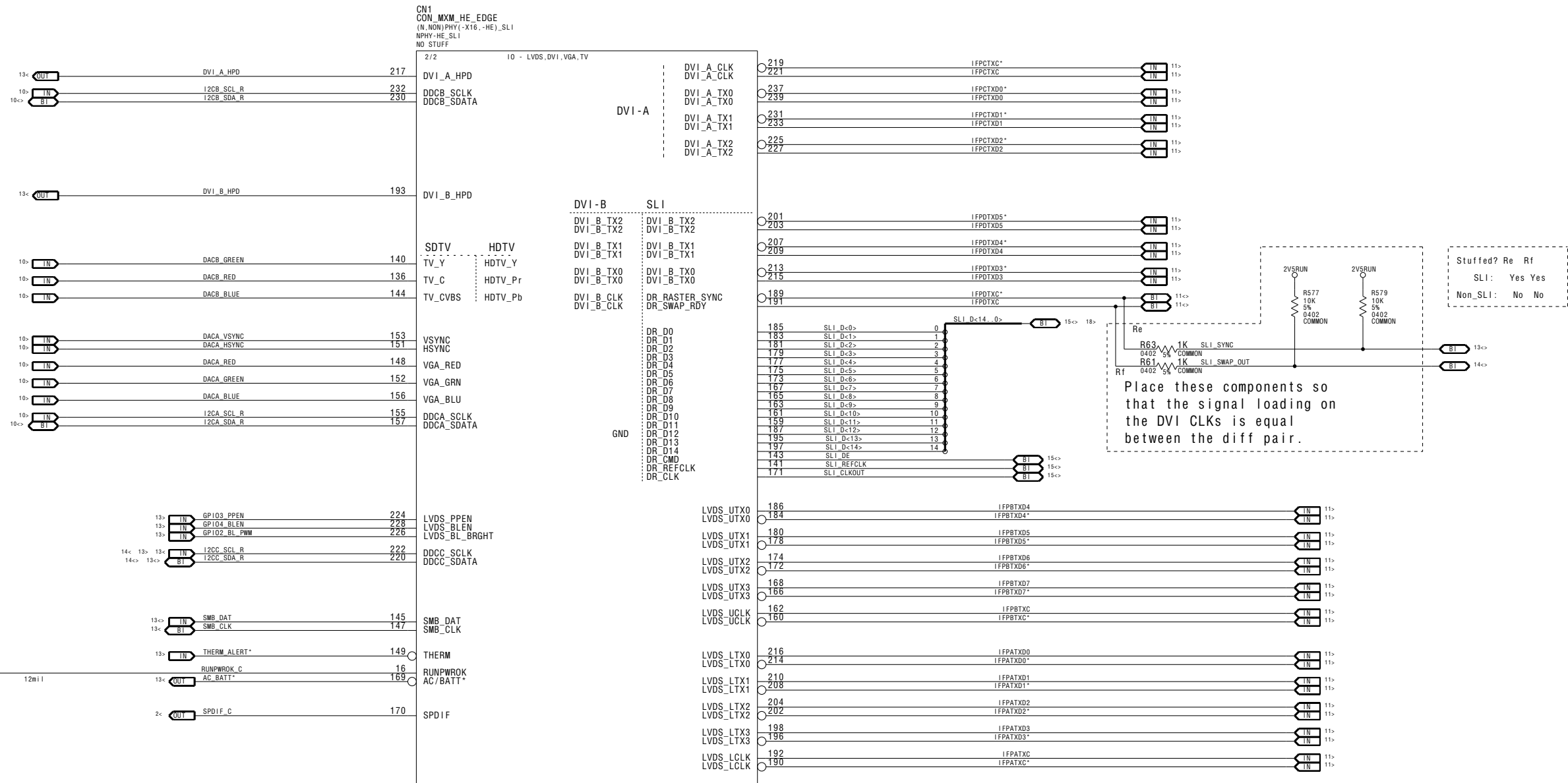
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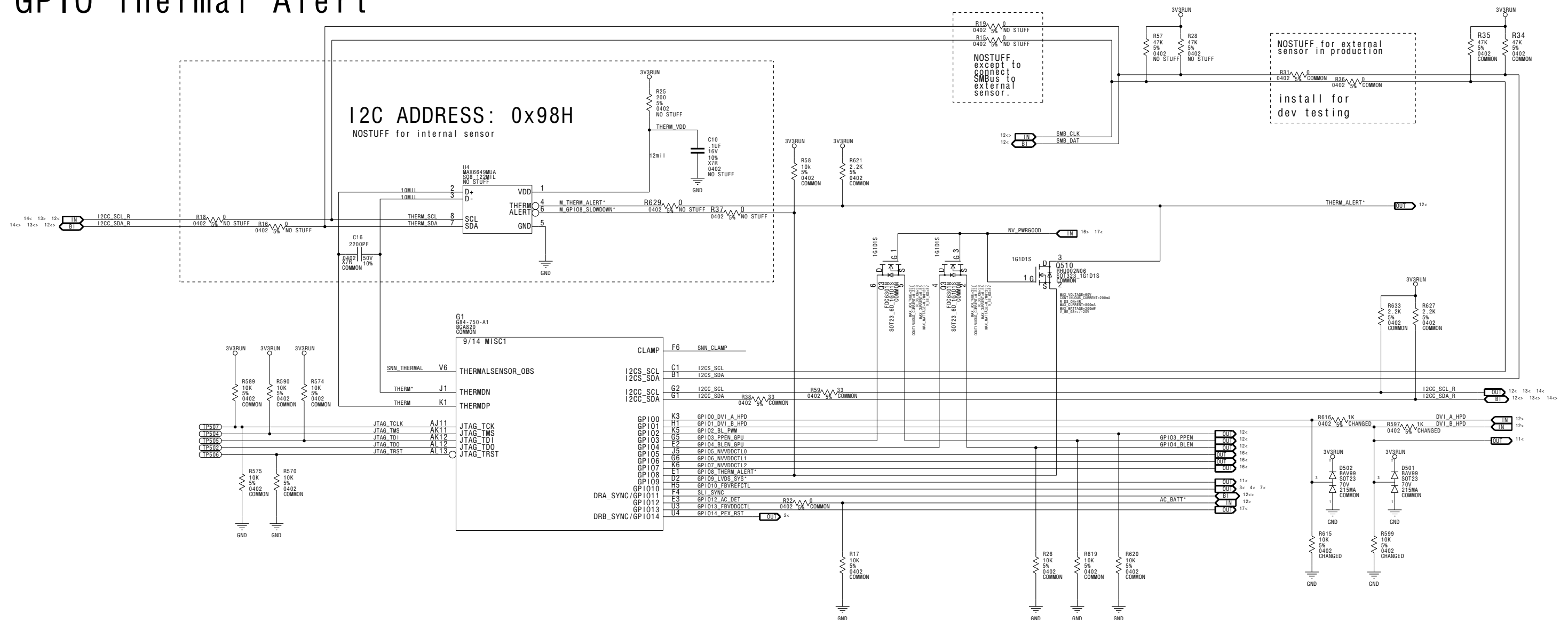
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MXM Connector IO-Section



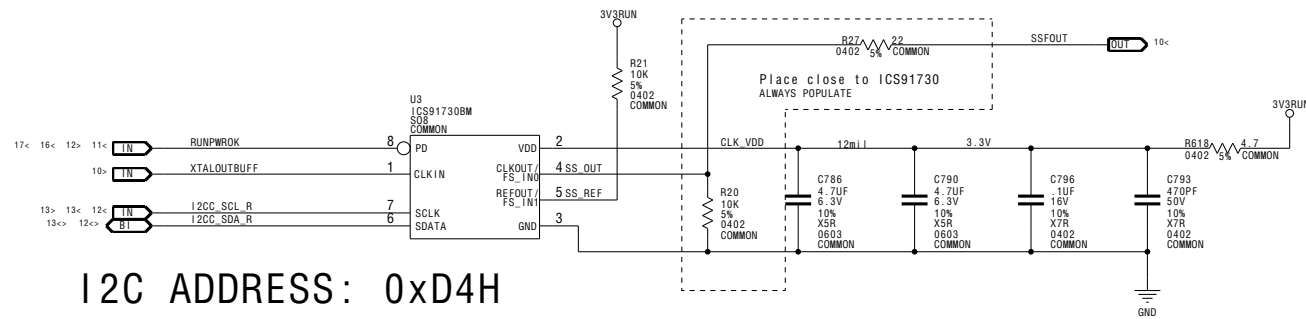
GPIO Thermal Alert



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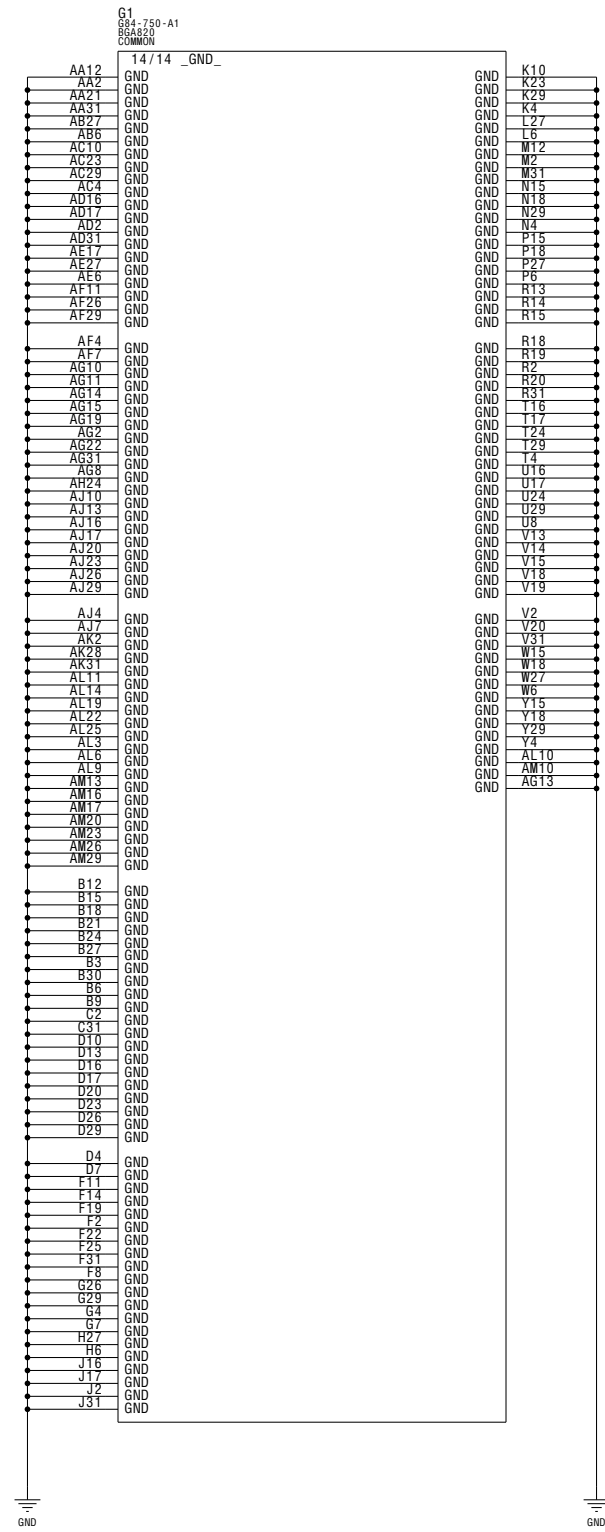
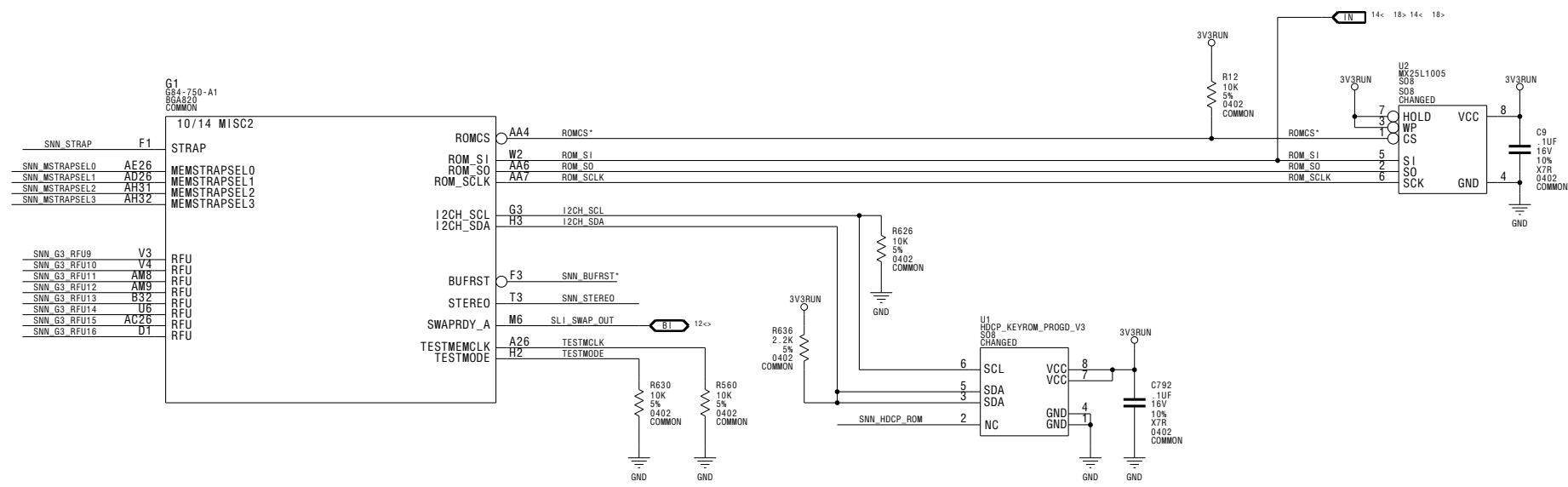
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SPREAD SPECTRUM CLOCK



I2C ADDRESS: 0xD4H

ROM Interface

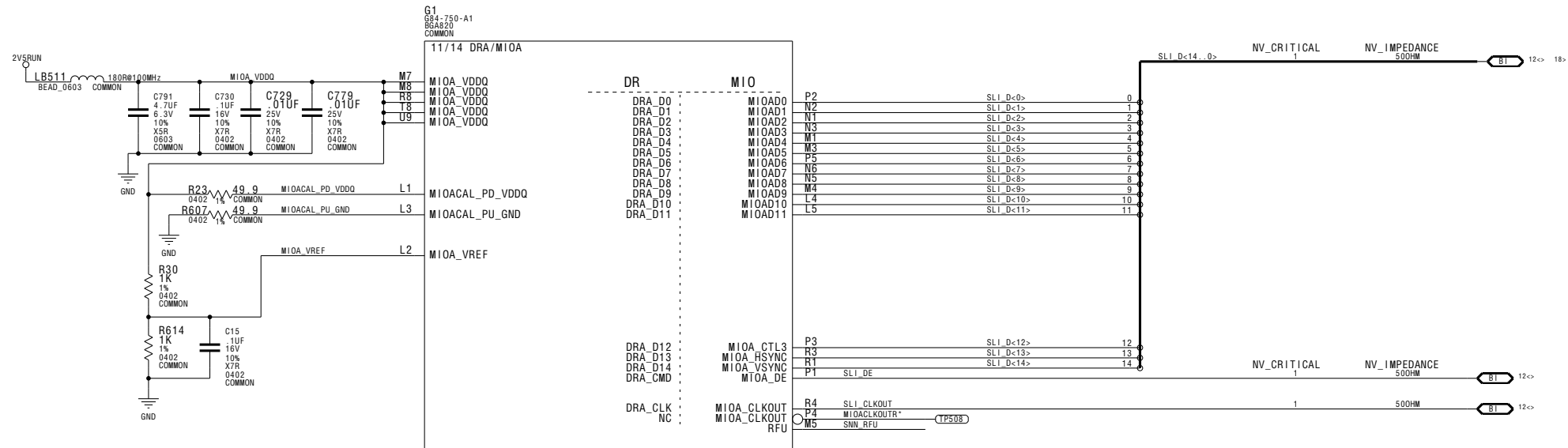


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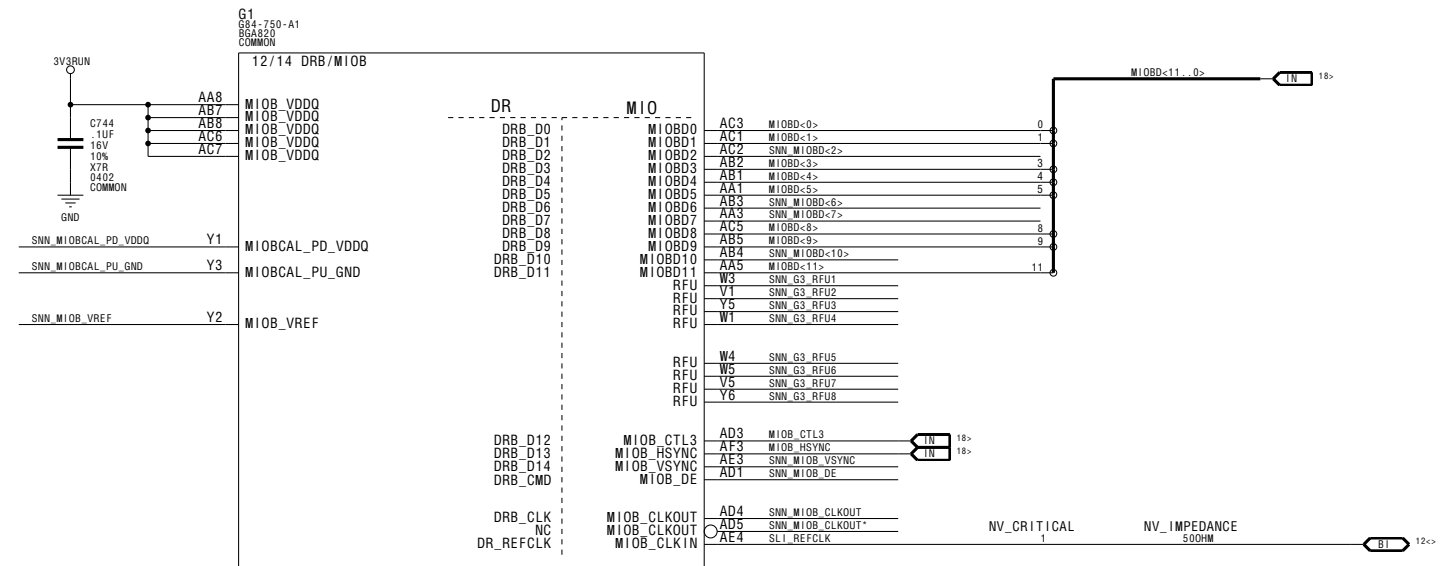
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MIOA



MIOB



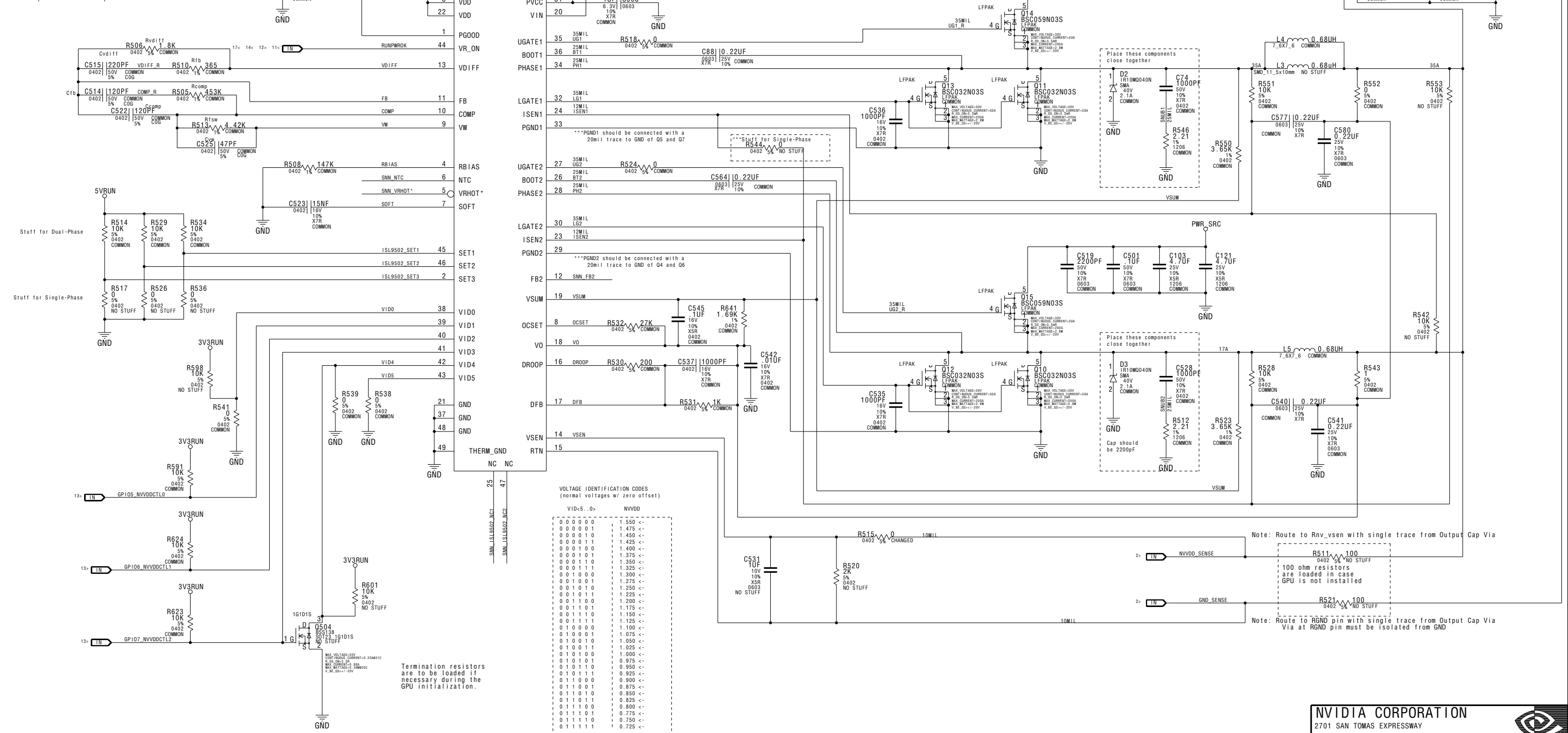
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Power Supply 1 - NVVDD

	Single-Phase	Dual-Phase
Rvdiff	1.8K	1.8K
Cvdiff	150pF	300pF
Rfb	365ohm	365ohm
Cfb	82pF	120pF
Rcomp	732K	412K
Ccomp	100pF	330pF



VOLTAGE IDENTIFICATION CODES (normal voltages w/ zero offset)

VID<5..0>	NVVDD
0 0 0 0 0	1.550
0 0 0 0 1	1.475
0 0 0 1 0	1.450
0 0 0 1 1	1.425
0 0 1 0 0	1.400
0 0 1 0 1	1.375
0 0 1 1 0	1.350
0 0 1 1 1	1.325
0 1 0 0 0	1.300
0 1 0 0 1	1.275
0 1 0 1 0	1.250
0 1 0 1 1	1.225
0 1 1 0 0	1.200
0 1 1 0 1	1.175
0 1 1 1 0	1.150
0 1 1 1 1	1.125
1 0 0 0 0	1.100
1 0 0 0 1	0.975
1 0 0 1 0	0.950
1 0 0 1 1	0.925
1 0 1 0 0	0.900
1 0 1 0 1	0.875
1 0 1 1 0	0.850
1 0 1 1 1	0.825
1 1 0 0 0	0.800
1 1 0 0 1	0.775
1 1 0 1 0	0.750
1 1 0 1 1	0.725

Termination resistors are to be loaded if necessary during the GPU initialization.

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ASSEMBLY: NVVDD Supply

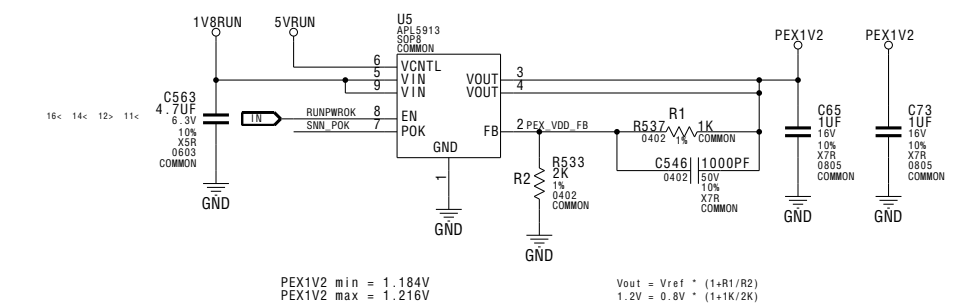
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Power Supply II - FBVDDQ, PEX_VDD, and LVDS_IOVDD

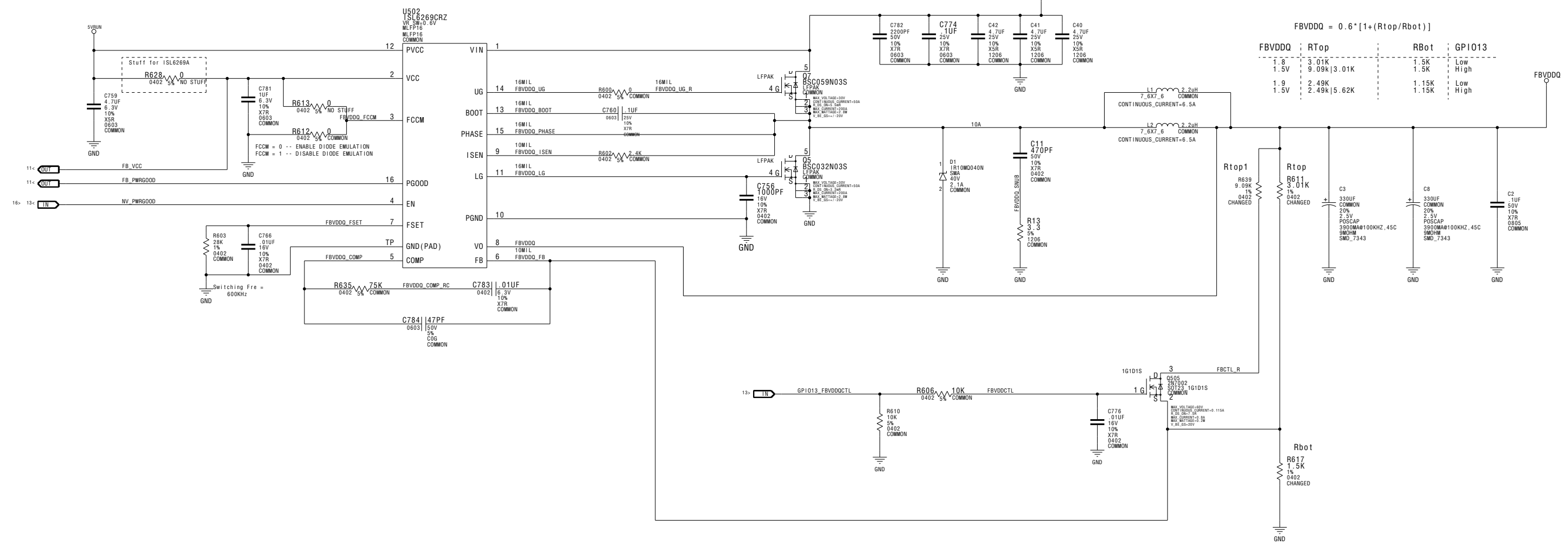
NETAtt	MIN_LINE_WIDTH	VOLTAGE
5V3RUN	16MIL	0.5A 5V
3V3RUN	16MIL	1.5A 3.3V
1V8RUN	16MIL	3.5A 1.8V
PEX1V2	16MIL	1A 1.2V
FBVDDQ	16MIL	10A 2.0V
NVDDQ	25MIL	1.25V
PWR_SRC	4A	2.2V
2V5RUN	16MIL	0.5A 2.5V
2V5RUN	16MIL	25A 0V

PEX_VDD

PEXVDD = 1.2V @ 1.8A



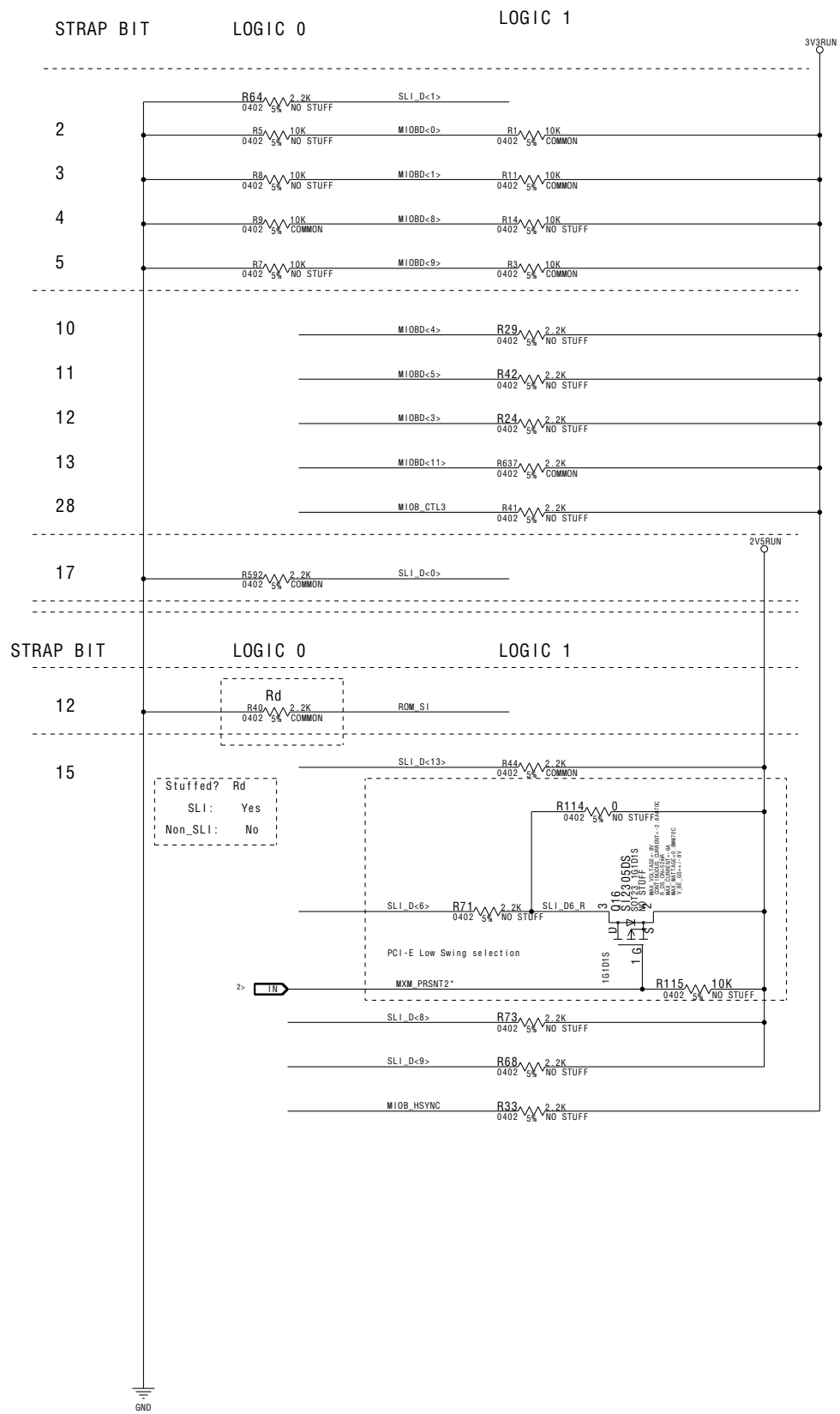
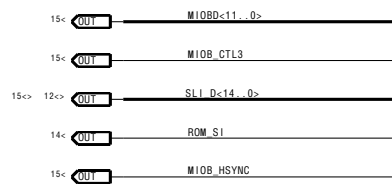
FBVDDQ



FBVDDQ	Rtop	Rbot	GPIO13
1.8	3.01K	1.5K	Low
1.5	9.09K	1.5K	High
1.9	2.49K	1.15K	Low
1.5	2.49K	1.15K	High

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REG: NV_STRAP_0

SUB_VENDOR 1 = Read from BIOS
 RAM_CFG_0 RAM_CFG[3:0]
 RAM_CFG_1 MS_1001: 16Mx32 GDDR3 SDRAM 128 Bit, Qimoda Dual Rank
 MS_1010: 16Mx32 GDDR3 SDRAM 128 Bit, Hynix Dual Rank
 RAM_CFG_2 MS_1011: 16Mx32 GDDR3 SDRAM 128 Bit, Samsung Dual Rank
 MS_0011: 16Mx32 GDDR3 SDRAM 128 Bit, Samsung Single Rank
 RAM_CFG_3 MS_0010: 16Mx32 GDDR3 SDRAM 128 Bit, Hynix Single Rank

PCI_DEVID_0 MS_00111: (G84M-600)
 MS_01000: (G84M-700)
 PCI_DEVID_1 MS_01001: (G84M-750)
 MS_01010: (G84M-610)
 PCI_DEVID_2 MS_01100: (G84GLM-950)
 MS_01101: (G84GLM-975)
 PCI_DEVID_3

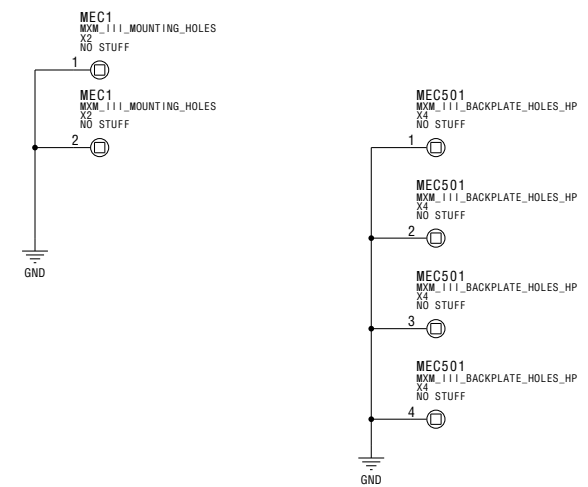
PCI_DEVID_EXT (4)

PEX_PLL_EN_TERM100

REG: NV_STRAP_1

MIOA_EN_3.3V
 Slot Clock Configuration

3G IO_PADCFG_LUT_ADR[0]
 3G IO_PADCFG_LUT_ADR[1]
 3G IO_PADCFG_LUT_ADR[2]
 3G IO_PADCFG_LUT_ADR[3]




ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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	A	B	C	D	E	F	G	H
1	RBIAS 16.2B	SNN_G3_RFU13 14.4A						
	REFCLK 2.2E	SNN_G3_RFU14 14.4A						
	REFCLK* 2.2E	SNN_G3_RFU15 14.4A						
	ROMCS* 14.3C 14.3E	SNN_G3_RFU16 14.4A						
	ROM_SCLK 14.3C 14.3E	SNN_HDCP_ROM 14.4D						
	ROM_S1 14.3E< 14.3E< 18.2A>	SNN_ISL9502_NC1 16.4C						
	18.3C	SNN_ISL9502_NC2 16.4C						
	ROM_SO 14.3C 14.3E	SNN_MIOBCAL_PD_VDD 15.4D						
	RUNPWROK 11.4A< 12.4A> 14.2A<	Q						
	16.2B< 17.1F<	SNN_MIOBCAL_PU_GND 15.4D						
	RUNPWROK_C 12.4C	SNN_MIOBD<2> 15.3F						
	SLI_CLKOUT 12.3F<> 15.2F<>	SNN_MIOBD<6> 15.4F						
	SLI_D6_R 18.4D	SNN_MIOBD<7> 15.4F						
	SLI_D<0> 12.3E 15.1D 18.3C	SNN_MIOBD<10> 15.4F						
	SLI_D<14..0> 12.3F<> 15.1F<>	SNN_MIOB_CLKOUT 15.4F						
	18.2A>	SNN_MIOB_CLKOUT* 15.4F						
	SLI_D<1> 12.3E 15.1D 18.1C	SNN_MIOB_DE 15.4F						
	SLI_D<2> 12.3E 15.1D	SNN_MIOB_VREF 15.4D						
	SLI_D<3> 12.3E 15.1D	SNN_MIOB_VSYNC 15.4F						
	SLI_D<4> 12.3E 15.1D	SNN_MSTRAPSEL0 14.3A						
	SLI_D<5> 12.3E 15.2D	SNN_MSTRAPSEL1 14.3A						
	SLI_D<6> 12.3E 15.2D 18.4C	SNN_MSTRAPSEL2 14.3A						
	SLI_D<7> 12.3E 15.2D	SNN_MSTRAPSEL3 14.4A						
	SLI_D<8> 12.3E 15.2D 18.4C	SNN_NTC 16.2B						
	SLI_D<9> 12.3E 15.2D 18.4C	SNN_POK 17.1F						
	SLI_D<10> 12.3E 15.2D	SNN_RFU 15.2D						
	SLI_D<11> 12.3E 15.2D	SNN_RFU1 2.1D						
	SLI_D<12> 12.3E 15.2D	SNN_RFU2 2.1D						
	SLI_D<13> 12.3E 15.2D 18.3C	SNN_STEREO 14.4C						
	SLI_D<14> 12.3E 15.2D	SNN_STRAP 14.3A						
	SLI_DE 12.3F<> 15.2F<>	SNN_THERMAL 13.3C						
	SLI_REFCLK 12.3F<> 15.4G<>	SNN_VRHOT* 16.3B						
	SLI_SWAP_OUT 12.3H<> 14.4C<>	SNUB1 16.2F						
	SLI_SYNC 12.3H<> 13.3G<>	SNUB2 16.4F						
	SMB_CLK 12.4C<> 13.2F<	SOFT 16.3B						
	SMB_DAT 12.4C< 13.2F<>	SPDIF 2.5F						
	SNN_BUFST* 14.4C	SPDIF_C 2.5H< 12.4C>						
	SNN_CLAMP 13.3D	SSFOUT 10.4B< 14.1D>						
	SNN_DACB_CSYNC 10.2D	SS_OUT 14.2C						
	SNN_DACC_BLUE 10.4D	SS_REF 14.2C						
	SNN_DACC_GREEN 10.3D	TESTCLK 14.4C						
	SNN_DACC_RED 10.3D	TESTMODE 14.4C						
	SNN_DACC_RSET 10.3C	THERM 13.3C						
	SNN_DACC_VREF 10.3C	THERM* 13.3C						
	SNN_FB2 16.3C	THERM_ALERT* 12.4C< 13.2H>						
	SNN_FBA0_NC1 4.2B	THERM_SCL 13.2C						
	SNN_FBA0_NC2 5.2B	THERM_SDA 13.2C						
	SNN_FBA0_NC3 5.2B	THERM_VDD 13.1D						
	SNN_FBA1_NC1 4.2E	TMDSIOVDD_AB_EN* 11.2B						
	SNN_FBA1_NC2 5.2E	TMDSIOVDD_C 11.4C						
	SNN_FBA1_NC3 5.2E	TMDSIOVDD_C_EN* 11.4B						
	SNN_FBA_CMD14 3.3E	TMDSIOVDD_D 11.5C						
	SNN_FBA_CMD26 3.3E	TMDSIOVDD_D_EN 11.5C						
	SNN_FBA_CMD28 3.4E	TMDSIOVDD_D_EN* 11.5B						
	SNN_FBA_NC1_D31 3.4E	TMDS_LVDS_IOVDD 11.2B						
	SNN_FBA_NC2_D32 3.4E	UG1 16.2C						
	SNN_FBC0_NC1 7.2B	UG1_R 16.2E						
	SNN_FBC0_NC2 8.2B	UG2 16.2C						
	SNN_FBC0_NC3 8.2B	UG2_R 16.3E						
	SNN_FBC1_NC1 7.2E	VDIFF 16.2B						
	SNN_FBC1_NC2 8.2E	VDIFF_R 16.2A						
	SNN_FBC1_NC3 8.2E	VID0 16.3B						
	SNN_FBC_CMD14 6.3E	VID4 16.3B						
	SNN_FBC_CMD26 6.3E	VID5 16.3B						
	SNN_FBC_CMD28 6.3E	VO 16.3C						
	SNN_FBC_PLLVDD 6.4E	VSEN 16.4C						
	SNN_FBVTT_AA23 6.1E	VSUM 16.3C 16.3F 16.4G						
	SNN_FBVTT_AB23 6.1E	VW 16.2B						
	SNN_FBVTT_H16 6.1E	XTALIN 10.5C						
	SNN_FBVTT_H17 6.1E	XTALOUT 10.5D						
	SNN_FBVTT_J9 6.1E	XTALOUTBUFF 10.4F> 14.2A<						
	SNN_FBVTT_J10 6.1E							
	SNN_FBVTT_J23 6.1E							
	SNN_FBVTT_J24 6.1E							
	SNN_FBVTT_K9 6.1E							
	SNN_FBVTT_K11 6.1E							
	SNN_FBVTT_K12 6.1E							
	SNN_FBVTT_K21 6.1E							
	SNN_FBVTT_K22 6.1E							
	SNN_FBVTT_K24 6.1E							
	SNN_FBVTT_L23 6.1E							
	SNN_FBVTT_M23 6.1E							
	SNN_FBVTT_T25 6.1E							
	SNN_FBVTT_U25 6.1E							
	SNN_G3_RFU1 15.4F							
	SNN_G3_RFU2 15.4F							
	SNN_G3_RFU3 15.4F							
	SNN_G3_RFU4 15.4F							
	SNN_G3_RFU5 15.4F							
	SNN_G3_RFU6 15.4F							
	SNN_G3_RFU7 15.4F							
	SNN_G3_RFU8 15.4F							
	SNN_G3_RFU9 14.4A							
	SNN_G3_RFU10 14.4A							
	SNN_G3_RFU11 14.4A							
	SNN_G3_RFU12 14.4A							
2								
3								
4								
5								

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