

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
D		263	PRODUCTION RELEASE	02/25/03	02/25/03

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Q26C MLB GEN X REV A (DVT)



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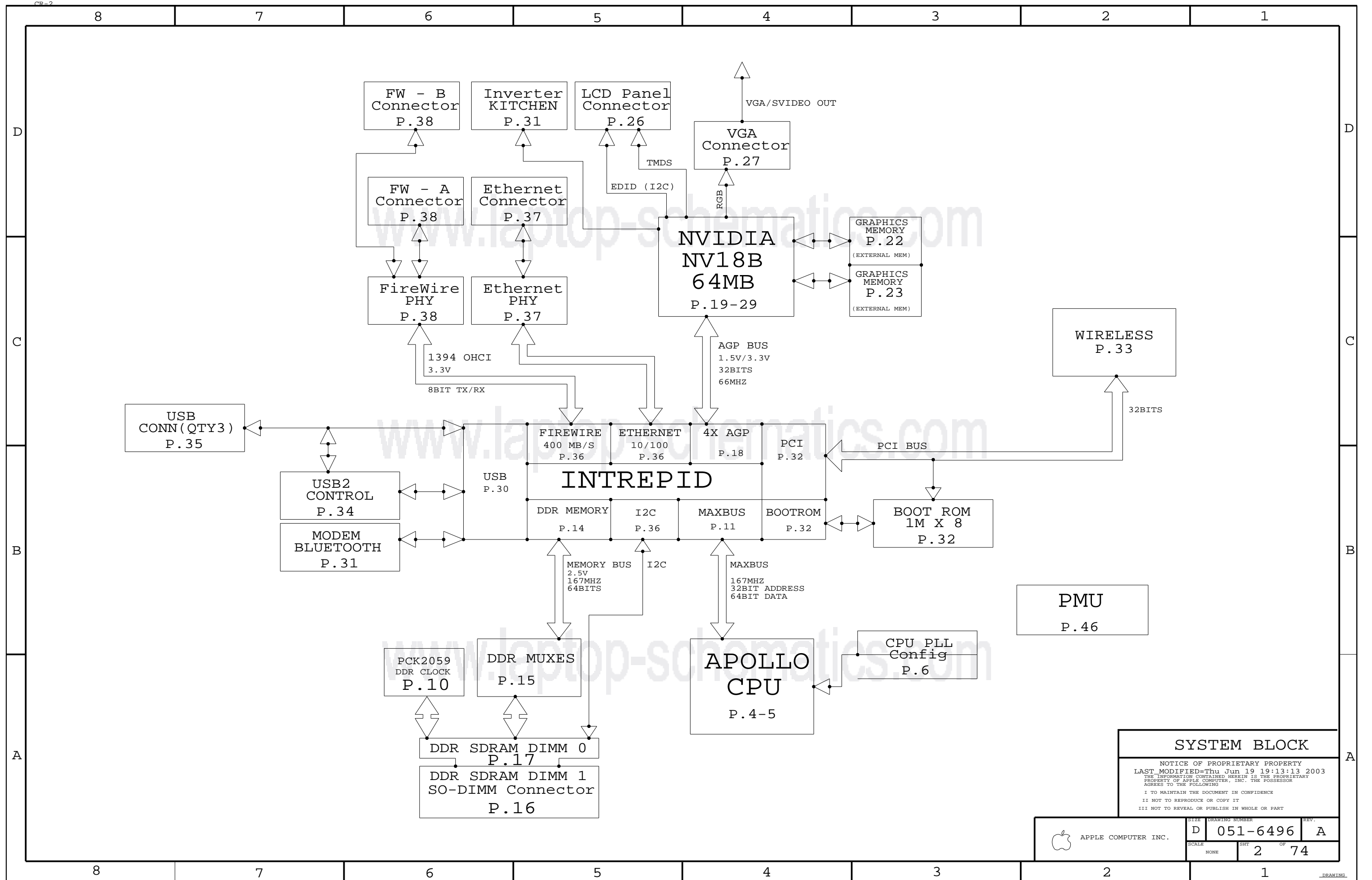
POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+2_5V_MAIN	ON	ON	OFF
+3V_MAIN	ON	ON	OFF
+5V_MAIN	ON	ON	OFF
+5V_SLEEP	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12V_SLEEP	ON	OFF	OFF
FW_PWR	ON	ON	OFF
+1.8V_SLEEP	ON	OFF	OFF
+MAXBUS_SLEEP	ON	OFF	OFF

SCHEMATIC AND PCB SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6496	1	SCHEM,MLB,Q26C,GENX	SCH1	CRITICAL	
820-1501	1	PCB,MLB,IMACG4	PCB1	CRITICAL	
825-2029	1	LBL,SER #,BARCODE	PCB1		
056-1158	1	DESIGN GUIDE,MCO,IMACG4	PCB1	CRITICAL	
057-0040	1	DFM,PNLZN DWG,MLB,Q26	PCB1	CRITICAL	
630-4766	1	630-4766,PCBA,H,Q26C,EEE PVL	HYNIX		OMIT
630-4767	1	630-4767,PCBA,S,Q26C,EEE PVM	SAMSUNG		OMIT

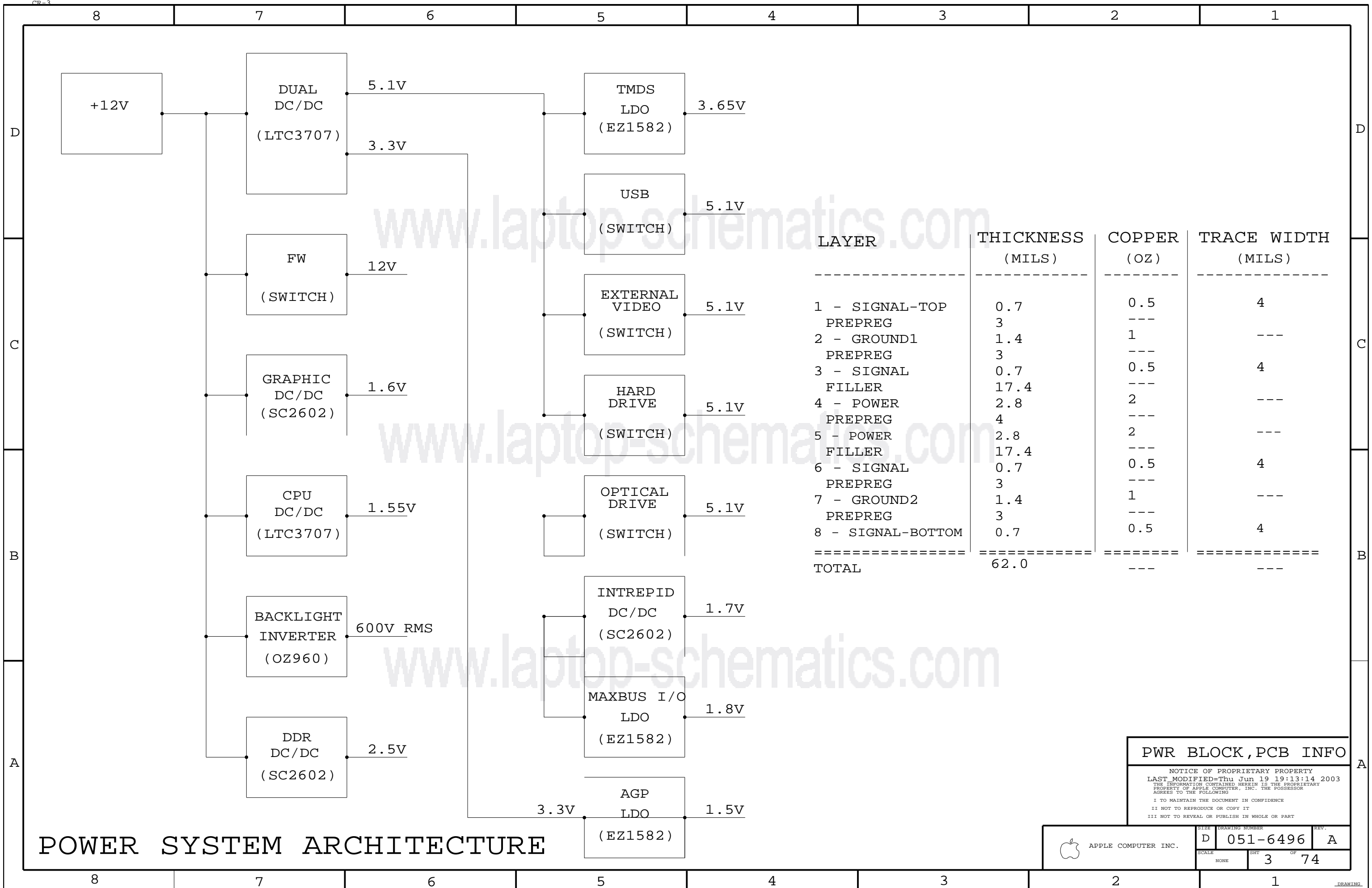
<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>xx: _____</p> <p>x.xx: _____</p> <p>x.xxx: _____</p> <p>ANGLES: _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <p style="text-align: center;"></p> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p>	<p>METRIC</p>	 Apple Computer Inc.
<p style="font-size: x-small;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>		<p>TITLE</p> <p style="font-size: large;">SCHEM,MLB,Q26,GEN X</p>
<p style="font-size: x-small;">MATERIAL/FINISH NOTED AS APPLICABLE</p> <p style="text-align: center;">D</p>		<p>DRAWING NUMBER</p> <p style="font-size: large;">051-6496</p> <p style="font-size: x-small;">REV. A</p> <p style="font-size: x-small;">SHT 1 OF 74</p>



SYSTEM BLOCK

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	NONE	051-6496	A
SCALE		SHT	OF
NONE		2	74



LAYER	THICKNESS (MILS)	COPPER (OZ)	TRACE WIDTH (MILS)
1 - SIGNAL-TOP	0.7	0.5	4
PREPREG	3	---	---
2 - GROUND1	1.4	1	---
PREPREG	3	---	---
3 - SIGNAL	0.7	0.5	4
FILLER	17.4	---	---
4 - POWER	2.8	2	---
PREPREG	4	---	---
5 - POWER	2.8	2	---
FILLER	17.4	---	---
6 - SIGNAL	0.7	0.5	4
PREPREG	3	---	---
7 - GROUND2	1.4	1	---
PREPREG	3	---	---
8 - SIGNAL-BOTTOM	0.7	0.5	4
=====	=====	=====	=====
TOTAL	62.0	---	---

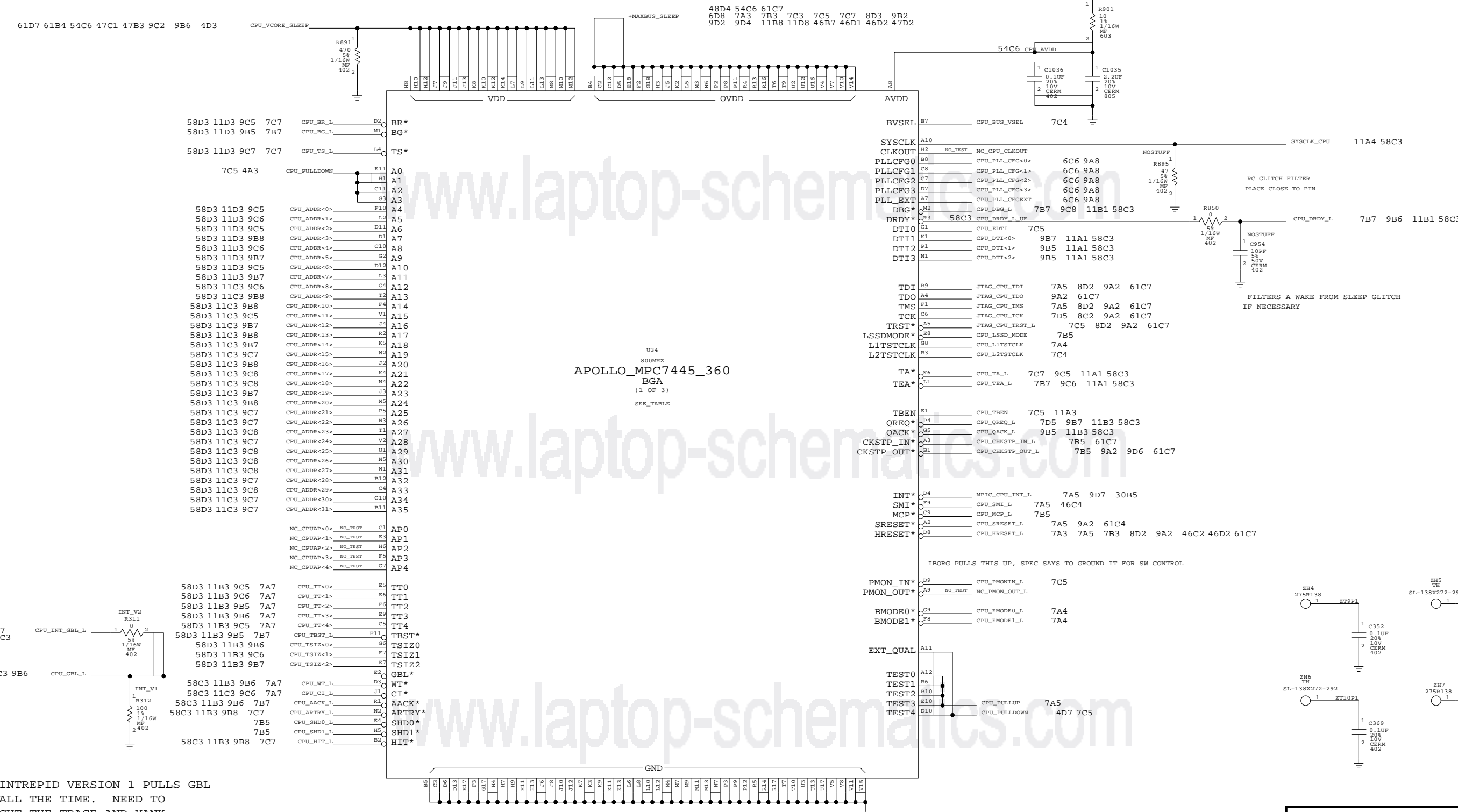
POWER SYSTEM ARCHITECTURE

PWR BLOCK, PCB INFO

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	SIZE: D DRAWING NUMBER: 051-6496 REV.: A
	SCALE: NONE SHT: 3 OF 74

CPU INTERNAL PLL FILTERING



U34
800MHZ
APOLLO_MPC7445_360
BGA
(1 OF 3)
SEE_TABLE

INTREPID VERSION 1 PULLS GBL
ALL THE TIME. NEED TO
CUT THE TRACE AND YANK
DOWN HARD FOR SNOOPING.
FIXED IN INTREPID VERSION 2.

CPU MECHANICAL PARTS SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
875-1475	1	PAD, THERMAL, CPU, U34	U341	CRITICAL	
870-1113	1	HEAT SINK, CPU, Q26, U34	U342	CRITICAL	DEV
870-1114	1	CLIP, HEAT SINK, CPU, Q26, U34	U343	CRITICAL	DEV
412-0042	1	SCREW, MACH, 3MM W, 8MM L, U34	U344	CRITICAL	DEV
835-0251	1	NUT, 3MM, U34	U345	CRITICAL	DEV

ALTERNATE APOLLO6 1.0 GHZ (SICOH VS. FTEOS)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S2783	337S2782		U34	ALT PART FOR SICOH

MPC7450 MAXBUS

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APPLE COMPUTER INC. **D** 051-6496 **A**

SCALE NONE SHT 4 OF 74

APOLLO_MPC7445_360

NC_CPUCRUD<0> NO_TEST F18 NC_F18
 NC_CPUCRUD<1> NO_TEST F17 NC_F17
 NC_CPUCRUD<2> NO_TEST F19 NC_F19
 NC_CPUCRUD<3> NO_TEST H19 NC_H19
 NC_CPUCRUD<4> NO_TEST H18 NC_H18
 NC_CPUCRUD<5> NO_TEST H17 NC_H17
 NC_CPUCRUD<6> NO_TEST H16 NC_H16
 NC_CPUCRUD<7> NO_TEST E19 NC_E19
 NC_CPUCRUD<8> NO_TEST D18 NC_D18
 NC_CPUCRUD<9> NO_TEST F16 NC_F16
 NC_CPUCRUD<10> NO_TEST G16 NC_G16
 NC_CPUCRUD<11> NO_TEST D19 NC_D19
 NC_CPUCRUD<12> NO_TEST F15 NC_F15
 NC_CPUCRUD<13> NO_TEST G19 NC_G19
 NC_CPUCRUD<14> NO_TEST E16 NC_E16
 NC_CPUCRUD<15> NO_TEST D17 NC_D17
 NC_CPUCRUD<16> NO_TEST D16 NC_D16

U34
 800MHZ
 BGA
 (3 OF 3)

NC_CPUCRUD<17> NO_TEST P15 NC_P15
 NC_CPUCRUD<18> NO_TEST L15 NC_L15
 NC_CPUCRUD<19> NO_TEST N15 NC_N15
 NC_CPUCRUD<20> NO_TEST P18 NC_P18
 NC_CPUCRUD<21> NO_TEST N14 NC_N14
 NC_CPUCRUD<22> NO_TEST M14 NC_M14
 NC_CPUCRUD<23> NO_TEST M17 NC_M17
 NC_CPUCRUD<24> NO_TEST N13 NC_N13
 NC_CPUCRUD<25> NO_TEST N16 NC_N16
 NC_CPUCRUD<26> NO_TEST M19 NC_M19
 NC_CPUCRUD<27> NO_TEST M16 NC_M16
 NC_CPUCRUD<28> NO_TEST P19 NC_P19
 NC_CPUCRUD<29> NO_TEST N17 NC_N17
 NC_CPUCRUD<30> NO_TEST M15 NC_M15
 NC_CPUCRUD<31> NO_TEST L17 NC_L17
 NC_CPUCRUD<32> NO_TEST L14 NC_L14
 NC_CPUCRUD<33> NO_TEST K15 NC_K15
 NC_CPUCRUD<34> NO_TEST J14 NC_J14
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 NC_CPUCRUD<36> NO_TEST J19 NC_J19
 NC_CPUCRUD<37> NO_TEST J15 NC_J15
 NC_CPUCRUD<38> NO_TEST K19 NC_K19
 NC_CPUCRUD<39> NO_TEST J16 NC_J16
 NC_CPUCRUD<40> NO_TEST H15 NC_H15
 NC_CPUCRUD<41> NO_TEST L16 NC_L16
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 NC_CPUCRUD<43> NO_TEST M18 NC_M18
 NC_CPUCRUD<44> NO_TEST L19 NC_L19
 NC_CPUCRUD<45> NO_TEST L18 NC_L18
 NC_CPUCRUD<46> NO_TEST K18 NC_K18
 NC_CPUCRUD<47> NO_TEST J17 NC_J17
 NC_CPUCRUD<48> NO_TEST K16 NC_K16
 NC_CPUCRUD<49> NO_TEST C19 NC_C19
 NC_CPUCRUD<50> NO_TEST D15 NC_D15
 NC_CPUCRUD<51> NO_TEST G15 NC_G15
 NC_CPUCRUD<52> NO_TEST C18 NC_C18
 NC_CPUCRUD<53> NO_TEST A16 NC_A16
 NC_CPUCRUD<54> NO_TEST B19 NC_B19
 NC_CPUCRUD<55> NO_TEST A19 NC_A19
 NC_CPUCRUD<56> NO_TEST D14 NC_D14
 NC_CPUCRUD<57> NO_TEST E15 NC_E15
 NC_CPUCRUD<58> NO_TEST B15 NC_B15
 NC_CPUCRUD<59> NO_TEST B17 NC_B17
 NC_CPUCRUD<60> NO_TEST C17 NC_C17
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 NC_CPUCRUD<63> NO_TEST E14 NC_E14
 NC_CPUCRUD<64> NO_TEST H14 NC_H14
 NC_CPUCRUD<65> NO_TEST G14 NC_G14
 NC_CPUCRUD<66> NO_TEST C15 NC_C15
 NC_CPUCRUD<67> NO_TEST A17 NC_A17
 NC_CPUCRUD<68> NO_TEST G12 NC_G12
 NC_CPUCRUD<69> NO_TEST F14 NC_F14
 NC_CPUCRUD<70> NO_TEST F13 NC_F13
 NC_CPUCRUD<71> NO_TEST E13 NC_E13
 NC_CPUCRUD<72> NO_TEST B16 NC_B16
 NC_CPUCRUD<73> NO_TEST A15 NC_A15
 NC_CPUCRUD<74> NO_TEST C14 NC_C14
 NC_CPUCRUD<75> NO_TEST A18 NC_A18
 NC_CPUCRUD<76> NO_TEST A13 NC_A13
 NC_CPUCRUD<77> NO_TEST F12 NC_F12
 NC_CPUCRUD<78> NO_TEST A14 NC_A14
 NC_CPUCRUD<79> NO_TEST G11 NC_G11
 NC_CPUCRUD<80> NO_TEST C13 NC_C13

NC_CPUCRUD<81> NO_TEST N12 NC_N12
 NC_CPUCRUD<82> NO_TEST N18 NC_N18
 NC_CPUCRUD<83> NO_TEST K17 NC_K17
 NC_CPUCRUD<84> NO_TEST N19 NC_N19
 NC_CPUCRUD<85> NO_TEST B18 NC_B18
 NC_CPUCRUD<86> NO_TEST E12 NC_E12
 NC_CPUCRUD<87> NO_TEST B13 NC_B13
 NC_CPUCRUD<88> NO_TEST B14 NC_B14
 NC_CPUCRUD<89> NO_TEST A6 NC_A6

APOLLO_MPC7445_360

U34
 800MHZ
 BGA
 (2 OF 3)

58D3 11D1 9C5 CPU_DATA<0> R15 D0
 58D3 11D1 9C7 CPU_DATA<1> M15 D1
 58D3 11D1 9C8 CPU_DATA<2> T14 D2
 58D3 11D1 9C6 CPU_DATA<3> V16 D3
 58D3 11D1 9C7 CPU_DATA<4> M16 D4
 58D3 11D1 9C8 CPU_DATA<5> T15 D5
 58D3 11D1 9C5 CPU_DATA<6> U15 D6
 58D3 11D1 9C8 CPU_DATA<7> P14 D7
 58D3 11D1 9D6 CPU_DATA<8> V13 D8
 58D3 11D1 9D5 CPU_DATA<9> M13 D9
 58D3 11D1 9C7 CPU_DATA<10> T13 D10
 58D3 11D1 9C6 CPU_DATA<11> P13 D11
 58D3 11D1 9C6 CPU_DATA<12> U14 D12
 58D3 11D1 9C7 CPU_DATA<13> M14 D13
 58D3 11D1 9C8 CPU_DATA<14> R12 D14
 58D3 11C1 9D6 CPU_DATA<15> T12 D15
 58D3 11C1 9C5 CPU_DATA<16> M12 D16
 58D3 11C1 9D7 CPU_DATA<17> V12 D17
 58D3 11C1 9C5 CPU_DATA<18> N11 D18
 58D3 11C1 9D5 CPU_DATA<19> N10 D19
 58D3 11C1 9D5 CPU_DATA<20> R11 D20
 58D3 11C1 9D8 CPU_DATA<21> U11 D21
 58D3 11C1 9D7 CPU_DATA<22> M11 D22
 58D3 11C1 9D8 CPU_DATA<23> T11 D23
 58D3 11C1 9D5 CPU_DATA<24> R10 D24
 58D3 11C1 9D7 CPU_DATA<25> N9 D25
 58D3 11C1 9D6 CPU_DATA<26> P10 D26
 58D3 11C1 9D7 CPU_DATA<27> U10 D27
 58D3 11C1 9D8 CPU_DATA<28> R9 D28
 58D3 11C1 9D8 CPU_DATA<29> M10 D29
 58D3 11C1 9D6 CPU_DATA<30> U9 D30
 58D3 11C1 9D7 CPU_DATA<31> V9 D31
 58D3 11D8 11C1 9D7 CPU_DATA<32> M5 D32
 58D3 11D8 11C1 9D8 CPU_DATA<33> U6 D33
 58D3 11D8 11C1 9D8 CPU_DATA<34> T5 D34
 58D3 11D8 11C1 9D7 CPU_DATA<35> U5 D35
 58D3 11D8 11C1 9D5 CPU_DATA<36> M7 D36
 58D3 11C1 9D6 CPU_DATA<37> E6 D37
 58D3 11C1 9D6 CPU_DATA<38> P7 D38
 58D3 11C1 9D6 CPU_DATA<39> V6 D39
 58D3 11D5 11C1 9D7 CPU_DATA<40> P17 D40
 58D3 11D5 11B1 9D5 CPU_DATA<41> R19 D41
 58D3 11D5 11B1 9C6 CPU_DATA<42> V18 D42
 58D3 11D5 11B1 9C5 CPU_DATA<43> R18 D43
 58D3 11D5 11B1 9C8 CPU_DATA<44> V19 D44
 58D3 11C5 11B1 9C7 CPU_DATA<45> T19 D45
 58D3 11C5 11B1 9C5 CPU_DATA<46> U19 D46
 58D3 11C5 11B1 9C7 CPU_DATA<47> M19 D47
 58D3 11B8 11B1 9C6 CPU_DATA<48> U18 D48
 58D3 11B8 11B1 9C5 CPU_DATA<49> M17 D49
 58D3 11B8 11B1 9C8 CPU_DATA<50> M18 D50
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 58D3 11B8 11B1 9C6 CPU_DATA<52> T18 D52
 58D3 11B8 11B1 9C7 CPU_DATA<53> T17 D53
 58D3 11B8 11B1 9D7 CPU_DATA<54> M3 D54
 58D3 11B8 11B1 9C6 CPU_DATA<55> V17 D55
 58D3 11B1 9D8 CPU_DATA<56> U4 D56
 58D3 11B5 11B1 9D6 CPU_DATA<57> U8 D57
 58D3 11B5 11B1 9D5 CPU_DATA<58> U7 D58
 58D3 11B5 11B1 9D8 CPU_DATA<59> K7 D59
 58D3 11B5 11B1 9D8 CPU_DATA<60> P6 D60
 58D3 11B5 11B1 9D5 CPU_DATA<61> R8 D61
 58D3 11B5 11B1 9D5 CPU_DATA<62> M8 D62
 58D3 11B5 11B1 9D6 CPU_DATA<63> T8 D63

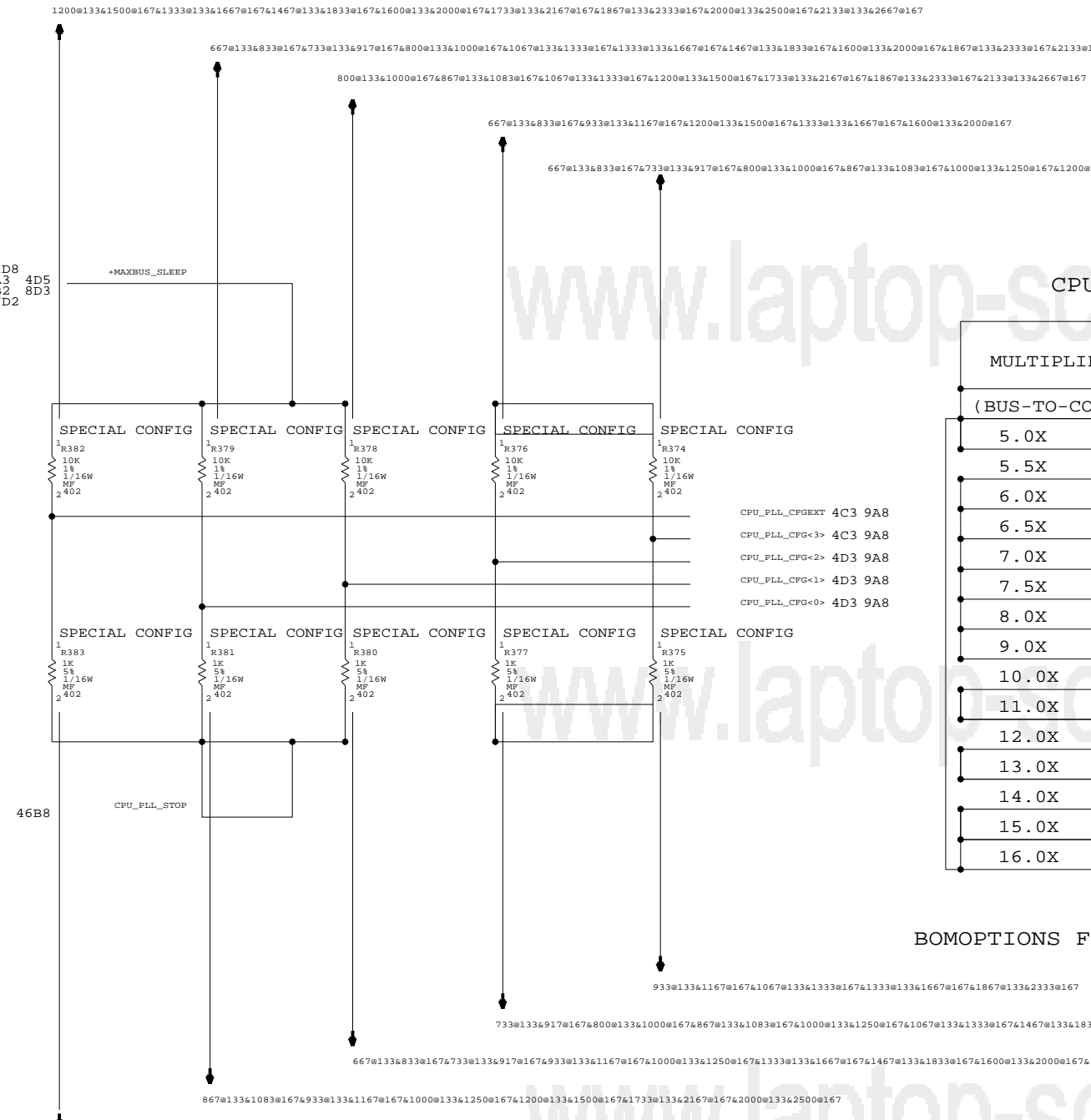
NC_CPUDP<0> NO_TEST T3 DP0
 NC_CPUDP<1> NO_TEST M4 DP1
 NC_CPUDP<2> NO_TEST T4 DP2
 NC_CPUDP<3> NO_TEST M9 DP3
 NC_CPUDP<4> NO_TEST M6 DP4
 NC_CPUDP<5> NO_TEST V3 DP5
 NC_CPUDP<6> NO_TEST N8 DP6
 NC_CPUDP<7> NO_TEST M6 DP7

MPC7450 - 2

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	D	051-6496	A
SCALE	NONE	SHT	5 OF 74

BOMOPTIONS FOR UPPER-SET OF RESISTORS



CPU FREQUENCY CONFIGURATION (SUPPORTED CPU & BUS SPEEDS)

MULTIPLIER (BUS-TO-CORE)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG
	167MHZ	133MHZ	
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
9.0X	1500	1200	1 0111 17
10.0X	1667	1333	1 1010 1A
11.0X	1833	1467	1 1001 19
12.0X	2000	1600	1 1011 1B
13.0X	2167	1733	1 0101 15
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D

CPU FREQUENCY CONFIGURATION (OTHER POSSIBLE CPU & BUS SPEEDS)

MULTIPLIER (BUS-TO-CORE)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG
	167MHZ	133MHZ	
0.0X	PLL OFF		0 1111 0F
1.0X (11.5X)	167 (1917)	133 (1533)	0 0000 00
PLL BYPASS	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
2.5X (8.5X)	417 (1417)	333 (1133)	0 0110 06
3.0X	500	400	0 1000 08
3.5X (13.5X)	583 (2250)	467 (1800)	0 1110 0E
4.0X	667	533	0 1010 0A
4.5X (9.5X)	750 (1583)	600 (1267)	0 0111 07
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
10.5X	1750	1400	1 1000 18
28.0X	4667	3733	1 1110 1E
12.5X	2083	1667	1 1111 1F

BOMOPTIONS FOR LOWER-SET OF RESISTORS

CPU SPEED & BUS RATIO SUPPORT

THE CONFIGURATION RESISTORS BELOW ARE SELF CONFIGURING WHEN THE ENGINEER SELECTS THE APPROPRIATE CPU AND BUS SPEED BOM OPTION, THE APPROPRIATE RESISTORS ARE AUTOMATICALLY SELECTED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S2674	1	IC, APOLLO, N5, V3.3, 1.0GHZ	U34		1000@133
116S1473	2	RES, 4.7K-OHM, 5%, 1/16W, 0402	R887, R368		1000@133
114S1004	1	RES, 10K-OHM, 1%, 1/16W, 0402	R866		1000@133
337S2769	1	IC, APOLLO6, N5, V3.3, 1.250GHZ	U34		1250@167
116S1473	3	RES, 4.7K-OHM, 5%, 1/16W, 0402	R887, R368, R357		1250@167
337S2782	1	IC, APOLLO6, N5, V3.3, 1.0GHZ	U34		1000@167
116S1473	3	RES, 4.7K-OHM, 5%, 1/16W, 0402	R887, R368, R357		1000@167

CPU BUS RATIO BITS

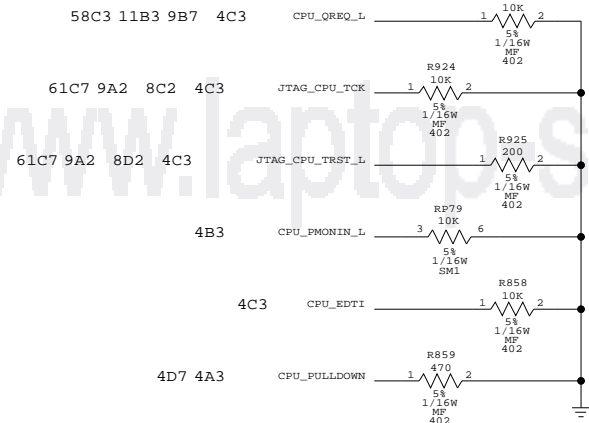
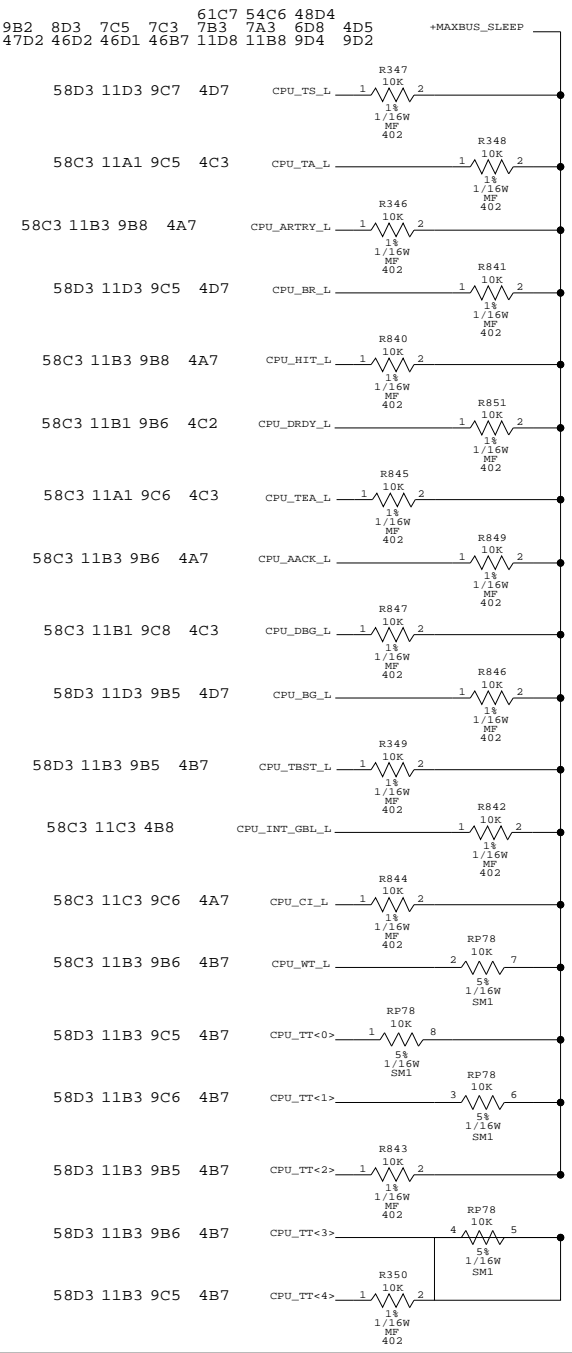
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 SCALE NONE SHT 6 OF 74

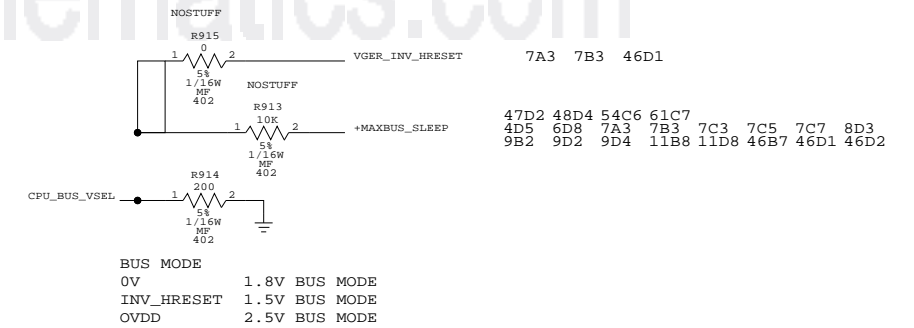
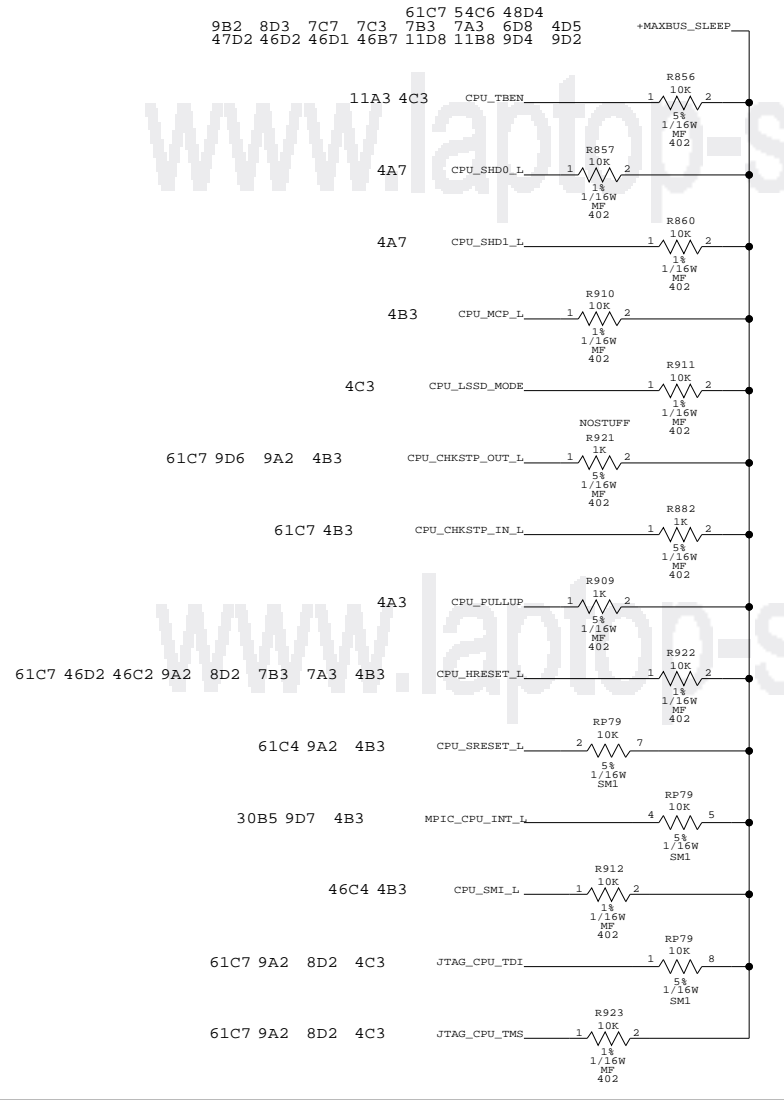
BMODE <0> <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L L	1 1	???	01	yes unavail
L !hr	1 0	Max	01	yes unavail
L hr	1 1	???	00	yes unavail
L H	1 0	Max	00	yes unavail
!hr L	0 1	MB+	01	yes unavail
!hr !hr	0 0	60x	01	yes unavail
!hr hr	0 1	MB+	00	yes unavail
!hr H	0 0	60x	00	yes unavail
hr L	1 1	???	01	norm unavail
hr !hr	1 0	Max	01	norm
hr hr	1 1	???	00	norm unavail
HR H	1 0	MAX	00	NORM <- DEFAULT
H L	0 1	MB+	01	norm unavail
H !hr	0 0	60x	01	norm
H hr	0 1	MB+	00	norm unavail
H H	0 0	60x	00	norm

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L	HIGH	60X BUS MODE
CPU_BUS_VSEL	CPU_HRESET_L	MAX BUS MODE
	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE
CPU_L3_VSEL	CPU_HRESET_L or L3_OVDD	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE

MAXBUS PULL-UPS



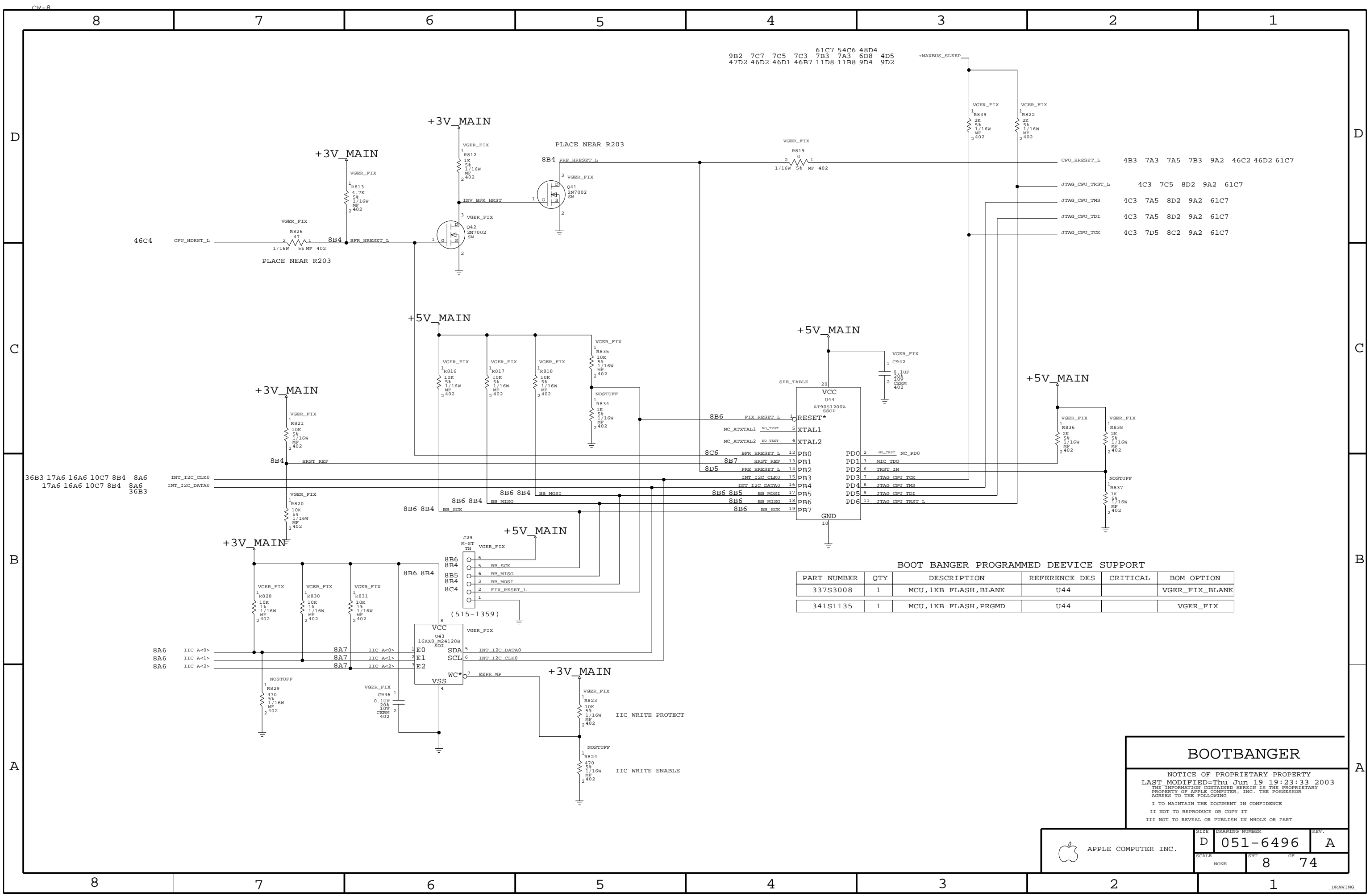
MPC7450 PULL-UPS



CPU CONFIG OPTIONS

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	NONE	051-6496	A
SCALE		SHT	OF
		7	74



BOOT BANGER PROGRAMMED DEEVICE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3008	1	MCU, 1KB FLASH, BLANK	U44		VGER_FIX_BLANK
341S1135	1	MCU, 1KB FLASH, PRGMD	U44		VGER_FIX

BOOTBANGER

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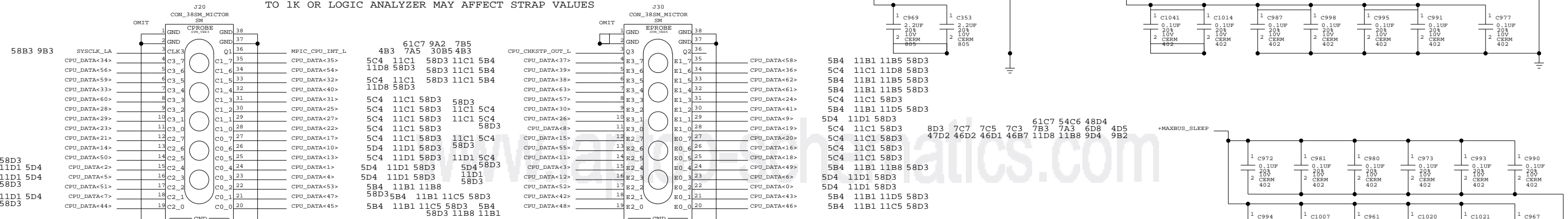
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	SCALE NONE	SHT 8	OF 74

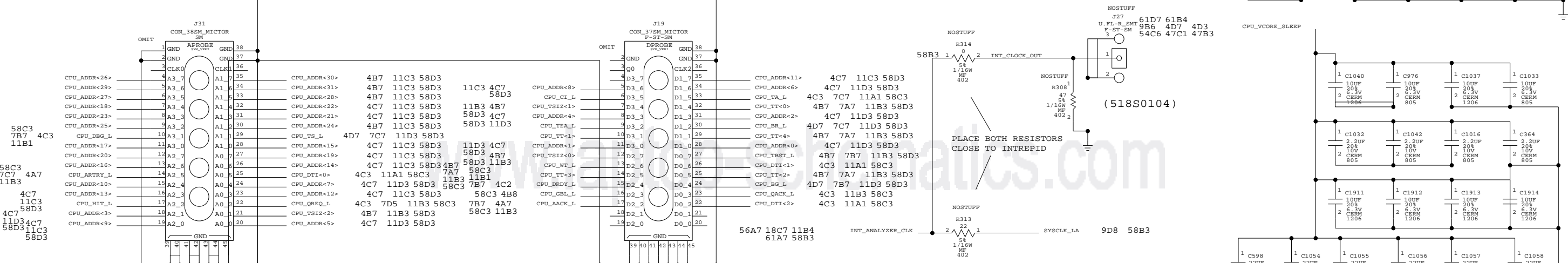
MAXBUS LOGIC ANALYZER SUPPORT

NOTE: INTREPID MAXBUS CONFIG STRAPS MUST DROP TO 1K OR LOGIC ANALYZER MAY AFFECT STRAP VALUES

61C7 54C6 48D4
8D3 7C7 7C5 7C3 7B3 7A3 6D8 4D5
47D2 46D2 46D1 46B7 11D8 11B8 9D2

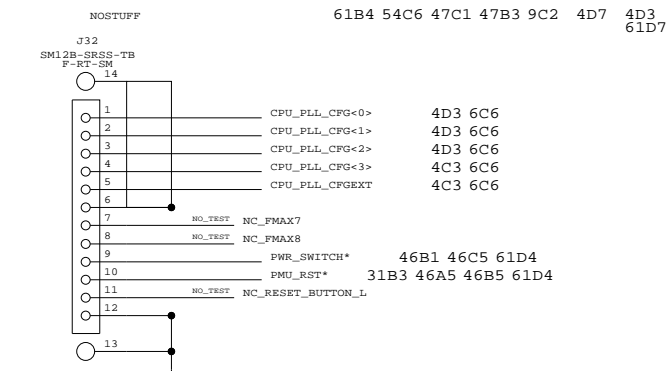


INTREPID CLOCK OUTPUT

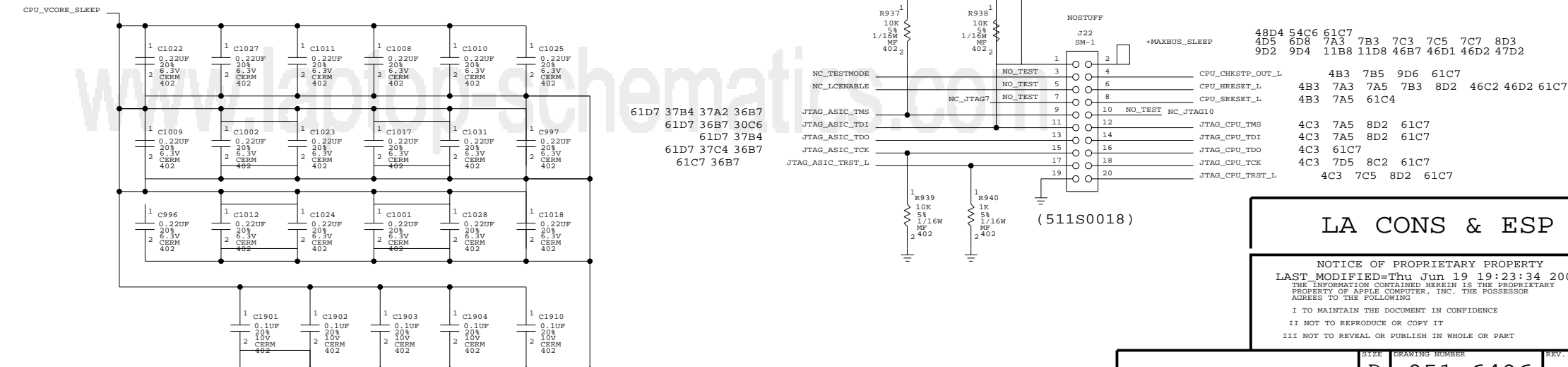


CPU CORE DECOUPLING

FMAX DEBUG CONNECTOR



(518S0105)



PULLDOWN ON TRST* STRONGER TO OVERCOME POSSIBLE LEAKAGE
+3V_MAIN

(511S0018)

LA CONS & ESP

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	D	051-6496	A
SCALE	NONE	SHT	9 OF 74

D

D

C

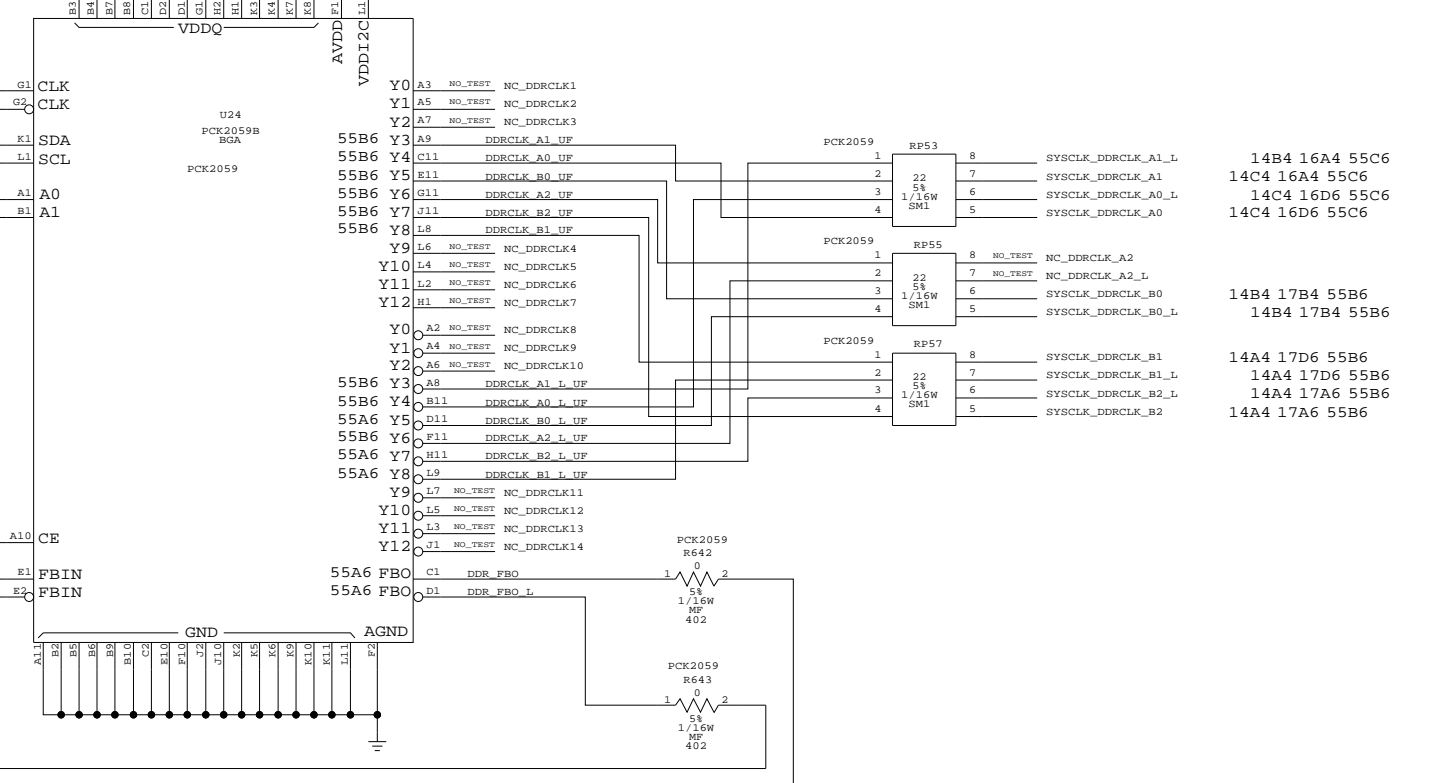
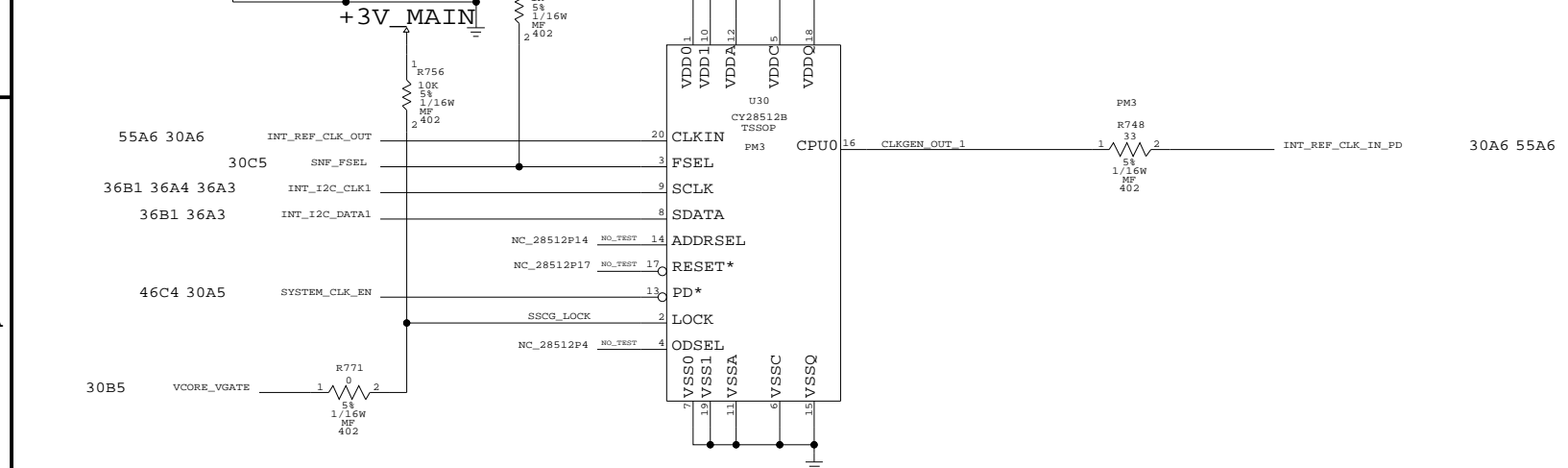
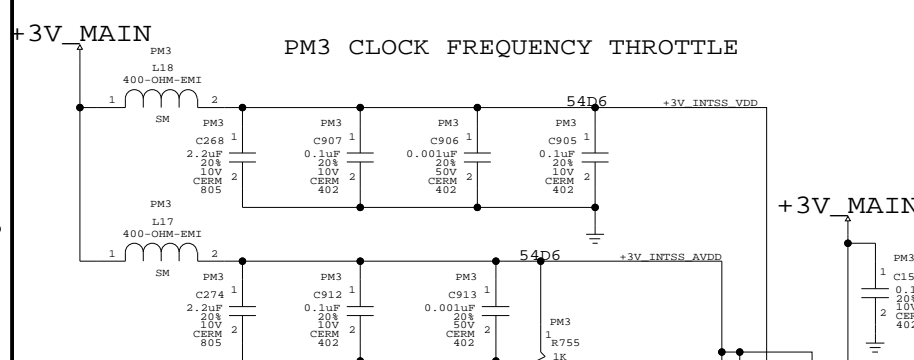
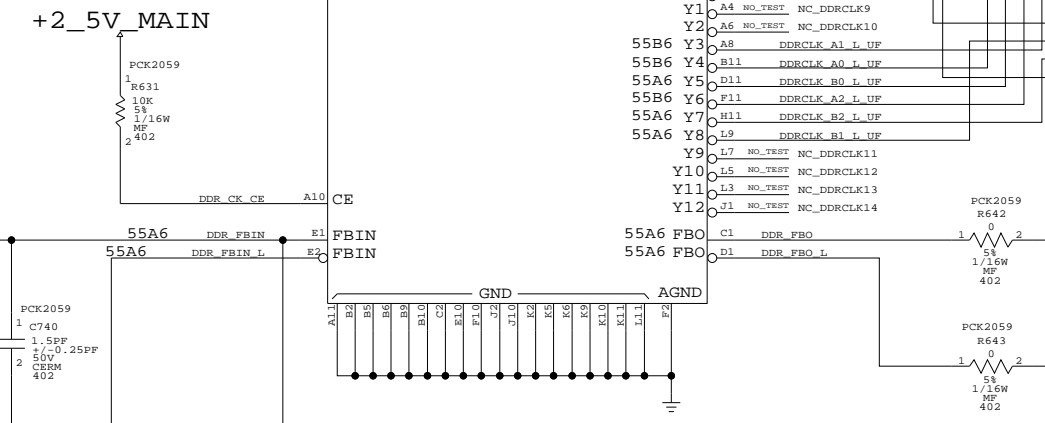
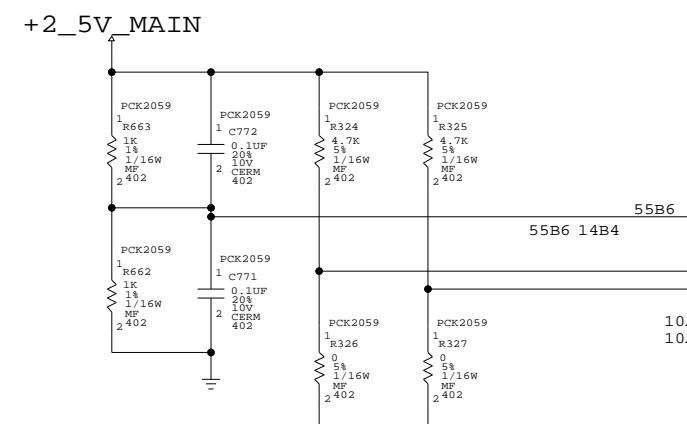
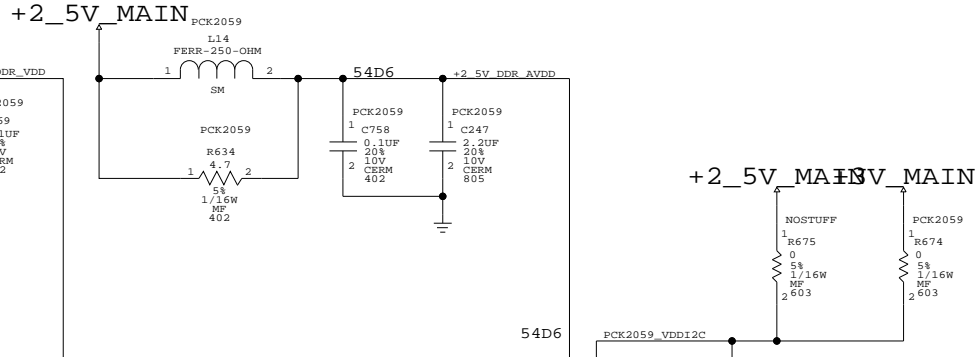
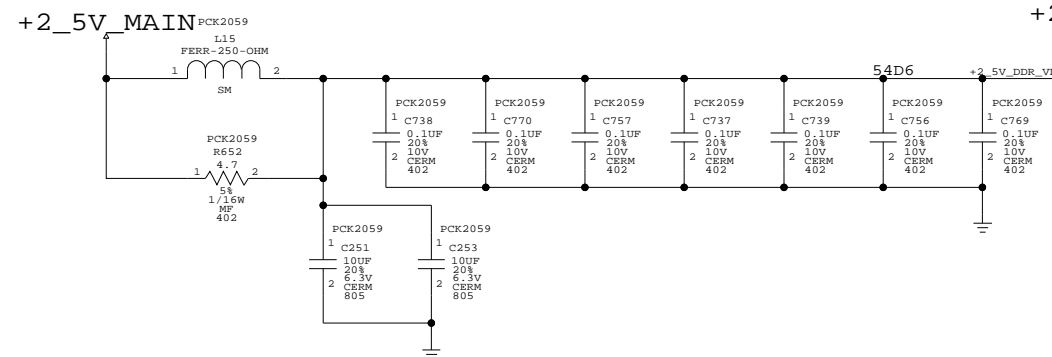
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B

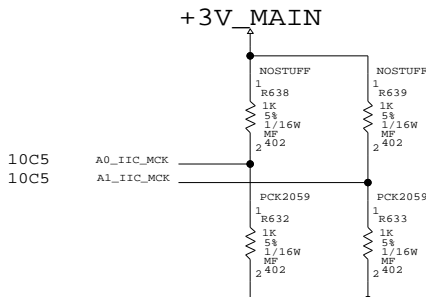
A

A



CLOCK CHIP ALTERNATE SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
359S0065	359S0059	U24	IC, CLK DVR, ZDB	PCK2059



CLOCKS

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SCALE: NONE SHEET: 10 OF 74

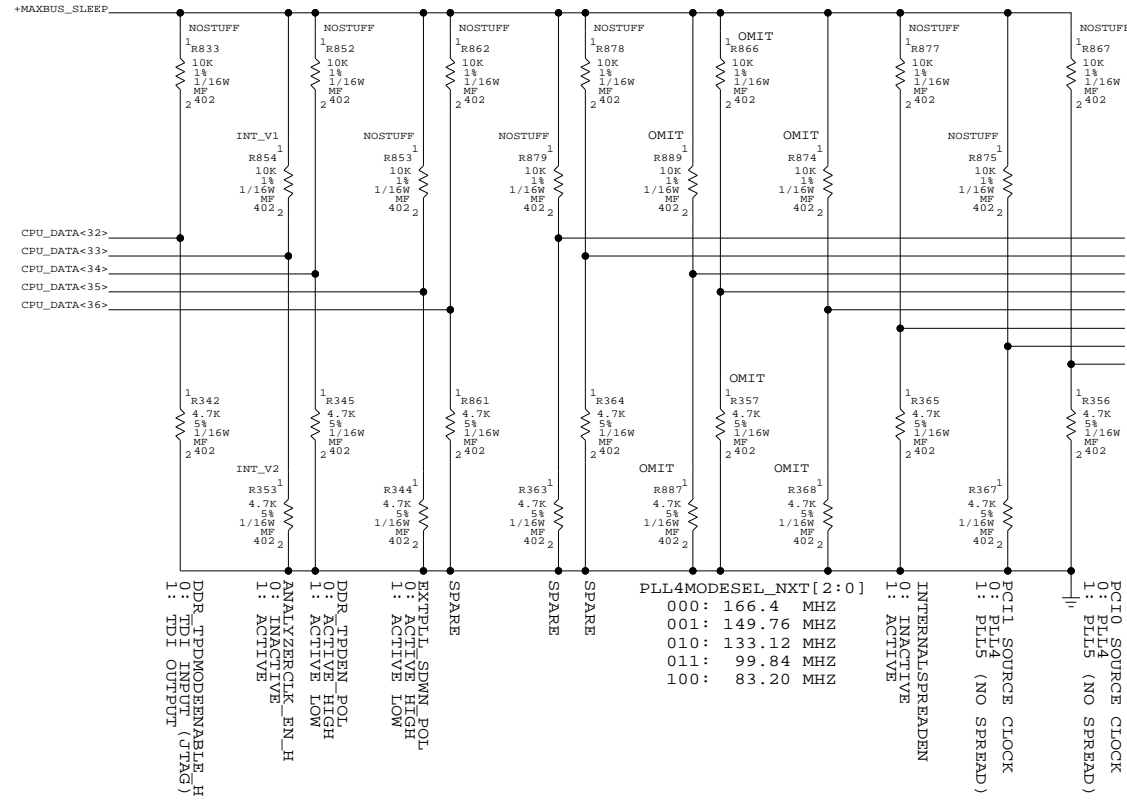
INTREPID BOOT STRAPS BITS 32 - 47

54D3 32D5 30D6 18D6

+1.5V_INTREPID_PLL

INTREPID V1.1 IS 133MHZ ONLY

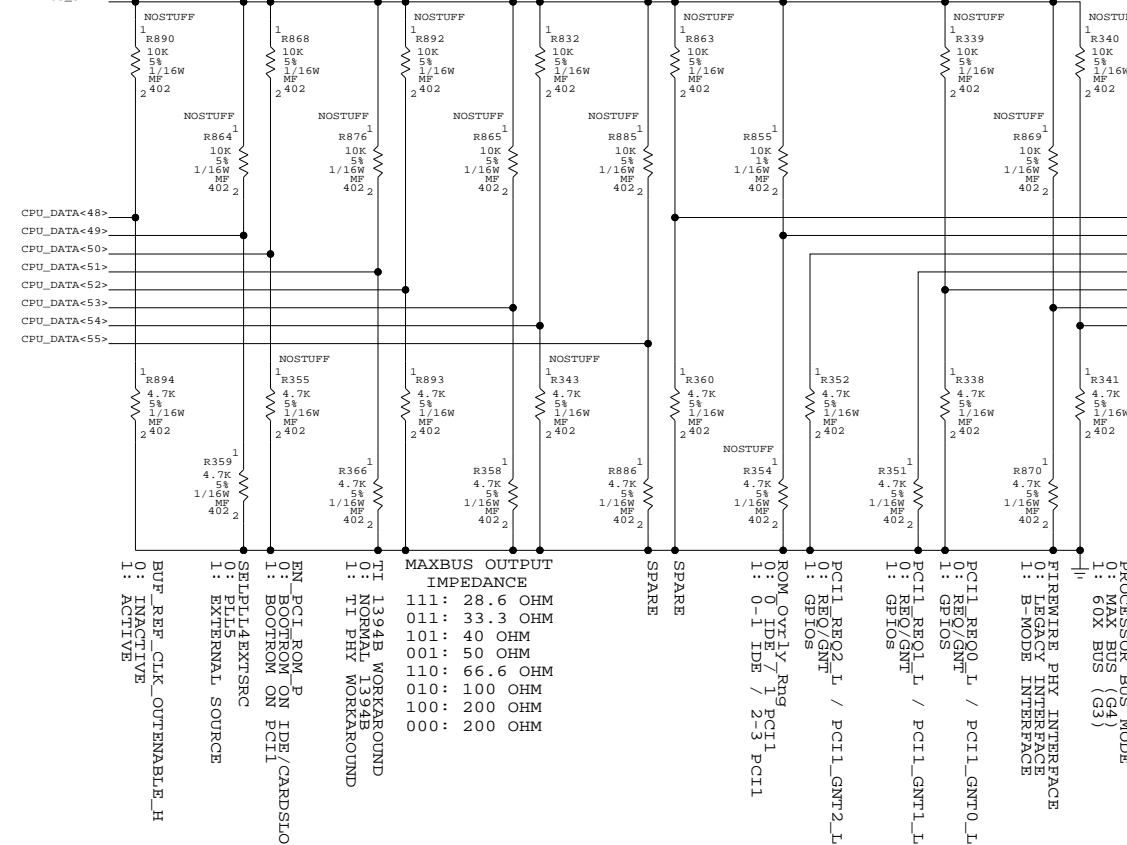
46D2 46D1 61C7
9B2 8D3 46B7
7A3 6D8 4D5
7C5 7C3 7B3
11B8 9D4 9D2
54C6 48D4 47D2



5B4 9D7 11C1 58D3
 5B4 9D5 11B1 58D3
 5B4 9C6 11B1 58D3
 5B4 9C5 11B1 58D3
 5B4 9C8 11B1 58D3
 5B4 9C7 11B1 58D3
 5B4 9C7 11B1 58D3

46D2 46D1 61C7
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11D8 9D4 9D2
54C6 48D4 47D2

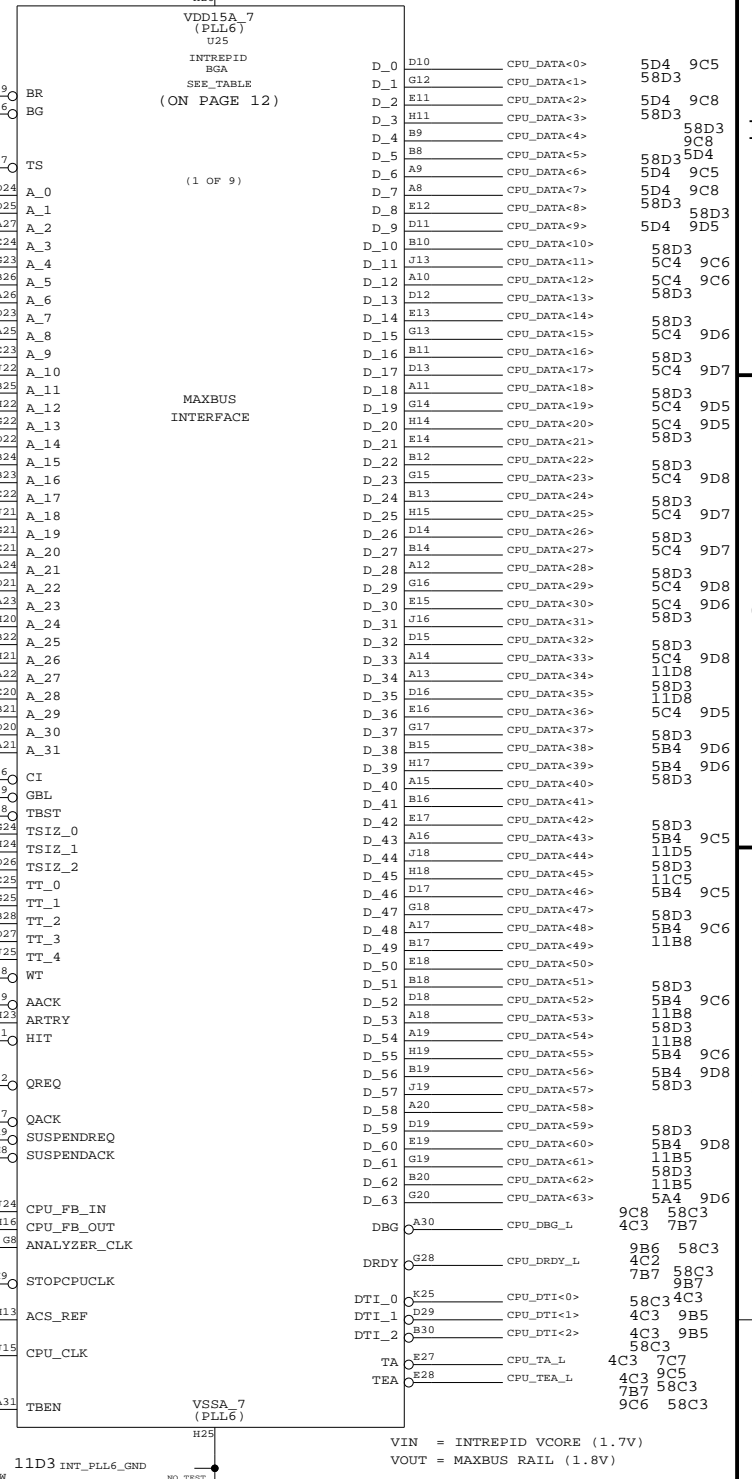
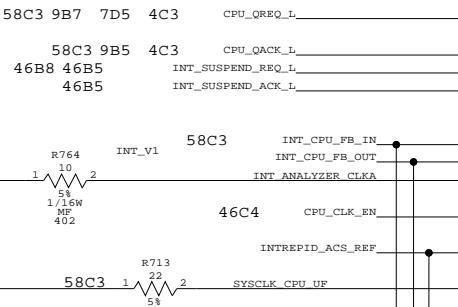
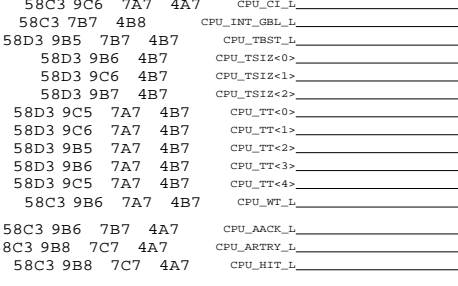
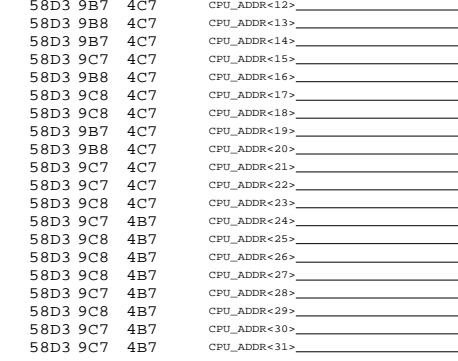
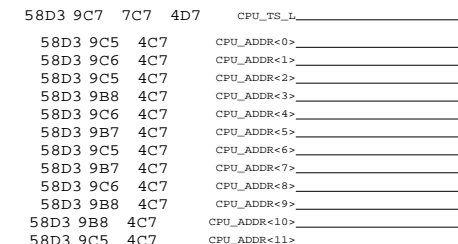
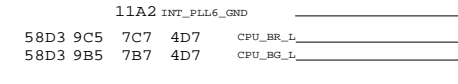
BITS 48 - 63



5B4 9D6 11B1 58D3
 5B4 9D5 11B1 58D3
 5B4 9D8 11B1 58D3
 5B4 9D8 11B1 58D3
 5B4 9D5 11B1 58D3
 5B4 9D5 11B1 58D3
 5A4 9D6 11B1 58D3

11B1 58D3
11B1 9C6 5B4
11B1 9C5 5B4
58D3
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58D3
11B1 9C7 5B4
58D3 5B4
58D3 5B4
58D3

A

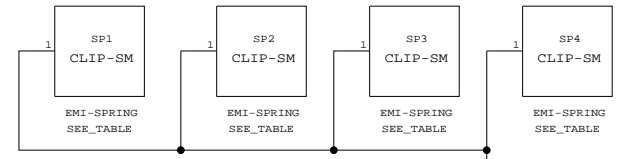
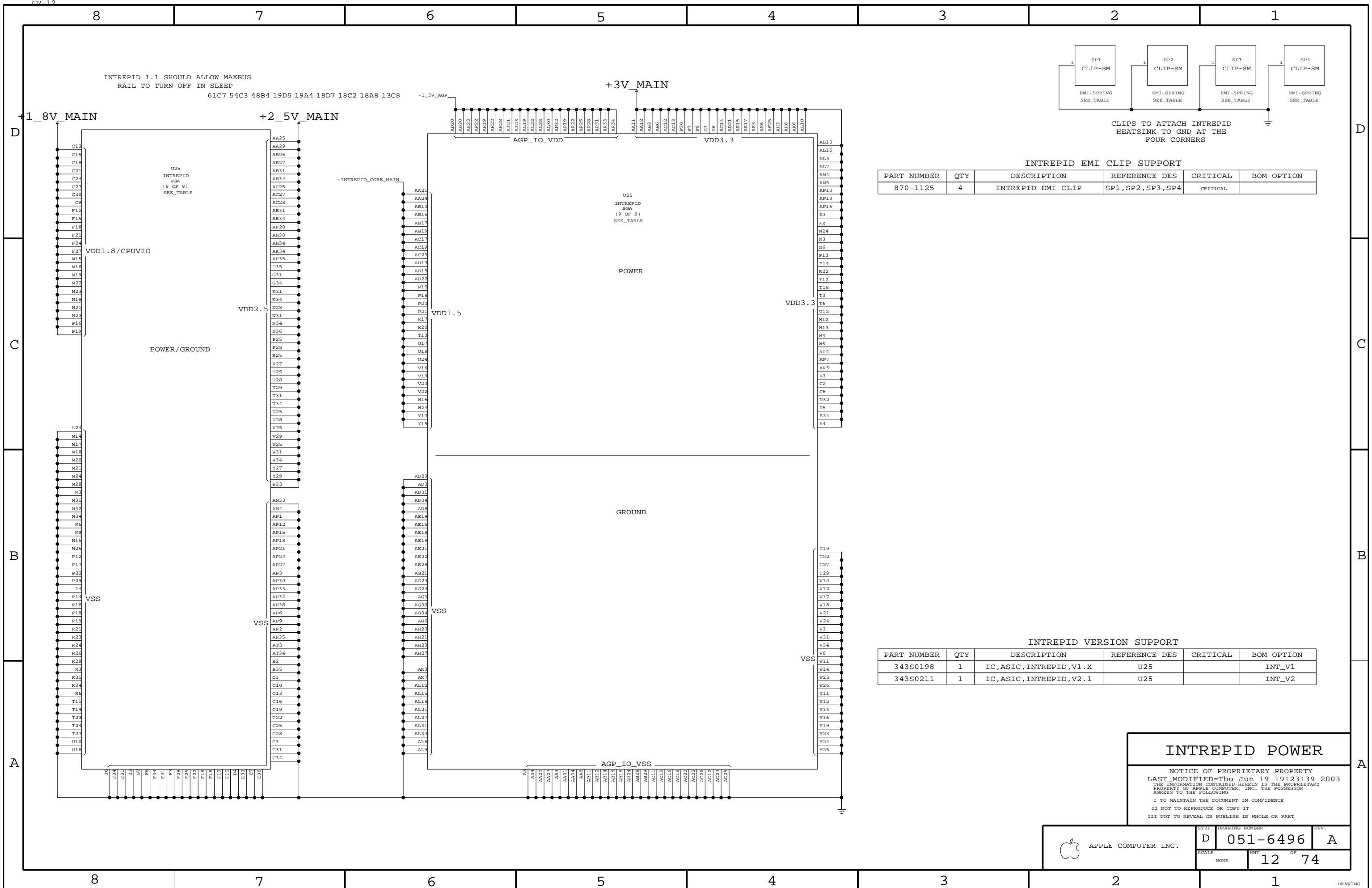


INTREPID MAX
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SIZE: D
 DRAWING NUMBER: 051-6496
 REV: A

SCALE: NONE
 SHEET: 11 OF 74



CLIPS TO ATTACH INTREPID HEATSINK TO GND AT THE FOUR CORNERS

INTREPID EMI CLIP SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1125	4	INTREPID EMI CLIP	SP1,SP2,SP3,SP4	CRITICAL	

INTREPID VERSION SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0198	1	IC,ASIC,INTREPID,V1.X	U25		INT_V1
343S0211	1	IC,ASIC,INTREPID,V2.1	U25		INT_V2

INTREPID POWER

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APPLE COMPUTER INC.	SIZE D SCALE NONE	DRAWING NUMBER 051-6496 SHEET 12 OF 74	REV. A
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8 7 6 5 4 3 2 1

+1_8V_MAIN

INTREPID MAXBUS DECOUPLING

24 Balls (0805)
4 X 10UF (0402)
32 X 0.22UF (0402)

49B2 48B3 12D6 61C7

+INTREPID_CORE_MAIN INTREPID CORE DECOUPLING

30 Balls (0805)
4 X 10UF (0402)
29 X 0.22UF (0402)

D

D

61C7
48B4
19A4
18C2
12D6
18A8
18D7
19D5
54C3

+1_5V_AGP

INTREPID AGP I/O DECOUPLING

21 Balls (0805)
4 X 10UF (0402)
24 X 0.22UF (0402)

+3V_MAIN

INTREPID 3.3V DECOUPLING

57 Balls (0805)
4 X 10UF (0402)
68 X 0.22UF (0402)

C

C

+2_5V_MAIN

INTREPID DDR DECOUPLING

44 Balls (0805)
4 X 10UF (0402)
51 X 0.22UF (0402)

B

B

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A

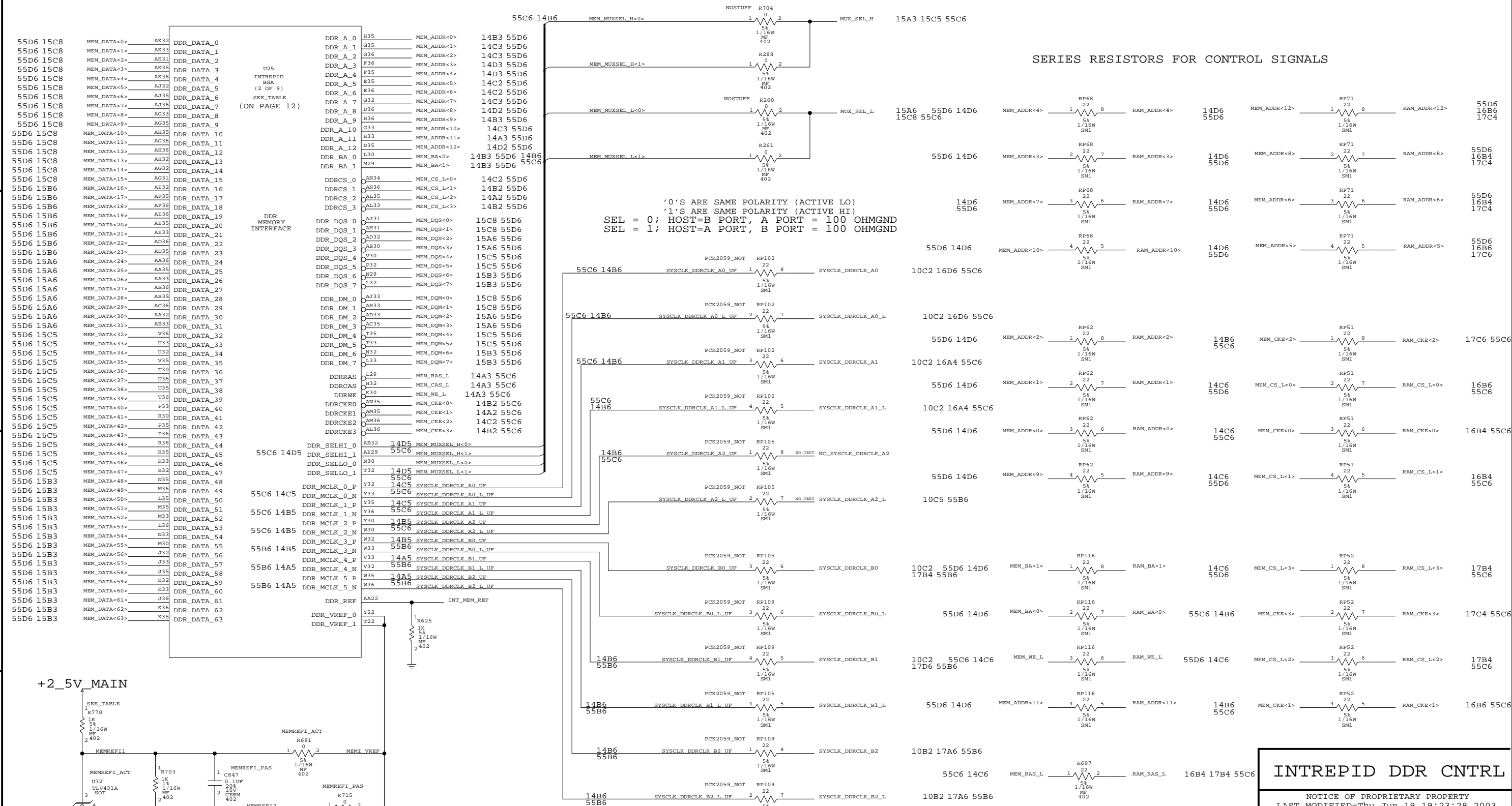
INTREPID BYPASS

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	SCALE	13	74

8 7 6 5 4 3 2 1

DDR MUX CONNECTIONS
0-ohm resistors to allow
rewiring if necessary



U25
INTREPID
BGA
(2 OF 9)
SEE_TABLE
(ON PAGE 12)

DDR
MEMORY
INTERFACE

SERIES RESISTORS FOR CONTROL SIGNALS

'0'S ARE SAME POLARITY (ACTIVE LO)
'1'S ARE SAME POLARITY (ACTIVE HI)
SEL = 0; HOST=B PORT, A PORT = 100 OHMGND
SEL = 1; HOST=A PORT, B PORT = 100 OHMGND

INTREPID DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES,1K-OHM,5%,1/16W,0402	R778		MEMREFI_ACT
116S1000	1	RES,0-OHM,5%,1/16W,0402	R778		MEMREFI_PAS

INTREPID DDR CNTRL

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SIZE	D	DRAWING NUMBER	051-6496	REV.	A
SCALE	NONE	SHT	14	OF	74

+2_5V_MAIN

+2_5V_MAIN

D

D

C

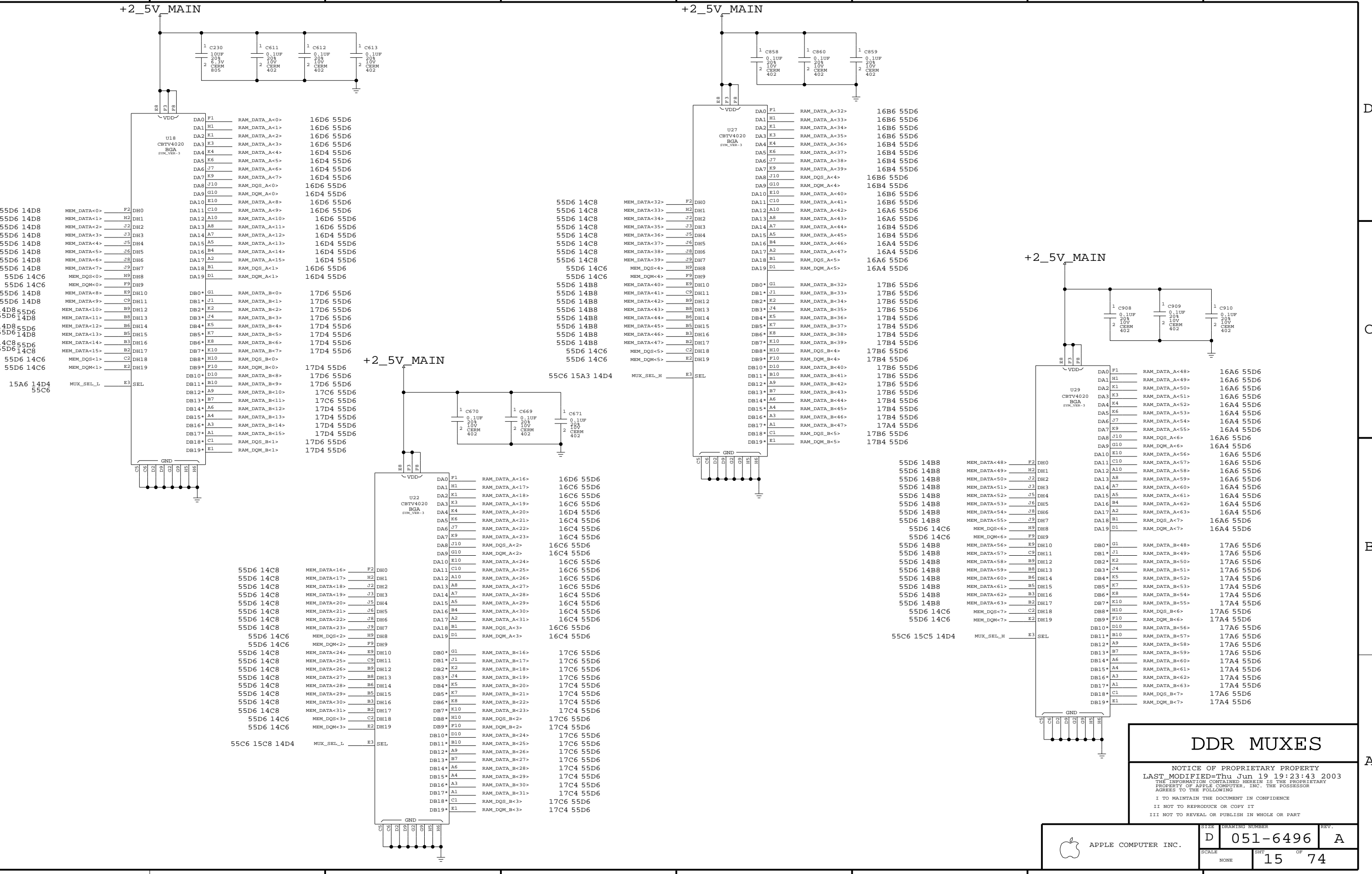
C

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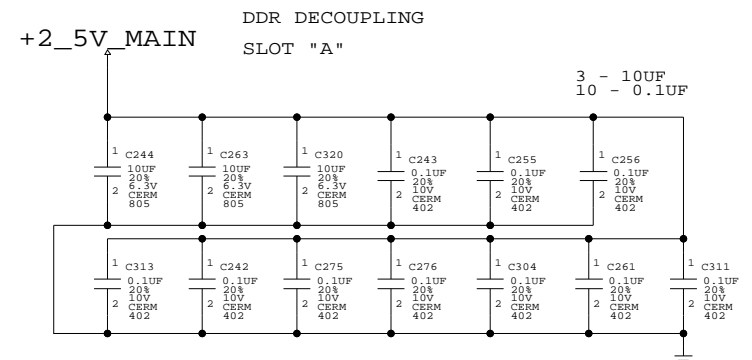
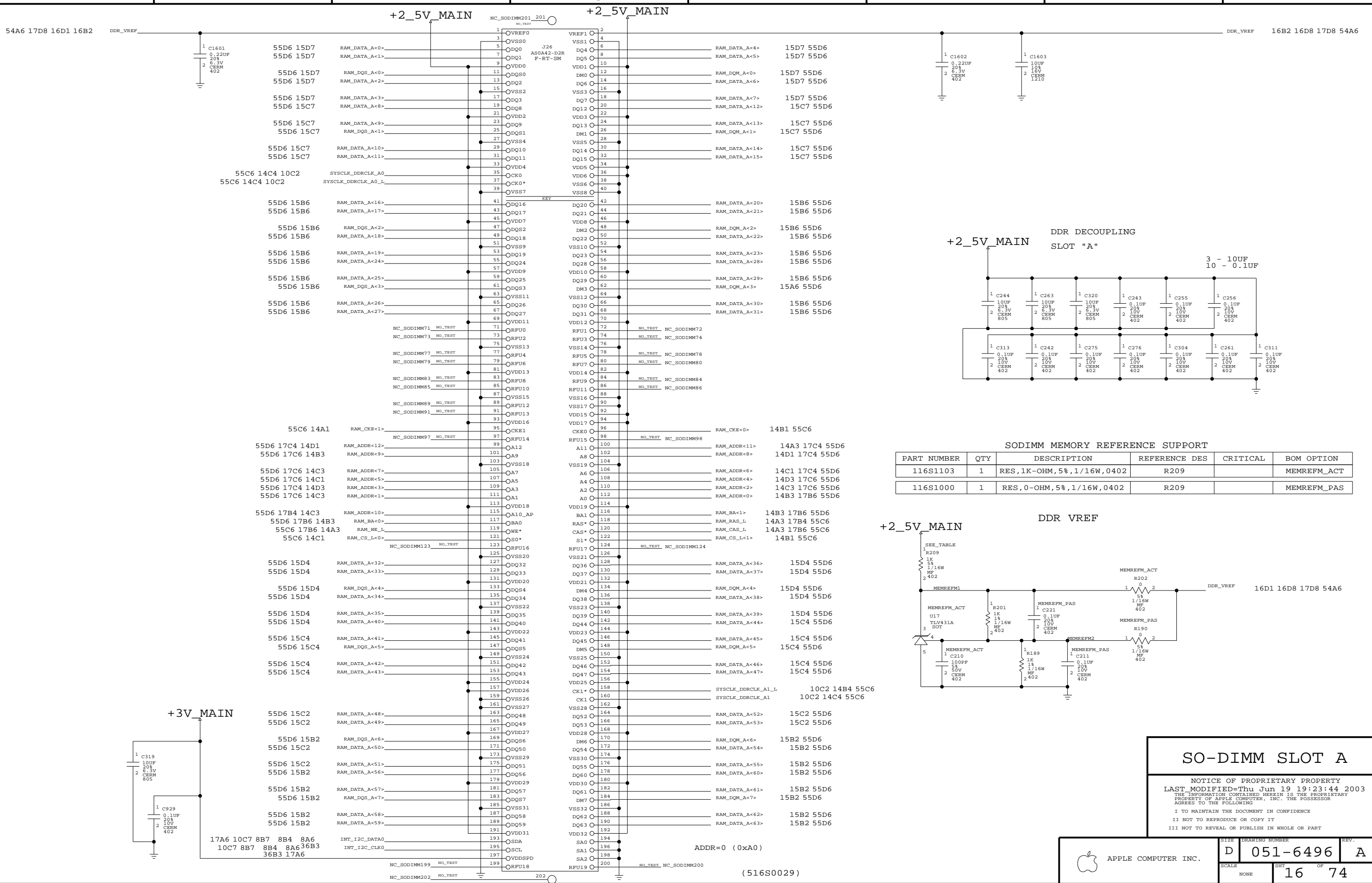
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DDR MUXES

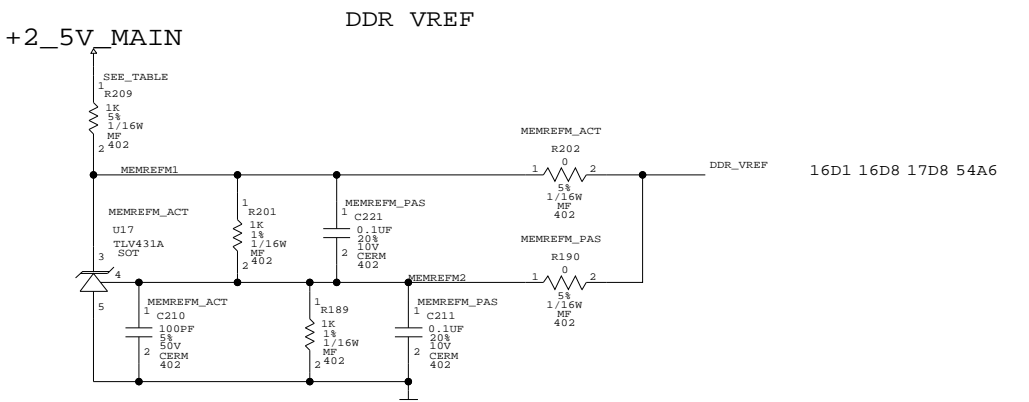
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	SCALE	SHT	OF
		15	74



SODIMM MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R209		MEMREFM_ACT
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R209		MEMREFM_PAS

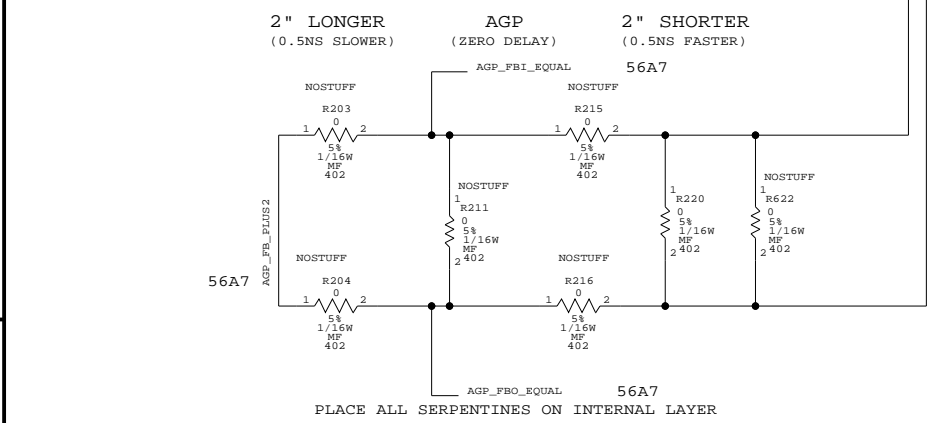
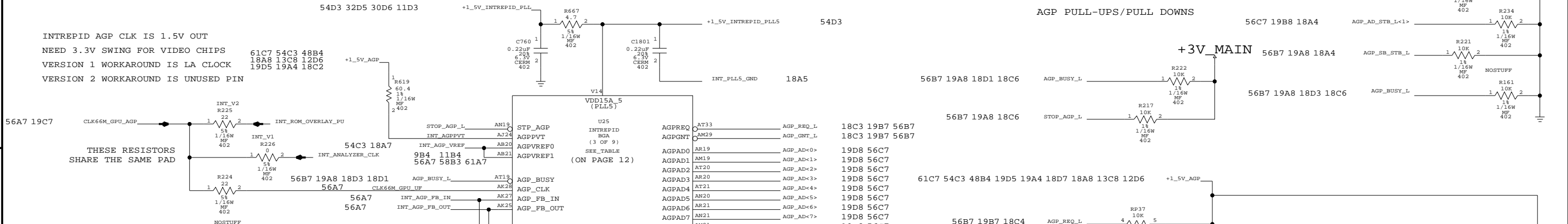


SO-DIMM SLOT A

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	SCALE: NONE	SHEET: 16	OF: 74

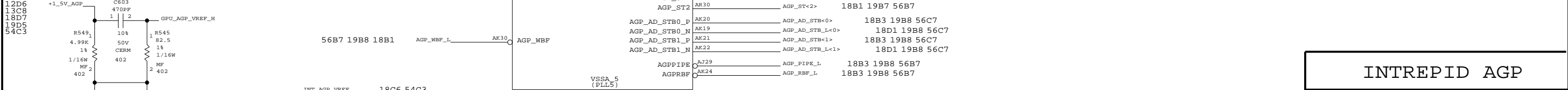
INTREPID AGP CLK IS 1.5V OUT
NEED 3.3V SWING FOR VIDEO CHIPS
VERSION 1 WORKAROUND IS LA CLOCK
VERSION 2 WORKAROUND IS UNUSED PIN




AGP INTERFACES
VOUT = AGPIO (1.5V)
VIN = VCORE (1.5V)

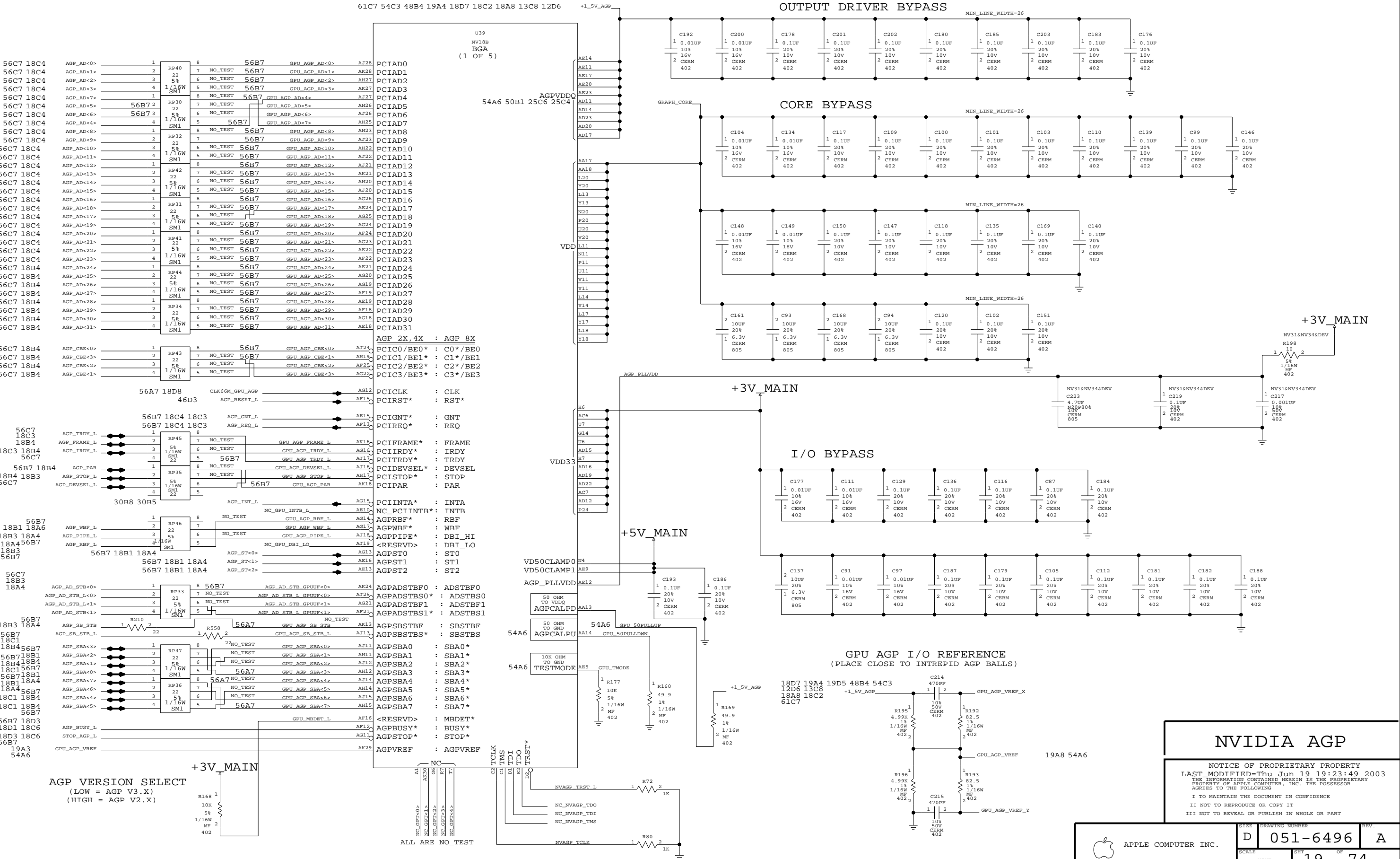


GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)



INTREPID AGP
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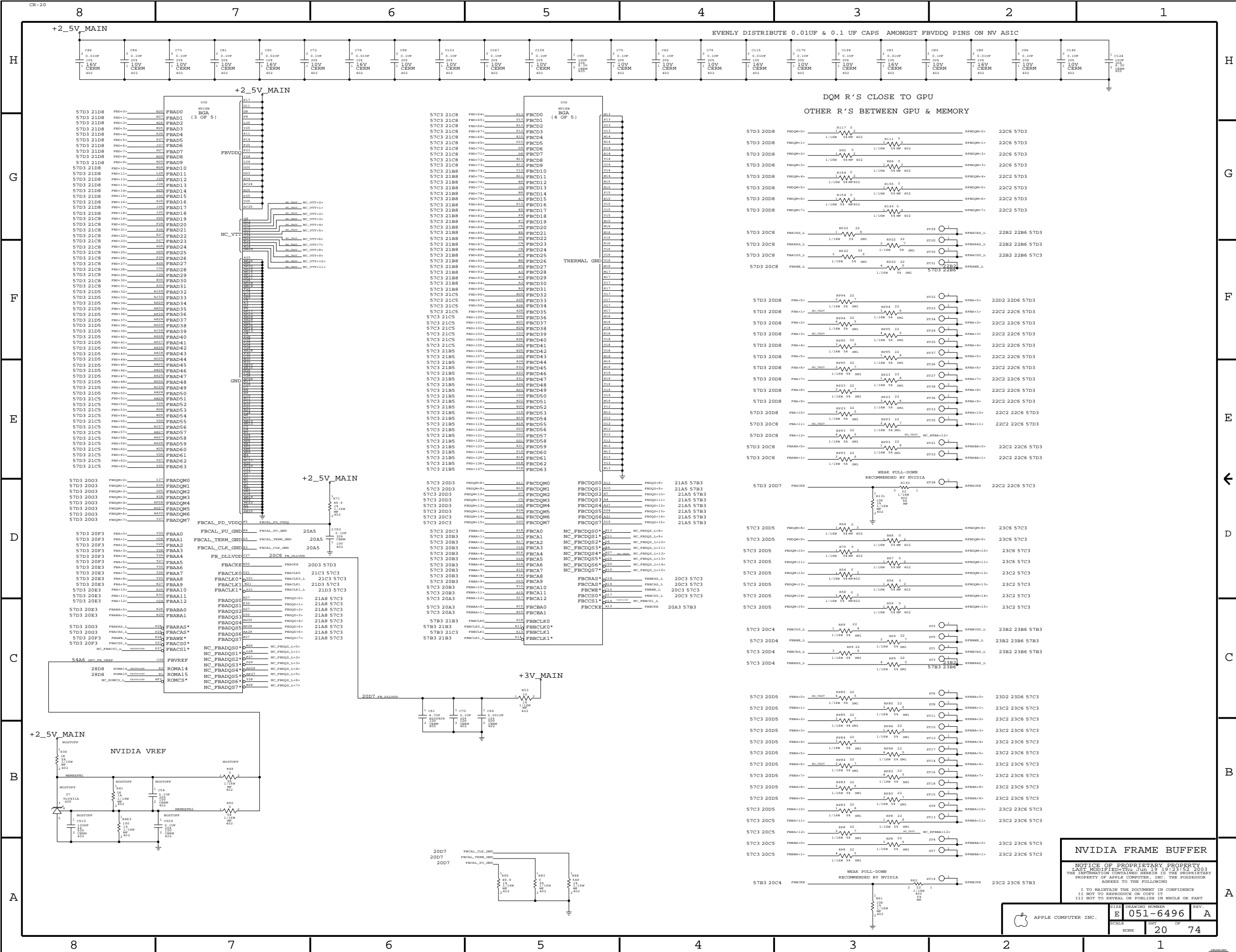
AGP VERSION SELECT
 (LOW = AGP V3.X)
 (HIGH = AGP V2.X)

GPU AGP I/O REFERENCE
 (PLACE CLOSE TO INTREPID AGP BALLS)

NVIDIA AGP

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NVIDIA FRAME BUFFER

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SCALE NONE

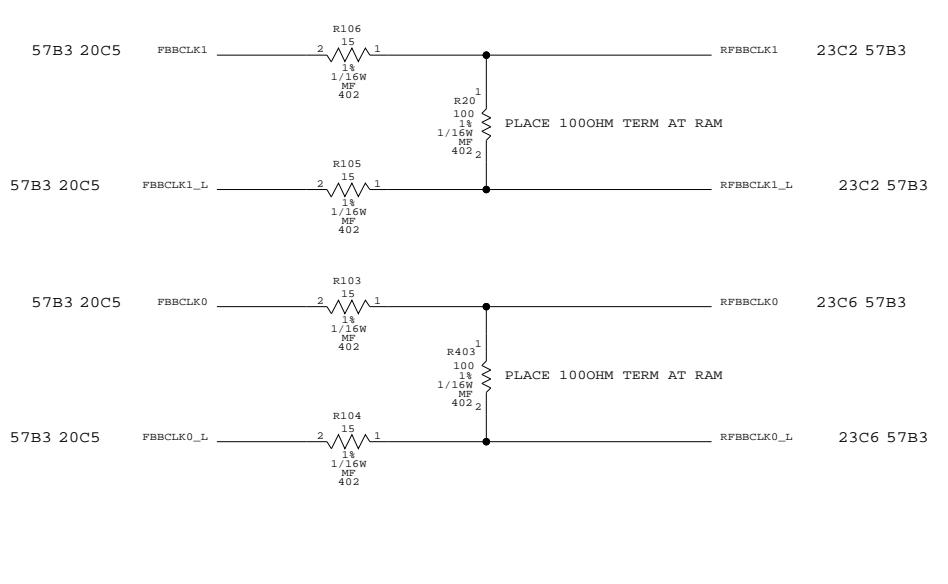
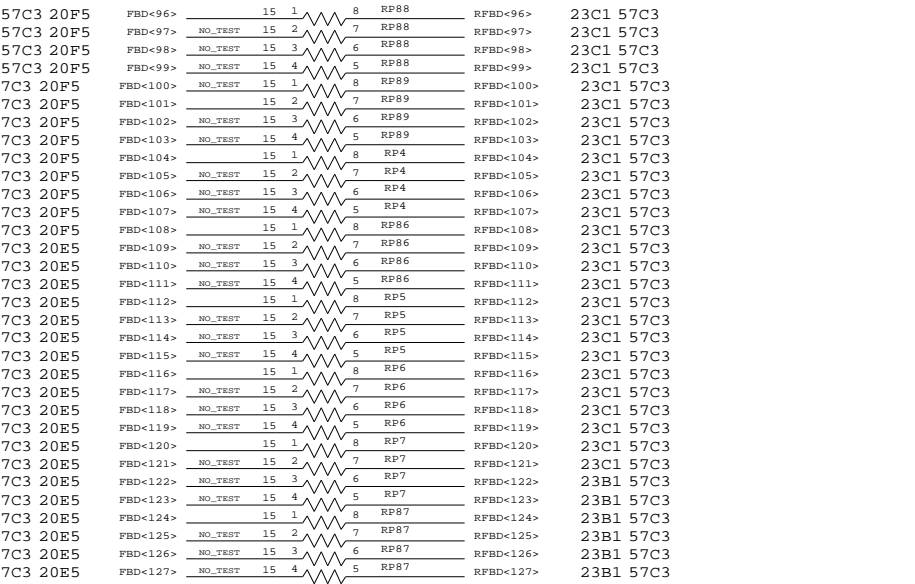
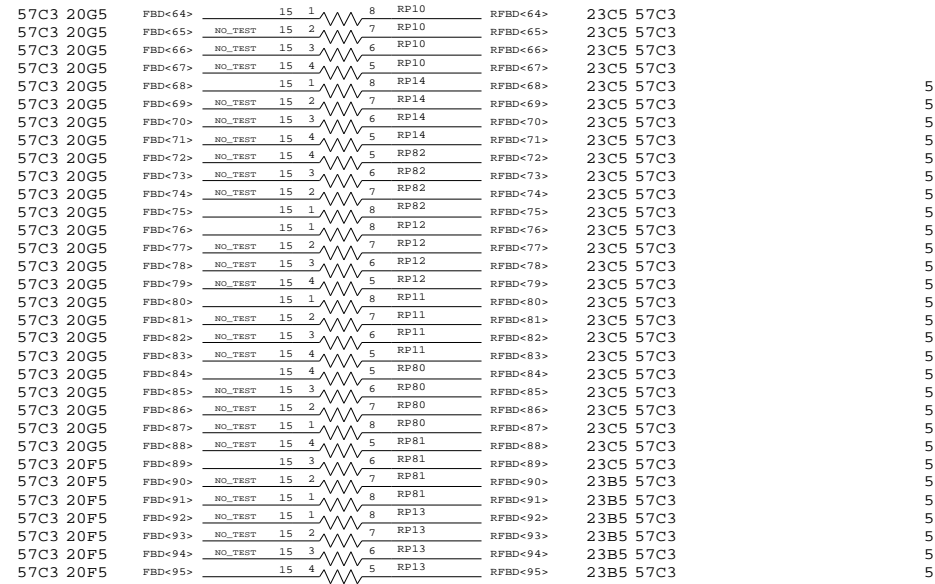
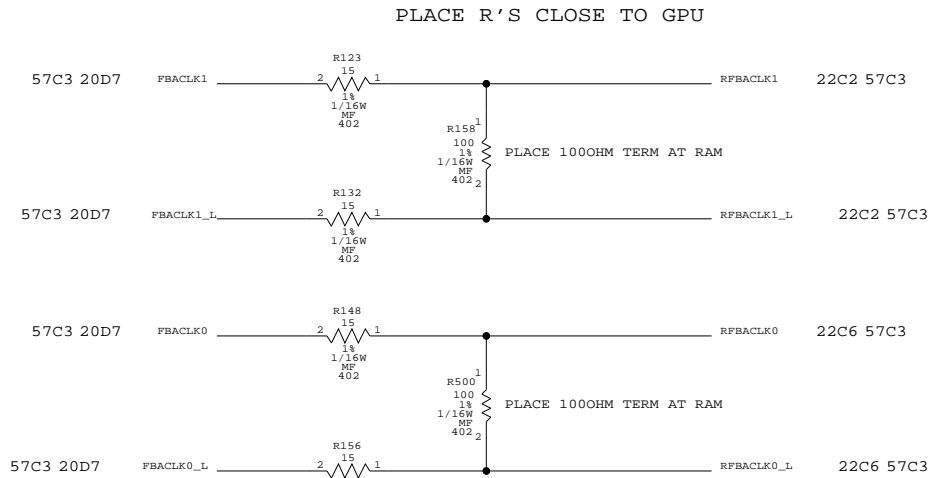
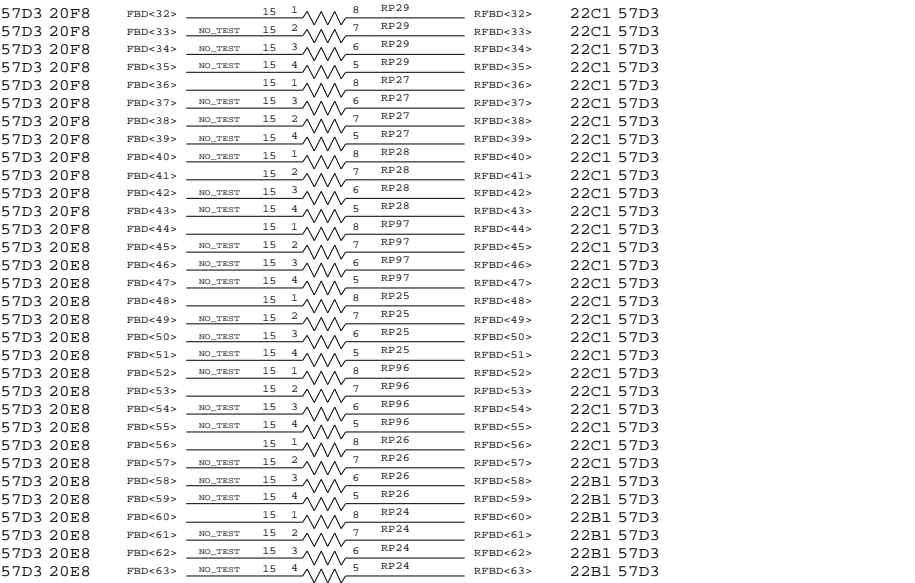
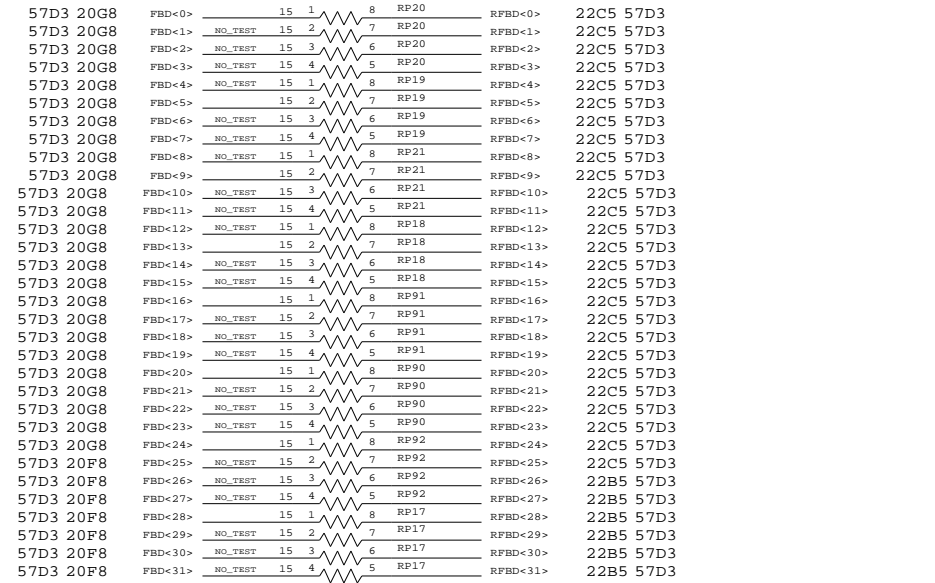
SHEET 20 OF 74

REV. A

DATE 051-6496

APPLE COMPUTER, INC.

PLACE R'S BETWEEN GPU & MEMORY

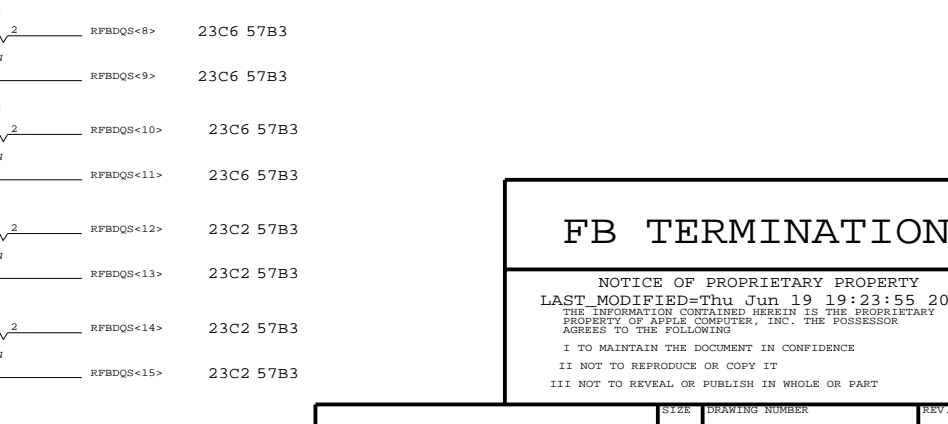
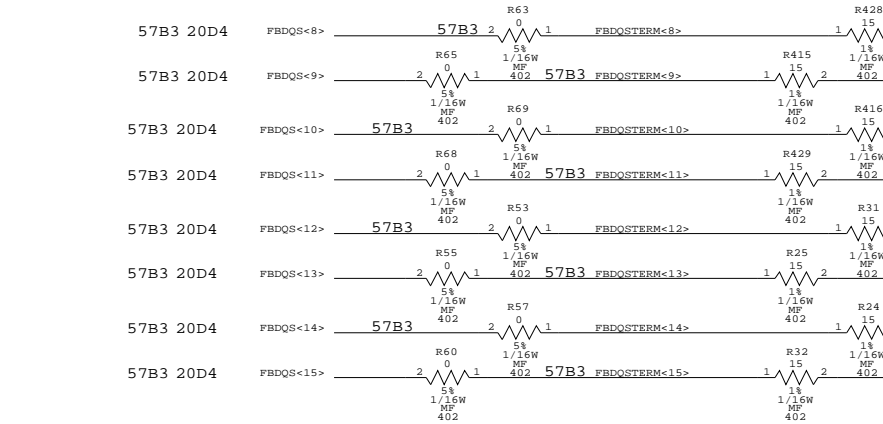
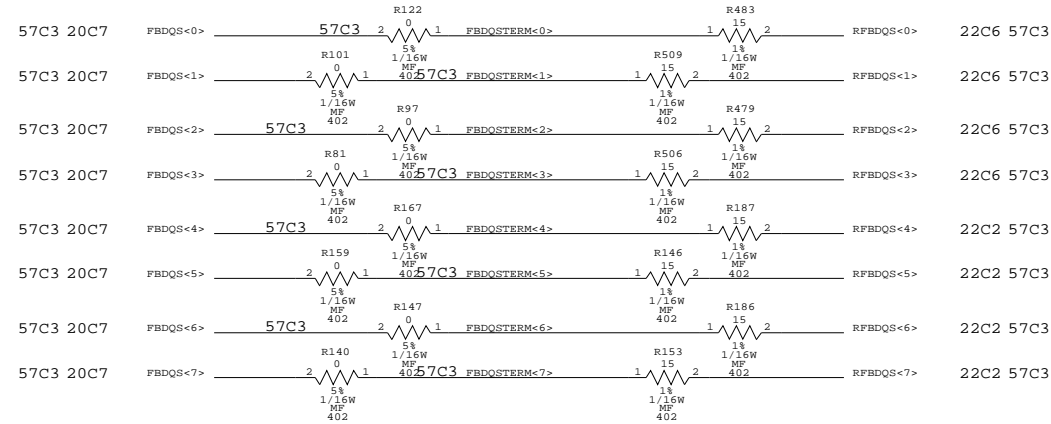


PLACE THESE R CLOSE TO GPU

PLACE THESE R CLOSE TO SGRAM

PLACE THESE R CLOSE TO GPU

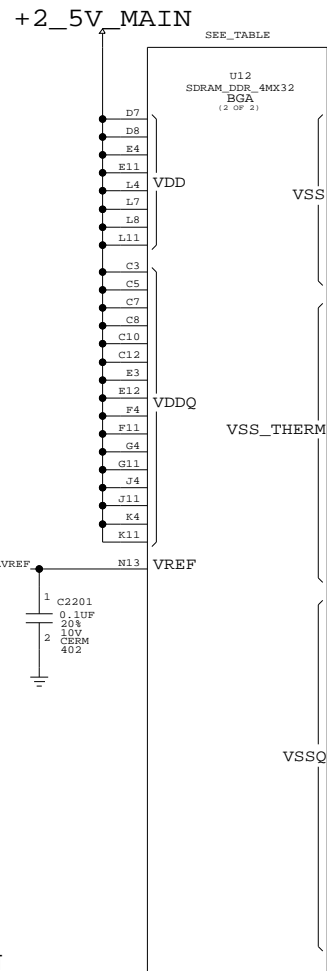
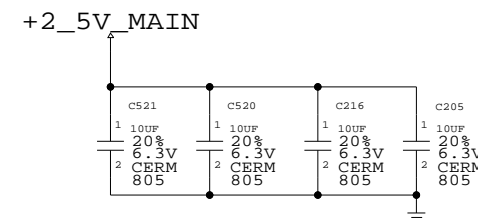
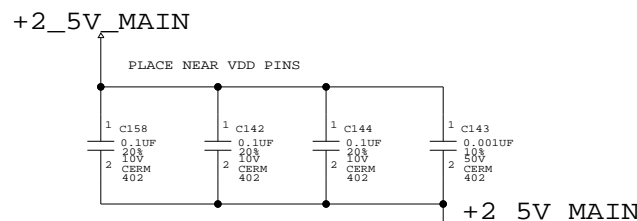
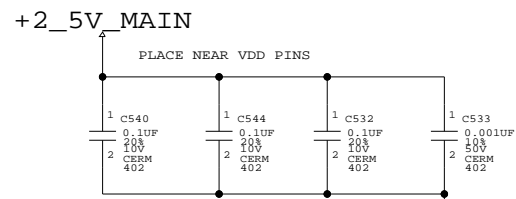
PLACE THESE R CLOSE TO SGRAM



FB TERMINATION

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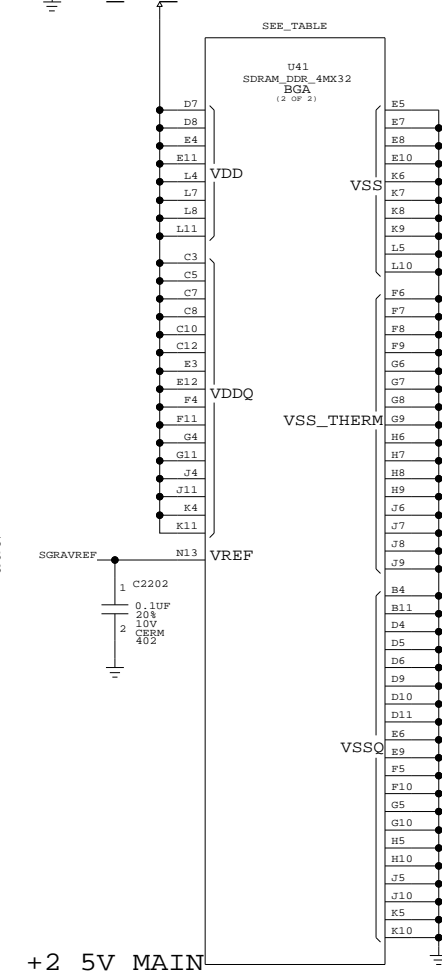


SEE_TABLE

57D3 22D2 20F2	RFBA<0>	N5	A0
57D3 22C2 20F2	RFBA<1>	N6	A1
57D3 22C2 20F2	RFBA<2>	M6	A2
57D3 22C2 20F2	RFBA<3>	N7	A3
57D3 22C2 20F2	RFBA<4>	N8	A4
57D3 22C2 20F2	RFBA<5>	M9	A5
57D3 22C2 20E2	RFBA<6>	N9	A6
57D3 22C2 20E2	RFBA<7>	N10	A7
57D3 22C2 20E2	RFBA<8>	N11	A8
57D3 22C2 20E2	RFBA<9>	M8	A9
57D3 22C2 20E2	RFBA<10>	L6	A10
57D3 22C2 20E2	RFBA<11>	M7	A11
57C3 21A6	RFBDQS<0>	B2	DQS0
57C3 21A6	RFBDQS<1>	H13	DQS1
57C3 21A6	RFBDQS<2>	H2	DQS2
57C3 21A6	RFBDQS<3>	B13	DQS3
57D3 20G2	RFBDQM<0>	B3	DM0
57D3 20G2	RFBDQM<1>	H12	DM1
57D3 20G2	RFBDQM<2>	H3	DM2
57D3 20G2	RFBDQM<3>	B12	DM3
57D3 22C2 20E2	RFBABA<0>	N4	BA0
57D3 22C2 20E2	RFBABA<1>	M5	BA1
57C3 21C1	RFBACKL0	M11	CK
57C3 21C1	RFBACKL1_L	M12	CK
57C3 22C2 20D2	RFBACKE	N12	CKE
57C3 22B2 20F2	RFBACKS0_L	N2	CS
57D3 22B2 20G2	RFBARAS_L	M2	RAS
57D3 22B2 20G2	RFBACKAS_L	L2	CAS
57D3 22B2 20F2	RFBAWE_L	L3	WE
NO_TEST	NC_FB1<0>	C4	
NO_TEST	NC_FB1<1>	C11	
NO_TEST	NC_FB1<2>	H4	
NO_TEST	NC_FB1<3>	H11	
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NO_TEST	NC_FB1<6>	M3	
NO_TEST	NC_FB1<7>	M4	
NO_TEST	NC_FB1<8>	N3	
NO_TEST	NC_FB1<9>	L9	
NO_TEST	NC_FB1<10>	M10	

SEE_TABLE

DQ0	C6	RFBD<0>	21D7 57D3
DQ1	C6	RFBD<1>	21D7 57D3
DQ2	B6	RFBD<2>	21D7 57D3
DQ3	B5	RFBD<3>	21D7 57D3
DQ4	C2	RFBD<4>	21D7 57D3
DQ5	D3	RFBD<5>	21D7 57D3
DQ6	D2	RFBD<6>	21D7 57D3
DQ7	E2	RFBD<7>	21D7 57D3
DQ8	K13	RFBD<8>	21D7 57D3
DQ9	K12	RFBD<9>	21D7 57D3
DQ10	J13	RFBD<10>	21D7 57D3
DQ11	J12	RFBD<11>	21D7 57D3
DQ12	G13	RFBD<12>	21D7 57D3
DQ13	G12	RFBD<13>	21D7 57D3
DQ14	F13	RFBD<14>	21D7 57D3
DQ15	F12	RFBD<15>	21D7 57D3
DQ16	F2	RFBD<16>	21D7 57D3
DQ17	F2	RFBD<17>	21D7 57D3
DQ18	G3	RFBD<18>	21D7 57D3
DQ19	G2	RFBD<19>	21C7 57D3
DQ20	J3	RFBD<20>	21C7 57D3
DQ21	J2	RFBD<21>	21C7 57D3
DQ22	K2	RFBD<22>	21C7 57D3
DQ23	K3	RFBD<23>	21C7 57D3
DQ24	E13	RFBD<24>	21C7 57D3
DQ25	D13	RFBD<25>	21C7 57D3
DQ26	D12	RFBD<26>	21C7 57D3
DQ27	C13	RFBD<27>	21C7 57D3
DQ28	B10	RFBD<28>	21C7 57D3
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DQ30	C9	RFBD<30>	21C7 57D3
DQ31	B8	RFBD<31>	21C7 57D3

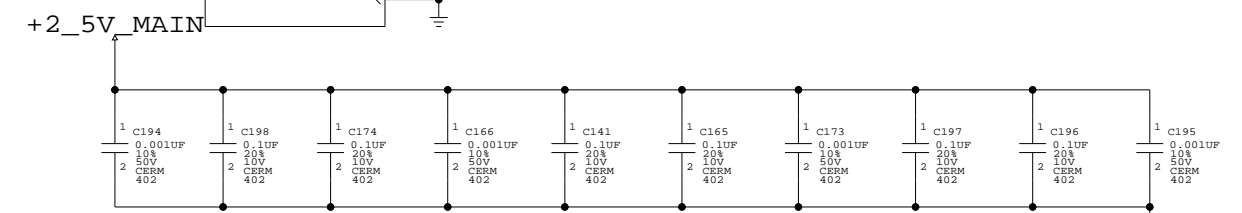
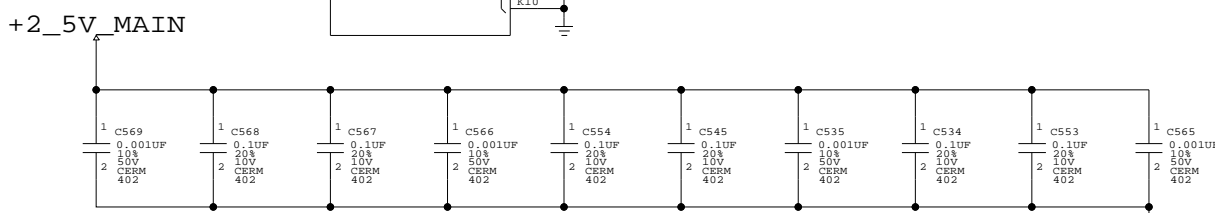


SEE_TABLE

DQ0	B7	RFBD<32>	21D4 57D3
DQ1	C6	RFBD<33>	21D4 57D3
DQ2	B6	RFBD<34>	21D4 57D3
DQ3	B5	RFBD<35>	21D4 57D3
DQ4	C2	RFBD<36>	21D4 57D3
DQ5	D3	RFBD<37>	21D4 57D3
DQ6	D2	RFBD<38>	21D4 57D3
DQ7	E2	RFBD<39>	21D4 57D3
DQ8	K13	RFBD<40>	21D4 57D3
DQ9	K12	RFBD<41>	21D4 57D3
DQ10	J13	RFBD<42>	21D4 57D3
DQ11	J12	RFBD<43>	21D4 57D3
DQ12	G13	RFBD<44>	21D4 57D3
DQ13	G12	RFBD<45>	21D4 57D3
DQ14	F13	RFBD<46>	21D4 57D3
DQ15	F12	RFBD<47>	21D4 57D3
DQ16	F2	RFBD<48>	21D4 57D3
DQ17	F2	RFBD<49>	21D4 57D3
DQ18	G3	RFBD<50>	21D4 57D3
DQ19	G2	RFBD<51>	21C4 57D3
DQ20	J3	RFBD<52>	21C4 57D3
DQ21	J2	RFBD<53>	21C4 57D3
DQ22	K2	RFBD<54>	21C4 57D3
DQ23	K3	RFBD<55>	21C4 57D3
DQ24	E13	RFBD<56>	21C4 57D3
DQ25	D13	RFBD<57>	21C4 57D3
DQ26	D12	RFBD<58>	21C4 57D3
DQ27	C13	RFBD<59>	21C4 57D3
DQ28	B10	RFBD<60>	21C4 57D3
DQ29	B9	RFBD<61>	21C4 57D3
DQ30	C9	RFBD<62>	21C4 57D3
DQ31	B8	RFBD<63>	21C4 57D3

SEE_TABLE

57C3 21A6	RFBDQS<4>	B2	DQS0
57C3 21A6	RFBDQS<5>	H13	DQS1
57C3 21A6	RFBDQS<6>	H2	DQS2
57C3 21A6	RFBDQS<7>	B13	DQS3
57D3 20G2	RFBDQM<4>	B3	DM0
57D3 20G2	RFBDQM<5>	H12	DM1
57D3 20G2	RFBDQM<6>	H3	DM2
57D3 20G2	RFBDQM<7>	B12	DM3
57D3 22C6 20E2	RFBABA<0>	N4	BA0
57D3 22C6 20E2	RFBABA<1>	M5	BA1
57C3 21D1	RFBACKL1	M11	CK
57C3 21D1	RFBACKL1_L	M12	CK
57C3 22C6 20D2	RFBACKE	N12	CKE
57C3 22B6 20F2	RFBACKS0_L	N2	CS
57D3 22B6 20G2	RFBARAS_L	M2	RAS
57D3 22B6 20G2	RFBACKAS_L	L2	CAS
57D3 22B6 20F2	RFBAWE_L	L3	WE
NO_TEST	NC_FB2<0>	C4	
NO_TEST	NC_FB2<1>	C11	
NO_TEST	NC_FB2<2>	H4	
NO_TEST	NC_FB2<3>	H11	
NO_TEST	NC_FB2<4>	L12	
NO_TEST	NC_FB2<5>	L13	
NO_TEST	NC_FB2<6>	M3	
NO_TEST	NC_FB2<7>	M4	
NO_TEST	NC_FB2<8>	N3	
NO_TEST	NC_FB2<9>	L9	
NO_TEST	NC_FB2<10>	M10	



+2_5V_MAIN

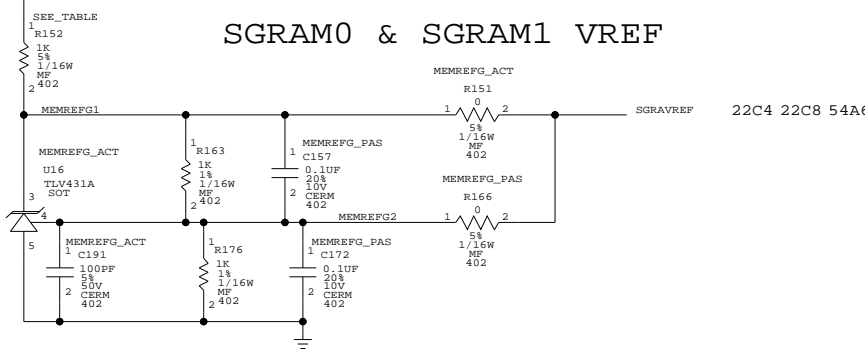
+2_5V_MAIN

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	275_SAMSUNG
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	300_HYNIX_32M
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	300_SAMSUNG_32M
333S0250	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	275_HYNIX

SGRAM0 & SGRAM1 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R152		MEMREFG_ACT
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R152		MEMREFG_PAS

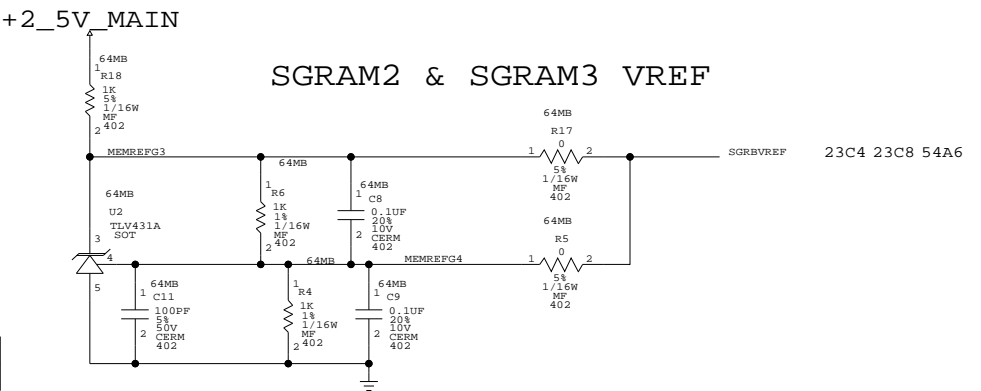
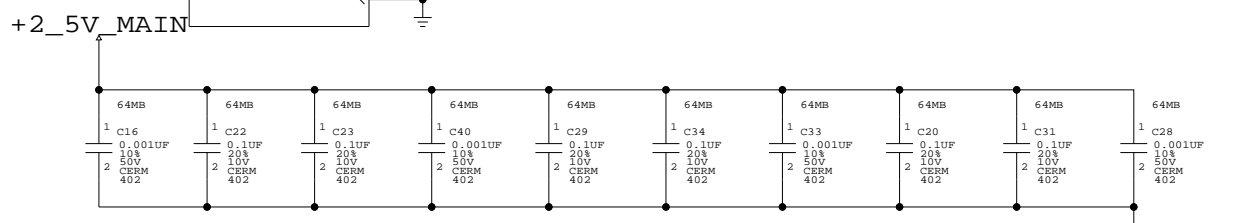
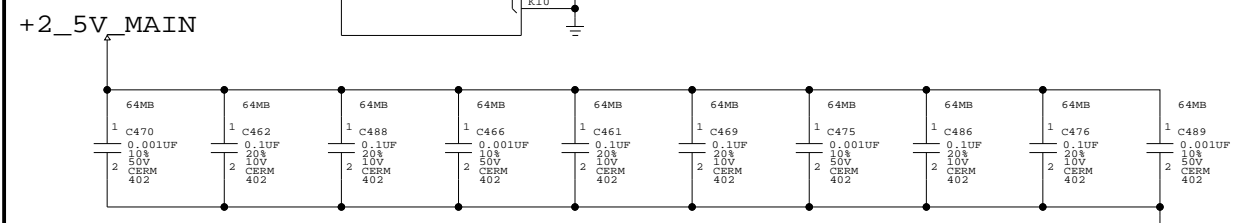
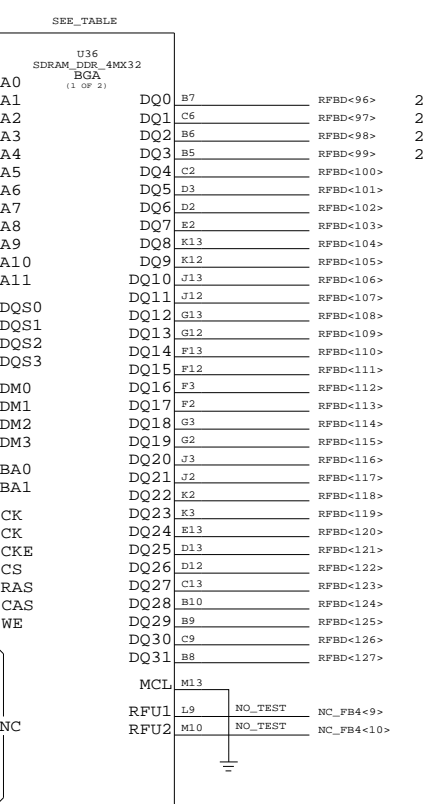
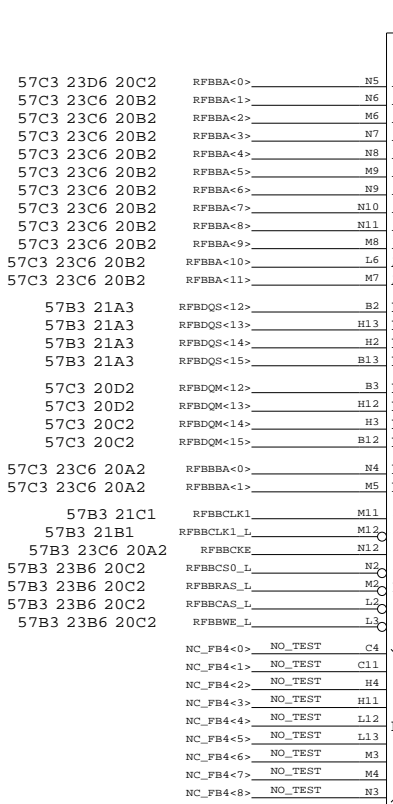
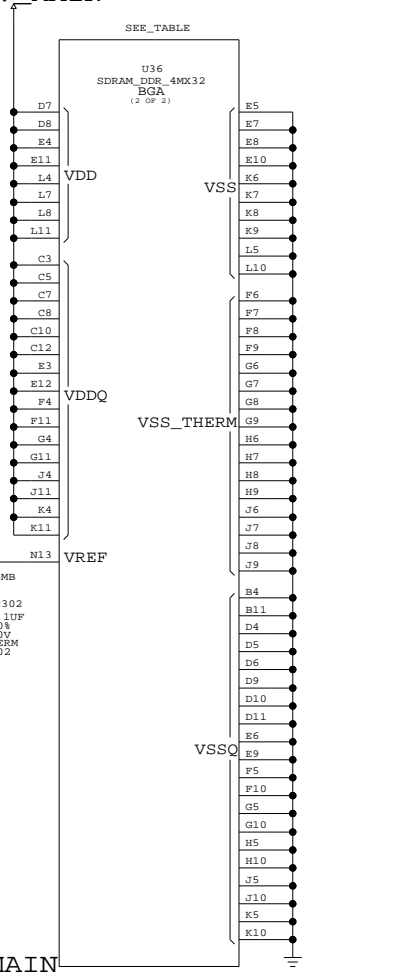
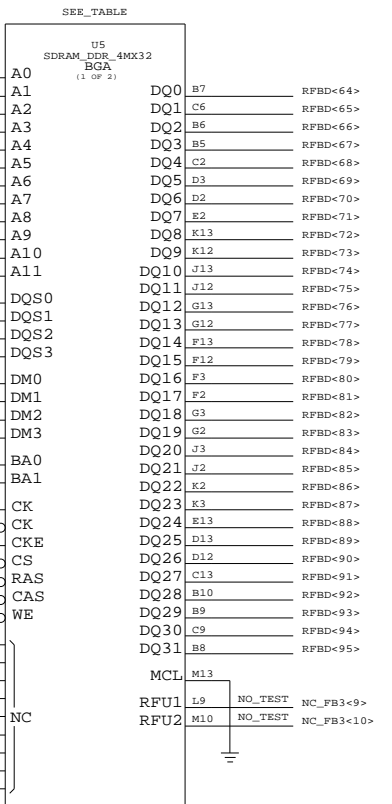
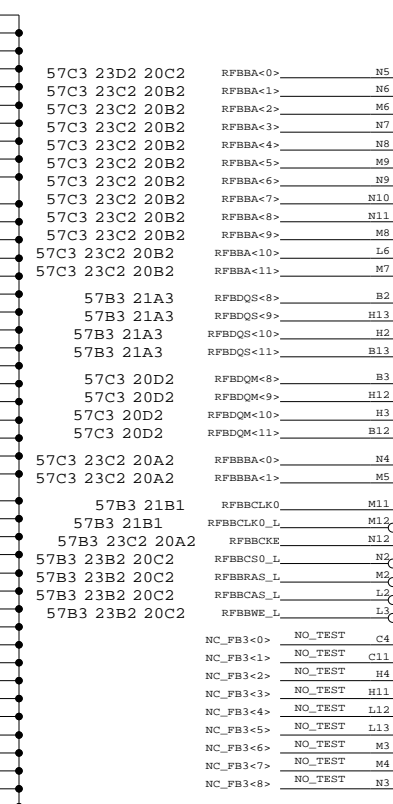
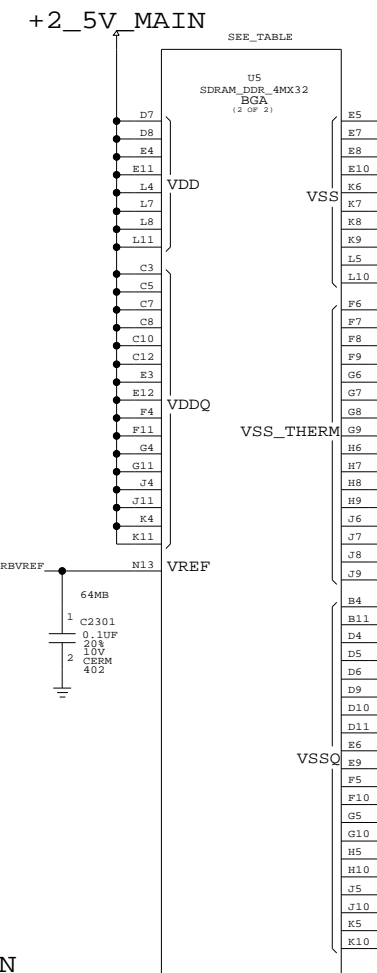
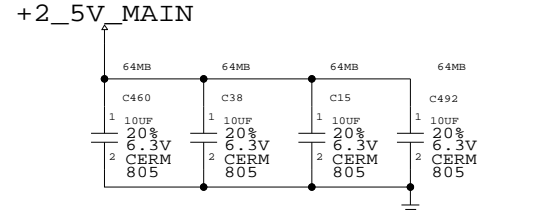
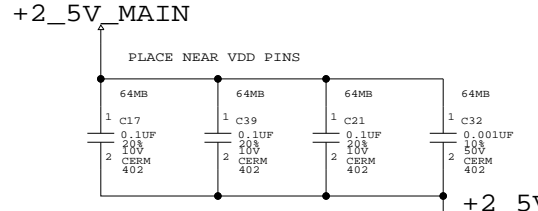
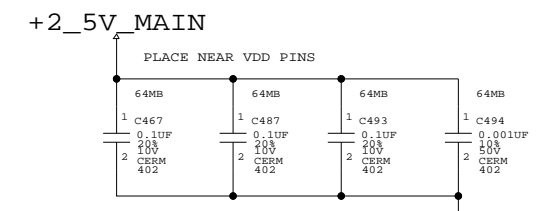


SGRAM0 & SGRAM1

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SCALE: NONE SHT: 22 OF 74



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5, U36	CRITICAL	300_SAMSUNG_64M
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5, U36	CRITICAL	300_HYNIX_64M

SGRAM2 & SGRAM3 DDR MEMORY REFERENCE SUPPORT

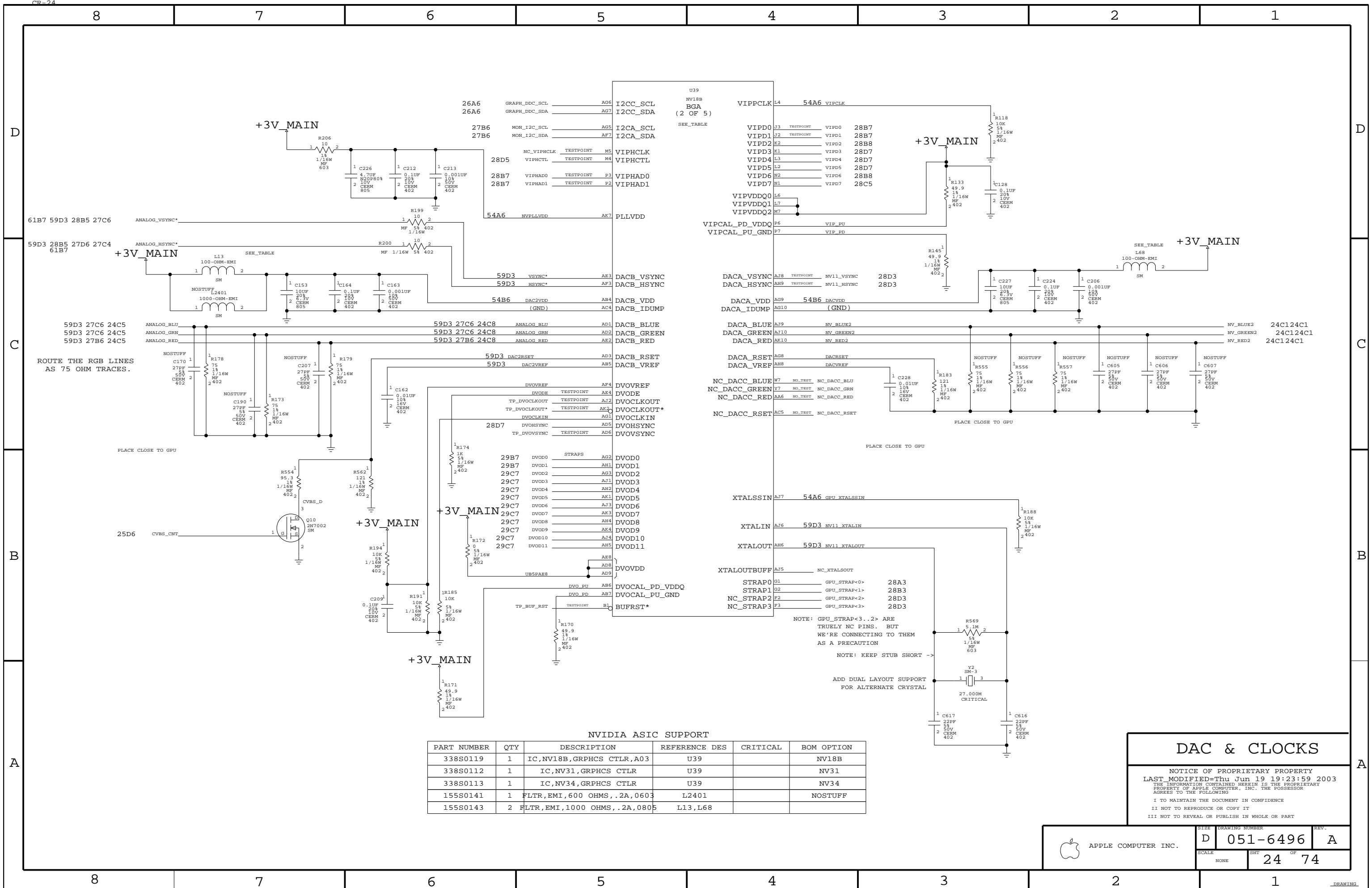
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R18		64MB
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R18		64MB

SGRAM2 & SGRAM3

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D	051-6496	A
SCALE	SHT	OF
NONE	23	74



ROUTE THE RGB LINES AS 75 OHM TRACES.

PLACE CLOSE TO GPU

PLACE CLOSE TO GPU

NOTE: GPU_STRAP<3..2> ARE TRUELY NC PINS. BUT WE'RE CONNECTING TO THEM AS A PRECAUTION
NOTE: KEEP STUB SHORT ->

ADD DUAL LAYOUT SUPPORT FOR ALTERNATE CRYSTAL

NVIDIA ASIC SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0119	1	IC,NV18B,GRPHCS CTLR,A03	U39		NV18B
338S0112	1	IC,NV31,GRPHCS CTLR	U39		NV31
338S0113	1	IC,NV34,GRPHCS CTLR	U39		NV34
155S0141	1	FLTR,EMI,600 OHMS,.2A,0603	L2401		NOSTUFF
155S0143	2	FLTR,EMI,1000 OHMS,.2A,0805	L13,L68		

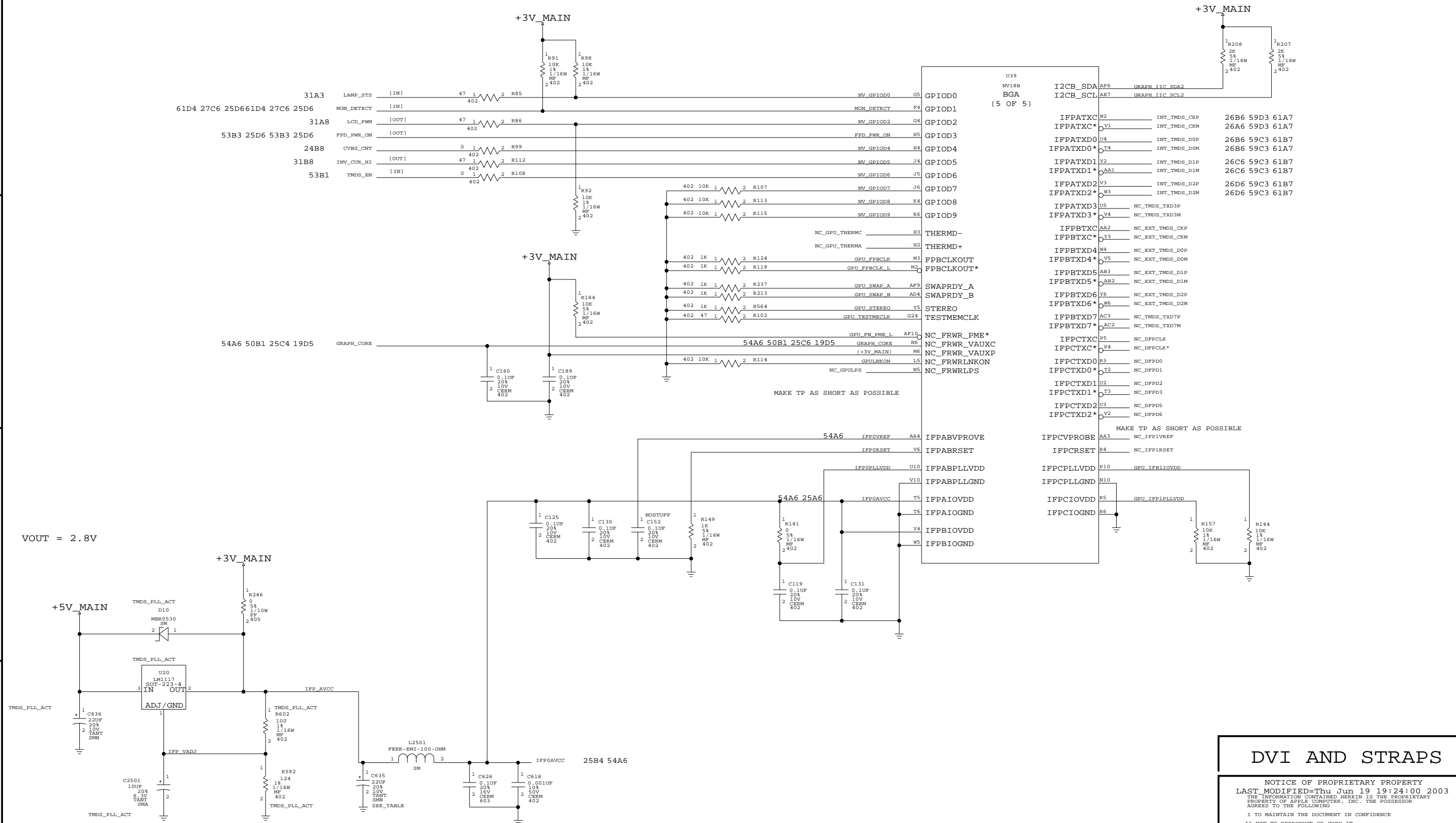
DAC & CLOCKS

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APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-6496	REV.	A
	SCALE	NONE	SHT	24	OF	74

D
C
B
A

D
C
B
A



VOUT = 2.8V

DVI AND STRAPS

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THE STUFFING OF AN 0805 PACKAGE ONTO C635S LARGER TANT PADS IS CORRECT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S1063	1	1UF, 10%, 10V, 0805, CERM	C635		

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6496	A
SCALE	SHT	OF
NONE	25	74

D

D

C

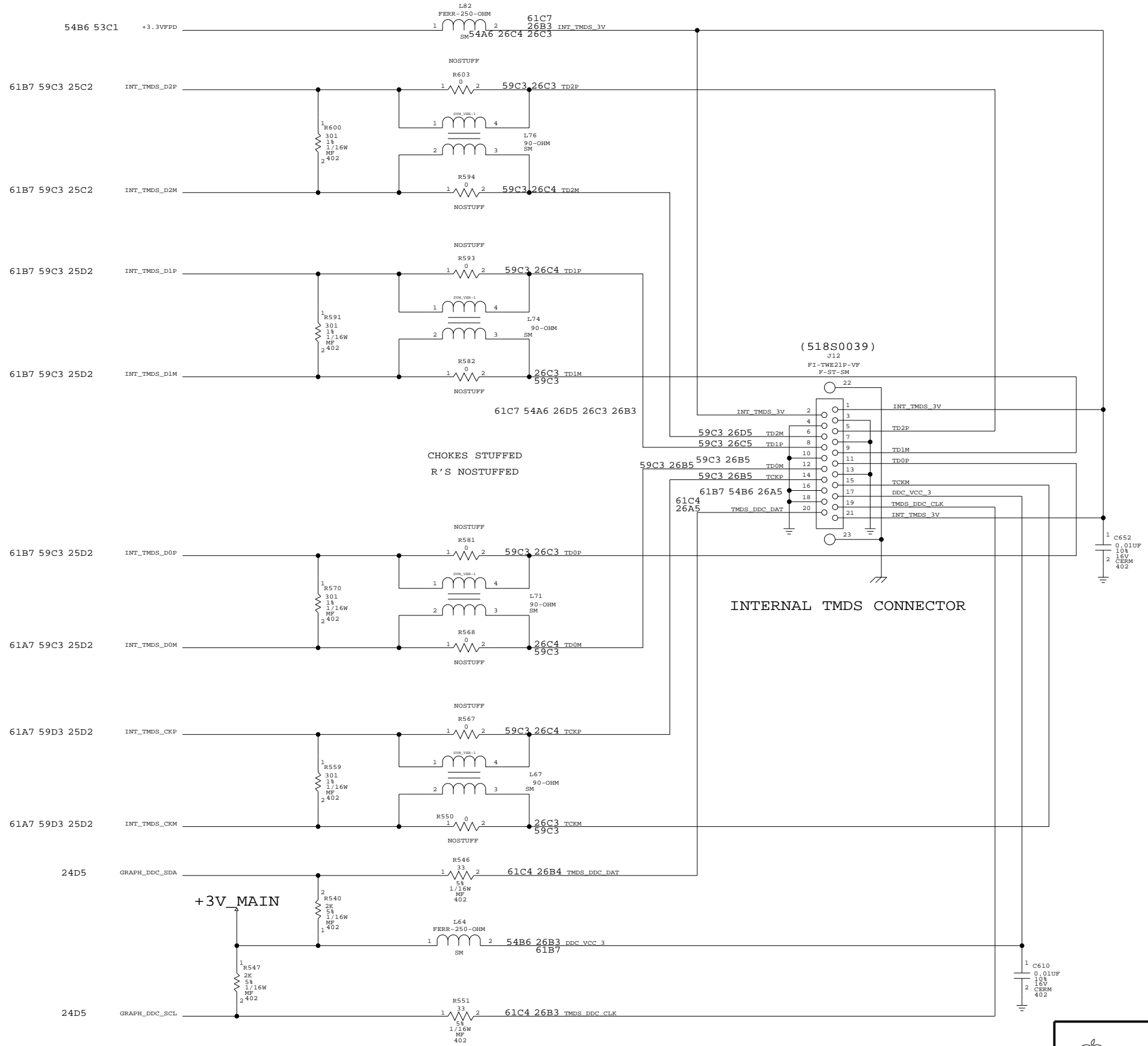
C

B

B

A

A



TMDS

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	APPLE COMPUTER INC.		SIZE	DRAWING NUMBER	REV.
			NONE	051-6496	A
			SCALE	SHT	OF
				26	74

D

C

B

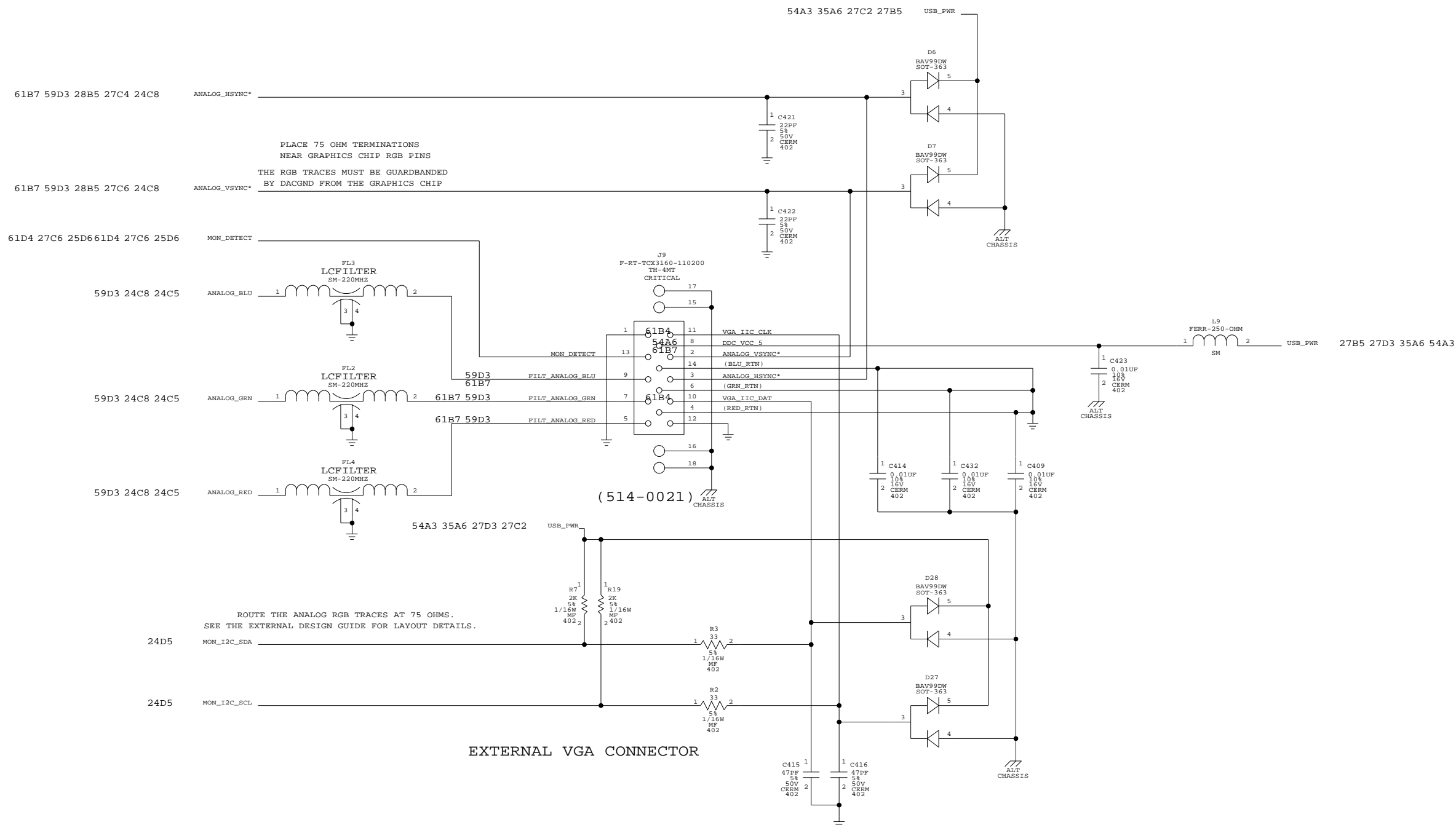
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D

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EXTERNAL VGA

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	SIZE D SCALE NONE	DRAWING NUMBER 051-6496	REV. A
	SHEET 27 OF 74		

D

D

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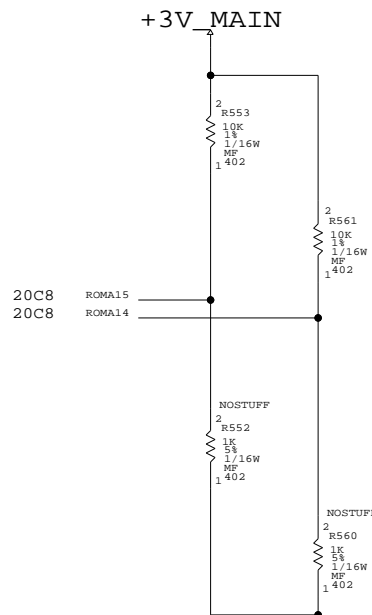
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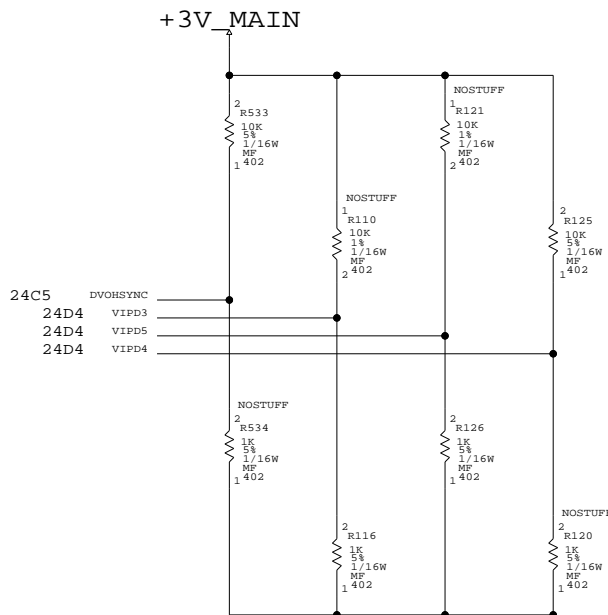
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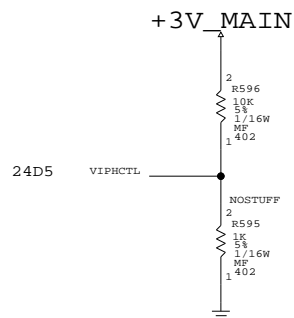
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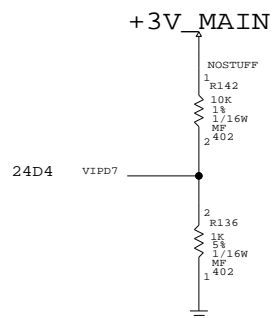
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
 [1..0] = [ROMA15,ROMA14]
 00 = PARALLEL
 01 = SERIAL AT25F
 10 = SERIAL SST45VF
 * 11 = SERIAL FUTURE



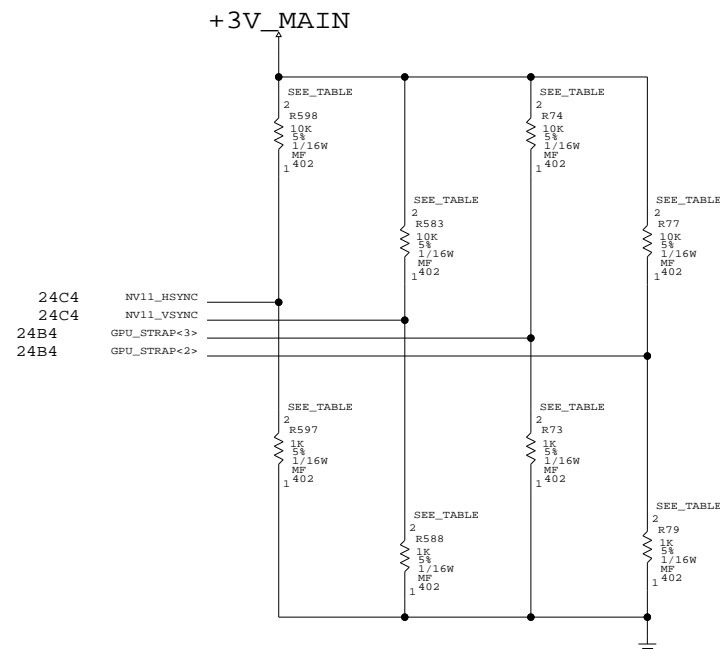
(3) PCI DEVICE ID
 [3..0] = [DVOHSYNC, VIPD3, VIPD5, VIPD4]
 0010 = 0X112 GEFORCE2 GO
 0011 = 0X113 QUADRO2 GO
 0100 = 0X114 NV17M
 0000 = 0X110 GEFORCE2GO MX (NV11B)
 * 1001 = NV18B, NV31, NV34



(5) HOST MODE
 [0] = [VIPHCTL]
 0 = PCI MODE
 * 1 = AGP MODE

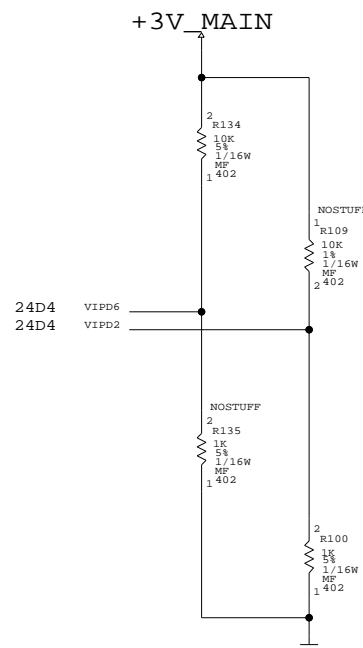


(6) AGP SIDEBAND
 [0] = [VIPD7]
 * 0 = ENABLE AGP SIDEBAND
 1 = DISABLE AGP SIDEBAND

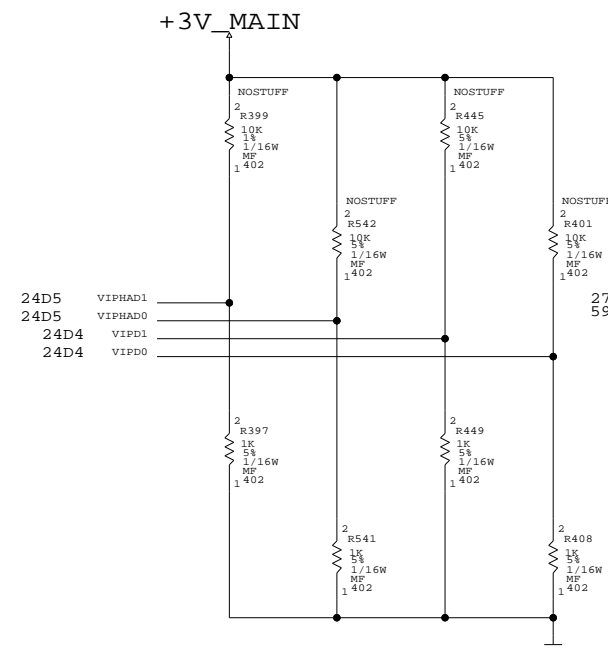


(8) FRAME BUFFER MEMORY TYPE
 [3..0] = [NV11_HSYNC, NV11_VSYNC, GPU_STRAP<3>, GPU_STRAP<2>]
 1111 = 222MHZ
 1101 = 275MHZ SAMSUNG
 1100 = 275MHZ HYNIX

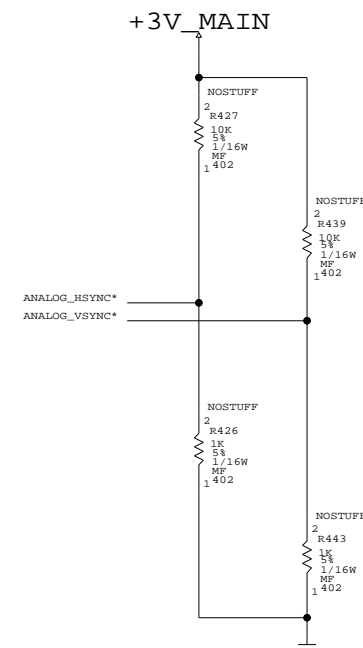
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1104	3	RES, 10KOHM, 5%, 0402	R598, R583, R77		275_SAMSUNG
116S1103	1	RES, 1KOHM, 5%, 0402	R73		275_SAMSUNG
116S1104	2	RES, 10KOHM, 5%, 0402	R598, R583		275_HYNIX
116S1103	2	RES, 1KOHM, 5%, 0402	R73, R79		275_HYNIX
116S1104	3	RES, 10KOHM, 5%, 0402	R596, R583, R77		300_SAMSUNG_32M
116S1103	1	RES, 1KOHM, 5%, 0402	R73		300_SAMSUNG_32M
116S1104	2	RES, 10KOHM, 5% 0402	R598, R583		300_HYNIX_32M
116S1103	2	RES, 1KOHM, 5% 0402	R73, R79		300_HYNIX_32M



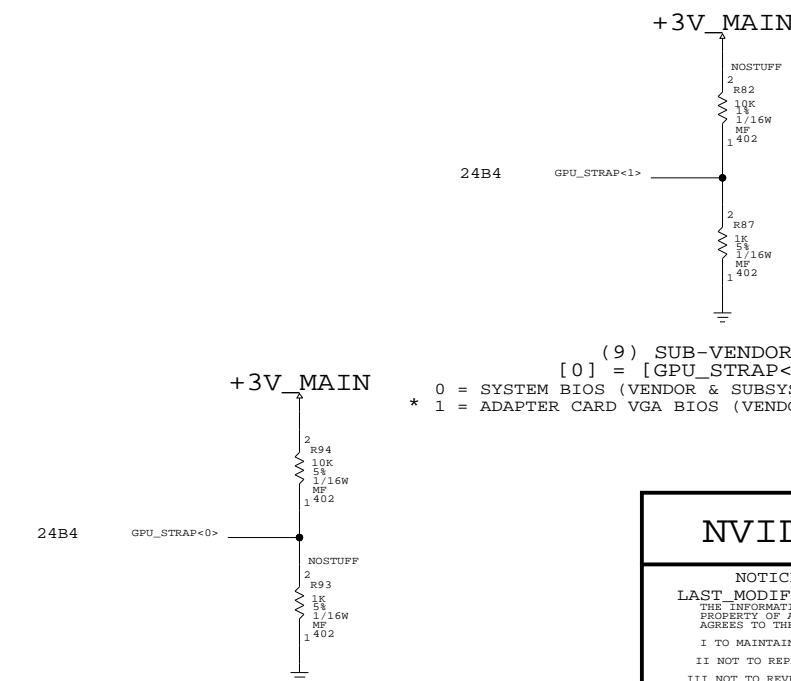
(2) CRYSTAL FREQUENCY SELECT
 [1..0] = [VIPD6, VIPD2]
 00 = 13.5MHZ
 01 = 14.38MHZ
 * 10 = 27MHZ
 11 = {UNDEFINED}



(4) USER DEFINED STRAPS
 [3..0] = [VIPHAD1, VIPHAD0, VIPD1, VIPD0]
 THESE BITS ARE UNDEFINED BUT THEY
 MUST BE KEPT LOW DURING RESET



(7) TV MODE
 [1..0] = [ANALOG_HSYNC*, ANALOG_VSYNC*]
 00 = SECAM
 01 = NTSC
 10 = PAL
 * 11 = DISABLED
 (THESE RESISTORS ARE ALL NOSTUFF)



(9) SUB-VENDOR
 [0] = [GPU_STRAP<1>]
 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
 * 1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)

(10) PCI ADDRESS BUS
 [0] = [GPU_STRAP<0>]
 0 = REVERSED
 * 1 = NORMAL

NVIDIA STRAPS 1

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D	051-6496	A
SCALE	SHT	OF
NONE	28	74

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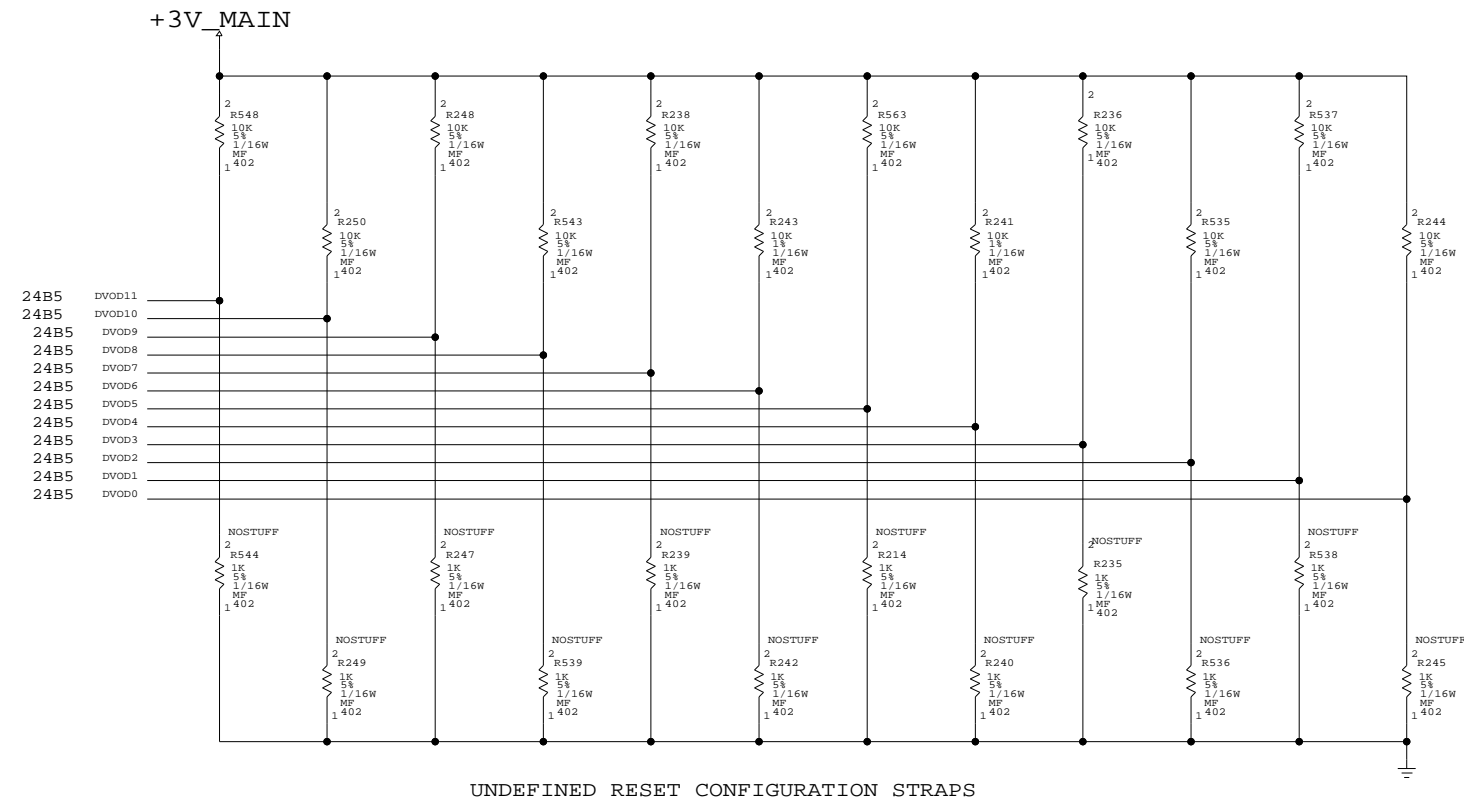
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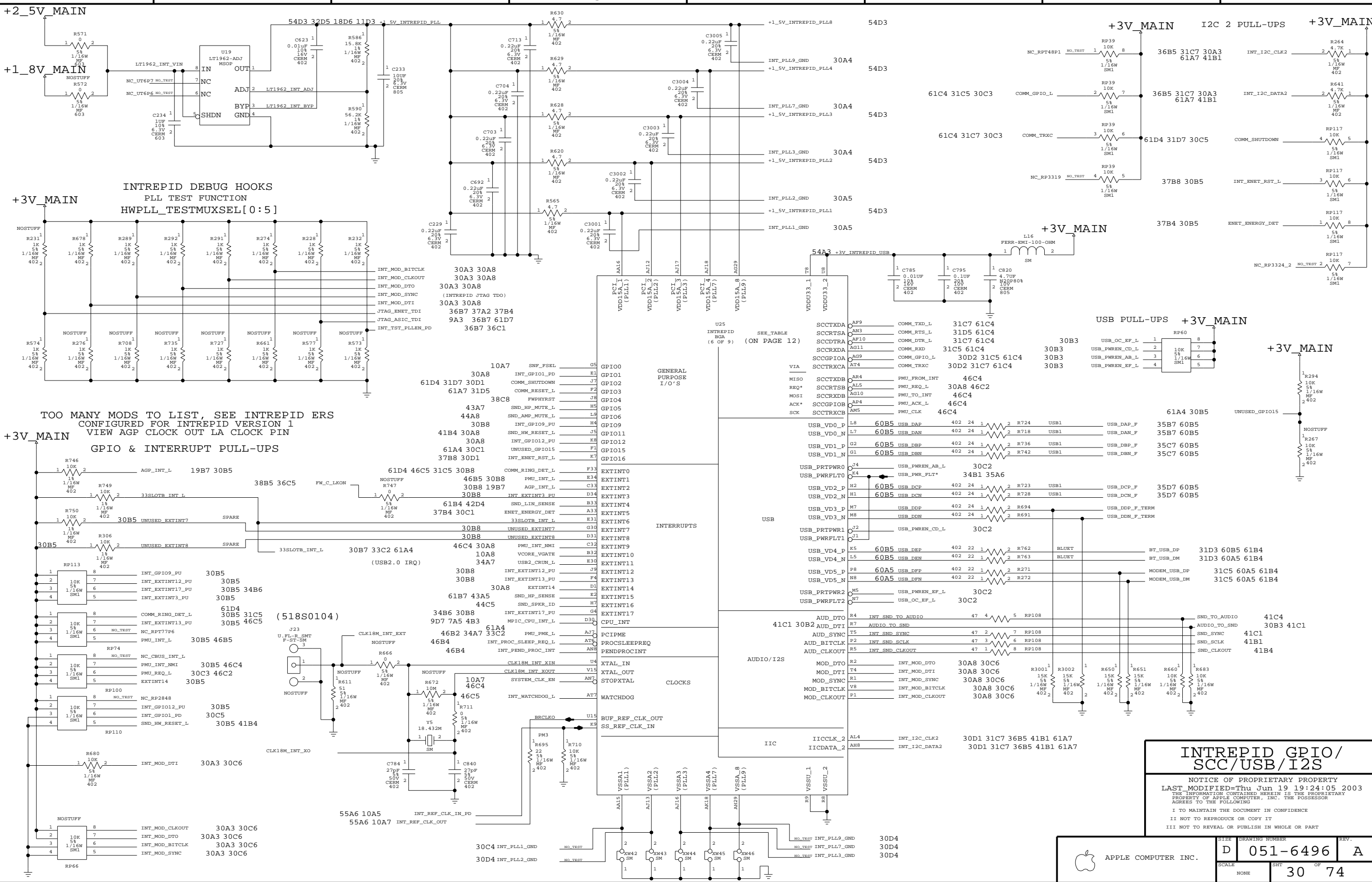
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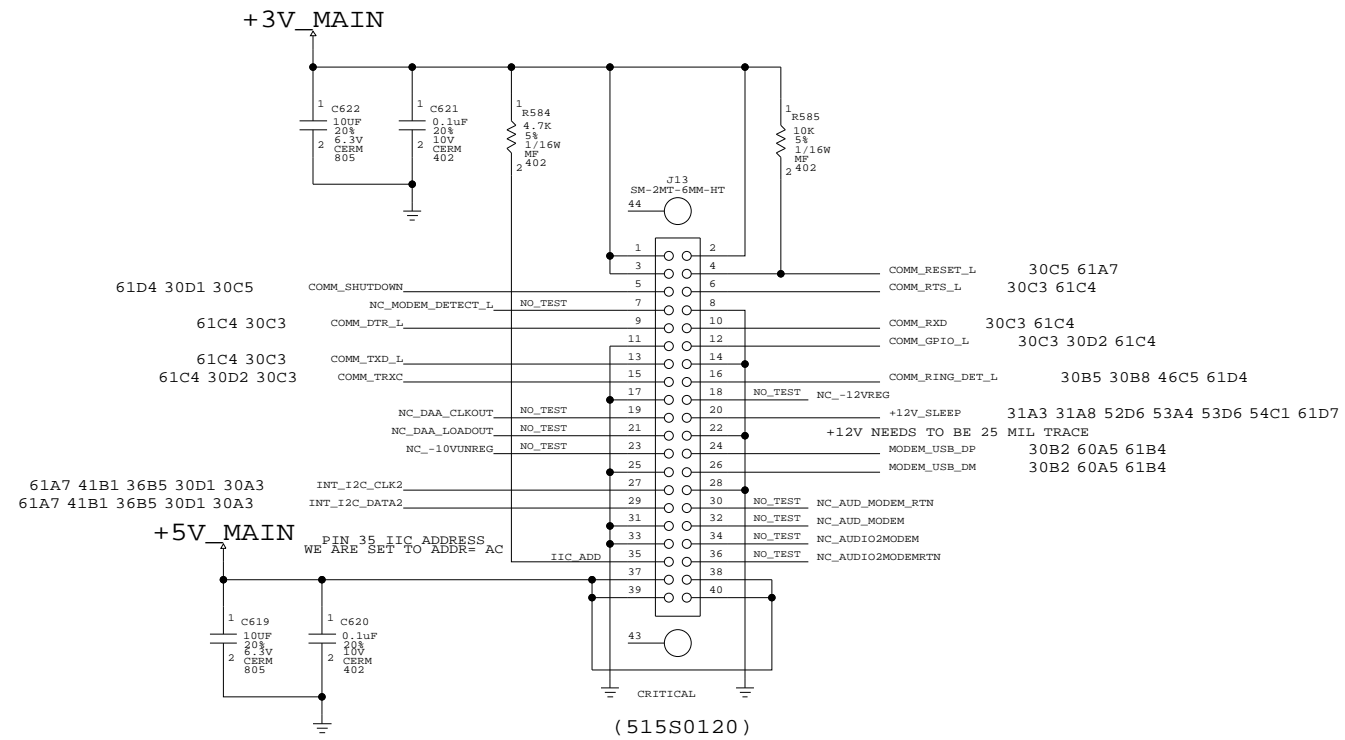
NVIDIA STRAPS 2

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SCALE	SHT		OF
NONE	29		74



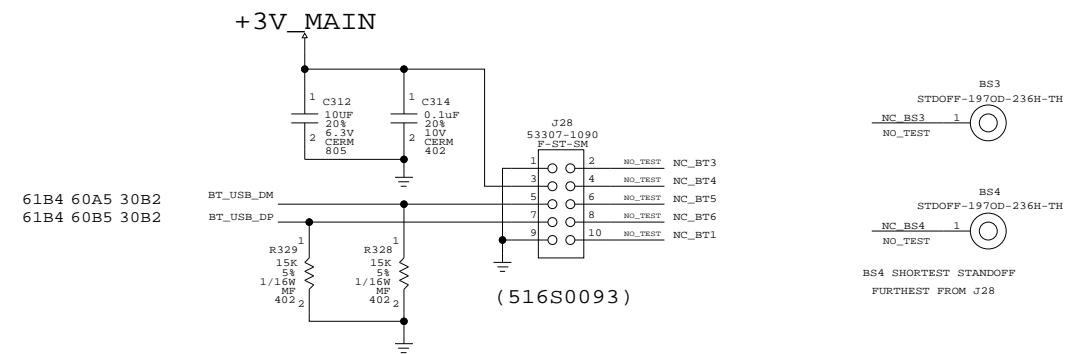
MODEM BOARD CONNECTOR
(DASH II)



MODEM STANDOFF SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1034	2	STDOFF-19709-236H-TH	BS1, BS2		

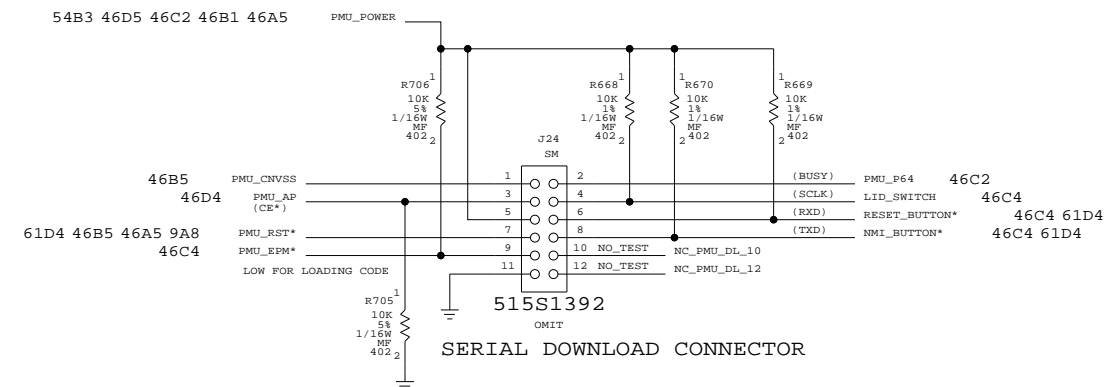
BLUETOOTH CONNECTOR



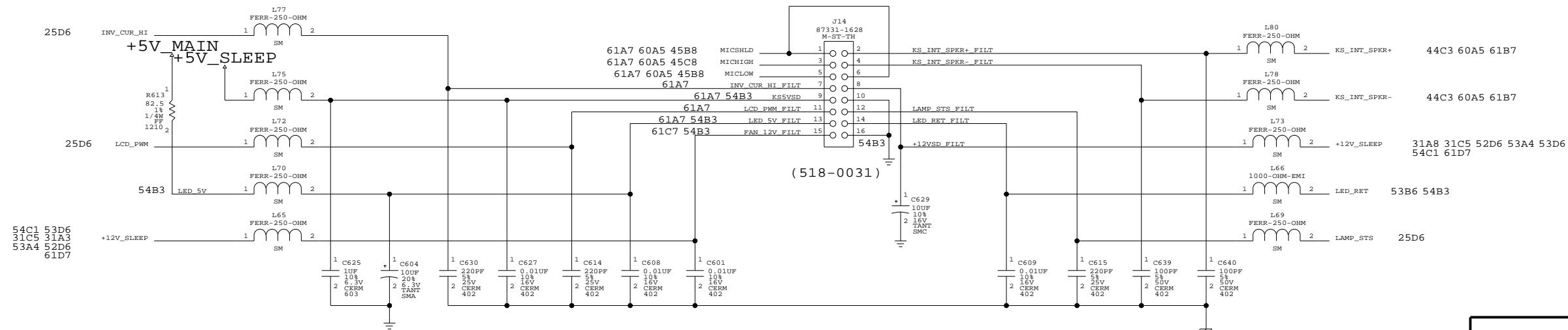
BLUETOOTH CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-0170	1	STDOFF, BLUETOOTH, SHORT	BS4		
860-0171	1	STDOFF, BLUETOOTH, LONG	BS3		

SERIAL DOWNLOAD INTERFACE



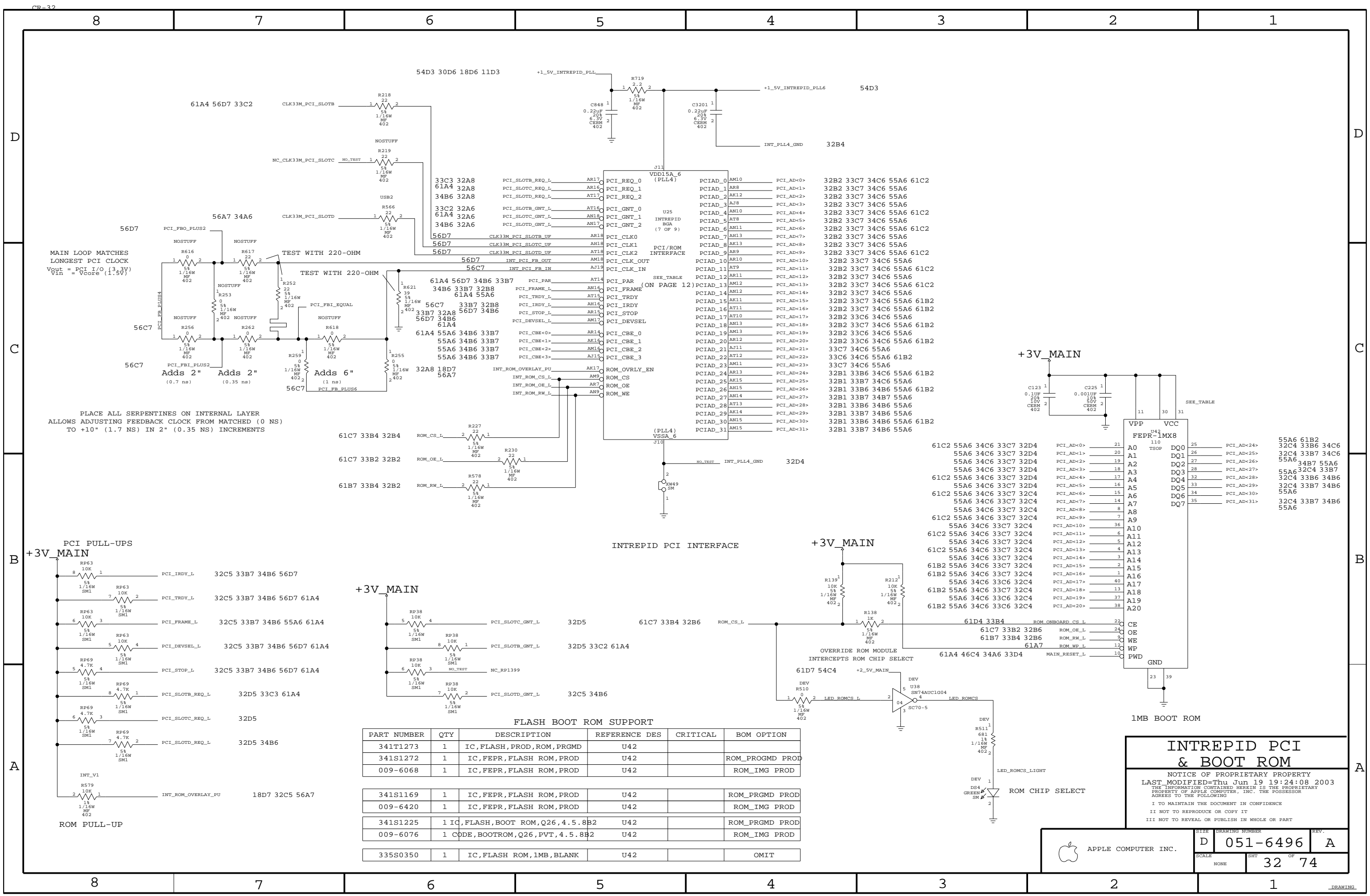
'KITCHEN SINK' CONNECTOR
(MICROPHONE, INTERNAL SPEAKER CONNECTIONS
INVERTER, LCD, LED & FAN POWER)



MODEM, BLUETOOTH,
KITCHEN SINK
& SERIAL DOWNLOAD

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SCALE		SHT	OF
		31	74



FLASH BOOT ROM SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341T1273	1	IC, FLASH, PROD, ROM, PRGMD	U42		
341S1272	1	IC, FEPR, FLASH ROM, PROD	U42		ROM_PROGMD PROD
009-6068	1	IC, FEPR, FLASH ROM, PROD	U42		ROM_IMG PROD
341S1169	1	IC, FEPR, FLASH ROM, PROD	U42		ROM_PROGMD PROD
009-6420	1	IC, FEPR, FLASH ROM, PROD	U42		ROM_IMG PROD
341S1225	1	IC, FLASH, BOOT ROM, Q26, 4.5.8B2	U42		ROM_PROGMD PROD
009-6076	1	CODE, BOOTROM, Q26, PVT, 4.5.8B2	U42		ROM_IMG PROD
335S0350	1	IC, FLASH ROM, 1MB, BLANK	U42		OMIT

INTREPID PCI & BOOT ROM

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	SCALE NONE SHEET 32 OF 74

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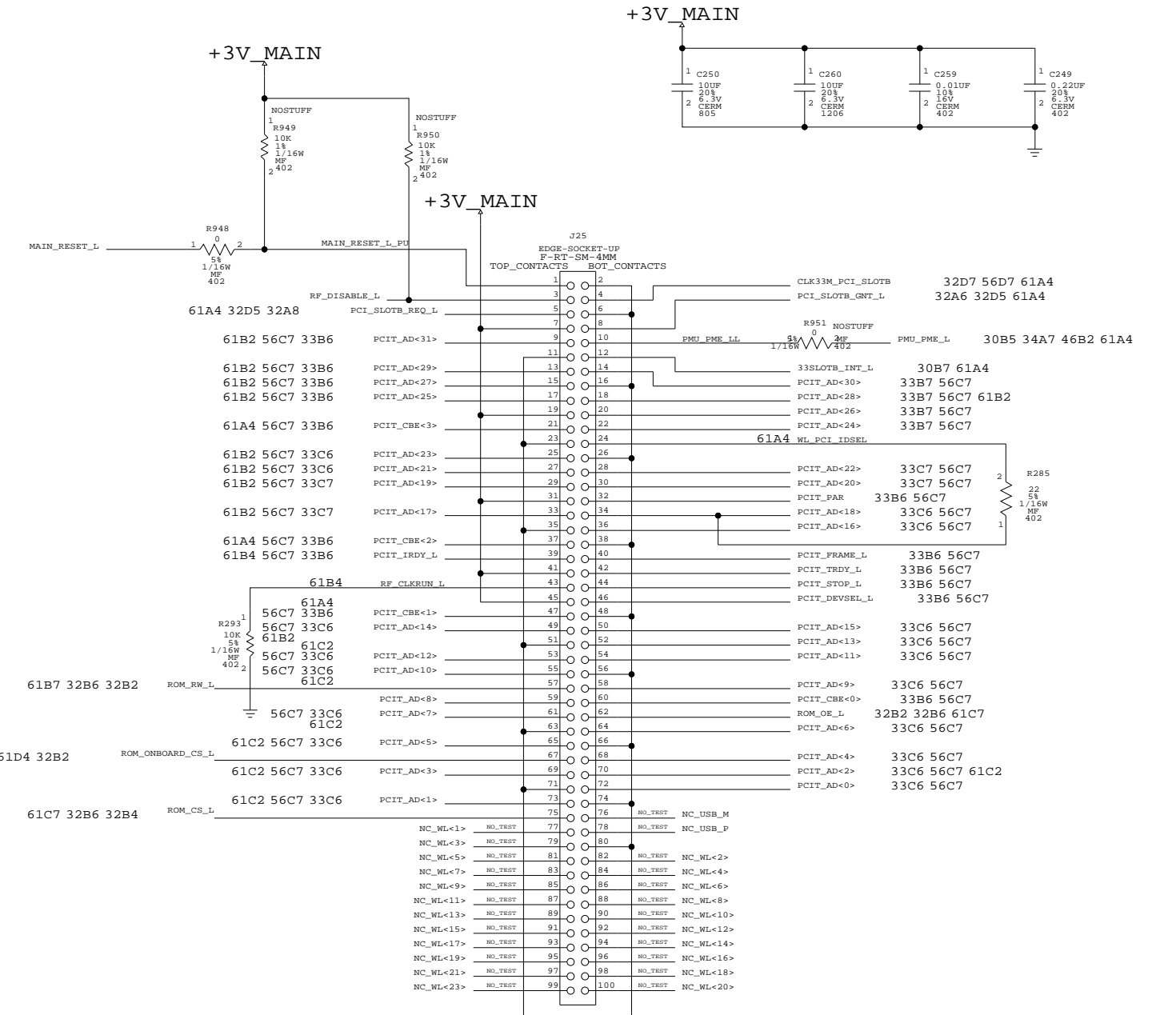
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PLACE RP'S NEAR WIRELESS CONNECTOR

61C2	55A6	34C6	32D4	32B2	PCI_AD<0>	1	RP77	8	PCI_AD<0>	33B2	56C7
	55A6	34C6	32D4	32B2	PCI_AD<1>	2	33	7	PCI_AD<1>	33B3	56C7
	55A6	34C6	32D4	32B2	PCI_AD<2>	3	58	6 NO_TEST	PCI_AD<2>	33B2	56C7
	55A6	34C6	32D4	32B2	PCI_AD<3>	4	SM1	5	PCI_AD<3>	33B3	56C7
61C2	55A6	34C6	32D4	32B2	PCI_AD<4>	1	RP75	8	PCI_AD<4>	33B2	56C7
	55A6	34C6	32D4	32B2	PCI_AD<5>	2	33	7	PCI_AD<5>	33B3	56C7
	55A6	34C6	32C4	32B2	PCI_AD<6>	3	58	6 NO_TEST	PCI_AD<6>	33B2	56C7
	55A6	34C6	32C4	32B2	PCI_AD<7>	4	SM1	5	PCI_AD<7>	33B3	56C7
61C2	55A6	34C6	32C4	32B2	PCI_AD<8>	1	RP73	8	PCI_AD<8>	33B3	56C7
	55A6	34C6	32C4	32B2	PCI_AD<9>	2	33	7 NO_TEST	PCI_AD<9>	33B2	56C7
	55A6	34C6	32C4	32B2	PCI_AD<10>	3	58	6	PCI_AD<10>	33B3	56C7
	55A6	34C6	32C4	32B2	PCI_AD<11>	4	SM1	5 NO_TEST	PCI_AD<11>	33B2	56C7
61C2	55A6	34C6	32C4	32B2	PCI_AD<12>	1	RP72	8	PCI_AD<12>	33B3	56C7
	55A6	34C6	32C4	32B2	PCI_AD<13>	2	33	7 NO_TEST	PCI_AD<13>	33B2	56C7
	55A6	34C6	32C4	32B2	PCI_AD<14>	3	58	6	PCI_AD<14>	33C3	56C7
	55A6	34C6	32C4	32B2	PCI_AD<15>	4	SM1	5 NO_TEST	PCI_AD<15>	33C2	56C7
61B2	55A6	34C6	32C4	32B2	PCI_AD<16>	1	RP59	8	PCI_AD<16>	33C2	56C7
	61B2	56C7	33C3		PCI_AD<17>	2	33	7	PCI_AD<17>	32B2	32C4
	61B2	56C7	33C3		PCI_AD<18>	3	58	6	PCI_AD<18>	33C2	56C7
	61B2	56C7	33C3		PCI_AD<19>	4	SM1	5	PCI_AD<19>	32B2	32C4
	55A6	34C6	32C4		PCI_AD<23>	1	RP58	8	PCI_AD<23>	33C3	56C7
	55A6	34C6	32C4		PCI_AD<21>	2	33	7	PCI_AD<21>	33C3	56C7
	56C7	33C2			PCI_AD<22>	3	58	6	PCI_AD<22>	32C4	34C6
	56C7	33C2			PCI_AD<20>	4	SM1	5	PCI_AD<20>	32B2	32C4
55A6	34B7	32C4	32B1		PCI_AD<27>	1	RP56	8	PCI_AD<27>	33C3	56C7
	55A6	34C6	32C4	32B1	PCI_AD<25>	2	33	7	PCI_AD<25>	33C3	56C7
	56C7	33C2			PCI_AD<26>	3	58	6	PCI_AD<26>	32B1	32C4
	56C7	33C2			PCI_AD<24>	4	SM1	5	PCI_AD<24>	32B1	32C4
61B2	56C7	33C2			PCI_AD<28>	1	RP54	8	PCI_AD<28>	32B1	32C4
	56C7	33C2			PCI_AD<30>	2	33	7	PCI_AD<30>	32B1	32C4
	55A6	34B6	32C4	32B1	PCI_AD<31>	3	58	6	PCI_AD<31>	33C3	56C7
	55A6	34B6	32C4	32B1	PCI_AD<29>	4	SM1	5	PCI_AD<29>	33C3	56C7
	61A4	56D7	34B6	32C5	PCI_PAR	1	RP61	8	PCI_PAR	33C2	56C7
61A4	55A6	34B6	32C5	32B8	PCI_FRAME_L	2	33	7 NO_TEST	PCI_FRAME_L	33C2	56C7
	61A4	56D7	34B6	32C5	PCI_TRDY_L	3	58	6 NO_TEST	PCI_TRDY_L	33C2	56C7
	56D7	34B6	32C5	32B8	PCI_IRDY_L	4	SM1	5 NO_TEST	PCI_IRDY_L	33C3	56C7
61A4	56D7	34B6	32C5	32A8	PCI_STOP_L	1	RP67	8	PCI_STOP_L	33C2	56C7
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	55A6	34B6	32C5		PCI_CBE<1>	3	58	6	PCI_CBE<1>	33C3	56C7
	61A4	55A6	34B6	32C5	PCI_CBE<0>	4	SM1	5 NO_TEST	PCI_CBE<0>	33B2	56C7
	55A6	34B6	32C5		PCI_CBE<2>	1	RP64	8	PCI_CBE<2>	33C3	56C7
	55A6	34B6	32C5		PCI_CBE<3>	2	33	7	PCI_CBE<3>	33C3	56C7
	NC_PCIR0	NO_TEST	3	1/16W	NO_TEST	3	58	6 NO_TEST	NC_PCITR0		
	NC_PCIR1	NO_TEST	4	SM1	NO_TEST	4	SM1	5 NO_TEST	NC_PCITR1		

61A4 46C4 34A6 32A2



(516S0046)

WIRELESS CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
815-7245	1	WIRELESS CARD GUIDE, J25	J251		
452-0411	2	NUT, HEX, M2 X 1.5H, J25	J252, J253		
452-0412	2	SCREW, M2 X 0.4 X 6.0 L, J25	J254, J255		

WIRELESS PCI

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SCALE	NONE	SHT	33	OF	74

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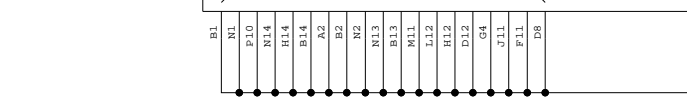
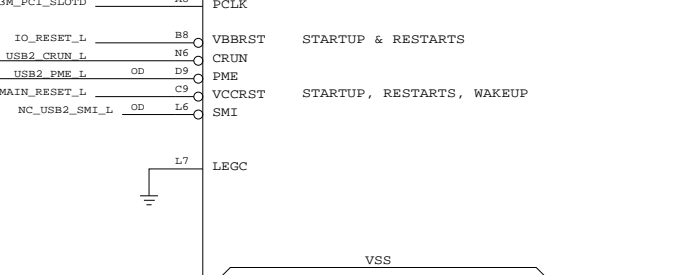
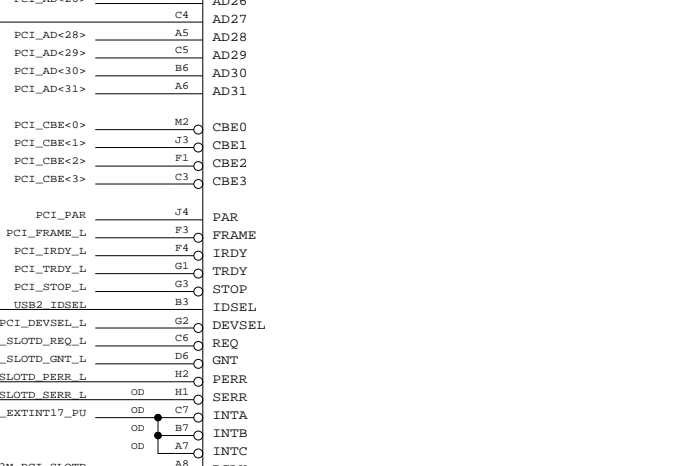
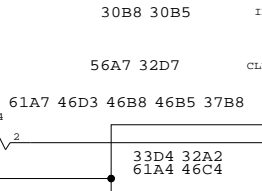
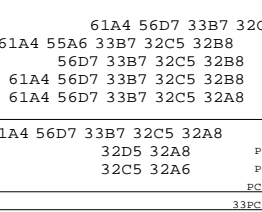
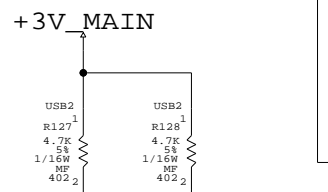
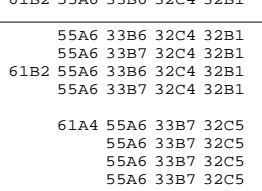
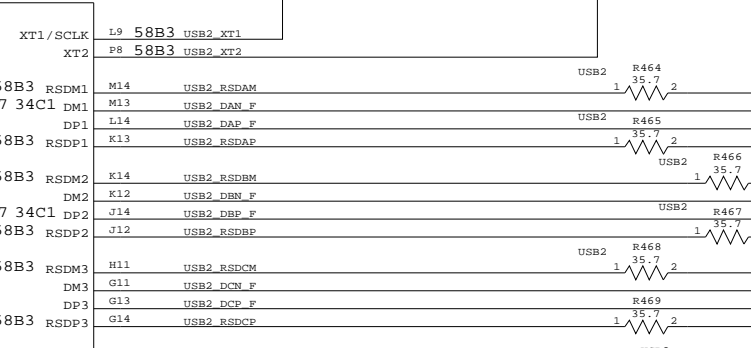
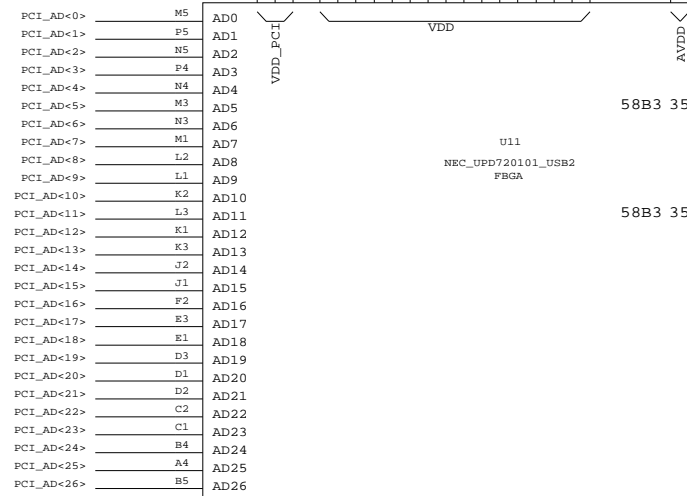
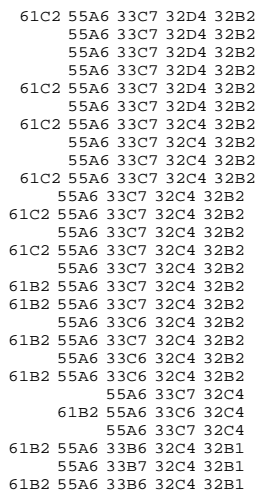
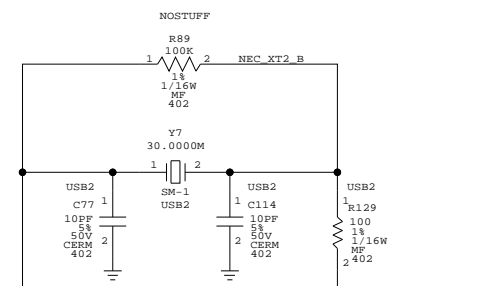
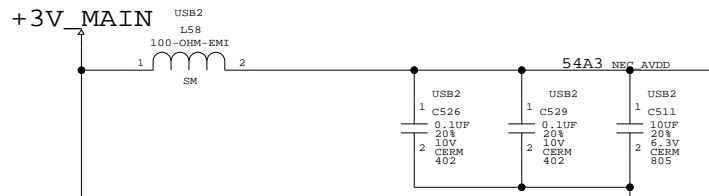
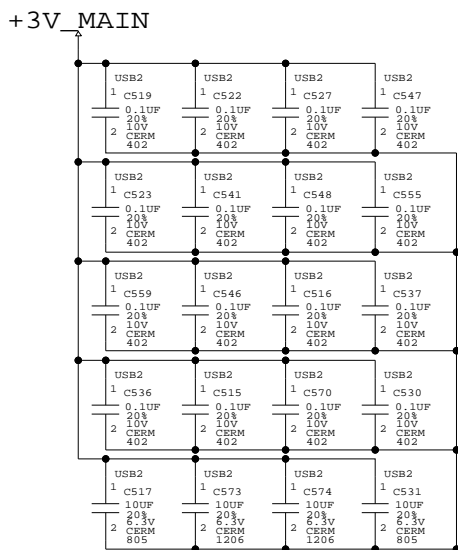
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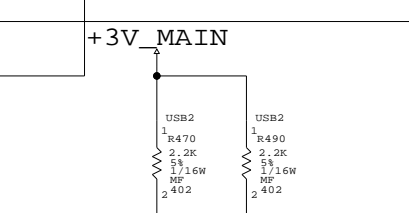
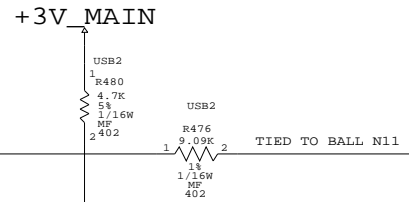
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OVERLAP STUFFING OF 35.7OHMS HERE WITH 0OHMS ON SH31 TO MINIMIZE STUBS

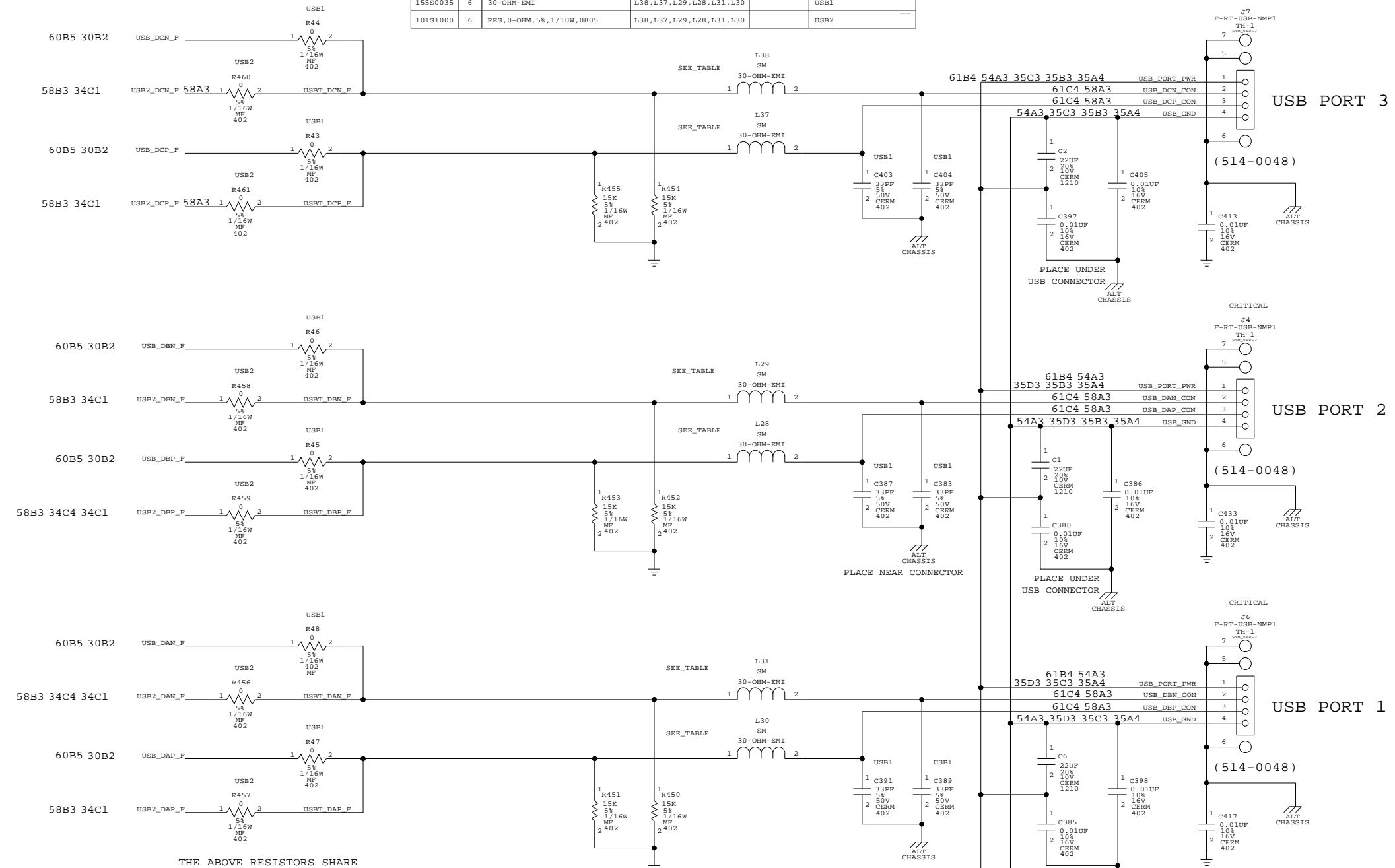


USB2 CONTROLLER

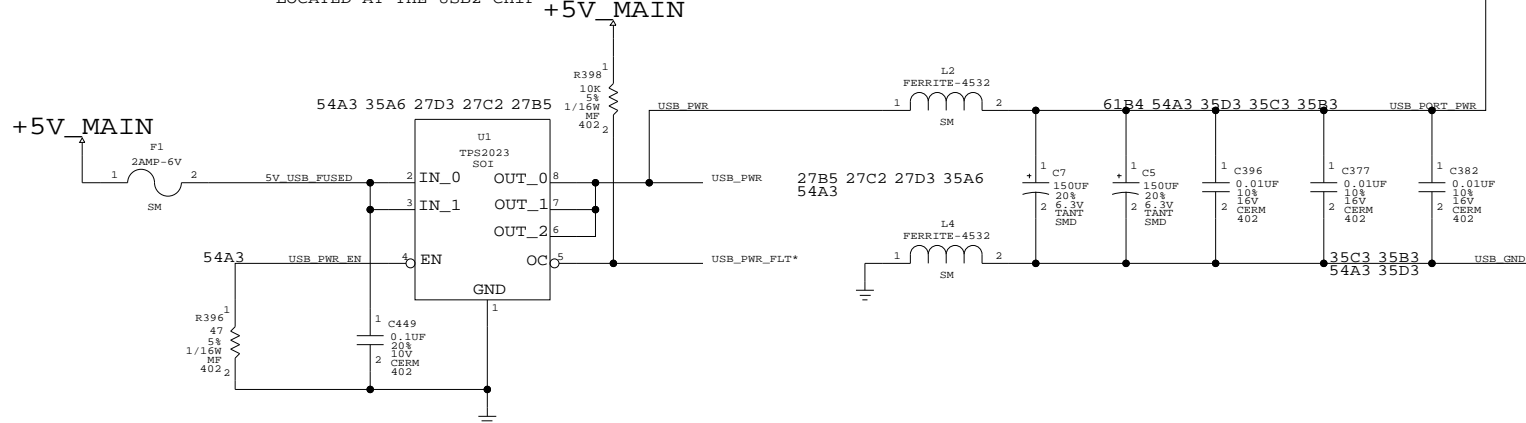
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	SCALE	NONE	SHT	34	OF	74

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0035	6	30-OHM-EMI	L38, L37, L29, L28, L31, L30		USB1
101S1000	6	RES, 0-OHM, 5%, 1/10W, 0805	L38, L37, L29, L28, L31, L30		USB2



THE ABOVE RESISTORS SHARE THE SAME PIN-2 PAD AND ARE LOCATED AT THE USB2 CHIP



USB CONNS & PWR

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	NONE	051-6496	A
SCALE		SHT	OF
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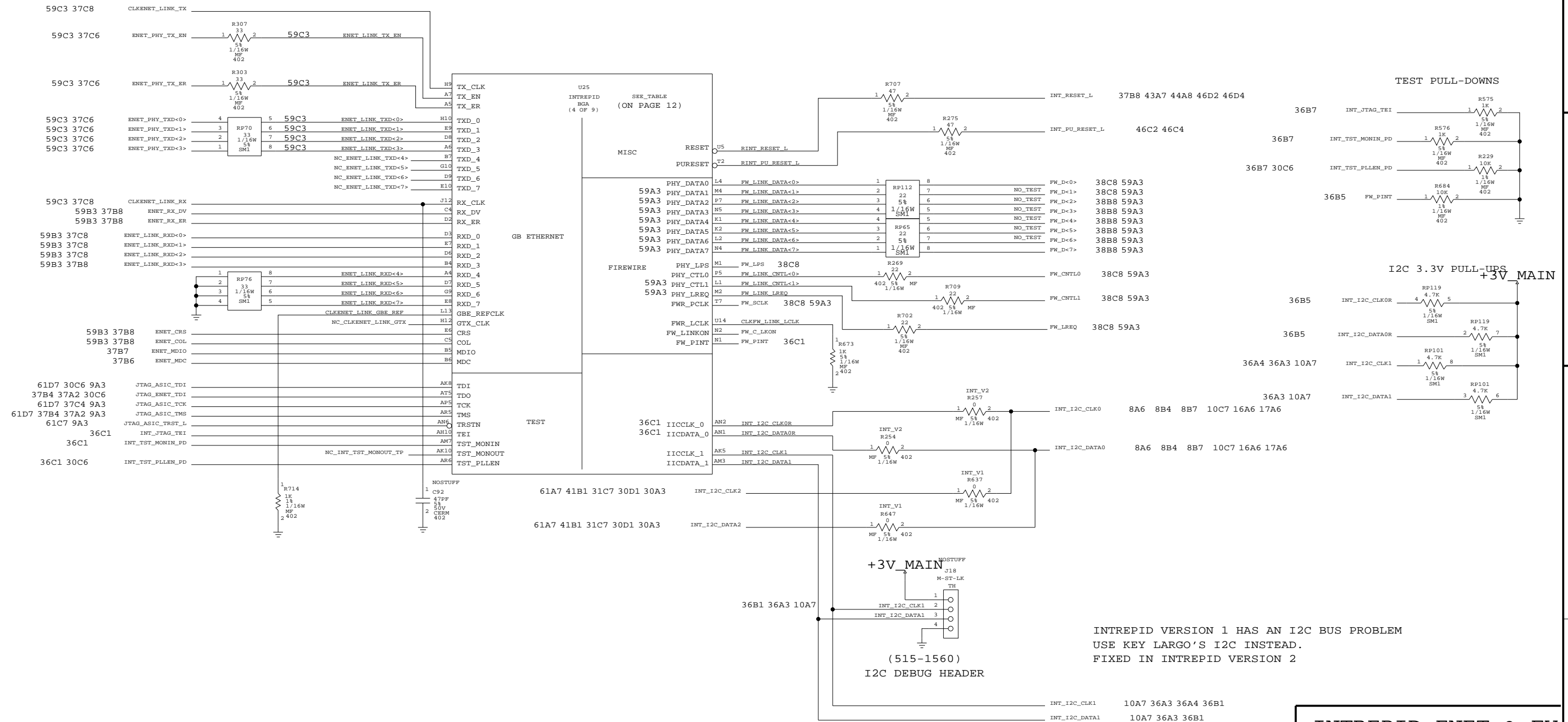
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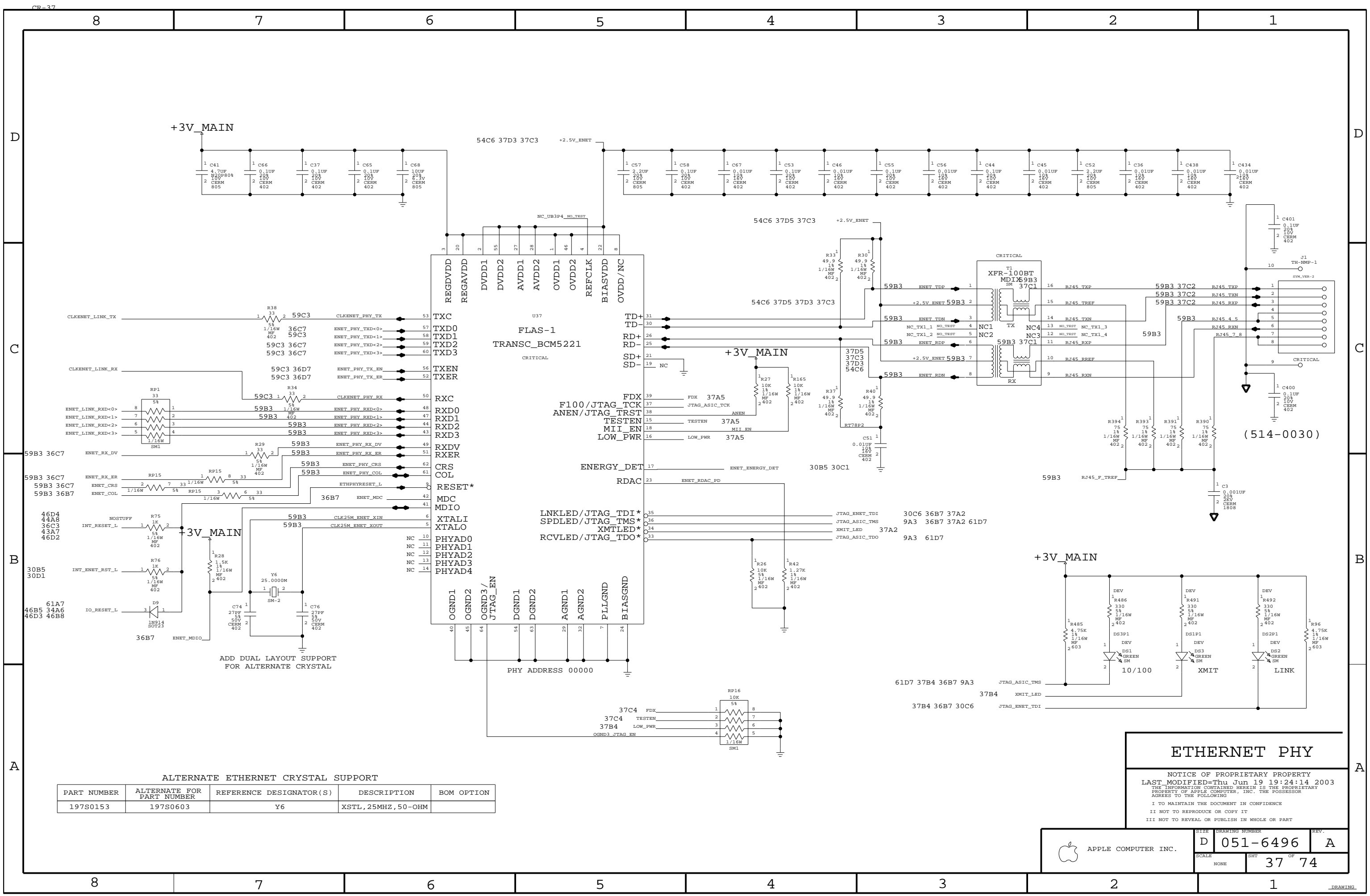
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INTREPID ENET & FW

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	SCALE	NONE	SHT	36	OF	74



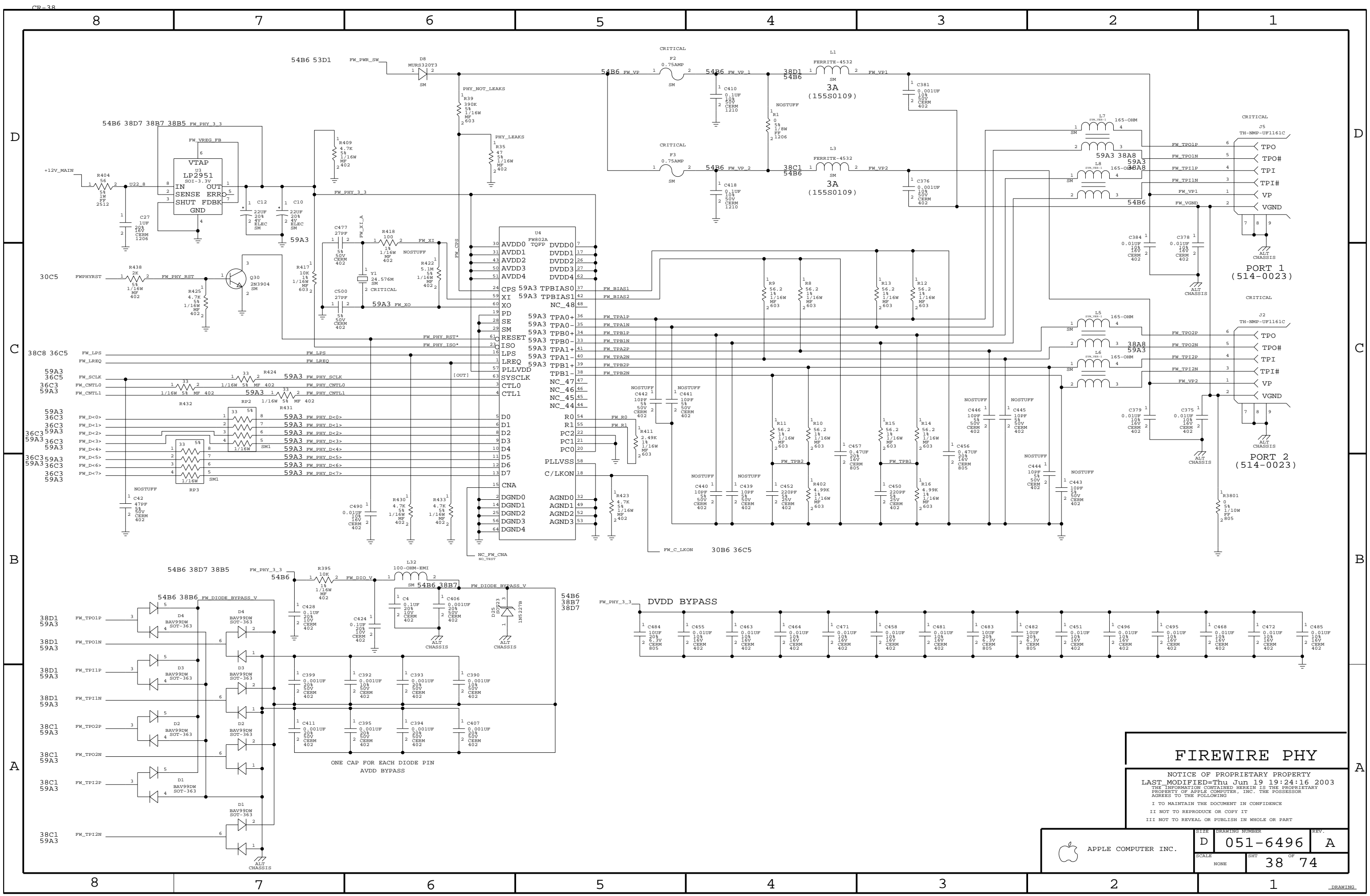
ALTERNATE ETHERNET CRYSTAL SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S0153	197S0603	Y6	XSTL, 25MHZ, 50-OHM	

ETHERNET PHY

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	SCALE: NONE	SHEET: 37	OF: 74



FIREWIRE PHY

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	SCALE NONE	SHEET 38	OF 74

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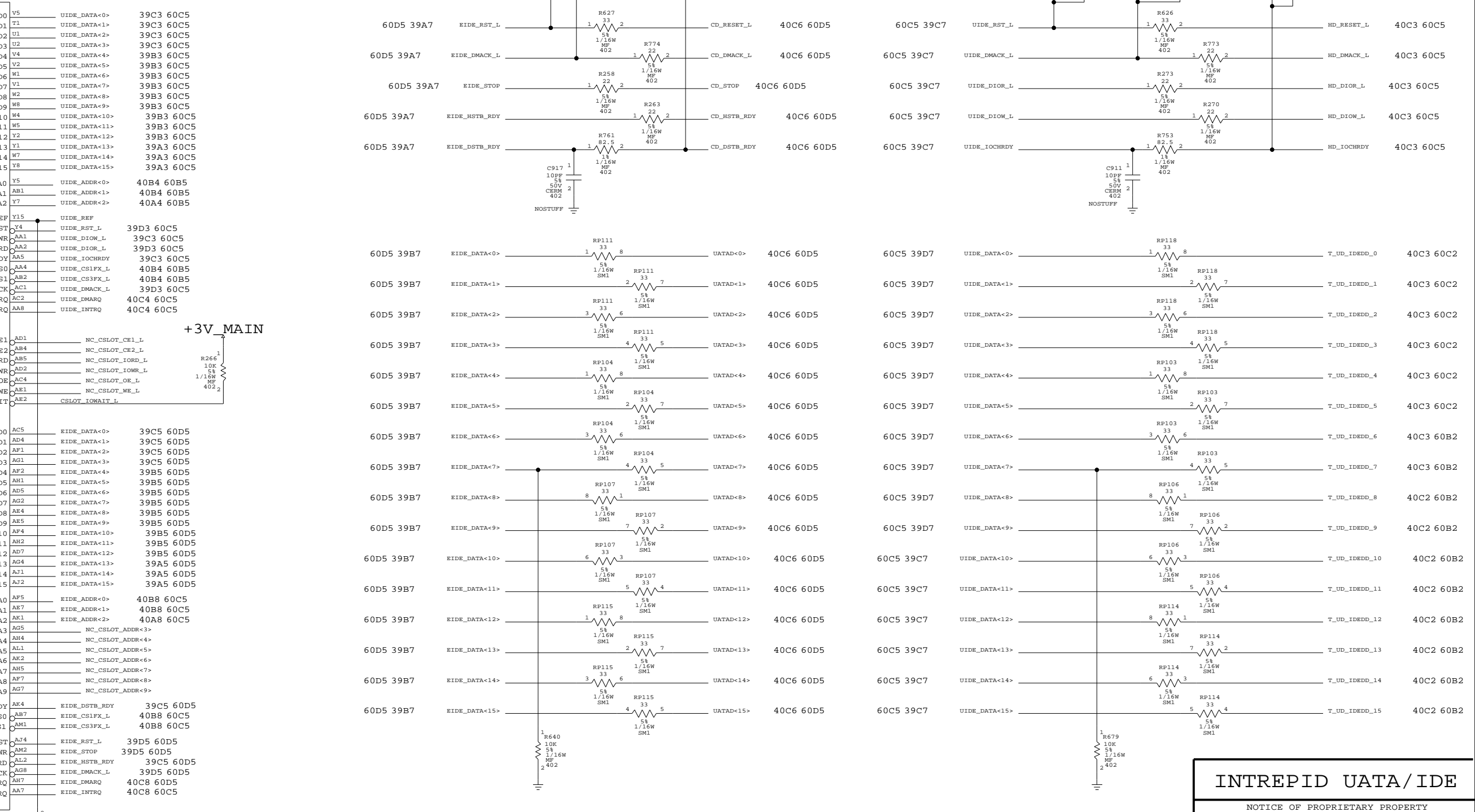
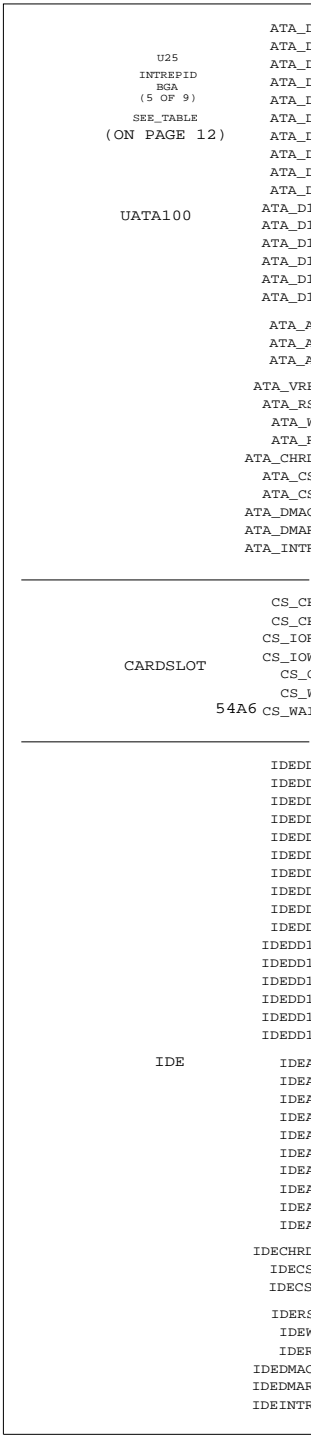
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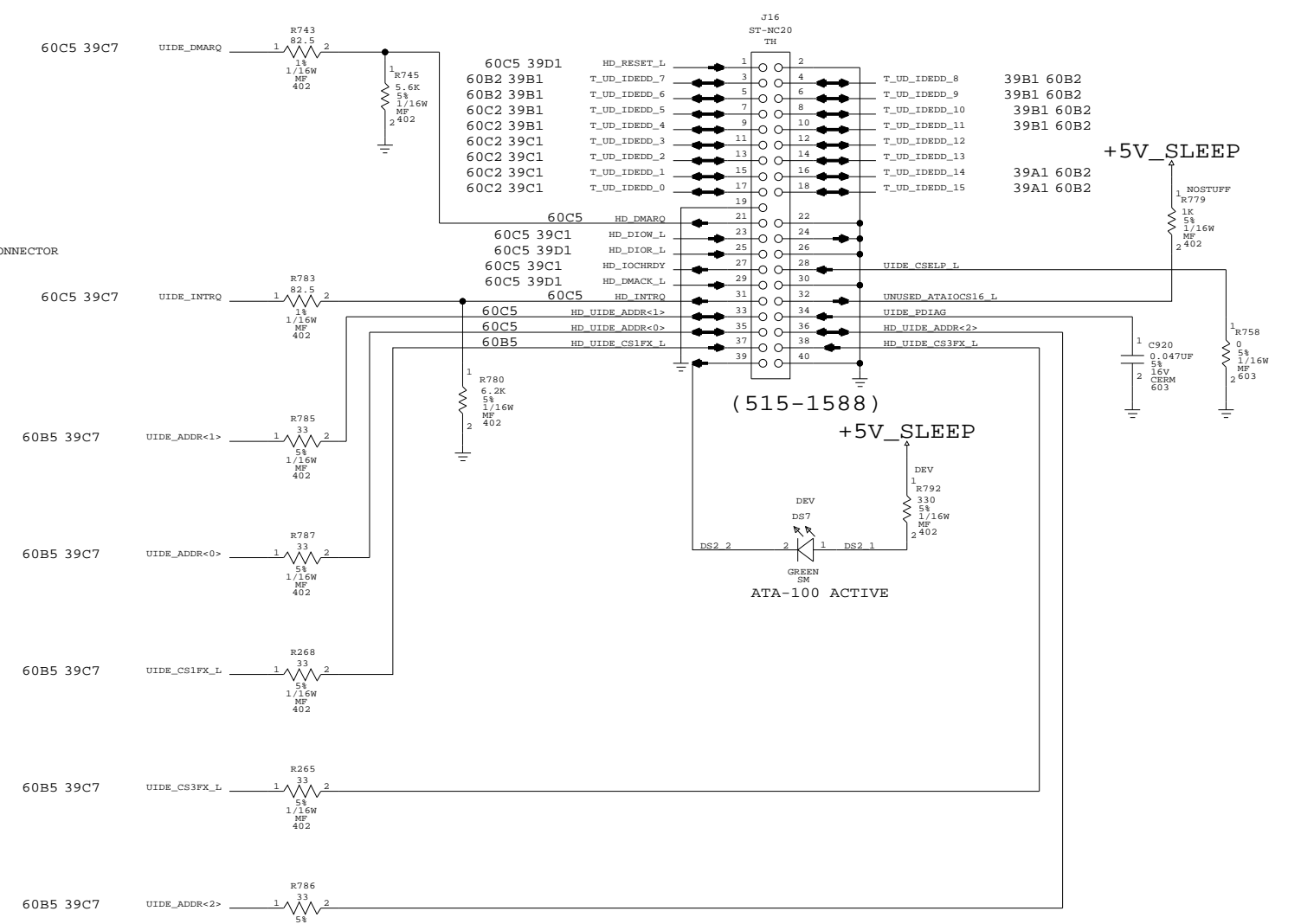
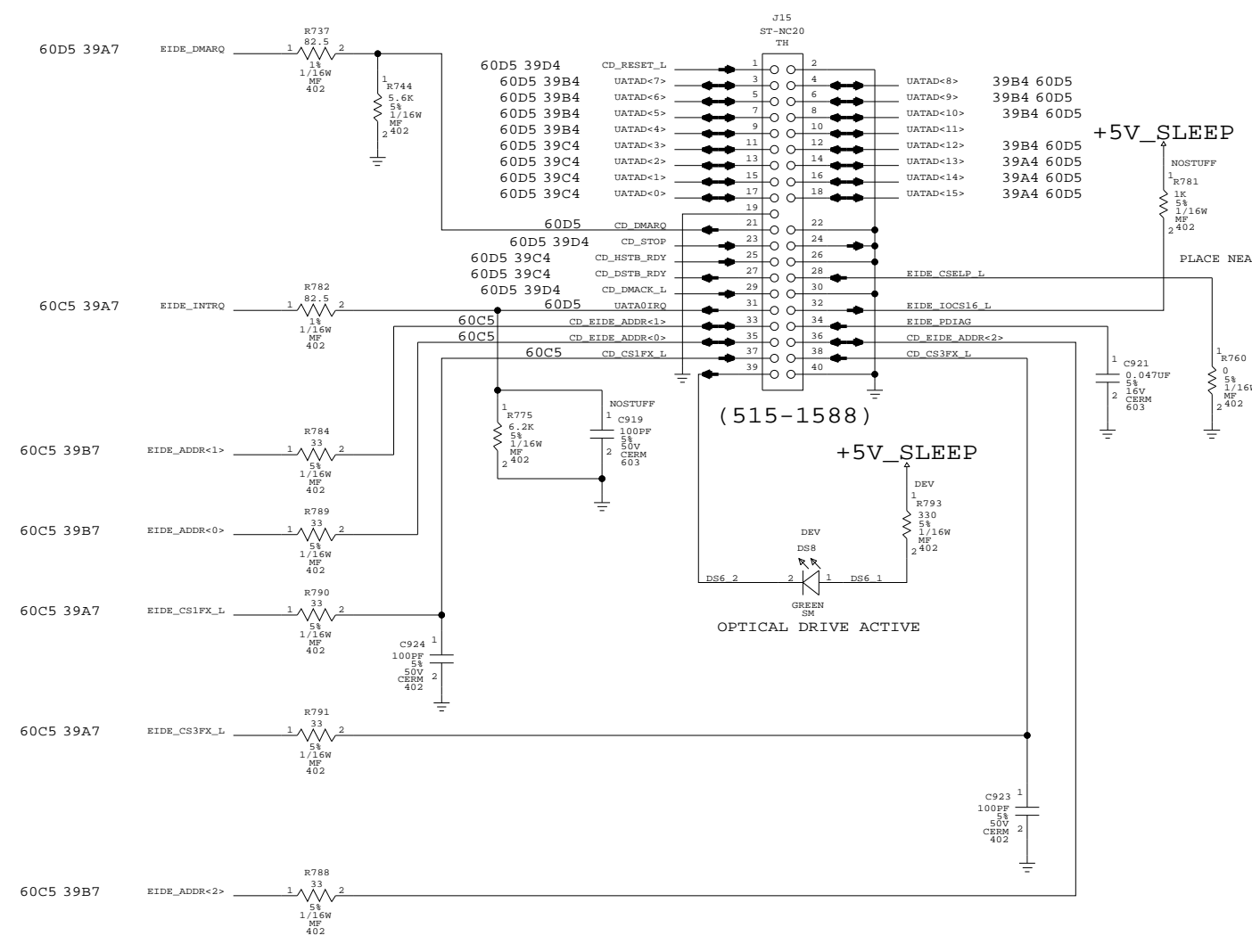
INTREPID UATA/IDE

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	SCALE	NONE	SHT	39	OF	74

OPTICAL DRIVE INTERFACE

ATA-100 INTERFACE

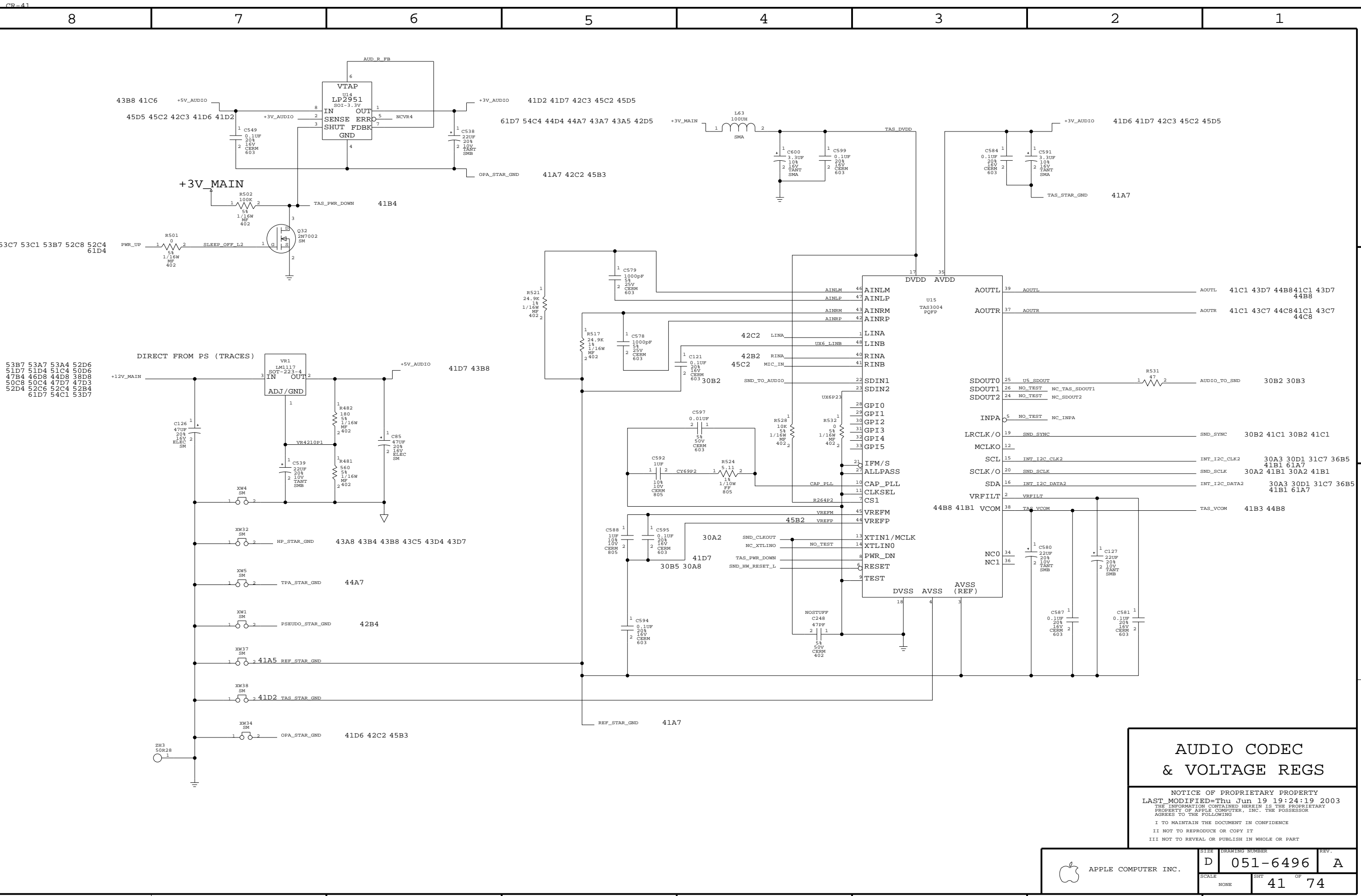


CD/HD CONS

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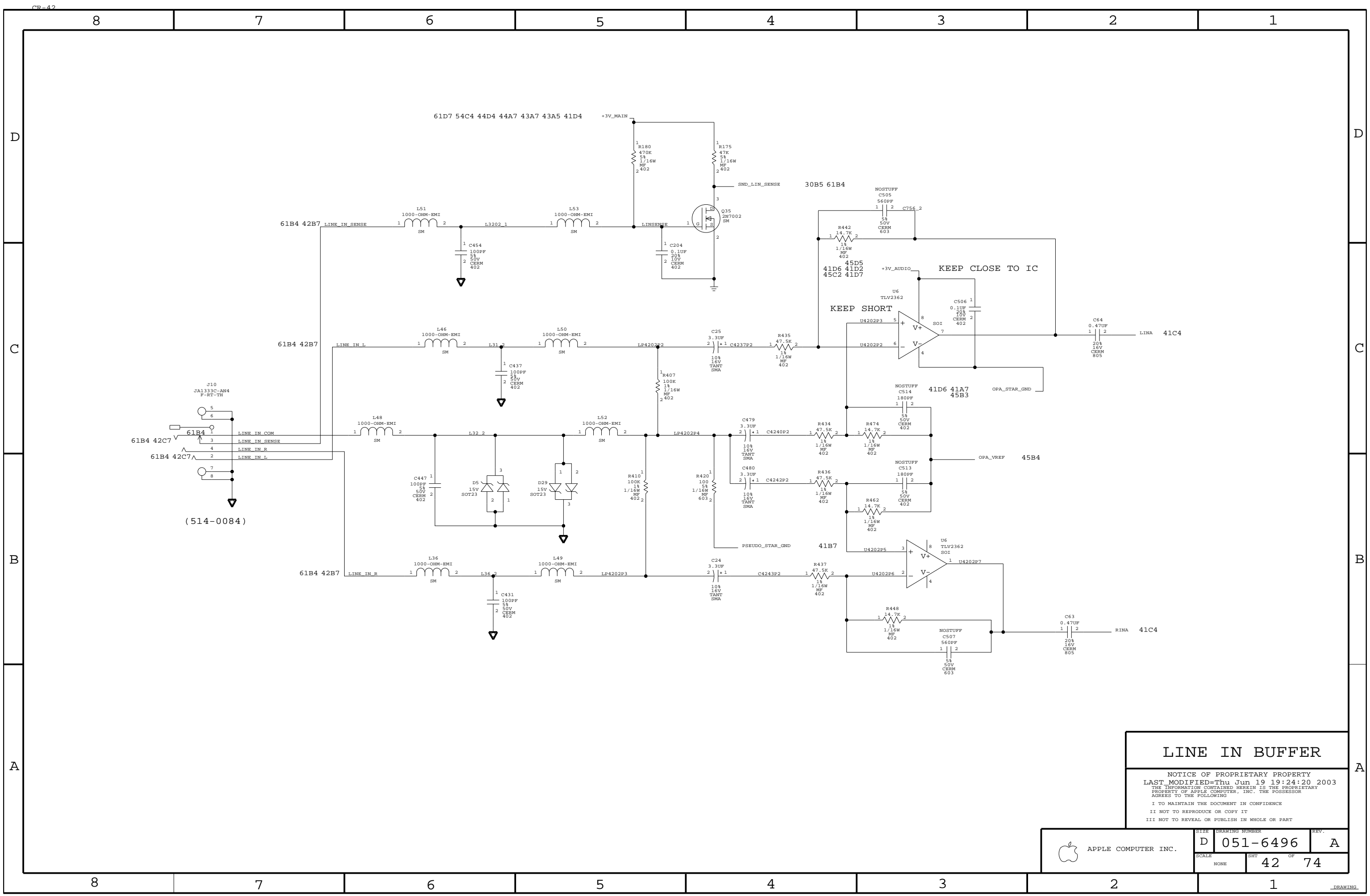
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	NONE	051-6496	A
SCALE		SHT	OF
		40	74



AUDIO CODEC & VOLTAGE REGS

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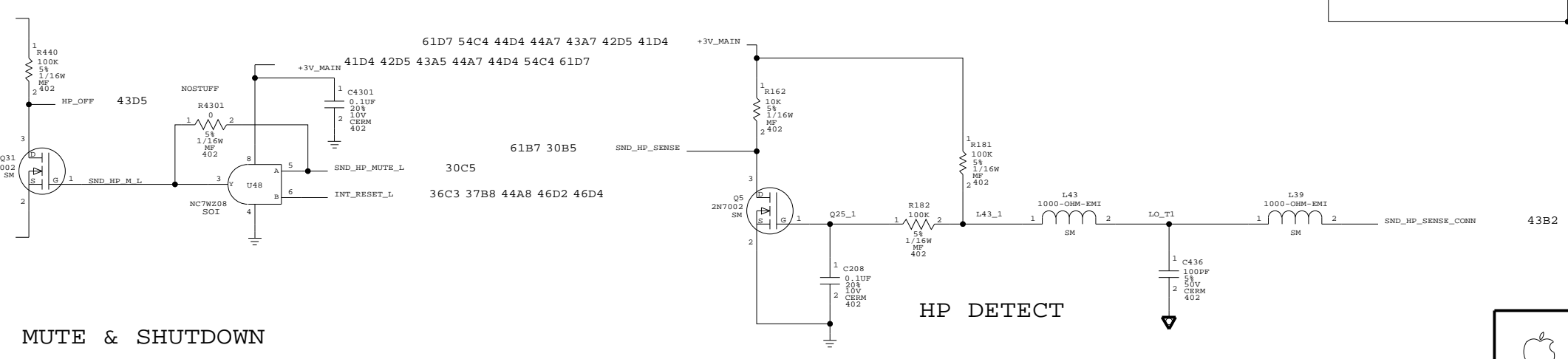
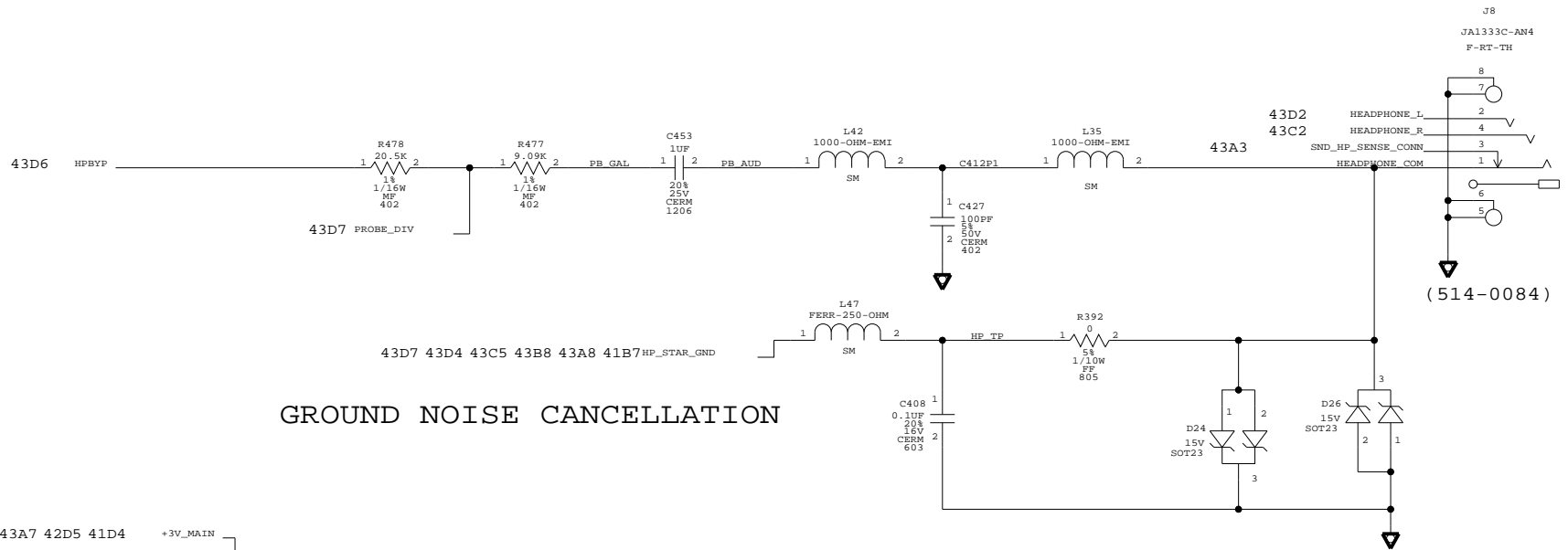
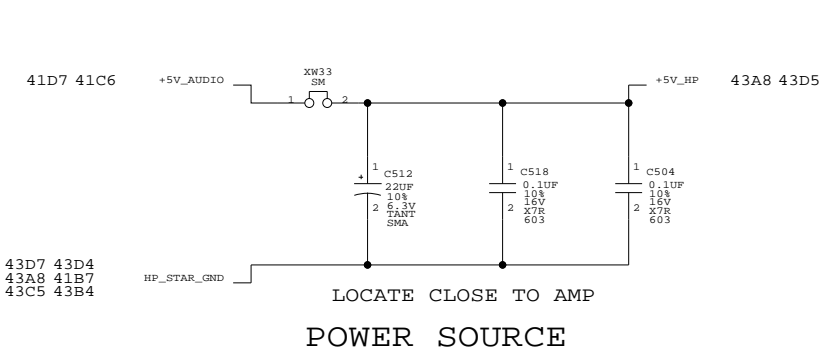
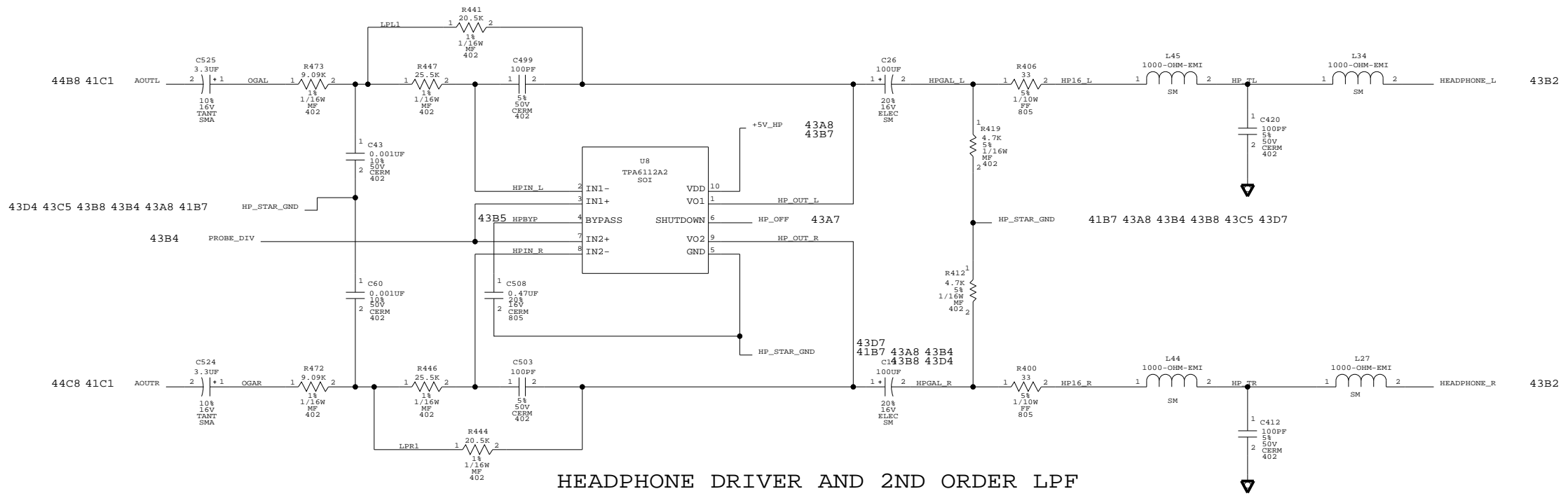
	DRAWING NUMBER	REV.
	D 051-6496	A
SCALE	SHT	OF
NONE	41	74



LINE IN BUFFER

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	SHEET 42	OF 74	



HEADPHONE OUT AMP

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	NONE	051-6496	A
SCALE		SHT	OF
		43	74

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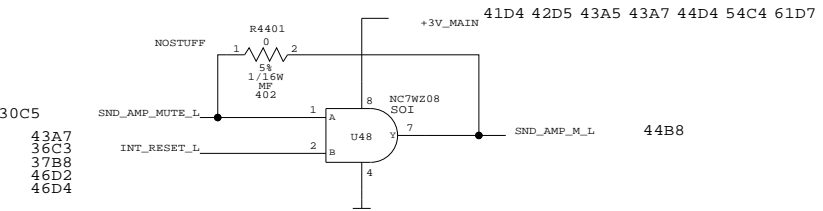
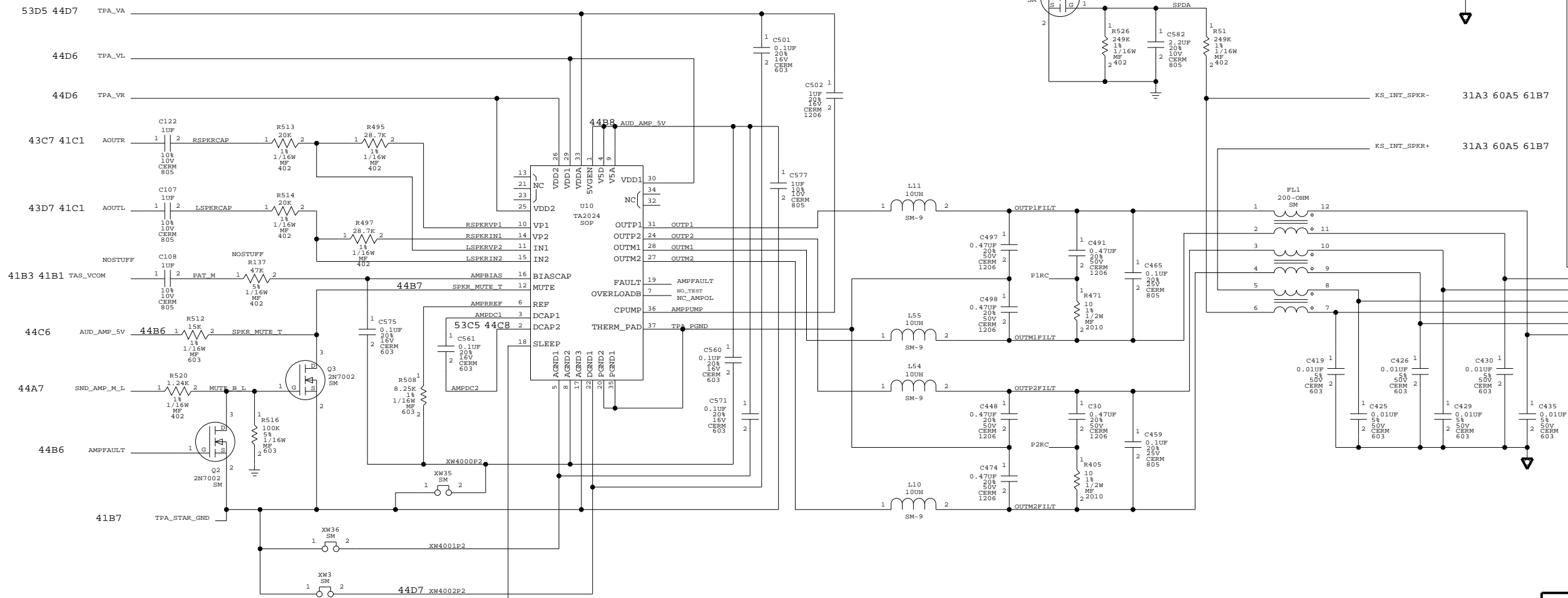
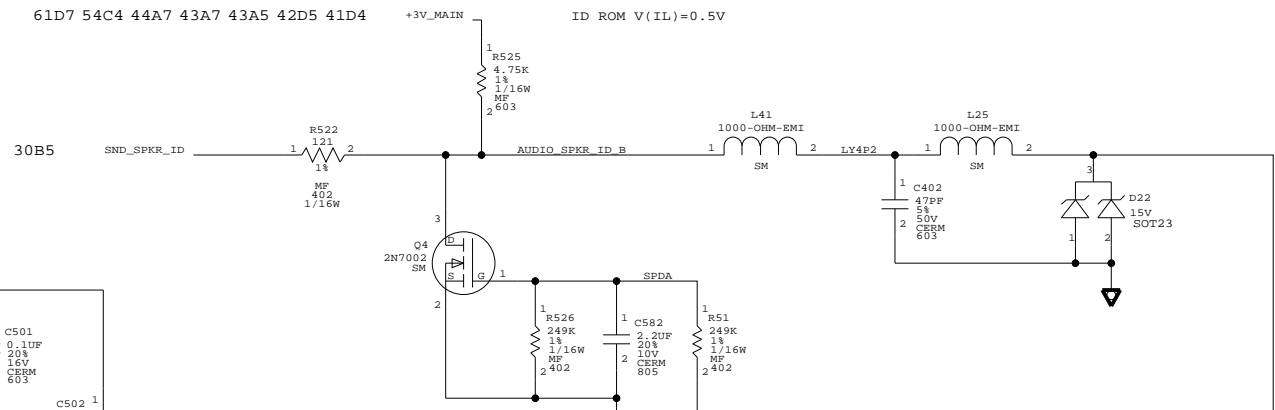
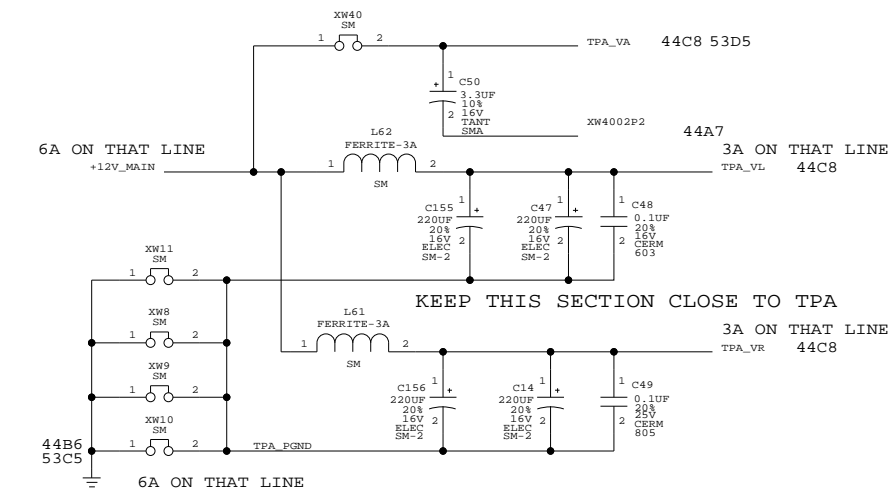
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SPEAKER AMP

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	SCALE	44	74

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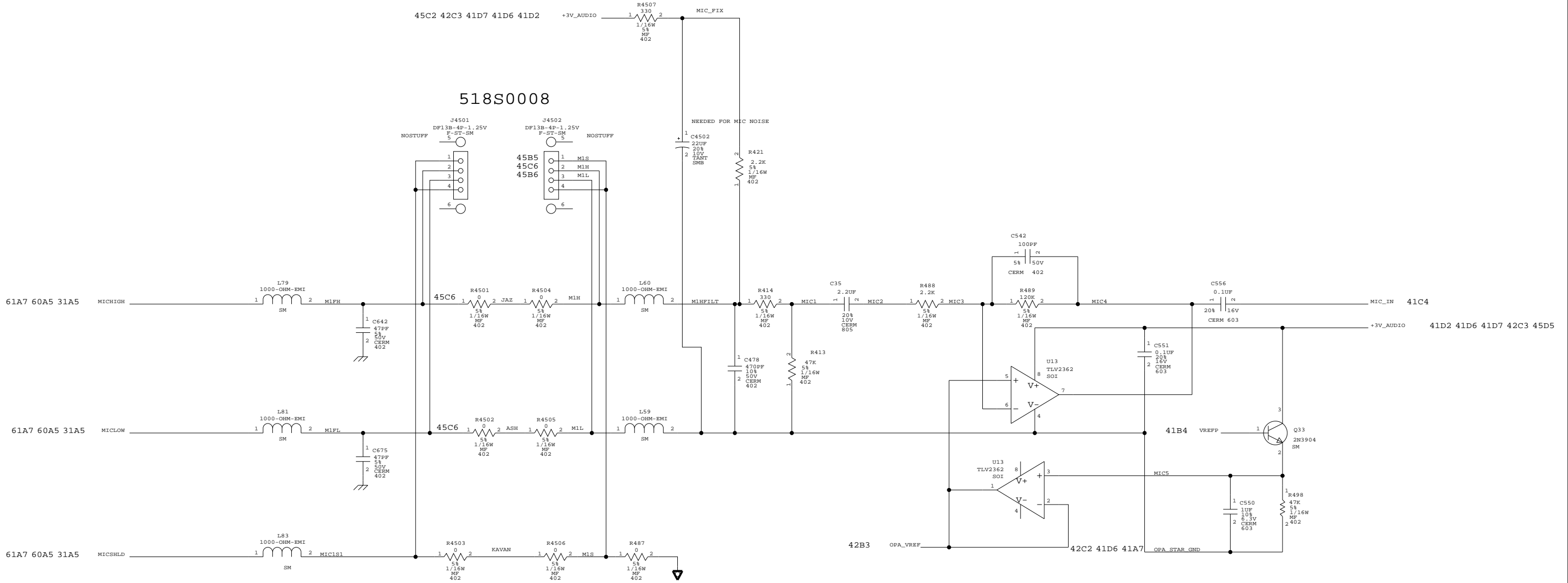
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PLACE R4501, R4502 AND R4503 NEAR AUDIO

PLACE R4504, R4505 AND R4506 NEAR KITCHENSINK

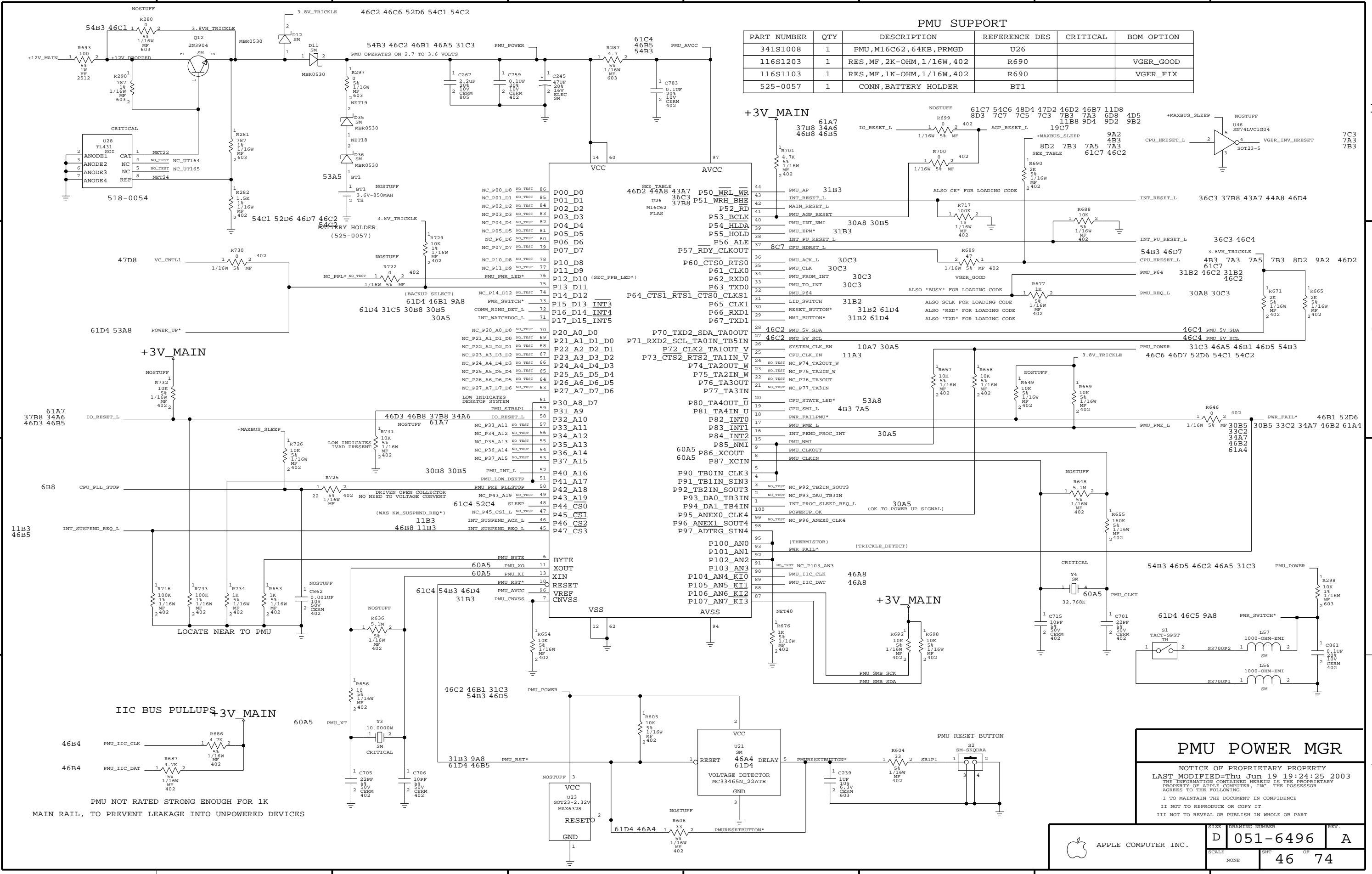
MIC PREAMP

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	NONE	051-6496	A
SCALE		SHT	OF
		45	74

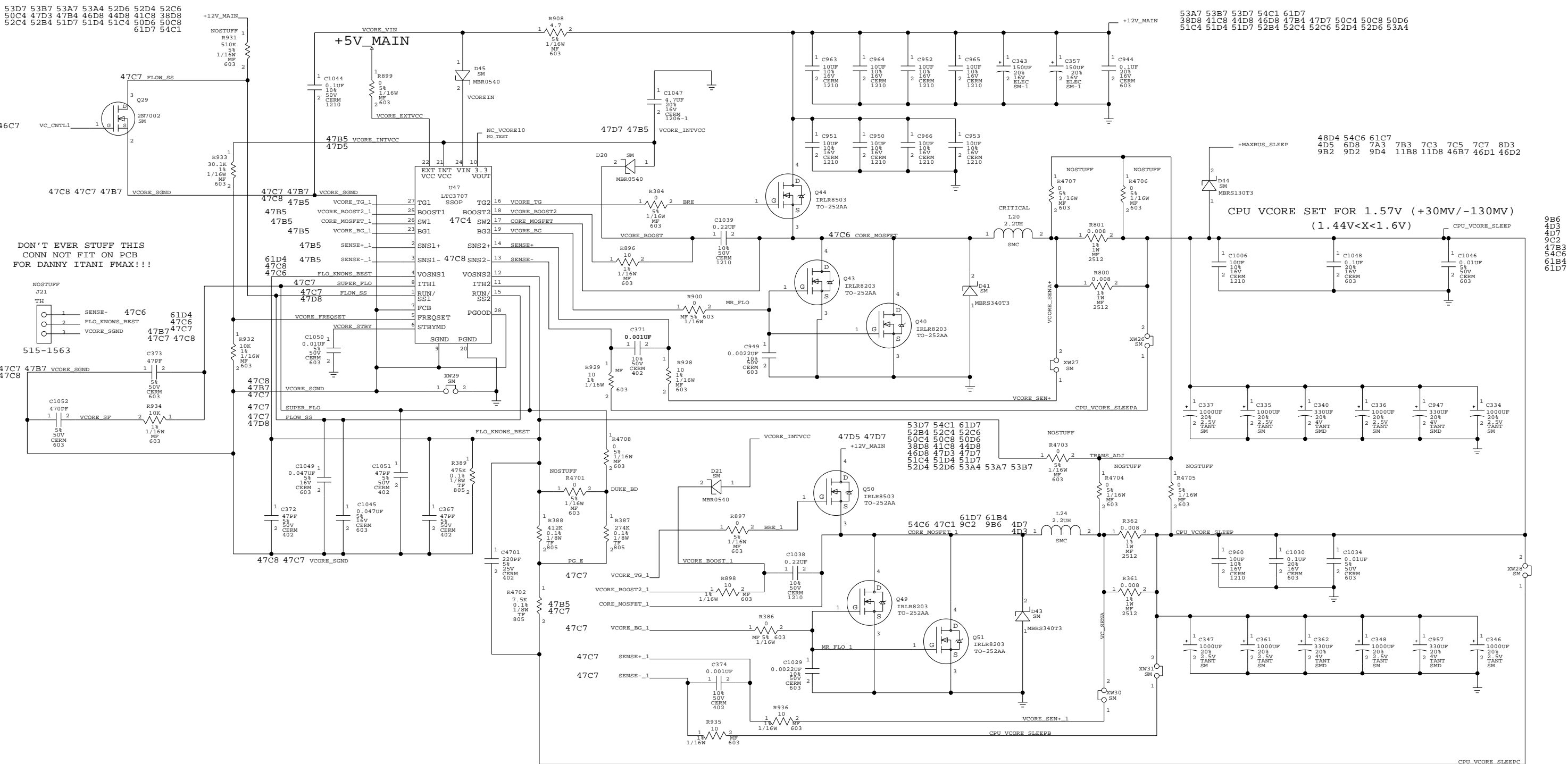
PMU SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1008	1	PMU, M16C62, 64KB, PRMGD	U26		
116S1203	1	RES, MF, 2K-OHM, 1/16W, 402	R690		VGER_GOOD
116S1103	1	RES, MF, 1K-OHM, 1/16W, 402	R690		VGER_FIX
525-0057	1	CONN, BATTERY HOLDER	BT1		

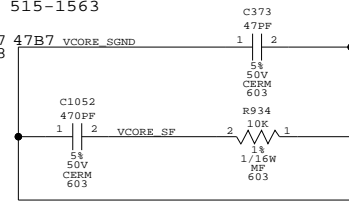
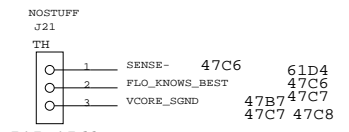


PMU POWER MGR

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DON'T EVER STUFF THIS
CONN NOT FIT ON PCB
FOR DANNY ITANI FMAX!!!



KUMA SERVER(1):HARDWARE:KUMA DESIGNS:KUMA POWER SUPPLIES:VCORE WITH AVP TABLES

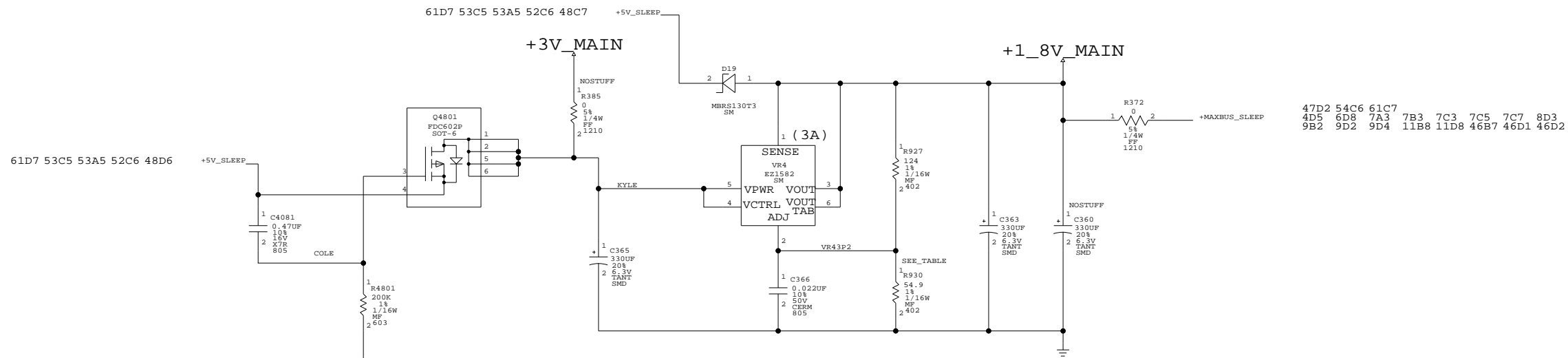
PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0018	128S0012	C340,C362,C947,C957	330UF, 2.5V, TANT	

CPU & AGP VREGS

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	SCALE	NONE	SHT	47	OF	74

INTREPID MAXBUS & CPU OVDD POWER CONVERTER
(OFF DURING SLEEP)

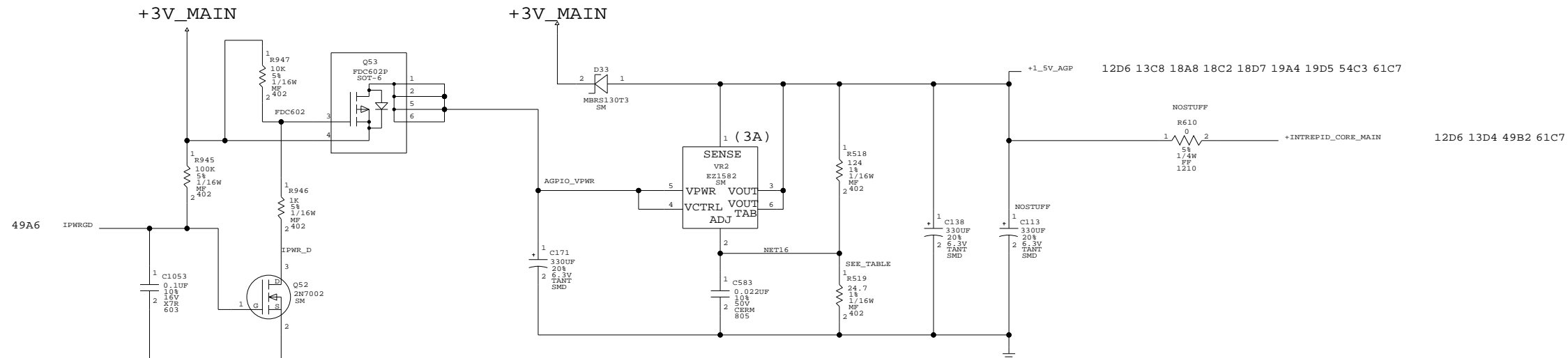


47D2 54C6 61C7
4D5 6D8 7A3 7B3 7C3 7C5 7C7 8D3
9B2 9D2 9D4 11B8 11D8 46B7 46D1 46D2

MAXBUS I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S2491	1	RES, FF, 24.9-OHM, 1%	R930		MAXIO_1'50V
114S3481	1	RES, FF, 34.8-OHM, 1%	R930		MAXIO_1'65V
114S4421	1	RES, FF, 44.2-OHM, 1%	R930		MAXIO_1'70V
114S5491	1	RES, FF, 54.9-OHM, 1%	R930		MAXIO_1'80V

AGP I/O POWER CONVERTER



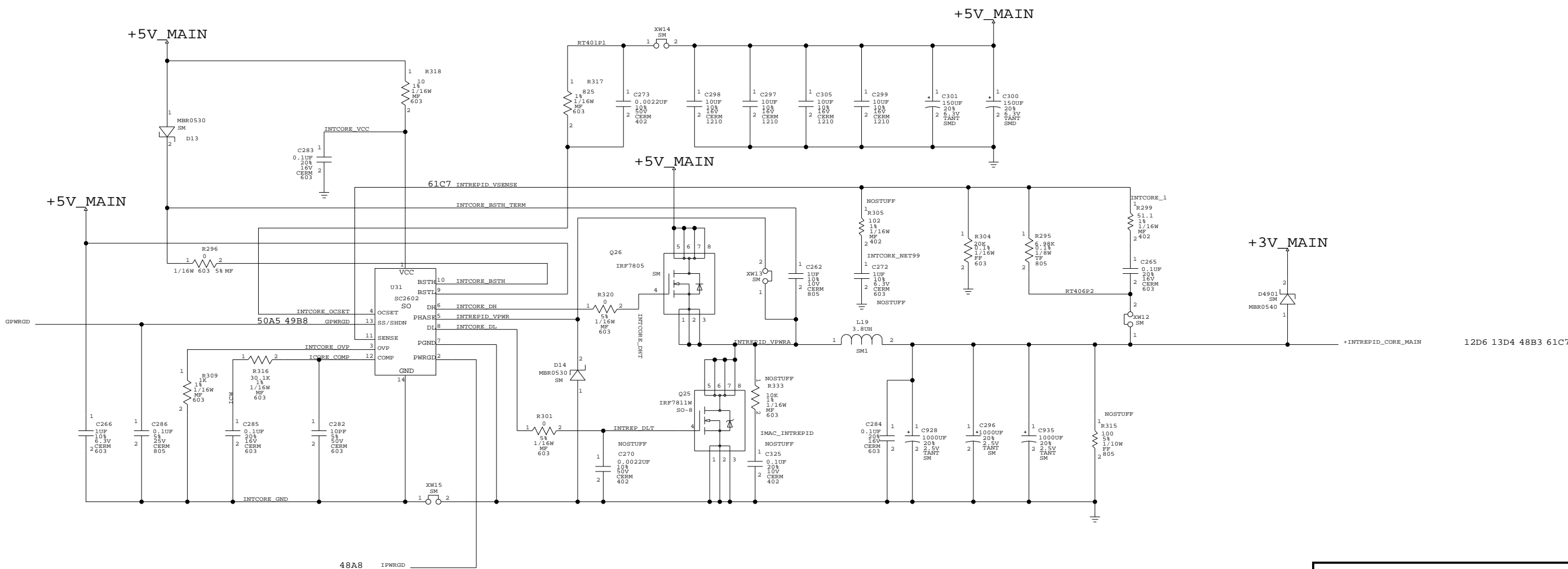
AGP I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S2491	1	RES, FF, 24.9-OHM, 1%	R519		AGPIO_1'50V
114S3481	1	RES, FF, 34.8-OHM, 1%	R519		AGPIO_1'65V
114S4421	1	RES, FF, 44.2-OHM, 1%	R519		AGPIO_1'70V
114S5491	1	RES, FF, 54.9-OHM, 1%	R519		AGPIO_1'80V

CPU & AGP VREGS

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	NONE	051-6496	A
SCALE		SHT	OF
		48	74



TABLES FOR INTREPID CORE RESISTOR VALUES TO VOLTAGES ARE LOCATED AT KUMA SERVER(1):HARDWARE:KUMA DESIGNS;KUMA POWER SUPPLIES;ICORE R TOLERANCE

INTREPID CORE

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	SCALE NONE	SHIT 49	OF 74

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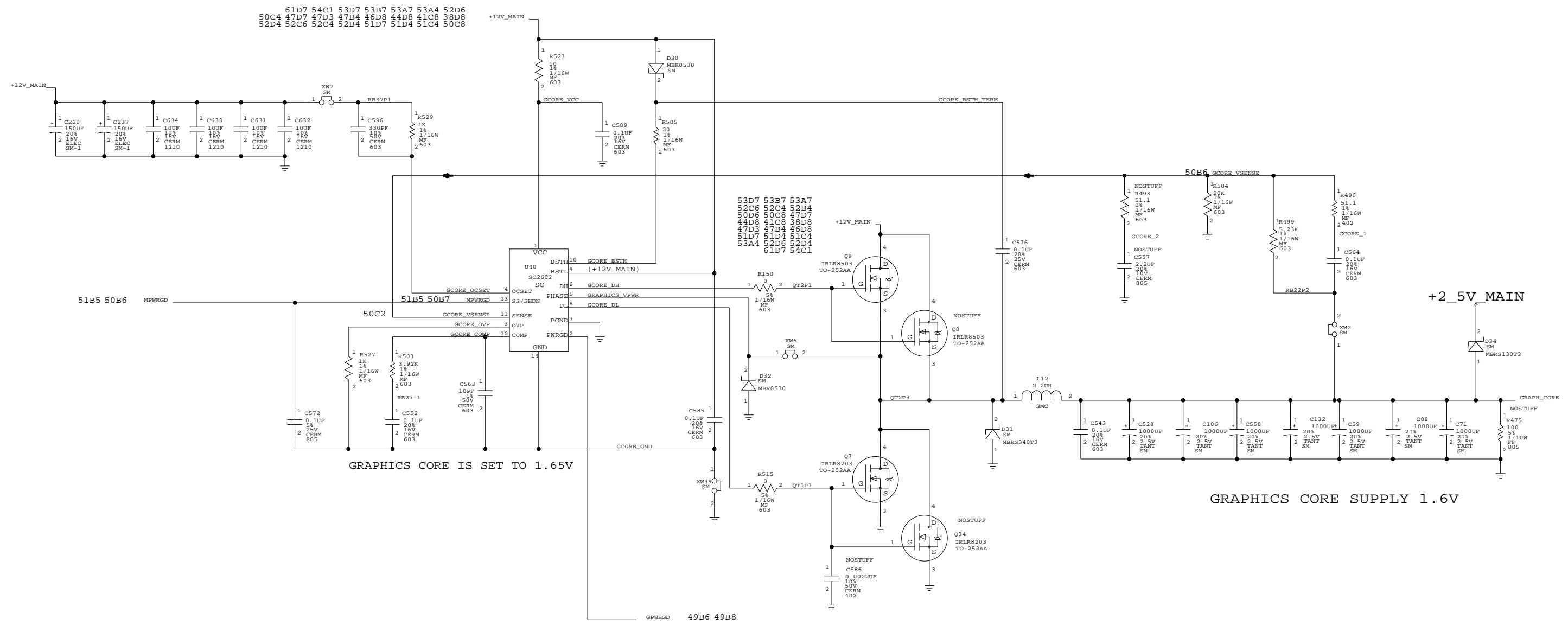
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GRAPHICS CORE

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	NONE	051-6496	A
SCALE		SHT	OF
		50	74

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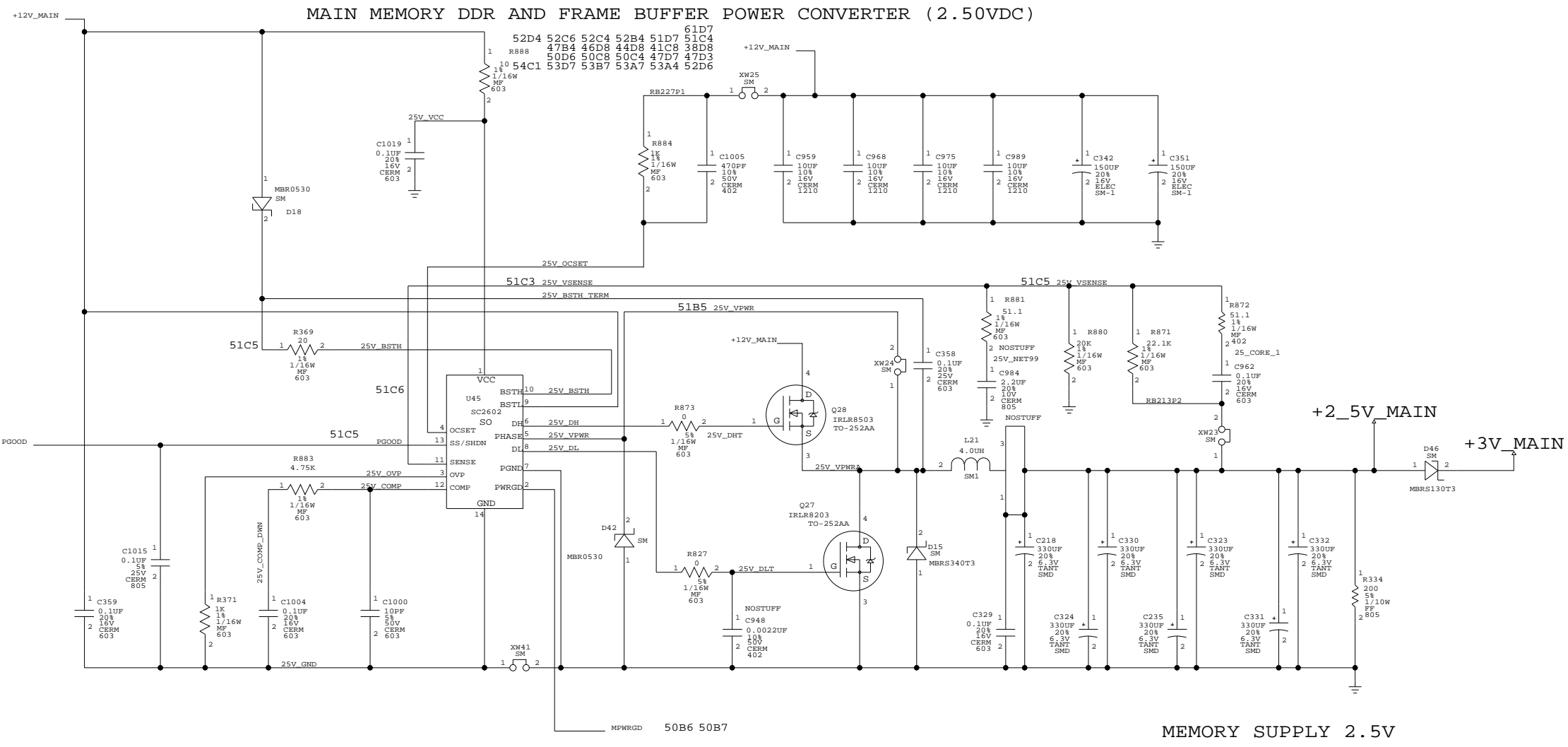
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61D7 54C1 53D7 53B7 53A7 53A4 52D6
50C4 47D7 47D3 47B4 46D8 44D8 41C8 38D8
52D4 52C6 52C4 52B4 51D4 51C4 50D6 50C8



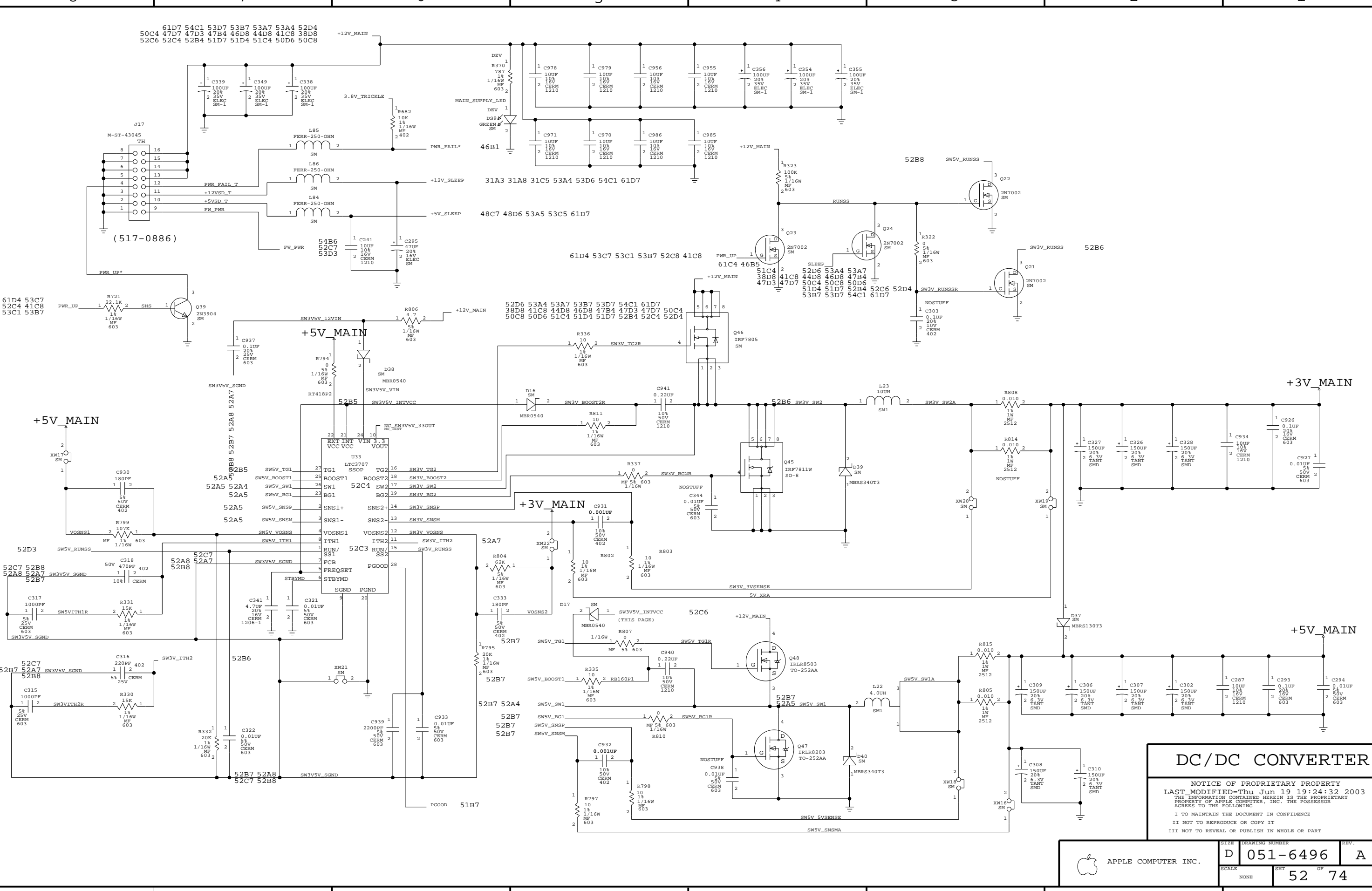
MEMORY PS

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	NONE	051-6496	A
SCALE		SHT	OF
		51	74

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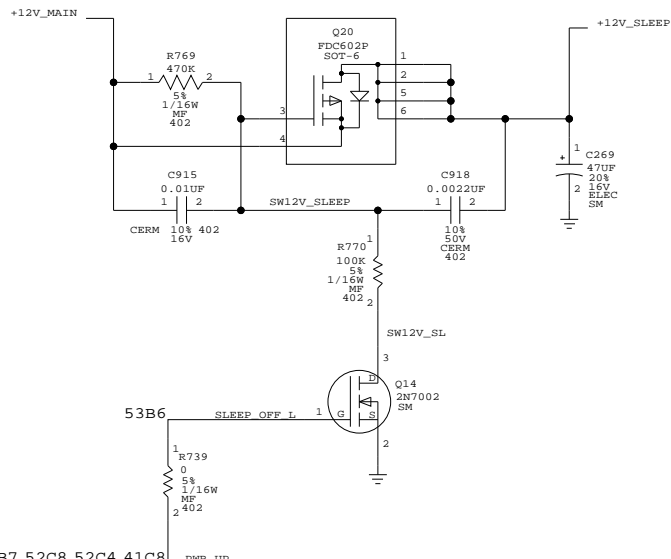
DC/DC CONVERTER

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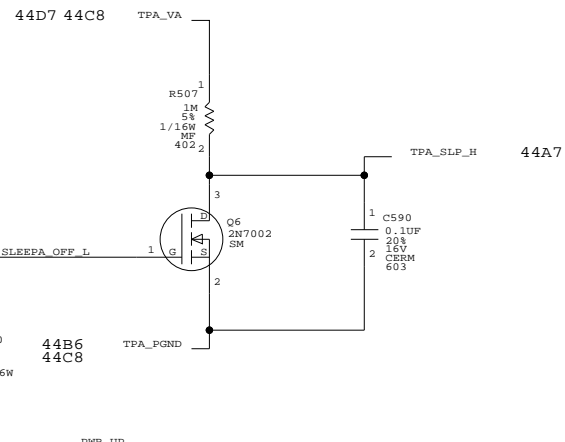
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6496	A
SCALE		SHT	OF
		52	74

+12V MAIN POWER SWITCH (OFF DURING SLEEP)

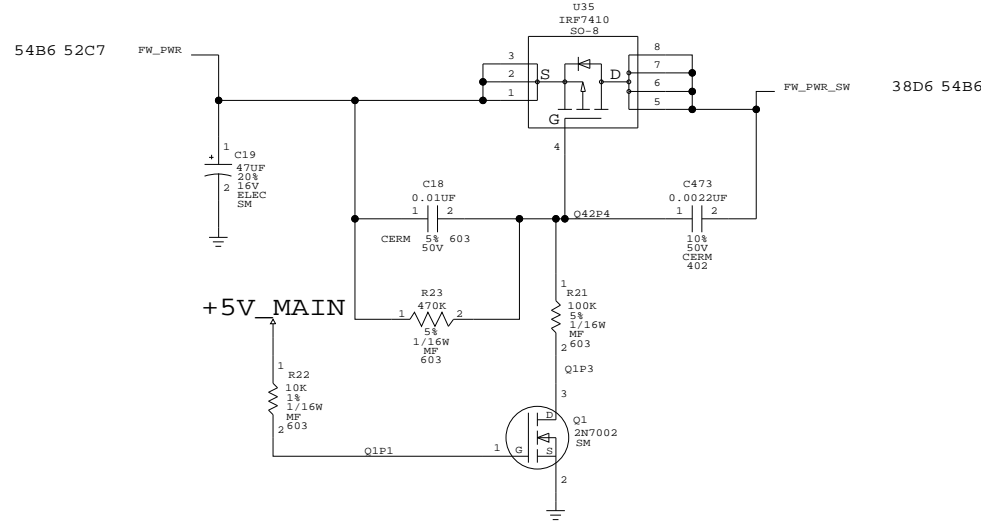
61D7 54C1 53B7
52C4 52B4 51D7 51D4 51C4
47B4 46D8 44D8 41C8 38D8
50D6 50C8 50C4 47D7 47D3
53A7 53A4 52D6 52D4 52C6



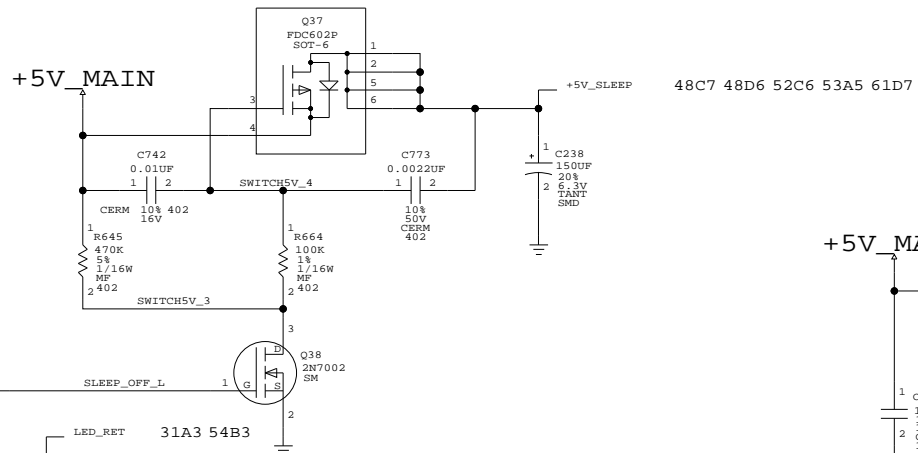
AUDIO SLEEP SWITCH (OFF DURING SLEEP)



FIREWIRE POWER SWITCH

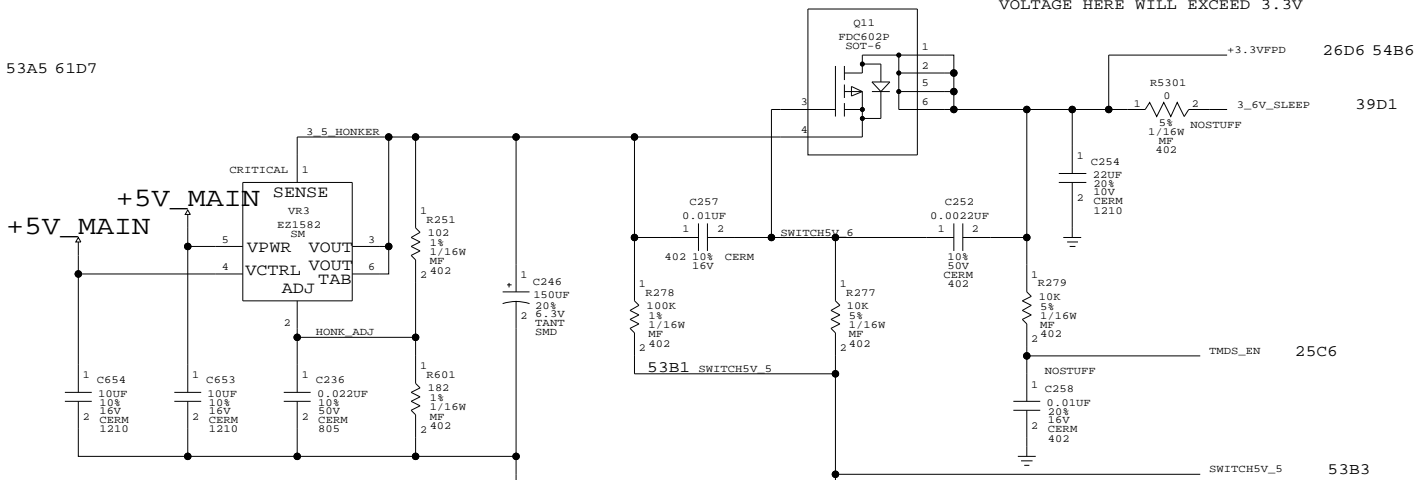


+5V POWER SWITCH (OFF DURING SLEEP)



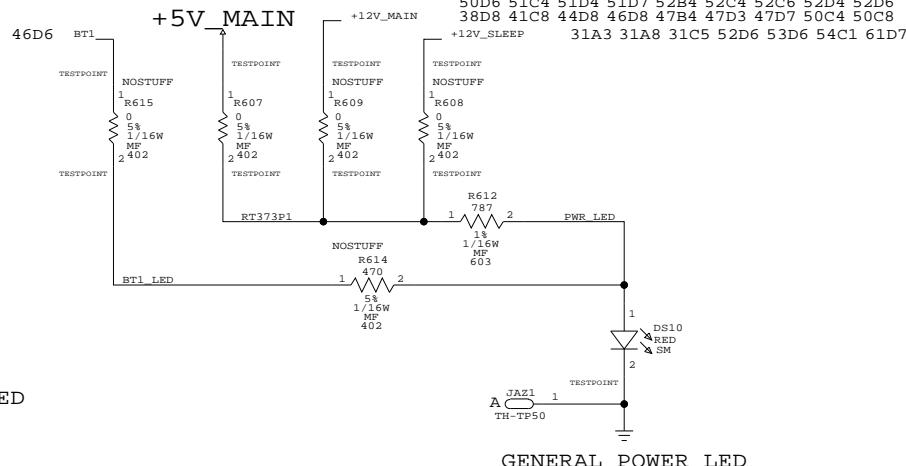
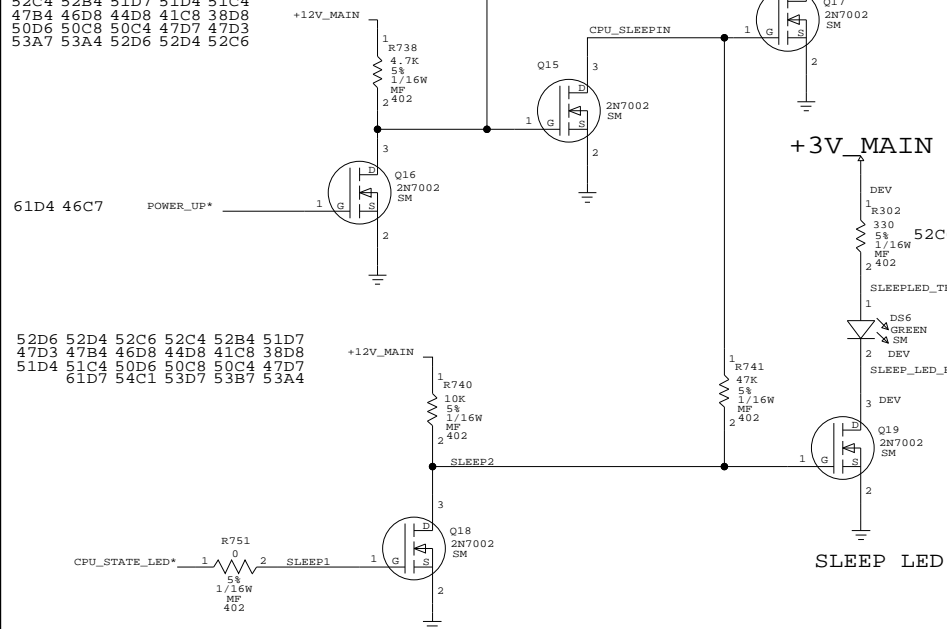
TMDS POWER CONVERTER & SWITCH (OFF DURING SLEEP)

VOLTAGE TO SUPPORT 3.3V AT PANEL
VOLTAGE HERE WILL EXCEED 3.3V



+5V POWER, SLEEP & TESTPOINT LEDS (TESTPOINT LED IS USED FOR SERVICE AND IF NOT ILLUMINATED, TELLS USER ITS OK TO ADD MEMORY)

61D7 54C1 53D7
52C4 52B4 51D7 51D4 51C4
47B4 46D8 44D8 41C8 38D8
50D6 50C8 50C4 47D7 47D3
53A7 53A4 52D6 52D4 52C6



+5V/+12V, AUDIO FW & TMDS PWR

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	D	051-6496	A
SCALE	SHT	OF	
NONE	53	74	

CLOCK POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+2_5V_DDR_AVDD	10	2.5	20
+2_5V_DDR_VDD	10	2.5	20
+3V_INTSS_AVDD	10	3.3	20
+3V_INTSS_VDD	10	3.3	20
PCK2059_VDD12C	10	2.5	20

10D4
10D5
10B7
10B6
10D4

CPU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+MAXBUS_SLEEP	10	1.8	20
CPU_AVDD	10	1.85	20
CPU_VCORE_SLEEP	10	1.85	20

4D5 6D8 7A3 7B3 7C3 7C5 7C7 8D3 9B2 9D2 9D4
4D3 11B8 11D8 46B7 46D1 46D2 47D2 48D4 61C7
4D3 4D7 9B6 9C2 47B3 47C1 61B4 61D7

ETHERNET POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+2_5V_ENET	10	2.5	20

37C3 37D3 37D5

FIREWIRE POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
FW_DIO_V	10	3.3	20
FW_DIODE_BYPASS_V	10	3.3	20
FW_PWR	10	24	20
FW_PWR_SW	10	24	20
FW_PHY_3_3	10	3.3	20
FW_VGND	10	0	20
FW_VP	10	12	20
FW_VP1	10	12	20
FW_VP2	10	12	20
FW_VP_1	10	12	20
FW_VP_2	10	12	20

38B6
38B6 38B7
52C7 53D3
38D6 53D1
38B5 38B7 38D7
38D1
38D5
38D1 38D3
38C1 38D3
38D4
38D4

GRAPHICS POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3_3VFPD	10	3.6	20
DAC2VDD	10	3.3	20
DACVDD	10	3.3	20
DDC_VCC_3	10	3.3	20
DDC_VCC_5	10	5	20
DDR_VREF	10	1.25	20
IFPDVCC	10	3.8	20
IFPDVREF	10	3.8	20
INT_TMDS_3V	10	3.6	20
GPU_AGP_VREF	10	0.75	20
GPU_FB_VREF	10	1.25	20
GRAPH_CORE	10	1.6	20
NPVLLVDD	10	3.3	20
SGRVAVREF	10	1.25	20
SGRBVREF	10	1.25	20

26D6 53C1
24C5
24C4
26A5 26B3 61B7
27C4 61B7
16B2 16D1 16D8 17D8
25A6 25B4
25B4
26B3 26C3 26C4 26D5 61C7
19A3 19A8
20C8
19D5 25C4 25C6 50B1
24D5
22A3 22C4 22C8
23A3 23C4 23C8

GPU_50PULLUP	1.5	19A5
GPU_50PULLDOWN	0	19A5
GPU_TMODE	0	19A5
GPU_XTALSSIN	0	24B4
VPCLK	0	24D4
CSLOT_IOWAIT_L	3.3	39B7
EIDE_CSELP_L	0	40C6
EIDE_IOCS16_L	5	40C6
UIDE_CSELP_L	0	40C2
UNUSED_ATAIOC16_L	5	40C2

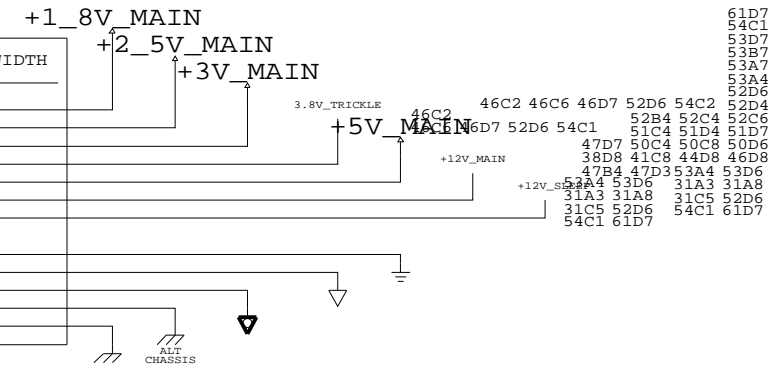
INTREPID POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_5V_INTREPID_PLL	10	1.5	20
+1_5V_INTREPID_PLL1	10	1.5	20
+1_5V_INTREPID_PLL2	10	1.5	20
+1_5V_INTREPID_PLL3	10	1.5	20
+1_5V_INTREPID_PLL4	10	1.5	20
+1_5V_INTREPID_PLL5	10	1.5	20
+1_5V_INTREPID_PLL6	10	1.5	20
+1_5V_INTREPID_PLL7	10	1.5	20
+1_5V_INTREPID_PLL8	10	1.5	20
+1_5V_AGP	10	1.5	20
INT_AGP_VREF	10	0.75	20

11D3 18D6 30D6 32D5
30C4
30D4
30D4
30D4
30D4
18D5
32D4
11D2
30D4
12D6 13C8 18A8 18C2 18D7 19A4 19D5 48B4 61C7
18A7 18C6

MAIN POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_8V_MAIN	10	1.8	20
+2_5V_MAIN	10	2.5	20
+3V_MAIN	10	3.3	20
3_8V_TRICKLE	10	3.8	20
+5V_MAIN	10	5	20
+12V_MAIN	10	12	20
+12V_SLEEP	10	12	20
GND	10	0	20
AGND	10	0	20
ANALOGGND	10	0	20
ALTCHGND	10	0	20
CHGND	10	0	20



PMU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
3_8V_TRICKLE	10	3.8	20
PMU_AVCC	10	3.5	20
PMU_POWER	10	3.5	20

46C1 46D7
46B5 46D4 61C4
31C3 46A5 46B1 46C2 46D5

SYSTEM POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+12VSD_FILT	10	12	20
FAN_12V_FILT	10	12	20
KS5VSD	10	5	20
LED_5V	10	5	20
LED_5V_FILT	10	5	20
LED_RET	10	0	20
LED_RET_FILT	10	0	20

31A5
31A5 61C7
31A5 61A7
31A8
31A5 61A7
31A3 53B6
31A5 61A7

USB POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3V_INTREPID_USB	10	3.3	20
NEC_AVDD	10	3.3	20
USB_GND	10	0	20
USB_PORT_PWR	10	5	20
USB_PWR	10	5	20
USB_PWR_EN	10	0	20

30C4
34D5
35A4 35B3 35C3 35D3
35A4 35B3 35C3 35D3
61B4 27B5 27C2 27D3
35A6

POWER CONSTRAINTS

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SIG_NAME	RATSNBST_SCHEDULE	MAX_VIAS	DELAY_RULE	STUB_LENGTH	MIN_NECK_WIDTH	MAX_EXPOSED_LENGTH	NO_TEST	FUNC_TEST	PULSE_PARAM
15C5 15B6 15B3 15A6 14D8 14C8 14B8 15C8	MEM_GROUP0:::150	8	:::1300		3				167 MHZ
17D6 17D4 17C6 17C4	MEM_GROUP0 A:::180	8	:::1800		3				167 MHZ
15C7 15C4 15B7 15B4 15B2 15A6 15A2	MEM_GROUP0 B:::180	2	:::2400		3				167 MHZ
17B6 17B4 17A6 17A4	MEM_GROUP0:::180	3	:::1300		3				167 MHZ
16D6 16C6 16B6	MEM_GROUP0 A:::180	3	:::1700		3				167 MHZ
16A6 15D7 15D4 15C7 15C4 15B6 15B2	MEM_GROUP0 B:::180	2	:::2400		3				167 MHZ
15C7 15C4 15B7 15B4 15B2 15A6 15A2	MEM_GROUP0:::180	3	:::1300		3				167 MHZ
17D6 17C6 17B6 17A6	MEM_GROUP0 A:::180	3	:::1800		3				167 MHZ
15C7 15C4 15B7 15B4 15B2 15A6 15A2 17D4 17C4 17B4 17A4	MEM_GROUP0 B:::180	2	:::2400		3				167 MHZ
14D6 14D3 14D2 14C3 14C2 14B3 14A3	MEM_ADDR:::200	3	:::600						
16B4 14D3 14D1 14C3 14C1 14B3 14A3	RAM_ADDR:::1300	4	:::3500	200					
17C6 17C4 17B6 17B4 16B6 14D6 14B3	MEM_ADDR:::1300	3	:::600						
17B6 16B6 16B4 14B3	RAM_ADDR:::1300	4	:::4000	200					
14C6 14C2 14B2 14A2	MEM_ADDR:::200	3	:::600		10 MIL SPACING				
16B6 16B4 14C1 14B1	RAM_CS_GROUP0:::400	3	:::2000:3500		10 MIL SPACING				
17B4 14B1 14A1	RAM_CS_GROUP1:::350	2	:::2000:3500		10 MIL SPACING				
14C6 14A3	MEM_ADDR:::200	3	:::600						
14C6 14A3	MEM_ADDR:::200	3	:::600						
14C6 14A3	MEM_ADDR:::280	3	:::600						
17B6 16B4 14A3	RAM_ADDR:::2000	4	:::4000	200					
17B4 16B4 14A3	RAM_ADDR:::2000	4	:::4000	200					
17B6 16B6 14A3	RAM_ADDR:::2000	4	:::4000	200					
14C6 14C2 14B6 14B2 14A2	MEM_ADDR:::200	3	:::600		10 MIL SPACING				
16B6 16B4 14B1 14A1	RAM_CS_GROUP0:::400	3	:::2500		10 MIL SPACING				
17C6 17C4 14C1 14B1	RAM_CS_GROUP1:::350	2	:::2500		10 MIL SPACING				
14D5 14B6	MEM_MUXSEL_H<0..1>	3	:::1000						167 MHZ
14D5 14B6	MEM_MUXSEL_L<0..1>	3	:::1000						167 MHZ
15C5 15A3 14D4	MUX_SEL_H	4	:::2000	200					167 MHZ
15C8 15A6 14D4	MUX_SEL_L	4	:::2000	200					167 MHZ
14C5 14B6	SYSCLK_DDRCLK_A0_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14C5 14B6	SYSCLK_DDRCLK_A0_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
16D6 14C4 10C2	SYSCLK_DDRCLK_A0_UF	3	:::2600	200	8 MIL SPACING	270			167 MHZ
16D6 14C4 10C2	SYSCLK_DDRCLK_A0_L_UF	3	:::2600	200	8 MIL SPACING	270			167 MHZ
14C5 14B6	SYSCLK_DDRCLK_A1_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B6 14B5	SYSCLK_DDRCLK_A1_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
16A4 14C4 10C2	SYSCLK_DDRCLK_A1_UF	3	:::2600	200	8 MIL SPACING	270			167 MHZ
16A4 14C4 10C2	SYSCLK_DDRCLK_A1_L_UF	3	:::2600	200	8 MIL SPACING	270			167 MHZ
14B6 14B5	SYSCLK_DDRCLK_A2_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B6 14B5	SYSCLK_DDRCLK_A2_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B4 10C5	SYSCLK_DDRCLK_A2_UF	3	:::750		8 MIL SPACING	270			167 MHZ
14B6 14B5	SYSCLK_DDRCLK_B0_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B6 14B5	SYSCLK_DDRCLK_B0_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
17B4 14B4 10C2	SYSCLK_DDRCLK_B0_UF	3	:::3500	200	8 MIL SPACING	270			167 MHZ
17B4 14B4 10C2	SYSCLK_DDRCLK_B0_L_UF	3	:::3500	200	8 MIL SPACING	270			167 MHZ
14B6 14A5	SYSCLK_DDRCLK_B1_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B6 14A5	SYSCLK_DDRCLK_B1_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
17D6 14A4 10C2	SYSCLK_DDRCLK_B1_UF	3	:::3500	200	8 MIL SPACING	270			167 MHZ
17D6 14A4 10C2	SYSCLK_DDRCLK_B1_L_UF	3	:::3200	200	8 MIL SPACING	270			167 MHZ
14B6 14A5	SYSCLK_DDRCLK_B2_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
14B6 14A5	SYSCLK_DDRCLK_B2_L_UF	3	:::500:850		8 MIL SPACING	270			167 MHZ
17A6 14A4 10B2	SYSCLK_DDRCLK_B2_UF	3	:::3500	200	8 MIL SPACING	270			167 MHZ
17A6 14A4 10B2	SYSCLK_DDRCLK_B2_L_UF	3	:::3500	200	8 MIL SPACING	270			167 MHZ
10C5	DDR_CLK_VDD_2	3	:::1000			400			167 MHZ
10C3	DDRCLK_A0_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10C3	DDRCLK_A1_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10C3	DDRCLK_A2_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10C3	DDRCLK_B0_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10C3	DDRCLK_B1_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10C3	DDRCLK_B2_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_A0_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_A1_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_A2_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_B0_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_B1_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDRCLK_B2_L_UF	3	:::400:500		8 MIL SPACING	270			167 MHZ
10B3	DDR_FBO	3	:::500		8 MIL SPACING	270			167 MHZ
10B3	DDR_FBO_L	3	:::500		8 MIL SPACING	270			167 MHZ
10B5	DDR_FBIN	8	:::1550:1615		8 MIL SPACING	400			167 MHZ
10B5	DDR_FBIN_L	8	:::1600:1650		8 MIL SPACING	270			167 MHZ
30A6 10A7	INT_REF_CLK_OUT	3	:::1500		10 MIL SPACING	270			49.92 MHZ
30A6 10A7	INT_REF_CLK_OUT_UF	8	:::1500		10 MIL SPACING	270			49.92 MHZ
10A6	CLKGEN_OUT_1	3	:::500		10 MIL SPACING	270			66.56 MHZ
10A6	CLKGEN_OUT_1_UF	8	:::2500		10 MIL SPACING	270			66.56 MHZ
33C7 33C6 33B7 33B6 61C2 30A6 10A5	MIN_DAISSY_CHAIN	6	:::6000:8000	500					33 MHZ
61B2 34C6 34B7 34B6 61A4 34B6 33B7 32C5	MIN_DAISSY_CHAIN	6	:::6000:8000	500					33 MHZ
61A4 34B6 33B7 32C5 32B8	MIN_DAISSY_CHAIN	7	:::6000:8000	500					33 MHZ

DIGITAL SIGNAL CONSTRAINTS

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DIGITAL SIGNALS

RATSNEST_SCHEDULE

GROUP	SIG_NAME	MATCHED_DELAY	MAX VIAS	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	MAX EXPOSED LENGTH	PULSE PARAM	
	FBD<0..63>	GPU_FBDDATA_A:::225	4	:::800				300 MHZ	20E8 20F8 20G8 21C5 21C8 21D5 21D8
	RFBD<0..63>	RAM_FBDDATA_A:::300	4	:::1000				300 MHZ	21C4 21C7 21D4 21D7 22B1 22B5 22C1 22C5
	FBDDQ<0..7>	GPU_FBDDQ_A:::200	4	:::800				300 MHZ	20D8 20G3
	RFBDQ<0..7>	RAM_FBDDQ_A:::200	4	:::1000				300 MHZ	20G2 22C2 22C6
	FBA<0..12>	GPU_FBADDR_A:::200	4	:::700				300 MHZ	20C8 20D8 20E3 20F3
	RFBA<0..12>	RAM_FBADDR_A:::530	5	:::2400	2350			300 MHZ	20E2 20F2 22C2 22C6 22D2 22D6
	FBABA<0..3>	GPU_FBADDR_A:::200	4	:::600				300 MHZ	20C8 20E3
	RFBABA<0..3>	RAM_FBADDR_A:::530	5	:::2400	50			300 MHZ	20E2 22C2 22C6
	FBRAS_L	GPU_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20G3
	FRBAS_L	RAM_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20G3
	FBAWE_L	GPU_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20F3
	RFBAS_L	RAM_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20F3
	FBCS0_L	GPU_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20F3
	RFCS0_L	RAM_FBCNTL_A:::200	4	:::400				300 MHZ	20C8 20F3
	FBACKE	GPU_FBCNTL_A:::200	5	:::400	100			300 MHZ	20D3 20D7
	RFBAS_L	RAM_FBCNTL_A:::350	5	:::2700	50			300 MHZ	20G2 22B2 22B6
	RFBAS_L	RAM_FBCNTL_A:::500	5	:::2700	50			300 MHZ	20G2 22B2 22B6
	RFBAWE_L	RAM_FBCNTL_A:::500	5	:::2700	50			300 MHZ	20F2 22B2 22B6
	RFBAS0_L	RAM_FBCNTL_A:::350	5	:::2700	50			300 MHZ	20F2 22B2 22B6
	RFBAS0_L	RAM_FBCNTL_A:::500	5	:::2700	50			300 MHZ	20F2 22B2 22B6
	RFBCKE	RAM_FBCNTL_A:::500	5	:::2700	50			300 MHZ	20D2 22C2 22C6
	FBDQS<0..7>	GPU_FBDDQS_A:::100	3	:::350				300 MHZ	20C7 21A8
	RFBDQS<0..7>	RAM_FBDDQS_A:::50	3	:::1500		10 MIL SPACING		300 MHZ	21A7
	FBDQSTERM<0..7>	FBDQSTERM_A:::50	3	:::150		10 MIL SPACING		300 MHZ	21A6 22C2 22C6
	RFBDQSTERM<0..7>	RAM_FBDDQS_A:::55	3	:::150			200	300 MHZ	20D7 21C3
	FBACLK0	GPU_FBCLK_A:::50	3	:::150			200	300 MHZ	20D7 21C3
	RFBACLK0_L	RAM_FBCLK_A:::50	3	:::150			200	300 MHZ	20D7 21C3
	FBACLK1	GPU_FBCLK_A:::50	3	:::150			200	300 MHZ	20D7 21D3
	RFBACLK1_L	RAM_FBCLK_A:::50	3	:::150			200	300 MHZ	20D7 21D3
	FBACLK1	RAM_FBCLK_A:::80	3	:::2500			200	300 MHZ	21D1 22C2
	RFBACLK1_L	RAM_FBCLK_A:::80	3	:::2500			200	300 MHZ	21D1 22C2
	FBACLK0	RAM_FBCLK_A:::70	3	:::2500			200	300 MHZ	21C1 22C6
	RFBACLK0_L	RAM_FBCLK_A:::70	3	:::2500			200	300 MHZ	21C1 22C6
	FBD<64..127>	GPU_FBDDATA_B:::225	4	:::800				300 MHZ	20E5 20F5 20G5 21B5 21B8 21C5 21C8
	RFBD<64..127>	RAM_FBDDATA_B:::325	4	:::1000				300 MHZ	21B4 21B7 21C4 21C7 23B1 23B5 23C1 23C5
	FBDDQ<8..15>	GPU_FBDDQ_B:::120	4	:::800				300 MHZ	20C3 20D3 20D5
	RFBDQ<8..15>	RAM_FBDDQ_B:::120	4	:::1000				300 MHZ	20C2 20D2 23C2 23C6
	FBA<0..12>	GPU_FBADDR_B:::120	4	:::600				300 MHZ	20A3 20B3 20C3 20C5 20D5
	RFBA<0..12>	RAM_FBADDR_B:::370	5	:::2400	50			300 MHZ	20B2 20C2 23C2 23C6 23D2 23D6
	FBABA<0..3>	GPU_FBADDR_B:::120	4	:::600				300 MHZ	20A3 20C5
	RFBABA<0..3>	RAM_FBADDR_B:::370	5	:::2400	50			300 MHZ	20A2 23C2 23C6
	FBRAS_L	GPU_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20D4
	FRBAS_L	RAM_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20D4
	FBAWE_L	GPU_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20D4
	RFBAS_L	RAM_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20D4
	FBCS0_L	GPU_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20C4
	RFCS0_L	RAM_FBCNTL_B:::120	4	:::400				300 MHZ	20C3 20C4
	FBACKE	GPU_FBCNTL_B:::120	5	:::400	100			300 MHZ	20A3 20C4
	RFBAS_L	RAM_FBCNTL_B:::2000	5	:::3500	3550			300 MHZ	20C2 23B2 23B6
	RFBAS_L	RAM_FBCNTL_B:::2000	5	:::3500	3550			300 MHZ	20C2 23B2 23B6
	FBAWE_L	RAM_FBCNTL_B:::2000	5	:::3500	3550			300 MHZ	20C2 23B2 23B6
	RFBAS0_L	RAM_FBCNTL_B:::2000	5	:::3500	3550			300 MHZ	20C2 23B2 23B6
	RFBAS0_L	RAM_FBCNTL_B:::2000	5	:::3500	3550			300 MHZ	20A2 23C2 23C6
	FBDQS<8..15>	GPU_FBDDQS_B:::100	3	:::350		10 MIL SPACING		300 MHZ	20D4 21A5
	RFBDQS<8..15>	RAM_FBDDQS_B:::60	3	:::1500		10 MIL SPACING		300 MHZ	21A4
	FBDQSTERM<8..15>	FBDQSTERM_B:::50	3	:::150		10 MIL SPACING		300 MHZ	21A3 23C2 23C6
	RFBDQSTERM<8..15>	RAM_FBDDQS_B:::50	3	:::150			200	300 MHZ	20C5 21B3
	FBACLK0	GPU_FBCLK_B:::50	3	:::150			200	300 MHZ	20C5 21B3
	RFBACLK0_L	RAM_FBCLK_B:::50	3	:::150			200	300 MHZ	20C5 21B3
	FBACLK1	GPU_FBCLK_B:::50	3	:::150			200	300 MHZ	20C5 21C3
	RFBACLK1_L	RAM_FBCLK_B:::50	3	:::150			200	300 MHZ	20C5 21B3
	FBACLK1	RAM_FBCLK_B:::90	4	:::2500			200	300 MHZ	21C1 23C2
	RFBACLK1_L	RAM_FBCLK_B:::90	3	:::2500			200	300 MHZ	21B1 23C2
	FBACLK0	RAM_FBCLK_B:::90	3	:::2500			200	300 MHZ	21B1 23C6
	RFBACLK0_L	RAM_FBCLK_B:::90	3	:::2500			200	300 MHZ	21B1 23C6

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SIGNAL CONSTRAINTS

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DIGITAL SIGNALS

GROUP	SIG_NAME	MATCHED_DELAY	MAX_VIAS	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MAX_EXPOSED_LENGTH	
MAXBUS	CPU_ADDR<0..31>	CPU_ADDR_GROUP	71250	:::5000	250			166 MHZ		4B7 4C7 9B7 9B8 9C5 9C6 9C7 9C8 11C3 11D3 11D8
	CPU_DATA<0..63>	CPU_DATA_GROUP	7400	:::5000	1550			166 MHZ		5A4 5B4 5C4 5D4 9C5 9C6 9C7 9C8 9D5 9D6 9D7 9D8
	CPU_BR_L	CPU_CNTL_GROUP	7100	:::5000	250	10 MIL SPACING		166 MHZ		4D7 7C7 9C5 11D3 11B1 11B5 11B8 11C1 11C5 11D1 11D5
	CPU_BG_L	CPU_CNTL_GROUP	7100	:::5000	250	10 MIL SPACING		166 MHZ		4D7 7B7 9B5 11D3
	CPU_TS_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4D7 7C7 9C7 11D3
	CPU_TT<0..4>	CPU_CNTL_GROUP	7300	:::5000	250	10 MIL SPACING		166 MHZ		4B7 7A7 9B5 9B6 9C5 9C6 11B3
	CPU_TBST_L	CPU_CNTL_GROUP	7100	:::5000	250	10 MIL SPACING		166 MHZ		4B7 7B7 9B5 11B3
	CPU_TSHZ<0..2>	CPU_CNTL_GROUP	7260	:::5000	250	10 MIL SPACING		166 MHZ		4B7 9B6 9B7 9C6 11B3
	CPU_AKTRY_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4A7 7C7 9B8 11B3
	CPU_AACK_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4A7 7B7 9B6 11B3
	CPU_GBL_L	CPU_CNTL_GROUP	7000	:::1000	250	10 MIL SPACING		166 MHZ		4B8 9B6
	CPU_INT_GBL_L	CPU_CNTL_GROUP	5100	:::3500	250	10 MIL SPACING		166 MHZ		4B8 7B7 11C3
	CPU_CI_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4A7 7A7 9C6 11C3
	CPU_HIT_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4A7 7C7 9B8 11B3
	CPU_DBG_L	CPU_CNTL_GROUP	7000	:::3500	250	10 MIL SPACING		166 MHZ		4C3 7B7 9C8 11B1
	CPU_DRDY_L	CPU_CNTL_GROUP	5100	:::500	250	10 MIL SPACING		166 MHZ		4C2 7B7 9B6 11B1
	CPU_WT_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4B7 7A7 9B6 11B3
	CPU_DRDY_L_UP		2	:::5000	250	10 MIL SPACING		166 MHZ		4C3
	CPU_DTI<0..2>	CPU_CNTL_GROUP	7150	:::5000	250	10 MIL SPACING		166 MHZ		4C3 9B5 9B7 11A1
	CPU_TA_L	CPU_CNTL_GROUP	7100	:::5000	250	10 MIL SPACING		166 MHZ		4C3 7C7 9C5 11A1
	CPU_TEA_L	CPU_CNTL_GROUP	7100	:::5000	250	10 MIL SPACING		166 MHZ		4C3 7B7 9C6 11A1
	CPU_QREQ_L	CPU_CNTL_GROUP	7000	:::5000	250	10 MIL SPACING		166 MHZ		4C3 7D5 9B7 11B3
	CPU_QACK_L	CPU_CNTL_GROUP	1000	:::4000	250	10 MIL SPACING		166 MHZ		4C3 9B5 11B3
	SYSCLK_CPU_UP		2	:::150				166 MHZ	315	11A3
	SYSCLK_CPU		4	:::2200	2400 200	10 MIL SPACING		166 MHZ	315	4D2 11A4
	INT_CPU_FB_OUT		3	:::1000	200			166 MHZ	315	11B3
	CPU_FBO_PLUS1		3	:::200	200			166 MHZ	315	11A4
	CPU_FBI_PLUS1		3	:::1400	1500 200			166 MHZ	315	11A4
	CPU_FB_MINUS3		4	:::900	1000 200			166 MHZ	315	11A4
	INT_CPU_FB_IN		4	:::1000	200			166 MHZ	315	11B3
	CPU_FB_PLUS2		3	:::900	1000			166 MHZ	315	11A5
	CPU_FB_PLUS3		3	:::2900	3000			166 MHZ	315	11A4
	INT_ANALYZER_CLK		3	:::300				166 MHZ		9B4 11B4 18C7 56A7 61A7
	SYSCLK_LA		2	:::2000				166 MHZ		9B3 9D8
	INT_CLOCK_OUT		3	:::3000				166 MHZ		9C4
	MIN LINE WIDTH									
	USB2_XT1		3	:::1000	100	10 MIL SPACING		30 MHZ		DIFFERENTIAL_PAIR
USB2_XT2_B		3	:::1000	100	10 MIL SPACING		30 MHZ			34C4
USB2_XT2		3	:::100	100	10 MIL SPACING		30 MHZ			34C4
USB2_EREF		2	:::100							34B4
USB2_RSDAM	USB2_RSDA:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_RSDAP	USB2_RSDA:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_RSDBM	USB2_RSDB:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_RSDBP	USB2_RSDB:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_RSDCM	USB2_RSDC:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_RSDCP	USB2_RSDC:::20	2	:::500		8 MIL SPACING	3.5	480 MHZ			34C4
USB2_DAN_F	USB2_DMA:::30	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN_DAI5Y_CHAIN	34C1 34C4 35B7
USB2_DAP_F	USB2_DMA:::30	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN_DAI5Y_CHAIN	34C1 35B7
USB2_DBN_F	USB2_DMB:::20	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN_DAI5Y_CHAIN	34C1 35C7
USB2_DBP_F	USB2_DMB:::20	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN_DAI5Y_CHAIN	34C1 34C4 35C7
USB2_DCN_F	USB2_DMC:::20	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN_DAI5Y_CHAIN	34C1 35D7
USB2_DCP_F	USB2_DMC:::20	3	:::500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN_DAI5Y_CHAIN	34C1 35D7
USBT_DAN_F	USB2_DMAT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN_DAI5Y_CHAIN	35B6
USBT_DAP_F	USB2_DMAT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN_DAI5Y_CHAIN	35B6
USBT_DBN_F	USB2_DMBT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN_DAI5Y_CHAIN	35C6
USBT_DBP_F	USB2_DMBT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN_DAI5Y_CHAIN	35C6
USBT_DCN_F	USB2_DMCT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN_DAI5Y_CHAIN	35D6
USBT_DCP_F	USB2_DMCT:::60	4	:::3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN_DAI5Y_CHAIN	35D6
USB_DAN_CON	USB2_CONA:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN_DAI5Y_CHAIN	35C3 61C4
USB_DAP_CON	USB2_CONA:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN_DAI5Y_CHAIN	35C3 61C4
USB_DBN_CON	USB2_CONB:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN_DAI5Y_CHAIN	35B3 61C4
USB_DBP_CON	USB2_CONB:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN_DAI5Y_CHAIN	35B3 61C4
USB_DCN_CON	USB2_CONC:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN_DAI5Y_CHAIN	35D3 61C4
USB_DCP_CON	USB2_CONC:::30	2	:::750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN_DAI5Y_CHAIN	35D3 61C4

SIGNAL CONSTRAINTS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6496	A
SCALE	SHT	OF	
NONE	58	74	

DIGITAL SIGNALS

GROUP	SIG_NAME	MATCHED_DELAY	MAX_VIAS	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	MIN_LINE_WIDTH	MAX_EXPOSED_LENGTH	PULSE_PARAM
NEW	VSYNC*		3	:::1000					24C5
STUFF	ANALOG_VSYNC*		4	:::3500					24C8 27C6 28B5 61B7
HERE	HSYNC*		3	:::1000					24C5
	ANALOG_HSYNC*		5	:::3500					24C8 27C4 27D6 28B5 61B7
	ANALOG_BLU		4	:::4000	200	10 MIL SPACING	5.8		24C5 24C8 27C6
	ANALOG_GRN		4	:::4000	200	10 MIL SPACING	5.8		24C5 24C8 27C6
	ANALOG_RED		4	:::4000	200	10 MIL SPACING	5.8		24C5 24C8 27B6
	FILT_ANALOG_RED		2	:::500		10 MIL SPACING	5.8		27C5 61B7
	FILT_ANALOG_GRN		2	:::500		10 MIL SPACING	5.8		27C5 61B7
	FILT_ANALOG_BLU		2	:::500		10 MIL SPACING	5.8		27C5 61B7
	DAC2RSET			:::1000		10 MIL SPACING			24C6
	DAC2VREF			:::1000		10 MIL SPACING			24C5
	NV11_XTALIN		4	:::1000	100	8 MIL SPACING		27 MHZ	24B4
	NV11_XTALOUT		4	:::1000	100	8 MIL SPACING		27 MHZ	24B4
	INT_TMDS_CK	TMDS:::120	3		50	8 MIL SPACING	TMDS_CLK		25D2 26B6 61A7
	INT_TMDS_CKM	TMDS:::120	3		50	8 MIL SPACING	TMDS_CLK		25D2 26A6 61A7
	INT_TMDS_D0P	TMDS:::120	3		50	8 MIL SPACING	TMDS_D0		25D2 26B6 61B7
	INT_TMDS_D0M	TMDS:::120	3		50	8 MIL SPACING	TMDS_D0		25D2 26B6 61A7
	INT_TMDS_D1P	TMDS:::120	3		50	8 MIL SPACING	TMDS_D1		25D2 26C6 61B7
	INT_TMDS_D1M	TMDS:::120	3		50	8 MIL SPACING	TMDS_D1		25D2 26C6 61B7
	INT_TMDS_D2P	TMDS:::120	3		50	8 MIL SPACING	TMDS_D2		25C2 26D6 61B7
	INT_TMDS_D2M	TMDS:::120	3		50	8 MIL SPACING	TMDS_D2		25C2 26D6 61B7
	TCKP	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_CLK		26B5 26C4
	TCKM	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_CLK		26A5 26C3
	TD0P	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D0		26B5 26C3
	TD0M	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D0		26B5 26C4
	TD1P	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D1		26C4 26C5
	TD1M	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D1		26C3 26C5
	TD2P	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D2		26C3 26D5
	TD2M	TMDSFILT:::50	2		20	8 MIL SPACING	TMDSFILT_D2		26C4 26D5
	ENET_LINK_TX_EN		4	:::1000				25 MHZ	36D6
	ENET_LINK_TX_ER		4	:::1000				25 MHZ	36D6
	ENET_LINK_TXD<0..3>		4	:::1000				25 MHZ	36C6
	ENET_PHY_TX_EN		4	:::5600				25 MHZ	36D7 37C6
	ENET_PHY_TX_ER		4	:::5600				25 MHZ	36D7 37C6
	ENET_PHY_TXD<0..3>		4	:::4600:5600				25 MHZ	36C7 37C6
	CLKENET_LINK_TX		4	:::4600:5600				25 MHZ	36D7 37C8
	CLKENET_PHY_TX		4	:::1000				25 MHZ	37C6
	CLKENET_LINK_RX		4	:::4600:5600				25 MHZ	36C7 37C8
	CLKENET_PHY_RX		4	:::1000				25 MHZ	37C6
	ENET_PHY_RXD<0..3>		4	:::1000				25 MHZ	37B6 37C6
	ENET_PHY_RX_DV		4	:::1000				25 MHZ	37B6
	ENET_PHY_RX_ER		4	:::1000				25 MHZ	37B6
	ENET_PHY_CRS		4	:::1000				25 MHZ	37B6
	ENET_PHY_COL		4	:::1000				25 MHZ	37B6
	ENET_LINK_RXD<0..3>		4	:::4600:5600				25 MHZ	36C7 37B8 37C8
	ENET_CRS		4	:::4600:5600				25 MHZ	36C7 37B8
	ENET_COL		4	:::4600:5600				25 MHZ	36B7 37B8
	ENET_RX_DV		4	:::4600:5600				25 MHZ	36C7 37B8
	ENET_RX_ER		4	:::4600:5600				25 MHZ	36C7 37B8
	CLK25M_ENET_XIN		3	:::1000	100	8 MIL SPACING			25 MHZ 37B6
	CLK25M_ENET_XOUT		3	:::1000	100	8 MIL SPACING			25 MHZ 37B6
	ENET_TDP	ETHTD:::70	3	:::4000	3150	10 MIL SPACING	ETH_TXD	100 MHZ	37C3
	ENET_TDM	ETHTD:::70	3	:::4000	3150	10 MIL SPACING	ETH_TXD	100 MHZ	37C3
	ENET_RDP	ETHRD:::70	3	:::4000	3150	10 MIL SPACING	ETH_RXD	100 MHZ	37C3
	ENET_RDM	ETHRD:::70	3	:::4000	3150	10 MIL SPACING	ETH_RXD	100 MHZ	37C3
	RJ45_TAP	RJTXD:::70	2	:::750		2KV ISO	RJ45_TXD	100 MHZ	37C1 37C2
	RJ45_TXN	RJTXD:::70	2	:::750		2KV ISO	RJ45_TXD	100 MHZ	37C1 37C2
	RJ45_RXP	RJRXD:::70	2	:::750		2KV ISO	RJ45_RXD	100 MHZ	37C1 37C2
	RJ45_RXN	RJRXD:::70	2	:::750		2KV ISO	RJ45_RXD	100 MHZ	37C1 37C2
	RJ45_TREF					2KV ISO			37C2
	RJ45_RREF					2KV ISO			37C2
	RJ45_4_5					2KV ISO			37C1
	RJ45_7_8					2KV ISO			37C1
	RJ45_F_TREF					2KV ISO			37B2
	FW_LINK_DATA<0..7>		4	:::1000					36C5
	FW_LINK_CNTRL<0..1>		4	:::1000				49.152 MHZ	36C5
	FW_LINK_LREQ		4	:::1000				49.152 MHZ	36C5
	FW_SCLK		4	:::3500:4500				49.152 MHZ	36C5 38C8
	FW_D<0..7>		4	:::3700:4700				49.152 MHZ	36C3 38B8 38C8
	FW_CNTRL0		4	:::3700:4700				49.152 MHZ	36C3 38C8
	FW_CNTRL1		4	:::3700:4700				49.152 MHZ	36C3 38C8
	FW_LREQ		4	:::3700:4700				49.152 MHZ	36C3 38C8
	FW_PHY_SCLK		4	:::500				49.152 MHZ	38C7
	FW_PHY_CNTRL0		4	:::1000				49.152 MHZ	38C7
	FW_PHY_CNTRL1		4	:::1000				49.152 MHZ	38C7
	FW_PHY_D<0..7>		4	:::1000				49.152 MHZ	38B7 38C7
	FW_X1		3	:::1000	100	8 MIL SPACING		24.576 MHZ	38C6
	FW_X0		3	:::1000	100	8 MIL SPACING		24.576 MHZ	38C6
	FW_BIAS1								38C5
	FW_BIAS2								38C5
	FW_TPA1P	FWTPA1:::50	3	:::1220	5000		FW_TPA1	400 MHZ	38C5
	FW_TPA1N	FWTPA1:::50	3	:::1220	5000		FW_TPA1	400 MHZ	38C5
	FW_TPB1P	FWTPB1:::50	3	:::1220	5000		FW_TPB1	400 MHZ	38C5
	FW_TPB1N	FWTPB1:::50	3	:::1220	5000		FW_TPB1	400 MHZ	38C5
	FW_TPA2P	FWTPA2:::50	3	:::1220	5000		FW_TPA2	400 MHZ	38C5
	FW_TPA2N	FWTPA2:::50	3	:::1220	5000		FW_TPA2	400 MHZ	38C5
	FW_TPB2P	FWTPB2:::50	3	:::1220	5000		FW_TPB2	400 MHZ	38C5
	FW_TPB2N	FWTPB2:::50	3	:::1220	5000		FW_TPB2	400 MHZ	38C5
	FW_TPO1P	FWTPO1:::50	3	:::1220	5000		FW_TPO1	400 MHZ	38D1
	FW_TPO1N	FWTPO1:::50	3	:::1220	5000		FW_TPO1	400 MHZ	38A8 38D1
	FW_TPL1P	FWTPL1:::50	3	:::1220	5000		FW_TPL1	400 MHZ	38A8 38D1
	FW_TPL1N	FWTPL1:::50	3	:::1220	5000		FW_TPL1	400 MHZ	38A8 38D1
	FW_TPO2P	FWTPO2:::50	3	:::1220	5000		FW_TPO2	400 MHZ	38A8 38C1
	FW_TPO2N	FWTPO2:::50	3	:::1220	5000		FW_TPO2	400 MHZ	38A8 38C1
	FW_TPL2P	FWTPL2:::50	3	:::1220	5000		FW_TPL2	400 MHZ	38A8 38C1
	FW_TPL2N	FWTPL2:::50	3	:::1220	5000		FW_TPL2	400 MHZ	38A8 38C1

SIGNAL CONSTRAINTS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6496	A
SCALE	NONE	SHT	59 OF 74

DIGITAL SIGNALS (CONT'D)

GROUP	SIG_NAME	MATCHED_DELAY	MAX_VIAS	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM
CD DRIVE BUS	EIDE_RST_L			:::3500:5500				33 MHZ 39A7 39D5
	EIDE_DMACK_L			:::3500:5500				33 MHZ 39A7 39D5
	EIDE_STOP			:::5500				33 MHZ 39A7 39D5
	EIDE_HSTB_RDY			:::5500				33 MHZ 39A7 39C5
	EIDE_DSTB_RDY			:::3500:5500				33 MHZ 39A7 39C5
	EIDE_DATA<0..15>			:::3500:5500				33 MHZ 39A5 39B5 39B7 39C5
	CD_RESET_L			:::1000				33 MHZ 39D4 40C6
	CD_DMACK_L			:::4000				33 MHZ 39D4 40C6
	CD_STOP			:::5000				33 MHZ 39D4 40C6
	CD_HSTB_RDY			:::5000				33 MHZ 39C4 40C6
	CD_DSTB_RDY			:::1000				33 MHZ 39C4 40C6
	UATA<0..15>			:::1000				33 MHZ 39A4 39B4 39C4 40C6
	CD_DMARQ			:::1000				33 MHZ 40C6
	EIDE_DMARQ			:::3500:5500				33 MHZ 39A7 40C8
	UATA<IO>			:::1000				33 MHZ 40C6
	EIDE_INTRO			:::3500:5500				33 MHZ 39A7 40C8
	CD_EIDE_ADDR<0..2>			:::1000				33 MHZ 40C6
	EIDE_ADDR<0..2>			:::3500:5500				33 MHZ 39B7 40A8 40B8
	CD_CS1FX_L			:::1000				33 MHZ 40C6
	EIDE_CS1FX_L			:::3500:5500				33 MHZ 39A7 40B8
CD_CS3FX_L			:::1000				33 MHZ 40C6	
EIDE_CS3FX_L			:::3500:5500				33 MHZ 39A7 40B8	
HD DRIVE BUS	UIDE_RST_L	HD_DATA:::5500		:::100:6000	500			100 MHZ 39C7 39D3
	UIDE_DMACK_L	HD_DATA:::5500		:::100:6000	500			100 MHZ 39C7 39D3
	UIDE_DIOR_L	HD_DATA:::5500		:::100:6000				100 MHZ 39C7 39D3
	UIDE_DIOW_L	HD_DATA:::5500		:::6000				100 MHZ 39C3 39C7
	UIDE_IOCHRDY	HD_DATA:::5500		:::100:6000	500			100 MHZ 39C3 39C7
	UIDE_DATA<0..15>	HD_DATA:::5500		:::100:6000				100 MHZ 39A3 39B3 39C3 39C7 39D7
	HD_RESET_L			:::1000				100 MHZ 39D1 40C3
	HD_DMACK_L			:::1000				100 MHZ 39D1 40C3
	HD_DIOR_L			:::5500				100 MHZ 39D1 40C3
	HD_DIOW_L			:::5500				100 MHZ 39C1 40C3
	HD_IOCHRDY			:::1000				100 MHZ 39C1 40C3
	HD_DMARQ			:::1000				100 MHZ 40C3
	UIDE_DMARQ	HD_DATA:::5500		:::100:6000				100 MHZ 39C7 40C4
	HD_INTRO			:::1000	500			100 MHZ 40C3
	UIDE_INTRO	HD_DATA:::5500		:::100:6000				100 MHZ 39C7 40C4
	HD_UIDE_ADDR<0..2>			:::1000				100 MHZ 40C2 40C3
	UIDE_ADDR<0..2>	HD_DATA:::5500		:::100:6000				100 MHZ 39C7 40A4 40B4
	HD_UIDE_CS1FX_L			:::6000				100 MHZ 40C3
	UIDE_CS1FX_L	HD_DATA:::5500		:::6000				100 MHZ 39C7 40B4
	HD_UIDE_CS3FX_L			:::6000				100 MHZ 40C2
UIDE_CS3FX_L	HD_DATA:::5500		:::6000				100 MHZ 39C7 40B4	
CLK_18M_INT_XOUT			3	:::1000	100	8 MIL SPACING	18.432 MHZ 60B5	
CLK_18M_INT_XOUT			3	:::1000	100	8 MIL SPACING	18.432 MHZ 60B5	
CLK_18M_INT_XOUT			3	:::200	50	8 MIL SPACING	18.432 MHZ 60B5	
USB_DAP	USBA:::500						30B3	
USB_DAN	USBA:::500						30B3	
USB_DAP_F	USBA_F:::500				100		30B2 35B7	
USB_DAN_F	USBA_F:::500				100		30B2 35B7	
USB_DBP	USBB:::500						30B3	
USB_DBN	USBB:::500						30B3	
USB_DBP_F	USBB_F:::500				100		30B2 35C7	
USB_DBN_F	USBB_F:::500				100		30B2 35C7	
USB_DCP	USBC:::500						30B3	
USB_DCN	USBC:::500						30B3	
USB_DCP_F	USBC_F:::500				100		30B2 35D7	
USB_DCN_F	USBC_F:::500				100		30B2 35D7	
USB_DEP	USBE:::500						30B3	
USB_DEN	USBE:::500						30B3	
BT_USB_DP	USBE_F:::500				100		30B2 31D3 61B4	
BT_USB_DM	USBE_F:::500				100		30B2 31D3 61B4	
USB_DFP	USBF:::500						30B3	
USB_DFN	USBF:::500						30B3	
MODEM_USB_DP	USBF_F:::500				100		30B2 31C5 61B4	
MODEM_USB_DM	USBF_F:::500				100		30B2 31C5 61B4	
PMU_X0			3	:::1000	100	8 MIL SPACING	10 MHZ 46B5	
PMU_X1			3	:::1000	100	8 MIL SPACING	10 MHZ 46B5	
PMU_XT			3	:::300	50	8 MIL SPACING	10 MHZ 46A6	
PMU_CLKOUT			3	:::1000	100	8 MIL SPACING	32.768 MHZ 46B4	
PMU_CLKIN			3	:::1000	100	8 MIL SPACING	32.768 MHZ 46B4	
PMU_CLKT			3	:::300	50	8 MIL SPACING	32.768 MHZ 46B2	
MICSHLD						10 MIL SPACING	31A5 45B8 61A7	
MICHIGH						10 MIL SPACING	31A5 45C8 61A7	
MICLOW						10 MIL SPACING	31A5 45B8 61A7	
KS_INT_SPKR+						10 MIL SPACING	31A3 44C3 61B7	
KS_INT_SPKR-						10 MIL SPACING	31A3 44C3 61B7	

SIG_NAME	DELAY_RULE	PULSE_PARAM
T_UD_IDEDD_0	:::1000	100 MHZ 39C1 40C3
T_UD_IDEDD_1	:::1000	100 MHZ 39C1 40C3
T_UD_IDEDD_2	:::1000	100 MHZ 39C1 40C3
T_UD_IDEDD_3	:::1000	100 MHZ 39C1 40C3
T_UD_IDEDD_4	:::1000	100 MHZ 39B1 40C3
T_UD_IDEDD_5	:::1000	100 MHZ 39B1 40C3
T_UD_IDEDD_6	:::1000	100 MHZ 39B1 40C3
T_UD_IDEDD_7	:::1000	100 MHZ 39B1 40C3
T_UD_IDEDD_8	:::1000	100 MHZ 39B1 40C2
T_UD_IDEDD_9	:::1000	100 MHZ 39B1 40C2
T_UD_IDEDD_10	:::1000	100 MHZ 39B1 40C2
T_UD_IDEDD_11	:::1000	100 MHZ 39B1 40C2
T_UD_IDEDD_12	:::1000	100 MHZ 39A1 40C2
T_UD_IDEDD_13	:::1000	100 MHZ 39A1 40C2
T_UD_IDEDD_14	:::1000	100 MHZ 39A1 40C2
T_UD_IDEDD_15	:::1000	100 MHZ 39A1 40C2

SIGNAL CONSTRAINTS

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	D	051-6496	A
SCALE	NONE	SHT	60 OF 74

FUNC_TEST

+1_SV_MAIN	FUNC_TEST	54C4
+12V_MAIN	FUNC_TEST	53B7 53D7 54C1
+12V_SLEEP	FUNC_TEST	38D8 41C8 44D8 46D8 47B4 47D3 47D7 50C4 50C8 50D6
+12V_SLEEPA	FUNC_TEST	31A3 31A8 31C5 52D6 53A4 53D6 54C1
+5V_MAIN	FUNC_TEST	54C4
+5V_SLEEP	FUNC_TEST	48C7 48D6 52C6 53A5 53C5
+2_5V_MAIN	FUNC_TEST	32A3 54C4
+3V_MAIN	FUNC_TEST	41D4 42D5 43A5 43A7 44A7 44D4 54C4
CPU_VCORE_SLEEP	FUNC_TEST	4D3 4D7 9B6 9C2 47B3 47C1 54C6 61B4
JTAG_ASIC_TCK	FUNC_TEST	9A3 36B7 37C4
JTAG_ASIC_TDI	FUNC_TEST	9A3 30C6 36B7
JTAG_ASIC_TDO	FUNC_TEST	9A3 37B4
JTAG_ASIC_TMS	FUNC_TEST	9A3 36B7 37A2 37B4
JTAG_ASIC_TRST_L	FUNC_TEST	9A3 36B7
INT_TMS_3V	FUNC_TEST	26B3 26C3 26C4 26D5 54A6
+1_5V_AGP	FUNC_TEST	12D6 13C8 18A8 18C2 18D7 19A4 19D5 48B4 54C3
FAN_12V_FILT	FUNC_TEST	31A5 54B3
+INTREFID_CORE_MAIN	FUNC_TEST	12D6 13D4 48B3 49B2
INTREFID_VSENSE	FUNC_TEST	49C6
OVDD_ADJ	FUNC_TEST	
CPU_CHKSTP_OUT_L	FUNC_TEST	4B3 7B5 9A2 9D6
CPU_CHKSTP_IN_L	FUNC_TEST	4B3 7B5
CPU_HRESET_L	FUNC_TEST	4B3 7A3 7A5 7B3 8D2 9A2 46C2 46D2
JTAG_CPU_TCK	FUNC_TEST	4C3 7D5 8C2 9A2
JTAG_CPU_TDI	FUNC_TEST	4C3 7A5 8D2 9A2
JTAG_CPU_TDO	FUNC_TEST	4C3 9A2
JTAG_CPU_TMS	FUNC_TEST	4C3 7A5 8D2 9A2
JTAG_CPU_TRST_L	FUNC_TEST	4C3 7C5 8D2 9A2
+MAXBUS_SLEEP	FUNC_TEST	4D5 6D8 7A3 7B3 7C3 7C5 7C7 8D3 9B2 9D2
ROM_CS_L	FUNC_TEST	9D4 11B8 11D8 46B7 46D1 46D2 47D2 48D4 54C6
ROM_OE_L	FUNC_TEST	32B4 32B6 33B4
ROM_RM_L	FUNC_TEST	32B2 32B6 33B2
DDC_VCC_3	FUNC_TEST	32B2 32B6 33B4
DDC_VCC_5	FUNC_TEST	26A5 26B3 54B6
SND_HP_SENSE	FUNC_TEST	27C4 54A6
ANALOG_HSYNC*	FUNC_TEST	30B5 43A5
ANALOG_VSYNC*	FUNC_TEST	24C8 27C4 27D6 28B5 59D3
FILT_ANALOG_BLU	FUNC_TEST	24C8 27C6 28B5 59D3
FILT_ANALOG_RED	FUNC_TEST	27C5 59D3
FILT_ANALOG_GRN	FUNC_TEST	27C5 59D3
GND	FUNC_TEST	27C5 59D3
KS_INT_SPKR+	FUNC_TEST	31A3 44C3 60A5
KS_INT_SPKR-	FUNC_TEST	31A3 44C3 60A5
INT_TMS_D2P	FUNC_TEST	25C2 26D6 59C3
INT_TMS_D2M	FUNC_TEST	25C2 26D6 59C3
INT_TMS_D1P	FUNC_TEST	25D2 26C6 59C3
INT_TMS_D1M	FUNC_TEST	25D2 26C6 59C3
INT_TMS_D0P	FUNC_TEST	25D2 26B6 59C3
INT_TMS_D0M	FUNC_TEST	25D2 26B6 59C3
INT_TMS_CKX	FUNC_TEST	25D2 26B6 59D3
INT_TMS_CKM	FUNC_TEST	25D2 26A6 59D3
INV_CUR_H1_FILT	FUNC_TEST	31A5
IO_RESET_L	FUNC_TEST	34A6 37B8 46B5 46B8 46D3
KS5VSD	FUNC_TEST	31A5 54B3
INT_I2C_CLK2	FUNC_TEST	30A3 30D1 31C7 36B5 41B1
INT_I2C_DATA2	FUNC_TEST	30A3 30D1 31C7 36B5 41B1
INT_ANALYZER_CLK	FUNC_TEST	9B4 11B4 18C7 56A7 58B3
LAMP_STS_FILT	FUNC_TEST	31A5
LCD_PWM_FILT	FUNC_TEST	31A5
LED_SV_FILT	FUNC_TEST	31A5 54B3
LED_RET_FILT	FUNC_TEST	31A5 54A3
MICSHLD	FUNC_TEST	31A5 45B8 60A5
MICHIGH	FUNC_TEST	31A5 45C8 60A5
MICLOW	FUNC_TEST	31A5 45B8 60A5
COMM_RESET_L	FUNC_TEST	30C5 31D5
IIC_ADD	FUNC_TEST	31C6
ROM_WP_L	FUNC_TEST	32A2

FUNC_TEST

COMM_SHUTDOWN	FUNC_TEST	30C5 30D1 31D7
MON_DETECT	FUNC_TEST	25D6 27C6
FLO_KNWS_BEST	FUNC_TEST	47C6 47C7 47C8
NMI_BUTTON*	FUNC_TEST	31B2 46C4
PWR_SWITCH*	FUNC_TEST	9A8 46B1 46C5 61D4
PMU_RST*	FUNC_TEST	9A8 31B3 46A5 46B5
PMURRESETBUTTON*	FUNC_TEST	46A4
PWR_SWITCH*	FUNC_TEST	9A8 46B1 46C5 61D4
PWR_UP	FUNC_TEST	41C8 52C4 52C8 53B7 53C1 53C7
POWER_UP*	FUNC_TEST	46C7 53A8
RESET_BUTTON*	FUNC_TEST	31B2 46C4
COMM_RING_DET_L	FUNC_TEST	30B5 30B8 31C5 46C5
ROM_ONBOARD_CS_L	FUNC_TEST	32B2 33B4
COMM_DTR_L	FUNC_TEST	30C3 31C7
COMM_TXD_L	FUNC_TEST	30C3 31C7
COMM_TXC	FUNC_TEST	30C3 30D2 31C7
COMM_RTS_L	FUNC_TEST	30C3 31D5
COMM_RXD	FUNC_TEST	30C3 31C5
COMM_GPIO_L	FUNC_TEST	30C3 30D2 31C5
SLEEP	FUNC_TEST	46B5 52C4
CPU_SRESET_L	FUNC_TEST	4B3 7A5 9A2
PMU_AVCC	FUNC_TEST	46B5 46D4 54B3
TMS_DDC_CLK	FUNC_TEST	26A5 26B3
TMS_DDC_DAT	FUNC_TEST	26A5 26B4
USB_DCN_CON	FUNC_TEST	35D3 58A3
USB_DCP_CON	FUNC_TEST	35D3 58A3
USB_DBN_CON	FUNC_TEST	35B3 58A3
USB_DRP_CON	FUNC_TEST	35B3 58A3
USB_DAN_CON	FUNC_TEST	35C3 58A3
USB_DAP_CON	FUNC_TEST	35C3 58A3
BT_USB_DP	FUNC_TEST	30B2 31D3 60B5
BT_USB_DM	FUNC_TEST	30B2 31D3 60A5
MODEM_USB_DP	FUNC_TEST	30B2 31C5 60A5
MODEM_USB_DM	FUNC_TEST	30B2 31C5 60A5
USB_PORT_PWR	FUNC_TEST	35A4 35B3 35C3 35D3 54A3
VGA_IIC_CLK	FUNC_TEST	27C4
VGA_IIC_DAT	FUNC_TEST	27C4
CPU_VCORE_SLEEP	FUNC_TEST	4D3 4D7 9B6 9C2 47B3 47C1 54C6 61D7
LINK_IN_COM	FUNC_TEST	42B7
LINK_IN_R	FUNC_TEST	42B6 42B7
LINK_IN_SENSE	FUNC_TEST	42B7 42C7
LINK_IN_L	FUNC_TEST	42B7 42C7
SND_LIN_SENSE	FUNC_TEST	30B5 42D4
OUT_R	FUNC_TEST	
LINEOUT_COMM2	FUNC_TEST	
LINE_OUT_L	FUNC_TEST	
PCIT_IRDY_L	FUNC_TEST	33B6 33C3 56C7
RF_CLKRUN_L	FUNC_TEST	33C3
NC_RF_DISABLE_L	FUNC_TEST	
PCI_DEVSEL_L	FUNC_TEST	32A8 32C5 33B7 34B6 56D7
PCI_STOP_L	FUNC_TEST	32A8 32C5 33B7 34B6 56D7
PCI_TRDY_L	FUNC_TEST	32B8 32C5 33B7 34B6 56D7
PCI_FRAME_L	FUNC_TEST	32B8 32C5 33B7 34B6 55A6
PCI_PAR	FUNC_TEST	32C5 33B7 34B6 56D7
WL_PCI_IDSEL	FUNC_TEST	33C2
33SLOTR_INT_L	FUNC_TEST	30B7 33C2
PMU_PME_L	FUNC_TEST	30B5 33C2 34A7 46B2
PCI_SLOTB_GNT_L	FUNC_TEST	32A6 32D5 33C2
CLK33M_PCI_SLOTB	FUNC_TEST	32D7 33C2 56D7
PCI_SLOTB_REQ_L	FUNC_TEST	32A8 32D5 33C3
MAIN_RESET_L	FUNC_TEST	32A2 33D4 34A6 46C4
PCI_CBE<0>	FUNC_TEST	32C5 33B7 34B6 55A6
PCIT_CBE<1>	FUNC_TEST	33B6 33C3 56C7
PCIT_CBE<2>	FUNC_TEST	33B6 33C3 56C7
PCIT_CBE<3>	FUNC_TEST	33B6 33C3 56C7
UNUSED_GPIO15	FUNC_TEST	30B5 30C1


FUNC_TEST

PCI_AD<0>	FUNC_TEST	32B2 32D4 33C7 34C6 55A6
PCIT_AD<1>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<2>	FUNC_TEST	33B2 33C6 56C7
PCIT_AD<3>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<4>	FUNC_TEST	32B2 32D4 33C7 34C6 55A6
PCIT_AD<5>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<6>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<7>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<8>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<9>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<10>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<11>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<12>	FUNC_TEST	33B3 33C6 56C7
PCIT_AD<13>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<14>	FUNC_TEST	33C3 33C6 56C7
PCIT_AD<15>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<16>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<17>	FUNC_TEST	33C3 33C7 56C7
PCIT_AD<18>	FUNC_TEST	32B2 32C4 33C7 34C6 55A6
PCIT_AD<19>	FUNC_TEST	33C3 33C7 56C7
PCIT_AD<20>	FUNC_TEST	32B2 32C4 33C6 34C6 55A6
PCIT_AD<21>	FUNC_TEST	33C3 33C6 56C7
PCIT_AD<22>	FUNC_TEST	32C4 33C6 34C6 55A6
PCIT_AD<23>	FUNC_TEST	33C3 33C6 56C7
PCIT_AD<24>	FUNC_TEST	32B1 32C4 33B6 34C6 55A6
PCIT_AD<25>	FUNC_TEST	33B6 33C3 56C7
PCIT_AD<26>	FUNC_TEST	32B1 32C4 33B6 34B6 55A6
PCIT_AD<27>	FUNC_TEST	33B6 33C3 56C7
PCIT_AD<28>	FUNC_TEST	33B7 33C2 56C7
PCIT_AD<29>	FUNC_TEST	33B6 33C3 56C7
PCIT_AD<30>	FUNC_TEST	32B1 32C4 33B6 34B6 55A6
PCIT_AD<31>	FUNC_TEST	33B6 33C3 56C7

CONSTRAINT TABLES

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	D	051-6496	A
SCALE	NONE	SHT	61 OF 74

	8	7	6	5	4	3	2	1		
	<p>*** Signal Cross-Reference *** --- for the entire design --</p> <p>+1_5V_AGP 12D6 13C8 18A8 18C2 18D7 19A4 19D5 48B4 54C3 61C7</p> <p>+1_5V_INTREPID_PLL 11D3 18D6 30D6 32D5 54D3</p> <p>+1_5V_INTREPID_PLL1 30C4 54D3</p> <p>+1_5V_INTREPID_PLL2 30D4 54D3</p> <p>+1_5V_INTREPID_PLL3 30D4 54D3</p> <p>+1_5V_INTREPID_PLL4 30D4 54D3</p> <p>+1_5V_INTREPID_PLL5 18D5 54D3</p> <p>+1_5V_INTREPID_PLL6 32D4 54D3</p> <p>+1_5V_INTREPID_PLL7 11D2 54D3</p> <p>+1_5V_INTREPID_PLL8 30D4 54D3</p> <p>+1_8V_MAIN 54C4 61D7</p> <p>+2_5V_ENET 37C3 37D3 37D5 54C6</p> <p>+2_5V_DDR_AVDD 10D4 54D6</p> <p>+2_5V_DDR_VDD 10D5 54D6</p> <p>+2_5V_MAIN 32A3 54C4 61D7</p> <p>+3.3VFPD 26D6 53C1 54B6</p> <p>+3V_AUDIO 41D2 41D6 41D7 42C3 45C2 45D5</p> <p>+3V_INTREPID_USB 30C4 54A3</p> <p>+3V_INTSS_AVDD 10B7 54D6</p> <p>+3V_INTSS_VDD 10B6 54D6</p> <p>+3V_MAIN 41D4 42D5 43A5 43A7 44A7 44D4 54C4 61D7</p> <p>+5VSD_T 52D7</p> <p>+5V_AUDIO 41C6 41D7 43B8</p> <p>+5V_HP 43A8 43B7 43D5</p> <p>+5V_MAIN 54C4 61D7</p> <p>+5V_SLEEP 48C7 48D6 52C6 53A5 53C5 61D7</p> <p>+12VSD_FILT 31A5 54B3</p> <p>+12VSD_T 52D7</p> <p>+12V_DROPPED 46D8</p> <p>+12V_MAIN 38D8 41C8 44D8 46D8 47B4 47D3 47D7 50C4 50C8 50D6 51C4 51D4 51D7 52B4 52C4 52C6 52D4 52D6 53A4 53A7 53B7 53D7 54C1 61D7</p> <p>+12V_SLEEP 31A3 31A8 31C5 52D6 53A4 53D6 54C1 61D7</p> <p>+12V_SLEEPA 61D7</p> <p>+INTREPID_CORE_MAIN 12D6 13D4 48B3 49B2 61C7</p> <p>+MAXBUS_SLEEP 4D5 6D8 7A3 7B3 7C3 7C5 7C7 8D3 9B2 9D2 9D4 11B8 11D8 46B7 46D1 46D2 47D2 48D4 54C6 61C7</p> <p>3.8VH_TRICKLE 46C1 46D7 54B3</p> <p>3.8V_TRICKLE 46C2 46C6 46D7 52D6 54C1 54C2</p> <p>3_5_HONKER 53C4</p> <p>3_6V_SLEEP 39D1 53C1</p> <p>5V_USB_FUSED 35A7</p> <p>5V_XRA 52B4</p> <p>25V_BSTH 51C5 51C6</p> <p>25V_BSTH_TERM 51C5</p> <p>25V_COMP 51B6</p> <p>25V_COMP_DWN 51B6</p> <p>25V_DH 51B5</p> <p>25V_DHT 51B5</p> <p>25V_DL 51B5</p> <p>25V_DLT 51B4</p> <p>25V_GND 51B6</p> <p>25V_NET99 51C3</p> <p>25V_OCSET 51C5</p> <p>25V_OVP 51B6</p> <p>25V_VCC 51C6</p> <p>25V_VPWR 51B5 51C5</p> <p>25V_VPWRA 51B4</p> <p>25V_VSENSE 51C3 51C5</p> <p>25_CORE_1 51C3</p> <p>33PCI_SLOTD_SERR_L 34B6</p> <p>33SLOTB_INT_L 30B7 33C2 61A4</p> <p>2059_IIC_CLK 10C5</p> <p>2059_IIC_DAT 10C5</p> <p>A0_IIC_MCK 10A4 10C5</p> <p>A1_IIC_MCK 10A4 10C5</p> <p>AGND 54C4</p> <p>AGPIO_VPWR 48B6</p> <p>AGP_AD<31..0> 18B4 18C4 19C8 19D8 56C7</p> <p>AGP_AD_STB<1..0> 18A4 18B3 19B8 56C7</p> <p>AGP_AD_STB_GPUUF<1..0> 19B7 56B7</p> <p>AGP_AD_STB_L<1..0> 18A4 18D1 19B8 56C7</p> <p>AGP_AD_STB_L_GPUUF<1..0> 19B7 56B7</p>		<p>AGP_BUSY_L 18C6 18D1 18D3 19A8 56B7</p> <p>AGP_CBE<3..0> 18B4 19C8 56C7</p> <p>AGP_DEVSEL_L 18B4 18C3 19B8 56C7</p> <p>AGP_FBI_EQUAL 18C7 56A7</p> <p>AGP_FBO_EQUAL 18B7 56A7</p> <p>AGP_FB_PLUS2 18B8 56A7</p> <p>AGP_FRAME_L 18B4 18C3 19B8 56C7</p> <p>AGP_GNT_L 18C3 18C4 19B7 56B7</p> <p>AGP_INT_L 19B7 30B5 30B8</p> <p>AGP_IRDY_L 18B4 18C3 19B8 56C7</p> <p>AGP_PAR 18B4 19B8 56B7</p> <p>AGP_PIPE_L 18A4 18B3 19B8 56B7</p> <p>AGP_PLLVDD 19C5</p> <p>AGP_RBF_L 18A4 18B3 19B8 56B7</p> <p>AGP_REQ_L 18C3 18C4 19B7 56B7</p> <p>AGP_RESET_L 19C7 46D3</p> <p>AGP_SBA<7..0> 18A4 18B1 18B4 18C1 19A8 56B7</p> <p>AGP_SB_STB 18A4 18B3 19A8 56B7</p> <p>AGP_SB_STB_L 18A4 18D1 19A8 56B7</p> <p>AGP_ST<2..0> 18A4 18B1 19B7 56B7</p> <p>AGP_STOP_L 18B3 18B4 19B8 56C7</p> <p>AGP_TRDY_L 18B3 18B4 19B8 56C7</p> <p>AGP_WBF_L 18A6 18B1 19B8 56B7</p> <p>AINLM 41C4</p> <p>AINLP 41C4</p> <p>AINRM 41C4</p> <p>AINRP 41C4</p> <p>ALTCHGND 54C4</p> <p>AMPBIAS 44B6</p> <p>AMPDC1 44B6</p> <p>AMPDC2 44B6</p> <p>AMPPFAULT 44B6 44B8</p> <p>AMPPUMP 44B6</p> <p>AMPRREF 44B6</p> <p>ANALOGGND 54C4</p> <p>ANALOG_BLU 24C5 24C8 27C6 59D3</p> <p>ANALOG_GRN 24C5 24C8 27C6 59D3</p> <p>ANALOG_HSYNC* 24C8 27C4 27D6 28B5 59D3 61B7</p> <p>ANALOG_RED 24C5 24C8 27B6 59D3</p> <p>ANALOG_VSYNC* 24C8 27C6 28B5 59D3 61B7</p> <p>ANEN 37C4</p> <p>AOUTL 41C1 43D7 44B8</p> <p>AOUTR 41C1 43C7 44C8</p> <p>ASH 45B6</p> <p>AUDIO_SPKR_ID_B 44C4</p> <p>AUDIO_TO_SND 30B2 30B3 41C1</p> <p>AUD_AMP_5V 44B8 44C6</p> <p>AUD_R_FB 41D6</p> <p>BB_MISO 8B4 8B6</p> <p>BB_MOSI 8B4 8B5 8B6</p> <p>BB_SCK 8B4 8B6</p> <p>BFR_HRESET_L 8B4 8C6</p> <p>BRCLKO 30A5</p> <p>BRE 47C5</p> <p>BRE_1 47B5</p> <p>BT1 46D6 53A5</p> <p>BT1_LED 53A5</p> <p>BT_USB_DM 30B2 31D3 60A5 61B4</p> <p>BT_USB_DP 30B2 31D3 60B5 61B4</p> <p>C412P1 43B3</p> <p>C756_2 42D3</p> <p>C4237P2 42C4</p> <p>C4240P2 42C4</p> <p>C4242P2 42B4</p> <p>C4243P2 42B4</p> <p>CAP_PLL 41B4</p> <p>CD_CS1FX_L 40C6 60C5</p> <p>CD_CS3FX_L 40C6 60C5</p> <p>CD_DMACK_L 39D4 40C6 60D5</p> <p>CD_DMARQ 40C6 60D5</p> <p>CD_DSTB_RDY 39C4 40C6 60D5</p> <p>CD_EIDE_ADDR<2..0> 40C6 60C5</p> <p>CD_HSTB_RDY 39C4 40C6 60D5</p> <p>CD_RESET_L 39D4 40C6 60D5</p> <p>CD_STOP 39D4 40C6 60D5</p> <p>CHGND 54C4</p> <p>CLK18M_INT_EXT 30B6</p> <p>CLK18M_INT_XIN 30A5</p> <p>CLK18M_INT_XO 30A6</p> <p>CLK18M_INT_XOUT 30A5</p> <p>CLK25M_ENET_XIN 37B6 59B3</p>		<p>CLK25M_ENET_XOUT 37B6 59B3</p> <p>CLK33M_PCI_SLOTB 32D7 33C2 56D7 61A4</p> <p>CLK33M_PCI_SLOTB_UF 32C5 56D7</p> <p>CLK33M_PCI_SLOTC_UF 32C5 56D7</p> <p>CLK33M_PCI_SLOTD 32D7 34A6 56A7</p> <p>CLK33M_PCI_SLOTD_UF 32C5 56D7</p> <p>CLK66M_GPU_AGP 18D8 19C7 56A7</p> <p>CLK66M_GPU_UF 18C6 56A7</p> <p>CLKENET_LINK_GBE_REF 36C6</p> <p>CLKENET_LINK_RX 36C7 37C8 59C3</p> <p>CLKENET_LINK_TX 36D7 37C8 59C3</p> <p>CLKENET_PHY_RX 37C6 59C3</p> <p>CLKENET_PHY_TX 37C6 59C3</p> <p>CLKFW_LINK_LCLK 36C5</p> <p>CLKGEN_OUT_1 10A6 55A6</p> <p>CLK_18M_INT_XOUT 60B5</p> <p>COLE 48C7</p> <p>COMM_DTR_L 30C3 31C7 61C4</p> <p>COMM_GPIO_L 30C3 30D2 31C5 61C4</p> <p>COMM_RESET_L 30C5 31D5 61A7</p> <p>COMM_RING_DET_L 30B5 30B8 31C5 46C5 61D4</p> <p>COMM_RTS_L 30C3 31D5 61C4</p> <p>COMM_RXD 30C3 31C5 61C4</p> <p>COMM_SHUTDOWN 30C5 30D1 31D7 61D4</p> <p>COMM_TRXC 30C3 30D2 31C7 61C4</p> <p>COMM_TXD_L 30C3 31C7 61C4</p> <p>CORE_MOSFET 47C4 47C6</p> <p>CORE_MOSFET_1 47B5 47C7</p> <p>CPU_AACK_L 4A7 7B7 9B6 11B3 58C3</p> <p>CPU_ADDR<31..0> 4B7 4C7 9B7 9B8 9C5 9C6 9C7 9C8 11C3 11D3 58D3</p> <p>CPU_ARTRY_L 4A7 7C7 9B8 11B3 58C3</p> <p>CPU_AVDD 4D3 54C6</p> <p>CPU_BG_L 4D7 7B7 9B5 11D3 58D3</p> <p>CPU_BR_L 4D7 7C7 9C5 11D3 58D3</p> <p>CPU_BUS_VSEL 4D3 7C4</p> <p>CPU_CHKSTP_IN_L 4B3 7B5 61C7</p> <p>CPU_CHKSTP_OUT_L 4B3 7B5 9A2 9D6 61C7</p> <p>CPU_CI_L 4A7 7A7 9C6 11C3 58C3</p> <p>CPU_CLK_EN 11A3 46C4</p> <p>CPU_DATA<63..0> 5A4 5B4 5C4 5D4 9C5 9C6 9C7 9C8 9D5 9D6 9D7 9D8 11B1 11B5 11B8 11C1 11C5 11D1 11D5 11D8 58D3</p> <p>CPU_DBG_L 4C3 7B7 9C8 11B1 58C3</p> <p>CPU_DRDY_L 4C2 7B7 9B6 11B1 58C3</p> <p>CPU_DRDY_L_UF 4C3 58C3</p> <p>CPU_DTI<2..0> 4C3 9B5 9B7 11A1 58C3</p> <p>CPU_EDTI 4C3 7C5</p> <p>CPU_EMODE0_L 4B3 7A4</p> <p>CPU_EMODE1_L 4B3 7A4</p> <p>CPU_FBI_PLUS1 11A4 58C3</p> <p>CPU_FBO_PLUS1 11A4 58C3</p> <p>CPU_FB_MINUS3 11A4 58C3</p> <p>CPU_FB_PLUS2 11A5 58C3</p> <p>CPU_FB_PLUS3 11A4 58B3</p> <p>CPU_GBL_L 4B8 9B6 58C3</p> <p>CPU_HDRST_L 8C7 46C4</p> <p>CPU_HIT_L 4A7 7C7 9B8 11B3 58C3</p> <p>CPU_HRESET_L 4B3 7A3 7A5 7B3 8D2 9A2 46C2 46D2 61C7</p> <p>CPU_INT_GBL_L 4B8 7B7 11C3 58C3</p> <p>CPU_L1TSTCLK 4C3 7A4</p> <p>CPU_L2TSTCLK 4C3 7C4</p> <p>CPU_LSSD_MODE 4C3 7B5</p> <p>CPU_MCP_L 4B3 7B5</p> <p>CPU_PLL_CFG<3..0> 4C3 4D3 6C6 9A8</p> <p>CPU_PLL_CFGEXT 4C3 6C6 9A8</p> <p>CPU_PLL_STOP 6B8 46B8</p> <p>CPU_PMONIN_L 4B3 7C5</p> <p>CPU_PULLDOWN 4A3 4D7 7C5</p> <p>CPU_PULLUP 4A3 7A5</p> <p>CPU_QACK_L 4C3 9B5 11B3 58C3</p> <p>CPU_QREQ_L 4C3 7D5 9B7 11B3 58C3</p> <p>CPU_SHD0_L 4A7 7B5</p> <p>CPU_SHD1_L 4A7 7B5</p> <p>CPU_SLEEPIN 53B7</p> <p>CPU_SMI_L 4B3 7A5 46C4</p> <p>CPU_SRESET_L 4B3 7A5 9A2 61C4</p> <p>CPU_STATE_LED* 46C4 53A8</p> <p>CPU_TA_L 4C3 7C7 9C5 11A1 58C3</p> <p>CPU_TBEN 4C3 7C5 11A3</p>		<p>CPU_TBST_L 4B7 7B7 9B5 11B3 58D3</p> <p>CPU_TEA_L 4C3 7B7 9C6 11A1 58C3</p> <p>CPU_TSIZ<2..0> 4B7 9B6 9B7 9C6 11B3 58D3</p> <p>CPU_TS_L 4D7 7C7 9C7 11D3 58D3</p> <p>CPU_TT<4..0> 4B7 7A7 9B5 9B6 9C5 9C6 11B3 58D3</p> <p>CPU_VCORE_SLEEP 4D3 4D7 9B6 9C2 47B3 47C1 54C6 61B4 61D7</p> <p>CPU_VCORE_SLEEPA 47C3</p> <p>CPU_VCORE_SLEEPA 47C3</p> <p>CPU_VCORE_SLEEPA 47C3</p> <p>CPU_VCORE_SLEEPC 47A1</p> <p>CPU_WT_L 4B7 7A7 9B6 11B3 58C3</p> <p>CSLOT_IOWAIT_L 39B7 54A6</p> <p>CVBS_CNT 24B8 25D6</p> <p>CVBS_D 24B7</p> <p>CY69P2 41B5</p> <p>DAC2RSET 24C6 59D3</p> <p>DAC2VDD 24C5 54B6</p> <p>DAC2VREF 24C5 59D3</p> <p>DACRSET 24C4</p> <p>DACVDD 24C4 54B6</p> <p>DACVREF 24C4</p> <p>DDC_VCC_3 26A5 26B3 54B6 61B7</p> <p>DDC_VCC_5 27C4 54A6 61B7</p> <p>DDRCLK_A0_L_UF 10B3 55B6</p> <p>DDRCLK_A0_UF 10C3 55B6</p> <p>DDRCLK_A1_L_UF 10B3 55B6</p> <p>DDRCLK_A1_UF 10C3 55B6</p> <p>DDRCLK_A2_L_UF 10B3 55B6</p> <p>DDRCLK_A2_UF 10C3 55B6</p> <p>DDRCLK_B0_L_UF 10B3 55A6</p> <p>DDRCLK_B0_UF 10C3 55B6</p> <p>DDRCLK_B1_L_UF 10B3 55A6</p> <p>DDRCLK_B1_UF 10C3 55B6</p> <p>DDRCLK_B2_L_UF 10B3 55A6</p> <p>DDRCLK_B2_UF 10C3 55B6</p> <p>DDR_CK_CE 10B5</p> <p>DDR_CLK_VDD_2 10C5 55B6</p> <p>DDR_FBIN 10B5 55A6</p> <p>DDR_FBIN_L 10B5 55A6</p> <p>DDR_FBO 10B3 55A6</p> <p>DDR_FBO_L 10B3 55A6</p> <p>DDR_VREF 16B2 16D1 16D8 17D8 54A6</p> <p>DS1P1 37B2</p> <p>DS2P1 37B1</p> <p>DS2_1 40B2</p> <p>DS2_2 40B2</p> <p>DS3P1 37B2</p> <p>DS6_1 40B6</p> <p>DS6_2 40B6</p> <p>DUKE_BD 47B5</p> <p>DVOCCLKIN 24C5</p> <p>DVD0 24B5 29B7</p> <p>DVD01 24B5 29B7</p> <p>DVD02 24B5 29C7</p> <p>DVD03 24B5 29C7</p> <p>DVD04 24B5 29C7</p> <p>DVD05 24B5 29C7</p> <p>DVD06 24B5 29C7</p> <p>DVD07 24B5 29C7</p> <p>DVD08 24B5 29C7</p> <p>DVD09 24B5 29C7</p> <p>DVD010 24B5 29C7</p> <p>DVD011 24B5 29C7</p> <p>DVODE 24C5</p> <p>DVOHSYNC 24C5 28D7</p> <p>DVOVREF 24C5</p> <p>DVO_PD 24B5</p> <p>DVO_PU 24B5</p> <p>EEPR_WP 8A6</p> <p>EIDE_ADDR<2..0> 39B7 40A8 40B8 60C5</p> <p>EIDE_CS1FX_L 39A7 40B8 60C5</p> <p>EIDE_CS3FX_L 39A7 40B8 60C5</p> <p>EIDE_CSELP_L 40C6 54A6</p> <p>EIDE_DATA<15..0> 39A5 39B5 39B7 39C5 60D5</p> <p>EIDE_DMACK_L 39A7 39D5 60D5</p> <p>EIDE_DMARQ 39A7 40C8 60D5</p> <p>EIDE_DSTB_RDY 39A7 39C5 60D5</p> <p>EIDE_HSTB_RDY 39A7 39C5 60D5</p> <p>EIDE_INTRQ 39A7 40C8 60C5</p> <p>EIDE_IOCS16_L 40C6 54A6</p> <p>EIDE_PDIAG 40C6</p>		<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. 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	8	7	6	5	4	3	2	1		
			<p>SCALE NONE</p>		<p>SIZE DRAWING NUMBER D 051-6496</p>		<p>REV. A</p>			
	<p>SCALE NONE</p>		<p>SHEET 62 OF 74</p>							

	8	7	6	5	4	3	2	1
D	EIDE_RST_L 39A7 39D5 60D5 EIDE_STOP 39A7 39D5 60D5 ENET_COL 36B7 37B8 59B3 ENET_CRIS 36C7 37B8 59B3 ENET_ENERGY_DET 30B5 30C1 37B4 ENET_LINK_RXD<7..0> 36C6 36C7 37B8 37C8 59B3 ENET_LINK_TXD<3..0> 36C6 59C3 ENET_LINK_TX_EN 36D6 59C3 ENET_LINK_TX_ER 36D6 59C3 ENET_MDC 36B7 37B6 ENET_MDIO 36B7 37B7 ENET_PHY_COL 37B6 59B3 ENET_PHY_CRIS 37B6 59B3 ENET_PHY_RXD<3..0> 37B6 37C6 59B3 ENET_PHY_RX_DV 37B6 59B3 ENET_PHY_RX_ER 37B6 59B3 ENET_PHY_TXD<3..0> 36C7 37C6 59C3 ENET_PHY_TX_EN 36D7 37C6 59C3 ENET_PHY_TX_ER 36D7 37C6 59C3 ENET_RDAC_PD 37B5 ENET_RDN 37C3 59B3 ENET_RDP 37C3 59B3 ENET_RX_DV 36C7 37B8 59B3 ENET_RX_ER 36C7 37B8 59B3 ENET_TDN 37C3 59B3 ENET_TDP 37C3 59B3 ETHPHYRESET_L 37B6 EXTINT14 30A8 30B5 FAN_12V_FILT 31A5 54B3 61C7 FBA<12..0> 20C8 20D8 20E3 20F3 57D3 FBABA<1..0> 20C8 20E3 57D3 FBACAS_L 20C8 20G3 57D3 FBACKE 20D3 20D7 57D3 FBACLK0 20D7 21C3 57C3 FBACLK0_L 20D7 21C3 57C3 FBACLK1 20D7 21D3 57C3 FBACLK1_L 20D7 21D3 57C3 FBACSO_L 20C8 20F3 57D3 FBARAS_L 20C8 20G3 57D3 FBAWE_L 20C8 20F3 57D3 FBBA<12..0> 20A3 20B3 20C3 20C5 20D5 57C3 FBBBA<1..0> 20A3 20C5 57C3 FBBCAS_L 20C3 20D4 57C3 FBBCKE 20A3 20C4 57B3 FBBCLK0 20C5 21B3 57B3 FBBCLK0_L 20C5 21B3 57B3 FBBCLK1 20C5 21C3 57B3 FBBCLK1_L 20C5 21B3 57B3 FBBCS0_L 20C3 20C4 57C3 FBBRAS_L 20C3 20D4 57C3 FBBWE_L 20C3 20D4 57C3 FBCAL_CLK_GND 20A5 20D7 FBCAL_PD_VDDQ 20D7 FBCAL_PU_GND 20A5 20D7 FBCAL_TERM_GND 20A5 20D7 FBD<127..0> 20E5 20E8 20F5 20F8 20G5 20G8 21B5 21B8 21C5 21C8 21D5 21D8 57C3 57D3 FBDQM<15..0> 20C3 20D3 20D5 20D8 20G3 57C3 57D3 FBDQS<15..0> 20C7 20D4 21A5 21A8 57B3 57C3 FBDQSTERM<15..0> 21A4 21A7 57B3 57C3 FB_DLLVDD 20C6 20D7 FDC602 48B7 FDX 37A5 37C4 FILT_ANALOG_BLU 27C5 59D3 61B7 FILT_ANALOG_GRN 27C5 59D3 61B7 FILT_ANALOG_RED 27C5 59D3 61B7 FIX_RESET_L 8B6 8C4 FLOW_SS 47C7 47D8 FLO_KNOWS_BEST 47C6 47C7 47C8 61D4 FPD_PWR_ON 25D6 53B3 FPD_PWR_ON_T 53B3 FWPHYRST 30C5 38C8 FW_BIAS1 38C5 59A3 FW_BIAS2 38C5 59A3 FW_CNTRL0 36C3 38C8 59A3 FW_CNTRL1 36C3 38C8 59A3 FW_CPS 38C6 FW_C_LKON 30B6 36C5 38B5 FW_D<7..0> 36C3 38B8 38C8 59A3 FW_DIODE_BYPASS_V 38B6 38B7 54B6 FW_DIO_V 38B6 54B6	FW_LINK_CNTRL<1..0> 36C5 59A3 FW_LINK_DATA<7..0> 36C5 59A3 FW_LINK_LREQ 36C5 59A3 FW_LPS 36C5 38C8 FW_LREQ 36C3 38C8 59A3 FW_PHY_3_3 38B5 38B7 38D7 54B6 FW_PHY_CNTRL0 38C7 59A3 FW_PHY_CNTRL1 38C7 59A3 FW_PHY_D<7..0> 38B7 38C7 59A3 FW_PHY_ISO* 38C6 FW_PHY_RST 38C8 FW_PHY_RST* 38C6 FW_PHY_SCLK 38C7 59A3 FW_PINT 36B5 36C1 FW_PWR 52C7 53D3 54B6 FW_PWR_SW 38D6 53D1 54B6 FW_R0 38C5 FW_R1 38C5 FW_SCLK 36C5 38C8 59A3 FW_TPA1N 38C5 59A3 FW_TPA1P 38C5 59A3 FW_TPA2N 38C5 59A3 FW_TPA2P 38C5 59A3 FW_TPB1 38B3 FW_TPB1N 38C5 59A3 FW_TPB1P 38C5 59A3 FW_TPB2 38B4 FW_TPB2N 38C5 59A3 FW_TPB2P 38C5 59A3 FW_TPI1N 38A8 38D1 59A3 FW_TPI1P 38A8 38D1 59A3 FW_TPI2N 38A8 38C1 59A3 FW_TPI2P 38A8 38C1 59A3 FW_TPOLN 38A8 38D1 59A3 FW_TPOLP 38B8 38D1 59A3 FW_TPO2N 38A8 38C1 59A3 FW_TPO2P 38A8 38C1 59A3 FW_VGND 38D1 54B6 FW_VP 38D5 54B6 FW_VP1 38D1 38D3 54B6 FW_VP2 38C1 38D3 54B6 FW_VP_1 38D4 54B6 FW_VP_2 38D4 54B6 FW_VREG_FB 38D7 FW_XI 38C6 59A3 FW_XI_A 38C6 FW_XO 38C6 59A3 GCORE_1 50C2 GCORE_2 50C3 GCORE_BSTH 50C5 GCORE_BSTH_TERM 50C3 GCORE_COMP 50B6 GCORE_DH 50B5 GCORE_DL 50B5 GCORE_GND 50B5 GCORE_OCSET 50B6 GCORE_OVP 50B6 GCORE_VCC 50C6 GCORE_VSENSE 50B6 50C2 GPULLNKN 25C4 GPU_50PULLDWN 19A5 54A6 GPU_50PULLUP 19A5 54A6 GPU_AGP_AD<31..0> 19C7 19D7 56B7 GPU_AGP_CBE<3..0> 19C7 56B7 GPU_AGP_DEVSEL_L 19B7 56B7 GPU_AGP_FRAME_L 19B7 56B7 GPU_AGP_IRDY_L 19B7 56B7 GPU_AGP_PAR 19B7 56B7 GPU_AGP_PIPE_L 19B7 56A7 GPU_AGP_RBF_L 19B7 56A7 GPU_AGP_SBA<7..0> 19A7 56A7 GPU_AGP_SB_STB 19A7 56A7 GPU_AGP_SB_STB_L 19A7 56A7 GPU_AGP_STOP_L 19B7 56B7 GPU_AGP_TRDY_L 19B7 56B7 GPU_AGP_VREF 19A3 19A8 54A6 GPU_AGP_VREF_H 18A8 GPU_AGP_VREF_L 18A8 GPU_AGP_VREF_X 19A3 GPU_AGP_VREF_Y 19A3 GPU_AGP_WBF_L 19B7	GPU_FB_VREF 20C8 54A6 GPU_FPBCLK 25C4 GPU_FPBCLK_L 25C4 GPU_FW_PME_L 25C4 GPU_IFB1IOVDD 25B2 GPU_IFP1PLLVD 25B2 GPU_MBDL 19A7 GPU_STEREO 25C4 GPU_STRAP<3..0> 24B4 28A3 28B3 28D3 GPU_SWAP_A 25C4 GPU_SWAP_B 25C4 GPU_TESTMECLK 25C4 GPU_TMODE 19A5 54A6 GPU_XTALSSIN 24B4 54A6 GPWRGD 49B6 49B8 50A5 GRAPHICS_VPWR 50B5 GRAPH_CORE 19D5 25C4 25C6 50B1 54A6 GRAPH_DDC_SCL 24D5 26A6 GRAPH_DDC_SDA 24D5 26A6 GRAPH_IIC_SCL2 25D2 GRAPH_IIC_SDA2 25D2 HD_DIOR_L 39D1 40C3 60C5 HD_DIOW_L 39C1 40C3 60C5 HD_DMACK_L 39D1 40C3 60C5 HD_DMARQ 40C3 60C5 HD_INTRQ 40C3 60C5 HD_IOCHRQ 39C1 40C3 60C5 HD_RESET_L 39D1 40C3 60C5 HD_UIDE_ADDR<2..0> 40C2 40C3 60C5 HD_UIDE_CS1FX_L 40C3 60B5 HD_UIDE_CS3FX_L 40C2 60B5 HEADPHONE_COM 43B2 HEADPHONE_L 43B2 43D2 HEADPHONE_R 43B2 43C2 HONK_ADJ 53B4 HP16_L 43D4 HP16_R 43C4 HPBVP 43B5 43D6 HPGAL_L 43D4 HPGAL_R 43C4 HPIN_L 43D6 HPIN_R 43D6 HP_OFF 43A7 43D5 HP_OUT_L 43D5 HP_OUT_R 43D5 HP_STAR_GND 41B7 43A8 43B4 43B8 43C5 43D4 43D7 HP_TL 43D3 HP_TP 43B3 HP_TR 43C3 HRST_REF 8B4 8B7 HSYNC* 24C5 59D3 ICORE_COMP 49B6 ICW 49B7 IFPOAVCC 25A6 25B4 54A6 IFP0PLLVD 25B4 IFPORSET 25B4 IFPOVREF 25B4 54A6 IFP_AVCC 25A7 IFP_VADJ 25A8 IIC A<2..0> 8A6 8A7 IIC_ADD 31C6 61A7 IMAC_INTREPID 49B4 INTCORE_1 49B3 INTCORE_BSTH 49B6 INTCORE_BSTH_TERM 49B6 INTCORE_DH 49B6 INTCORE_DHT 49B5 INTCORE_DL 49B6 INTCORE_GND 49A7 INTCORE_NET99 49B4 INTCORE_OCSET 49B6 INTCORE_OVP 49B6 INTCORE_VCC 49C7 INTREPID_ACS_REF 11A3 INTREPID_VPWR 49B6 INTREPID_VPWR_A 49B4 INTREPID_VSENSE 49C6 61C7 INTREP_DLT 49B5 INT_AGPPVT 18C6 INT_AGP_FB_IN 18C6 56A7 INT_AGP_FB_OUT 18C6 56A7	INT_AGP_VREF 18A7 18C6 54C3 INT_ANALYZER_CLK 9B4 11B4 18C7 56A7 58B3 61A7 INT_ANALYZER_CLKA 11B3 INT_CLOCK_OUT 9C4 58B3 INT_CPU_FB_IN 11B3 58C3 INT_CPU_FB_OUT 11B3 58C3 INT_ENET_RST_L 30B5 30D1 37B8 INT_EXTINT3_PU 30B5 30B8 INT_EXTINT12_PU 30B5 30B8 INT_EXTINT13_PU 30B5 30B8 INT_EXTINT17_PU 30B5 30B8 34B6 INT_GPI01_PD 30A8 30C5 INT_GPI09_PU 30B5 30B8 INT_GPI012_PU 30A8 30B5 INT_I2C_CLK0 8A6 8B4 8B7 10C7 16A6 17A6 36B3 INT_I2C_CLK0R 36B5 36C1 INT_I2C_CLK1 10A7 36A3 36A4 36B1 INT_I2C_CLK2 30A3 30D1 31C7 36B5 41B1 61A7 INT_I2C_DATA0 8A6 8B4 8B7 10C7 16A6 17A6 36B3 INT_I2C_DATA0R 36B5 36C1 INT_I2C_DATA1 10A7 36A3 36B1 INT_I2C_DATA2 30A3 30D1 31C7 36B5 41B1 61A7 INT_JTAG_TEI 36B7 36C1 INT_MEM_REF 14B6 INT_MOD_BITCLK 30A3 30A8 30C6 INT_MOD_CLKOUT 30A3 30A8 30C6 INT_MOD_DTI 30A3 30A8 30C6 INT_MOD_DTO 30A3 30A8 30C6 INT_MOD_SYNC 30A3 30A8 30C6 INT_PCI_FB_IN 32C5 56C7 INT_PCI_FB_OUT 32C5 56D7 INT_PEND_PROC_INT 30A5 46B4 INT_PLL1_GND 30A5 30C4 INT_PLL2_GND 30A5 30D4 INT_PLL3_GND 30A4 30D4 INT_PLL4_GND 32B4 32D4 INT_PLL5_GND 18A5 18D5 INT_PLL6_GND 11A2 11D3 INT_PLL7_GND 30A4 30D4 INT_PLL9_GND 30A4 30D4 INT_PROC_SLEEP_REQ_L 30A5 46B4 INT_PU_RESET_L 36C3 46C2 46C4 INT_REF_CLK_IN_PD 10A5 30A6 55A6 INT_REF_CLK_OUT 10A7 30A6 55A6 INT_REF_CLK_OUT_UF 55A6 INT_RESET_L 36C3 37B8 43A7 44A8 46D2 46D4 INT_ROM_CS_L 32C5 INT_ROM_OE_L 32C5 INT_ROM_OVERLAY_PU 18D7 32A8 32C5 56A7 INT_ROM_RW_L 32C5 INT_SND_CLKOUT 30A3 INT_SND_SCLK 30A3 INT_SND_SYNC 30B3 INT_SND_TO_AUDIO 30B3 INT_SPKR+ 44B1 INT_SPKR- 44B1 INT_SUSPEND_ACK_L 11B3 46B5 INT_SUSPEND_REQ_L 11B3 46B5 46B8 INT_TMDS_3V 26B3 26C3 26C4 26D5 54A6 61C7 INT_TMDS_CKM 25D2 26A6 59D3 61A7 INT_TMDS_CKP 25D2 26B6 59D3 61A7 INT_TMDS_DOM 25D2 26B6 59C3 61A7 INT_TMDS_D0P 25D2 26B6 59C3 61B7 INT_TMDS_DIM 25D2 26C6 59C3 61B7 INT_TMDS_D1P 25D2 26C6 59C3 61B7 INT_TMDS_D2M 25C2 26D6 59C3 61B7 INT_TMDS_D2P 25C2 26D6 59C3 61B7 INT_TST_MONIN_PD 36B7 36C1 INT_TST_PLEN_PD 30C6 36B7 36C1 INT_WATCHDOG_L 30A5 46C5 INV_BFR_HRST 8D6 INV_CUR_HI 25D6 31B8 INV_CUR_HI_FILT 31A5 61A7 IO_RESET_L 34A6 37B8 46B5 46B8 46D3 61A7 IPWRGD 48A8 49A6 IPWR_D 48A7 JAZ 45C6 JTAG_ASIC_TCK 9A3 36B7 37C4 61D7 JTAG_ASIC_TDI 9A3 30C6 36B7 61D7 JTAG_ASIC_TDO 9A3 37B4 61D7 JTAG_ASIC_TMS 9A3 36B7 37A2 37B4 61D7	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. 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SCALE	DRAWING NUMBER	REV.
NONE	D 051-6496	A
SHEET	63	OF 74

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D	JTAG_ASIC_TRST_L 9A3 36B7 61C7 JTAG_CPU_TCK 4C3 7D5 8C2 9A2 61C7 JTAG_CPU_TDI 4C3 7A5 8D2 9A2 61C7 JTAG_CPU_TDO 4C3 9A2 61C7 JTAG_CPU_TMS 4C3 7A5 8D2 9A2 61C7 JTAG_CPU_TRST_L 4C3 7C5 8D2 9A2 61C7 JTAG_ENET_TDI 30C6 36B7 37A2 37B4 KAVAN 45B6 KSSVSD 31A5 54B3 61A7 KS_INT_SPKR+ 31A3 44C3 60A5 61B7 KS_INT_SPKR+_FILT 31A5 KS_INT_SPKR- 31A3 44C3 60A5 61B7 KS_INT_SPKR-_FILT 31A5 KYLE 48C6 L31_2 42C6 L32_2 42B6 L36_2 42B6 L43_1 43A4 L3202_1 42C6 LAMP_STS 25D6 31A3 LAMP_STS_FILT 31A5 61A7 LCD_PWM 25D6 31A8 LCD_PWM_FILT 31A5 61A7 LED_5V 31A8 54B3 LED_5V_FILT 31A5 54B3 61A7 LED_RET 31A3 53B6 54B3 LED_RET_FILT 31A5 54A3 61A7 LED_ROMCS 32A3 LED_ROMCS_L 32A4 LED_ROMCS_LIGHT 32A3 LID_SWITCH 31B2 46C4 LINA 41C4 42C2 LINEOUT_COMM2 61B4 LINE_IN_COM 42B7 61B4 LINE_IN_L 42B7 42C7 61B4 LINE_IN_R 42B6 42B7 61B4 LINE_IN_SENSE 42B7 42C7 61B4 LINE_OUT_L 61B4 LINSENSE 42C5 LOW_PWR 37A5 37B4 LO_T1 43A4 LP4202P2 42C5 LP4202P3 42B5 LP4202P4 42B5 LPL1 43D6 LPR1 43C6 LSPKRCAP 44B8 LSPKRIN2 44B6 LSPKRVP2 44B6 LT1962_INT_ADJ 30D7 LT1962_INT_BYP 30D7 LT1962_INT_VIN 30D7 LY4P2 44C3 M1FH 45C7 M1FL 45B7 M1H 45C6 M1HFILT 45C5 M1L 45B6 45C6 M1S 45B5 45C6 MAIN_RESET_L 32A2 33D4 34A6 46C4 61A4 MAIN_RESET_L_PU 33D3 MAIN_SUPPLY_LED 52D6 MEMI_VREF 14A6 MEMREFG1 22A5 MEMREFG2 22A4 MEMREFG3 23A5 MEMREFG4 23A4 MEMREFI1 14A8 MEMREFI2 14A7 MEMREFM1 16B3 MEMREFM2 16B2 MEMREFN1 20B8 MEMREFN2 20B7 MEM_ADDR<12..0> 14A3 14B3 14C2 14C3 14D2 14D3 14D6 55D6 MEM_BA<1..0> 14B3 14D6 55D6 MEM_CAS_L 14A3 14C6 55C6 MEM_CKE<3..0> 14A2 14B2 14B6 14C2 14C6 55C6 MEM_CS_L<3..0> 14A2 14B2 14C2 14C6 55D6 MEM_DATA<63..0> 14B8 14C8 14D8 15A6 15B3 15B6 15C5 15C8 55D6	MEM_DQM<7..0> 14C6 15A6 15B3 15C5 15C8 55D6 MEM_DQS<7..0> 14C6 15A6 15B3 15C5 15C8 55D6 MEM_MUXSEL_H<1..0> 14B6 14D5 55C6 MEM_MUXSEL_L<1..0> 14B6 14D5 55C6 MEM_RAS_L 14A3 14C6 55C6 MEM_WE_L 14A3 14C6 55C6 MIC1 45C4 MIC1S1 45B7 MIC2 45C4 MIC3 45C4 MIC4 45C3 MIC5 45B3 MICHIGH 31A5 45C8 60A5 61A7 MICLOW 31A5 45B8 60A5 61A7 MICSHLD 31A5 45B8 60A5 61A7 MIC_FIX 45D5 MIC_IN 41C4 45C2 MIC_TDO 8B3 MII_EN 37C4 MODEM_USB_DM 30B2 31C5 60A5 61B4 MODEM_USB_DP 30B2 31C5 60A5 61B4 MON_DETECT 25D6 27C6 61D4 MON_I2C_SCL 24D5 27B6 MON_I2C_SDA 24D5 27B6 MPIC_CPU_INT_L 4B3 7A5 9D7 30B5 MPWRGD 50B6 50B7 51B5 MR_FLO 47C5 MR_FLO_1 47B4 MUTE_B_L 44B8 MUX_SEL_H 14D4 15A3 15C5 55C6 MUX_SEL_L 14D4 15A6 15C8 55C6 M_SPD_WP 17A7 M_VDDID 17A7 NCV4 41D6 NC_-10VUNREG 31C6 NC_-12VREG 31C6 NC_28512P4 10A7 NC_28512P14 10A7 NC_28512P17 10A7 NC_AMPOL 44B6 NC_ATXTAL1 8C4 NC_ATXTAL2 8B4 NC_AUDIO2MODEM 31C6 NC_AUDIO2MODEMRTN 31C6 NC_AUD_MODEM 31C6 NC_AUD_MODEM_RTN 31C6 NC_BIGDIMM9 17D6 NC_BIGDIMM10 17D6 NC_BIGDIMM44 17C6 NC_BIGDIMM45 17B6 NC_BIGDIMM47 17B6 NC_BIGDIMM49 17B6 NC_BIGDIMM51 17B6 NC_BIGDIMM71 17A6 NC_BIGDIMM101 17D4 NC_BIGDIMM102 17D4 NC_BIGDIMM103 17D4 NC_BIGDIMM113 17C4 NC_BIGDIMM134 17C4 NC_BIGDIMM135 17C4 NC_BIGDIMM140 17B4 NC_BIGDIMM142 17B4 NC_BIGDIMM144 17B4 NC_BIGDIMM163 17A4 NC_BIGDIMM167 17A4 NC_BIGDIMM173 17A4 NC_BS1 31B7 NC_BS2 31B6 NC_BS3 31D1 NC_BS4 31D1 NC_BT1 31D2 NC_BT3 31D2 NC_BT4 31D2 NC_BT5 31D2 NC_BT6 31D2 NC_CBUS_INT_L 30A8 NC_CLK33M_PCI_SLOT 32D7 NC_CLKENET_LINK_GTX 36C6 NC_CPUAP<4..0> 4B7 NC_CPUCRUD<89..0> 5A7 5B7 5C7 5D7 NC_CPUUD<7..0> 5A4	NC_CPU_CLKOUT 4D3 NC_CSLOT_ADDR<9..3> 39A7 39B7 NC_CSLOT_CE1_L 39C7 NC_CSLOT_CE2_L 39C7 NC_CSLOT_IORD_L 39C7 NC_CSLOT_TOWR_L 39C7 NC_CSLOT_OE_L 39B7 NC_CSLOT_WE_L 39B7 NC_DAA_CLKOUT 31C6 NC_DAA_LOADOUT 31C6 NC_DACC_BLU 24C4 NC_DACC_GRN 24C4 NC_DACC_RED 24C4 NC_DACC_RSET 24C4 NC_DDRCLK1 10C3 NC_DDRCLK2 10C3 NC_DDRCLK3 10C3 NC_DDRCLK4 10C3 NC_DDRCLK5 10C3 NC_DDRCLK6 10C3 NC_DDRCLK7 10C3 NC_DDRCLK8 10C3 NC_DDRCLK9 10C3 NC_DDRCLK10 10C3 NC_DDRCLK11 10B3 NC_DDRCLK12 10B3 NC_DDRCLK13 10B3 NC_DDRCLK14 10B3 NC_DDRCLK_A2 10C2 NC_DDRCLK_A2_L 10C2 NC_DFPCLK 25C2 NC_DFPCLK* 25C2 NC_DFPD0 25C2 NC_DFPD1 25C2 NC_DFPD2 25C2 NC_DFPD3 25C2 NC_DFPD5 25B2 NC_DFPD6 25B2 NC_ENET_LINK_TXD<7..4> 36C6 NC_EXT_TMDS_CKM 25C2 NC_EXT_TMDS_CKP 25C2 NC_EXT_TMDS_DOM 25C2 NC_EXT_TMDS_D0P 25C2 NC_EXT_TMDS_D1M 25C2 NC_EXT_TMDS_D1P 25C2 NC_EXT_TMDS_D2M 25C2 NC_EXT_TMDS_D2P 25C2 NC_FB1<10..0> 22B5 22B6 NC_FB2<10..0> 22B1 22B2 NC_FB3<10..0> 23B5 23B6 NC_FB4<10..0> 23B1 23B2 NC_FBACS1_L 20C8 NC_FBBCS1_L 20C4 NC_FBDQS_L<15..0> 20C7 20D4 NC_FMAX7 9A8 NC_FMAX8 9A8 NC_FW_CNA 38B6 NC_GPU<4..0> 19A6 NC_GPULFS 25C4 NC_GPU_DBI_LO 19B7 NC_GPU_INTB_L 19B7 NC_GPU_THERMA 25C4 NC_GPU_THERMC 25C4 NC_IFP1RSET 25B2 NC_IFP1VREF 25B2 NC_INPA 41C2 NC_INT_TST_MONOUT_TP 36B6 NC_JTAG7 9A3 NC_JTAG10 9A2 NC_LCENABLE 9A3 NC_MODEM_DETECT_L 31C6 NC_NVAGP_TDI 19A5 NC_NVAGP_TDO 19A5 NC_NVAGP_TMS 19A5 NC_P00_D0 46D5 NC_P01_D1 46D5 NC_P02_D2 46C5 NC_P03_D3 46C5 NC_P04_D4 46C5 NC_P05_D5 46C5 NC_P6_D6 46C5	NC_P07_D7 46C5 NC_P10_D8 46C5 NC_P11_D9 46C5 NC_P14_D12 46C5 NC_P20_A0_D0 46C5 NC_P21_A1_D1_D0 46C5 NC_P22_A2_D2_D1 46C5 NC_P23_A3_D3_D2 46C5 NC_P24_A4_D4_D3 46C5 NC_P25_A5_D5_D4 46C5 NC_P26_A6_D6_D5 46C5 NC_P27_A7_D7_D6 46C5 NC_P33_A11 46B5 NC_P34_A12 46B5 NC_P35_A13 46B5 NC_P36_A14 46B5 NC_P37_A15 46B5 NC_P43_A19 46B5 NC_P45_CS1_L 46B5 NC_P74_TA2OUT_W 46C4 NC_P75_TA2IN_W 46C4 NC_P76_TA3OUT 46C4 NC_P77_TA3IN 46C4 NC_P92_TB2IN_SOUT3 46B4 NC_P93_DA0_TB3IN 46B4 NC_P96_ANEX0_CLK4 46B4 NC_P103_AN3 46B4 NC_PCIR0 33B7 NC_PCIR1 33B7 NC_PCITR0 33B6 NC_PCITR1 33B6 NC_PD0 8B3 NC_PMON_OUT_L 4B3 NC_PMU_DL_10 31B2 NC_PMU_DL_12 31B2 NC_PPL* 46C6 NC_RESET_BUTTON_L 9A8 NC_RFBA<12..12> 20E2 NC_RFBBA<12..12> 20A2 NC_RF_DISABLE_L 61A4 NC_ROMCS_L 20C8 NC_RP1PIN4 18B3 NC_RP1399 32A6 NC_RP2848 30A8 NC_RP3319 30D2 NC_RP3324_2 30C1 NC_RPT48P1 30D2 NC_RPT77P6 30B8 NC_SDOUT2 41C2 NC_SODIMM71 16C6 NC_SODIMM72 16C5 NC_SODIMM73 16C6 NC_SODIMM74 16C5 NC_SODIMM77 16C6 NC_SODIMM78 16C5 NC_SODIMM79 16C6 NC_SODIMM80 16C5 NC_SODIMM83 16C6 NC_SODIMM84 16C5 NC_SODIMM85 16C6 NC_SODIMM86 16C5 NC_SODIMM89 16C6 NC_SODIMM91 16C6 NC_SODIMM97 16B6 NC_SODIMM98 16B5 NC_SODIMM123 16B6 NC_SODIMM124 16B5 NC_SODIMM199 16A6 NC_SODIMM200 16A5 NC_SODIMM201 16D5 NC_SODIMM202 16A6 NC_SW3V5V_33OUT 52C6 NC_SYSCLK_DDRCLK_A2 14B4 NC_TAS_SDOUT1 41C2 NC_TESTMODE 9A3 NC_TMDS_TXD3M 25C2 NC_TMDS_TXD3P 25C2 NC_TMDS_TXD7M 25C2 NC_TMDS_TXD7P 25C2 NC_TX1_1 37C3 NC_TX1_2 37C3					
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	D	051-6496	A
SCALE	SHEET		OF
NONE	64		74



ZT11P1 4B1

SW3V_TG2 52B6
 SW3V_TG2R 52C5
 SW3V_VOSNS 52B6
 SW5VITH1R 52B8
 SW5V_SVSENSE 52A4
 SW5V_BG1 52A5 52B7
 SW5V_BG1R 52A5
 SW5V_BOOST1 52A5 52B7
 SW5V_ITH1 52B7
 SW5V_RUNSS 52B8 52D3
 SW5V_SNSM 52A5 52B7
 SW5V_SNSMA 52A4
 SW5V_SNSP 52A5 52B7
 SW5V_SW1 52A4 52A5 52B7
 SW5V_SW1A 52A3
 SW5V_TG1 52B5 52B7
 SW5V_TG1R 52B4
 SW5V_VOSNS 52B7
 SW12V_SL 53C7
 SW12V_SLEEP 53D7
 SWITCH5V_3 53B6
 SWITCH5V_4 53B6
 SWITCH5V_5 53B1 53B3
 SWITCH5V_6 53B2
 SYSCLK_CPU 4D2 11A4 58C3
 SYSCLK_CPU_UF 11A3 58C3
 SYSCLK_DDRCLK_A0 10C2 14C4 16D6 55C6
 SYSCLK_DDRCLK_A0_L 10C2 14C4 16D6 55C6
 SYSCLK_DDRCLK_A0_L_UF 14B6 14C5 55C6
 SYSCLK_DDRCLK_A0_UF 14B6 14C5 55C6
 SYSCLK_DDRCLK_A1 10C2 14C4 16A4 55C6
 SYSCLK_DDRCLK_A1_L 10C2 14B4 16A4 55C6
 SYSCLK_DDRCLK_A1_L_UF 14B5 14B6 55C6
 SYSCLK_DDRCLK_A1_UF 14B6 14C5 55C6
 SYSCLK_DDRCLK_A2_L 10C5 14B4 55B6
 SYSCLK_DDRCLK_A2_L_UF 14B5 14B6 55C6
 SYSCLK_DDRCLK_A2_UF 14B5 14B6 55C6
 SYSCLK_DDRCLK_B0 10C2 14B4 17B4 55B6
 SYSCLK_DDRCLK_B0_L 10C2 14B4 17B4 55B6
 SYSCLK_DDRCLK_B0_L_UF 14B5 14B6 55B6
 SYSCLK_DDRCLK_B0_UF 14B5 14B6 55B6
 SYSCLK_DDRCLK_B1 10C2 14A4 17D6 55B6
 SYSCLK_DDRCLK_B1_L 10C2 14A4 17D6 55B6
 SYSCLK_DDRCLK_B1_L_UF 14A5 14B6 55B6
 SYSCLK_DDRCLK_B1_UF 14A5 14B6 55B6
 SYSCLK_DDRCLK_B2 10B2 14A4 17A6 55B6
 SYSCLK_DDRCLK_B2_L 10B2 14A4 17A6 55B6
 SYSCLK_DDRCLK_B2_L_UF 14A5 14B6 55B6
 SYSCLK_DDRCLK_B2_UF 14A5 14B6 55B6
 SYSCLK_LA 9B3 9D8 58B3
 SYSTEM_CLK_EN 10A7 30A5 46C4
 TAS_DVDD 41D3
 TAS_PWR_DOWN 41B4 41D7
 TAS_STAR_GND 41A7 41D2
 TAS_VCOM 41B1 41B3 44B8
 TCKM 26A5 26C3 59C3
 TCKP 26B5 26C4 59C3
 TD0M 26B5 26C4 59C3
 TD0P 26B5 26C3 59C3
 TD1M 26C3 26C5 59C3
 TD1P 26C4 26C5 59C3
 TD2M 26C4 26D5 59C3
 TD2P 26C3 26D5 59C3
 TESTEN 37A5 37C4
 TMDS_DDC_CLK 26A5 26B3 61C4
 TMDS_DDC_DAT 26A5 26B4 61C4
 TMDS_EN 25C6 53B1
 TPA_PGND 44B6 44C8 53C5
 TPA_SLP_H 44A7 53D4
 TPA_STAR_GND 41B7 44A7
 TPA_VA 44C8 44D7 53D5
 TPA_VL 44C8 44D6
 TPA_VR 44C8 44D6
 TP_BUF_RST 24B5
 TP_DVOCLKOUT 24C5
 TP_DVOCLKOUT* 24C5
 TP_DVOVSYNC 24B5
 TRANS_ADJ 47B3
 TRST_IN 8B3
 T_UD_IDEDD_0 39C1 40C3 60C2
 T_UD_IDEDD_1 39C1 40C3 60C2

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 T_UD_IDEDD_11 39B1 40C2 60B2
 T_UD_IDEDD_12 39B1 40C2 60B2
 T_UD_IDEDD_13 39A1 40C2 60B2
 T_UD_IDEDD_14 39A1 40C2 60B2
 T_UD_IDEDD_15 39A1 40C2 60B2
 U5_SDOUT 41C3
 U22_8 38D8
 U4202P2 42C3
 U4202P3 42C3
 U4202P5 42B3
 U4202P6 42B3
 U4202P7 42B3
 UATA0IRQ 40C6 60D5
 UATAD<15..0> 39A4 39B4 39C4 40C6 60D5
 UB5PAE8 24B5
 UIDE_ADDR<2..0> 39C7 40A4 40B4 60B5
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 UIDE_CS3FX_L 39C7 40B4 60B5
 UIDE_CSELP_L 40C2 54A6
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 UIDE_DIOW_L 39C3 39C7 60C5
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 UIDE_DMARQ 39C7 40C4 60C5
 UIDE_INTRQ 39C7 40C4 60C5
 UIDE_IOCHRDY 39C3 39C7 60C5
 UIDE_PDIAG 40C2
 UIDE_REF 39C7
 UIDE_RST_L 39C7 39D3 60C5
 UNUSED_ATAIOCS16_L 40C2 54A6
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 UNUSED_EXTINT8 30B5 30B8
 UNUSED_GPIO15 30B5 30C1 61A4
 USB2_CRUN_L 30B5 34A7
 USB2_DAN_F 34C1 34C4 35B7 58B3
 USB2_DAP_F 34C1 35B7 58B3
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 USB2_RSADAP 34C4 58B3
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 USB2_RSDBP 34C4 58B3
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 USB2_RSDCP 34C4 58B3
 USB2_XT1 34C4 58B3
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 USBT_DCP_F 35D6 58A3
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 USB_DCN_CON 35D3 58A3 61C4
 USB_DCN_F 30B2 35D7 60B5
 USB_DCP 30B3 60B5
 USB_DCP_CON 35D3 58A3 61C4
 USB_DCP_F 30B2 35D7 60B5
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 USB_DFN 30B3 60A5
 USB_DFP 30B3 60A5
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 USB_OC_EF_L 30B3 30C2
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 USB_PWR 27B5 27C2 27D3 35A6 54A3
 USB_PWREN_AB_L 30B3 30C2
 USB_PWREN_CD_L 30B3 30C2
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 USB_PWR_FLT* 30B3 34B1 35A6
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 VCOREIN 47D6
 VCORE_BG 47C6
 VCORE_BG_1 47B5 47C7
 VCORE_BOOST 47C5
 VCORE_BOOST2 47C6
 VCORE_BOOST2_1 47B5 47C7
 VCORE_BOOST_1 47B5
 VCORE_EXTVCC 47D7
 VCORE_FREQSET 47C7
 VCORE_INTVCC 47B5 47D5 47D7
 VCORE_SEN+ 47C3
 VCORE_SEN+_1 47A3
 VCORE_SENA+ 47C3
 VCORE_SF 47C8
 VCORE_SGND 47B7 47C7 47C8
 VCORE_STBY 47C7
 VCORE_TG 47C6
 VCORE_TG_1 47B5 47C7
 VCORE_VGATE 10A8 30B5
 VCORE_VIN 47D7
 VC_CNTL1 46C7 47D8
 VC_SENA 47B3
 VGA_IIC_CLK 27C4 61B4
 VGA_IIC_DAT 27C4 61B4
 VGER_INV_HRESET 7A3 7B3 7C3 46D1
 VIPCLK 24D4 54A6
 VIPD0 24D4 28B7
 VIPD1 24D4 28B7
 VIPD2 24D4 28B8
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 VIPD4 24D4 28D7
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 VIPD6 24D4 28B8
 VIPD7 24D4 28C5
 VIPHAD0 24D5 28B7
 VIPHAD1 24D5 28B7
 VIPHCTL 24D5 28D5
 VIP_PD 24C4
 VIP_PU 24C4
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 VOSNS2 52B5
 VR43P2 48C5
 VR4210P1 41B7
 VREFM 41B4
 VREFP 41B4 45B2
 VRFILT 41B3
 VSYNC* 24C5 59D3
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 XMIT_LED 37A2 37B4
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 XW4001P2 44A7
 XW4002P2 44A7 44D7
 ZT8P1 4A1
 ZT9P1 4B2
 ZT10P1 4A2

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	NONE	D 051-6496	A
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	<p>*** Unit Cross-Reference *** --- for the entire design --</p>							
D	BS1 PCB_STANDOFF 31B5 BS2 PCB_STANDOFF 31B6 BS3 PCB_STANDOFF 31D1 BS4 PCB_STANDOFF 31D1 BT1 BATTERY 46D6 C1 CAP 35C3 C2 CAP 35D3 C3 CAP 37B1 C4 CAP 38B6 C5 CAP_P 35A5 C6 CAP 35B3 C7 CAP_P 35A5 C8 CAP 23A4 C9 CAP 23A4 C10 CAP_P 38D7 C11 CAP 23A5 C12 CAP_P 38D7 C13 CAP_P 43C4 C14 CAP_P 44C7 C15 CAP 23D2 C16 CAP 23B4 C17 CAP 23D5 C18 CAP 53D2 C19 CAP_P 53D3 C20 CAP 23B2 C21 CAP 23D5 C22 CAP 23B4 C23 CAP 23B4 C24 CAP_P 42B4 C25 CAP_P 42C4 C26 CAP_P 43D4 C27 CAP 38D8 C28 CAP 23B1 C29 CAP 23B3 C30 CAP 44B4 C31 CAP 23B2 C32 CAP 23D4 C33 CAP 23B2 C34 CAP 23B3 C35 CAP 45C4 C36 CAP 37D2 C37 CAP 37D7 C38 CAP 23D2 C39 CAP 23D5 C40 CAP 23B3 C41 CAP 37D7 C42 CAP 38B8 C43 CAP 43D6 C44 CAP 37D3 C45 CAP 37D2 C46 CAP 37D4 C47 CAP_P 44D7 C48 CAP 44D7 C49 CAP 44C7 C50 CAP_P 44D7 C51 CAP 37B3 C52 CAP 37D2 C53 CAP 37D4 C54 CAP 20B8 C55 CAP 37D3 C56 CAP 37D3 C57 CAP 37D5 C58 CAP 37D5 C59 CAP_P 50B2 C60 CAP 43C6 C61 CAP 20B6 C62 CAP 20D6 C63 CAP 42B2 C64 CAP 42C2 C65 CAP 37D6 C66 CAP 37D7 C67 CAP 37D4 C68 CAP 37D6 C69 CAP 20B5 C70 CAP 20B6 C71 CAP_P 50B1 C72 CAP 20H7 C73 CAP 20H7	C74 CAP 37B7 C75 CAP 20H5 C76 CAP 37B7 C77 CAP 34D3 C78 CAP 20H6 C79 CAP 20H4 C80 CAP 20H2 C81 CAP 20H7 C82 CAP 20H4 C83 CAP 20H3 C84 CAP 20H8 C85 CAP_P 41C6 C86 CAP 20H8 C87 CAP 19B3 C88 CAP_P 50B1 C89 CAP 20H2 C90 CAP 20H7 C91 CAP 19B4 C92 CAP 36B6 C93 CAP 19C4 C94 CAP 19C3 C95 CAP 20H5 C96 CAP 20H2 C97 CAP 19B3 C98 CAP 20H6 C99 CAP 19D2 C100 CAP 19D3 C101 CAP 19D3 C102 CAP 19C3 C103 CAP 19D3 C104 CAP 19D4 C105 CAP 19B3 C106 CAP_P 50B2 C107 CAP 44B8 C108 CAP 44B8 C109 CAP 19D3 C110 CAP 19D2 C111 CAP 19B4 C112 CAP 19B2 C113 CAP_P 48A4 C114 CAP 34D3 C115 CAP 20H3 C116 CAP 19B3 C117 CAP 19D4 C118 CAP 19C3 C119 CAP 25B4 C120 CAP 19C3 C121 CAP 41C4 C122 CAP 44C8 C123 CAP 32C2 C124 CAP 20H1 C125 CAP 25B5 C126 CAP_P 41C7 C127 CAP_P 41B2 C128 CAP 24D3 C129 CAP 19B3 C130 CAP 25B5 C131 CAP 25B4 C132 CAP_P 50B2 C133 CAP 20H6 C134 CAP 19D4 C135 CAP 19C3 C136 CAP 19B3 C137 CAP 19B4 C138 CAP_P 48A5 C139 CAP 19D2 C140 CAP 19C2 C141 CAP 22B3 C142 CAP 22D5 C143 CAP 22D4 C144 CAP 22D5 C145 CAP 20H2 C146 CAP 19D1 C147 CAP 19C3 C148 CAP 19C4 C149 CAP 19C4 C150 CAP 19C4 C151 CAP 19C3 C152 CAP 25B5 C153 CAP 24C7 C154 CAP 10B6	C155 CAP_P 44D7 C156 CAP_P 44C7 C157 CAP 22A4 C158 CAP 22D5 C159 CAP 20H5 C160 CAP 25C6 C161 CAP 19C4 C162 CAP 24C6 C163 CAP 24C6 C164 CAP 24C7 C165 CAP 22B3 C166 CAP 22B3 C167 CAP 20H5 C168 CAP 19C4 C169 CAP 19C3 C170 CAP 24C7 C171 CAP_P 48A6 C172 CAP 22A4 C173 CAP 22B2 C174 CAP 22B4 C175 CAP 20H3 C176 CAP 19D2 C177 CAP 19B4 C178 CAP 19D4 C179 CAP 19B3 C180 CAP 19D3 C181 CAP 19B2 C182 CAP 19B2 C183 CAP 19D2 C184 CAP 19B2 C185 CAP 19D3 C186 CAP 19B4 C187 CAP 19B3 C188 CAP 19B1 C189 CAP 25C5 C190 CAP 24C7 C191 CAP 22A5 C192 CAP 19D5 C193 CAP 19B5 C194 CAP 22B4 C195 CAP 22B1 C196 CAP 22B2 C197 CAP 22B2 C198 CAP 22B4 C199 CAP 20H3 C200 CAP 19D4 C201 CAP 19D4 C202 CAP 19D3 C203 CAP 19D3 C204 CAP 42C5 C205 CAP 22D2 C206 CAP 24C2 C207 CAP 24C7 C208 CAP 43A5 C209 CAP 24B6 C210 CAP 16A3 C211 CAP 16A2 C212 CAP 24D6 C213 CAP 24D6 C214 CAP 19A3 C215 CAP 19A3 C216 CAP 22D2 C217 CAP 19C1 C218 CAP_P 51B3 C219 CAP 19C2 C220 CAP_P 50C8 C221 CAP 16B3 C222 CAP 18A8 C223 CAP 19C2 C224 CAP 24C2 C225 CAP 32C2 C226 CAP 24D6 C227 CAP 24C3 C228 CAP 24C3 C229 CAP 30C6 C230 CAP 15D7 C231 CAP 13C8 C232 CAP 13C8 C233 CAP 30D6 C234 CAP 30D7 C235 CAP_P 51B3	C236 CAP 53B3 C237 CAP_P 50C8 C238 CAP_P 53C5 C239 CAP 46A4 C240 CAP 13B8 C241 CAP 52C6 C242 CAP 16C3 C243 CAP 16C2 C244 CAP 16C3 C245 CAP_P 46D5 C246 CAP_P 53B3 C247 CAP 10D4 C248 CAP 41B4 C249 CAP 33D1 C250 CAP 33D2 C251 CAP 10D7 C252 CAP 53B2 C253 CAP 10D7 C254 CAP 53B1 C255 CAP 16C2 C256 CAP 16C1 C257 CAP 53B2 C258 CAP 53B2 C259 CAP 33D1 C260 CAP 33D2 C261 CAP 16C1 C262 CAP 49B4 C263 CAP 16C3 C264 CAP 13C4 C265 CAP 49B3 C266 CAP 49B8 C267 CAP 46D6 C268 CAP 10B8 C269 CAP_P 53D6 C270 CAP 49A5 C271 CAP 13B8 C272 CAP 49B4 C273 CAP 49C5 C274 CAP 10B8 C275 CAP 16C2 C276 CAP 16C2 C277 CAP 13B8 C278 CAP 13C6 C279 CAP 13C5 C280 CAP 13C6 C281 CAP 13C6 C282 CAP 49B6 C283 CAP 49C7 C284 CAP 49B4 C285 CAP 49B7 C286 CAP 49B7 C287 CAP 52A1 C288 CAP 13D8 C289 CAP 13D8 C290 CAP 13D8 C291 CAP 13D8 C292 CAP 13D4 C293 CAP 52A1 C294 CAP 52A1 C295 CAP_P 52C6 C296 CAP_P 49B3 C297 CAP 49C4 C298 CAP 49C5 C299 CAP 49C4 C300 CAP_P 49C3 C301 CAP_P 49C4 C302 CAP_P 52A2 C303 CAP 52C3 C304 CAP 16C2 C305 CAP 49C4 C306 CAP_P 52A2 C307 CAP_P 52A2 C308 CAP_P 52A3 C309 CAP_P 52A3 C310 CAP_P 52A2 C311 CAP 16C1 C312 CAP 31D3 C313 CAP 16C3 C314 CAP 31D3 C315 CAP 52A8 C316 CAP 52A8				
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	SCALE	SHEET	OF
	NONE	67	74

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	SCALE	SHEET	OF
	NONE	68	74

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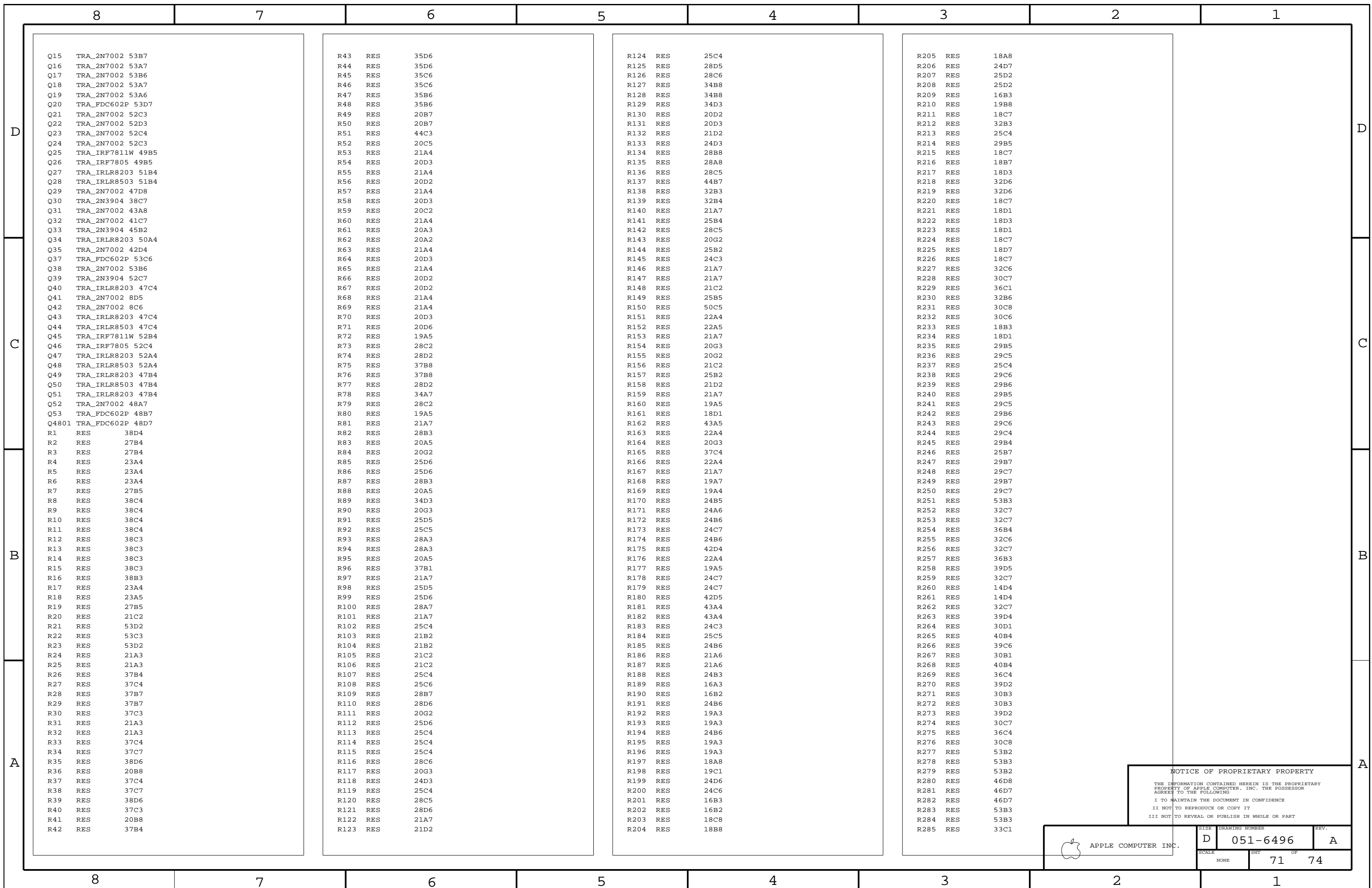
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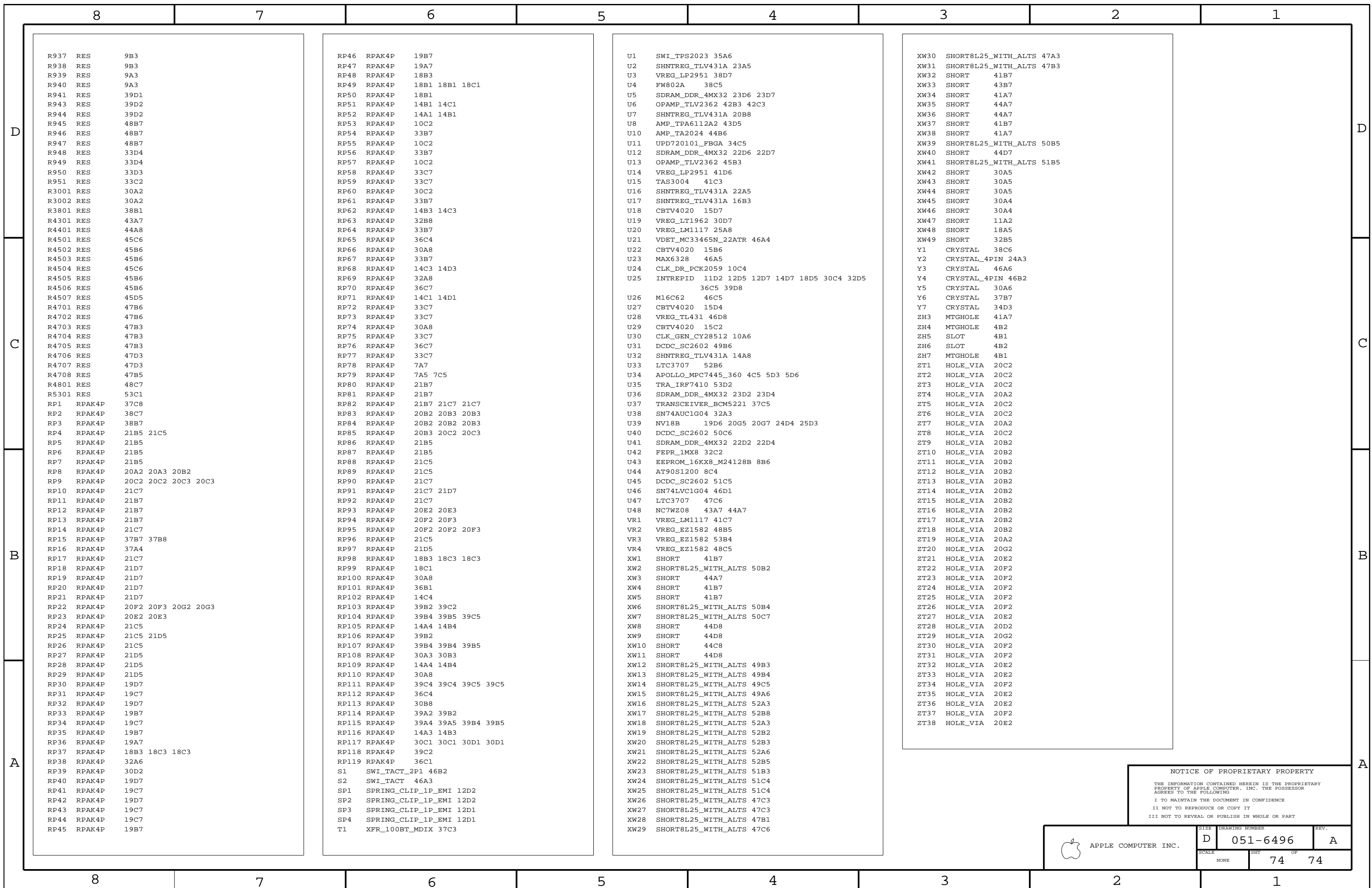
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SCALE	NONE	SHEET	72 OF 74

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D	R613 RES 31A8 R614 RES 53A4 R615 RES 53A5 R616 RES 32C7 R617 RES 32C7 R618 RES 32C7 R619 RES 18D6 R620 RES 30D5 R621 RES 32C6 R622 RES 18C6 R623 RES 39D5 R624 RES 39A7 R625 RES 14B6 R626 RES 39D2 R627 RES 39D5 R628 RES 30D5 R629 RES 30D5 R630 RES 30D5 R631 RES 10B5 R632 RES 10A3 R633 RES 10A3 R634 RES 10D5 R635 RES 39D3 R636 RES 46B6 R637 RES 36B3 R638 RES 10A3 R639 RES 10A3 R640 RES 39A5 R641 RES 30D1 R642 RES 10B3 R643 RES 10B3 R644 RES 10B5 R645 RES 53B6 R646 RES 46C1 R647 RES 36B4 R648 RES 46B2 R649 RES 46C3 R650 RES 30A2 R651 RES 30A2 R652 RES 10D7 R653 RES 46B7 R654 RES 46A5 R655 RES 46B2 R656 RES 46A6 R657 RES 46C3 R658 RES 46C3 R659 RES 46C2 R660 RES 30A2 R661 RES 30C7 R662 RES 10C6 R663 RES 10C6 R664 RES 53B6 R665 RES 46C1 R666 RES 30A6 R667 RES 18D6 R668 RES 31C3 R669 RES 31C2 R670 RES 31C2 R671 RES 46C1 R672 RES 30A6 R673 RES 36B4 R674 RES 10D3 R675 RES 10D3 R676 RES 46B4 R677 RES 46C2 R678 RES 30C8 R679 RES 39A2 R680 RES 30A8 R681 RES 14A7 R682 RES 52D6 R683 RES 30A2 R684 RES 36C1 R685 RES 53B6 R686 RES 46A7 R687 RES 46A7 R688 RES 46C2 R689 RES 46C3 R690 RES 46D3 R691 RES 30B3 R692 RES 46A3 R693 RES 46D8	R694 RES 30B3 R695 RES 30A5 R696 RES 14A7 R697 RES 14A3 R698 RES 46A3 R699 RES 46D3 R700 RES 46D3 R701 RES 46D4 R702 RES 36C4 R703 RES 14A8 R704 RES 14D4 R705 RES 31B3 R706 RES 31C3 R707 RES 36D4 R708 RES 30C8 R709 RES 36C4 R710 RES 30A5 R711 RES 30A6 R712 RES 11A3 R713 RES 11A3 R714 RES 36B7 R715 RES 14A7 R716 RES 46B8 R717 RES 46C3 R718 RES 30B3 R719 RES 32D5 R720 RES 11D3 R721 RES 52C8 R722 RES 46C6 R723 RES 30B3 R724 RES 30C3 R725 RES 46B6 R726 RES 46B7 R727 RES 30C7 R728 RES 30B3 R729 RES 46C6 R730 RES 46C7 R731 RES 46B6 R732 RES 46C7 R733 RES 46B7 R734 RES 46B7 R735 RES 30C7 R736 RES 30B3 R737 RES 40C7 R738 RES 53B7 R739 RES 53C7 R740 RES 53A7 R741 RES 53A6 R742 RES 30B3 R743 RES 40C4 R744 RES 40C7 R745 RES 40C3 R746 RES 30B8 R747 RES 30B6 R748 RES 10A5 R749 RES 30B8 R750 RES 30B8 R751 RES 53A8 R752 RES 11A3 R753 RES 39C2 R754 RES 39D4 R755 RES 10B7 R756 RES 10A7 R757 RES 11A4 R758 RES 40C1 R759 RES 39D2 R760 RES 40C5 R761 RES 39C5 R762 RES 30B3 R763 RES 30B3 R764 RES 11B4 R765 RES 11A4 R766 RES 11A3 R767 RES 39D2 R768 RES 39D5 R769 RES 53D7 R770 RES 53D7 R771 RES 10A7 R772 RES 11A4 R773 RES 39D2 R774 RES 39D4	R775 RES 40C7 R776 RES 11A4 R777 RES 11A4 R778 RES 14A8 R779 RES 40C1 R780 RES 40C3 R781 RES 40C5 R782 RES 40C7 R783 RES 40C4 R784 RES 40C7 R785 RES 40C4 R786 RES 40A4 R787 RES 40B4 R788 RES 40A7 R789 RES 40B7 R790 RES 40B7 R791 RES 40B7 R792 RES 40B2 R793 RES 40B6 R794 RES 52C7 R795 RES 52A6 R796 RES 17A8 R797 RES 52A5 R798 RES 52A5 R799 RES 52B8 R800 RES 47C3 R801 RES 47C3 R802 RES 52B5 R803 RES 52B5 R804 RES 52B6 R805 RES 52A3 R806 RES 52C6 R807 RES 52B5 R808 RES 52C3 R809 RES 17A8 R810 RES 52A5 R811 RES 52C5 R812 RES 8D6 R813 RES 8D6 R814 RES 52B3 R815 RES 52B3 R816 RES 8C6 R817 RES 8C6 R818 RES 8C5 R819 RES 8D4 R820 RES 8B7 R821 RES 8C7 R822 RES 8D3 R823 RES 8A5 R824 RES 8A5 R825 RES 17A3 R826 RES 8C7 R827 RES 51B5 R828 RES 8B7 R829 RES 8A7 R830 RES 8B7 R831 RES 8B6 R832 RES 11B6 R833 RES 11D7 R834 RES 8C5 R835 RES 8C5 R836 RES 8C2 R837 RES 8B2 R838 RES 8C2 R839 RES 8D3 R840 RES 7C7 R841 RES 7C7 R842 RES 7B7 R843 RES 7A7 R844 RES 7A7 R845 RES 7B7 R846 RES 7B7 R847 RES 7B7 R848 RES 7D5 R849 RES 7B7 R850 RES 4C2 R851 RES 7B7 R852 RES 11D7 R853 RES 11D7 R854 RES 11D7 R855 RES 11B6	R856 RES 7C5 R857 RES 7B5 R858 RES 7C5 R859 RES 7C5 R860 RES 7B5 R861 RES 11C7 R862 RES 11D7 R863 RES 11B6 R864 RES 11B7 R865 RES 11B7 R866 RES 11D6 R867 RES 11D5 R868 RES 11B7 R869 RES 11B5 R870 RES 11A5 R871 RES 51C3 R872 RES 51C3 R873 RES 51C5 R874 RES 11D6 R875 RES 11D5 R876 RES 11B7 R877 RES 11D5 R878 RES 11D6 R879 RES 11D6 R880 RES 51C3 R881 RES 51C3 R882 RES 7B5 R883 RES 51B6 R884 RES 51C5 R885 RES 11B6 R886 RES 11A6 R887 RES 11C6 R888 RES 51D5 R889 RES 11D6 R890 RES 11B8 R891 RES 4D6 R892 RES 11B7 R893 RES 11B7 R894 RES 11B8 R895 RES 4D2 R896 RES 47C5 R897 RES 47B5 R898 RES 47B5 R899 RES 47D6 R900 RES 47C5 R901 RES 4D3 R902 RES 7A4 R903 RES 7A4 R904 RES 7A4 R905 RES 7A4 R906 RES 7B4 R907 RES 7B4 R908 RES 47D6 R909 RES 7B5 R910 RES 7B5 R911 RES 7B5 R912 RES 7A5 R913 RES 7C4 R914 RES 7C4 R915 RES 7C4 R916 RES 7B4 R917 RES 7A4 R918 RES 7C4 R919 RES 7B4 R920 RES 7B4 R921 RES 7B5 R922 RES 7A5 R923 RES 7A5 R924 RES 7D5 R925 RES 7C5 R926 RES 7B4 R927 RES 48C5 R928 RES 47C5 R929 RES 47C5 R930 RES 48C5 R931 RES 47D7 R932 RES 47C7 R933 RES 47D7 R934 RES 47C8 R935 RES 47A5 R936 RES 47A5	D			
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	NONE	D 051-6496	A
	SHEET	OF	
	73	74	




R937 RES 9B3
R938 RES 9B3
R939 RES 9A3
R940 RES 9A3
R941 RES 39D1
R943 RES 39D2
R944 RES 39D2
R945 RES 48B7
R946 RES 48B7
R947 RES 48B7
R948 RES 33D4
R949 RES 33D4
R950 RES 33D3
R951 RES 33C2
R3001 RES 30A2
R3002 RES 30A2
R3801 RES 38B1
R4301 RES 43A7
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R4705 RES 47B3
R4706 RES 47D3
R4707 RES 47D3
R4708 RES 47B5
R4801 RES 48C7
R5301 RES 53C1
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RP3 RPAK4P 38B7
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RP118 RPAK4P 39C2
RP119 RPAK4P 36C1
S1 SWI_TACT_2P1 46B2
S2 SWI_TACT 46A3
SP1 SPRING_CLIP_1P_EMI 12D2
SP2 SPRING_CLIP_1P_EMI 12D2
SP3 SPRING_CLIP_1P_EMI 12D1
SP4 SPRING_CLIP_1P_EMI 12D1
T1 XFR_100BT_MDIX 37C3

U1 SWI_TPS2023 35A6
U2 SHNTREG_TLV431A 23A5
U3 VREG_LP2951 38D7
U4 FW802A 38C5
U5 SDRAM_DDR_4MX32 23D6 23D7
U6 OPAMP_TLV2362 42B3 42C3
U7 SHNTREG_TLV431A 20B8
U8 AMP_TPA6112A2 43D5
U10 AMP_TA2024 44B6
U11 UPD720101_FBGA 34C5
U12 SDRAM_DDR_4MX32 22D6 22D7
U13 OPAMP_TLV2362 45B3
U14 VREG_LP2951 41D6
U15 TAS3004 41C3
U16 SHNTREG_TLV431A 22A5
U17 SHNTREG_TLV431A 16B3
U18 CBTV4020 15D7
U19 VREG_LT1962 30D7
U20 VREG_LM1117 25A8
U21 VDET_MC33465N_22ATR 46A4
U22 CBTV4020 15B6
U23 MAX6328 46A5
U24 CLK_DR_PCK2059 10C4
U25 INTREPID 11D2 12D5 12D7 14D7 18D5 30C4 32D5
U26 M16C62 46C5
U27 CBTV4020 15D4
U28 VREG_TL431 46D8
U29 CBTV4020 15C2
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U31 DCDC_SC2602 49B6
U32 SHNTREG_TLV431A 14A8
U33 LTC3707 52B6
U34 APOLLO_MPC7445_360 4C5 5D3 5D6
U35 TRA_IRF7410 53D2
U36 SDRAM_DDR_4MX32 23D2 23D4
U37 TRANSCEIVER_BCM5221 37C5
U38 SN74AUC1G04 32A3
U39 NV18B 19D6 20G5 20G7 24D4 25D3
U40 DCDC_SC2602 50C6
U41 SDRAM_DDR_4MX32 22D2 22D4
U42 FEPR_LMX8 32C2
U43 EEPROM_16KX8_M24128B 8B6
U44 AT90S1200 8C4
U45 DCDC_SC2602 51C5
U46 SN74LVCI604 46D1
U47 LTC3707 47C6
U48 NC7WZ08 43A7 44A7
VR1 VREG_LM1117 41C7
VR2 VREG_EZ1582 48B5
VR3 VREG_EZ1582 53B4
VR4 VREG_EZ1582 48C5
XW1 SHORT 41B7
XW2 SHORT8L25_WITH_ALTS 50B2
XW3 SHORT 44A7
XW4 SHORT 41B7
XW5 SHORT 41B7
XW6 SHORT8L25_WITH_ALTS 50B4
XW7 SHORT8L25_WITH_ALTS 50C7
XW8 SHORT 44D8
XW9 SHORT 44D8
XW10 SHORT 44C8
XW11 SHORT 44D8
XW12 SHORT8L25_WITH_ALTS 49B3
XW13 SHORT8L25_WITH_ALTS 49B4
XW14 SHORT8L25_WITH_ALTS 49C5
XW15 SHORT8L25_WITH_ALTS 49A6
XW16 SHORT8L25_WITH_ALTS 52A3
XW17 SHORT8L25_WITH_ALTS 52B8
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XW19 SHORT8L25_WITH_ALTS 52B2
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XW25 SHORT8L25_WITH_ALTS 51C4
XW26 SHORT8L25_WITH_ALTS 47C3
XW27 SHORT8L25_WITH_ALTS 47C3
XW28 SHORT8L25_WITH_ALTS 47B1
XW29 SHORT8L25_WITH_ALTS 47C6

XW30 SHORT8L25_WITH_ALTS 47A3
XW31 SHORT8L25_WITH_ALTS 47B3
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XW33 SHORT 43B7
XW34 SHORT 41A7
XW35 SHORT 44A7
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XW44 SHORT 30A5
XW45 SHORT 30A4
XW46 SHORT 30A4
XW47 SHORT 11A2
XW48 SHORT 18A5
XW49 SHORT 32B5
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Y2 CRYSTAL_4PIN 24A3
Y3 CRYSTAL 46A6
Y4 CRYSTAL_4PIN 46B2
Y5 CRYSTAL 30A6
Y6 CRYSTAL 37B7
Y7 CRYSTAL 34D3
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ZH4 MTGHOLE 4B2
ZH5 SLOT 4B1
ZH6 SLOT 4B2
ZH7 MTGHOLE 4B1
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