3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 

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**PCB SPECS**

**THICKNESS** : 1.2 MM / 0.047 IN  
1/2 OZ CU THICKNESS: 0.7 MILS  
1.0 OZ CU THICKNESS: 1.4 MILS

**IMPEDANCE** : 50 OHMS +/- 10%  
**DIELECTRIC** : FR-4  
**LAYER COUNT** : 12  
**SIGNAL TRACE WIDTH** : 4 MILS  
**SIGNAL TRACE SPACING** : 4 MILS  
**PREPREG THICKNESS** : 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

**BOARD STACK-UP AND CONSTRUCTION**

1. PREPREG (3MIL)  
2. PREPREG (3MIL)  
3. LAMINATE (4MIL)  
4. PREPREG (3MIL)  
5. LAMINATE (4MIL)  
6. PREPREG (2MIL)  
7. LAMINATE (3MIL)  
8. PREPREG (2MIL)  
9. LAMINATE (4MIL)  
10. PREPREG (3MIL)  
11. LAMINATE (4MIL)  
12. PREPREG (3MIL)

**SIGNAL** (1/3 OZ + COPPER PLATING)  
**GROUND** (1/2 OZ)  
**SIGNAL** (1/2 OZ)  
**SIGNAL** (1/2 OZ)  
**GROUND** (1/2 OZ)  
**CUT POWER PLANE (1 OZ)**  
**GROUND** (1/2 OZ)  
**SIGNAL** (1/2 OZ)  
**SIGNAL** (1/2 OZ)  
**GROUND** (1/2 OZ)  
**SIGNAL** (1/3 OZ + COPPER PLATING)
CPU PLL CONFIG CIRCUITRY

PLL SPEED BASED ON 167MHZ - 1GHZ/667MHZ

CPU PLL CONFIGURATION

MULTIPLIER

<table>
<thead>
<tr>
<th>MULTIPLIER</th>
<th>BUS TO CORE (MHZ)</th>
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<tr>
<td>0.0X</td>
<td>PLL OFF</td>
<td>0 1111 0F</td>
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<td>1.0X</td>
<td>PLL BYPASS</td>
<td>0 0011 03</td>
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<tr>
<td>2.0X</td>
<td>333 267</td>
<td>0 0100 04</td>
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<td>3.0X</td>
<td>500 400</td>
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<td>2250 1800</td>
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<td>18.0X</td>
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<tr>
<td>28.0X</td>
<td>4667 3733</td>
<td>1 1110 1E</td>
</tr>
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CPU FREQUENCY CONFIGURATION

APOLLO REV 3.0

1) IF MANUFACTURER'S NAME IS NOT ON THIS SHEET, ADD IT TO MAINTAIN THE DOCUMENT IN CONFIDENCE
2) DETAIL SHEET NOT TO REPRODUCE OR COPY IT
L3 REFERENCE VOLTAGE

- R624, 1/16W, 5%
- R645, 402, MF
- CERM, 1/16W, 1%
- C667, 20%10V

Split caps of same value evenly between SRAM chips

- L3_DQPD<1>, L3_DQPD<0>
- JTAG_L3_TCK
- L3_PULLDOWN<1>

HAVE TO CONNECT L3_ADDR17 TO THIS PIN

- 6.3V, CERM
- 10UF, CERM

Directly underneath the chips

- BALL F9, K9 CONNECTED TO GND
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
NOTE: Designers using AGP slot should use J10 when a connector block.

AGP pixel_clock is routed the same length as CBUS_PCI_GNT_L.

Intrepid AGP/PCI

Series resistors for boot ROM control signals place close to Intrepid side.

USB2 and CROS REQ REMAINS ON +3.3V_MAIN because these chips are powered in sleep.
MAP17 BOOT STRAPS
## CRC-29

**SHUTDOWN STATE (BATT)**

- **SLEEP** (AC)
- **RUN** (AC)
- **RUNNING OR WHEN ASLEEP ON AC**

### PMU_POWER_UP_L

- **+PBUS**
- **33V_PMU**
- **AC_IN**
- **1.5AMP-33V**

### AC_IN_FW_CNTL

- **+FW_FUSE**
- **BAS16TW**
- **2N7002DW**
- **AC_IN_FW_GATE**

### POWER_UP

- **Q17**
- **1/16W**
- **20%16V**

### CLEAR OUT ALL PLANES UNDER TRANSFORMERS

- **FW_TPB0N**
- **FW_TPB0P**
- **FW_TPA0N**
- **FW_TPA0P**

### FIREWIRE A

- **PORT 1**

### FIREWIRE B - BILINGUAL

- **PORT 0**

### NOTICE OF PROPRIETARY PROPERTY

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A brief should be hard connected to logic ground for speed signaling and connection detection currents per 1394B spec.

**REV.** 29 44

**DRAWING NUMBER** 051-6442

**APPLE COMPUTER INC.**
### Differential Signals

**INTERNAL LAYER**
- \( \varepsilon_r = 4.3 \) (Dielectric Constant)
- \( W = 4\text{mil} \) (Trace Width)
- \( B = 12.2\text{mil} \) (Dist between 2 GND planes)
- \( T = 0.7\text{mil} \) (Trace Thickness)
- \( S = 1\text{mil} \) (Separation of Diff traces)
- Single = 51.5\text{ohm}
- Diff = 99.8\text{ohm}

**For Firewire**

**INTERNAL LAYER (USB1.1/USB 2.0)**
- \( \varepsilon_r = 4.3 \) (Dielectric Constant)
- \( W = 3.4\text{mil} \) (Trace Width)
- \( B = 12.2\text{mil} \) (Dist between 2 GND planes)
- \( T = 0.7\text{mil} \) (Trace Thickness)
- \( S = 1\text{mil} \) (Separation of Diff traces)
- Single = 53.7\text{ohm}
- Diff = 107.1\text{ohm}

**SIGNAL CONSTRAINTS - PAGE 2**

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**For Firewire**
REV 2.0 - 08/26/02

- CHANGED STUFFING OPTION TO RAISE PLL VOLTAGE TO 1.95V FOR FW
- ADDED 5 SPEAKER CLIPS SYMBOLS
- ADDED FOUR PULL-DOWN RESISTORS ON CKE FOR DDR MEMORY
- CHANGED TO NEW 30PIN TUBA CONNECTOR WITH SOLDER TAPS
- CHANGED TO TOP CONTACT SPIDEY CONNECTOR
- UPDATED BOM OPTION FOR SSCG
- CHANGED Q47 AND Q58 TO 7811W FOR BOM CONSOLIDATION - ALSO CHANGED R348 AND R353 TO 113K TO ADJUST CURRENT LIMIT
- CONNECTED MAX4172 POWER TO +ADAPTER_SW TO SAVE 1MA WHEN RUNNING ON BATTERY ONLY
- ADDED TWO 0805 ZERO OHM RESISTORS TO FEED IN EITHER +2_5V_SLEEP OR +2_5V_MAIN TO INTREPID
- LOADED IN NEW MECHANICAL SYMBOLS FOR WIRELESS, CARDBUS, AND HARD/OPTICAL DRIVES
- CHANGED ESD AND LATE VG PROTECTION FOR FIREWIRE
- NEW BOOT ROM AND LMU PART NUMBERS
- ADDED TWO 4.7UF BULK CAPS NEAR THE FAN CONNECTORS
- ADDED PULL-DOWN TO P50'S CLKRUN_L SIGNAL AND NO CONNECTED P50'S PME SIGNAL
- CHGND1 NOW SPLITS INTO CHGND1 AND CHGND6 BECAUSE OF FIREWIRE B ROUTING ON THE SURFACE

REV 3.0 - 09/29/02

- ADDED INTREPID SSCG CHIP SUPPORT
- REMOVED PROTO1 CONNECTOR OPTIONS
- UPDATED USB 2.0 SIGNAL CONSTRAINTS
- CORRECTED PMU PART NUMBER
- REMOVED NO_TEST=TRUE PROPERTY ON MAXBUS/L3 BUS
- ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL
- UPDATED MORE CONSTRAINTS
- CHANGED TO SI3446DV FOR FAN FETS
- FINALIZED ALL CHANGES FOR SI1162 PART - RUNNING HIGH SWING MODE
- ADDED PART NUMBER TABLE FOR SPEAKER CLIP
- UPDATED DVI_HPD CIRCUIT PER HYDRA IMPLEMENTATION
- ADDED SILICON IMAGE SI1162 - FIRST PASS
- REPLACED LMC6462 WITH LMC7111 BECAUSE ONLY NEED 1 OP-AMP
- ADDED C843 TO SPEED UP Q10 TURN ON AND CHANGED Q14 TURN ON TO AC_IN
- DELETED OLD BATTERY CURRENT LIMITER CIRCUIT
- DISCONNECTED FW_LKON FROM INT_EXTINT3_PU BECAUSE FW_LKON OUTPUT NOW WORKS FINE
- CHANGED TO 10K PULL-DOWN FOR MOD_DTI, MOD_SYNC, AND MOD_BITCLK - PER INTREPID PADS SPREADSHEET
- CHANGED TO NEW MOUNTING HOLE SIZES - ALL INCREASED BY 0.2MM IN DIAMETER EXCEPT FOR THREE CPU MTG HOLES
- DELETED ALL INTREPID_REV1 STUFFING OPTION
- REMOVED PROTO1 CONNECTOR OPTIONS
- DELETED PULL-UP RESISTOR TO VCORE_VCC ON VGATE SINCE THERE'S A 10K PULL-UP RESISTOR ON INTREPID SIDE
- FIXED AGP CLOCK CONSTRAINTS
- SWITCHED TO NEW 16PIN MODEM CONNECTOR
- REMOVED NO_TEST=TRUE PROPERTY ON MAXBUS/L3 BUS
- ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL
- REV 4.0 - 10/24/02

- ADDED 2 JUMPERS FOR PMU_RESET_BUTTON_L AND PMU_NMI_BUTTON_L
- ADDED 0 OHM RESISTOR FOR POWER BUTTON - DEBUG
- UPDATED L3 SYMBOLS TO REFLECT MISSING SA17 SIGNAL ON 4MBIT PARTS VS. 8MBIT PARTS
- NO STUFFED L4 AND L5, FIREWIRE COMMON MODE CHOKES
- NO STUFFED 4700PF FOR 14V PBUS GATE - C741
- CHANGED FL1 TO NEW COMMON MODE CHOKES FOR FIREWIRE A
- MERGED MAXBUS_MAIN WITH MAXBUS_SLEEP BECAUSE INTREPID MAXBUS I/O CAN BE POWERED DOWN IN SLEEP (PG 16, 17)
- UPDATED BOM OPTION FOR SSCG
- CHANGED SCHEMATIC NUMBER TO 051-6425 AND PCB NUMBER TO 820-1502
- REMOVED ALL JUMPERS FOR PRODUCTION (PG TOO MANY)
- REMOVED U1 BECAUSE NO USING 1.5V MAXBUS NOR 1.5V L3 INTERFACE STRAPS
- REMOVED R621 AND CONNECTED R608 TO GROUND WITH 10K RESISTOR TO ENSURE KBD LED IS OFF WHEN LMU IS IN RESET
- REMOVED R451 TO 10K FROM 100K - OTHERWISE, IT MAY BE TOO WEAK
- REMOVED 1.5V AGP(DOUBLED BYPASS), C24, C20 - 3VMAIN (DOUBLED BYPASS) FOR TESTPOINTS
- CHANGED STUFFING OPTION TO ENABLE 1.5V_LDO AND MAKE 1.5V_MAIN INTO 1.8V
- REMOVED COMMON MODE CHOKE FOR FIREWIRE B SIGNALS
- CHANGED STUFFING OPTION TO RAISE PLL VOLTAGE TO 1.95V FOR FW
- REMOVED COMMON MODE CHOKES FOR FIREWIRE A
- CHANGED TO SI3446DV FOR FAN FETS
- ADDED 5 SPEAKER CLIPS SYMBOLS
- ADDED FOUR PULL-DOWN RESISTORS ON CKE FOR DDR MEMORY
- CHANGED TO NEW 30PIN TUBA CONNECTOR WITH SOLDER TAPS
- CHANGED TO TOP CONTACT SPIDEY CONNECTOR
- UPDATED BOM OPTION FOR SSCG
- CHANGED Q47 AND Q58 TO 7811W FOR BOM CONSOLIDATION - ALSO CHANGED R348 AND R353 TO 113K TO ADJUST CURRENT LIMIT
- CONNECTED MAX4172 POWER TO +ADAPTER_SW TO SAVE 1MA WHEN RUNNING ON BATTERY ONLY
- ADDED TWO 0805 ZERO OHM RESISTORS TO FEED IN EITHER +2_5V_SLEEP OR +2_5V_MAIN TO INTREPID
- LOADED IN NEW MECHANICAL SYMBOLS FOR WIRELESS, CARDBUS, AND HARD/OPTICAL DRIVES
- ADDED SILICON IMAGE SI1162 - FIRST PASS
- REPLACED LMC6462 WITH LMC7111 BECAUSE ONLY NEED 1 OP-AMP
- ADDED C843 TO SPEED UP Q10 TURN ON AND CHANGED Q14 TURN ON TO AC_IN
- DELETED OLD BATTERY CURRENT LIMITER CIRCUIT
- DISCONNECTED FW_LKON FROM INT_EXTINT3_PU BECAUSE FW_LKON OUTPUT NOW WORKS FINE
- CHANGED TO 10K PULL-DOWN FOR MOD_DTI, MOD_SYNC, AND MOD_BITCLK - PER INTREPID PADS SPREADSHEET
- CHANGED TO NEW MOUNTING HOLE SIZES - ALL INCREASED BY 0.2MM IN DIAMETER EXCEPT FOR THREE CPU MTG HOLES
- DELETED ALL INTREPID_REV1 STUFFING OPTION
- REMOVED PROTO1 CONNECTOR OPTIONS
- REMOVED NO_TEST=TRUE PROPERTY ON MAXBUS/L3 BUS
- CHANGED STUFFING OPTION TO ENABLE 1.5V_LDO AND MAKE 1.5V_MAIN INTO 1.8V
- ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL
- REV 5.0 - 12/03/02

- TEST IS ONLY TYPED ON 7-SHEEP NON (PG 23)
- COMPLIES WITH INSTRUCTION FOR THE COMMON MODE CHOKES
- CHANGED SCHEMATIC NUMBER TO 051-6425 AND PCB NUMBER TO 820-1502
- REMOVED L3 INTERFACE STRAPS
- Merged MAXBUS_MAIN WITH MAXBUS_SLEEP BECAUSE INTREPID MAXBUS I/O CAN BE POWERED DOWN IN SLEEP (PG 16, 17)
- ADDED INTREPID SSCG CHIP SUPPORT
- REMOVED PROTO1 CONNECTOR OPTIONS
- ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL
- REMOVED COMMON MODE CHOKE FOR FIREWIRE B SIGNALS
- CHANGED STUFFING OPTION TO RAISE PLL VOLTAGE TO 1.95V FOR FW