1. All resistance values are in ohms, 0.1 Watt or less.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

**Title Page and Contents**

- **Page 1**: Title Page and Contents
- **Page 2**: System Block Diagram
- **Page 3**: Power Block Diagram
- **Page 4**: PCB Notes and Holes
- **Page 5**: MPC7450 MAXBUS Interface
- **Page 6**: MPC7450 Data
- **Page 7**: CPU PLL and Configuration Straps
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- **Page 9**: Intrepid Memory Interface / Boot ROM
- **Page 10**: DDR Memory Mixes
- **Page 11**: 200Pin DDR Memory Sodim Connectors
- **Page 12**: Intrepid AGP 4x/PCI
- **Page 13**: Intrepid Emt/Pk/Usa/Usa Interfaces
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- **Page 18**: MAP31 AGP & Frame Buffer
- **Page 19**: MAP31 LVDS/TMD/FGPO & GPU Vcore
- **Page 20**: MAP31 Analog, Dvd Interface, Gnd
- **Page 21**: Video Connectors - Inverter, Dvi, Z-Video Dual-Channel Lvds
- **Page 22**: Lmi, Light Sensor, Boostgainer, Sleep Led
- **Page 23**: Internal Connectors - Dvd, Cardslot, Bard Drive, Left Usb/Bluetooth
- **Page 24**: Fan Controller, Maxim, Sound Serial Debug (Jolly Roger, Pwr/Bmt/Reset)
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- **Page 26**: Marvell Gigabit Ethernet Phy
- **Page 27**: Firewire A/B Phy
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- **Page 30**: Battery Charger and Connector
- **Page 31**: 12.8v System Power Supply / Pmu Power Supply
- **Page 32**: 3.3v / 5v System Power Supplies
- **Page 33**: Cpu Core Voltage Power Supply
- **Page 34**: 1.5v/ 1.8v / 2.5v System Power Supplies
- **Page 35**: Signal Constraints (1 of 2) - Digital/Clk
- **Page 36**: Signal Constraints (2 of 2) - Digital/Diff
- **Page 37**: Signal Constraints (3 of 3) - Power Nets
- **Page 38**: Functional Test Points
- **Page 39**: Revision History (1 of 1)
- **Page 40-41**: Signal Names
- **Page 42-43**: Component Locations

**BOM Options**

- 03_HOT
- 03_Cold
- GPU_SS
- GPU_Switch
- Serial_Debug
- Vcore_Offset
- 1_5v_Maxbus
- 1_5v_Maxbus
- NEC_USB
- 1_8v_Maxbus
- 1_8v_Maxbus
- BBANG
- BBANG
- Map31
- Map31
- SSCG
- SSCG
- 5v_Ad.Logic
- 5v_Ad.Logic
- 3v_Ad.Logic
- 3v_Ad.Logic
**PCB SPECS**

THICKNESS: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDEANCE: 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

**BOARD STACK-UP AND CONSTRUCTION**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIGNAL (1/3 OZ + COPPER PLATING)</td>
</tr>
<tr>
<td>2</td>
<td>PREPREG (3MIL)</td>
</tr>
<tr>
<td>3</td>
<td>LAMINATE (4MIL)</td>
</tr>
<tr>
<td>4</td>
<td>PREPREG (3MIL)</td>
</tr>
<tr>
<td>5</td>
<td>LAMINATE (4MIL)</td>
</tr>
<tr>
<td>6</td>
<td>PREPREG (2MIL)</td>
</tr>
<tr>
<td>7</td>
<td>LAMINATE (3MIL)</td>
</tr>
<tr>
<td>8</td>
<td>PREPREG (2MIL)</td>
</tr>
<tr>
<td>9</td>
<td>LAMINATE (4MIL)</td>
</tr>
<tr>
<td>10</td>
<td>PREPREG (3MIL)</td>
</tr>
<tr>
<td>11</td>
<td>LAMINATE (4MIL)</td>
</tr>
<tr>
<td>12</td>
<td>PREPREG (3MIL)</td>
</tr>
</tbody>
</table>

**BOARD INFORMATION**

APPLE COMPUTER INC. 051-6443 03
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

BIT 0..15

BIT 16..31

BIT 32..47

BIT 48..63
facilitate NAND-tree testing
<table>
<thead>
<tr>
<th>Name</th>
<th>Signal</th>
<th>Min Speed</th>
<th>Max Speed</th>
<th>Min Min</th>
<th>Max Min</th>
<th>Min Max</th>
<th>Max Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT_CPUFB_IN_NORM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT_CPUFB_OUT_SHORT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYSCLK_CPU</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>SYSCLK_CPU_UF</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CPU_TEA_L</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CPU_DATA&lt;0..31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_CI_L</td>
<td></td>
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<tr>
<td>CPU_QREQ_L</td>
<td></td>
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<tr>
<td>CPU_QACK_L</td>
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<td></td>
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<tr>
<td>CPU_WT_L</td>
<td></td>
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<tr>
<td>CPU_TA_L</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>MAP31</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ETHERNET</td>
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<tr>
<td>ENTITY</td>
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<tr>
<td>FIREWIRE</td>
<td></td>
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<tr>
<td>BUSY</td>
<td></td>
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<tr>
<td>CLOCKS</td>
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<tr>
<td>NEY</td>
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<tr>
<td>DDB</td>
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<tr>
<td>RAM</td>
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<tr>
<td>GROUP 0</td>
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<td></td>
<td></td>
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<tr>
<td>GROUP 1</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GROUP 2/3</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>GROUP 4/5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GROUP 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GROUP 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDR</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CONTROL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_ADDR&lt;12..0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM_DQM_A&lt;7&gt;</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM_DQS_A&lt;7&gt;</td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>MEM_DQS&lt;7&gt;</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>MEM_DQS&lt;6&gt;</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA&lt;55..48&gt;</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>RAM_DQM_B&lt;5..4&gt;</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>RAM_DQM_A&lt;5..4&gt;</td>
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<tr>
<td>MEM_DQM&lt;5..4&gt;</td>
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<tr>
<td>MEM_DQS&lt;5..4&gt;</td>
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<tr>
<td>MEM_DQM&lt;3..2&gt;</td>
<td></td>
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<tr>
<td>RAM_DQS_B&lt;3..2&gt;</td>
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<tr>
<td>RAM_DQS_A&lt;3..2&gt;</td>
<td></td>
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</tr>
<tr>
<td>MEM_DQS&lt;3..2&gt;</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>RAM_DQS_A&lt;1&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQS&lt;1&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA&lt;15..8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM_DQS_B&lt;0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQS&lt;0&gt;</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA&lt;7..0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_CLK27M_OUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPU_FBCLK1_L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPU_SSCLK_IN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPU_CLK27M_OUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPU_FBCLK1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ETHenet_PHY_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIENET_LINK_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIENET_PHY_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIENET_LINK_GBE_REF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIENET_PHY_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_CLK27M</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIK27M_GPU_XOUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIK33M_CBUS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIK33M_USB2_UF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIK66M_GPU_AGP_UF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLIK18M_INT_XOUT</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**TOTAL LENGTH CONTROLLED BY SPREADSHEET**

200.0000

**10 MIL SPACING**

250.0000

**5 MIL SPACING**

500.0000

**NET SPACING TYPE**

49.15 MHz:::

98.03 MHz:::

200.0000

25.00 MHz:::

125.0 MHz:::

500.0000

33.00 MHz:::

33.00 MHz:::

33.00 MHz:::

500.0000
### Differential Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Logic Type</th>
<th>Clock Type</th>
<th>Application Type</th>
<th>Technology Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>B</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>C</td>
<td></td>
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<tr>
<td>D</td>
<td></td>
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<td></td>
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<tr>
<td>E</td>
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<tr>
<td>F</td>
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<tr>
<td>G</td>
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<td>H</td>
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<td>I</td>
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<td>J</td>
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<td>K</td>
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<td>L</td>
<td></td>
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<td></td>
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<td>M</td>
<td></td>
<td></td>
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<td></td>
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<td>N</td>
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<tr>
<td>P</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Q</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>R</td>
<td></td>
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<td>V</td>
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<td>W</td>
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<td>Z</td>
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</tbody>
</table>

### Signal Constraints - Page 2

**INTERNAL LAYER**

- $\varepsilon_r = 4.3$ (Dielectric Constant)
- $W = \text{mils}$ (Trace Width)
- $B = 12.2\text{mils}$ (Distn Between 2 Gnd Planes)
- $T = 0.7\text{mils}$ (Trace Thickness)
- $S = \text{mils}$ (Separation of Diff Traces)
- $Z_{	ext{single}} = 51.7\text{ohms}$
- $Z_{	ext{off}} = 99.8\text{ohms}$

**FOR FIREWIRE**

- $\varepsilon_r = 4.3$ (Dielectric Constant)
- $W = \text{mils}$ (Trace Width)
- $B = 12.2\text{mils}$ (Distn Between 2 Gnd Planes)
- $T = 0.7\text{mils}$ (Trace Thickness)
- $S = \text{mils}$ (Separation of Diff Traces)
- $Z_{	ext{single}} = 53.3\text{ohms}$
- $Z_{	ext{off}} = 107.1\text{ohms}$

**INTERNAL LAYER (USB1.1/USB 2.0)**

- $\varepsilon_r = 4.3$ (Dielectric Constant)
- $W = \text{mils}$ (Trace Width)
- $B = 12.2\text{mils}$ (Distn Between 2 Gnd Planes)
- $T = 0.7\text{mils}$ (Trace Thickness)
- $S = \text{mils}$ (Separation of Diff Traces)
- $Z_{	ext{single}} = 51.5\text{ohms}$ (USB 1.1)/ 46.2ohms (USB 2.0)
- $Z_{	ext{off}} = 89.3\text{ohms}$ (USB 1.1)/ 89.4ohms (USB 2.0)

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### Part Cross-Reference for the entire design

<table>
<thead>
<tr>
<th>Column 1</th>
<th>Column 2</th>
<th>Column 3</th>
<th>Column 4</th>
<th>Column 5</th>
<th>Column 6</th>
<th>Column 7</th>
<th>Column 8</th>
<th>Column 9</th>
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</tr>
</tbody>
</table>

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**Notes:**

1. This is a part cross-reference for the entire design.
2. The columns represent different sections or layers of the design.
3. Each cell contains the component type, number, and possibly additional details.
4. The design is likely a circuit diagram with components placed in various rows and columns.

---

**Legend:**

- **TRA:** Transistor
- **IND:** Inductor
- **FUSE:** Fuse
- **DIODE:** Diode
- **RES:** Resistor

---

**Example Entries:**

- **TRA_2N7002DW 30:** Transistor 2N7002DW, section 30
- **IND_3P 32:** Inductor 3P, section 32
- **FUSE 30:** Fuse, section 30
- **DIODE_SCHOT 34:** Diode Schottky, section 34
- **RES 32:** Resistor, section 32

---

**Additional Information:**

- The diagram uses a grid format with labels for each section.
- Specific components and their placements are detailed in the table format provided.
- The design likely involves electronic components necessary for a specific application or circuit function.
R627 RES  34
R623 RES  24
R622 RES  14
R621 RES  13
R619 RES  22
R618 RES  22
R615 RES  22
R614 RES  14
R612 RES  23
R611 RES  19
R610 RES  19
R608 RES  19
R607 RES  19
R606 RES  22
R605 RES  22
R601 RES  23
R596 RES  29
R593 RES  29
R590 RES  25
R582 RES  22
R578 RES  30
R577 RES  27
R574 RES  27
R571 RES  30
R570 RES  30
R569 RES  29
R568 RES  22
R567 RES  30
R565 RES  30
R564 RES  27
R562 RES  29
R555 RES  27
R553 RES  24
R548 RES  30
R547 RES  27
R544 RES  29
R541 RES  31
R540 RES  25
R538 RES  32
R532 RES  22
R531 RES  25
R528 RES  32
R525 RES  27
R522 RES  27
R520 RES  32
R516 RES  27
R515 RES  32
R513 RES  29
R512 RES  30
R509 RES  27
R508 RES  31
R507 RES  32
R506 RES  32
R505 RES  29
R501 RES  29
R499 RES  30
R498 RES  30
R494 RES  27
R492 RES  29
R488 RES  30
R484 RES  27
R483 RES  31
R482 RES  32
R473 RES  30
R472 RES  28
R471 RES  27
R464 RES  27
R452 RES  8 7 6 5 4 3 2 1
ZT26 HOLE_VIA  4
ZT20 HOLE_VIA  4
ZT19 HOLE_VIA  4
ZT18 HOLE_VIA  4
ZT14 HOLE_VIA  4
ZT12 HOLE_VIA  4
ZT9  HOLE_VIA  4
ZT5  MTGHOLE   4
ZT2  MTGHOLE   4
Y3   CRYSTAL   26
Y2   CRYSTAL_4PIN  20
Y1   CRYSTAL   14
XW19 SHORT     30
XW17 JUMPER    31
XW16 JUMPER    32
XW15 SHORT     33
XW14 JUMPER    34
XW11 JUMPER    34
XW10 JUMPER    32
XW8  SHORT     32
XW4  SHORT     31
XW2  SHORT     19
XW1  SHORT     34
U51   MAX6804   29
U45   INTREPID  8 9 12 13 14 15
U41   MAX6649   19
U39   UPD720101_FBGA  25
U37   VREG_LT1962  27
U34   VREG_LM2594  27
U31   MAX1772   30
U29   TSB81BA3A  27
U25   VREG_LP2951  31
U18   LTC1625   31
U17   FEPR_1MX8  9
U15   COMPARATOR_LMC7211  30
U10   CBTV4020  10
U4    SN74AUC1G08  22
U2    SN74AUC1G08  22
SP6   SPKR_CLIP_P84  4
SP5   SPKR_CLIP_P84  4
SP2   SPKR_CLIP_P84  4
SH1   SHLD_3P_EMI  4
RP53  RPAK4P    22
RP52  RPAK4P    22 25
RP51  RPAK4P    14
RP47  RPAK4P    14
RP42  RPAK10P2C  22
RP41  RPAK4P    29
RP35  RPAK4P    9
RP28  RPAK4P    20
RP20  RPAK4P    12
RP16  RPAK4P    13
RP14  RPAK4P    13
RP13  RPAK4P    23
RP10  RPAK4P    23
RP9   RPAK4P    23
RP5   RPAK4P    23
ZT81  HOLE_VIA  4
ZT79  HOLE_VIA  4
ZT77  HOLE_VIA  4
ZT70  HOLE_VIA  4
ZT69  HOLE_VIA  4
ZT67  HOLE_VIA  4
ZT65  HOLE_VIA  4
ZT63  HOLE_VIA  4
ZT59  HOLE_VIA  4
ZT57  HOLE_VIA  4
ZT56  HOLE_VIA  4
ZT53  HOLE_VIA  4
ZT49  HOLE_VIA  4
ZT46  HOLE_VIA  4
ZT44  HOLE_VIA  4
ZT43  HOLE_VIA  4
ZT42  HOLE_VIA  4
ZT40  HOLE_VIA  4
ZT34  HOLE_VIA  4
ZT33  HOLE_VIA  4
ZT32  HOLE_VIA  4