ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

ALL CAPACITANCE VALUES ARE IN MICROFARADS.

ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
PCB SPECS

THICKNESS: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDEANCE: 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1. PREPREG (3MIL)

2. LAMINATE (4MIL)

3. PREPREG (3MIL)

4. LAMINATE (4MIL)

5. PREPREG (3MIL)

6. LAMINATE (2MIL)

7. PREPREG (3MIL)

8. LAMINATE (4MIL)

9. PREPREG (3MIL)

10. LAMINATE (4MIL)

11. PREPREG (3MIL)

12. LAMINATE (4MIL)

SIGNAL (1/3 OZ + COPPER PLATING)
GROUND (1/2 OZ)
SIGNAL (1/2 OZ)
SIGNAL (1/2 OZ)
GROUND (1/2 OZ)
CUT POWER PLANE (1 OZ)
CUT POWER PLANE (1 OZ)
GROUND (1/2 OZ)
SIGNAL (1/2 OZ)
SIGNAL (1/2 OZ)
GROUND (1/2 OZ)
SIGNAL (1/3 OZ + COPPER PLATING)
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
PCI FEEDBACK CLOCK MATCHES LONGEST PCI CLOCK ROUTE

INPUT IMPEDANCE IS ABOUT 20OHM

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

NOTE: Designs using AGP slot should

AGP_PFR_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP

NOTE: Images using AGP slot should use 39 OHM in resistor bars.

AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP

+3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

USB2 AND CH39 REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

AGP PULL-UPS/PULL DOWNS

INT_PCI_FB_OUT

USB2_PCI_REQ_L

CLK33M_CBUS_UF

PCI_FRAME_L

PCI_PAR

PCI_STOP

PCI_TRDY

AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP

NOTE: Designs using AGP slot should use 39 OHM in resistor bars.
1.175V -> 1.025V
1.30V -> 1.10V

GROUNDS SENSE VOLTAGE DIVIDER
This allows us to adjust the ground sense voltage.
U1P = 3.7V, U2P = 3.7V - (R1/R2). See more info in the comments.

NOTE: R101 (R1) do not affect the output value.

When A/B_ is high (fast), D4-00 read as-is
When A/B_ is low (slow), <D1> do not read as-is
><10K-ohm -> 0
100K-ohm -> 1

If all pull-ups are >=10K and all pull-downs are <=1K, V_a = V_b.
### Differential Signals

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS_L0</td>
<td>Low-Voltage Differential Signal</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>LVDS_L1</td>
<td>Low-Voltage Differential Signal</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>LVDS_U0</td>
<td>Low-Voltage Differential Signal</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>LVDS_U1</td>
<td>Low-Voltage Differential Signal</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>LVDS_P0</td>
<td>Low-Voltage Differential Signal</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>LVDS_P1</td>
<td>Low-Voltage Differential Signal</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

#### Internal Layer
- **ER** = 4.3 (Dielectric Constant)
- **W** = 4.0mil (Trace Width)
- **B** = 12.2mil (Dist Between 2 Ground Planes)
- **T** = 0.7mil (Trace Thickness)
- **S** = 10mil (Separation of Diff Traces)
- **Zsingle** = 51.57ohm
- **Zdiff** = 99.85ohm

#### Internal Layer (USB 1.1/2.0)
- **ER** = 4.3 (Dielectric Constant)
- **W** = 4mil (USB 1.1)/ 5mil (USB 2.0) (Trace Width)
- **B** = 12.2mil (Dist Between 2 Ground Planes)
- **T** = 0.7mil (Trace Thickness)
- **S** = 10mil (USB 1.1) (Separation of Diff Traces)
- **Zsingle** = 51.5ohm (USB 1.1)/ 46.2ohm (USB 2.0)
- **Zdiff** = 89.3ohm (USB 1.1)/ 89.4ohm (USB 2.0)

#### Signal Constraints - Page 2

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REVISION HISTORY

189)  changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS
185)  added C688,C690,C846,C905 for thermal pair filtering at fan controller
175)  swapped DN<0> and DP<0> on RP27 for layout
169)  added L16, C304, C327, C647 for filtering GPU VDDR4
162)  added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
159)  changed L30 to 3 pin symbol
156)  CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)
155)  removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
122)  changed FWB connector to new part with extra ground tabs (514S0059)
151)  changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)
149)  changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
146)  changed R321 to 2.49K to set Vcore offset to +25mV
144)  changed inner shield of FWB connector J26 to connect to chassis gnd
136)  add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
134)  removed R331 (CPU Vcore positioning resistor)
127)  added LC filter on SND_CLKOUT for EMI (80 and C899)
126)  added LC filter on SND_SYNC for EMI (L77 and C895)
124)  added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
123)  changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
119)  changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
117)  changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
116)  Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
112)  added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
111)  added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
109)  changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
108)  added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
101)  1 changing all the following: (for U56, U57, R718,R714)
97)  change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
96)  changing all the following: (for U56, U57, R718,R714)
94)  add CHGND4 and SLEEP_LED functional test points
93)  remove FANR_TACH functional test point
92)  change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
90)  no stuff R322 to eliminate 3V_sleep pump up
85)  repinout Sousaphone connector
77)  moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
76)  changed drain/source polarity of Q76 (FET from +BATT to Pbus)
69)  added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
68)  added Q83 and 100K R608 for 1.8V sequencing
67)  added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
65)  added R331 1mohm sense resistor to CPU Vcore
60)  changed D18 to 1N914
59)  added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
57)  changed R416 to 2.2ohms
56)  added Q58, R307, and C515 for GPU Vcore control inverter
55)  changed L30 to 2.2uH Tokin inductor (152S0139)
51)  changed C762 and C766 to 4.7uF 1206 caps
49)  changed C762 and C766 to 4.7uF 1206 caps
44)  move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
42)  add 165 ohm chokes on TMDS data pairs at connector (L, L, , and L)
38)   changed Vcore inductor (L36) to molded core part (152S0125)
37)  add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
33)  change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
29)  update sscg/nosscg stuffing option on intrepid boot straps
27)  added RP27,RP28,RP32, and RP57 for TMDS series termination
26)  added DP7 for M10 power sequencing
25)  updated physical constraints for M10 power nets
19) corrected path to correct for last checkin
16) changed fan controller to ADT7460
12) changed comments to eliminate references to L3 in power supply section
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

*** released for EVT 6/13/03 ***

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