1. ALL RESISTANCE VALUES ARE IN OHMS; 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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SCHEM, MLB, PB17 INCH

01/04/2007

BOM OPTIONS

STUFF

NO STUFF

D3_HOT

/ /

D3_COLD

/ /

GPU_SS

/ /

GPU_SWITCH

/ /

SERIAL_DEBUG

/ /

VCORE_OFFSET

/ /

1_5V_MAXBUS

/ /

1_8V_MAXBUS

/ /

BBANG

/ /

NO_BBANG

/ /

ATI_MEMIO_HI

/ /

ATI_MEMIO_LO

/ /

SSCG

/ /

NO_SSCG

/ /

3V_HD_LOGIC

/ /

5V_HD_LOGIC

/ /

1_5V_MAXBUS

/ /

1_8V_MAXBUS

/ /

3V_HD_LOGIC

/ /

EXT_TMDS

/ /

INT_TMDS

/ /

NO_4VCORE

/ /

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**PCB SPECS**

**THICKNESS**: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

**IMPEDANCE**: 50 OHMS +/- 10%

**DIELECTRIC**: FR-4

**LAYER COUNT**: 12

**SIGNAL TRACE WIDTH**: 4 MILS

**SIGNAL TRACE SPACING**: 4 MILS

**PREPREG THICKNESS**: 2-3 MILS

**SEE PCB CAD FILES FOR MORE SPECIFIC INFO.**

**BOARD STACK-UP AND CONSTRUCTION**

1. **PREPREG (3MIL)**
   - SIGNAL (1/3 OZ + COPPER PLATING)
2. **LAMINATE (4MIL)**
   - GROUND (1/2 OZ)
3. **PREPREG (3MIL)**
   - SIGNAL (1/2 OZ)
4. **LAMINATE (4MIL)**
   - SIGNAL (1/2 OZ)
5. **PREPREG (2MIL)**
   - GROUND (1/2 OZ)
6. **LAMINATE (3MIL)**
   - CUT POWER PLANE (1 OZ)
7. **PREPREG (3MIL)**
   - CUT POWER PLANE (1 OZ)
8. **LAMINATE (4MIL)**
   - GROUND (1/2 OZ)
9. **PREPREG (2MIL)**
   - SIGNAL (1/2 OZ)
10. **PREPREG (3MIL)**
    - SIGNAL (1/2 OZ)
11. **LAMINATE (4MIL)**
    - GROUND (1/2 OZ)
12. **PREPREG (3MIL)**
    - SIGNAL (1/3 OZ + COPPER PLATING)

---

**BOARD HOLES**

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

I/O AREA

INVERTER

SPEAKER CLIPS

GROUND VIAS

**BOARD INFORMATION**

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REV. 051-6582 4 44
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
**HARD DRIVE INTERFACE (UATA100)**

- **EIDE SERIES TERMINATION**
  - Place terminators near Intrepid

- **OPTICAL DRIVE INTERFACE (EIDE)**
  - Place pullup resistors close to Intrepid

- **WIRELESS INTERFACE**
  - Any sequencing requirement between +5V_RD_SLEEP and +5V_SLEEP?

- **BLUE TOOTH/LEFT-SIDE USB**
  - Place pullup resistors close to Intrepid

- **INTERNAL I/O CONNECTORS**
  - Notes of proprietary property

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---

**Optical Drive Interface (EIDE)**

- **EIDE_ADDR<1>**
- **EIDE_DATA<1>**
- **EIDE_DATA<9>**
- **EIDE_DATA<13>**
- **EIDE_DATA<12>**

**Wireless Interface**

- **EIDE_OPTICAL_RST_L**
- **EIDE_OPTICAL_RD_L**
- **EIDE_OPTICAL_INT**
- **EIDE_OPTICAL_DATA<7>**
- **EIDE_OPTICAL_DATA<13>**

**Bluetooth/Left-Side USB**

- **R116**
- **R13**
- **R8**
- **R3**
- **R6**

**Internal I/O Connectors**

- **PCI_AD<3>**
- **PCI_AD<17>**
- **PCI_CBE<2>**
- **PCI_AD<29>**
- **PCI_AD<7>**

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### SIGNAL CONSTRAINTS - PAGE 1

**DIGITAL SIGNALS**

**GROUP 2/3**

- **MAXBUS**
  - RAM_MUXSEL_L
  - RAM_MUXSEL_H
  - RAM_DQS_B<7>
  - RAM_DQS_A<7>
  - RAM_DQM_A<6>
  - RAM_DQS_B<6>
  - RAM_DQM_A<1>
  - RAM_DQS_A<1>
  - RAM_DQM_B<0>
  - CPU_TT<0..4>
  - RAM_CKE<3..0>
  - MEM_DQM<6>
  - MEM_DQM<1>
  - MEM_DQM<0>
  - RAM_DATA_B<63..56>
  - RAM_DATA_A<63..56>
  - RAM_DATA_A<47..32>
  - RAM_RAS_L
  - MEM_RAS_L
  - RAM_WE_L
  - CPU_GBL_L
  - CPU_DBG_L

**STUB_LENGTH**

- **TOTAL LENGTH CONTROLLED BY SPREADSHEET**

**TOTAL LENGTH CONTROLLED BY SPREADSHEET**

**NET_SPACING_TYPE**

- **10 MIL SPACING**

**PULSE_PARAM**

- **167 MHZ**
  - **83 MHZ**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR**

**APPLE COMPUTER INC.**

**INTREPID CRYSTALS**

**SOUND**

**SHOULD BE AT MOST 4 VIAS FOR CLK**
### POWER NET CONSTRAINTS

<table>
<thead>
<tr>
<th>Group</th>
<th>Sig_Name</th>
<th>Voltage</th>
<th>Notes</th>
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<tr>
<td>CPU</td>
<td>DOR RAM INTREF</td>
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<tr>
<td>CPU</td>
<td>INTREF ID PECG</td>
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<td>ADAPTER</td>
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**MIN_LINE_WIDTH**

1. 10
2. 15
3. 20
4. 25
5. 30
6. 35
7. 40
8. 45
9. 50

**MIN_NECK_WIDTH**

1. 5
2. 6
3. 8
4. 10
5. 12
6. 15
7. 20
8. 25

**VOLTAGE**

1. 0V
2. 1.0V
3. 1.2V
4. 1.8V
5. 2.5V
6. 3.3V
7. 4.85V
8. 5V
9. 12.6V

---

**SIGNAL CONSTRAINTS PAGE 3**

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**D 051-6582 C**

**38 44**
**REVISION HISTORY**

**6/19/03**
- Corrected path to correct for last checkin

**5/19/03**
- Integrated M10 pages from Q16 schematic and renumbered them

**3/28/03**
- Added BOM table to define correct part number for M10 without heatspreader (338S0133)

**3/19/03**
- Changed L30 to 2.2uH Tokin inductor (152S0139)
- Changed Pbus inductor (L37) to molded core part (152S0126)
- Added RP27,RP28,RP32, and RP57 for TMDS series termination
- Changed intrepid PLL LDO stuffing back to 1.8V main
- Changed Q58 on pg19 to Q80 to consolidate parts
- Removed D31 between +Batt and 24V_Pbus
- Add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
- Removed Q44 (5V sound sleep fet)
- Changed fan controller to ADT7460
- Added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F
- Added cap on gate of the second FET in Q87 for possible turn on delay (C903)
- Added C688,C690,C846,C905 for thermal pair filtering at fan controller
- Added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
- Changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
- Added C907 to prevent shoot-thru on Q68 (currently NO STUFF’ed)
- Changed C890 to 100pF for improved transient response (Takashi)
- Removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
- Swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
- Added cap on 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
- Changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
- Added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
- Add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
- Integrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
- Changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
- Added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
- Added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
- Changed D29 to B340B (3A part - 371S0159)
- Added LC filter on SND_CLKOUT for EMI (80 and C899)

**6/4/03**
- Changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
- Changed L36 to 1.2uH 18.3A (152S0125)
- Added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs

**5/19/03**
- Added 165 ohm chokes on TMDS data pairs at connector (L ,L , and L )

**5/19/03**
- Changed L30 to 152S0139 (Tokin CPI-1050-2R2) 11A

**6/25/03**
- Changed Fan control nets to FanL and FanR from Fan1 and Fan2

**6/24/03**
- Changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)

**6/19/03**
- Changed L30 to 2.2uH Tokin inductor (152S0139)

**5/19/03**
- Changed L36 to 1.2uH 18.3A (152S0125)

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