Revision Notes

29) changed L1115 to 2.2uH IHLP5050CE (152S0152)
12) moved BS510 to page 18 for syncing with Logic
47) changed all references to SMU_MANUAL_RESET_L to SMU_RESET_L
37) sync with Logic (Q43) to get DVO contraints
31) changed R1102 to 20K 1% 402
6) moved J790 (backup battery/R USB connector) to page 18 for syncing with Logic
2/7/04
2/6/04
2/3/04
2/2/04
42) changed C3676 to 10uF 20% 6.3V to adjust the Tdiode range
19) changed R2150 to 8.25 to reduce LED drive current to 20mA
18) added pg 73 to alias PCI_SB nets back to PCI to reconnect
30) changed C1121 to 680pF 402
49) added BOMOPTION for 2.8V CPU Avdd LDO
21) changed SMU_ADAPTER_ID to SMU_ONEWIRE
34) changed R5019 to 26.7K 1% to increase GPU Vcore current limit (rdar://3510721)
*** sync with Logic ***
14) changed C2150 to 20%
53) changed C8160-C8160 (SATA AC coupling caps) to 0.01uF per Marvell recommendation
52) added R1611 (1k pullup to PP3V3_ALL) on ADAPTER_ID to power SMU_ONEWIRE interface
27) changed C1068 to NO STUFF
3) changed R2191 to pulldown on SYS_LED
7) moved J1600 (BT/USB connector) to page 18 for syncing with Logic
13) moved J2130 (trackpad connector) to page 18 for syncing with Logic
22) added R1620 and R1621 to divide ALS output down to 2.5V
20) changed Q2113 to second FET in Q5909
1/14/04
2/23/04
2/19/04
2/12/04
2/11/04
2/10/04
28) removed Q1117 and C1114
3) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to BKFD_PROT_EN_L
4) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to ALS1_PHOTODIODE and ALS1_OP_IN32
32) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to CPUVCORE_CM_N and CPUVCORE_CS_N
36) added aliases on page 5 to set unused CKE, CS, and MUX controls back to TP
10) moved SP500-SP505 and SP9900 to (speaker wire clips) to page 18 for syncing with Logic
4) moved AGP Vref (R4802,R4803,C4818) circuit to M11 specific page (49)
45) changed L970 to 152S0154 (10uH) to reduce size
25) changed C720 to 0.22uF
43) changed R3677 to 40.2K 0.1% to adjust the Tdiode range
40) changed R3672 to 40.2K 0.1% to adjust the Tdiode range
38) changed R3671 to 100K 0.1% to adjust the Tdiode range
33) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to ALS1_PHOTODIODE and ALS1_OP_IN32
1.8V/1.5V/1.2V MAIN SUPPLIES
NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS reference used by monitoring BOM options provided by this page:

- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU

Caps should connect to GND_SMU.

NOTE: CPU current/voltage monitoring (CPU_VID<2>/CPU_VID<3>) requires 100K/330pF DC filter at SMU pins. Capi should connect to GND_SMU_AVSS. SMU_VPP should be same signal or power supply. If they are not, be sure that this will not affect other analog inputs such as AC adapter ID.

NOTE: Some primary and alternate functions require pull-ups that are not mounted on this page. Refer the latest SMT specification to ensure missing pull-ups are provided on another page.

NOTE: Pull-ups on other pages.
available remote sensor locations.

Power aliases required by this page:
- THERM_x
- THERM_xB
- PP3V_PWRON_THERM

Remote 1
- Place close to Shasta/GPU_Vcore
- Place close to CPU

Remote 2
- Place close to CPU_VCORE

Remote 3
- Place close to U3Lite

Remote 4
- CPU Thermal Sinks

Sensor Selection
Place 2 MAX1989 inputs can connect to two different sensors. These sensors should be close to MAX1989, alternately.

Resistors should be close to MAX1668.

First 3 MAX1668 inputs can connect to the first 3 sensors.
SMU Download / Serial Debug Connector

All debug pins here should be labeled appropriately to allow serial debug flow through without connector.

Debug "Buttons"

Add silkscreen:
- POWER
- RESET

Debug LEDs

Add silkscreen:
- RXD
- TXD
- DTR
- RTS
- SCCA
- RXD (TRXC)
- DTR (DTR#)
- RXD (SCCA)
- RXD (TXD)
Power Sequencing:

- Connect _PPPCI32_PWRON_SB to (NONE).

Power aliases required by this page:
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP2V5_PWRON_SB (to 5V or 3.3V)
- _PPPCI64_PWRON_SB (1.8V)
- _PP2V5_PWRON_SB (1.8V)

NOTE: PCI power uses the VDD supply to meet different drive timing characteristics required by the PCI standard. Power sequencing should be performed as follows:

1. Connect _PPPCI32_PWRON_SB to (NONE).
2. Power VCore rail before any other Shasta supplies.

Signal aliases required by this page:

Page Notes

Power sequencing:
- Must power Shasta VCore rail before any other Shasta supplies.
CPU Current Monitoring
Place close to CPU Power Supply

CPU Thermal Diode Circuit
Place close to CPU

CPU Voltage Monitoring
Place close to CPU

SMU Voltage Reference
Place close to SMU

CPU Temp Monitoring

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil

MIN_NECK_WIDTH=10 mil
MIN_LINE_WIDTH=10 mil
When GPUVCORE_CNTL_L = 0, Vout = 1.2V
Vout = 2V \times \left( \frac{R2}{R1+R2} \right) = 1.0V
When GPUVCORE_CNTL_L = 1, Vout = 1.0V

\text{R5050} \text{ from } 30.1K \text{ to } 37.4K

\text{R5004} \text{ to the high input}
Page Notes

Signal all names required by this page: 40

Not options provided by this page:

One Output Type: LVDS

Due to Clear: 6 mils

Length Tolerance: 3 mils

Primary Max Sep: 104 mils

Secondary Length: 225 mils

NOTE: Target differential impedance for 100 data pairs is 100 ohms.
NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM BOM options provided by this page:

- _PP3V3_PCI
- Power aliases required by this page:
PCI Devices implemented on this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

Signal aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Power aliases required by this page:
- CLOCKSPCI_CLK_USB2 _PCI_CLK33M_USB2

- RP7702
- RP7703
- SM1

- NEC_uPD720101_USB2

- 0.1uF
- CRITICAL
- FBGA
- VDD_PCI
- C8
- FBGA
- M4

- IPD
- IPD
- IPD

- TP_NEC_SRMOD
- TP_NEC_NANDTEST
- TP_NEC_TEST
- TP_NEC_AMC
- TP_NEC_SMC
- TP_NEC_NTEST1

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NOTE: This CardBus implementation does not provide 1.8V or 3.3V support.

Power Sequencing:
1. Assert RESET
2. _PPVIO_PCI
3. _PP2V5_PCI
4. _PP3V3_PCI
5. _PP5V_CBUS
6. _PPVPP_CBUS

Signal aliases required by this page:
- _PP2V5_PCI
- _PP3V3_PCI
- _PP5V_CBUS
- _PPVPP_CBUS

This CardBus implementation does not provide 1.8V or 3.3V support.

PC Card Power Switch

Make sure Vcc and Vpp are wide plane/traces to minimize inductance!

PC Card/CardBus Connector

CardBus Interface

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**Page Notes**

Power aliases required by this page:

- PATA_DEV_R
- PATA_DMARQ
- PATA_DD7
- PATA_DD<7>

Signal aliases required by this page:

- _PP1V8_SATABR
- _PP3V3_SATABR
- _PP1V8_SATABR
- _PP3V3_SATABR

**BRAD000 Config Straps (Device Mode):**

- 00 - Disable SATA Spread Spectrum Clocking
- 01 - 10 MHz
- 10 - 11 MHz (default)
- T<1..0> - VU Type
- R - Internal Pull-up
- W - Internal Pull-down

**Page Numbers:**

- SATA_1_BRIDGE (/ SATA_1_CONN)
- (NONE)

**Signal Connections:**

- SATA_1_BRIDGE
- SATA_1_CONN
- PATA
- SATA

**Page Numbers:**

- PATA_DEV_R
- PATA_DMARQ
- PATA_DD7
- PATA_DD<7>

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR
- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
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**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
- C8151
- C8152
- C8153
- C8154
- C8155
- C8156
- C8157
- C8158

**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

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**Notes:**

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- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

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- SATA_SATA_BR_RXD_PSATA_BR_RXD

**Master: Link**

**Serial ATA Bridge**

- C8150
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**Notes:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Signal Connections:**

- _PP1V8_SATABR
- _PP3V3_SATABR

**Notes:**

- SATA_SATA_BR_TXD_PSATA_BR_TXD
- SATA_SATA_BR_RXD_PSATA_BR_RXD
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Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM

Signal aliases required by this page:

BOM options provided by this page:

Signal aliases required by this page:

Supports both The Last Dash and Q52 Modems

Removed 10uF bulk cap because modem connector is close
to 5V power supply output caps

Modem Interface

APPEND PAGE

PP3V3_PWRON_MODEM

_PP5V_PWRON_MODEM

USB_MODEM_P

I2S1_RESET_L

UDASH_SDOWN

I2C_MODEM_SDA

_MODEM_RING2SYS_L

I2S1_MCLK

I2S1_SYNC

I2S1_BITCLK

I2S1_DEV_TO_SB_DTI

I2S1_SB_TO_DEV_DTO

Modem Connector

Supports both The Last Dash and Q52 Models

Removed 10uF bulk cap because modem connector is close
to 5V power supply output caps

Preliminary
E.M.I. Filtering

Audio Interface

Audio GPIO Pull-ups & Pull-downs

---

EMI Filtering

Sound Board Connector

Place shorts at 3.3V and 5V regulators

Place ground short near 3.3V and 5V regulators

---

Audio Interface

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5 103
### Electrical Constraints

No series termination on PCI signals

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