1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		397477	PRODUCTION RELEASED	08/31/05	?

SCHEM,MLB,PB15

Mon Aug 29 19:19:29 2005

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6888	1	SCHEM,MLB,PB15	SCH1	
820-1441	1	PCBF,MLB,PB15	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	EEE:T9Q	DMS630-7112
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	EEE:T9R	DMS630-7113

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,MLB,PB15"

DRAWING NUMBER 051-6888 REV. B

SHT 1 OF 40

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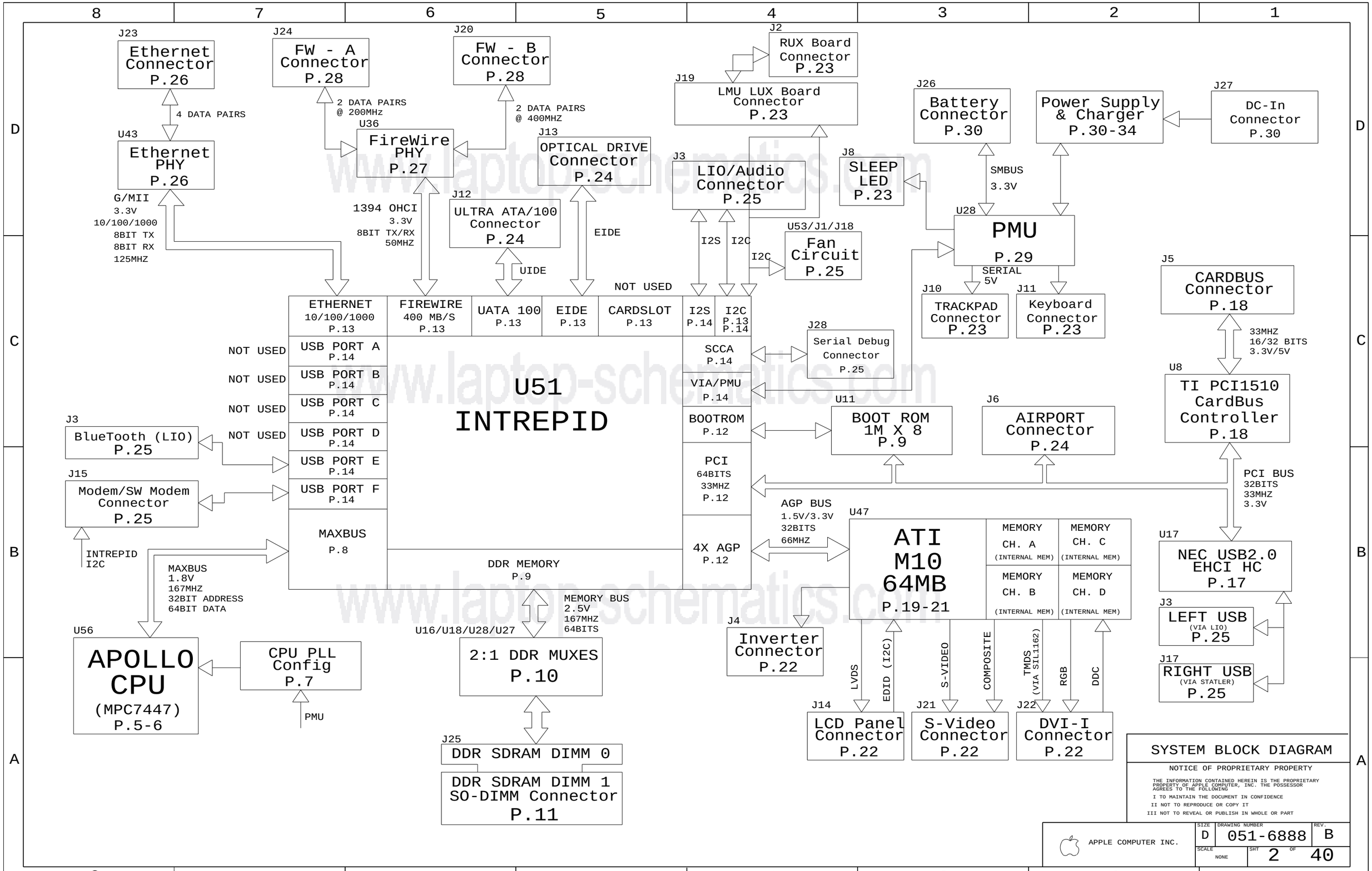
J23
Ethernet Connector P.26
4 DATA PAIRS
U43
Ethernet PHY P.26
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
J24
FW - A Connector P.28
2 DATA PAIRS @ 200MHz
U36
FireWire PHY P.27
1394 OHCI
3.3V
8BIT TX/RX
50MHZ
J20
FW - B Connector P.28
2 DATA PAIRS @ 400MHZ
J13
OPTICAL DRIVE Connector P.24
EIDE
J12
ULTRA ATA/100 Connector P.24
UIDE
J2
RUX Board Connector P.23
J19
LMU LUX Board Connector P.23
J3
LIO/Audio Connector P.25
I2S
I2C
I2C
U53/J1/J18
Fan Circuit P.25
J8
SLEEP LED P.23
J26
Battery Connector P.30
Power Supply & Charger P.30-34
J27
DC-In Connector P.30
SMBUS
3.3V
U28
PMU P.29
SERIAL
5V
J10
TRACKPAD Connector P.23
J11
Keyboard Connector P.23
NOT USED
ETHERNET 10/100/1000 P.13
FIREWIRE 400 MB/S P.13
UATA 100 P.13
EIDE P.13
CARDSLOT P.13
I2S P.14
I2C P.13 P.14
NOT USED
USB PORT A P.14
NOT USED
USB PORT B P.14
NOT USED
USB PORT C P.14
NOT USED
USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8
U51
INTREPID
SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12
J28
Serial Debug Connector P.25
U11
BOOT ROM 1M X 8 P.9
J6
AIRPORT Connector P.24
J5
CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U8
TI PCI1510 CardBus Controller P.18
PCI BUS
32BITS
33MHZ
3.3V
J3
BlueTooth (LIO) P.25
J15
Modem/SW Modem Connector P.25
INTREPID
I2C
MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
DDR MEMORY P.9
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27
2:1 DDR MUXES P.10
J25
DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11
U56
APOLLO CPU
(MPC7447)
P.5-6
CPU PLL Config P.7
PMU
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47
ATI M10 64MB P.19-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
J4
Inverter Connector P.22
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14
LCD Panel Connector P.22
J21
S-Video Connector P.22
J22
DVI-I Connector P.22
U17
NEC USB2.0 EHCI HC P.17
J3
LEFT USB (VIA LIO) P.25
J17
RIGHT USB (VIA STATLER) P.25
SYSTEM BLOCK DIAGRAM
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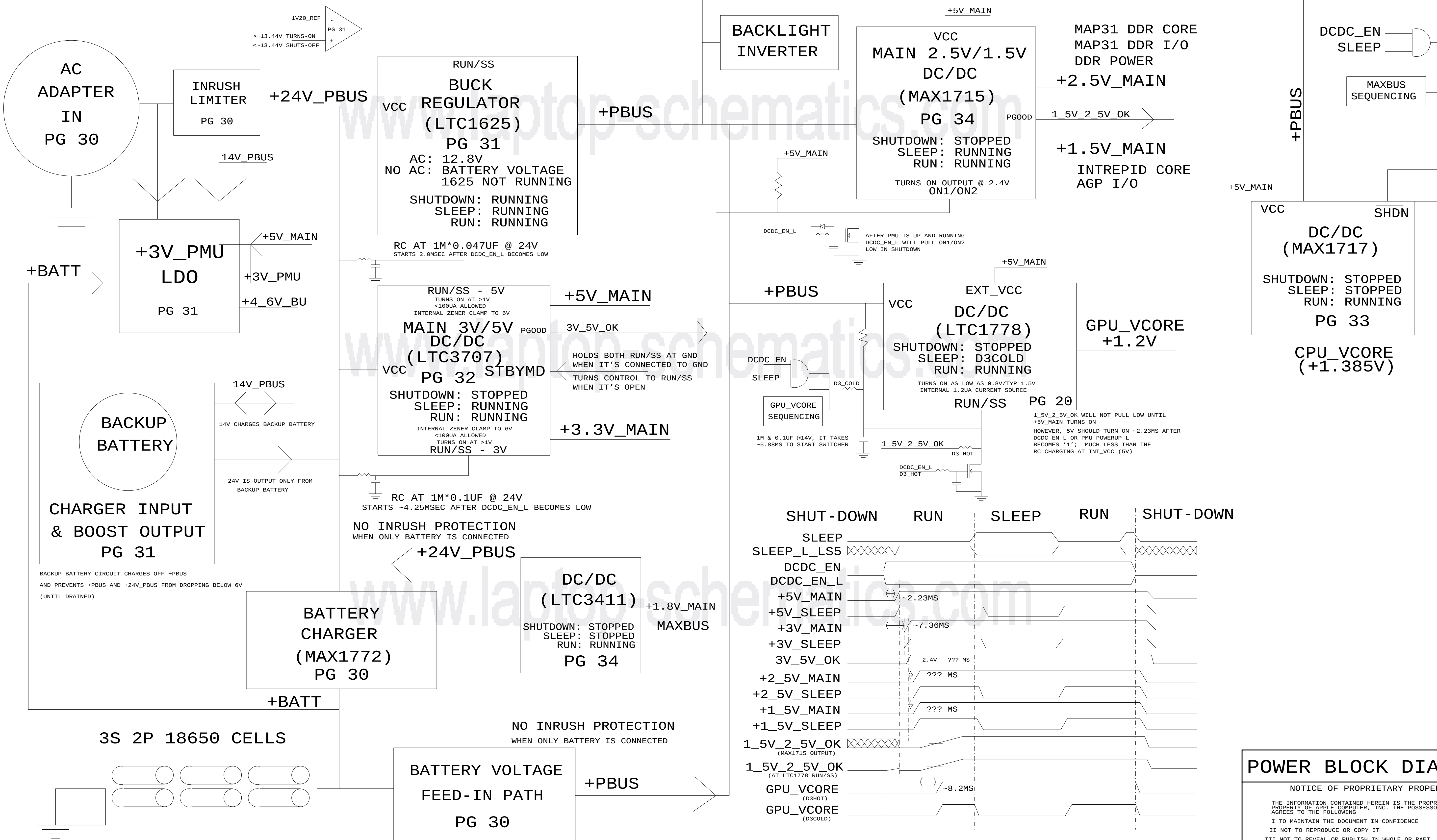
SIZE D
DRAWING NUMBER 051-6888
REV. B
SCALE NONE
SHT 2 OF 40

POWER SYSTEM ARCHITECTURE


8 7 6 5 4 3 2 1
D C B A
AC ADAPTER IN PG 30
INRUSH LIMITER PG 30
+24V_PBUS
1V20_REF
PG 31
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF
RUN/SS
VCC
BUCK REGULATOR (LTC1625) PG 31
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING
+PBUS
14V_PBUS
+3V_PMU LDO PG 31
+5V_MAIN
+3V_PMU
+4_6V_BU
+BATT
RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW
RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 32
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V
+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND
WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS
WHEN IT'S OPEN
+3.3V_MAIN
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 31
14V_PBUS
14V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)
RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS
BATTERY CHARGER (MAX1772) PG 30
+BATT
DC/DC (LTC3411)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 34
+1.8V_MAIN
MAXBUS
3S 2P 18650 CELLS
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 30
+PBUS
BACKLIGHT INVERTER
+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V
ON1/ON2
MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O
+5V_MAIN
DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN
+PBUS
+5V_MAIN
EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
PG 20
GPU_VCORE
+1.2V
DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES
~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL
+5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER
DCDC_EN_L OR PMU_POWERUP_L
BECOMES '1'; MUCH LESS THAN THE
RC CHARGING AT INT_VCC (5V)
+PBUS
DCDC_EN
SLEEP
MAXBUS SEQUENCING
+5V_MAIN
VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33
CPU_VCORE
(+1.385V)
SHUT-DOWN
RUN
SLEEP
RUN
SHUT-DOWN
SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN
~2.23MS
+5V_SLEEP
+3V_MAIN
~7.36MS
+3V_SLEEP
3V_5V_OK
2.4V - ??? MS
+2_5V_MAIN
??? MS
+2_5V_SLEEP
+1_5V_MAIN
??? MS
+1_5V_SLEEP
1_5V_2_5V_OK
(MAX1715 OUTPUT)
1_5V_2_5V_OK
(AT LTC1778 RUN/SS)
GPU_VCORE
(D3HOT)
~8.2MS
GPU_VCORE
(D3COLD)

POWER BLOCK DIAGRAM

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	SCALE NONE	SHT 3 OF 40	

PCB SPECS

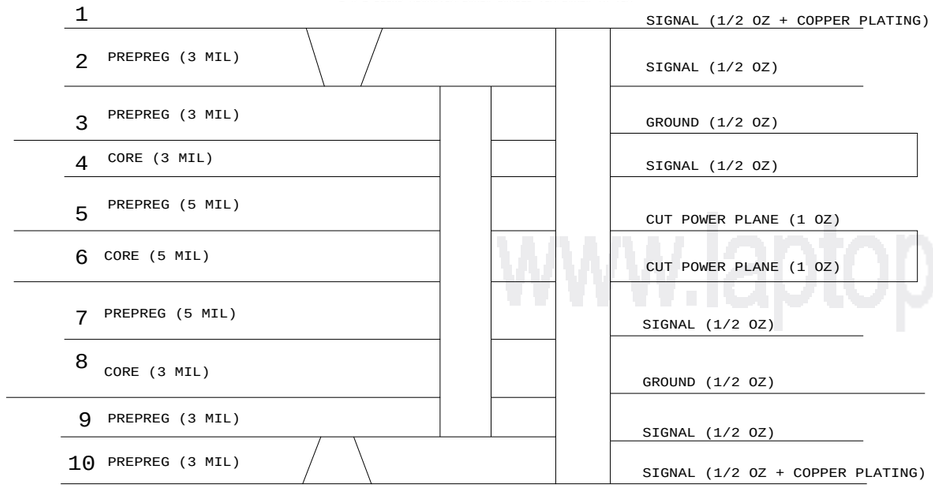
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER

SH1 OG-503040 SHLD-SM — CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301_SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302_SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10_SPN NO_TEST=TRUE

GROUND VIAS

ZT76, ZT28, ZT72, ZT69, ZT68, ZT64, ZT61, ZT38, ZT39, ZT40, ZT41, ZT46, ZT71, ZT78, ZT80 — HOLE-VIA-20R10

ZT50, ZT51, ZT52, ZT53, ZT57, ZT60, ZT82, ZT22, ZT17, ZT35, ZT45, ZT79, ZT81, ZT83, ZT49 — HOLE-VIA-20R10

ZT48, ZT47, ZT54, ZT55, ZT56, ZT84, ZT5, ZT15, ZT44, ZT4, ZT8, ZT6, ZT32, ZT3, ZT10 — HOLE-VIA-20R10

ZT11, ZT34, ZT20, ZT43, ZT70, ZT2, ZT9, ZT75, ZT73, ZT63, ZT77, ZT66, ZT62, ZT65, ZT13 — HOLE-VIA-20R10

ZT25, ZT19, ZT24, ZT67, ZT37, ZT29, ZT31, ZT1, ZT14, ZT12, ZT27, ZT26, ZT30, ZT33, ZT18 — HOLE-VIA-20R10

BOARD INFORMATION

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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 4 OF 40	

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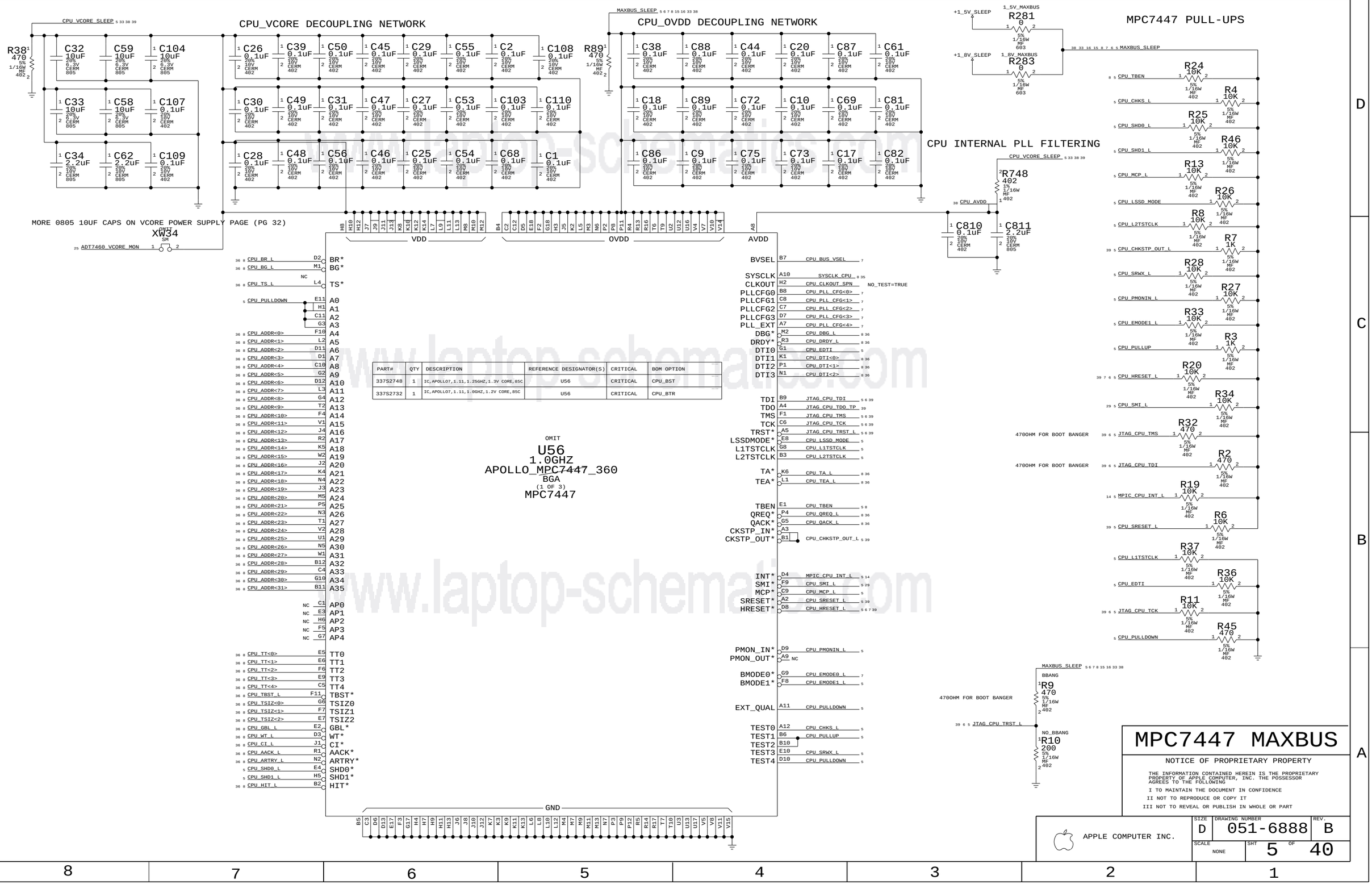

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2748	1	IC,APOLLO7,1.11,1.25GHZ,1.3V CORE,85C	U56	CRITICAL	CPU_BST
337S2732	1	IC,APOLLO7,1.11,1.0GHZ,1.2V CORE,85C	U56	CRITICAL	CPU_BTR

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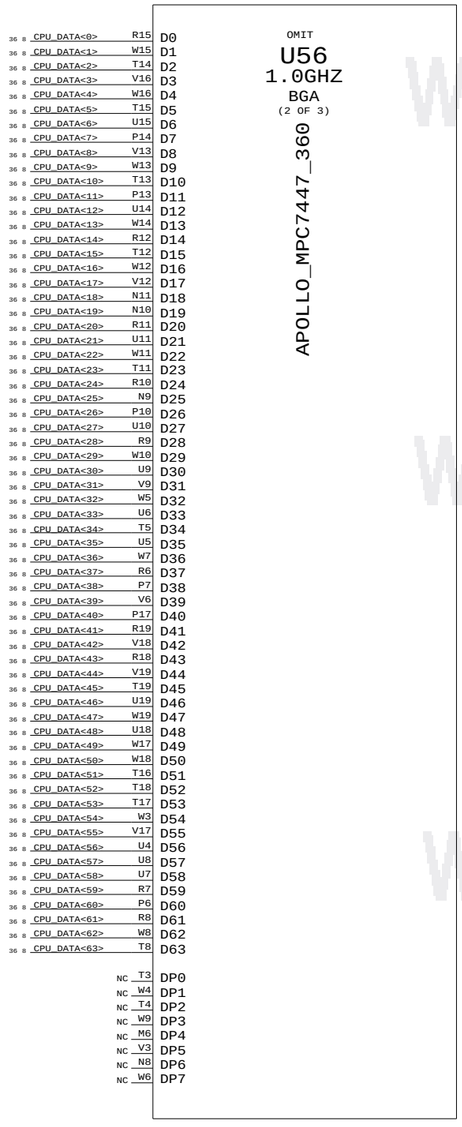
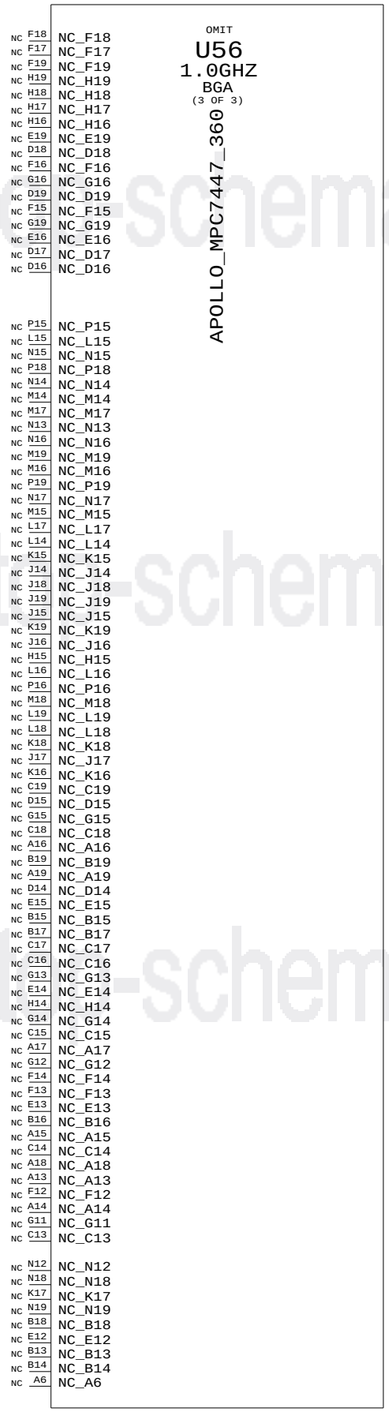
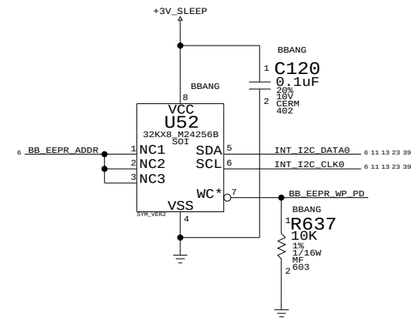
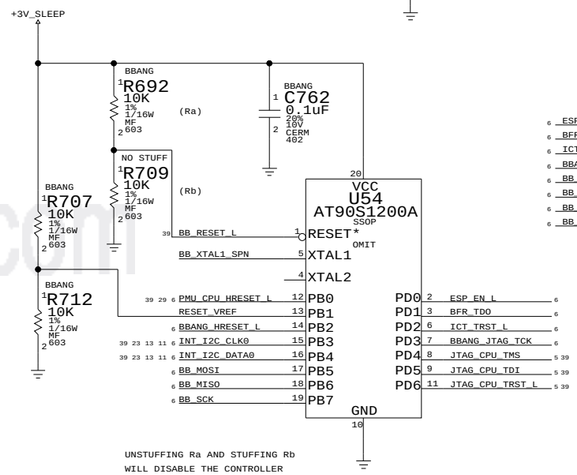
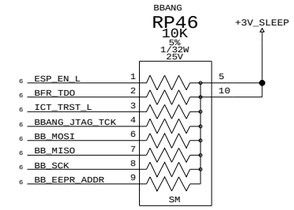
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON





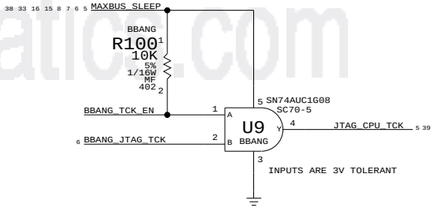


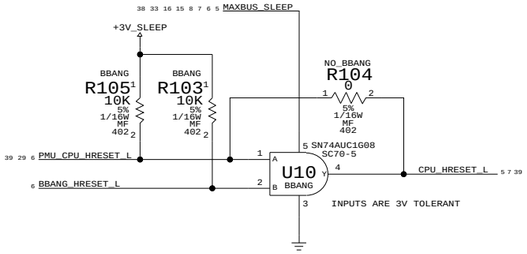




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	089-6240 FW GT4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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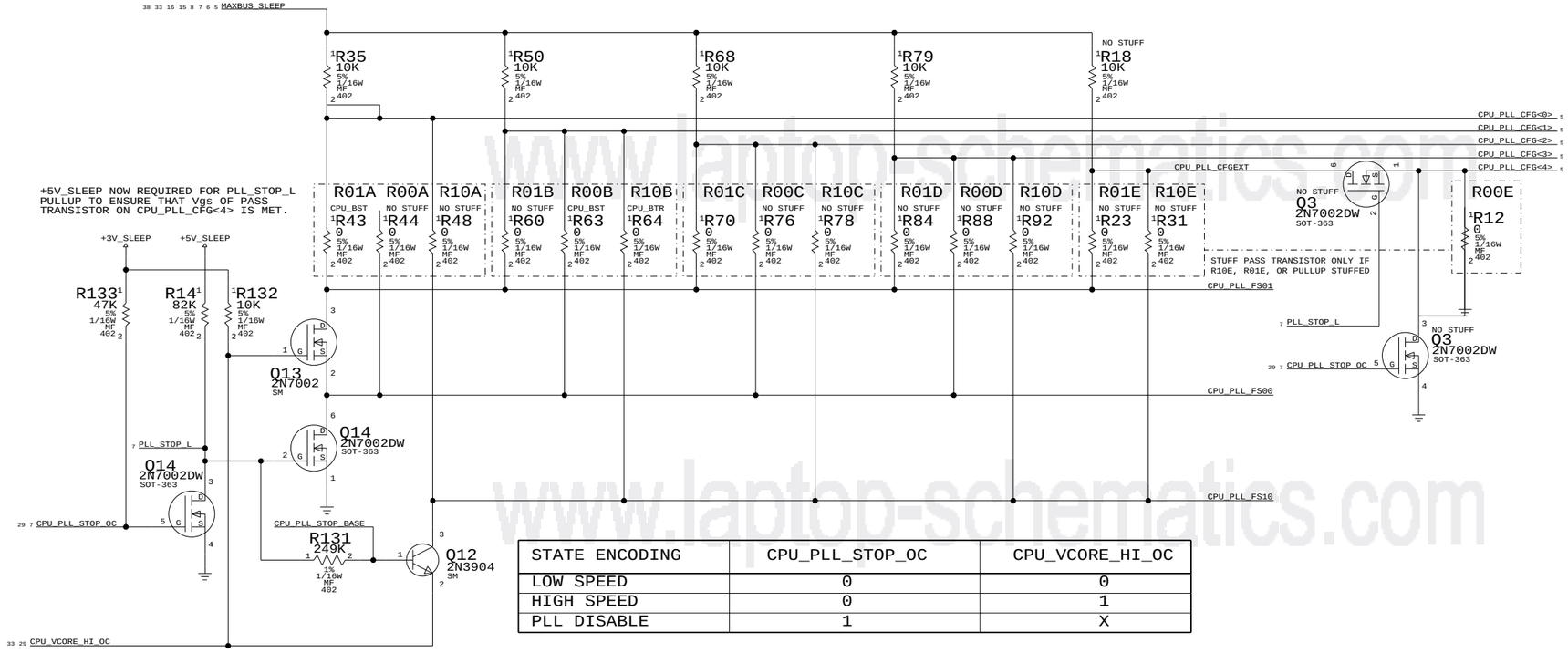
SIZE	DRAWING NUMBER	REV.
D	051-6888	B

SCALE	SHT	OF
NONE	6	40

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

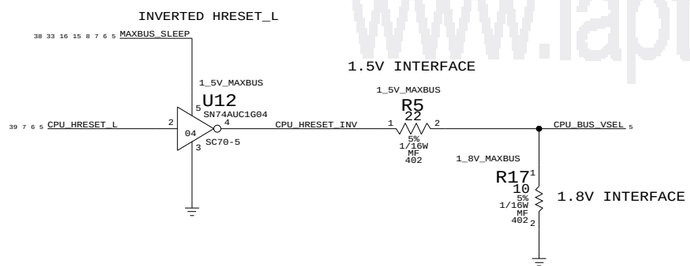
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4	0123	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

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CPU CONFIGURATION

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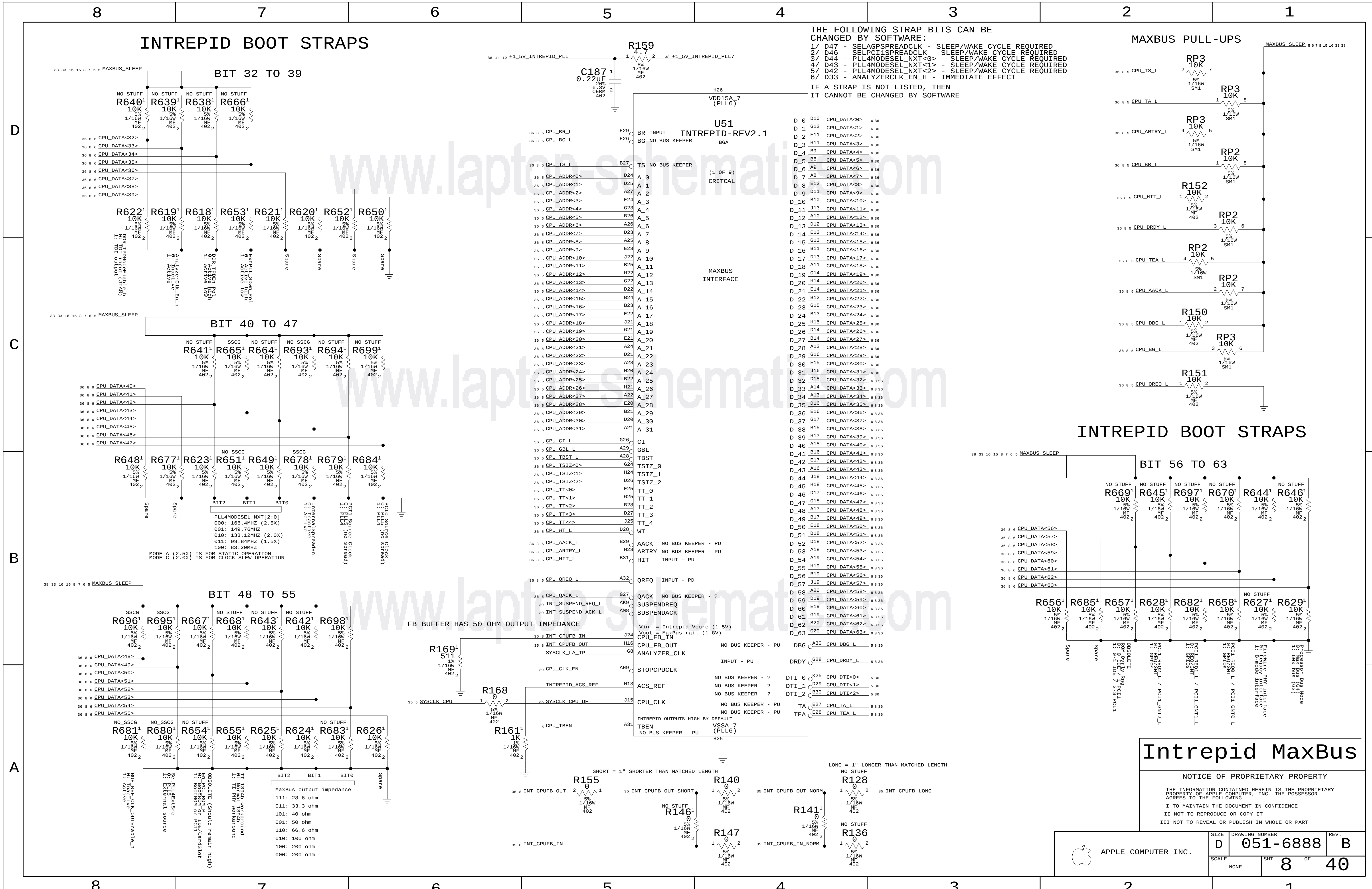
INTREPID BOOT STRAPS
BIT 32 TO 39
BIT 40 TO 47
BIT 48 TO 55
BIT 56 TO 63
MAXBUS PULL-UPS
THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT
IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE
U51
INTREPID-REV2.1
BGA
(1 OF 9)
CRITCAL
MAXBUS INTERFACE
VDD15A_7 (PLL6)
VSSA_7 (PLL6)
FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE
Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)
INTREPID OUTPUTS HIGH BY DEFAULT
PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ
MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION
MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm
SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH
Intrepid MaxBus
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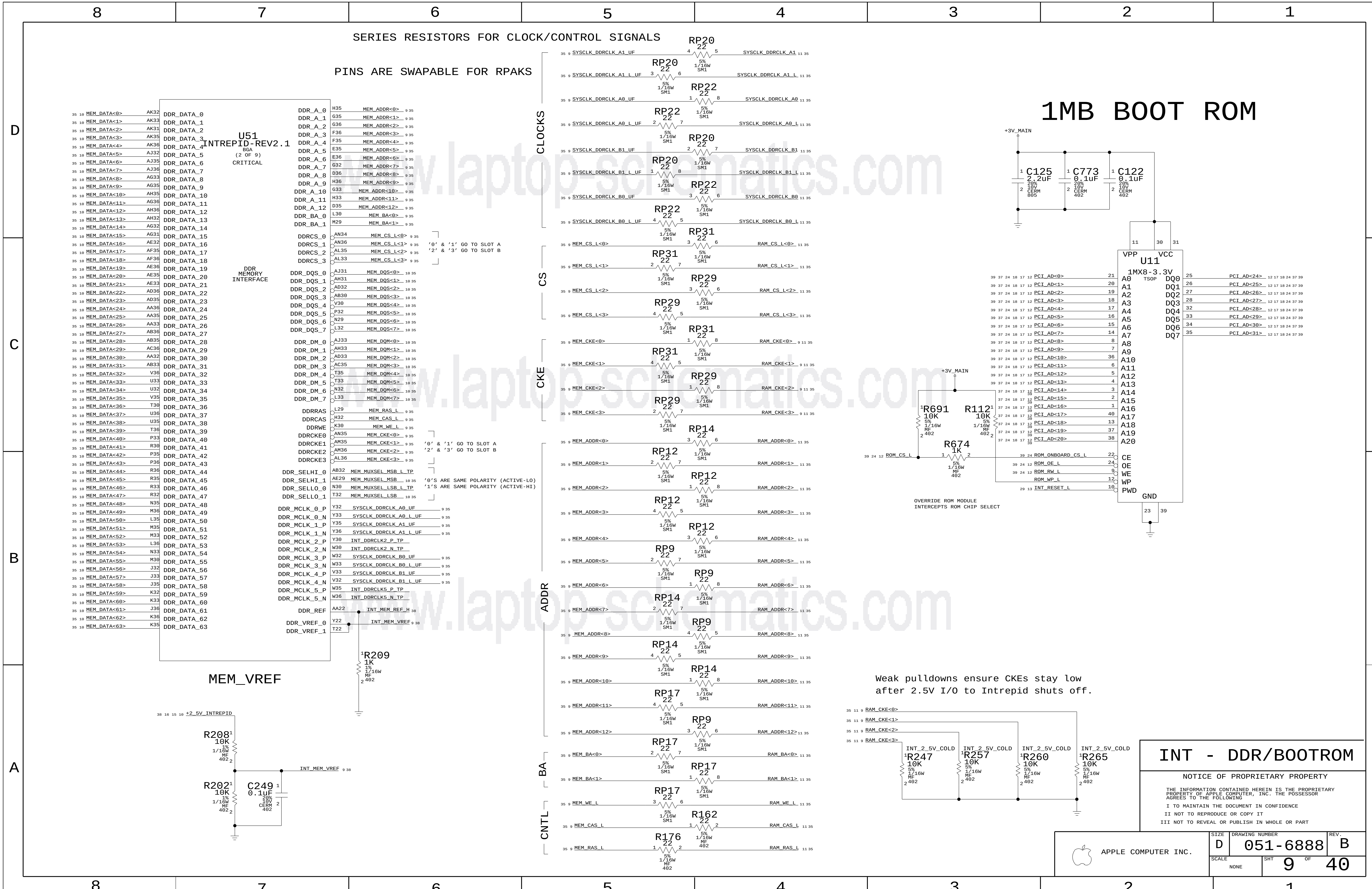
SIZE D
DRAWING NUMBER 051-6888
REV. B
SCALE NONE
SHT 8 OF 40


SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS
PINS ARE SWAPABLE FOR RPAKS
U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL
DDR
MEMORY
INTERFACE
MEM_VREF
CLOCKS
CS
CKE
ADDR
BA
CNTL
'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B
'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)
1MB BOOT ROM
+3V_MAIN
C125 2.2uF
C773 0.1uF
C122 0.1uF
U11
1MX8-3.3V
TSOP
R691 10K
R112 10K
R674 1K
ROM_CS_L
ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L
OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT
R209 1K
+2_5V_INTREPID
R208 10K
R202 10K
C249 0.1uF
INT_MEM_VREF
Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.
INT_2_5V_COLD
R247 10K
R257 10K
R260 10K
R265 10K
INT - DDR/BOOTROM
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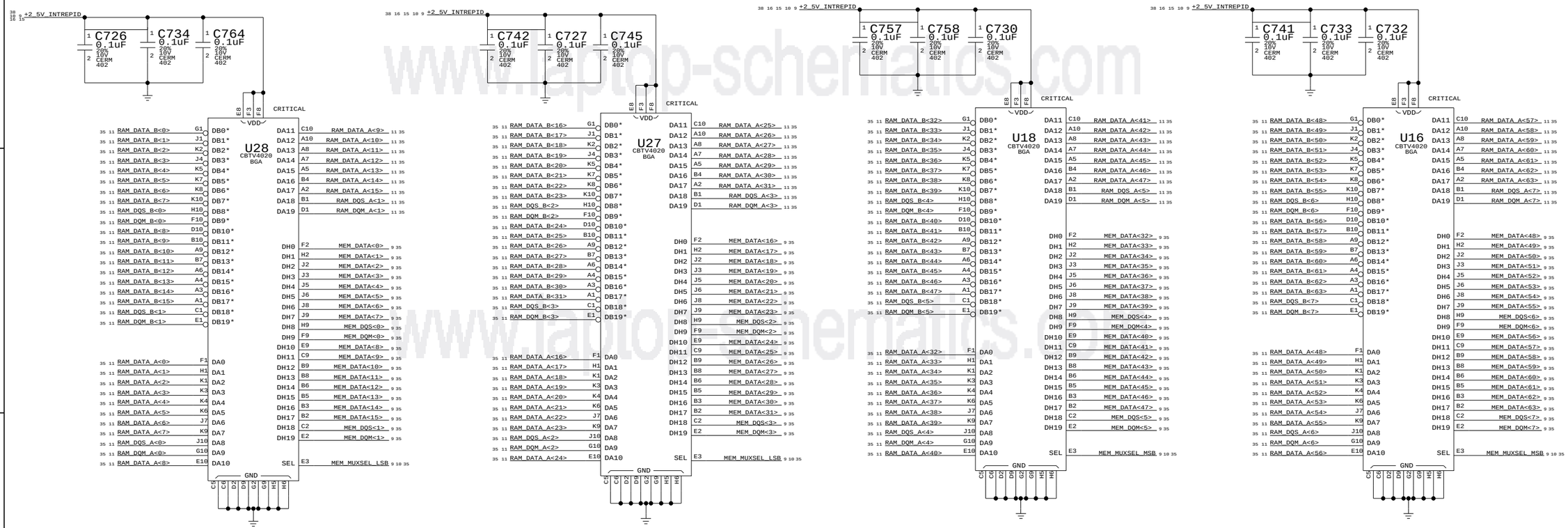
SHT 9 OF 40



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

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16BIT 2:1 DDR MUXES

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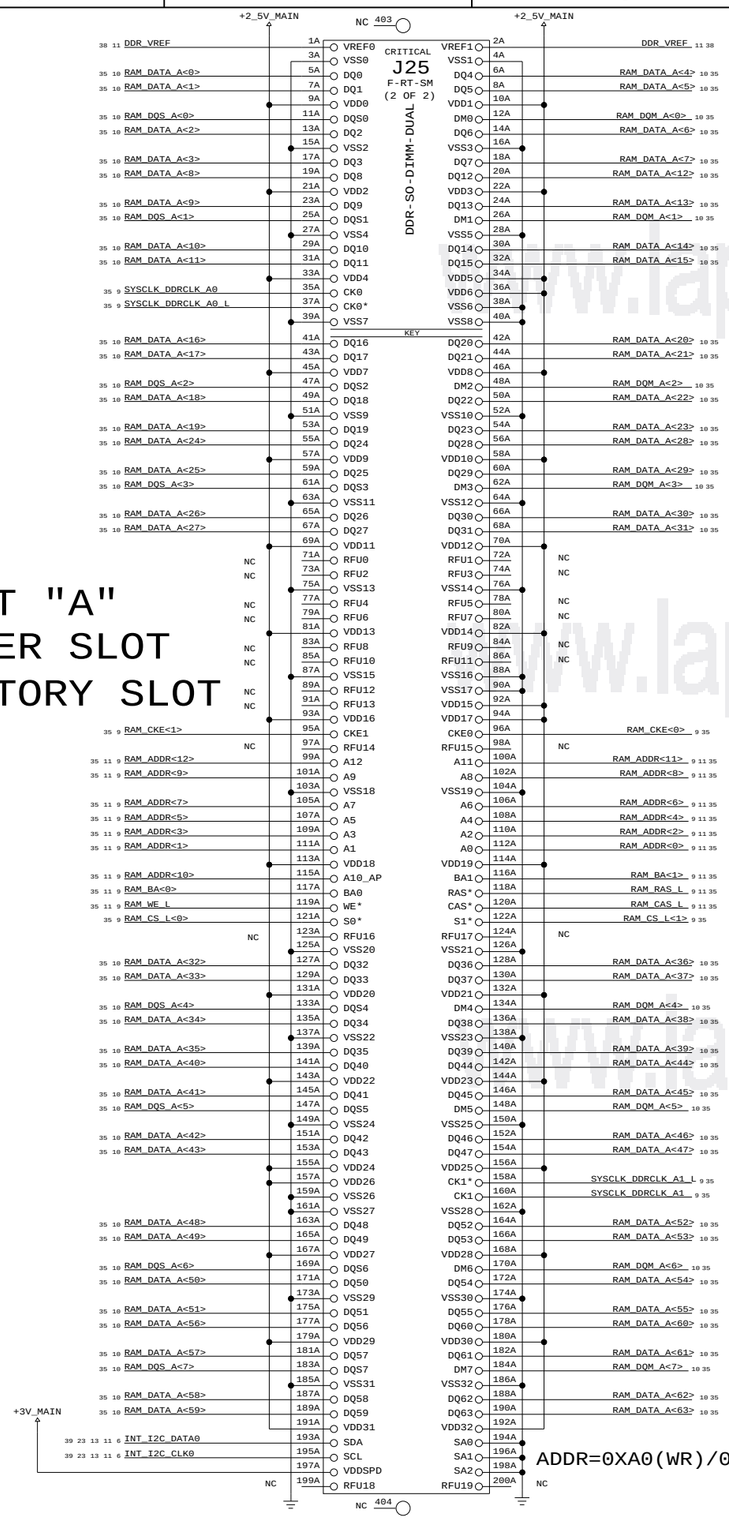
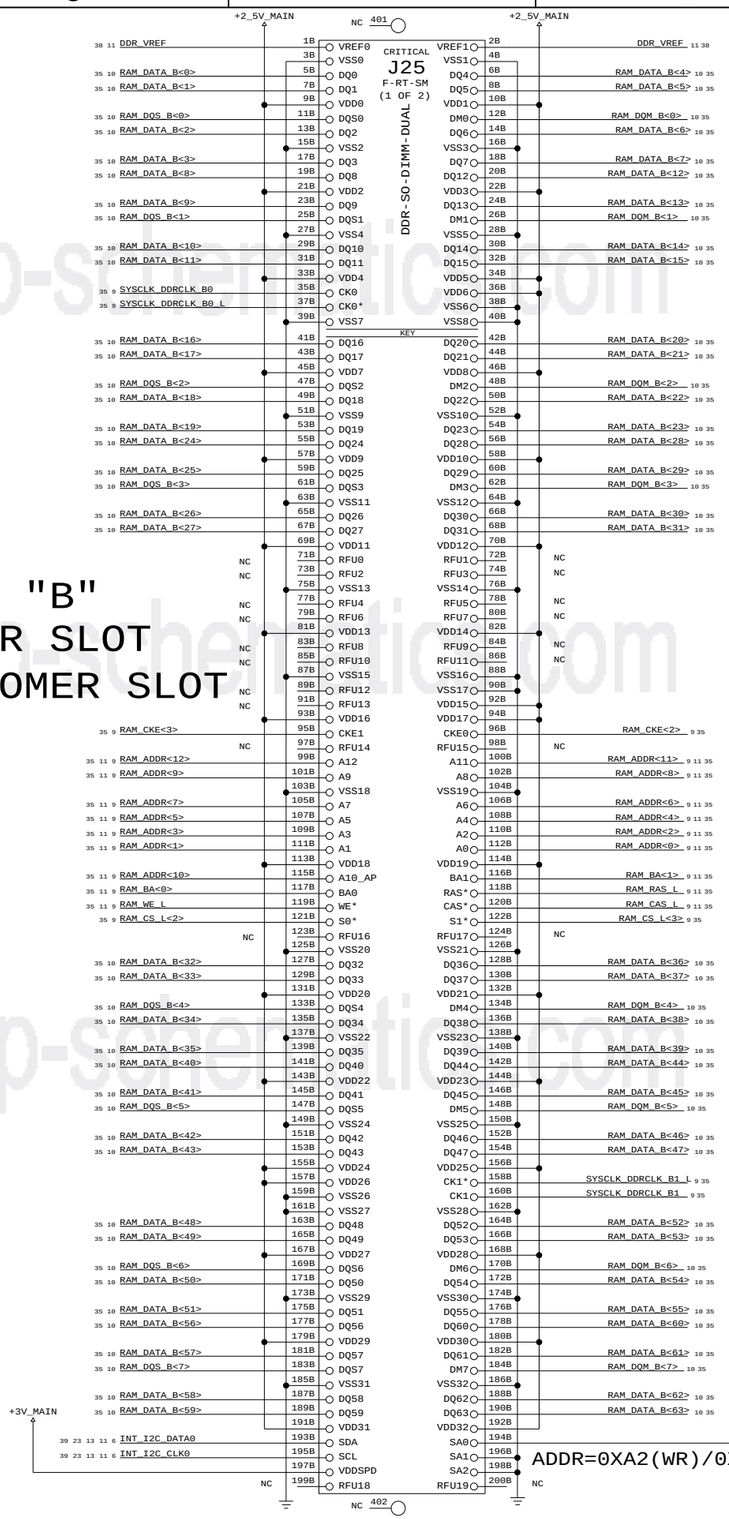
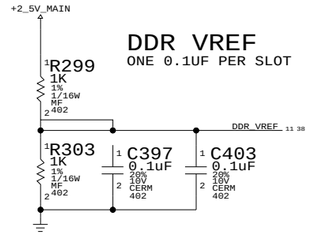
SIZE	DRAWING NUMBER	REV.
D	051-6888	B

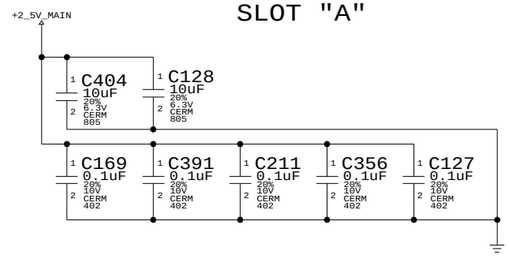
SCALE	SHT	OF
NONE	10	40

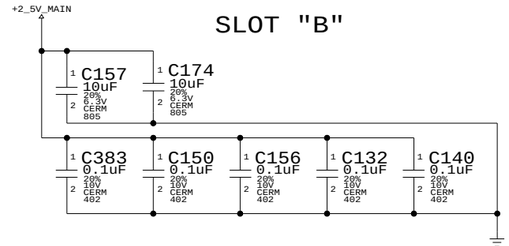




NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting







DDR SODIMM CONNS

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SCALE: NONE	SHT 11 OF 40	

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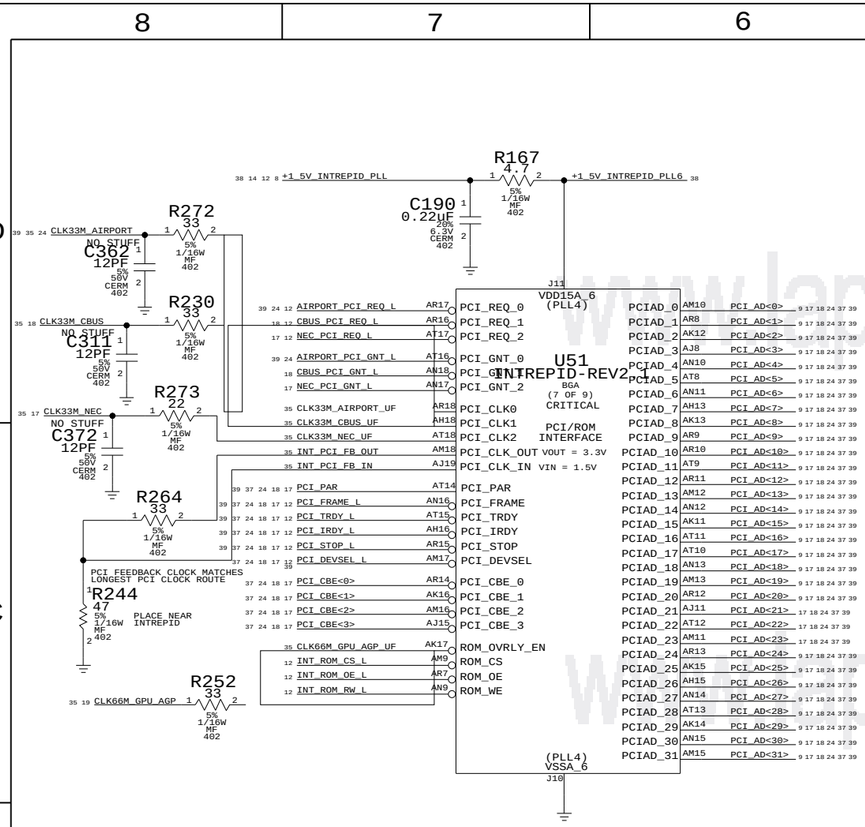

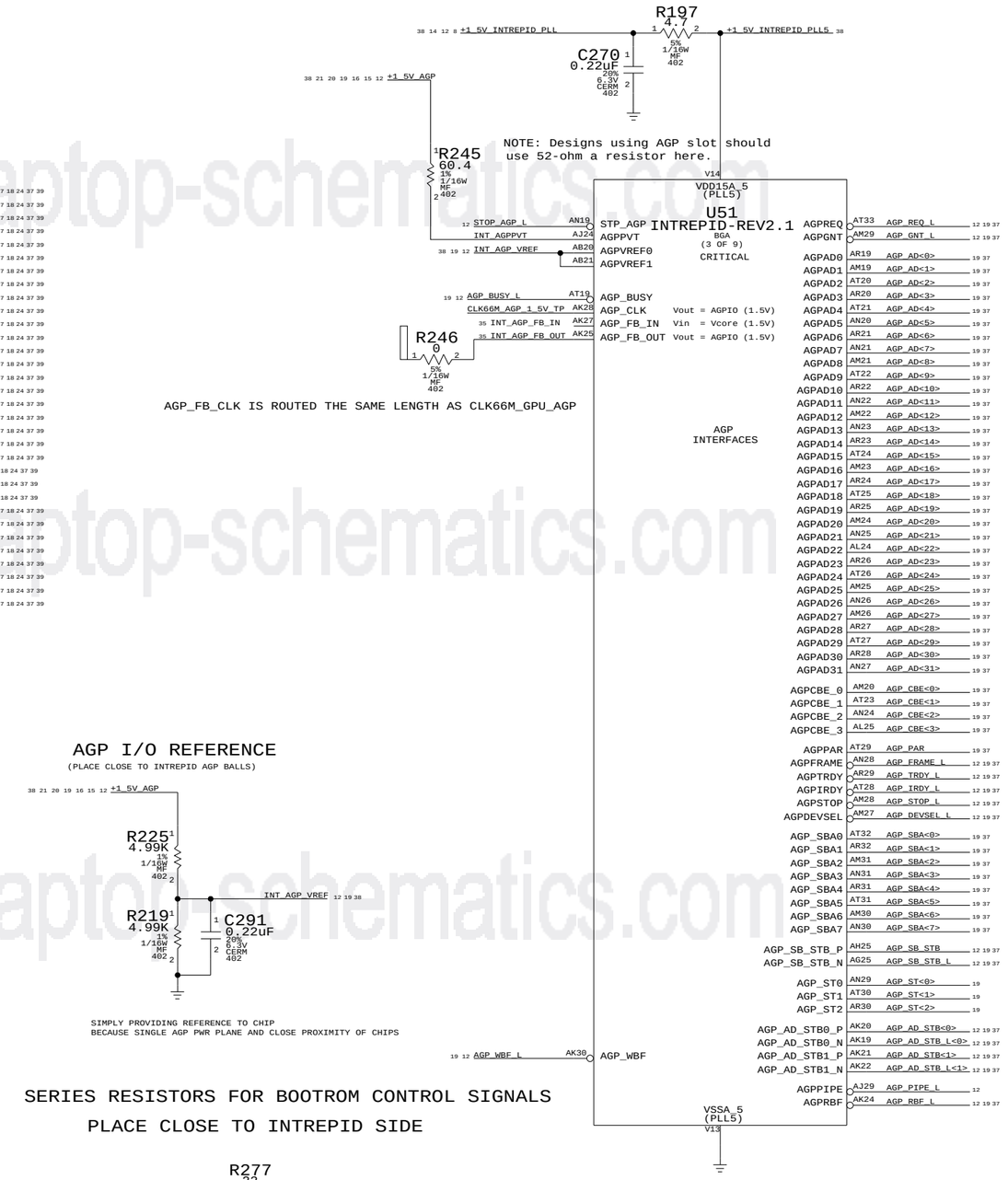

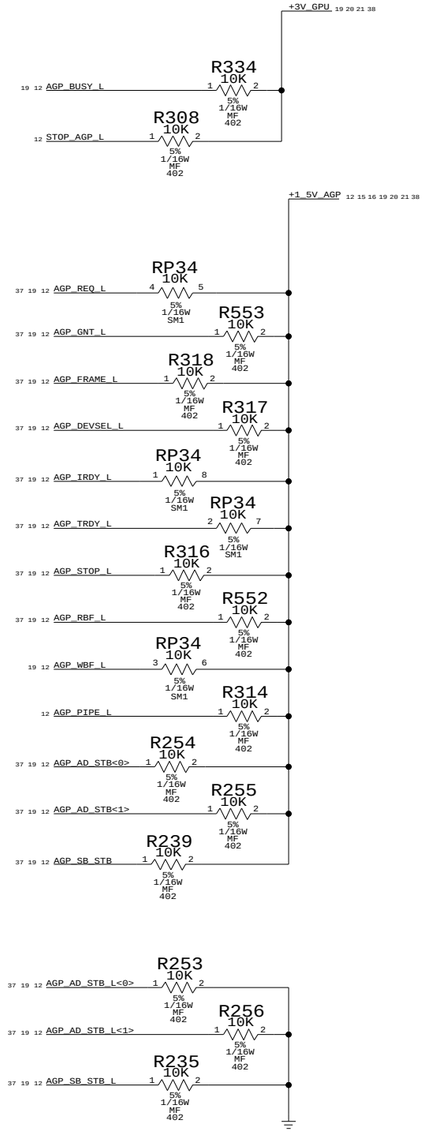

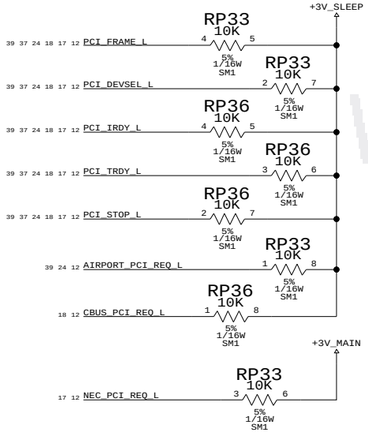

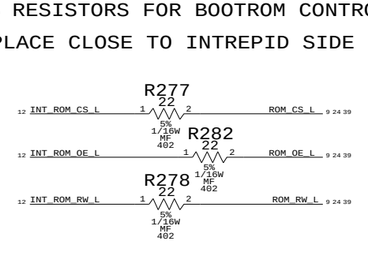

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INTREPID AGP/PCI

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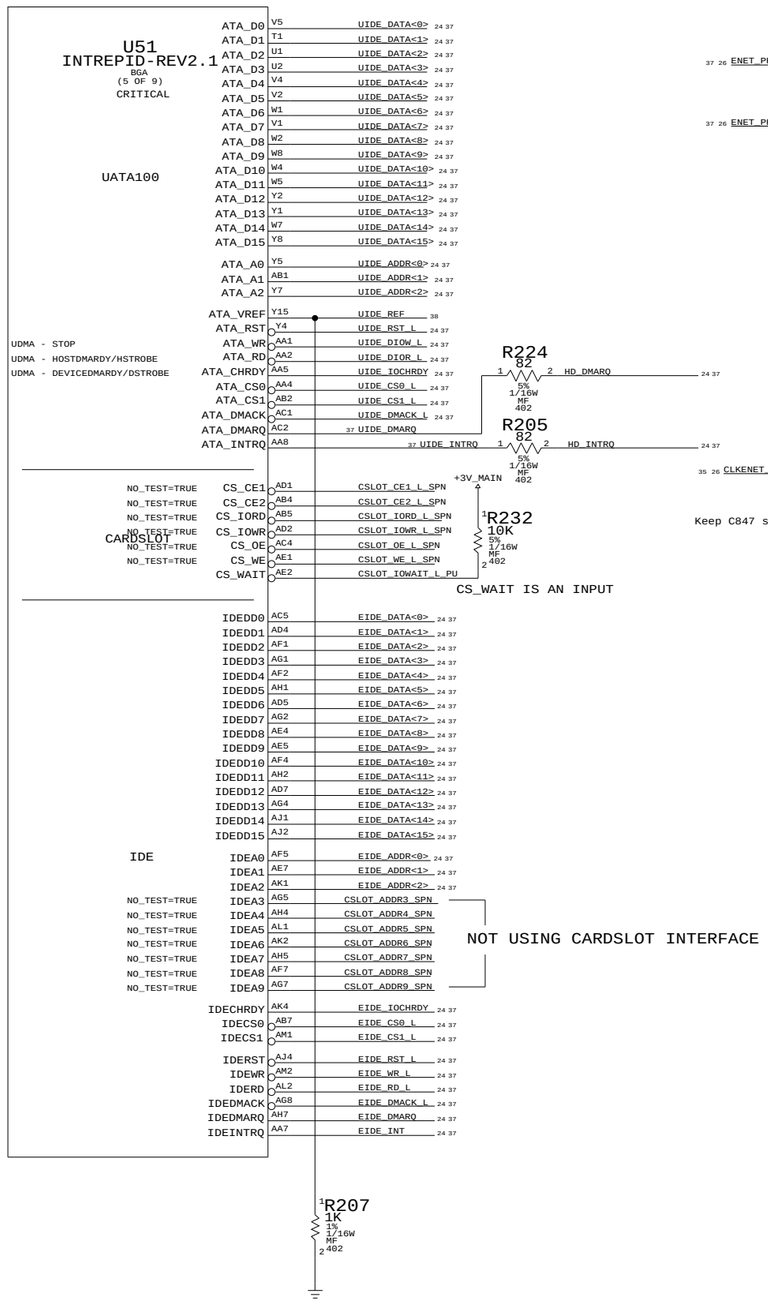
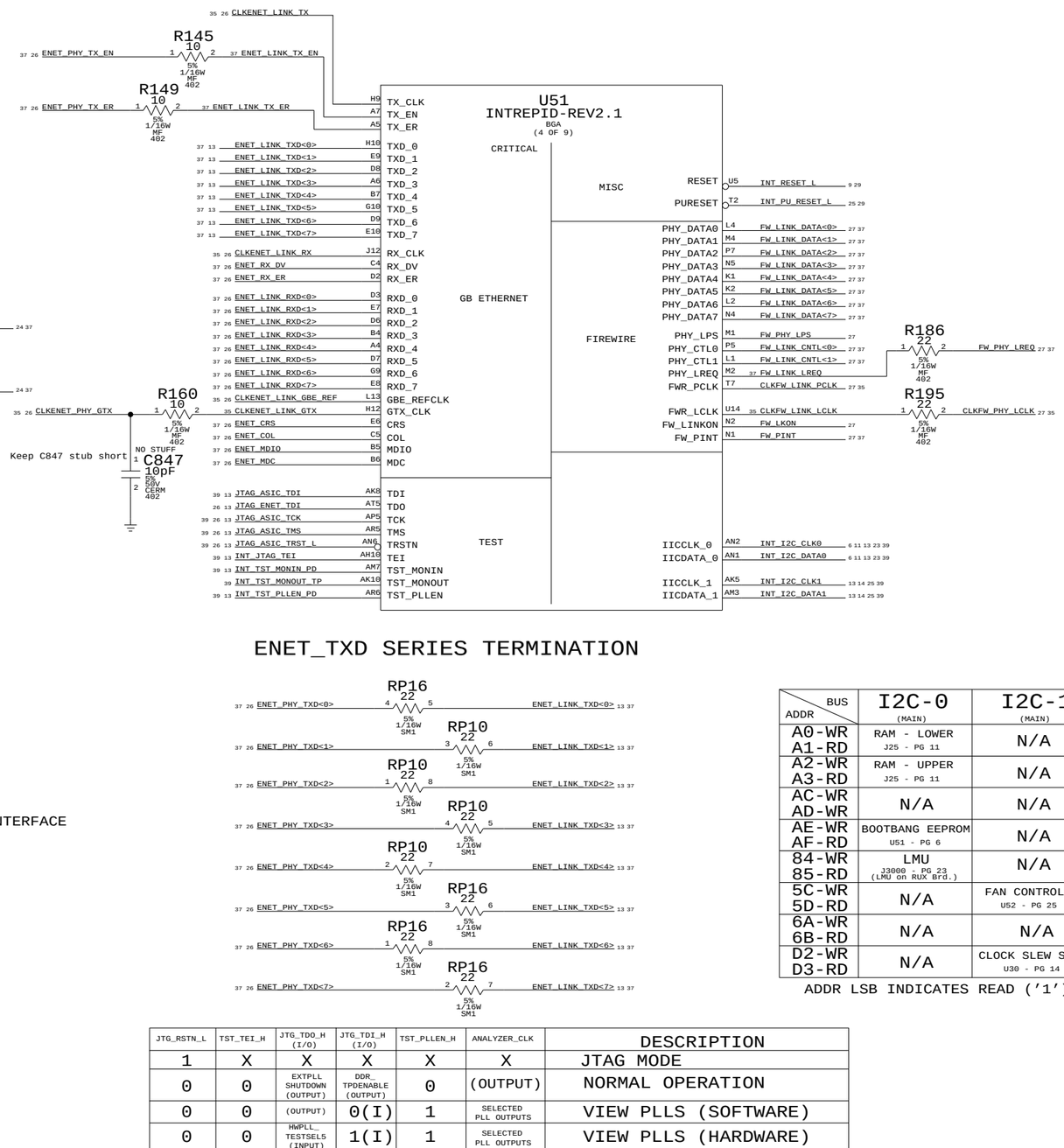
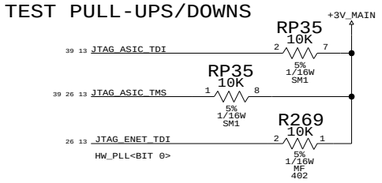
SCALE: NONE	SHT 12 OF 40	

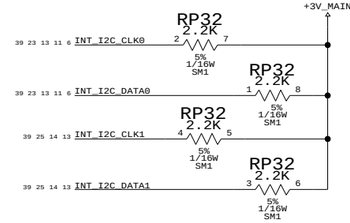




TEST PULL-UPS/DOWNS



I2C PULL-UPS



ENET_TXD SERIES TERMINATION

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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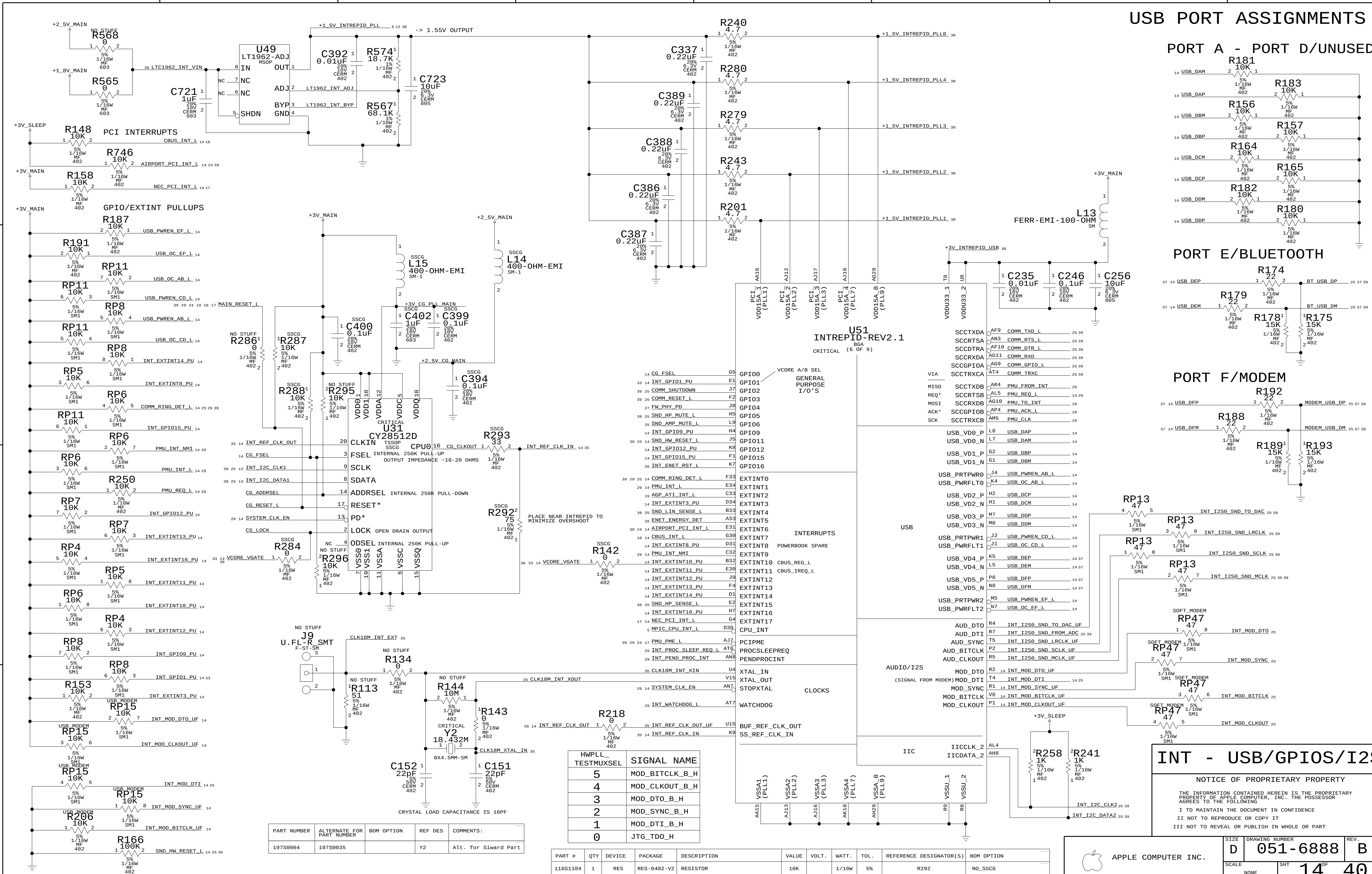
SCALE: NONE	SHT 13 OF 40	



HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

INT - USB/GPIOS/I2S

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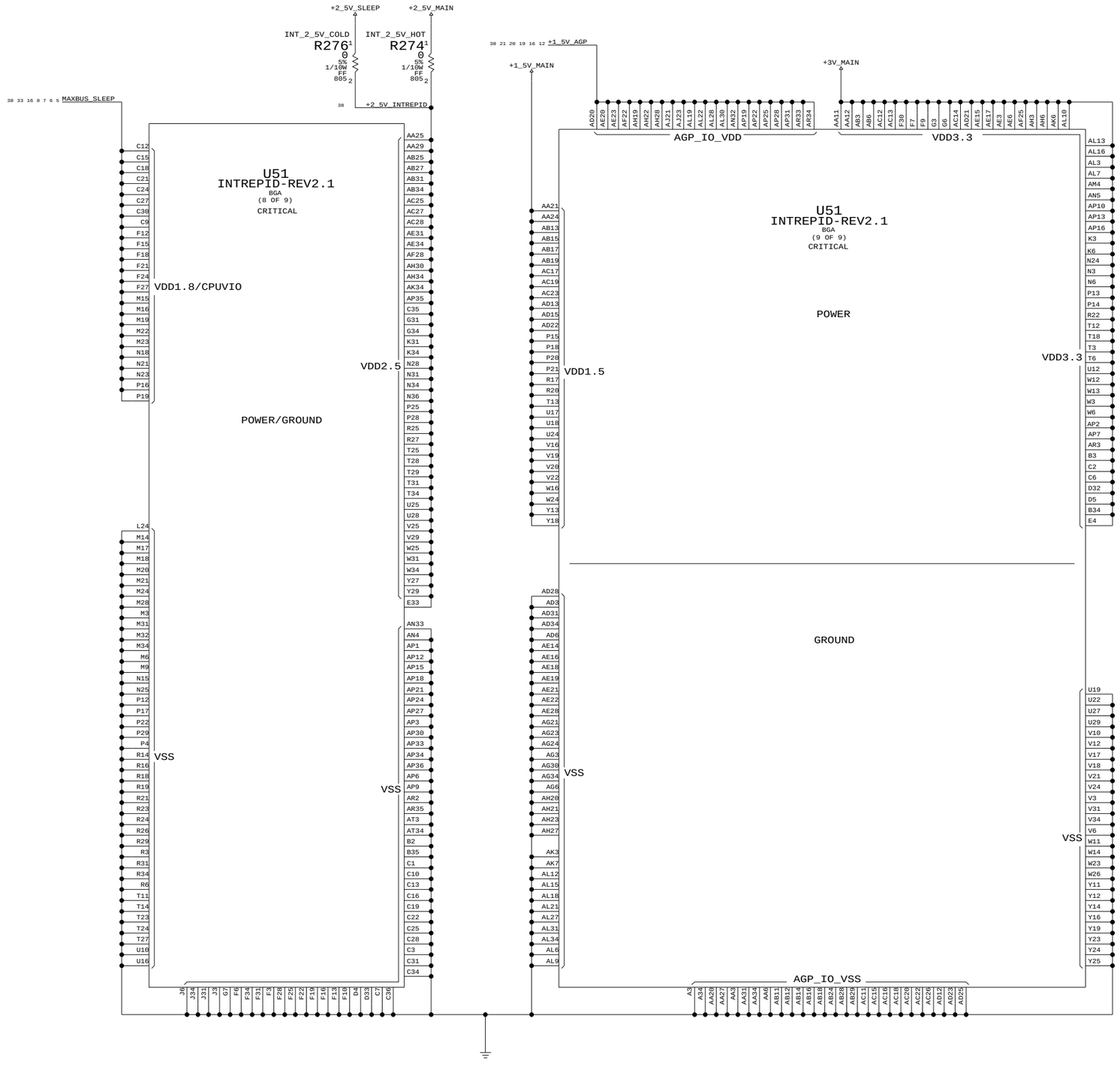
SIZE D | DRAWING NUMBER 051-6888 | REV. B

SCALE NONE | SHT 14 OF 40



Intrepid Power

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SCALE: NONE	SHT 15 OF 40	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 38 MAXBUS_SLEEP

C148 10uF 20% 6.3V CERM 805 · C142 10uF 20% 6.3V CERM 805 · C144 10uF 20% 6.3V CERM 805 · C146 10uF 20% 6.3V CERM 805

C182 0.22uF · C178 0.22uF · C141 0.22uF · C145 0.22uF · C214 0.22uF · C163 0.22uF · C164 0.22uF · C225 0.22uF · C160 0.22uF · C159 0.22uF
C204 0.22uF · C166 0.22uF · C205 0.22uF · C223 0.22uF · C229 0.22uF · C181 0.22uF · C207 0.22uF · C208 0.22uF · C183 0.22uF · C180 0.22uF
C165 0.22uF · C206 0.22uF · C147 0.22uF · C149 0.22uF · C179 0.22uF · C162 0.22uF · C161 0.22uF · C213 0.22uF

(20% 6.3V CERM 402)

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 · C325 10uF 20% 6.3V CERM 805 · C201 10uF 20% 6.3V CERM 805 · C200 10uF 20% 6.3V CERM 805

C299 0.22uF · C279 0.22uF · C262 0.22uF · C292 0.22uF · C248 0.22uF · C302 0.22uF · C300 0.22uF · C290 0.22uF · C272 0.22uF · C259 0.22uF
C301 0.22uF · C278 0.22uF · C226 0.22uF · C238 0.22uF · C250 0.22uF · C263 0.22uF · C224 0.22uF · C222 0.22uF · C261 0.22uF · C227 0.22uF
C271 0.22uF · C310 0.22uF · C288 0.22uF · C260 0.22uF · C303 0.22uF · C287 0.22uF · C258 0.22uF · C236 0.22uF · C289 0.22uF

(20% 6.3V CERM 402)

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

38 21 20 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 · C380 10uF 20% 6.3V CERM 805 · C382 10uF 20% 6.3V CERM 805 · C379 10uF 20% 6.3V CERM 805

C367 0.22uF · C319 0.22uF · C330 0.22uF · C363 0.22uF · C366 0.22uF · C332 0.22uF · C361 0.22uF · C320 0.22uF · C328 0.22uF · C364 0.22uF
C365 0.22uF · C329 0.22uF · C345 0.22uF · C346 0.22uF · C373 0.22uF · C344 0.22uF · C331 0.22uF · C312 0.22uF · C354 0.22uF · C347 0.22uF
C321 0.22uF

(20% 6.3V CERM 402)

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 · C376 10uF 20% 6.3V CERM 805 · C377 10uF 20% 6.3V CERM 805 · C375 10uF 20% 6.3V CERM 805

C170 0.22uF · C358 0.22uF · C268 0.22uF · C327 0.22uF · C342 0.22uF · C215 0.22uF · C352 0.22uF · C171 0.22uF · C158 0.22uF · C309 0.22uF
C175 0.22uF · C357 0.22uF · C351 0.22uF · C350 0.22uF · C286 0.22uF · C176 0.22uF · C189 0.22uF · C167 0.22uF · C371 0.22uF · C359 0.22uF
C285 0.22uF · C283 0.22uF · C269 0.22uF · C221 0.22uF · C234 0.22uF · C247 0.22uF · C257 0.22uF · C343 0.22uF · C313 0.22uF · C228 0.22uF
C360 0.22uF · C308 0.22uF · C318 0.22uF · C237 0.22uF · C317 0.22uF · C341 0.22uF · C177 0.22uF · C212 0.22uF · C349 0.22uF · C184 0.22uF

(20% 6.3V CERM 402)

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 · C322 10uF 20% 6.3V CERM 805 · C191 10uF 20% 6.3V CERM 805 · C202 10uF 20% 6.3V CERM 805

C304 0.22uF · C266 0.22uF · C172 0.22uF · C281 0.22uF · C243 0.22uF · C253 0.22uF · C334 0.22uF · C241 0.22uF · C348 0.22uF · C192 0.22uF
C306 0.22uF · C252 0.22uF · C275 0.22uF · C297 0.22uF · C240 0.22uF · C218 0.22uF · C274 0.22uF · C369 0.22uF · C368 0.22uF · C168 0.22uF
C265 0.22uF · C251 0.22uF · C216 0.22uF · C254 0.22uF · C305 0.22uF · C186 0.22uF · C219 0.22uF · C315 0.22uF · C264 0.22uF · C294 0.22uF
C323 0.22uF · C273 0.22uF · C242 0.22uF · C203 0.22uF · C333 0.22uF · C217 0.22uF · C230 0.22uF · C293 0.22uF · C231 0.22uF · C296 0.22uF
C239 0.22uF · C316 0.22uF · C185 0.22uF · C282 0.22uF · C295 0.22uF · C280 0.22uF

(20% 6.3V CERM 402)

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF · C139 0.22uF · C335 0.22uF · C735 0.22uF · C245 0.22uF · C736 0.22uF · C739 0.22uF · C395 0.22uF · C374 0.22uF · C385 0.22uF

(20% 6.3V CERM 402)

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

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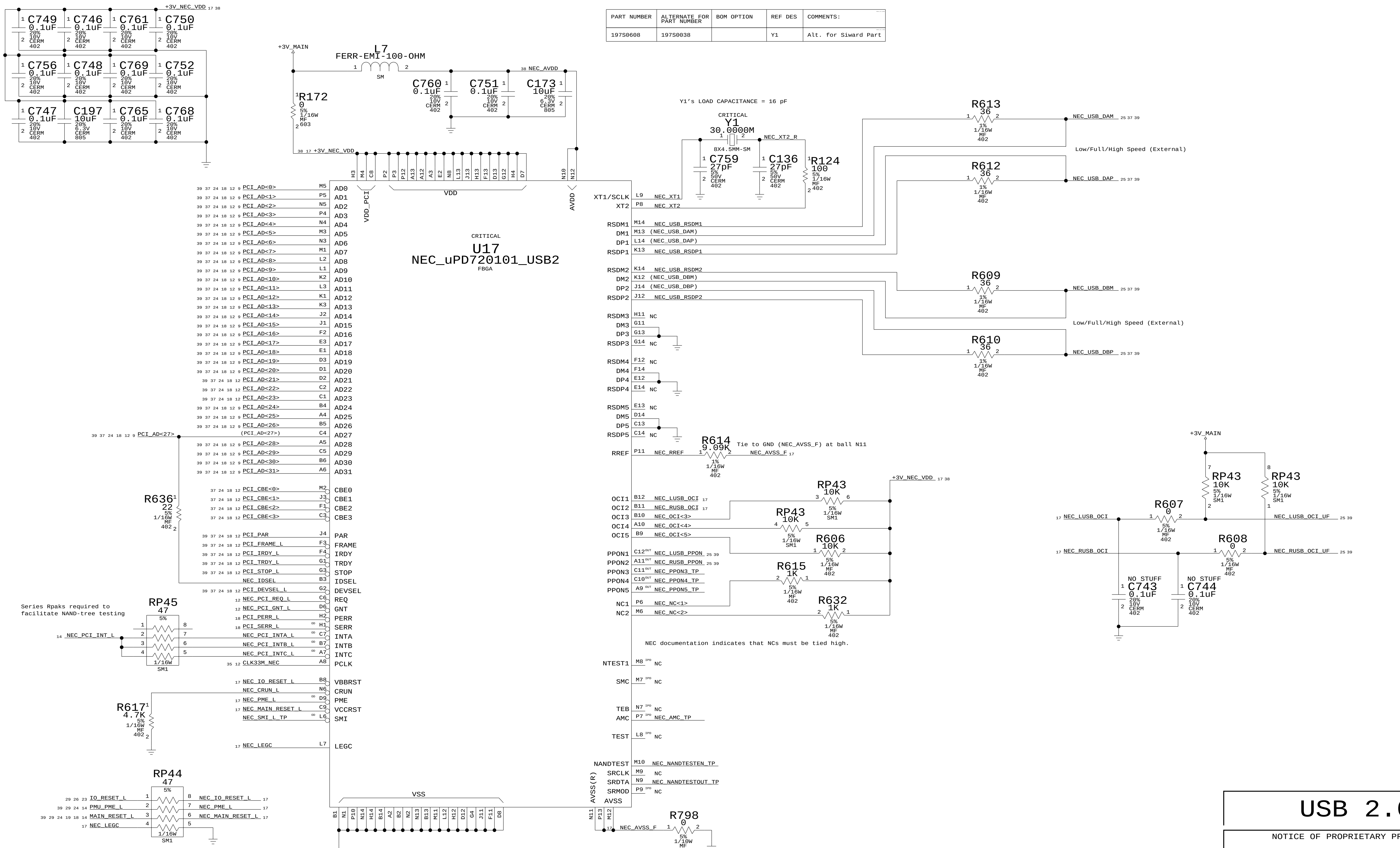
D	051-6888	B
SCALE: NONE	SHT 16 OF 40	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part



+3V_NEC_VDD 17 38
C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402
+3V_MAIN
L7 FERR-EMI-100-OHM SM
R172 0 5% 1/16W MF 603
C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805
38 NEC_AVDD
38 17 +3V_NEC_VDD
H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 N10 N12
VDD_PCI
VDD
AVDD
Y1's LOAD CAPACITANCE = 16 pF
CRITICAL
Y1 30.0000M 8X4.5MM-SM
NEC_XT2_R
C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402
CRITICAL
U17
NEC_uPD720101_USB2
FBGA
39 37 24 18 12 9 PCI_AD<0> M5 AD0
39 37 24 18 12 9 PCI_AD<1> P5 AD1
39 37 24 18 12 9 PCI_AD<2> N5 AD2
39 37 24 18 12 9 PCI_AD<3> P4 AD3
39 37 24 18 12 9 PCI_AD<4> N4 AD4
39 37 24 18 12 9 PCI_AD<5> M3 AD5
39 37 24 18 12 9 PCI_AD<6> N3 AD6
39 37 24 18 12 9 PCI_AD<7> M1 AD7
39 37 24 18 12 9 PCI_AD<8> L2 AD8
39 37 24 18 12 9 PCI_AD<9> L1 AD9
39 37 24 18 12 9 PCI_AD<10> K2 AD10
39 37 24 18 12 9 PCI_AD<11> L3 AD11
39 37 24 18 12 9 PCI_AD<12> K1 AD12
39 37 24 18 12 9 PCI_AD<13> K3 AD13
39 37 24 18 12 9 PCI_AD<14> J2 AD14
39 37 24 18 12 9 PCI_AD<15> J1 AD15
39 37 24 18 12 9 PCI_AD<16> F2 AD16
39 37 24 18 12 9 PCI_AD<17> E3 AD17
39 37 24 18 12 9 PCI_AD<18> E1 AD18
39 37 24 18 12 9 PCI_AD<19> D3 AD19
39 37 24 18 12 9 PCI_AD<20> D1 AD20
39 37 24 18 12 PCI_AD<21> D2 AD21
39 37 24 18 12 PCI_AD<22> C2 AD22
39 37 24 18 12 PCI_AD<23> C1 AD23
39 37 24 18 12 9 PCI_AD<24> B4 AD24
39 37 24 18 12 9 PCI_AD<25> A4 AD25
39 37 24 18 12 9 PCI_AD<26> B5 AD26
39 37 24 18 12 9 PCI_AD<27> (PCI_AD<27>) C4 AD27
39 37 24 18 12 9 PCI_AD<28> A5 AD28
39 37 24 18 12 9 PCI_AD<29> C5 AD29
39 37 24 18 12 9 PCI_AD<30> B6 AD30
39 37 24 18 12 9 PCI_AD<31> A6 AD31
37 24 18 12 PCI_CBE<0> M2 CBE0
37 24 18 12 PCI_CBE<1> J3 CBE1
37 24 18 12 PCI_CBE<2> F1 CBE2
37 24 18 12 PCI_CBE<3> C3 CBE3
R636 22 5% 1/16W MF 402
39 37 24 18 12 PCI_PAR J4 PAR
39 37 24 18 12 PCI_FRAME_L F3 FRAME
39 37 24 18 12 PCI_IRDY_L F4 IRDY
39 37 24 18 12 PCI_TRDY_L G1 TRDY
39 37 24 18 12 PCI_STOP_L G3 STOP
NEC_IDSEL B3 IDSEL
39 37 24 18 12 PCI_DEVSEL_L G2 DEVSEL
12 NEC_PCI_REQ_L C6 REQ
12 NEC_PCI_GNT_L D6 GNT
18 PCI_PERR_L H2 PERR
18 PCI_SERR_L OD H1 SERR
NEC_PCI_INTA_L OD C7 INTA
NEC_PCI_INTB_L OD B7 INTB
NEC_PCI_INTC_L OD A7 INTC
35 12 CLK33M_NEC A8 PCLK
Series Rpaks required to facilitate NAND-tree testing
RP45 47 5% 1/16W SM1
14 NEC_PCI_INT_L
17 NEC_IO_RESET_L B8 VBBRST
NEC_CRUN_L N6 CRUN
17 NEC_PME_L OD D9 PME
17 NEC_MAIN_RESET_L C9 VCCRST
NEC_SMI_L_TP OD L6 SMI
R617 4.7K 5% 1/16W MF 402
17 NEC_LEGC L7 LEGC
RP44 47 5% 1/16W SM1
29 26 23 IO_RESET_L — NEC_IO_RESET_L 17
39 29 24 14 PMU_PME_L — NEC_PME_L 17
39 29 24 19 18 14 MAIN_RESET_L — NEC_MAIN_RESET_L 17
17 NEC_LEGC
VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8
XT1/SCLK L9 NEC_XT1
XT2 P8 NEC_XT2
RSDM1 M14 NEC_USB_RSDM1
DM1 M13 (NEC_USB_DAM)
DP1 L14 (NEC_USB_DAP)
RSDP1 K13 NEC_USB_RSDP1
RSDM2 K14 NEC_USB_RSDM2
DM2 K12 (NEC_USB_DBM)
DP2 J14 (NEC_USB_DBP)
RSDP2 J12 NEC_USB_RSDP2
RSDM3 H11 NC
DM3 G11
DP3 G13
RSDP3 G14 NC
RSDM4 F12 NC
DM4 F14
DP4 E12
RSDP4 E14 NC
RSDM5 E13 NC
DM5 D14
DP5 C13
RSDP5 C14 NC
RREF P11 NEC_RREF
R614 9.09K 1% 1/16W MF 402
Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F 17
R613 36 1% 1/16W MF 402
NEC_USB_DAM 25 37 39
Low/Full/High Speed (External)
R612 36 1% 1/16W MF 402
NEC_USB_DAP 25 37 39
R609 36 1% 1/16W MF 402
NEC_USB_DBM 25 37 39
Low/Full/High Speed (External)
R610 36 1% 1/16W MF 402
NEC_USB_DBP 25 37 39
+3V_NEC_VDD 17 38
OCI1 B12 NEC_LUSB_OCI 17
OCI2 B11 NEC_RUSB_OCI 17
OCI3 B10 NEC_OCI<3>
OCI4 A10 NEC_OCI<4>
OCI5 B9 NEC_OCI<5>
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
PPON1 C12 OUT NEC_LUSB_PPON 25 39
PPON2 A11 OUT NEC_RUSB_PPON 25 39
PPON3 C11 OUT NEC_PPON3_TP
PPON4 C10 OUT NEC_PPON4_TP
PPON5 A9 OUT NEC_PPON5_TP
R615 1K 5% 1/16W MF 402
NC1 P6 NEC_NC<1>
NC2 M6 NEC_NC<2>
R632 1K 5% 1/16W MF 402
NEC documentation indicates that NCs must be tied high.
NTEST1 M8 IPD NC
SMC M7 IPD NC
TEB N7 IPD NC
AMC P7 IPD NEC_AMC_TP
TEST L8 IPD NC
NANDTEST M10 NEC_NANDTESTEN_TP
SRCLK M9 NC
SRDTA N9 NEC_NANDTESTOUT_TP
SRMOD P9 IPD NC
AVSS(R)
AVSS
N11 P13 M12
17 NEC_AVSS_F
R798 0 5% 1/10W MF 603
+3V_MAIN
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402
17 NEC_LUSB_OCI
NEC_LUSB_OCI_UF 25 39
R608 0 5% 1/16W MF 402
17 NEC_RUSB_OCI
NEC_RUSB_OCI_UF 25 39
NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

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	SCALE NONE	SHT 17 OF 40	

PCI1510 PULL-UPS

+3V_SLEEP

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)

R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)

R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805

C786 0.22uF 20% 6.3V CERM 402

C60 10uF 20% 6.3V CERM 805

C776 10uF 20% 6.3V CERM 805

C789 0.22uF 20% 6.3V CERM 402

C791 0.22uF 20% 6.3V CERM 402

C784 0.22uF 20% 6.3V CERM 402

C782 0.22uF 20% 6.3V CERM 402

C783 0.22uF 20% 6.3V CERM 402

C778 0.22uF 20% 6.3V CERM 402

C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

R719 22 5% 1/16W MF 402

R723 47 5% 1/16W MF 402 — MAIN_RESET_L (29 24 19 17 14)

RP1 10K 5% 1/32W 25V (SM)
- CBUS_MFUNC1_PD (18)
- CBUS_MFUNC2_PD (18)
- CBUS_MFUNC3_PD (18)
- CBUS_MFUNC4_PD (18)
- CBUS_MFUNC5_PD (18)
- CBUS_MFUNC6_PD (18)

U8 PCI1510GGU (BGA)

NC	H10	CLK_48_RSVD/NC
PCI1510_VR_EN_L	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0> (39 37 24 17 12 9)	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
(PCI_AD<19>)	H2	AD19
PCI_AD<20> (39 37 24 17 12 9)	G2	AD20
PCI_AD<21> (39 37 24 17 12)	G4	AD21
PCI_AD<22> (39 37 24 17 12)	F1	AD22
PCI_AD<23> (39 37 24 17 12)	C3	AD23
PCI_AD<24> (39 37 24 17 12 9)	F3	AD24
PCI_AD<25> (39 37 24 17 12 9)	E2	AD25
PCI_AD<26> (39 37 24 17 12 9)	F4	AD26
PCI_AD<27> (39 37 24 17 12 9)	B1	AD27
PCI_AD<28> (39 37 24 17 12 9)	D2	AD28
PCI_AD<29> (39 37 24 17 12 9)	E4	AD29
PCI_AD<30> (39 37 24 17 12 9)	D3	AD30
PCI_AD<31> (39 37 24 17 12 9)	E3	AD31
PCI_CBE<0> (37 24 17 12)	K6	C/BE0*
PCI_CBE<1> (37 24 17 12)	M3	C/BE1*
PCI_CBE<2> (37 24 17 12)	J2	C/BE2*
PCI_CBE<3> (37 24 17 12)	A1	C/BE3*
PCI_PAR (39 37 24 17 12)	N1	PAR
PCI_IRDY_L (39 37 24 17 12)	K1	IRDY
PCI_SERR_L (18 17)	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
PCI_PERR_L (18 17)	K3	PERR
PCI_FRAME_L (39 37 24 17 12)	J1	FRAME
PCI_STOP_L (39 37 24 17 12)	L1	STOP
PCI_TRDY_L (39 37 24 17 12)	J3	TRDY
PCI_DEVSEL_L (39 37 24 17 12)	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L (12)	C2	REQ
CBUS_PCI_GNT_L (12)	C1	GNT
CLK33M_CBUS (35 12)	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU (18)	N10	SUSPEND
CBUS_INT_L (14)	K7	MFUNC0
CBUS_MFUNC1_PD (18)	N9	MFUNC1
CBUS_MFUNC2_PD (18)	L9	MFUNC2
CBUS_MFUNC3_PD (18)	K10	MFUNC3
CBUS_MFUNC4_PD (18)	M10	MFUNC4
CBUS_MFUNC5_PD (18)	N12	MFUNC5
CBUS_MFUNC6_PD (18)	L10	MFUNC6
	L11	GRST

GND: A2 A11 D1 F13 H4 K8 M13 N2

CRITICAL — CLAMP FOR PC-CARD, CLAMP FOR PCI

	B11	VCCCB
	L3	VCCP
CBUS_VCCD0_L	N13	VCCD0*
CBUS_VCCD1_L	L12	VCCD1*
CBUS_VPPD0	K9	VPPD0
CBUS_VPPD1	M11	VPPD1
CBUS_DET_1_L (18 39)	L13	CD1*/CCD1*
CBUS_DET_2_L (18 39)	B5	CD2*/CCD2*
CBUS_IORD_L (18)	F12	IORD*/CAD13
CBUS_IOWR_L (18)	C11	IOWR*/CAD15
CBUS_OE_L (18)	G10	OE*/CAD11
CBUS_CE1_L (18)	H13	CE1*/CC/BE0*
CBUS_VS1 (18)	B2	VS1*/CVS1
CBUS_VS2 (18)	A9	VS2*/CVS2
CBUS_WE_L (18)	D13	WE*/CGNT*
CBUS_READY (18)	A6	RDY/IREQ*/CINT*
CBUS_RESET_L (18)	D8	RESET/CRST*
CBUS_REG_L (18)	A8	REG*/CC/BE3*
CBUS_BVD1_L (18)	C6	BVD1/CSTSCHG/STSCHG*/RI*
CBUS_BVD2_L (18)	D6	BVD2/SPKR*/CAUDIO
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*
CBUS_CE2_L (18)	G13	CE2/CAD10*
CBUS_INPACK_L (18)	B8	INPACK/CREQ*
CBUS_WAIT_L (18)	B6	WAIT/CSERR*
CBUS_ADDR<0> (18)	C7	A0/CAD26
CBUS_ADDR<1> (18)	D7	A1/CAD25
CBUS_ADDR<2> (18)	B7	A2/CAD24
CBUS_ADDR<3> (18)	D10	A3/CAD23
CBUS_ADDR<4> (18)	B12	A4/CAD22
CBUS_ADDR<5> (18)	C8	A5/CAD21
CBUS_ADDR<6> (18)	C9	A6/CAD20
CBUS_ADDR<7> (18)	A12	A7/CAD18
CBUS_ADDR<8> (18)	E11	A8/CC/BE1*
CBUS_ADDR<9> (18)	F11	A9/CAD14
CBUS_ADDR<10> (18)	G11	A10/CAD9
CBUS_ADDR<11> (18)	G12	A11/CAD12
CBUS_ADDR<12> (18)	D9	A12/CC/BE2*
CBUS_ADDR<13> (18)	E12	A13/CPAR
CBUS_ADDR<14> (18)	D12	A14/CPERR*
CBUS_ADDR<15> (18)	C10	A15/CIRDY*
CBUS_ADDR_16_UF	B13	A16/CCLK
CBUS_ADDR<17> (18)	F10	A17/CAD16
CBUS_ADDR<18> (18)	E13	A18/RSVD
CBUS_ADDR<19> (18)	A13	A19/CBLOCK*
CBUS_ADDR<20> (18)	E10	A20/CSTOP*
CBUS_ADDR<21> (18)	D11	A21/CDEVSEL*
CBUS_ADDR<22> (18)	C12	A22/CTRDY*
CBUS_ADDR<23> (18)	A10	A23/CFRAME*
CBUS_ADDR<24> (18)	B10	A24/CAD17
CBUS_ADDR<25> (18)	B9	A25/CAD19
CBUS_DATA<0> (18)	A4	D0/CAD27
CBUS_DATA<1> (18)	C4	D1/CAD29
CBUS_DATA<2> (18)	A3	D2/RSVD
CBUS_DATA<3> (18)	K11	D3/CAD0
CBUS_DATA<4> (18)	K12	D4/CAD1
CBUS_DATA<5> (18)	J13	D5/CAD3
CBUS_DATA<6> (18)	J10	D6/CAD5
CBUS_DATA<7> (18)	H12	D7/CAD7
CBUS_DATA<8> (18)	C5	D8/CAD28
CBUS_DATA<9> (18)	B4	D9/CAD30
CBUS_DATA<10> (18)	B3	D10/CAD31
CBUS_DATA<11> (18)	M12	D11/CAD2
CBUS_DATA<12> (18)	J11	D12/CAD4
CBUS_DATA<13> (18)	K13	D13/CAD6
CBUS_DATA<14> (18)	J12	D14/RSVD
CBUS_DATA<15> (18)	H11	D15/CAD8

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

+3V_MAIN

+5V_MAIN

R726 0 5% 1/16W MF 402 — SLEEP_L_LS5 (26 34 29 33 32)

TPS2211_SHTDWN_L

U4 TPS2211 SSOI

NC	9	
V_12	5	AVPP (10)
V_5_1	6	
V_5_2	3	AVCC0 (11)
V_3_1	4	AVCC1 (12)
V_3_2	13	AVCC2
VCCD0	1	
VCCD1	2	
VPPD0	15	
VPPD1	14	
SHTDWN	16	
GND	7	
OC	8	NC

+VPP_CBUS_SW (18 38)

+VCC_CBUS_SW (18 38)

C40 0.1uF 20% 10V CERM 402

C37 0.1uF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 16V CERM 805

C800 2.2uF 20% 16V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL

J5 QT500806-L111 M-ST-SM1

	2	1	CBUS_DATA<3> (18)
CBUS_DET_1_L (39 18)	4	3	CBUS_DATA<4> (18)
CBUS_DATA<11> (18)	6	5	CBUS_DATA<5> (18)
CBUS_DATA<12> (18)	8	7	CBUS_DATA<6> (18)
CBUS_DATA<13> (18)	10	9	
	12	11	CBUS_DATA<7> (18)
CBUS_DATA<14> (18)	14	13	CBUS_CE1_L (18)
CBUS_DATA<15> (18)	16	15	CBUS_ADDR<10> (18)
CBUS_CE2_L (18)	18	17	CBUS_OE_L (18)
CBUS_VS1 (18)	20	19	
	22	21	CBUS_ADDR<11> (18)
CBUS_IORD_L (18)	24	23	CBUS_ADDR<9> (18)
CBUS_IOWR_L (18)	26	25	CBUS_ADDR<8> (18)
CBUS_ADDR<17> (18)	28	27	CBUS_ADDR<13> (18)
CBUS_ADDR<18> (18)	30	29	
	32	31	CBUS_ADDR<14> (18)
CBUS_ADDR<19> (18)	34	33	CBUS_WE_L (18)
CBUS_ADDR<20> (18)	36	35	CBUS_READY (18)
CBUS_ADDR<21> (18)	38	37	+VCC_CBUS_SW (18 38)
+VCC_CBUS_SW (38 18)	40	39	
	42	41	+VPP_CBUS_SW (18 38)
+VPP_CBUS_SW (38 18)	44	43	CBUS_ADDR<16> (18)
CBUS_ADDR<22> (18)	46	45	CBUS_ADDR<15> (18)
CBUS_ADDR<23> (18)	48	47	CBUS_ADDR<12> (18)
CBUS_ADDR<24> (18)	50	49	
	52	51	CBUS_ADDR<7> (18)
CBUS_ADDR<25> (18)	54	53	CBUS_ADDR<6> (18)
CBUS_VS2 (18)	56	55	CBUS_ADDR<5> (18)
CBUS_RESET_L (18)	58	57	CBUS_ADDR<4> (18)
CBUS_WAIT_L (18)	60	59	
	62	61	CBUS_ADDR<3> (18)
CBUS_INPACK_L (18)	64	63	CBUS_ADDR<2> (18)
CBUS_REG_L (18)	66	65	CBUS_ADDR<1> (18)
CBUS_BVD2_L (18)	68	67	CBUS_ADDR<0> (18)
CBUS_BVD1_L (18)	70	69	
	72	71	CBUS_DATA<0> (18)
CBUS_DATA<8> (18)	74	73	CBUS_DATA<1> (18)
CBUS_DATA<9> (18)	76	75	CBUS_DATA<2> (18)
CBUS_DATA<10> (18)	78	77	CBUS_WP_L (18)
CBUS_DET_2_L (39 18)	80	79	

84 81 83 82

CARDBUS

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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 18 OF 40	

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

M10 AGP INTERFACE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 19 OF 40	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

MAIN_RESET_L IS TOGGLED FOR SLEEP

PLL NOISE SHOULD BE LESS THAN 100mV PEAK-TO-PEAK

(PLACE C408 CLOSE TO AGPREF PIN)

(PULL-UP to GPU_MEM_IO)

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC
(PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN AJ29)

(PLACE R315 CLOSE TO OSC)

(SET TO LOW SWING MODE)

Place C879 close to SI pin#2

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
GPU_TMDS_D0_CMF
GPU_TMDS_D1_CMF
GPU_TMDS_D2_CMF

Place all TMDS 10 ohms close to GPU

CRITICAL
U47
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

ATI_DVOD<0> AJ5 ZV_LCDDATA0
ATI_DVOD<1> AK5 ZV_LCDDATA1
ATI_DVOD<2> AG6 ZV_LCDDATA2
ATI_DVOD<3> AH6 ZV_LCDDATA3
ATI_DVOD<4> AJ6 ZV_LCDDATA4
ATI_DVOD<5> AK6 ZV_LCDDATA5
ATI_DVOD<6> AG7 ZV_LCDDATA6
ATI_DVOD<7> AH7 ZV_LCDDATA7
ATI_DVOD<8> AJ7 ZV_LCDDATA8
ATI_DVOD<9> AK7 ZV_LCDDATA9
ATI_DVOD<10> AG8 ZV_LCDDATA10
ATI_DVOD<11> AH8 ZV_LCDDATA11
NC AJ8 ZV_LCDDATA12
NC AK8 ZV_LCDDATA13
NC AG9 ZV_LCDDATA14
NC AH9 ZV_LCDDATA15
NC AJ9 ZV_LCDDATA16
NC AK9 ZV_LCDDATA17
NC AG10 ZV_LCDDATA18
NC AH10 ZV_LCDDATA19
ZV_LCDDATA20_PU AJ10 ZV_LCDDATA20
NC AK10 ZV_LCDDATA21
NC AG11 ZV_LCDDATA22
NC AH11 ZV_LCDDATA23

ATI_DVO_VSYNC AJ4 ZV_LCDCNTL0
ATI_DVO_HSYNC AK4 ZV_LCDCNTL1
ATI_DVOD_DE AH5 ZV_LCDCNTL2
ATI_DVO_CLKP AG5 ZV_LCDCNTL3

ATI_AGP_FBSKEW<0> AJ2 GPIO0
ATI_AGP_FBSKEW<1> AK2 GPIO1
ATI_X1CLK_SKEW<0> AK1 GPIO2
ATI_X1CLK_SKEW<1> AH3 GPIO3
ATI_BUS_CFG<0> AH2 GPIO4
ATI_BUS_CFG<1> AJ1 GPIO5
ATI_BUS_CFG<2> AF4 GPIO6
ATI_GPIO7_SPN AH1 GPIO7
ATI_GPIO8_PD AG3 GPIO8
ATI_GPIO9_SPN AF3 GPIO9
ATI_GPIO10_SPN AG2 GPIO10
ATI_GPIO11_SPN AF2 GPIO11
ATI_GPIO12_SPN AG1 GPIO12
ATI_GPIO13_SPN AF1 GPIO13
HPD_PWR_SNS_EN AE2 GPIO14
GPU_VCORE_CNTL_L AE1 GPIO15
ATI_SSCLK_IN M1 GPIO16

ATI_TMDS_DN<0> AJ13 TX0M
ATI_TMDS_DP<0> AK13 TX0P
ATI_TMDS_DN<1> AJ14 TX1M
ATI_TMDS_DP<1> AK14 TX1P
ATI_TMDS_DN<2> AJ15 TX2M
ATI_TMDS_DP<2> AK15 TX2P
ATI_TMDS_CLKN AJ12 TXCM
ATI_TMDS_CLKP AK12 TXCP

ATI_CLK27M_IN AJ29 XTALIN
NC AJ30 XTALOUT
ATI_TESTEN AH24 TESTEN
NC AJ26 SSIN

B24 VSS
B20 VSS
A24 VSS

ROMCSB AE5 NC
R AK28 22 GPU_R
G AK27 22 GPU_G
B AK26 22 GPU_B
VSYNC AG27 ATI_VSYNC 22
V2SYNC AG25 NC
HSYNC AG26 ATI_HSYNC 22
H2SYNC AG24 NC
RSET AK25 ATI_RSET
R2SET AJ24 ATI_R2SET
Y_G AK23 22 GPU_Y
C_R AK24 22 GPU_C
COMP_B AK22 22 GPU_COMP
DIGON AE13 22 FP_PWR_EN
BLON AF13 22 INV_ON_PWM
HPD1 AF11 GPU_HPD 22
AUXWIN AJ27 AUXWIN_PU
DDC1DATA AH28 GPU_DVI_DDC_DATA 22
DDC1CLK AH27 GPU_DVI_DDC_CLK 22
DDC2DATA AE12 LVDS_DDC_DATA 22 39
DDC2CLK AF12 LVDS_DDC_CLK 22 39
DDC3DATA AH26 SI_I2S_DATA 19
DDC3CLK AH25 SI_I2C_CLK 19

TXOUT_U0N AH18 LVDS_U0N 22 37
TXOUT_U0P AG18 LVDS_U0P 22 37
TXOUT_U1N AH19 LVDS_U1N 22 37
TXOUT_U1P AG19 LVDS_U1P 22 37 38
TXOUT_U2N AH20 LVDS_U2N 22 37
TXOUT_U2P AG20 LVDS_U2P 22 37
TXOUT_U3N AH22 LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P AG22 LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN AH21 CLKLVDS_UN 22 37
TXCLK_UP AG21 CLKLVDS_UP 22 37
TXOUT_L0N AK16 LVDS_L0N 22 37 39
TXOUT_L0P AJ16 LVDS_L0P 22 37 39
TXOUT_L1N AK17 LVDS_L1N 22 37 39
TXOUT_L1P AJ17 LVDS_L1P 22 37 39
TXOUT_L2N AK18 LVDS_L2N 22 37 39
TXOUT_L2P AJ18 LVDS_L2P 22 37 39
TXOUT_L3N AK20 LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P AJ20 LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN AK19 CLKLVDS_LN 22 37 39
TXCLK_LP AJ19 CLKLVDS_LP 22 37 39

SSOUT AJ25 NC
VSS A20
VSS B21

38 21 20 19 16 15 12 +1.5V_AGP

CRITICAL
Q23
SI3446DV
TSOP

GPU_CORE_OK 20 21
+GPU_VDD15_UF 20 38

C407 1000pF 10% 25V X7R 402

L17
FERR-220-OHM
0805

38 +1.5V_GPU_VDD15 (500mA)

C448 0.01uF 20% 16V CERM 402
C443 0.01uF 20% 16V CERM 402
C435 0.01uF 20% 16V CERM 402
C482 0.01uF 20% 16V CERM 402
C411 10uF 20% 6.3V CERM 805
C505 0.01uF 20% 16V CERM 402
C532 0.01uF 20% 16V CERM 402
C529 0.01uF 20% 16V CERM 402
C526 0.01uF 20% 16V CERM 402

CRITICAL
U47
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

F12 L6 T6 AB6 F17 G25 R25 AB25 → VDD15
AJ3 AF25 AG4 AH4 AF5 F6 G6 H6 P6 AD26 V6 W6 AC6 AD6 AE6 F7 F10 AE10 F11 AE11 F13 F14 AE14 AF14 W26 AF15 AE17 AC25 AE18 F23 F24 AE24 F25 M25 N25 W25 V25 → VDDC
G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 H7 H8 H23 H24 J7 J24 K7 K24 L7 L24 M7 M24 N7 N24 P7 P24 R7 R24 T7 T24 U7 U24 V7 V24 W7 W24 Y7 Y24 AA7 AA24 AB7 AB24 AC7 AC8 AC23 AC24 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 → VSS

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

39 38 20 19 GPU_VCORE

C484 10uF 20% 6.3V CERM 805
C485 10uF 20% 6.3V CERM 805
C440 0.22uF 20% 6.3V CERM 402
C441 0.22uF 20% 6.3V CERM 402
C445 0.22uF 20% 6.3V CERM 402
C446 0.22uF 20% 6.3V CERM 402
C449 0.22uF 20% 6.3V CERM 402
C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF 20% 6.3V CERM 402
C451 0.22uF 20% 6.3V CERM 402
C494 0.22uF 20% 6.3V CERM 402
C498 0.22uF 20% 6.3V CERM 402
C509 0.22uF 20% 6.3V CERM 402
C510 0.22uF 20% 6.3V CERM 402
C512 0.22uF 20% 6.3V CERM 402
C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF 20% 6.3V CERM 402
C525 0.22uF 20% 6.3V CERM 402
C528 0.22uF 20% 6.3V CERM 402
C531 0.22uF 20% 6.3V CERM 402
C533 0.22uF 20% 6.3V CERM 402
C477 0.22uF 20% 6.3V CERM 402
C486 0.22uF 20% 6.3V CERM 402
C495 0.22uF 20% 6.3V CERM 402

R332 715 1% 1/16W MF 402
R333 499 1% 1/16W MF 402
R359 75 1% 1/16W MF 402
R356 75 1% 1/16W MF 402
R360 75 1% 1/16W MF 402
R366 10K 5% 1/16W MF 402
R368 10K 5% 1/16W MF 402
R779 10K 5% 1/16W MF 402

38 21 20 19 12 +3V_GPU

R384 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402 NO STUFF
R382 10K 5% 1/16W MF 402 NO STUFF
R383 10K 5% 1/16W MF 402 NO STUFF
R385 10K 5% 1/16W MF 402 NO STUFF
R381 10K 5% 1/16W MF 402 NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0> 20
(GPIO1) ATI_AGP_FBSKEW<1> 20
(GPIO2) ATI_X1CLK_SKEW<0> 20
(GPIO3) ATI_X1CLK_SKEW<1> 20
(GPIO4) ATI_BUS_CFG<0> 20
(GPIO5) ATI_BUS_CFG<1> 20
(GPIO6) ATI_BUS_CFG<2> 20

R393 10K 5% 1/16W MF 402 NO STUFF
R396 10K 5% 1/16W MF 402 NO STUFF
R395 10K 5% 1/16W MF 402 NO STUFF
R391 10K 5% 1/16W MF 402 NO STUFF
R392 10K 5% 1/16W MF 402 NO STUFF
R394 10K 5% 1/16W MF 402 NO STUFF
R390 10K 5% 1/16W MF 402 NO STUFF

M10 Power Shut down Sequencing

+2_5V_SLEEP
XW11 SM
DP5 BAS16TW SOT-363
XW9 SM
38 +1.8V_ATI_PVDD 1 2 38 +1.8V_PVDD_NECK
+2_5V_SLEEP_NECK 1
XW12 SM
DP5 BAS16TW SOT-363
38 GPU_VCORE_NECK
+1.5V_AGP_NECK 38
XW4 SM
1 2 +1.5V_AGP 38 19 20 21
XW5 SM
DP5 BAS16TW SOT-363
38 +GPU_VDD15_NECK
+GPU_VDD15_UF 20 38

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	3	RES,MTL FILM,1/16W,75OHM 0402	R346,R342,R341	?

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS
+5V_MAIN
+3V_GPU

CRITICAL
Q48
SI7860DP
SO-8-PWRPK

C706 4.7uF 1% 25V CERM 1206
C708 4.7uF 20% 25V CERM 1206

D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603
C481 0.1uF 20% 25V CERM 603
1778_BST_RC

CRITICAL
Q49
IRF7832
SO-8

L64
2.1uH-11A
SM

D29
SM
MBRS130LT3

C838 0.001uF 20% 50V CERM 402 NO STUFF

OMIT
XW19
JUMPER
OPEN

GPU_VCORE 19 20 38 39
GPU_VCORE_SW 38
GPU_VCORE_SW_F 38

C704 22uF 20% 10V CERM 1210
CRITICAL
C705 330uF 20% 6.3V TANT CASE-D4
CRITICAL
C707 330uF 20% 6.3V TANT CASE-D4
CRITICAL
C711 330uF 20% 6.3V TANT CASE-D4

R329 4.99K 1% 1/10W MF 402
R328 18.2K 1% 1/16W MF 402
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402
R786 100K 5% 1/16W MF 402
C846 0.1uF 20% 10V CERM 402
R549 10K 5% 1/16W MF 402
C712 0.1uF 20% 10V CERM 402 NO STUFF

GPU_PWRMSR
HIGH_VCORE_DIV
HIGH_VCORE
GPU_VCORE_CNTL_RC
GPU_VCORE_CNTL
GPU_VCORE_CNTL_L 1 20

Q25 2N7002DW SOT-363
Q25 2N7002DW SOT-363

R559 100K 5% 1/16W MF 402
R556 100K 5% 1/16W MF 402
DP7 BAS16TW SOT-363
DP7 BAS16TW SOT-363
DP7 BAS16TW SOT-363
+1.5V_AGP 21 20 15 12 19 16 38
GPU_VCORE_PWR_SEQ
GPU_VCORE_SEQ_L
GPU_VCORE_SEQ
SLEEP_L_LS5 18 26 32 33 34
DCDC_EN 28 32 33
Q51 2N3904 SM
Q52 2N3904 SM
R558 10K 5% 1/16W MF 402
R555 33K 5% 1/16W MF 402

R343 0 5% 1/16W MF 402
R352 63.4K 1% 1/16W MF 402 NO STUFF
C466 4.7uF 20% 10V CERM 1206
1778_GND 38 38
R357 100K 5% 1/16W MF 402
C431 0.1uF 20% 25V CERM 603
38 1778_VCC
38 1778_VIN
+5V_MAIN

EXT TMI VCC VCC
U32
LTC1778
SSOP
CRITICAL

RUN/SS 1
ITH 5
VRNG 3
FCB 4
PGOOD 2
SGND 6
PGND 13
ION 7 38 1778_ION
BOOST 16 38 1778_BST
TG 15 38 1778_TG
SW 14
BG 12 38 1778_BG
VFB 8 38 1778_VFB

1778_SHDN_L
38 1778_ITH
38 1778_VRNG
38 1778_FCB
21 38 GPU_CORE_OK

R339 20K 1% 1/16W MF 402
38 1778_ITH_RC
C465 220pF 5% 25V CERM 402
C455 470pF 10% 50V CERM 402
R344 0 5% 1/16W MF 402 NO STUFF
R353 0 5% 1/16W MF 402
C480 0.1uF 20% 10V CERM 402
38 20 1778_GND

OMIT
XW6
SM

M10 CORE PWR/LVDS/TMDS

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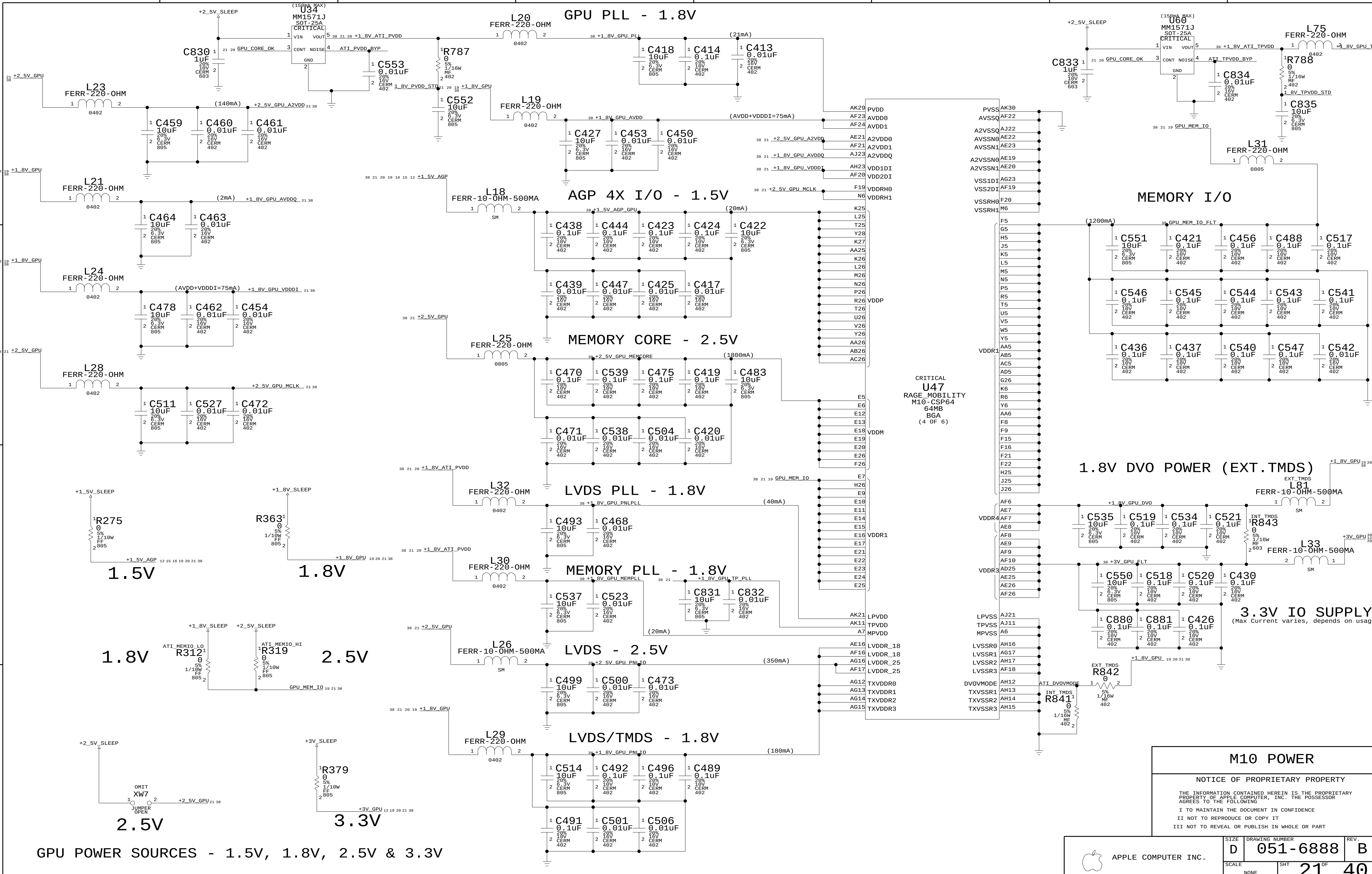
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 20 OF 40	



M10 POWER

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D	051-6888	B
SCALE NONE	SHT 21 OF 40	

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
U40 74AHC1G32 SM
U39 74AHC1G32 SM
20 ATI_VSYNC
20 ATI_HSYNC
4 ATI_VSYNC_BUF
4 ATI_HSYNC_BUF
L38 OMIT FERR-60-OHM-0.1A 0402
L36 OMIT FERR-60-OHM-0.1A 0402
2 VGA_VSYNC 22 39
2 VGA_HSYNC 22 39

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
L46 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
L47 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
TMDS_DN<0> 39 37 19
TMDS_DP<0> 39 37 19
TMDS_CONN_DN<0>
TMDS_CONN_DP<0>
TMDS_DN<2> 39 37 19
TMDS_DP<2> 39 37 19
TMDS_CONN_DN<2>
TMDS_CONN_DP<2>
TMDS_DN<1> 39 37 19
TMDS_DP<1> 39 37 19
TMDS_CONN_DN<1>
TMDS_CONN_DP<1>

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM SYM_VER-1
TMDS_CLKP 37 19
TMDS_CLKN 37 19
TMDS_CONN_CLKP 22 36 39
TMDS_CONN_CLKN 22 36 39

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP
F2 CRITICAL 0.5AMP-13.2V SM
L42 400-OHM-EMI SM-1
+5V_DDC_SLEEP 22 38 39
+5V_DDC_SLEEP_UF 38

Isolation required for DVI power switch

D19 SM MBR0530 DDC_CLK_ISO

J22 CRITICAL QH1112 F-RT-TH CHGND1 CHGND2

C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201
C667 0.01uF 20% 50V CERM 603

R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
R477 100 5% 1/16W MF 402
R469 100 5% 1/16W MF 402

DVI_DDC_CLK
DVI_DDC_DATA
DVI_HPD
(+5V_DDC_SLEEP)
DVI_DDC_CLK_UF
DVI_DDC_DATA_UF
DVI_HPD_UF
VGA_VSYNC 22 39
VGA_R 22 39
VGA_G 22 39
VGA_B 22 39
VGA_HSYNC 22 39

R464 0 5% 1/16W MF 402
PLACE NEAR C5A & C5B
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19

3V LEVEL SHIFTERS

+3V_SLEEP
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363
R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402
GPU_DVI_DDC_CLK 20
GPU_DVI_DDC_DATA 20
GPU_HPD 20
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, +5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q38 TP0610 SM
DVI_DDC_CLK_UF 39 22
+5V_DDC_SLEEP 39 38 22
DVI_TURN_ON
DVI_TURN_ON_ILIM
R473 680 5% 1/16W MF 402
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
DVI_TURN_ON_BASE
R460 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
SOFT_PWR_ON_L 23 29 33 39

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
C668 0.1uF 10% 10V CERM 402
R485 68.1K 1% 1/16W MF 402
HPD_4V_REF
U42 LMC7211 SM
R472 10K 1% 1/16W MF 402
DVI_HPD_UF 39 22
DVI_HPD_DIV
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
HPD_REF_EN_L
HPD_PWR_SW_BASE
R475 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
HPD_PWR_SW
R470 330 5% 1/16W MF 402
Q40 2N7002DW SOT-363
HPD_PWR_SNS_EN 20
R483 470K 5% 1/16W MF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0214	3	IND,FERRITE,27NH,10%,0805	L49,L43,L40	?
152S0210	3	IND,FERRITE,27NH,10%,0805	L50,L44,L41	?
131S1114	3	CAP,CER,1.5PF,+/-.25PF,0402	C642,C635,C632	?
131S1121	3	CAP,CER,8.2PF,+/-.25PF,0402	C641,C634,C631	?

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM
XW14 SM
L54 FERR-10-OHM-500MA SM
L56 FERR-10-OHM-500MA SM
GPU_TV_GND1 38
GPU_TV_GND2 38
TV_GND1 38 39
TV_GND2 38 39
L53 3.3uH 0603
L57 3.3uH 0603
L55 3.3uH 0603
GPU_Y 20
GPU_C 20
GPU_COMP 20
C657 0.01uF 20% 50V CERM 603
C656 560pF 10% 50V CERM 402
C663 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
C661 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
C664 560pF 10% 50V CERM 402
C659 0.01uF 20% 50V CERM 603
J21 CRITICAL MINIDIN RT-TH MH11773-WMR8A
TV_C 39
TV_Y 39
TV_COMP 39
CHGND1

Place GND shorts at graphics controller

LCD INTERFACE
LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402
LCD_PWREN_L
LCD_DIGON_L
Q28 2N7002 SM
FP_PWR_EN 22 20
Q29 TS3P SI3443DV
+3V_LCD_SW 38
L27 FERR-250-OHM SM
+3V_LCD (LVDS DDC POWER) 39 38
C503 0.001uF 20% 50V CERM 402
CHGND4
+3V_SLEEP
R543 100K 5% 1/10W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
LVDS_DDC_CLK 20 22 39
LVDS_DDC_DATA 20 22 39
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
NO STUFF
C702 0.001uF 20% 50V CERM 402
C548 0.001uF 20% 50V CERM 402
CHGND4
J14 CRITICAL G-501973 F-RT-SM

LVDS_DDC_CLK 22 20 39
LVDS_DDC_DATA 22 20 39
LVDS_L0N 37 20 39
LVDS_L0P 37 20 39
LVDS_L1N 37 20 39
LVDS_L1P 37 20 39
LVDS_L2N 39 37 20 39
LVDS_L2P 39 37 20 39
CLKLVDS_LN 39 37 20
CLKLVDS_LP 39 37 20
LVDS_U0N 37 20 39
LVDS_U0P 37 20 39
LVDS_U1N 37 20 39
LVDS_U1P 37 20 39
LVDS_U2N 37 20 39
LVDS_U2P 37 20 39
CLKLVDS_UN 37 20
CLKLVDS_UP 37 20
C549 0.001uF 20% 50V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603
CHGND3

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM
+14V_INV 38 1
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW 38
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402
FP_PWR_EN_L
C813 10uF 20% 6.3V CERM 805
C812 0.001uF 20% 50V CERM 402
+5V_INV_SW 39 38
J4 CRITICAL SM-2MT
FP_PWR_EN 22 20
L72 400-OHM-EMI SM-1
BRIGHT_PWM 39
C815 0.001uF 20% 50V CERM 402
INV_GND 39
+3V_MAIN
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
L1 FERR-250-OHM SM
C22 0.1uF 10% 10V CERM 402
INV_ON_PWM 20
NC7S32 SC70 U2
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

VIDEO CONNECTORS

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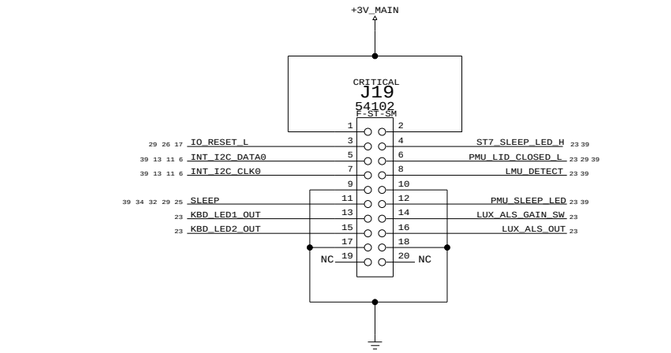
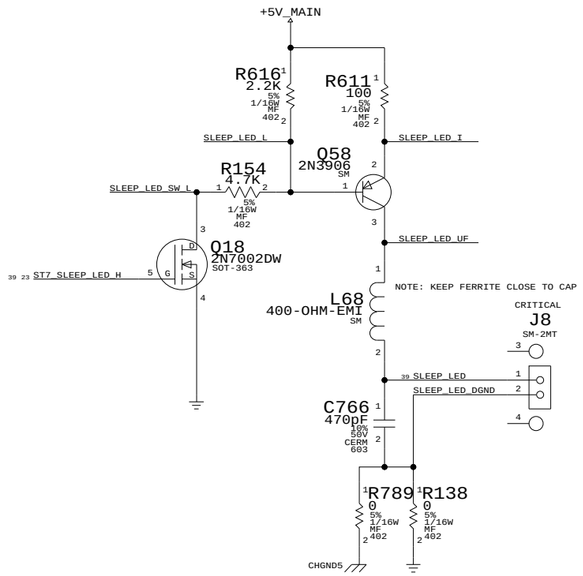
SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 22 OF 40	

LMU/RIGHT SENSOR CONNECTOR

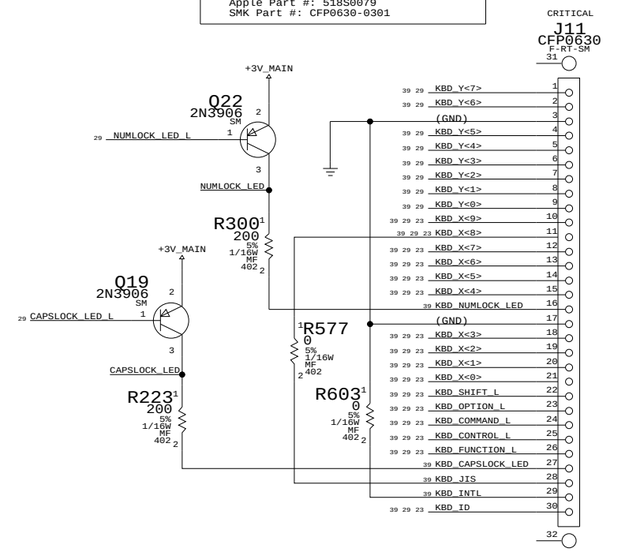


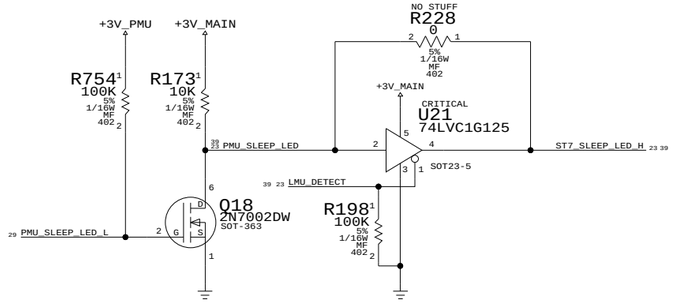
SLEEP LED



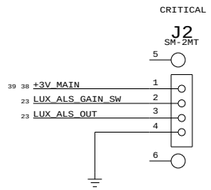
TOP CONTACT ZIF KEYBOARD CONN

CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301

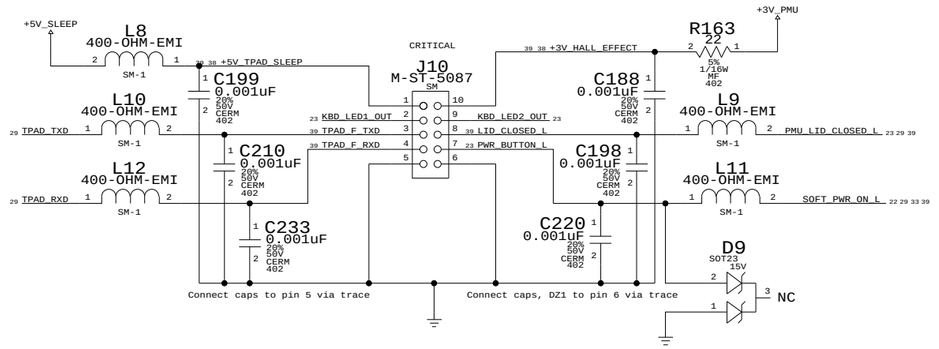




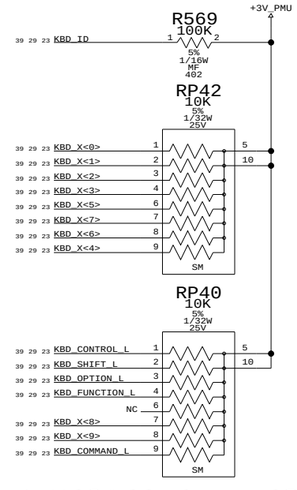
LEFT LIGHT SENSOR CONNECTOR



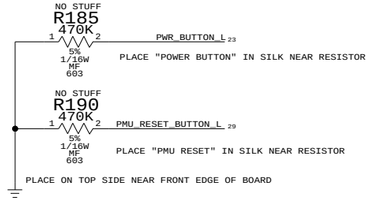
TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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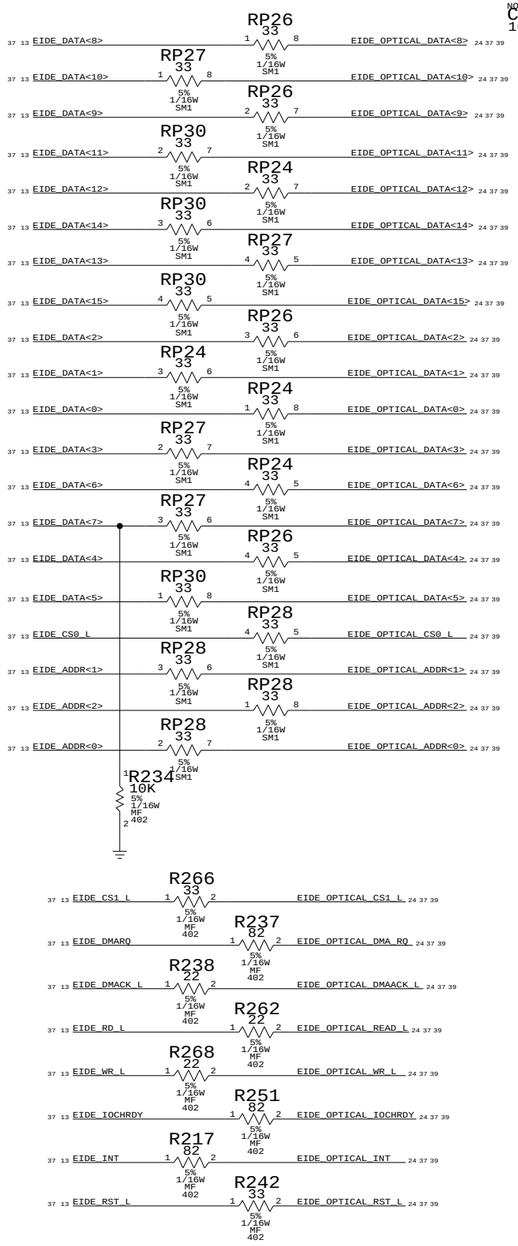
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B

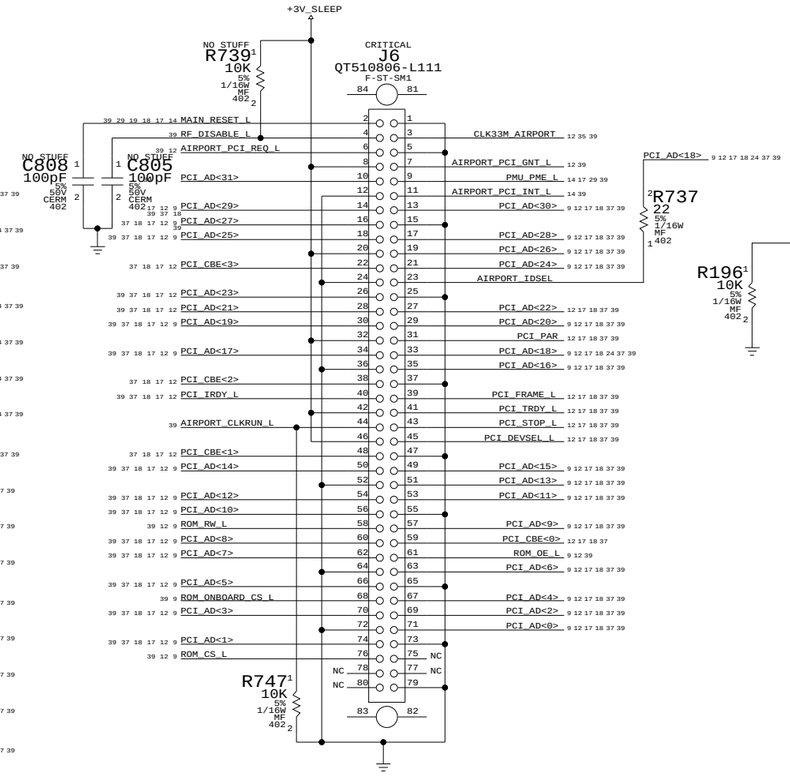
SCALE	SHT
NONE	23 OF 40

EIDE SERIES TERMINATION

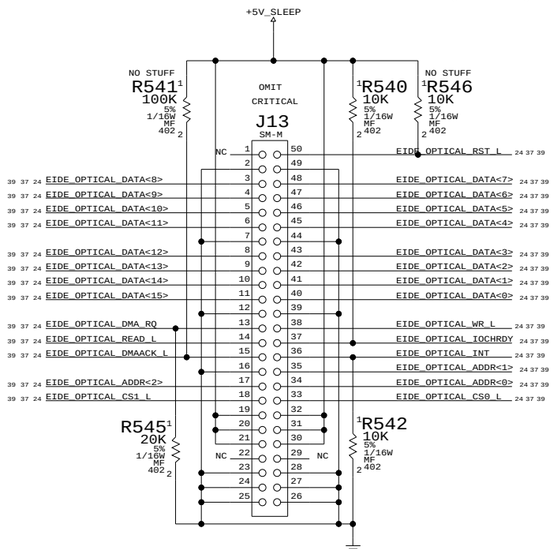
PLACE TERMINATORS NEAR INTREPID



WIRELESS INTERFACE

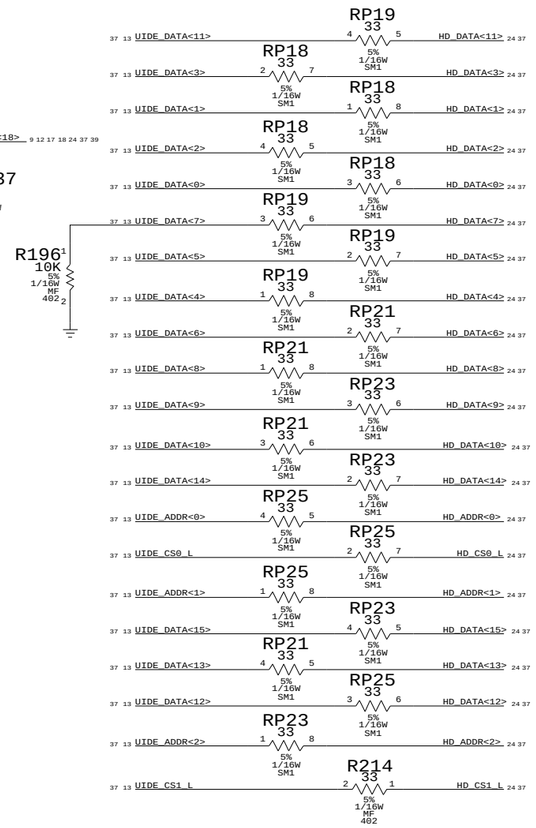


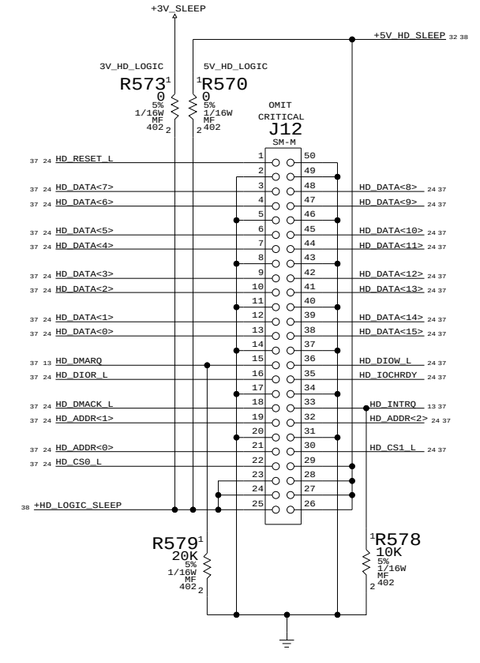
OPTICAL DRIVE INTERFACE (EIDE)



HARD DRIVE INTERFACE (UATA100)

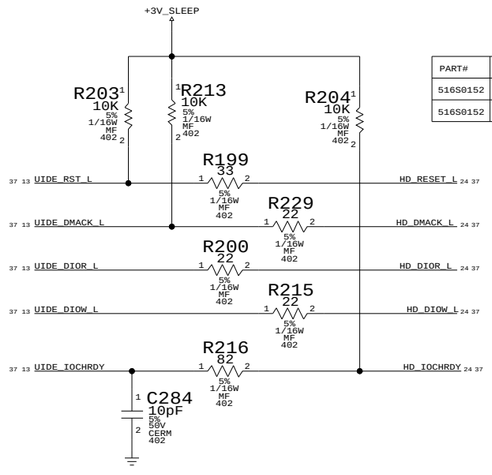
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J12	CRITICAL	?
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J13	CRITICAL	?

INTERNAL I/O CONNECTORS

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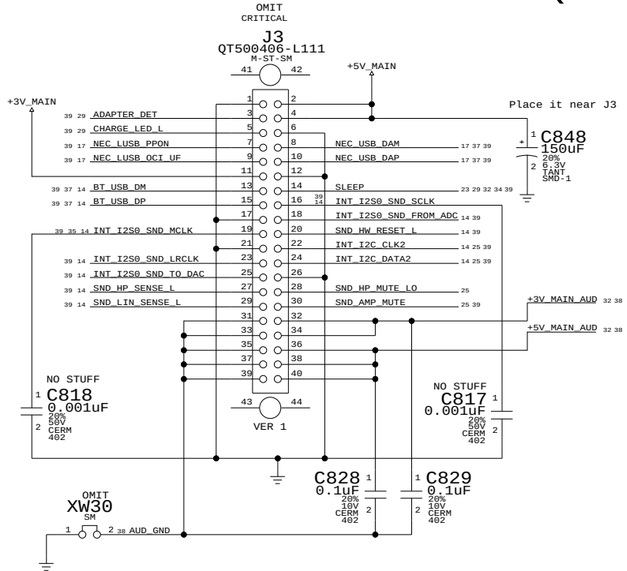
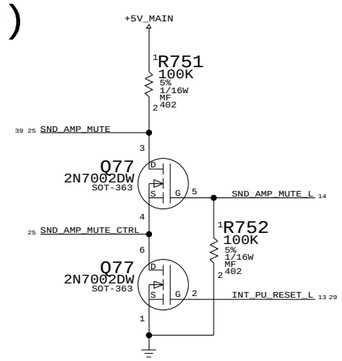
D	051-6888	B
SCALE: NONE	SHT 24 OF 40	

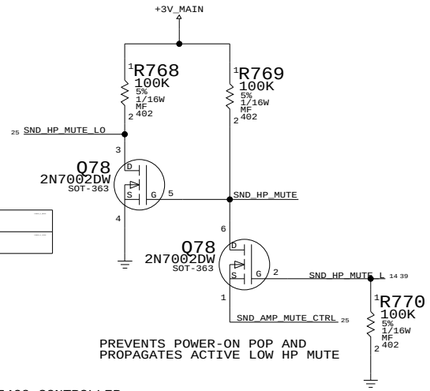
LEFT I/O & AUDIO BOARD (LIO)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD	J3	CRITICAL	?

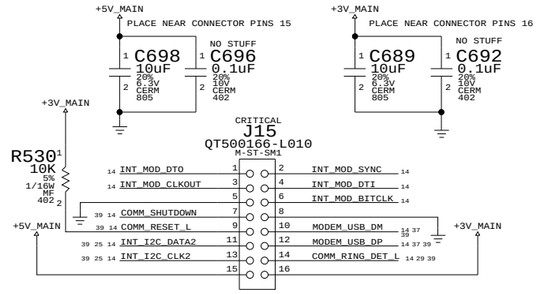


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



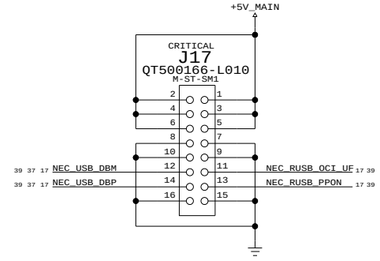
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

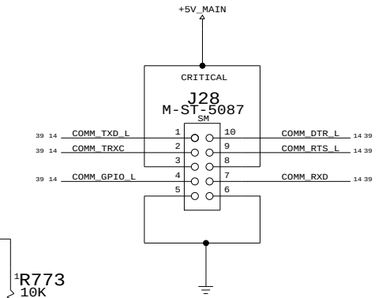


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

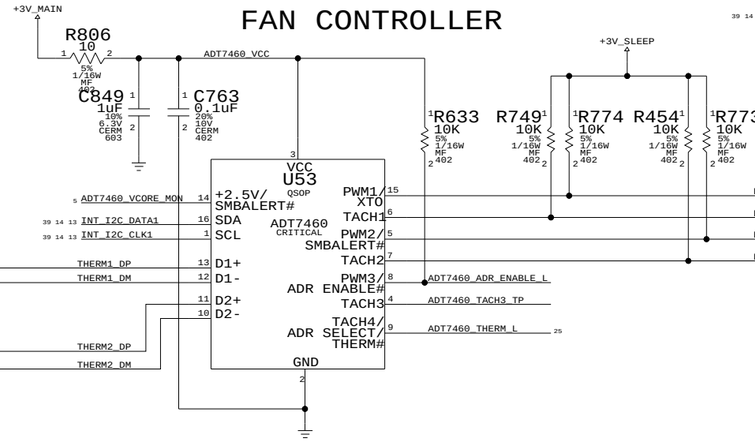


SERIAL DEBUG INTERFACE

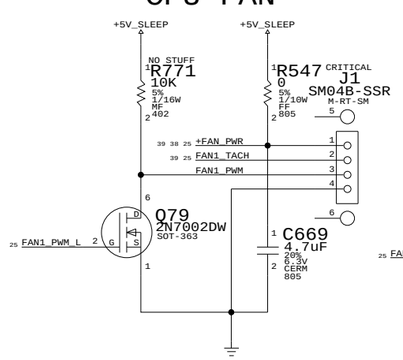


FAN INTERFACE

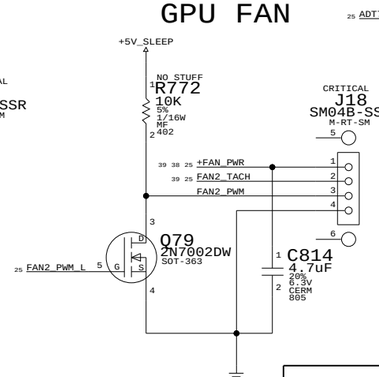
FAN CONTROLLER

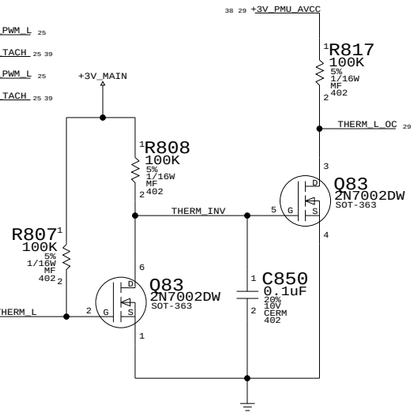


CPU FAN

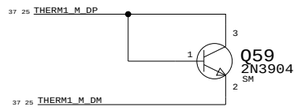


GPU FAN

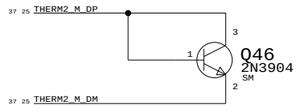




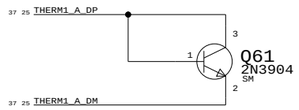
PLACE CLOSE TO CPU
MAIN1



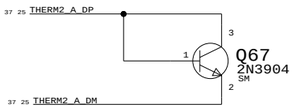
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



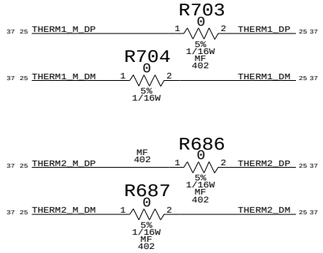
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



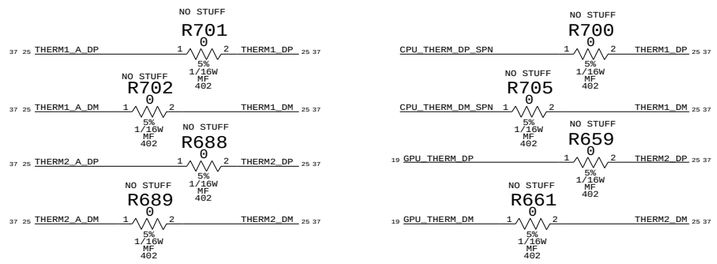
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



FAN/MODEM/SOUND/BACKUP BATT.

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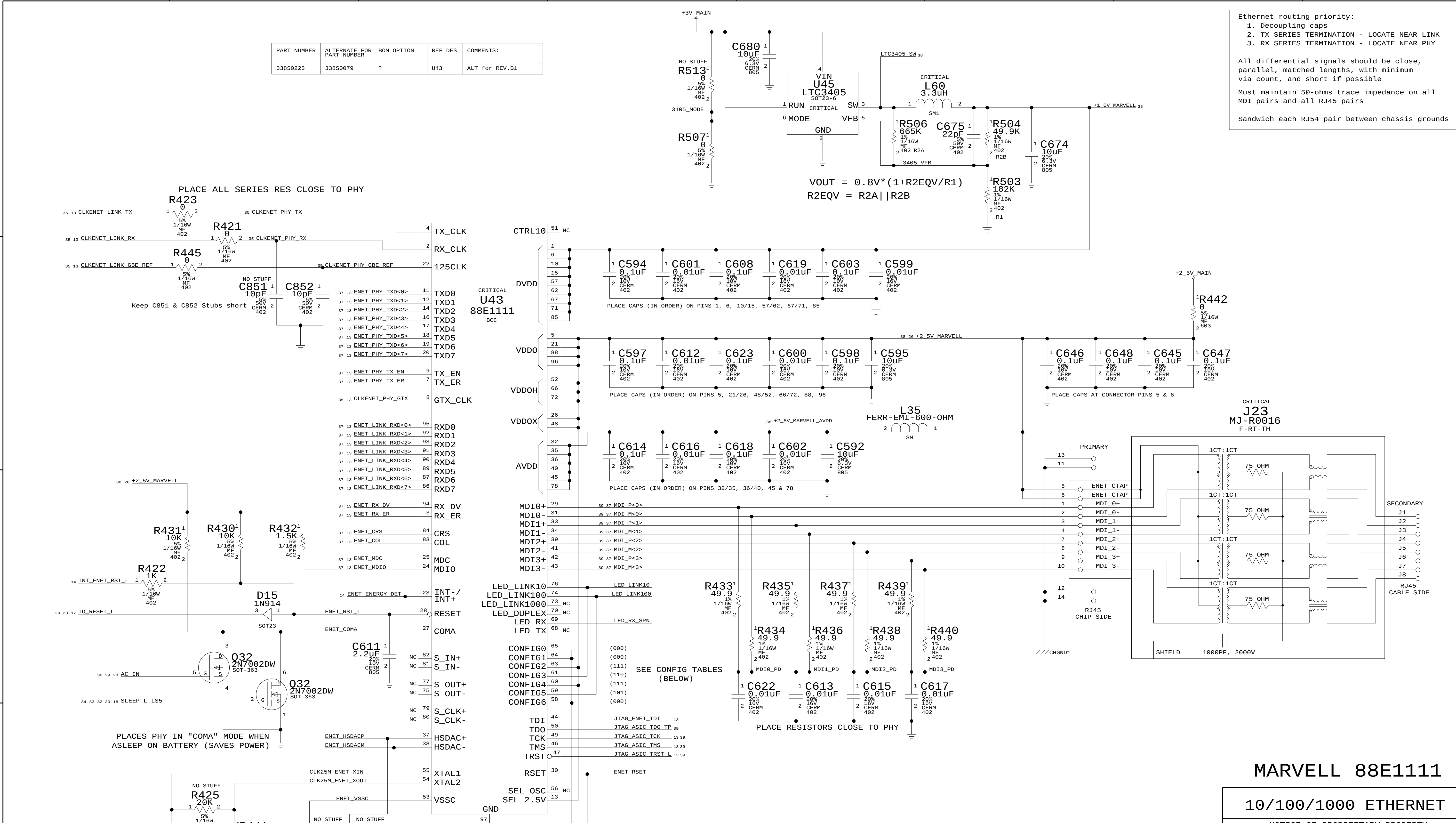
SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 25 OF 40	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U43	ALT for REV.B1

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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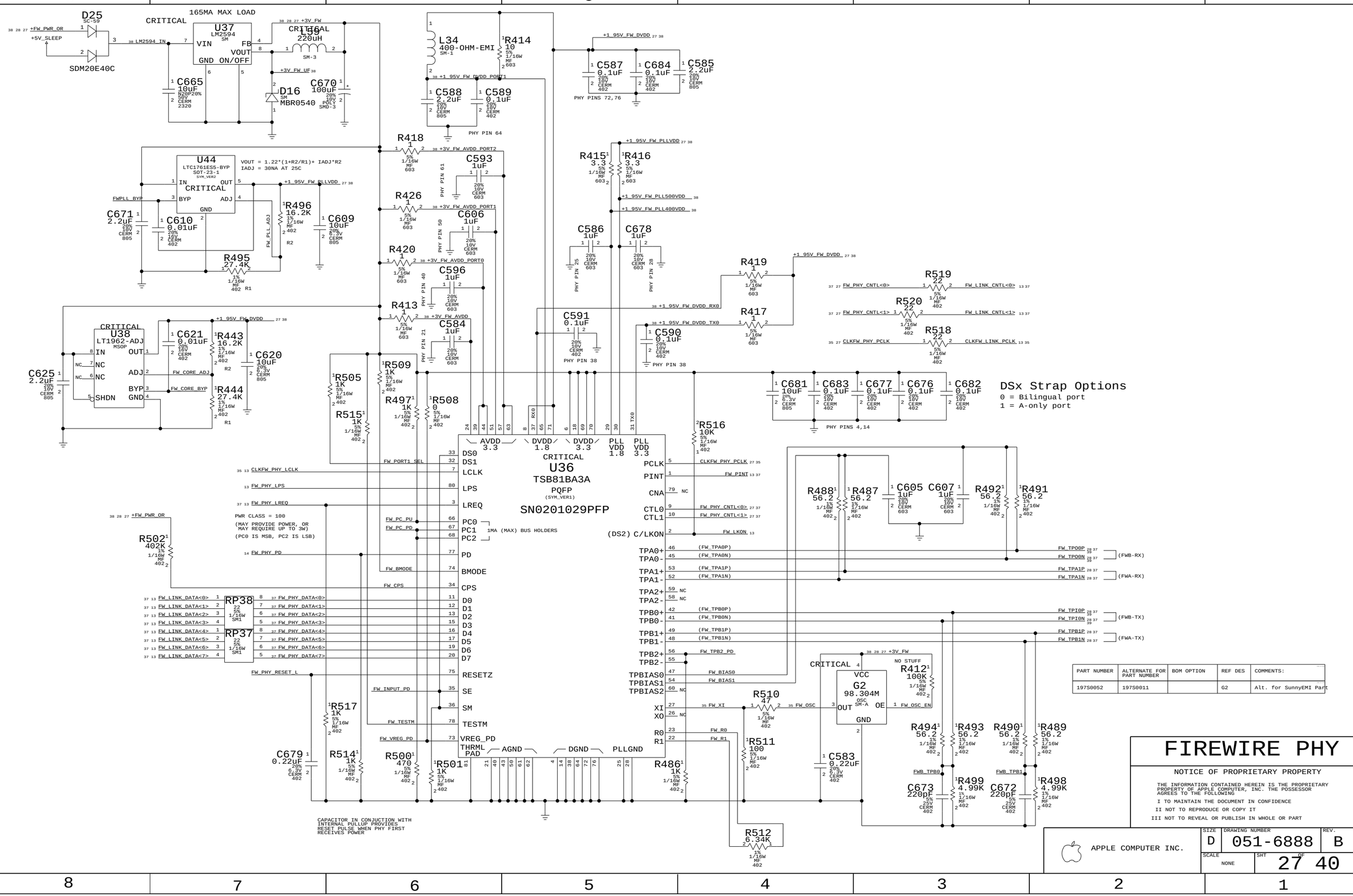
SIZE D | DRAWING NUMBER 051-6888 | REV. B
SCALE NONE | SHT 26 OF 40



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0052	197S0011		G2	Alt. for SunnyEMI Part

FIREWIRE PHY

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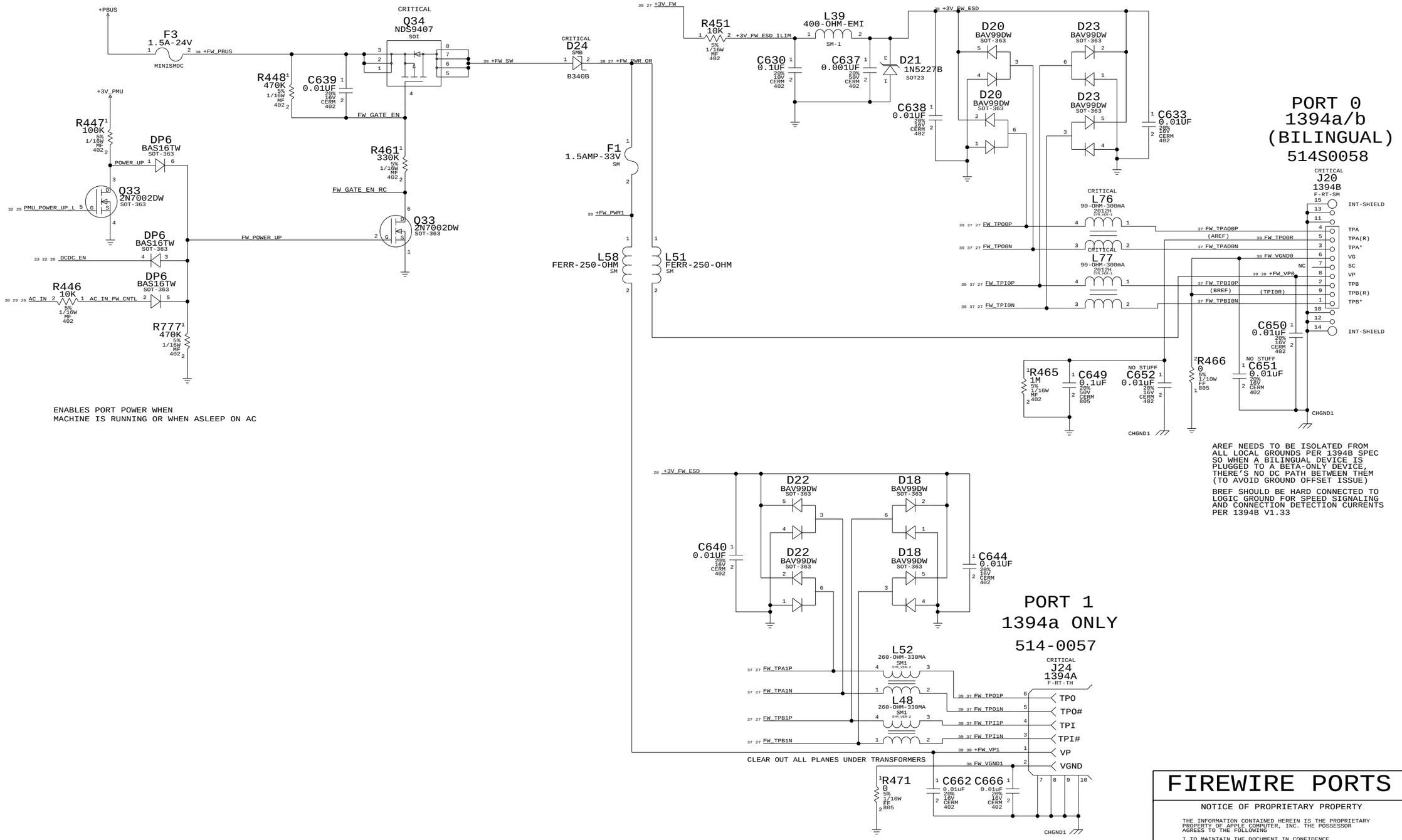
D	051-6888	B
SCALE: NONE	SHT 27 OF 40	

PORT POWER SWITCH



ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

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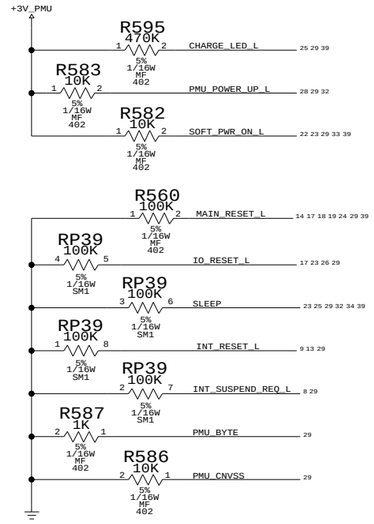
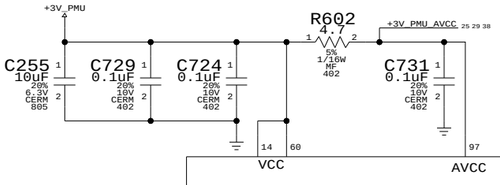
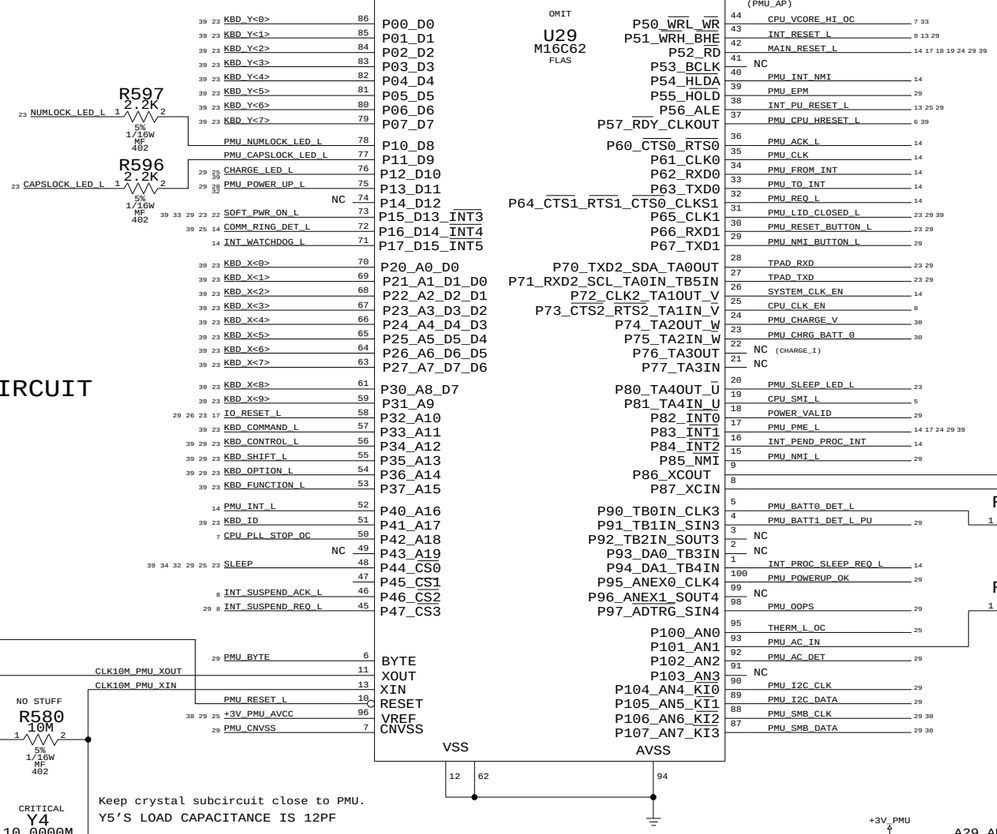
D	051-6888	B
SCALE: NONE	SHT 28 OF 40	

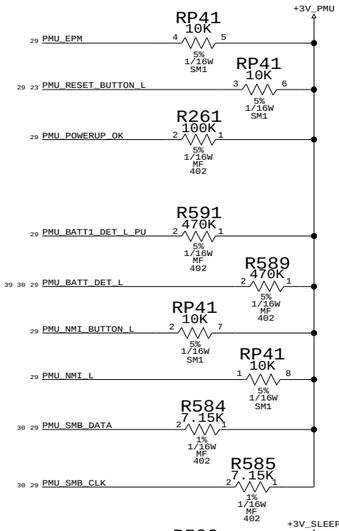




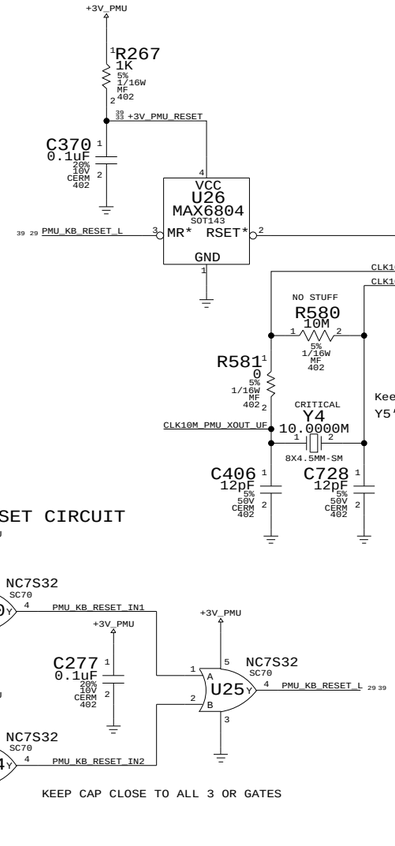
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. HLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.





UNDERVOLTAGE RESET CIRCUIT



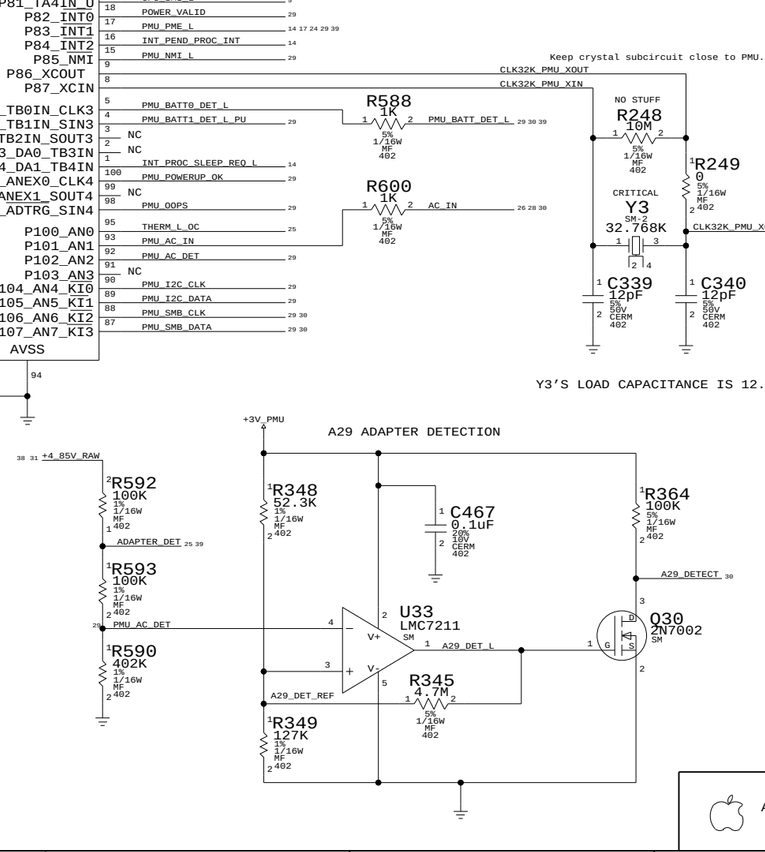
Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041		Y4	Alt. for Siward Part

PMU KEYBOARD RESET CIRCUIT

KEEP CAP CLOSE TO ALL 3 OR GATES

ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V



Keep crystal subcircuit close to PMU.
Y3'S LOAD CAPACITANCE IS 12.5PF

PMU

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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 29 OF 40	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/10W MF 402

C11 0.1uF 20% 50V CERM 805

GATE

AC_ENABLE_GATE

R51 20K 1% 1/16W MF 402

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/10W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

1V20_REF

U1 LMC7211 SM

AC_DIV

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

R41 1M 5% 1/16W MF 402

AC_IN

AC_IN_L

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

Q1 2N7002DW SOT-363

GREATER THAN 13.1V DETECT

BACKFEED PROTECTION

+ADAPTER_SW

Q69 SI4435DY SOI

GATE

+ADAPTER_SENSE

BKFD_PROT_GATE

R732 47K 5% 1/16W MF 402

C803 0.1uF 20% 16V CERM 402

R734 68K 5% 1/16W MF 402

BKFD_PROT_EN_L

Q9 2N7002DW SOT-363

AC_IN

CRITICAL
U3 MAX4172 TSSOP

RS+ RS- PG NC OUT GND

NC NC

MAX4172_OUT

CRITICAL
R77 2.21K 0.1% 1/16W MF 603

C36 0.01uF 20% 50V CERM 603

+24V_PBUS

PLACE U24 NEXT TO R382

CRITICAL
R61 0.025 1% 1W MF 2512

R82 4.7 5% 1/4W MF 402

R87 4.7 5% 1/4W MF 402

1772_CSSP

1772_CSSN

C71 0.47uF 10% 16V CERM 1206

C95 0.47uF 10% 16V CERM 1206

CSSP CSSN

U6 MAX1772 QSOP

DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CLS GND

CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT

1772_DCIN 1772_ACIN 1772_ACOK_L (+3V_PMU) 1772_VCTL 1772_ICTL 1772_ICHG 1772_IINP 1772_CCV 1772_CCI 1772_CCS 1772_REF 1772_CLS 1772_GND

1772_CELLS 1772_DLOV 1772_BST 1772_DHI 1772_LX 1772_DLO (GND) 1772_CSIP 1772_CSIN

C41 1uF 20% 16V CERM 603

C98 0.1uF 20% 25V CERM 603

C99 0.1uF 20% 25V CERM 603

R56 1K 1% 1/10W MF 402

R55 1K 1% 1/16W MF 402

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

1772_CCV_RC

C24 0.1uF 10% 16V CERM 402

R83 1K 1% 1/16W MF 402

C23 1uF 20% 10V CERM 603

R54 10K 1% 1/16W MF 402

R53 4.12K 1% 1/16W MF 402

R94 100K 5% 1/16W MF 402

XW1 SM

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

IAC_RC_COMP

C798 0.1uF 20% 16V CERM 402

+3V_PMU

C794 0.1uF 20% 16V CERM 402

R745 42.2K 0.1% 1/16W FF 603

IAC_FB

U55 LMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP

ADAPTER_I_REG

R727 10K 1% 1/16W MF 402

Place close to RS-

C826 0.01uF 20% 50V CERM 603

CURRENT_THRESHOLD

R736 42.2K 0.1% 1/16W FF 603

R738 82.5K 0.1% 1/16W FF 603

R742 51.1K 0.1% 1/16W FF 603

A29_CURRENT_ADJ

Q2 2N7002DW SOT-363

R744 100K 5% 1/16W MF 402

OVER_18V_ADJ

Q74 2N7002DW SOT-363

AC_GTR_18V

Q74 2N7002DW SOT-363

1772_ACOK_L

A29_DETECT

C809 1uF 20% 16V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+BATT

+24V_PBUS

F5 5AMP-125V SM-2

+PBUS

F4 5AMP-125V SM-2

+BATT_24V_FUSE

+BATT_14V_FUSE

Q6 SI4435DY SOI

GATE

Q7 SUD45P03 TO-252

R716 47K 5% 1/10W MF 402

R710 47K 5% 1/10W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

BATT_24PBUS_EN

BATT_14PBUS_EN

DP1 BAS16TW SOT-363

AC_IN_L

DP1 BAS16TW SOT-363

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

AC_IN_L_RC

C118 10uF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

R731 1K 1% 1/16W MF 402

BATT_LOW_L

BATTV_HIGH

R59 100K 5% 1/16W MF 402

Q4 2N7002DW SOT-363

BATTV_LOW

R75 5.23K 1% 1/16W MF 402

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

Q4 2N7002DW SOT-363

PMU_CHARGE_V

R741 100K 5% 1/16W MF 402

CHARGE_DISABLE

Q72 2N7002DW SOT-363

Q72 2N7002DW SOT-363

PMU_CHRG_BATT_0

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

C799 0.1uF 20% 16V CERM 402

U57 LMC7211 SM

R729 100K 1% 1/10W MF 402

R740 499K 1% 1/16W MF 402

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

BATT_LOW

A29_DETECT

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

Q2 2N7002DW SOT-363

+BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

+BATT_POS

(BATT_IN_PD)

BATT_CLK

BATT_DATA

PMU_BATT_DET_L

BATT_NEG

L5 FERR-EMI-100-OHM SM

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA

L2 FERR-50-OHM SM

R725 33 5% 1/8W FF 1206

D6 1N914 SOT23

1772_BST_ESR

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

C96 0.1uF 10% 50V CERM 805

CRITICAL
Q70 IRF7805 SM

C112 2.2uF 10% 50V CERM 1812

C117 2.2uF 10% 50V CERM 1812

C113 2.2uF 10% 50V CERM 1812

C115 2.2uF 10% 50V CERM 1812

C116 2.2uF 10% 50V CERM 1812

CRITICAL
L70 10uH SM1

+BATT_RSNS

R715 0.05 1% 1W MF 2512

D36 SM MBRS140T3

CRITICAL
Q64 IRF7811W SO-8

NO STUFF
C853 1000pF 10% 16V X7R 402

C780 4.7uF 20% 25V CERM 1206

C795 4.7uF 20% 25V CERM 1206

C790 4.7uF 20% 25V CERM 1206

C779 33uF 20% 25V ELEC SM1

R720 1 5% 1/16W MF 603

R713 1 5% 1/16W MF 603

C777 4.7uF 20% 25V CERM 1206

C792 4.7uF 20% 25V CERM 1206

C785 4.7uF 20% 25V CERM 1206

BATTERY CHARGER

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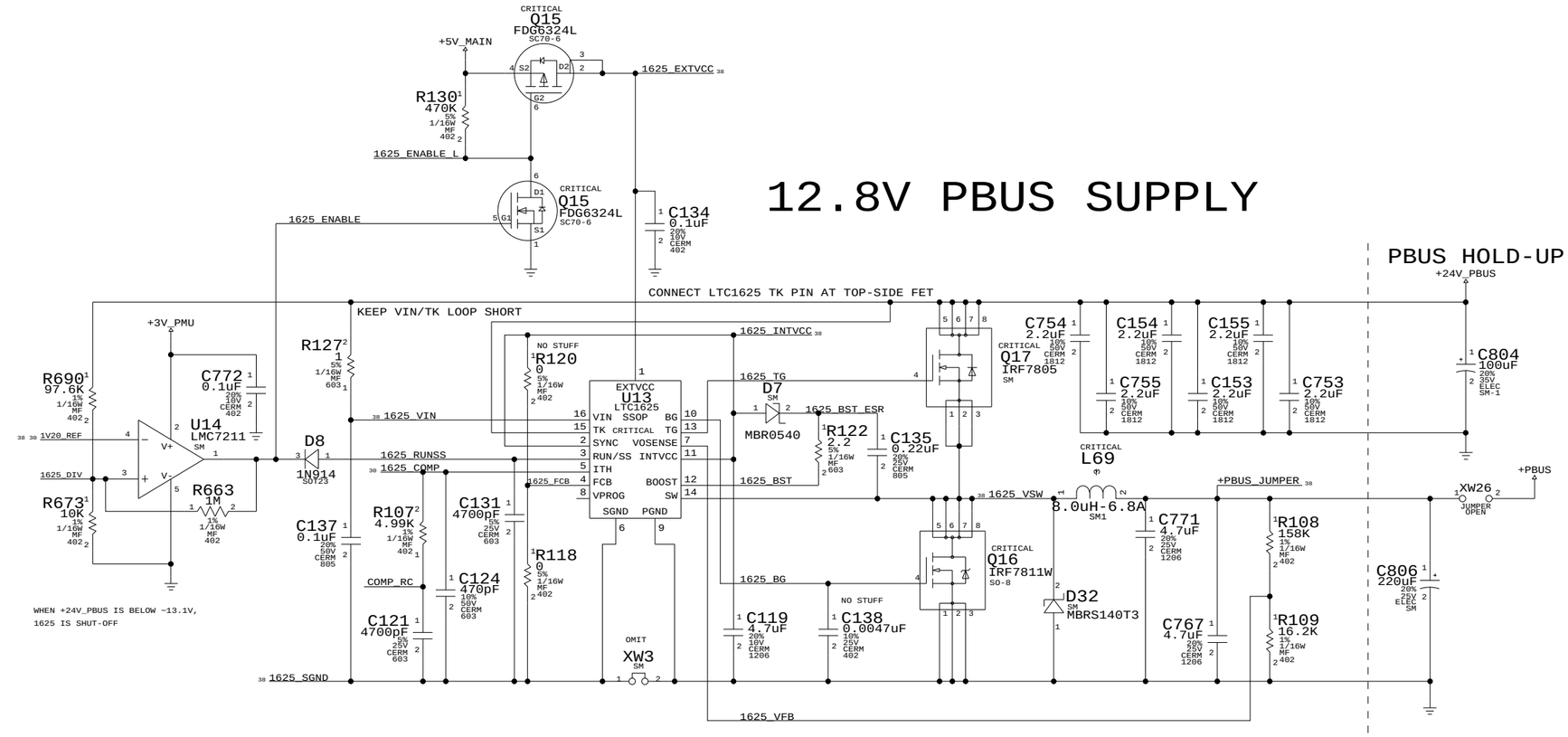
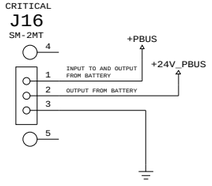
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 30 OF 40	

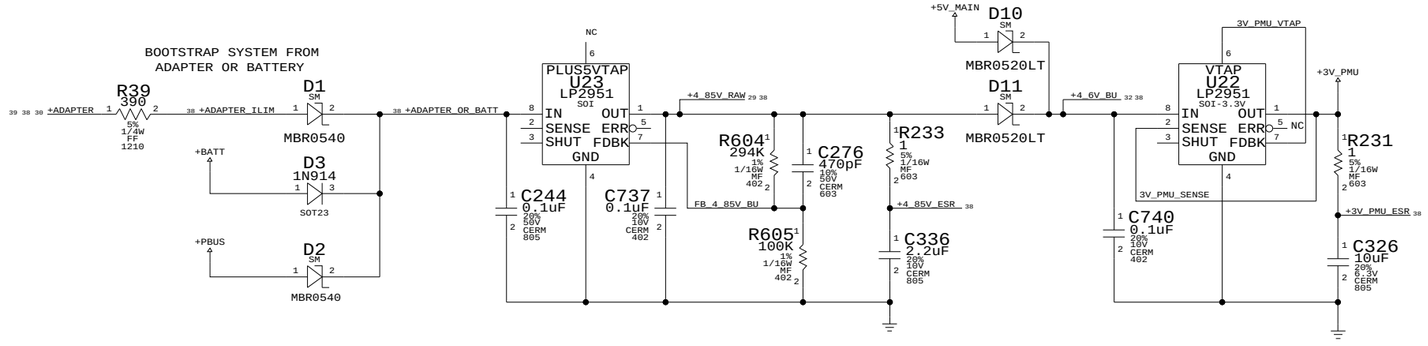
12.8V PBUS SUPPLY



BACKUP BATTERY



PMU SUPPLY



12.8V REGULATOR

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 31 OF 40	

3.3V/5V MAIN SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L

3V START TO TURN ON ~25MS AFTER DCDC_EN_L

DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN

POWERDOWN DELAY IS AROUND 4MS-15.6MS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

3.3V/5V REGULATOR

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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 32 OF 40	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V->1.025V

1.300V->1.075V
1.225V->1.050V
(value without offset)

1.25Ghz
1.0Ghz

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

Sense resistor R650 may not be needed!

Keep trace fat and short!!

(VCORE=1.385V for EVTB)

Keep trace fat and short!!

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

(For BEST config. R65 use 0-ohm RES,see BOM table)

Note:No stuff R67 to set skip mode of VCore

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.25Ghz 1.335V->1.080V
1.0Ghz 1.235V->1.060V

Connect MAX1717 GND pin 13
to GND at bottom-side FET

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

ROUTE AS DIFFERENTIAL PAIR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C774,C781,C788,C793,C797,C802	

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

Fmax Test Connections

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1000	1	RES,MF,0 ohm,5%,1/16W,0402,SMD	R65	?	CPU_BST
114S3573	1	RES,MF,1/16W,3.57K ohm,1%,0402,SMD	R97	?	CPU_BST

VCORE SUPPLY

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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE: NONE	SHT 33 OF 40	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M10 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6888 | REV. B

SCALE NONE | SHT 34 OF 40

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

T231	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	5	19 20
T233	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	5	19 20
T232	GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20
T234	GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20
T235	GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20
T236	GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20
T238	GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20
T237	GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	8	19 20

T240	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	5	19
T239	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	5	19
T242	SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19
T241	SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19
T243	SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19
T245	SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19
T244	SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19
T246	SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

T263	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610				19 20
T265	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000				19 20
T264	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000				19 20
T267	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000				19 20
T266	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::			19 20
T255	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700				19
T256	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000				19
T260	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000				19
T261	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000				19
T262	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::			19

T268	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22 39
T269	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22 39
T271	TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22
T270	TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22
T272	TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22
T273	TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22
T274	TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22
T275	TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	L:S:1650:1450	7					66 MHZ	12 19
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP BYTES 2-3	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ	12 19
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ	12 19
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	7					66.00 MHZ	12 19
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_PAR	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	9 12 17 18 24 39
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	12 17 18 24
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ	13 24
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL			(200)			100.0 MHZ	13 24
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ	13 24
	UIDE_ADDR<2..0>	L:S::650			(200)			100 MHZ	13 24
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ	13
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ	13
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ	24
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	13 24
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ	13 24
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ	13 24
	EIDE_ADDR<2..0>	L:S::850						33 MHZ	13 24
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_INT	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ	13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_RX_DV	L:S:8000 MIL:9000 MIL							13 26
	ENET_RX_ER	L:S:8000 MIL:9000 MIL							13 26
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_LINK_TXD<7..0>	L:S::600							13
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL	7						13 26
	ENET_LINK_TX_ER	L:S::400 MIL							13
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL	7						13 26
	ENET_LINK_TX_EN	L:S::400 MIL							13
	ENET_MDIO	L:S:8000 MIL:9000 MIL							13 26
	ENET_MDC	L:S:8000 MIL:9000 MIL							13 26
	ENET_COL	L:S:8000 MIL:9000 MIL							13 26
	ENET_CRS	L:S:8000 MIL:9000 MIL							13 26
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)			13 27
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)			27
	FW_LINK_CNTL<1..0>	L:S:9000:10000							13 27
	FW_PHY_CNTL<1..0>	L:S::300							27
	FW_LINK_LREQ	L:S::300 MIL							13
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL							13 27
	FW_PINT	L:S:8500 MIL:9500 MIL							13 27

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_DN<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_DN<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
USB 1.1 Zo = 90	ATI_TMDS_DP<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
USB 2.0 Zo = 90	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.6MIL (TRACE WIDTH)
S = 7MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	I311 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	I357 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	I356 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	I358 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	I308 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA
INVERTER
TRACKPAD
LVDS

Net	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
(ground)	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	I333 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	I346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	I347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	I348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	I349 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	I351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	I352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	I354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	I355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	I360 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	I361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
NEC USB2.0	I316 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	I317 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	I332 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	I312 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	I310 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I314 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I359 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	I315 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14

SIGNAL CONSTRAINTS - PAGE 3

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FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	I2	JTAG_ASIC_TMS	TRUE			13 26
	I3	JTAG_ASIC_TDI	TRUE			13
	I1	JTAG_ASIC_TDO_TP	TRUE			26
	I4	JTAG_ASIC_TCK	TRUE			13 26
	I6	JTAG_ASIC_TRST_L	TRUE			13 26
	I5	CPU_CHKSTP_OUT_L	TRUE			5
	I7	CPU_SRESET_L	TRUE			5
	I9	CPU_HRESET_L	TRUE			5 6 7
	I8	JTAG_CPU_TMS	TRUE			5 6
	I10	JTAG_CPU_TDI	TRUE			5 6
	I12	JTAG_CPU_TDO_TP	TRUE			5
	I11	JTAG_CPU_TCK	TRUE			5 6
	I13	JTAG_CPU_TRST_L	TRUE			5 6
	I18	INT_JTAG_TEI	TRUE			13
	I20	INT_TST_MONIN_PD	TRUE			13
	I19	INT_TST_MONOUT_TP	TRUE			13
	I21	INT_TST_PLLEN_PD	TRUE			13
INT I2C	I15	INT_I2C_CLK0	TRUE			6 11 13 23
	I14	INT_I2C_DATA0	TRUE			6 11 13 23
	I16	INT_I2C_CLK1	TRUE			13 14 25
	I17	INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	I211	+PBUS	TRUE			38
	I216	+24V_PBUS	TRUE			38
	I25	GPU_VCORE	TRUE			19 20 38
	I24	1778_VFB	TRUE			20 38
	I27	CPU_VCORE_SLEEP	TRUE			5 33 38
	I26	VCORE_FB	TRUE			33 38
	I213	+1_8V_MAIN	TRUE			38
	I218	+2_5V_MAIN	TRUE			38
	I219	+5V_MAIN	TRUE	2		38 39
	I220	+5V_SLEEP	TRUE	2		38 39
	I221	+3V_MAIN	TRUE	4		23 38
			TRUE		1000	IN
	I222	+3V_PMU	TRUE			38
CARDBUS	I36	CBUS_DET_1_L	TRUE		2000	18
	I35	CBUS_DET_2_L	TRUE		2000	18
DVI	I37	TMDS_DN<0..2>	TRUE		1000	19 22 37
	I38	TMDS_DP<0..2>	TRUE		1000	19 22 37
	I40	TMDS_CONN_CLKN	TRUE		1000	22 36
	I39	TMDS_CONN_CLKP	TRUE		1000	22 36
	I42	VGA_R	TRUE		1000	22
	I41	VGA_G	TRUE		1000	22
	I44	VGA_B	TRUE		1000	22
	I43	VGA_HSYNC	TRUE		1000	22
	I46	VGA_VSYNC	TRUE		1000	22
	I45	DVI_DDC_CLK_UF	TRUE		1000	22
	I47	DVI_DDC_DATA_UF	TRUE		1000	22
	I48	DVI_HPD_UF	TRUE		1000	22
	I49	+5V_DDC_SLEEP	TRUE		2000	22 38
			TRUE	2	2000	IN
CHGND1			TRUE	6	1000	IN
LVDS	I62	LVDS_L0N	TRUE		1000	20 22 37
	I51	LVDS_L0P	TRUE		1000	20 22 37
	I53	LVDS_L1N	TRUE		1000	20 22 37
	I55	LVDS_L1P	TRUE		1000	20 22 37
	I64	LVDS_L2N	TRUE		1000	20 22 37
	I57	LVDS_L2P	TRUE		1000	20 22 37
	I56	CLKLVDS_LN	TRUE		1000	20 22 37
	I58	CLKLVDS_LP	TRUE		1000	20 22 37
	I59	LVDS_DDC_CLK	TRUE		1000	20 22
	I60	LVDS_DDC_DATA	TRUE		1000	20 22
	I62	+3V_LCD	TRUE	2	2000	22 38
	I223	+3V_SLEEP	TRUE		2000	38 39
			TRUE	2	2000	IN
CHGND4			TRUE	6	1000	IN
INVERTER	I67	+14V_INV	TRUE		2000	22 38
	I66	+5V_INV_SW	TRUE		2000	22 38
	I68	BRIGHT_PWM	TRUE		2000	22
	I249	INV_GND	TRUE		2000	22
			TRUE		1000	IN
S-VIDEO	I70	TV_C	TRUE		2000	22
	I72	TV_Y	TRUE		2000	22
	I71	TV_COMP	TRUE		2000	22
	I73	TV_GND1	TRUE		2000	22 38
	I74	TV_GND2	TRUE		2000	22 38
LIO	I76	INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	I75	INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	I78	INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	I83	INT_I2S0_SND_SCLK	TRUE		1000	14 25
	I82	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	I77	SND_HP_MUTE_L	TRUE		1000	14 25
	I79	SND_AMP_MUTE	TRUE		1000	25
	I84	SND_HW_RESET_L	TRUE		1000	14 25
	I85	SND_HP_SENSE_L	TRUE		1000	14 25
	I86	SND_LIN_SENSE_L	TRUE		1000	14 25
	I81	INT_I2C_CLK2	TRUE		1000	14 25
	I80	INT_I2C_DATA2	TRUE		1000	14 25
	I87	ADAPTER_DET	TRUE		1000	25 29
	I88	CHARGE_LED_L	TRUE		1000	25 29
	I89	NEC_LUSB_OCI_UF	TRUE		1000	17 25
	I90	NEC_LUSB_PPON	TRUE		1000	17 25
	I222	+5V_MAIN	TRUE	2	2000	38 39
	I228	+5V_SLEEP	TRUE	2	3000	38 39
	I220	+3V_SLEEP	TRUE		2000	38 39

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	I94	NEC_USB_DAM	TRUE			17 25 37
	I92	NEC_USB_DAP	TRUE			17 25 37
	I95	NEC_USB_DBM	TRUE			17 25 37
	I97	NEC_USB_DBP	TRUE			17 25 37
	I98	BT_USB_DM	TRUE			14 25 37
	I96	BT_USB_DP	TRUE			14 25 37
	I101	MODEM_USB_DM	TRUE			14 25 37
	I100	MODEM_USB_DP	TRUE			14 25 37
RT. USB	I102	NEC_RUSB_PPON	TRUE			17 25
	I103	NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	I105	PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	I106	PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	I108	PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	I107	PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	I109	PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	I110	PCI_STOP_L	TRUE		1000	12 17 18 24 37
	I111	PCI_PAR	TRUE		1000	12 17 18 24 37
	I112	AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	I113	AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	I114	AIRPORT_PCI_INT_L	TRUE		1000	14 24
	I115	MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	I116	CLK33M_AIRPORT	TRUE		1000	12 24 35
	I118	PMU_PME_L	TRUE		1000	14 17 24 29
	I119	ROM_ONBOARD_CS_L	TRUE		1000	9 24
	I121	ROM_OE_L	TRUE		1000	9 12 24
	I122	ROM_CS_L	TRUE		1000	9 12 24
	I124	ROM_RW_L	TRUE		1000	9 12 24
	I227	RF_DISABLE_L	TRUE		1000	24
	I230	AIRPORT_CLKRUN_L	TRUE		1000	24
	I120	+3V_AIRPORT	TRUE	4	2000	38
			TRUE	6	1000	IN
OPTICAL	I126	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	I125	EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	I129	EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	I128	EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	I127	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	I131	EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	I130	EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	I133	EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	I134	EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	I132	EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	I135	EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	I139	+5V_TPAD_SLEEP	TRUE		3000	23 38
	I138	TPAD_F_TXD	TRUE		3000	23
	I136	TPAD_F_RXD	TRUE		3000	23
	I137	LID_CLOSED_L	TRUE		3000	23
	I139	+3V_HALL_EFFECT	TRUE		3000	23 38
	I139	SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	I141	COMM_RESET_L	TRUE		4000	14 25
	I140	COMM_SHUTDOWN	TRUE		4000	14 25
	I142	COMM_RING_DET_L	TRUE		4000	14 25 29
	I144	COMM_TXD_L	TRUE		4000	14 25
	I143	COMM_TRXC	TRUE		4000	14 25
	I146	COMM_GPIO_L	TRUE		4000	14 25
	I145	COMM_DTR_L	TRUE		4000	14 25
	I147	COMM_RTS_L	TRUE		4000	14 25
	I148	COMM_RXD	TRUE		4000	14 25
KEYBOARD	I149	KBD_ID	TRUE		3000	23 29
	I150	KBD_INTL	TRUE		3000	23
	I151	KBD_JIS	TRUE		3000	23
	I152	KBD_CAPSLOCK_LED	TRUE		3000	23
	I153	KBD_NUMLOCK_LED	TRUE		3000	23
	I154	KBD_FUNCTION_L	TRUE		3000	23 29
	I155	KBD_COMMAND_L	TRUE		3000	23 29
	I156	KBD_OPTION_L	TRUE		3000	23 29
	I157	KBD_CONTROL_L	TRUE		3000	23 29
	I158	KBD_SHIFT_L	TRUE		3000	23 29
	I159	KBD_X<0..9>	TRUE		3000	23 29
	I160	KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	I161	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	I162	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	I163	BATT_CLK	TRUE		1000	30
	I164	BATT_DATA	TRUE		1000	30
	I165	PMU_BATT_DET_L	TRUE		1000	29 30
FANS	I167	+FAN_PWR	TRUE		3000	25 38
	I168	FAN1_TACH	TRUE		3000	25
	I169	FAN2_TACH	TRUE		3000	25
	I170	FAN1_GND	TRUE		3000	38
	I171	FAN2_GND	TRUE		3000	38
ETHERNET	I172	MDI_P<0..3>	TRUE		1000	26 37
	I173	MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	I177	FW_TPO0P	TRUE		1000	27 28 37
	I176	FW_TPO0N	TRUE		1000	27 28 37
	I175	FW_TPO0R	TRUE		1000	28
	I179	FW_TPI0P	TRUE		1000	27 28 37
	I180	FW_TPI0N	TRUE		1000	27 28 37
	I182	+FW_VP0	TRUE		1000	28 38
	I181	FW_VGND	TRUE		1000	39

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	I183	FW_TPO1P	TRUE		1000	28 37
	I184	FW_TPO1N	TRUE		1000	28 37
	I185	FW_TPI1P	TRUE		1000	28 37
	I186	FW_TPI1N	TRUE		1000	28 37
	I187	+FW_VP1	TRUE		1000	28 38
	I188	FW_VGND	TRUE		1000	39
DC PWR IN	I190	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	I234	ST7_SLEEP_LED_H	TRUE			23
	I235	PMU_SLEEP_LED	TRUE			23
	I236	PMU_LID_CLOSED_L	TRUE			23 29
	I242	LMU_DETECT	TRUE			23
			TRUE	6	1000	IN
MISC.				(100 MIL PROBE PREFERRED)		
	I192	SLEEP_LED	TRUE			23
	I193	PMU_KB_RESET_L	TRUE			29
	I194	SLEEP	TRUE			23 25 29 32 34
	I195	PMU_CPU_HRESET_L	TRUE			6 29
	I196	BB_RESET_L	TRUE			6
	I240	+3V_PMU_RESET	TRUE			29 33

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6888 | REV. B

SCALE NONE | SHT 39 OF 40

REVISION HISTORY

Proto Release

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7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
          Added P59 SO-DIMM connector as placeholder (p.12)
          Added P59 LVDS connector as placeholder (p.22)
          Changed J9 to 10 pin Elco connector for modem (p.25)
          Changed PBUS holdup caps to P59 electrolytic cans (p.30)
7/23/02 - Removed L3 (p.8)
          Replaced processor with 360 pin Apollo (p.5,6)
7/24/02 - Added FETs between battery and PBUS rails for airline power (p.29)
8/10/02 - Added USB 2.0 (p.18)
8/20/02 - Removed spare pullup straps for Intrepid (p.9)
          Removed USB overcurrent protection [to be placed on other boards] (p.18)
          Changed right USB board connector to 16 pin Hirose connector (p.26)
          Changed LIO board connector to 40 pin Molex connector (p.26)
          Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)
8/26/02 - Removed 32 bypass caps for +3V_MAIN at Intrepid (p.16)
          Removed 5 bypass caps for +2_5V_MAIN at Intrepid (p.16)
          Removed 3 bypass caps for +1_5V_AGP at Intrepid (p.16)
          Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)
8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)
8/29/02 - Added dedicated Boot Banger circuit (p.6)
          Added 5 bypass caps to each SO-DIMM connector (p.11)
          Added quad voltage circuit for bus slewing architecture (p.32)
8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28)
          Changed to Q11 adpater detection scheme (p.28)
9/03/02 - Corrected upper LVDS single pin nets (p.20)
          Removed unintentional extra pulldown resistor at Intrepid (p.14)
9/17/02 - Numerous changes to stay in sync with P84 (all)
9/18/02 - Changed battery connector back to P84 part (p.29)
          Added LMU circuitry to eliminate extra board (p.23)
          Changed to P84 dual channel LVDS connector to reduce I2R cable losses(p.22)
9/19/02 - Removed unnecessary battery FETs [due to 3S only design] (p.29)
          Modified chassis gnds on some components (all)
          Removed LMU connector (p.23)
          Corrected battery connector [same as P84] (p.29)
          Removed P93 support (p.25)
          Removed second fuse from FW ports [single fuse provides adequate power] (p.27)
9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
          Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)
9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
          Swapped pins on L33, L35 for layout (p.31)
          Changed Y6 to smaller form-factor crystal (p.26)
9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
          Corrected holes and chassis gnds (p.4,all)
10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accomodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Clamped NEC NC pins high per documentation (p.17)
           Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
           Added SSCG/NO_SSCG stuffing options for CY28512 circuit (p.14)
           Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
           Removed Zebra 15/16 support per P84 (p.27)
           Added second FW port power fuse (p.27)
           Removed INT_CPUFB_IN cap per P84 (p.8)
           Replaced IRF7822 FETs with IRF7811W in battery charger and 14V PBUS switchers (p.29,30)
           Renamed optical interface for consistency (p.24,37)
           Corrected PLL_CFG<4> for Apollo 7 [needs to always be zero] (p.5,7)
           Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
           Added stuffing options to power fans off 3V or 5V (p.25)
10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)
10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)
10/15/02 - Moved FireWire connectors and port power switch to separate page (p.28)
           Changed SMBus pullups to 7.15K, 1% as per iBooks/P84 [involved component net swaps] (p.29)
           Added 0603 resistors as shorting pads for power up and reset (p.23)
           Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
           Added damping resistor option to LMU crystal (p.23)
           Changed INT_TST_PLLEN_PD to pulldown only [LA clk not used] (p.13)
           Changed JTAG_ENET_TDI to pullup [LA clk not used] (p.13)
           Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
           Changed BBANG_HRESET_L pullup to 3V_SLEEP (p.6)
           Changed FW_PC_PD, FW_PC_PU resistors to 5% (p.27)
           Added 1K pulldown and net FW_PD2 to FW PHY (p.27)
10/16/02 - Implemented new FW power switch and current limit (p.28)
           Renamed +14V_PBUS to +PBUS (p.all)
           Added A29 adapter detection circuit (p.29)
           Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
           Changed FW PHY pin DS1 to pullup to make Port 1 1394a only (p.27)
10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
           Changed keyboard ZIF to large SMK connector (p.23)
           Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)
10/22/02 - Mirrored wireless connector for P50 flex (p.24)
10/23/02 - Changed LMU/sleep LED interface per p84 (p.23)
           Changed LMU JTAG/I2C pinout/pullup/pulldown strategy per P84 (p.23)
           Changed fan FETs to SI3446DV per P84 (p.25)
           Pinned out audio connector (p.25)
           Pinned out right USB connector (p.25)
           Pinned out modem connector (p.25)
           Added 2 functional test points to wireless connector (p.24,38)
           Renamed FW low voltage power rails (p.27,37)
           Renamed Vcore VID nets to be consistent with P84 (p.33)
           Removed redundancy in DDR memory constraints (p.35)
10/24/02 - Changed FW DS2 strap to pullup to shut off port 2 (p.27)
           Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14)
           Updated PCI clock series R values per P84 (p.12)
           Changed power rail for ALS to +3V_MAIN per P84 (p.23)
           Added 0 ohm short and bypass cap for GPU VDDDVO per P84 (p.21,37)
           Split FW_VGND into FW_VGND0 and FW_VGND1 (p.28,37)
           Added TP nets to GPU for XOR-tree testing (p.19-21)
           Changed fan PWM output pullups to +3V_SLEEP to prevent pump-up (p.25)
10/28/02 - Added FW thermal pad ground hole back in (p.27)
           Repinned LMU pulldown for layout (p.23)
10/30/02 - Changed fan power rails to common net (p.25)
10/31/02 - Removed MLB ALS (p.23)
           Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)
11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
           Broke out quad OR-gate to discrete components for better placement (p.22,29)
11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
           Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
           Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
           Removed XW17, jumper for CPU_VCORE_SLEEP (p.33)
           Added decoupling cap to PMU reset OR gates (p.29)
11/08/02 - Changed FireWire PHY to Z17 (p.27)
           Added bulk caps to fan connectors (p.25)
           Added alternate chassis gnd connection for sleep LED (p.23)
11/11/02 - Removed +3V_MAIN option for P50 card (p.24)
11/13/02 - Removed LMU and associated circuitry (p.23)
11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18)
11/25/02 - Renamed all components (all pages)
11/26/02 - Removed chokes from 1394b data pairs (p.27,28)
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EVT RELEASE

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12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
           Replaced ADM1031 with ADT7460 [I2C Address Change!] (p.25)
           Added ADT7460 hookups to GPU thermal diode (p.21,25)
           Added FireWire B ESD protection circuits (p.28)
12/16/02 - Removed hole from FireWire ground pad (p.27)
           DDR memory connector renamed to J25 (p.11)
12/20/02 - Removed LT4210 from FireWire port power (p.28)
           Added F10,F20 as placeholders and experiment guides (p.28)
           Added diodes to OR +5V_SLEEP into FW PHY power supply (p.27)
12/26/02 - Updated CPU p/ns to production p/ns (p.5)
           Removed RC glitch filter on CPU_DRDY_L (p.5,36)
           Updated PCI source clock and internal spreading straps (p.8)
           Changed BootROM PWD signal to INT_RESET_L per P84 (p.9)
           Added CKE pulldowns per P84 (p.9)
           Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
           Updated SSCG/NO_SSCG BOM options (p.14)
           Renamed line-in and headphone sense lines to reflect active low signals (p.14,25.39)
           Added 0 ohm Rs to make 2_5V Intrepid rail hot or cold (p.15.16,38)
           NO STUFFed entire 1.5V LDO circuit (p.15)
           Stuffed USB OCI RC filters for 0 time constant [due to new port current limiters] (p.17)
           Renamed USB OCI/PPON signals for left/right ports (p.17,39)
           Updated GPU VCore to stay in sync with P84 ["jitter" improvement] (p.20)
           Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25)
           Added R800,R801 for eventual thermal diode in CPU (p.25)
           Renamed R2000 to R799, R2001 to R802, R2002 to R803 (p.25)
           Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28)
           Added caps to FW ESD circuit that were missed (p.28)
           Changed MAX4172 power source to save current on battery [per P84] (p.30)
           Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
           Replaced all 132S1061 [1uF,0805,10V,20%] with 132S0046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
           Replaced all 138S0351 [1uF,0603,6.3V,10%] with 132S0046 [1uF,0603,10V,20%] (p.27,30)
01/02/03 - Updated FireWire fuse topology to that of P84 (p.28)
           Updated system and power block diagrams (p.2,3)
01/03/03 - Corrected +2_5V_INTREPID connections to muxes and reference (p.9,10)
01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)
01/08/03 - Added 2N7002 circuits to ensure speakers are muted during power-up (p.25)
           Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)
01/09/03 - Added required pulldown to output of DVI HPD sense comparator (p.22)
           Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
           Updated S-video filter values to those of P84 (p.22)
01/10/03 - ZT7,ZT23,ZT61,ZT76,ZT89,ZT87,ZT22,ZT38,ZT60,ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4)
01/13/03 - Add L53, L54, L55 for TMDS Data<0:2> Diff Pair (p.22)
01/14/03 - Add C812 - C821 (Totol 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
           Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
           Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
           Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
           Add R810 & R811 for ALWAYS-ON FANs in Acrylic Build (p.25)
01/28/03 - Remove NV31/17 components (p.19-21)
           Add M10 (p.19-21)
02/07/03 - Add Power Net Constraints for M10 (p.38)
           Replace Singing PBus Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121
           with 126S0035 (or alt. 126S0036) (p.33)
02/11/03 - Add FW Power Net Constraints (p.38)
           Change signal constraints for AGP signals (p.36)
           Add LMU connector and components (p.23)
           Edit I2C table for LMU (p.13)
           Change R580 to 19.6K (p.14)
           Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
           Change Ferrite Bean of ATI power supply to correct values (p.21)
           Remove C141 PBUS CAP (p.31)
02/12/03 - Change and Rotate Keyboard Connector (p.23)
           Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)
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EVT RELEASE (continue)

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02/13/03 - Add C825 (p.30)
02/17/03 - Rename all Reference Designators
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EVT ENCLOSURE RELEASE

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03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
           Add PU at PMU_SLEEP_LED_L for LMU (p.23)
           Change stuffing option for clock slewing & PLL5 (p.14)
           Change ATI M10 GPIO8 to Pull-down (p.20)
           Remove Memory MUX 0ohm Resistors (p.10)

03/28/03 - Due to MLB outline change at DVI connector, CHGND1 has to be splitted into
           CHGND1 & CHGND2 (P 4 & 22)
           Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32)
           R601 change from 100K to 4.7K (P 29)
           Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
           Add C826 at U3 RS- pin (P 30)
           Change D3 to 1N914 PN Junction Diode(P 31)

03/31/03 - Change AGPTEST Pull-up to 47ohm (it was 40ohm) (P 20)
           Add circuits to prevent start-up Headphone POP (P 25)
           Change all 1210 4.7uF to 1206 4.7uF Cap (138S0531) (various pages)
           Modify FAN circuit to PWM active low signal (P25)

04/08/03 - Add SOFT MODEM support (P 14 & 25)
           Add 10-Pin ELCO connector for Serial Debug Interface (P 25)
           Change Q7 from SI4435DY to SUD45P03-10 (P 30)
           Remove D34 RS3AB (P 30)

04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28)
           Change PBUS L69 and VCORE L71 Inductor (P 31 & 33)
           Change C643 10uF Cap to 1206 package part (P 28)
           Change all 6 VCORE Caps to 220uF Al Poly Cap 128S0024 (P 33)
           Add Mitsumi MM1571J regulator to provide 1.8V TPVDD (P 21)
           Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail(P 21)

04/16/03 - Add FW Port ShutDown/PowerOn Circuit (P 28)
           Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)

04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)

04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)

04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
           Combine Q35 and Q36 into a Dual Package Part (P 22)
           SWAP the ADT7460 Temperature Sense pair (P 25)
           Change FW PHY to production part (P 26)

04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24)
           Add 0402 Res between ATI PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
           Add 90ohm common mode choke at TMDS data <0..2> pairs (P 22)
           Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)

04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)
04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)
05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)
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DVT RELEASE

```
05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (p.31)
05/27/03 - Change RP31 to 4.7K for I2C timing specification  (p.13)
           Change Q62 & Q65 to SI7860DP part (p.33)
           Change Q60, Q63 & Q66 to IRF7832 part and split C102 into 3 10pF caps (p.33)
           Enable VCore Burst(Skip) Mode by no stuffing R67 (p.33)
           Enable 3V/5V Burst Mode by changing R406 & R407 to 100K ohm  (p.32)
           Change Q48 to SI7860DP part (p.20)
           Change Q49 to IRF7832 part (p.20)
           Enable GPUCore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343  (p.20)
           Reduce audible noise by changing L64 to 152S0139  (p.20)
           Add C838, C840, C839, C844 & C845 10pF caps near the power switchers FETs  (p.20, 32 & 34)
           Change PWM_L Fan input (both L&R Fans) to +5V_SLEEP pull-up (p.25)
05/30/03 - Connect SLEEP_LED_DGND to digital ground instead of CHGND5 (p.23)
06/03/03 - Add CPU Core Voltage offset option circuit (p.33)
           GPU Vcore on/off timimg (p.20)
06/05/03 - Change FW-B connector to 514S0058 with internal shield pins (p.28)
06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (p.38)
           Change the +2_5V_sleep FET to reduce Voltage drop on the rail (p.34)
06/12/03 - Change CBUS & USB2 REQ LINE Pullup to +3V_MAIN (p.12)
           Add 0 ohm at USB AVSS GND (p.17)
           Change TMDS common mode choke to TDK AMC2012-900H part (p.22)
           Change HD_DMACK_L pullup R213 to 10K (p.24)
           Add C847, C851 & C852 at ENET CLK for EMC (p.13 & 26)
           Change Q34 to FDS3672 (p.28)
           Change Q82 pin#4 connection to system digital GND (p.33)
           Add C848 150uF cap at J3 for +5V_MAIN USB2 power (p.25)
           Add C853 1000pF cap at Q64 (p.30)
           Add RC at ADT7460 power rail for noise isolation (p.25)
           Isolate THERM# signal at ADT7460 by using double inverters for THERM_L_OC  (p.25)
           Remove redundant pullup R601 for THERM_L_OC (p.29)
           Remove SH2 EMI spring at CHGND5 (p.23)
           Add additional PWR/GND pins at J17 for R-USB board (p.25)
06/13/03 - New SODIMM connector with 4 through-hole mounting pins (p.11)
           Change CPU config stuffing option at R63 and R64 (p.7)
           Stuff R288 for Cypress Clk chip (p.14)
           Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (p.12)
           Change the TMDS Termination Resistor values to 162ohm (p.20)
           Connect C847 at R160.1 (p.13)
           Add 1000pF caps at ADT7460 D_plus/minus pairs (p.25)
           Add SI1162 DVI transmitter to prevent leakage from DVI connector to the system (p.19&20)
06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (p.20&32)
           Remove R271 0ohm resistor (p.34)
           Edit Signal Constraints for TMDS routing and ENET routing (p.36&37)
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DVT2 RELEASE

```
07/06/03 - Change R97 & R98 to 0402 package (p.33)
           No Stuff R835 (p.19)
           Change R198 to 100K ohm resistor (p.23)
           Add Common Mode Choke L77 & L76 at FWB pairs (p.28)
           Removed current monitoring IC for firewire port power (p.28)
           Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (p.19)
```

PRODUCTION RELEASE

```
07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34)
08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p. 32)
           Change CPU VCORE setting for both BEST and BETTER configurations  (p. 33)
08/07/03 - Change CPU VCORE setting for both BEST and BETTER configurations again (p. 33)
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PRODUCTION RELEASE

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08/18/03 - Change CPU VCORE setting for BEST configuration to: 1.335V(High)->1.080V(Low) (p. 33)
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PRODUCTION RELEASE(Version B) for 051-6888

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08/29/05 - Added 338S0223 (88E1111 Rev. B1) as an option
08/29/05 - Added 128S0034 as an option
08/29/05 - Deleted 740S0006 as EOL
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