

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
			DATE	DATE	DATE
01		279015	ENGINEERING RELEASED		06/06/03 ?

Oct 27 12:25:21 2003

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Q59 MLB CONFIG "A"

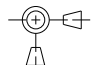

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+2_5V_MAIN	ON	ON	OFF
+3V_MAIN	ON	ON	OFF
+5V_MAIN	ON	ON	OFF
+5V_SLEEP	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12V_SLEEP	ON	OFF	OFF
FW_PWR	ON	ON	OFF
+1.8V_SLEEP	ON	OFF	OFF
+MAXBUS_SLEEP	ON	OFF	OFF

SCHEMATIC AND PCB SUPPORT

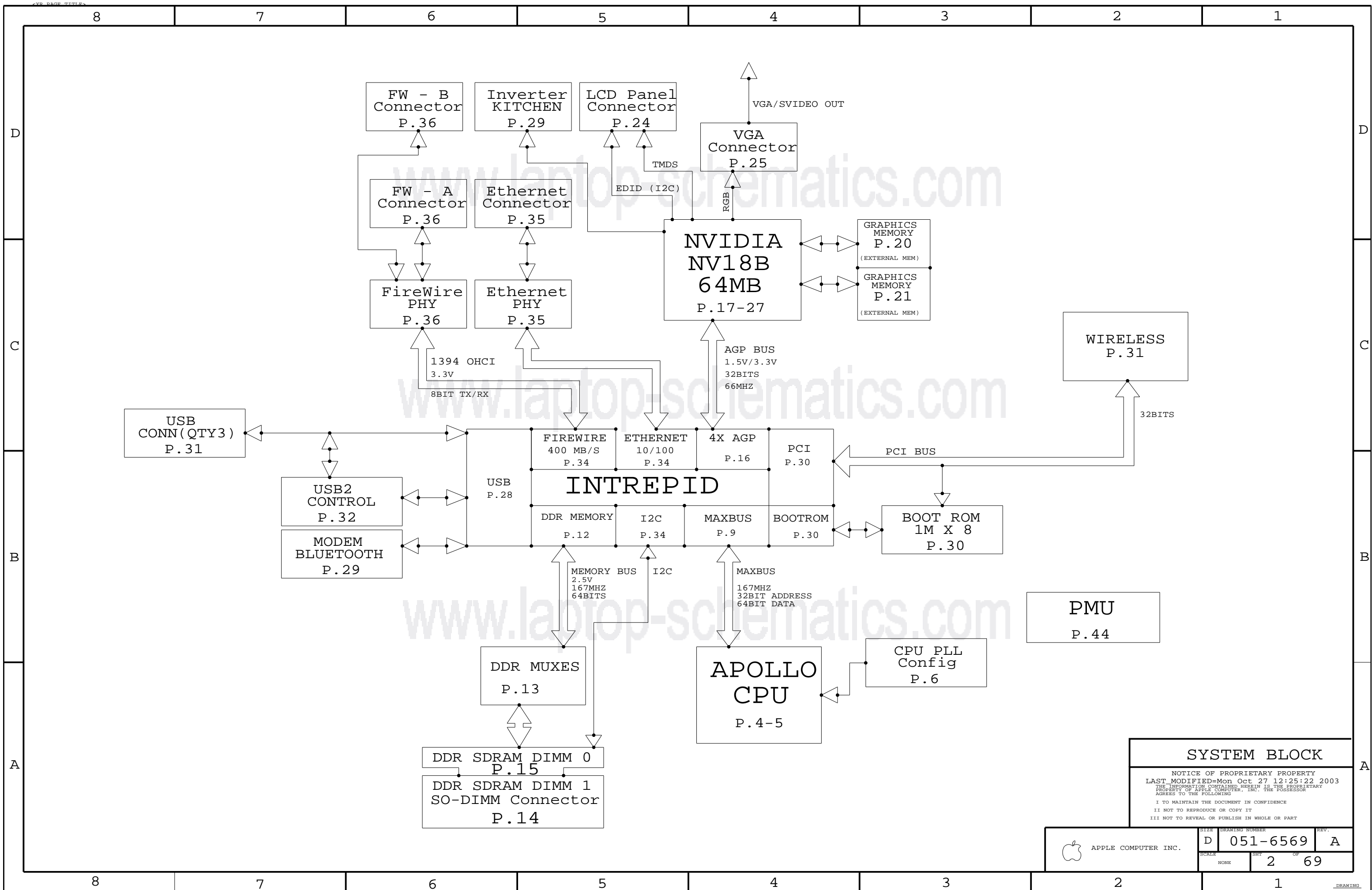
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6569	1	SCHEM,MLB,Q59	SCH1	CRITICAL	
820-1599	1	PCB,MLB,IMACG4.A,B,C	PCB1	CRITICAL	
825-2029	1	LBL,SER #,BARCODE	PCB1		
056-1158	1	DESIGN GUIDE,MCO,IMACG4	PCB1	CRITICAL	
057-0085	1	DFM,PNLZN DWG,MLB,Q59	PCB1	CRITICAL	
630-XXXX	1	630-XXXX,PCBA,H,Q59,EEE XXX	HYNIX		OMIT
630-XXXX	1	630-XXXX,PCBA,S,Q59,EEE XXX	SAMSUNG		OMIT

PCB,UL RECOGNIZED, MIN.130 DEG. C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94. PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, TEMPERATURE RATING AND FLAME RATING.

DIMENSIONS ARE IN MILLIMETERS XX : _____ X.XX : _____ X.XXX : _____ ANGLES : _____ DO NOT SCALE DRAWING  THIRD ANGLE PROJECTION	METRIC		 Apple Computer Inc.		
	DRAFTER <input checked="" type="checkbox"/>	DESIGN CR <input checked="" type="checkbox"/>	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
	ENG APPD <input checked="" type="checkbox"/>	MFG APPD <input checked="" type="checkbox"/>	TITLE SCHEM,MLB,Q59A		
	QA APPD <input checked="" type="checkbox"/>	DESIGNER <input checked="" type="checkbox"/>	DRAWING NUMBER 051-6569 REV. A		
RELEASE <input checked="" type="checkbox"/>	SCALE <input checked="" type="checkbox"/> NONE	MATERIAL/FINISH NOTED AS APPLICABLE SIZE D SHEET 1 OF 69			

D
C
B
A

D
C
B
A

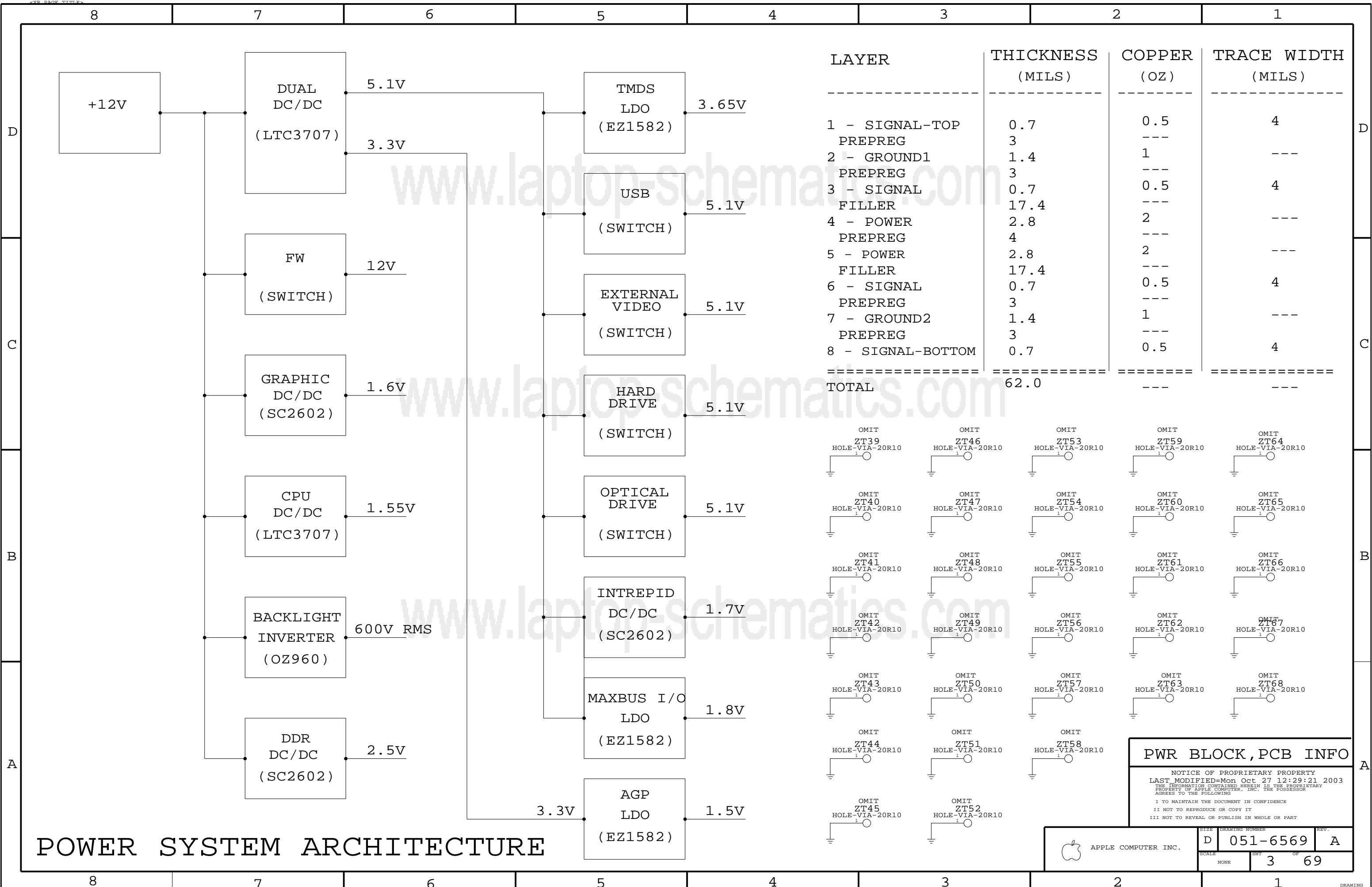


SYSTEM BLOCK

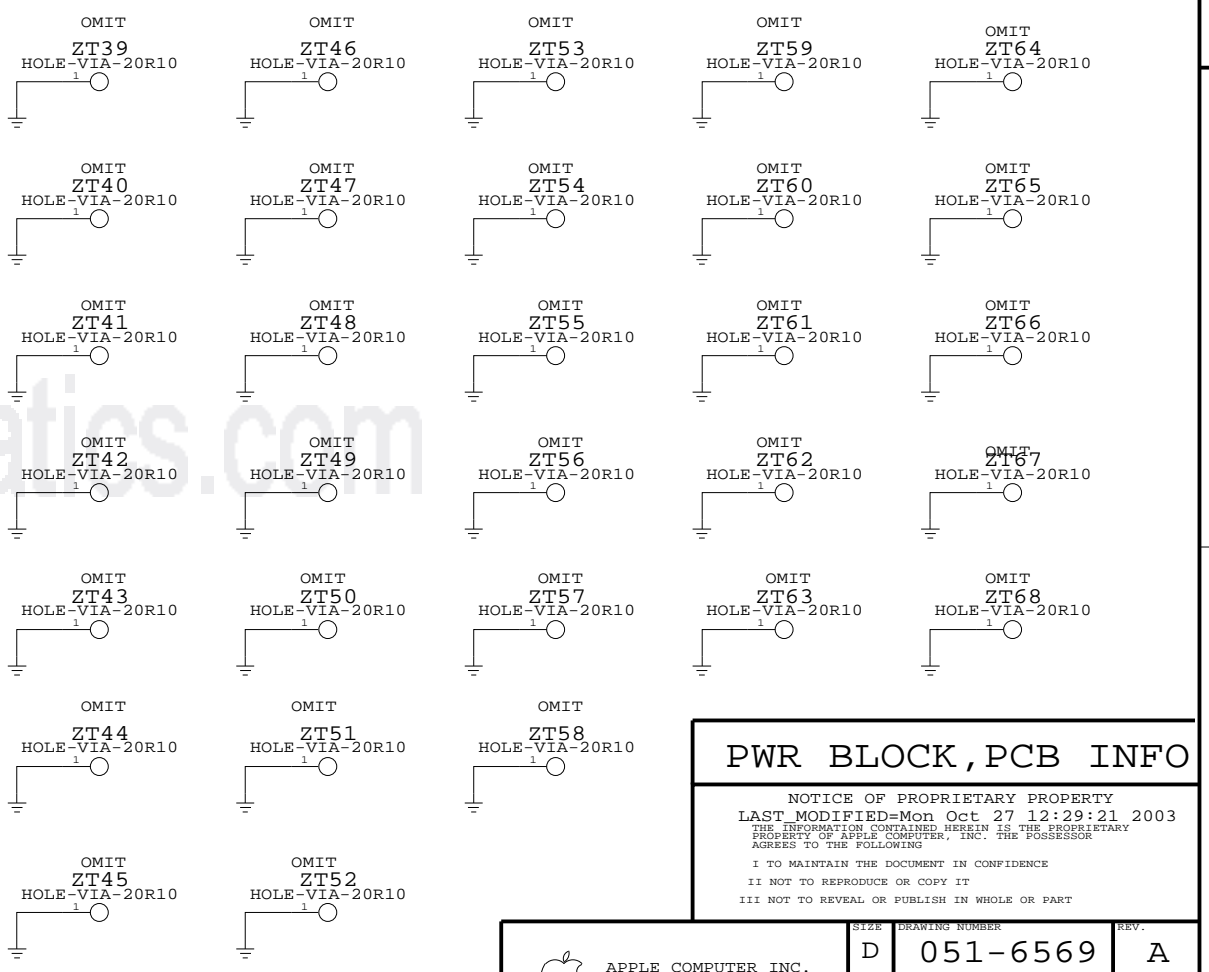
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6569	A
	SCALE	SHT	OF
	NONE	2	69



LAYER	THICKNESS (MILS)	COPPER (OZ)	TRACE WIDTH (MILS)
1 - SIGNAL-TOP	0.7	0.5	4
PREPREG	3	---	---
2 - GROUND1	1.4	1	---
PREPREG	3	---	---
3 - SIGNAL	0.7	0.5	4
FILLER	17.4	---	---
4 - POWER	2.8	2	---
PREPREG	4	---	---
5 - POWER	2.8	2	---
FILLER	17.4	---	---
6 - SIGNAL	0.7	0.5	4
PREPREG	3	---	---
7 - GROUND2	1.4	1	---
PREPREG	3	---	---
8 - SIGNAL-BOTTOM	0.7	0.5	4
=====	=====	=====	=====
TOTAL	62.0	---	---



PWR BLOCK, PCB INFO

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POWER SYSTEM ARCHITECTURE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE	SHT	OF
NONE	3	69

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 4D7< 8B7< 8C1< 45D2< 52C6> 59B5> 59D7>

59D7> 59B5> 52C6> 45D2< 8C1< 8B7< 4D3< CPU_VCORE_SLEEP

+MAXBUS_SLEEP 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3< 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2< 46D4< 52C6> 59C7>

D

D

C

C

B

B

A

A

- 56D3> 9D3<> 8B4<> 7C7< CPU_BR_L D2 BR*
- 56D3> 9D3<> 8B4<> 7B7< CPU_BG_L M1 BG*
- 56D3> 9D3<> 8B7<> 7C7< CPU_TS_L L4 TS*
- 7C5< 4A3< CPU_PULLDOWN
- 56D3> 9D3<> 8B4<> CPU_ADDR<0> E11 A0
- 56D3> 9D3<> 8B5<> CPU_ADDR<1> L2 A5
- 56D3> 9D3<> 8B4<> CPU_ADDR<2> D11 A6
- 56D3> 9D3<> 8B8<> CPU_ADDR<3> D1 A7
- 56D3> 9D3<> 8B5<> CPU_ADDR<4> C10 A8
- 56D3> 9D3<> 8B7<> CPU_ADDR<5> G2 A9
- 56D3> 9D3<> 8C4<> CPU_ADDR<6> D12 A10
- 56D3> 9D3<> 8B7<> CPU_ADDR<7> L3 A11
- 56D3> 9D3<> 8C5<> CPU_ADDR<8> G4 A12
- 56D3> 9C3<> 8B8<> CPU_ADDR<9> T2 A13
- 56D3> 9C3<> 8B8<> CPU_ADDR<10> F4 A14
- 56D3> 9C3<> 8C4<> CPU_ADDR<11> V1 A15
- 56D3> 9C3<> 8B7<> CPU_ADDR<12> J4 A16
- 56D3> 9C3<> 8B8<> CPU_ADDR<13> R2 A17
- 56D3> 9C3<> 8B7<> CPU_ADDR<14> K5 A18
- 56D3> 9C3<> 8B7<> CPU_ADDR<15> M2 A19
- 56D3> 9C3<> 8B8<> CPU_ADDR<16> J2 A20
- 56D3> 9C3<> 8B8<> CPU_ADDR<17> K4 A21
- 56D3> 9C3<> 8C8<> CPU_ADDR<18> M4 A22
- 56D3> 9C3<> 8B7<> CPU_ADDR<19> J3 A23
- 56D3> 9C3<> 8B8<> CPU_ADDR<20> M5 A24
- 56D3> 9C3<> 8C7<> CPU_ADDR<21> P5 A25
- 56D3> 9C3<> 8C7<> CPU_ADDR<22> N3 A26
- 56D3> 9C3<> 8C8<> CPU_ADDR<23> T1 A27
- 56D3> 9C3<> 8B7<> CPU_ADDR<24> V2 A28
- 56D3> 9C3<> 8B8<> CPU_ADDR<25> U1 A29
- 56D3> 9C3<> 8C8<> CPU_ADDR<26> N5 A30
- 56D3> 9C3<> 8C7<> CPU_ADDR<27> W1 A31
- 56D3> 9C3<> 8C7<> CPU_ADDR<28> B12 A32
- 56D3> 9C3<> 8C8<> CPU_ADDR<29> C4 A33
- 56D3> 9C3<> 8C7<> CPU_ADDR<30> G10 A34
- 56D3> 9C3<> 8C7<> CPU_ADDR<31> B11 A35
- NC_CPUAP<0> NO_TEST C1 AP0
- NC_CPUAP<1> NO_TEST E3 AP1
- NC_CPUAP<2> NO_TEST H6 AP2
- NC_CPUAP<3> NO_TEST F5 AP3
- NC_CPUAP<4> NO_TEST G7 AP4
- 56D3> 9B3<> 8B4<> 7A7< CPU_TT<0> E5 TT0
- 56D3> 9B3<> 8B5<> 7A7< CPU_TT<1> E6 TT1
- 56D3> 9B3<> 8B4<> 7A7< CPU_TT<2> F6 TT2
- 56D3> 9B3<> 8B5<> 7A7< CPU_TT<3> E9 TT3
- 56D3> 9B3<> 8B4<> 7A7< CPU_TT<4> C5 TT4
- 56D3> 9B3<> 8B4<> 7B7< CPU_TBST_L F11 TBST*
- 56D3> 9B3<> 8B5<> CPU_TSIZ<0> G6 TSIZ0
- 56D3> 9B3<> 8B5<> CPU_TSIZ<1> F7 TSIZ1
- 56D3> 9B3<> 8B7<> CPU_TSIZ<2> E7 TSIZ2
- GBL* E2 GBL*
- WT* D3 WT*
- 56C3> 9B3<> 8C5<> 7A7< CPU_CI_L J1 CI*
- 56C3> 9B3<> 8B5<> 7B7< CPU_AACK_L R1 AACK*
- 56C3> 9B3<> 8B8<> 7C7< CPU_ARTRY_L N2 ARTRY*
- 7B5< CPU_SHD0_L R4 SHD0*
- 7B5< CPU_SHD1_L R5 SHD1*
- 56C3> 9B3< 8B8<> 7C7< CPU_HIT_L B2 HIT*

U34
800MHZ
APOLLO_MPC7445_360
BGA
(1 OF 3)
SEE_TABLE

- BVSEL B7 CPU_BUS_VSEL 7C4<
- SYSCLK A10 NC_CPU_CLKOUT
- CLKOUT H2 NO_TEST CPU_PLL_CFG<0> 6C6< 8A8<>
- PLLFCFG0 B8 CPU_PLL_CFG<1> 6C6< 8A8<>
- PLLFCFG1 C8 CPU_PLL_CFG<2> 6C6< 8A8<>
- PLLFCFG2 D7 CPU_PLL_CFG<3> 6C6< 8A8<>
- PLLFCFG3 D7 CPU_PLL_CFGEXT 6C6< 8A8<>
- PLL_EXT A7
- DBG* M2 CPU_DBG_L 7B7< 8B8<> 9B1<> 56C3>
- DRDY* R3 CPU_DRDY_L UF 56C3>
- DTI0 G1 CPU_EDTI 7C5<
- DTI1 K1 CPU_DTI<0> 8B7<> 9A1<> 56C3>
- DTI2 F1 CPU_DTI<1> 8B4<> 9A1<> 56C3>
- DTI3 N1 CPU_DTI<2> 8B4<> 9A1<> 56C3>
- TDI B9 JTAG_CPU_TDI 7A5< 8A3<> 59C7>
- TDO A4 JTAG_CPU_TDO 8A3<> 59C7>
- TMS F1 JTAG_CPU_TMS 7A5< 8A3<> 59C7>
- TCK C6 JTAG_CPU_TCK 7D5< 8A3<> 59C7>
- TRST* A5 JTAG_CPU_TRST_L 7C5< 8A3<> 59C7>
- LSSDMODE* E8 CPU_LSSD_MODE 7B5<
- L1TSTCLK G8 CPU_L1TSTCLK 7B4<
- L2TSTCLK B3 CPU_L2TSTCLK 7C4<
- TA* K6 CPU_TA_L 7C7< 8C4<> 9A1<> 56C3>
- TEA* L1 CPU_TEA_L 7B7< 8B5<> 9A1<> 56C3>
- TBEN E1 CPU_TBEN 7C5< 9A3<>
- QREQ* F4 CPU_QREQ_L 7D5< 8B7<> 9B3<> 56C3>
- QACK* G5 CPU_QACK_L 8B4<> 9B3<> 56C3>
- CKSTP_IN* A3 CPU_CHKSTP_IN_L 7B5< 59C7>
- CKSTP_OUT* B1 CPU_CHKSTP_OUT_L 7B5< 8A3<> 8D5<> 59C7>
- INT* C4 MPIC_CPU_INT_L 7A5< 8D7<> 28B5>
- SMI* F9 CPU_SMI_L 7A5< 44C4<>
- MCP* C9 CPU_MCP_L 7B5<
- SRESET* A2 CPU_SRESET_L 7A5< 8A3<> 59C5>
- HRESET* D8 CPU_HRESET_L 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C7>
- IBORG PULLS THIS UP, SPEC SAYS TO GROUND IT FOR SW CONTROL
- PMON_IN* D9 CPU_PMONIN_L 7C5<
- PMON_OUT* A9 NO_TEST NC_PMON_OUT_L
- BMODE0* G9 CPU_EMODE0_L 7A4<
- BMODE1* F8 CPU_EMODE1_L 7A4<
- EXT_QUAL A11
- TEST0 A12
- TEST1 B6
- TEST2 B10
- TEST3 E10
- TEST4 D10
- CPU_PULLUP 7A5<
- CPU_PULLDOWN 4D7<> 7C5<

R901
10
1/16W
MP
603

C1036
0.1UF
10V
CERM
402

C1035
2.2UF
16V
CERM
805

R895
47
1/16W
MP
402

R850
5
1/16W
MP
402

C954
10PF
50V
CERM
402

RC GLITCH FILTER
PLACE CLOSE TO PIN

FILTERS A WAKE FROM SLEEP GLITCH
IF NECESSARY

OMIT
ZH4
275R138

C352
0.1UF
10V
CERM
402

OMIT
ZH6
275R138

C369
0.1UF
10V
CERM
402

OMIT
ZH5
275R138

C345
0.1UF
10V
CERM
402

OMIT
ZH7
275R138

C370
0.1UF
10V
CERM
402

INTREPID VERSION 1 PULLS GBL
ALL THE TIME. NEED TO
CUT THE TRACE AND YANK
DOWN HARD FOR SNOOPING.
FIXED IN INTREPID VERSION 2.

CPU MECHANICAL PARTS SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
875-1475	1	PAD, THERMAL, CPU, U34	U341	?	
870-1113	1	HEAT SINK, CPU, Q26, U34	U342	?	DEV
870-1114	1	CLIP, HEAT SINK, CPU, Q26, U34	U343	?	DEV
412-0042	1	SCREW, MACH, 3MM W, 8MM L, U34	U344	?	DEV
835-0251	1	NUT, 3MM, U34	U345	?	DEV

MPC7450 MAXBUS

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	D	051-6569	A
SCALE	SHT	OF	
NONE	4	69	

APOLLO_MPC7445_360

NC_CPUCRUD<0>	NO_TEST	F18	NC_F18
NC_CPUCRUD<1>	NO_TEST	F17	NC_F17
NC_CPUCRUD<2>	NO_TEST	F19	NC_F19
NC_CPUCRUD<3>	NO_TEST	H19	NC_H19
NC_CPUCRUD<4>	NO_TEST	H18	NC_H18
NC_CPUCRUD<5>	NO_TEST	H17	NC_H17
NC_CPUCRUD<6>	NO_TEST	H16	NC_H16
NC_CPUCRUD<7>	NO_TEST	E19	NC_E19
NC_CPUCRUD<8>	NO_TEST	D18	NC_D18
NC_CPUCRUD<9>	NO_TEST	F16	NC_F16
NC_CPUCRUD<10>	NO_TEST	G16	NC_G16
NC_CPUCRUD<11>	NO_TEST	D19	NC_D19
NC_CPUCRUD<12>	NO_TEST	F15	NC_F15
NC_CPUCRUD<13>	NO_TEST	G19	NC_G19
NC_CPUCRUD<14>	NO_TEST	E16	NC_E16
NC_CPUCRUD<15>	NO_TEST	D17	NC_D17
NC_CPUCRUD<16>	NO_TEST	D16	NC_D16

NC_CPUCRUD<17>	NO_TEST	P15	NC_P15
NC_CPUCRUD<18>	NO_TEST	L15	NC_L15
NC_CPUCRUD<19>	NO_TEST	N15	NC_N15
NC_CPUCRUD<20>	NO_TEST	P18	NC_P18
NC_CPUCRUD<21>	NO_TEST	N14	NC_N14
NC_CPUCRUD<22>	NO_TEST	M14	NC_M14
NC_CPUCRUD<23>	NO_TEST	M17	NC_M17
NC_CPUCRUD<24>	NO_TEST	N13	NC_N13
NC_CPUCRUD<25>	NO_TEST	N16	NC_N16
NC_CPUCRUD<26>	NO_TEST	M19	NC_M19
NC_CPUCRUD<27>	NO_TEST	M16	NC_M16
NC_CPUCRUD<28>	NO_TEST	P19	NC_P19
NC_CPUCRUD<29>	NO_TEST	N17	NC_N17
NC_CPUCRUD<30>	NO_TEST	M15	NC_M15
NC_CPUCRUD<31>	NO_TEST	L17	NC_L17
NC_CPUCRUD<32>	NO_TEST	L14	NC_L14
NC_CPUCRUD<33>	NO_TEST	K15	NC_K15
NC_CPUCRUD<34>	NO_TEST	J14	NC_J14
NC_CPUCRUD<35>	NO_TEST	J18	NC_J18
NC_CPUCRUD<36>	NO_TEST	J19	NC_J19
NC_CPUCRUD<37>	NO_TEST	J15	NC_J15
NC_CPUCRUD<38>	NO_TEST	K19	NC_K19
NC_CPUCRUD<39>	NO_TEST	J16	NC_J16
NC_CPUCRUD<40>	NO_TEST	H15	NC_H15
NC_CPUCRUD<41>	NO_TEST	L16	NC_L16
NC_CPUCRUD<42>	NO_TEST	P16	NC_P16
NC_CPUCRUD<43>	NO_TEST	M18	NC_M18
NC_CPUCRUD<44>	NO_TEST	L19	NC_L19
NC_CPUCRUD<45>	NO_TEST	L18	NC_L18
NC_CPUCRUD<46>	NO_TEST	K18	NC_K18
NC_CPUCRUD<47>	NO_TEST	J17	NC_J17
NC_CPUCRUD<48>	NO_TEST	K16	NC_K16
NC_CPUCRUD<49>	NO_TEST	C19	NC_C19
NC_CPUCRUD<50>	NO_TEST	D15	NC_D15
NC_CPUCRUD<51>	NO_TEST	G15	NC_G15
NC_CPUCRUD<52>	NO_TEST	C18	NC_C18
NC_CPUCRUD<53>	NO_TEST	A16	NC_A16
NC_CPUCRUD<54>	NO_TEST	B19	NC_B19
NC_CPUCRUD<55>	NO_TEST	A19	NC_A19
NC_CPUCRUD<56>	NO_TEST	D14	NC_D14
NC_CPUCRUD<57>	NO_TEST	E15	NC_E15
NC_CPUCRUD<58>	NO_TEST	B15	NC_B15
NC_CPUCRUD<59>	NO_TEST	B17	NC_B17
NC_CPUCRUD<60>	NO_TEST	C17	NC_C17
NC_CPUCRUD<61>	NO_TEST	C16	NC_C16
NC_CPUCRUD<62>	NO_TEST	G13	NC_G13
NC_CPUCRUD<63>	NO_TEST	E14	NC_E14
NC_CPUCRUD<64>	NO_TEST	H14	NC_H14
NC_CPUCRUD<65>	NO_TEST	G14	NC_G14
NC_CPUCRUD<66>	NO_TEST	C15	NC_C15
NC_CPUCRUD<67>	NO_TEST	A17	NC_A17
NC_CPUCRUD<68>	NO_TEST	G12	NC_G12
NC_CPUCRUD<69>	NO_TEST	F14	NC_F14
NC_CPUCRUD<70>	NO_TEST	F13	NC_F13
NC_CPUCRUD<71>	NO_TEST	E13	NC_E13
NC_CPUCRUD<72>	NO_TEST	B16	NC_B16
NC_CPUCRUD<73>	NO_TEST	A15	NC_A15
NC_CPUCRUD<74>	NO_TEST	C14	NC_C14
NC_CPUCRUD<75>	NO_TEST	A18	NC_A18
NC_CPUCRUD<76>	NO_TEST	A13	NC_A13
NC_CPUCRUD<77>	NO_TEST	F12	NC_F12
NC_CPUCRUD<78>	NO_TEST	A14	NC_A14
NC_CPUCRUD<79>	NO_TEST	G11	NC_G11
NC_CPUCRUD<80>	NO_TEST	C13	NC_C13

NC_CPUCRUD<81>	NO_TEST	N12	NC_N12
NC_CPUCRUD<82>	NO_TEST	N18	NC_N18
NC_CPUCRUD<83>	NO_TEST	K17	NC_K17
NC_CPUCRUD<84>	NO_TEST	N19	NC_N19
NC_CPUCRUD<85>	NO_TEST	B18	NC_B18
NC_CPUCRUD<86>	NO_TEST	E12	NC_E12
NC_CPUCRUD<87>	NO_TEST	B13	NC_B13
NC_CPUCRUD<88>	NO_TEST	B14	NC_B14
NC_CPUCRUD<89>	NO_TEST	A6	NC_A6

U34
800MHZ
BGA
(3 OF 3)

APOLLO_MPC7445_360

56D3> 9D1<> 8C4<>	CPU_DATA<0>	R15	D0
56D3> 9D1<> 8C7<>	CPU_DATA<1>	M15	D1
56D3> 9D1<> 8C8<>	CPU_DATA<2>	T14	D2
56D3> 9D1<> 8C5<>	CPU_DATA<3>	V16	D3
56D3> 9D1<> 8C7<>	CPU_DATA<4>	M16	D4
56D3> 9D1<> 8C8<>	CPU_DATA<5>	T15	D5
56D3> 9D1<> 8C4<>	CPU_DATA<6>	U15	D6
56D3> 9D1<> 8C8<>	CPU_DATA<7>	F14	D7
56D3> 9D1<> 8C5<>	CPU_DATA<8>	V13	D8
56D3> 9D1<> 8C4<>	CPU_DATA<9>	M13	D9
56D3> 9D1<> 8C7<>	CPU_DATA<10>	T13	D10
56D3> 9D1<> 8C5<>	CPU_DATA<11>	F13	D11
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56D3> 9C1<> 8C4<>	CPU_DATA<19>	N10	D19
56D3> 9C1<> 8C4<>	CPU_DATA<20>	R11	D20
56D3> 9C1<> 8C8<>	CPU_DATA<21>	U11	D21
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U34
800MHZ
BGA
(2 OF 3)

NC_CPUDP<0>	NO_TEST	T3	DP0
NC_CPUDP<1>	NO_TEST	M4	DP1
NC_CPUDP<2>	NO_TEST	T4	DP2
NC_CPUDP<3>	NO_TEST	M9	DP3
NC_CPUDP<4>	NO_TEST	M6	DP4
NC_CPUDP<5>	NO_TEST	V3	DP5
NC_CPUDP<6>	NO_TEST	N8	DP6
NC_CPUDP<7>	NO_TEST	M6	DP7

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BOMOPTIONS FOR UPPER-SET OF RESISTORS

1200@133&1500@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

667@133&833@167&733@133&917@167&800@133&1000@167&1067@133&1333@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1867@133&2333@167&2133@133&2667@167

800@133&1000@167&867@133&1083@167&1067@133&1333@167&1200@133&1500@167&1733@133&2167@167&1867@133&2333@167&2133@133&2667@167

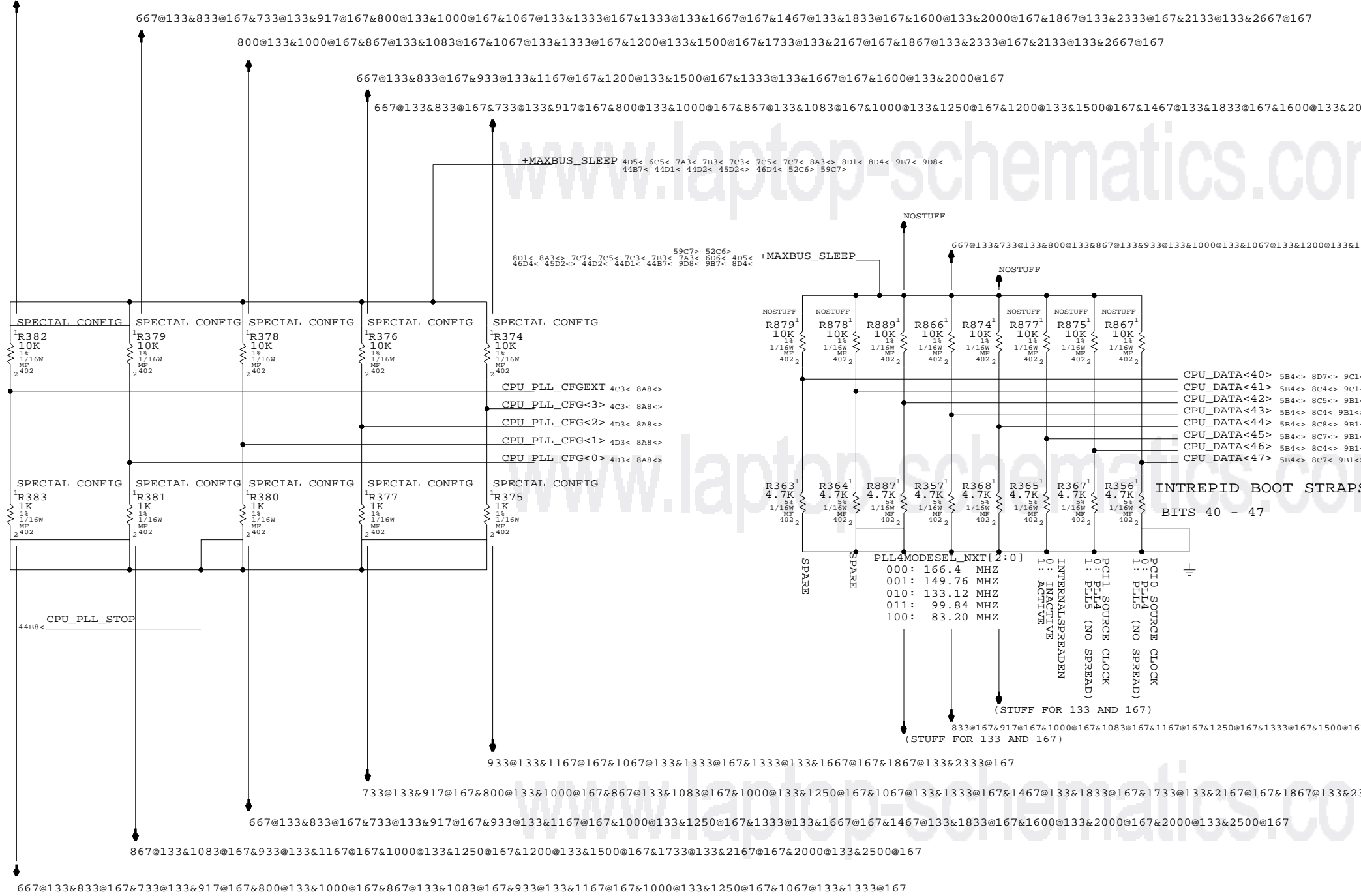
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CPU FREQUENCY CONFIGURATION (SUPPORTED CPU & BUS SPEEDS)

MULTIPLIER (BUS-TO-CORE)	CORE FREQUENCY (AT BUS FREQUENCY)	CPU_PLL_CFG
	167MHZ	133MHZ
5.0X	833	667
5.5X	917	733
6.0X	1000	800
6.5X	1083	867
7.0X	1167	933
7.5X	1250	1000
8.0X	1333	1067
9.0X	1500	1200
10.0X	1667	1333
11.0X	1833	1467
12.0X	2000	1600
13.0X	2167	1733
14.0X	2333	1867
15.0X	2500	2000
16.0X	2667	2133



CPU SPEED & BUS RATIO SUPPORT
THE CONFIGURATION RESISTORS BELOW ARE SELF CONFIGURING
WHEN THE ENGINEER SELECTS THE APPROPRIATE CPU AND
BUS SPEED BOM OPTION, THE APPROPRIATE RESISTORS ARE
ARE AUTOMATICALLY SELECTED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S2799	1	IC, APOLLO6, SICOH, 1.0GHZ, 1.5V+30/-130MV, 28W, 85C	U34	CRITICAL	1000@167
337S2801	1	IC, APOLLO6, SICOH, 1.25GHZ, 1.57V+70/-70MV, 35W, 85C	U34	CRITICAL	1250@167

CPU BUS RATIO BITS

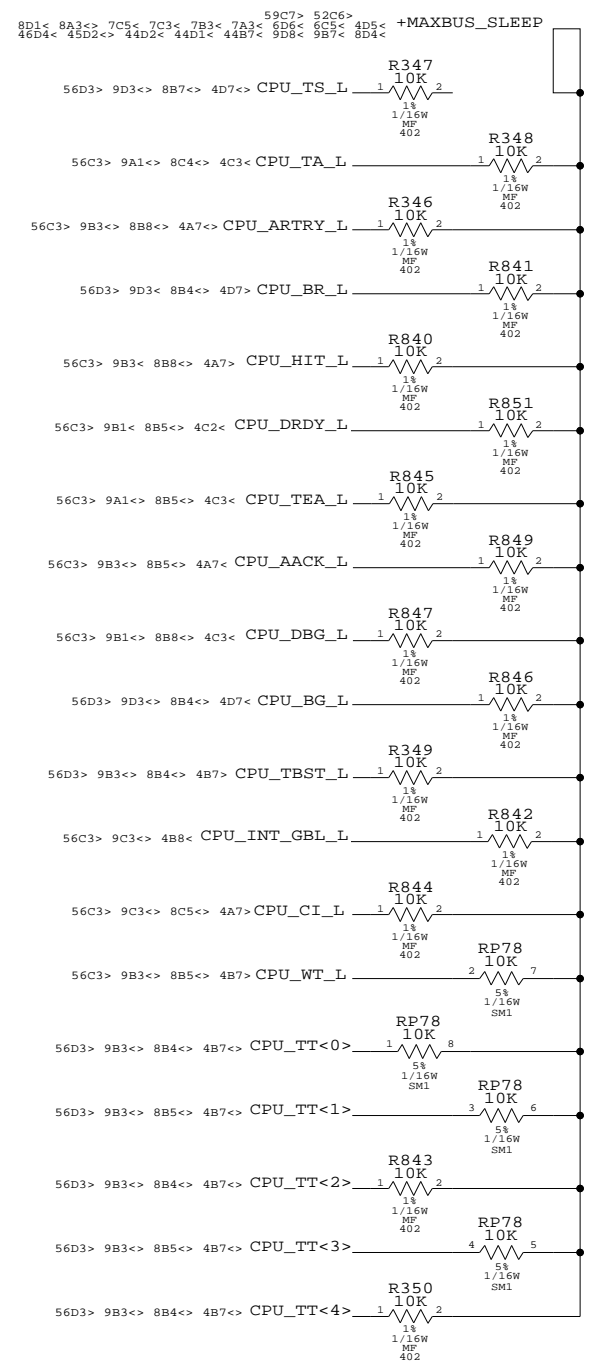
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NONE	6		69

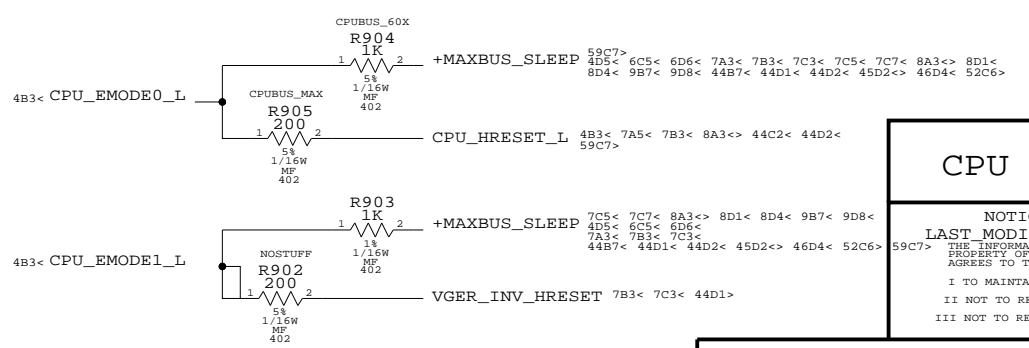
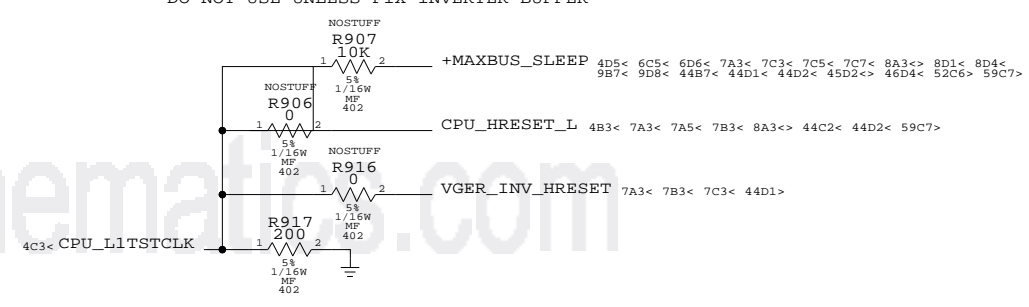
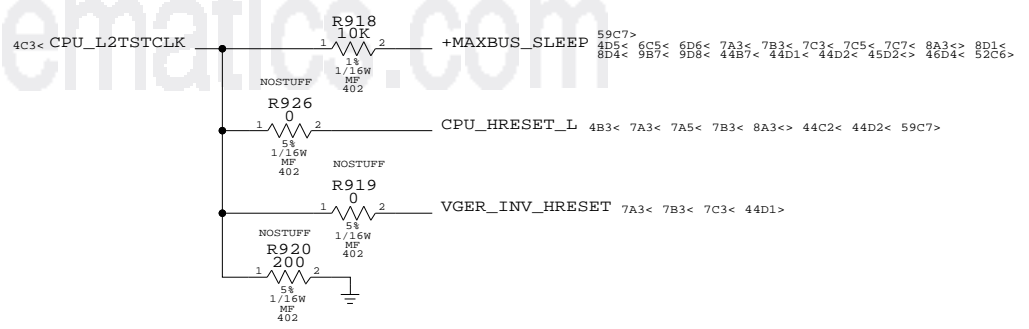
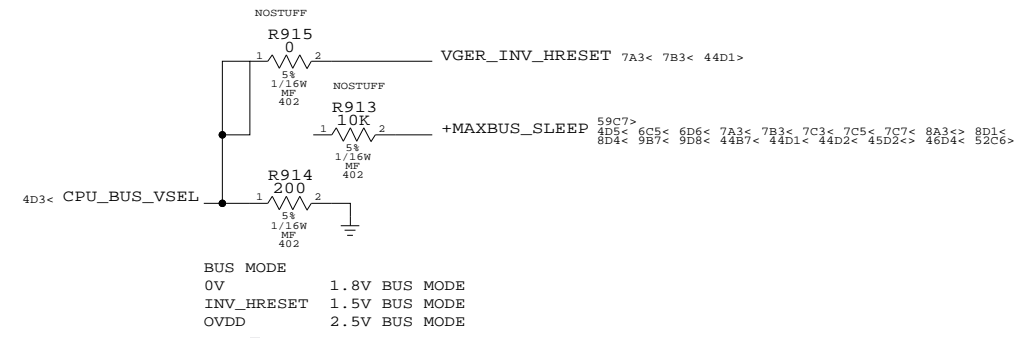
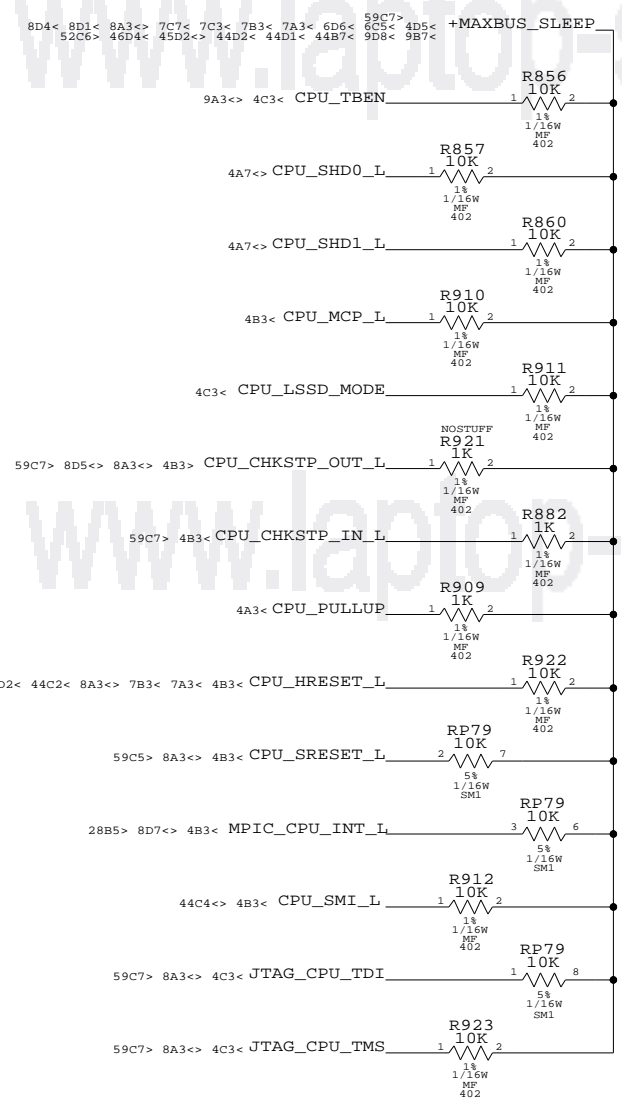
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L L	1 1	???	01	yes unavail
L !hr	1 0	Max	01	yes unavail
L hr	1 1	???	00	yes unavail
L H	1 0	Max	00	yes unavail
!hr L	0 1	MB+	01	yes unavail
!hr !hr	0 0	60x	01	yes unavail
!hr hr	0 1	MB+	00	yes unavail
!hr H	0 0	60x	00	yes unavail
hr L	1 1	???	01	norm unavail
hr !hr	1 0	Max	01	norm unavail
hr hr	1 1	???	00	norm unavail
HR H	1 0	MAX	00	NORM <- DEFAULT
H L	0 1	MB+	01	norm unavail
H !hr	0 0	60x	01	norm unavail
H hr	0 1	MB+	00	norm unavail
H H	0 0	60x	00	norm unavail

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L	HIGH	60X BUS MODE
CPU_BUS_VSEL	CPU_HRESET_L	MAX BUS MODE
	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE
CPU_L3_VSEL	CPU_HRESET_L or L3_OVDD	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE

MAXBUS PULL-UPS

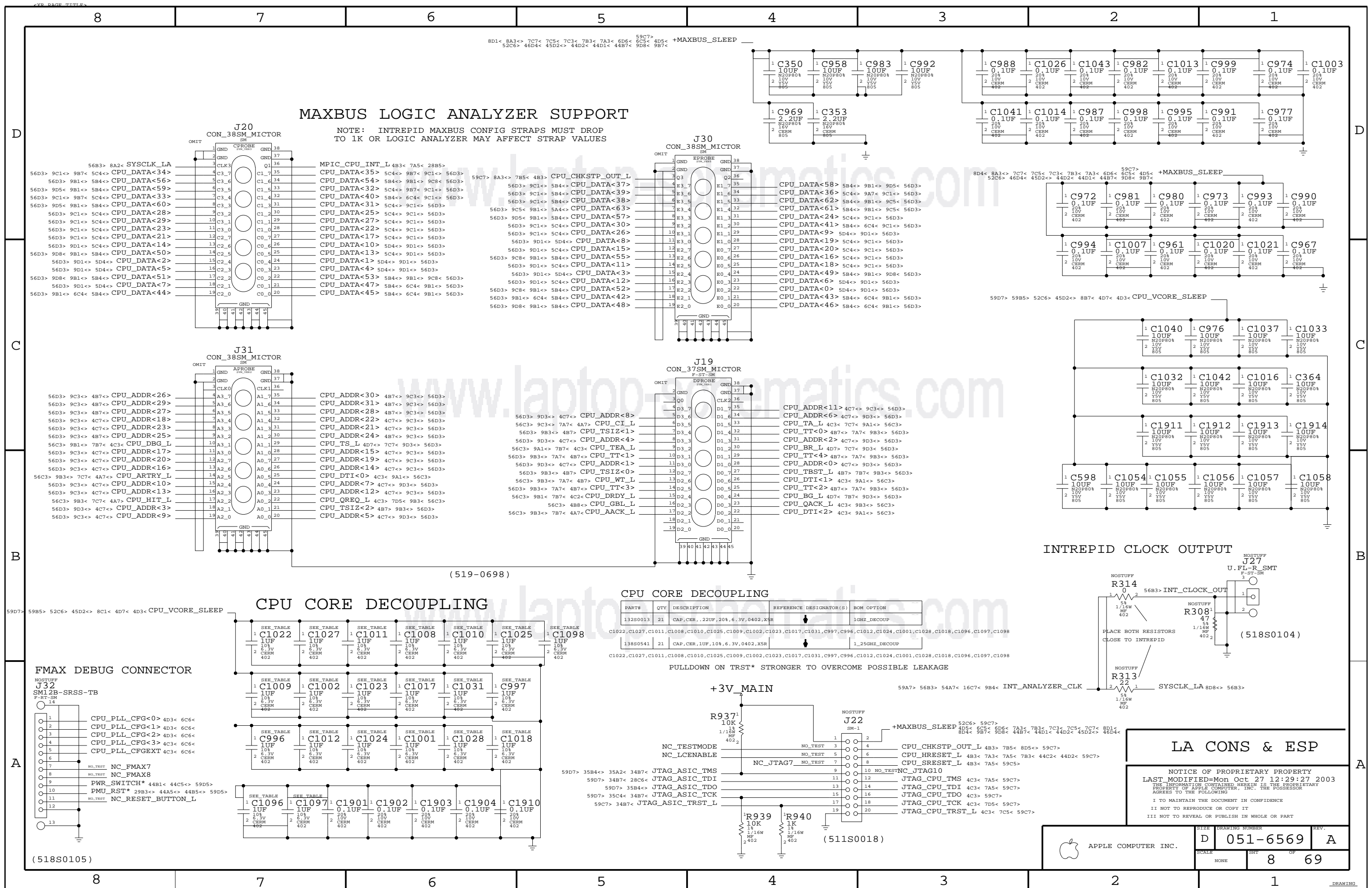


MPC7450 PULL-UPS



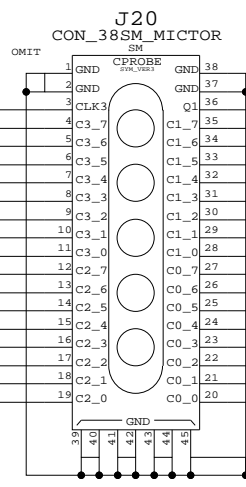
CPU CONFIG OPTIONS		
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NONE	7	69	

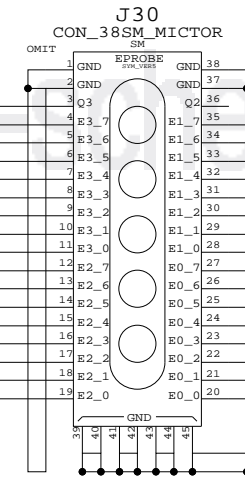


MAXBUS LOGIC ANALYZER SUPPORT

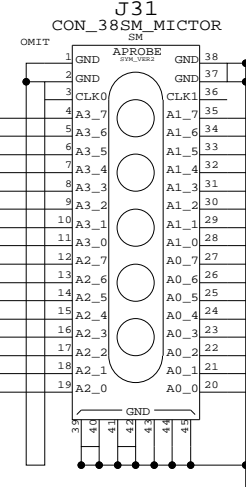
NOTE: INTREPID MAXBUS CONFIG STRAPS MUST DROP TO 1K ON LOGIC ANALYZER MAY AFFECT STRAP VALUES



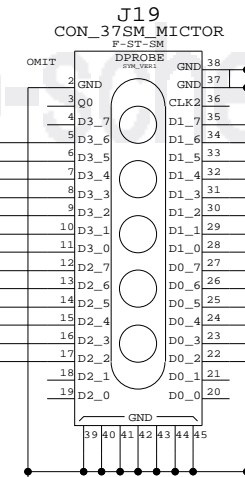
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- CPU_DATA<35> 5C4< 9B7< 9C1< 56D3>
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- CPU_DATA<40> 5B4< 6C4< 9C1< 56D3>
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- CPU_DATA<22> 5C4< 9C1< 56D3>
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- CPU_DATA<4> 5D4< 9D1< 56D3>
- CPU_DATA<53> 5B4< 9B1< 9C8< 56D3>
- CPU_DATA<45> 5B4< 6C4< 9B1< 56D3>



- 59C7> 8A3< 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< +MAXBUS_SLEEP
- 52C6> 46D4< 45D2< 44D2< 44D1< 44B7< 9D8< 9B7<
- CPU_DATA<58> 5B4< 9B1< 9D5< 56D3>
- CPU_DATA<36> 5C4< 9A7< 9C1< 56D3>
- CPU_DATA<62> 5B4< 9B1< 9C5< 56D3>
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- CPU_DATA<24> 5C4< 9C1< 56D3>
- CPU_DATA<41> 5B4< 6C4< 9C1< 56D3>
- CPU_DATA<9> 5D4< 9D1< 56D3>
- CPU_DATA<19> 5C4< 9C1< 56D3>
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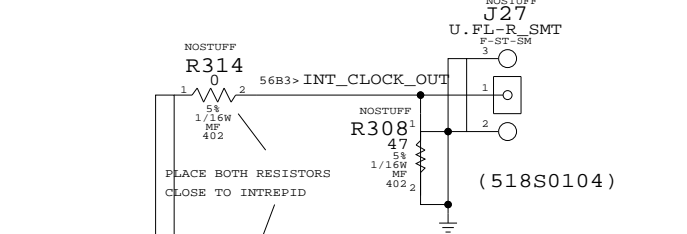


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- CPU_DBG_L 4B3< 7C7< 4A7< 56C3>
- CPU_ADDR<17> 4C7< 9C3< 56D3>
- CPU_ADDR<20> 4C7< 9C3< 56D3>
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- CPU_ADDR<7> 4C7< 9D3< 56D3>
- CPU_ADDR<12> 4C7< 9C3< 56D3>
- CPU_QREQ_L 4C3< 7D5< 9B3< 56C3>
- CPU_TSIZ<2> 4B7< 9B3< 56D3>
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- CPU_TT<0> 4B7< 7A7< 9B3< 56D3>
- CPU_ADDR<2> 4C7< 9D3< 56D3>
- CPU_BR_L 4D7< 7C7< 9D3< 56D3>
- CPU_TT<4> 4B7< 7A7< 9B3< 56D3>
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- CPU_TBST_L 4B7< 7B7< 9B3< 56D3>
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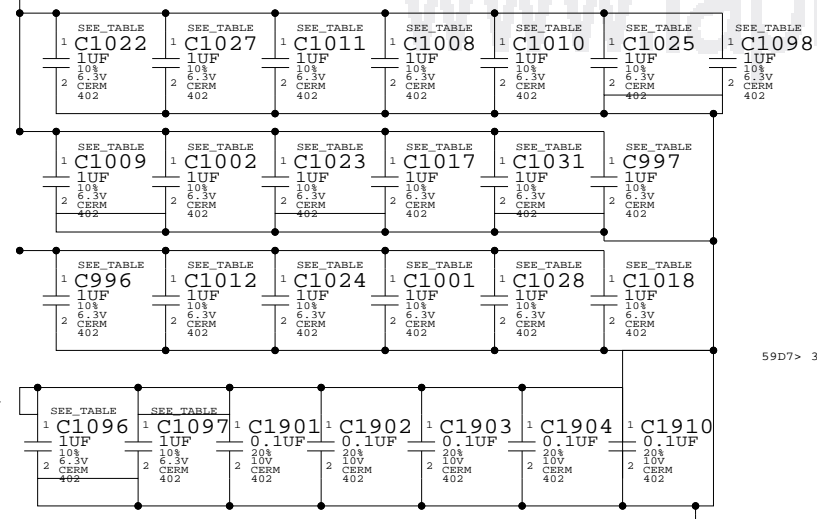


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INTREPID CLOCK OUTPUT



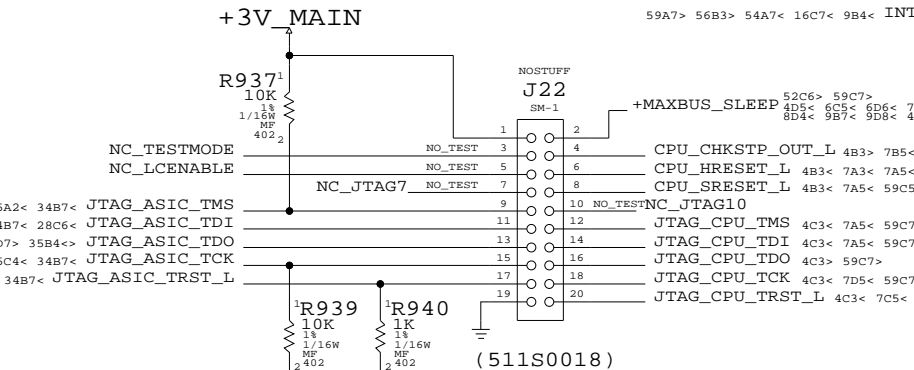
CPU CORE DECOUPLING



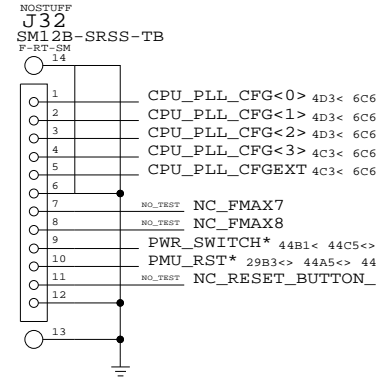
CPU CORE DECOUPLING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
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138S0541	21	CAP,CER,1UF,10%,6.3V,0402,X5R	C1022,C1027,C1011,C1008,C1010,C1025,C1009,C1002,C1023,C1017,C1031,C997,C996,C1012,C1024,C1001,C1028,C1018,C1096,C1097,C1098	1_25GHZ_DECOUP

PULLDOWN ON TRST* STRONGER TO OVERCOME POSSIBLE LEAKAGE



FMAX DEBUG CONNECTOR



LA CONS & ESP

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INTREPID BOOT STRAPS

INTREPID V1.1 IS 133MHZ ONLY

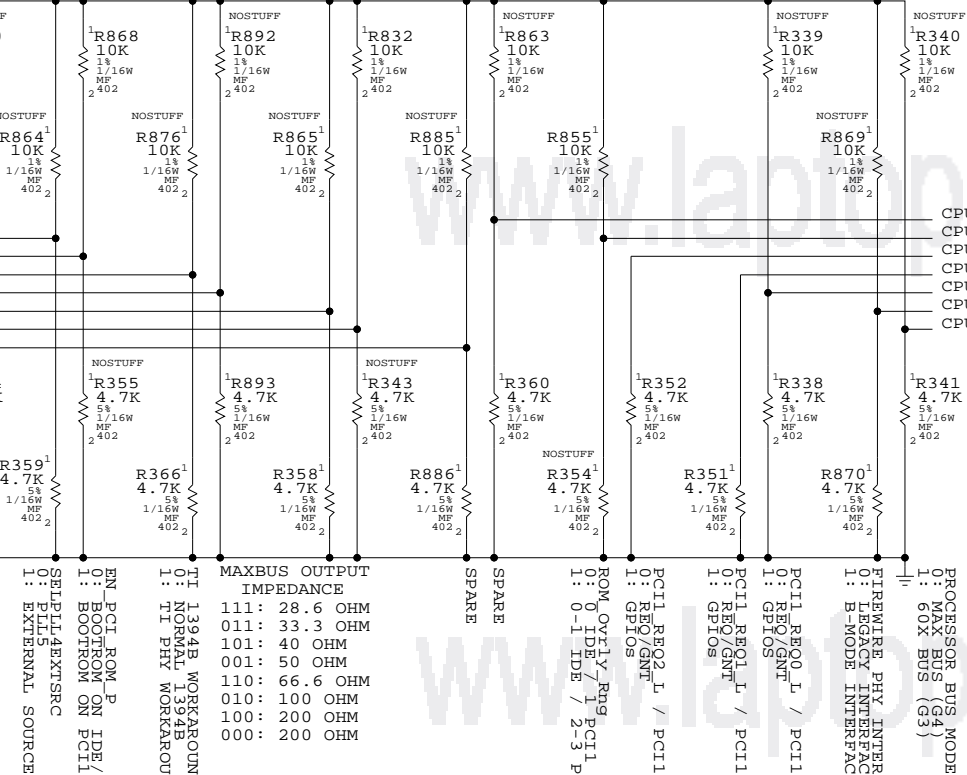
52C6> 46D4< 45D2<>
8D4< 8D1< 8A3<>
7A3< 6D6< 6C5< 4D5<
7C7< 7C5< 7C3< 7B3<
44D2< 44D1< 44B7< 8B7<
52C7>

56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<48>
56D3> 9B1<> 8C4<> 5B4<> CPU_DATA<49>
56D3> 9B1<> 8C8<> 5B4<> CPU_DATA<50>
56D3> 9B1<> 8C8<> 5B4<> CPU_DATA<51>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<52>
56D3> 9B1<> 8C7<> 5B4<> CPU_DATA<53>
56D3> 9B1<> 8D7<> 5B4<> CPU_DATA<54>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<55>

45D2<> 44D2< 44D1< 44B7<
7C3< 7B3< 7A3< 6D6< 6C5< 4D5<
9D8< 8D4< 8D1< 8A3<> 7C7< 7C5<
52C7> 52C6> 46D4<

56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<32>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<33>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<34>
56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<35>
56D3> 9C1<> 8D4<> 5C4<> CPU_DATA<36>

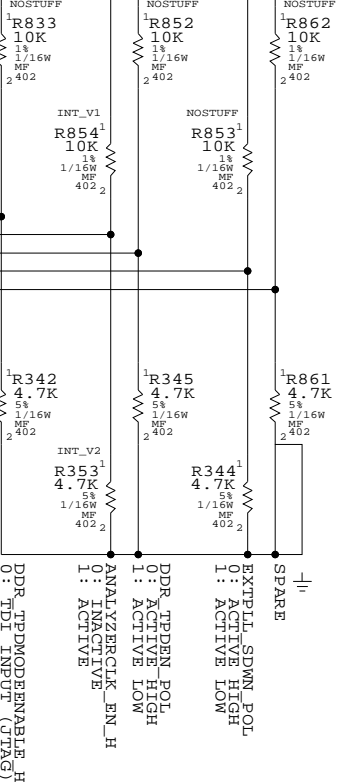
BITS 48 - 63



MAXBUS OUTPUT IMPEDANCE
111: 28.6 OHM
011: 33.3 OHM
101: 40 OHM
001: 50 OHM
110: 66.6 OHM
010: 100 OHM
100: 200 OHM
000: 200 OHM

PROCESSOR BUS MODE
1: 6X BUS (G3)

BITS 32 - 39



DPR_TPMODENABLE_H
0: INACTIVE
1: TDI OUTPUT

ANALYZERCLK_EN_H
1: ACTIVE
0: INACTIVE

EXTPLI_SPWRN_POL
1: ACTIVE HIGH
0: ACTIVE LOW

DPR_TPMODENABLE_H
0: INACTIVE
1: TDI OUTPUT

52D3> 30D5< 28D6<> 16D6< +1_5V_INTREPID_PLL

+1_5V_INTREPID_PLL7 52D3>

56D3> 8B4<> 7C7< 4D7> CPU_BR_L
56D3> 8B4<> 7B7< 4D7> CPU_BG_L

56D3> 8B7<> 7C7< 4D7> CPU_TS_L

56D3> 8B4<> 4C7<> CPU_ADDR<0>
56D3> 8B5<> 4C7<> CPU_ADDR<1>
56D3> 8B4<> 4C7<> CPU_ADDR<2>
56D3> 8B8<> 4C7<> CPU_ADDR<3>
56D3> 8B5<> 4C7<> CPU_ADDR<4>
56D3> 8B7<> 4C7<> CPU_ADDR<5>
56D3> 8C4<> 4C7<> CPU_ADDR<6>
56D3> 8B7<> 4C7<> CPU_ADDR<7>
56D3> 8C5<> 4C7<> CPU_ADDR<8>
56D3> 8B8<> 4C7<> CPU_ADDR<9>
56D3> 8C4<> 4C7<> CPU_ADDR<10>
56D3> 8C4<> 4C7<> CPU_ADDR<11>
56D3> 8B7<> 4C7<> CPU_ADDR<12>
56D3> 8B8<> 4C7<> CPU_ADDR<13>
56D3> 8B7<> 4C7<> CPU_ADDR<14>
56D3> 8B7<> 4C7<> CPU_ADDR<15>
56D3> 8B8<> 4C7<> CPU_ADDR<16>
56D3> 8B8<> 4C7<> CPU_ADDR<17>
56D3> 8B8<> 4C7<> CPU_ADDR<18>
56D3> 8B7<> 4C7<> CPU_ADDR<19>
56D3> 8B8<> 4C7<> CPU_ADDR<20>
56D3> 8C7<> 4C7<> CPU_ADDR<21>
56D3> 8C7<> 4C7<> CPU_ADDR<22>
56D3> 8C8<> 4C7<> CPU_ADDR<23>
56D3> 8B7<> 4B7<> CPU_ADDR<24>
56D3> 8B8<> 4B7<> CPU_ADDR<25>
56D3> 8C8<> 4B7<> CPU_ADDR<26>
56D3> 8C8<> 4B7<> CPU_ADDR<27>
56D3> 8C7<> 4B7<> CPU_ADDR<28>
56D3> 8C8<> 4B7<> CPU_ADDR<29>
56D3> 8C7<> 4B7<> CPU_ADDR<30>
56D3> 8C7<> 4B7<> CPU_ADDR<31>

56C3> 8C5<> 7A7< 4A7> CPU_CI_L
56C3> 7B7< 4B8< CPU_INT_GBL_L
56D3> 8B4<> 7B7< 4B7> CPU_TBST_L
56D3> 8B5<> 4B7> CPU_TSI<0>
56D3> 8B5<> 4B7> CPU_TSI<1>
56D3> 8B7< 4B7> CPU_TSI<2>
56D3> 8B4<> 7A7< 4B7> CPU_TT<0>
56D3> 8B5<> 7A7< 4B7> CPU_TT<1>
56D3> 8B4<> 7A7< 4B7> CPU_TT<2>
56D3> 8B5<> 7A7< 4B7> CPU_TT<3>
56D3> 8B4<> 7A7< 4B7> CPU_TT<4>
56C3> 8B5<> 7A7< 4B7> CPU_WT_L
56C3> 8B5<> 7B7< 4A7> CPU_AACK_L
56C3> 8B8<> 7C7< 4A7> CPU_ARTRY_L
56C3> 8B8<> 7C7< 4A7> CPU_HIT_L

56C3> 8B7<> 7D5< 4C3> CPU_QREQ_L
56C3> 8B4<> 4C3< CPU_QACK_L
44B8<> INT_SUSPEND_REQ_L
44B5<> INT_SUSPEND_ACK_L

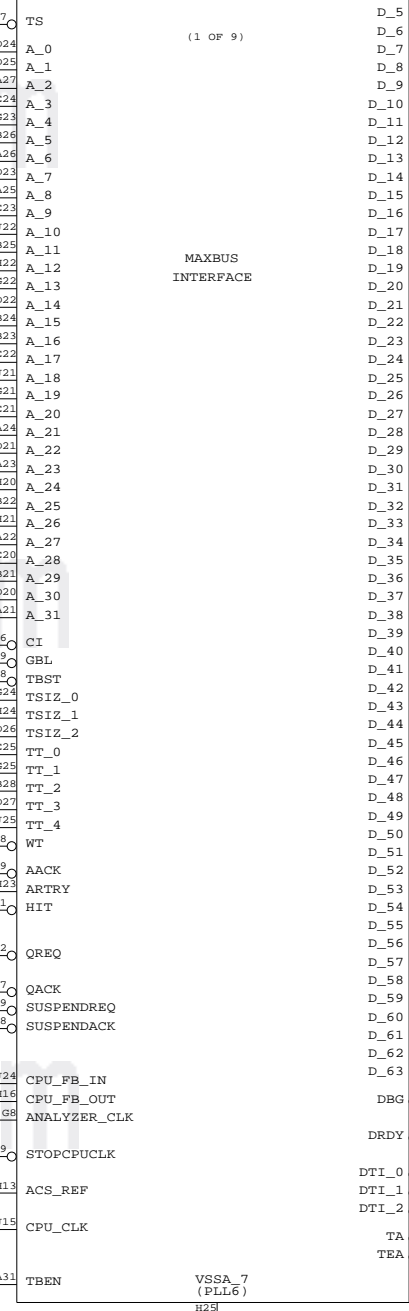
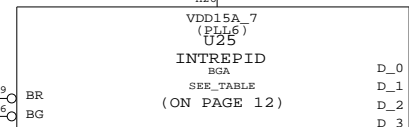
59A7> 56B3> 54A7< 16C7< 8A2< INT_ANALYZER_CLK
44C4<> CPU_CLK_EN

56C3> 4D2< SYSCLK_CPU

56B3> CPU_FB_PLUS3
56C3> CPU_FB_MINUS3
56C3> CPU_FBI_PLUS1
56C3> CPU_FBO_PLUS1

ADDS 2" (0.35 NS)
ADDS 1" (0.17 NS)
ADDS 3" (0.5 NS)

ALLOWS ADJUSTING FB CLOCK FROM -3" (0.5 NS) TO +2" (0.35 NS) IN 1" (0.17 NS) INCREMENTS
PLACE ALL SERPENTINES ON INTERNAL LAYER



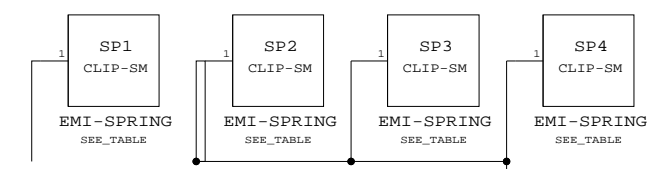
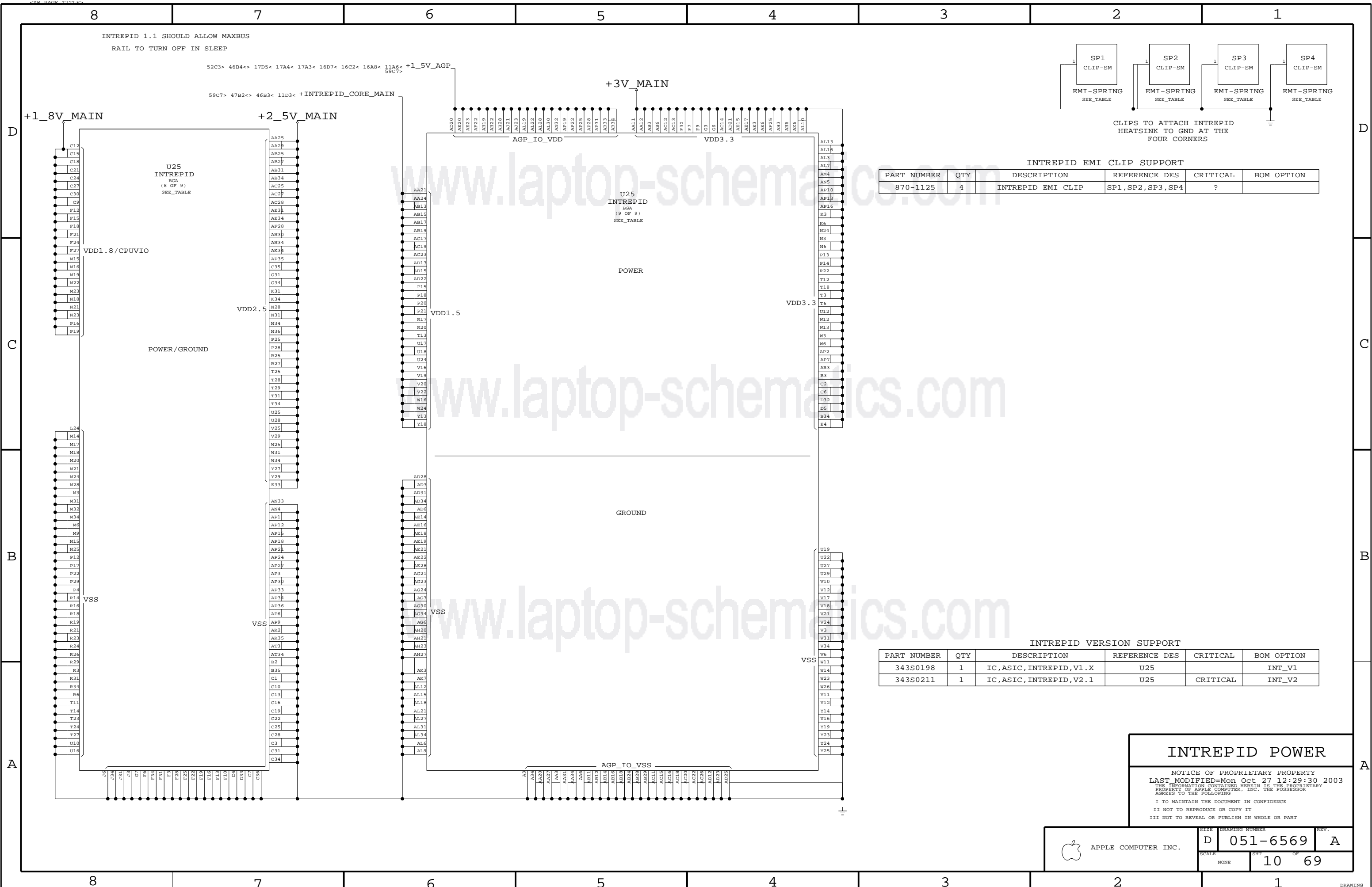
(1 OF 9)

VIN = INTREPID VCORE (1.7V)
VOUT = MAXBUS RAIL (1.8V)

INTREPID MAX

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SHEET		OF	
9		69	



CLIPS TO ATTACH INTREPID HEATSINK TO GND AT THE FOUR CORNERS

INTREPID EMI CLIP SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1125	4	INTREPID EMI CLIP	SP1, SP2, SP3, SP4	?	

INTREPID VERSION SUPPORT

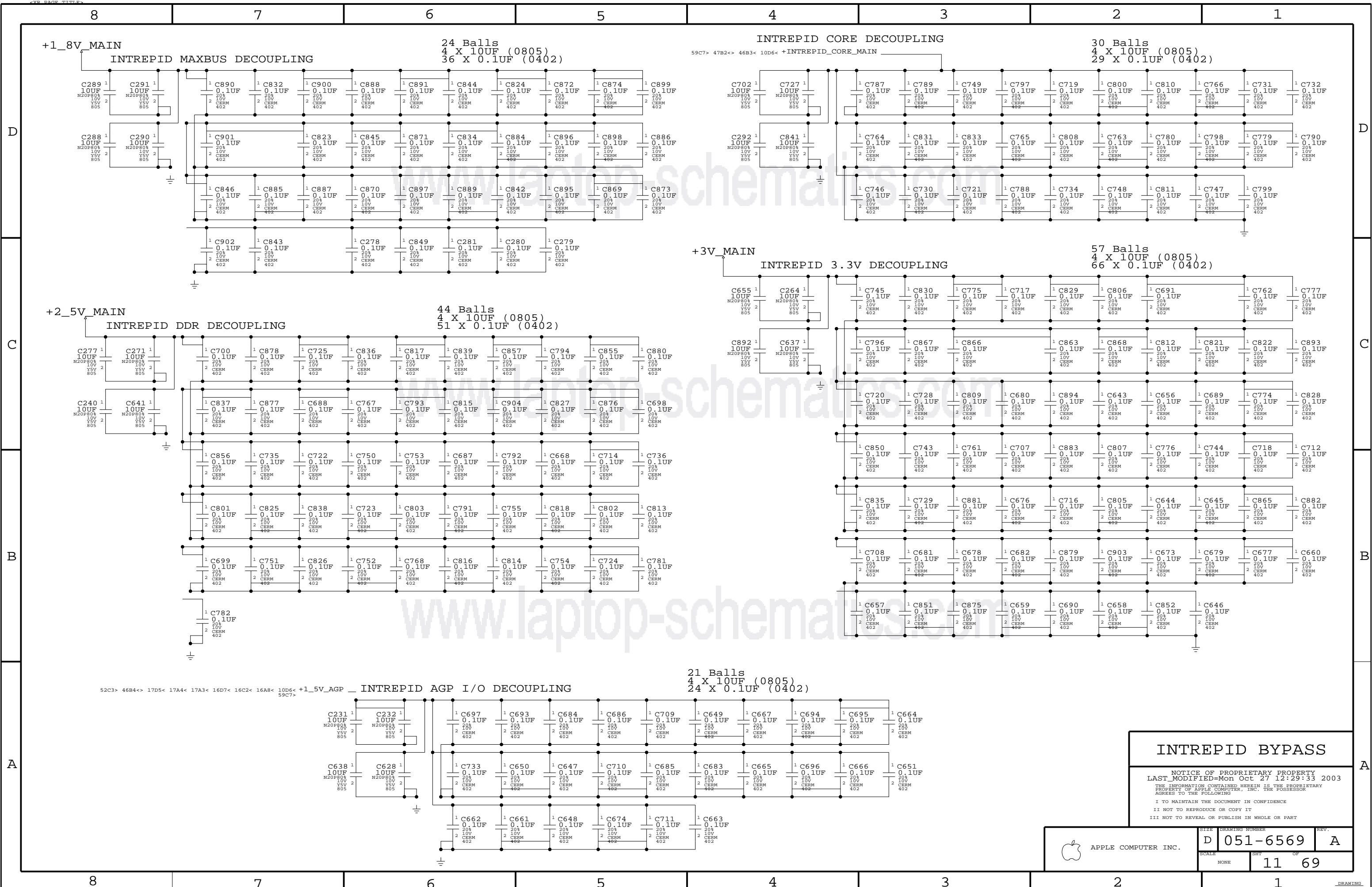
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0198	1	IC, ASIC, INTREPID, V1.X	U25		INT_V1
343S0211	1	IC, ASIC, INTREPID, V2.1	U25	CRITICAL	INT_V2

INTREPID POWER

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NONE	10		69



+1_8V_MAIN

INTREPID MAXBUS DECOUPLING

24 Balls
 4 X 10UF (0805)
 36 X 0.1UF (0402)

INTREPID CORE DECOUPLING

30 Balls
 4 X 10UF (0805)
 29 X 0.1UF (0402)

+2_5V_MAIN

INTREPID DDR DECOUPLING

44 Balls
 4 X 10UF (0805)
 51 X 0.1UF (0402)

+3V_MAIN

INTREPID 3.3V DECOUPLING

57 Balls
 4 X 10UF (0805)
 66 X 0.1UF (0402)

INTREPID AGP I/O DECOUPLING

21 Balls
 4 X 10UF (0805)
 24 X 0.1UF (0402)

INTREPID BYPASS

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SCALE: NONE SHIT OF 11 69

APPLE COMPUTER INC. DRAWING NUMBER: D 051-6569 REV. A

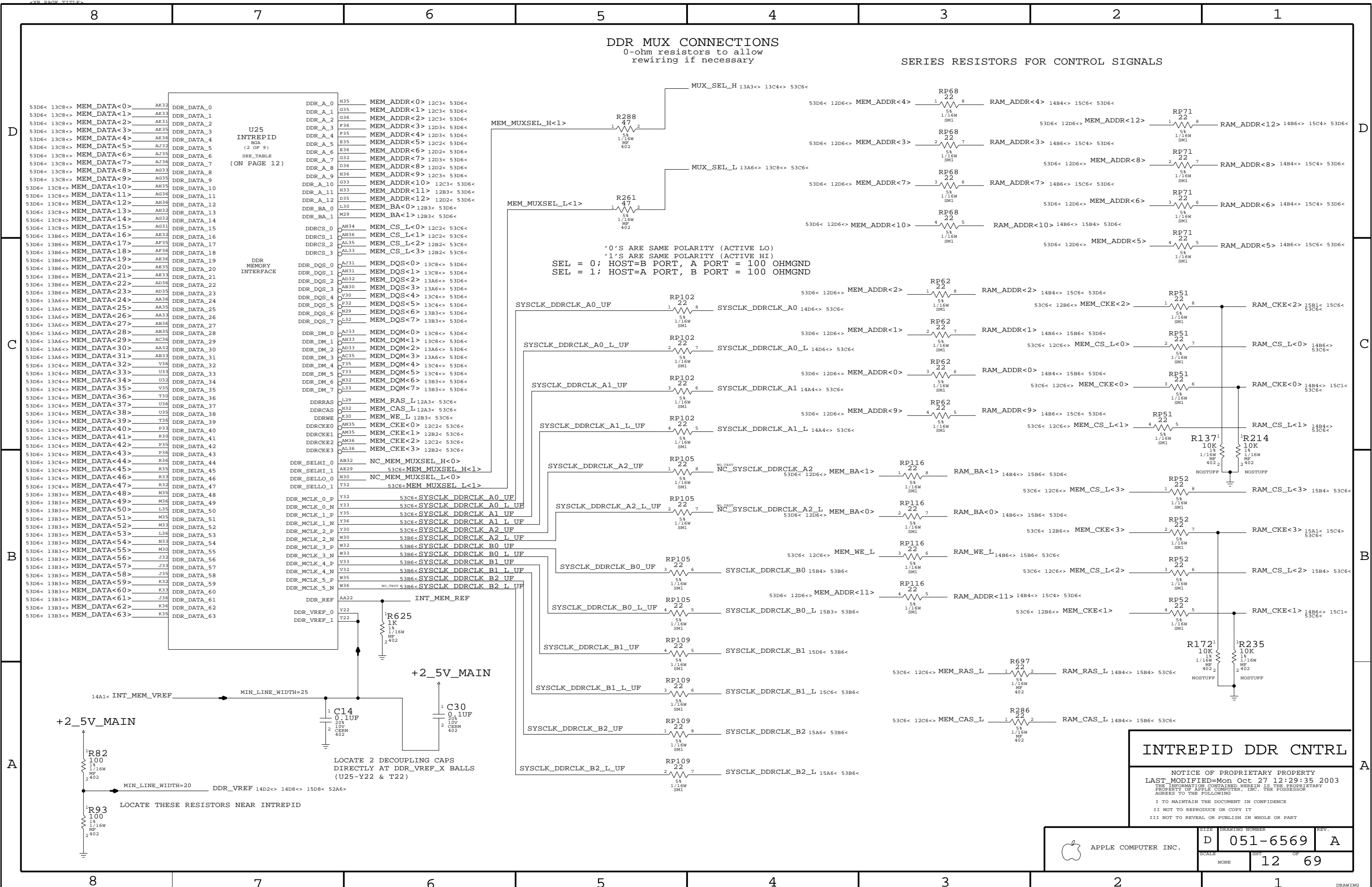
SCALE: NONE SHIT OF 11 69

APPLE COMPUTER INC. DRAWING NUMBER: D 051-6569 REV. A

DDR MUX CONNECTIONS

0-ohm resistors to allow rewiring if necessary

SERIES RESISTORS FOR CONTROL SIGNALS



D

C

B

A

D

C

B

A

U25
INTREPID
BGA
(2 OF 9)
SEE TABLE
(ON PAGE 12)

DDR
MEMORY
INTERFACE

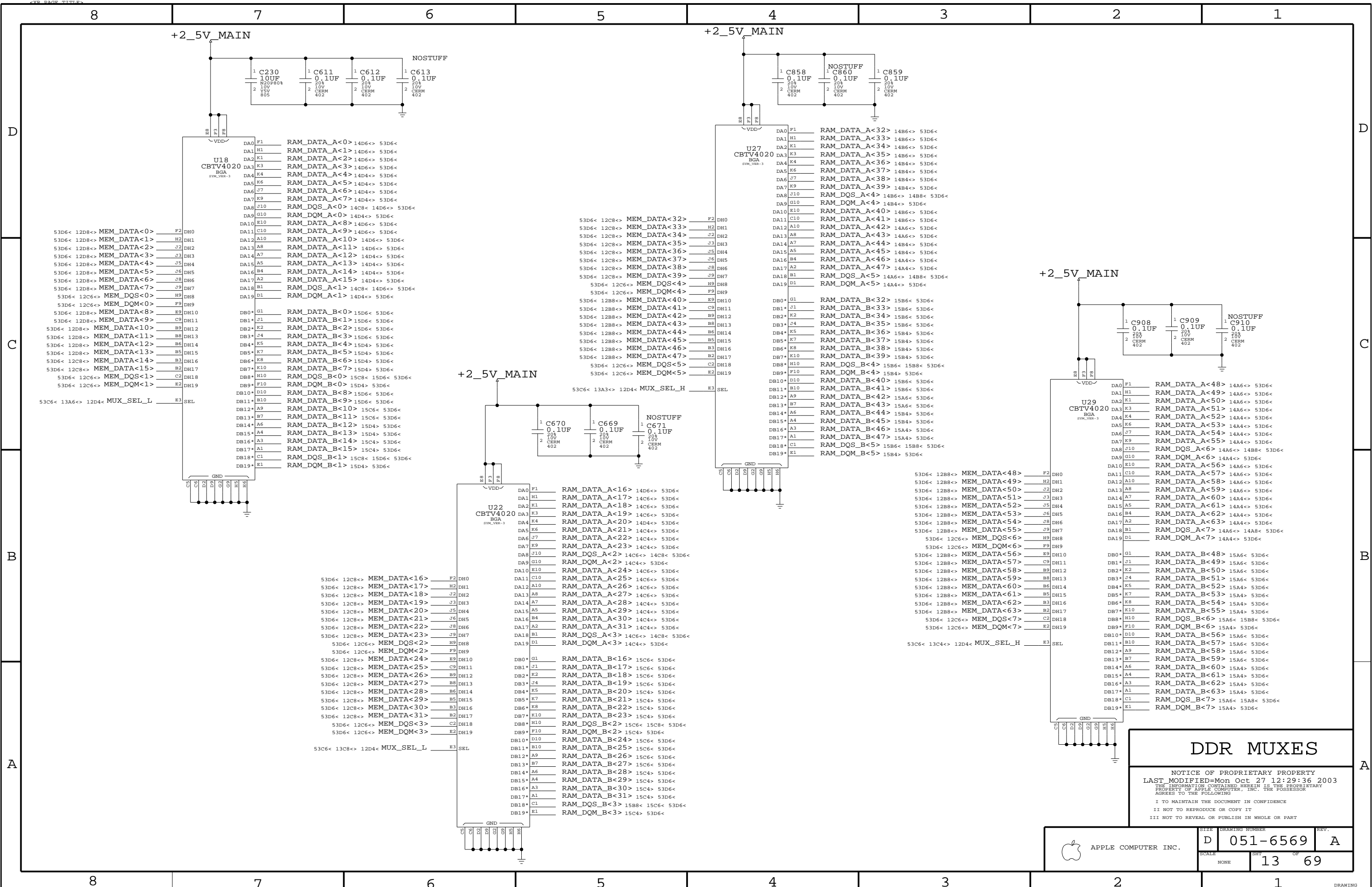
'0'S ARE SAME POLARITY (ACTIVE LO)
'1'S ARE SAME POLARITY (ACTIVE HI)
SEL = 0; HOST=B PORT, A PORT = 100 OHMGND
SEL = 1; HOST=A PORT, B PORT = 100 OHMGND

INTREPID DDR CNTRL

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DRAWING



DDR MUXES

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	SCALE: NONE	SHEET: 13	OF: 69

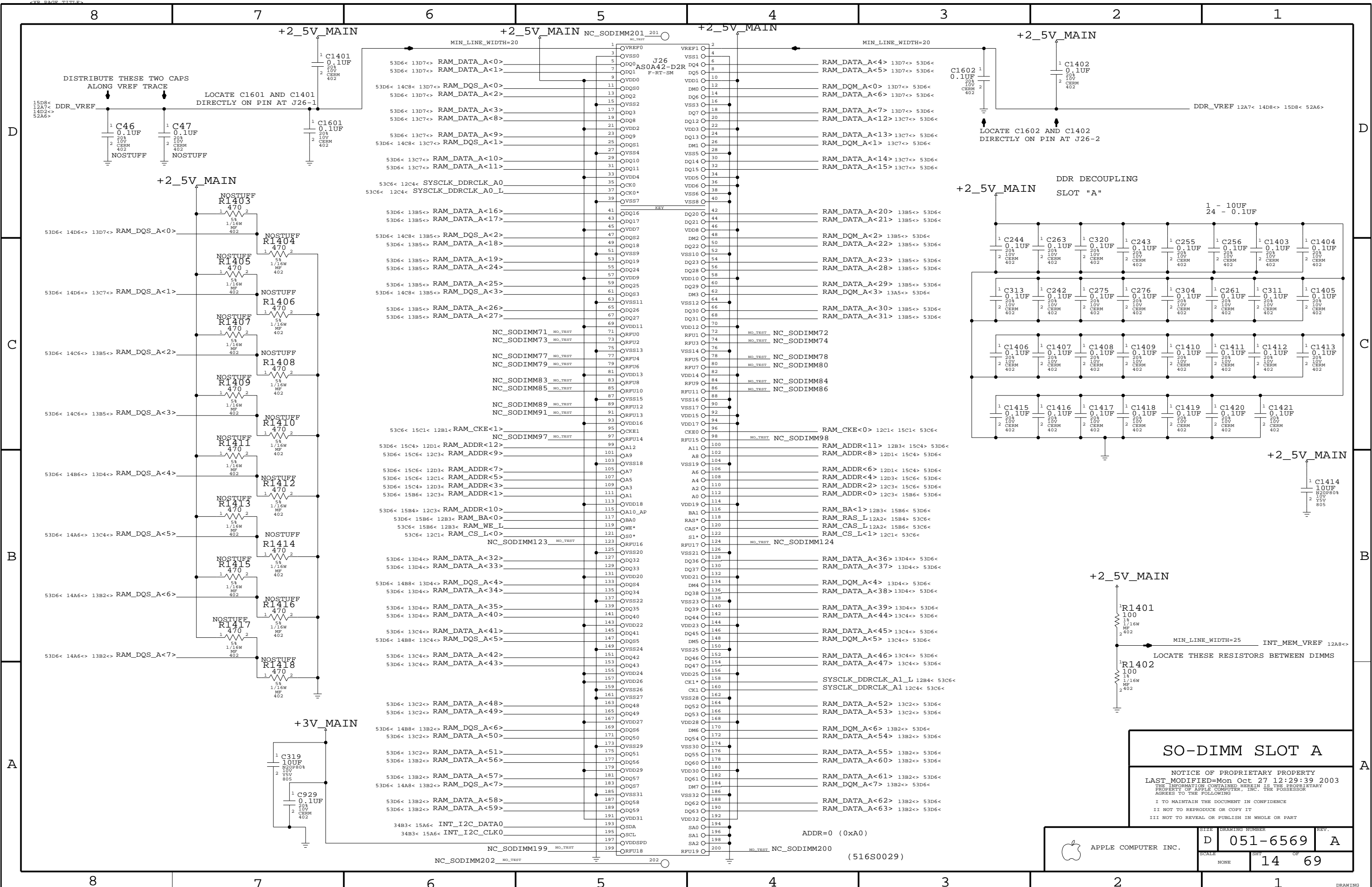
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

D
C
B
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D
C
B
A

DRAWING



D

C

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D

C

B

A

SO-DIMM SLOT A

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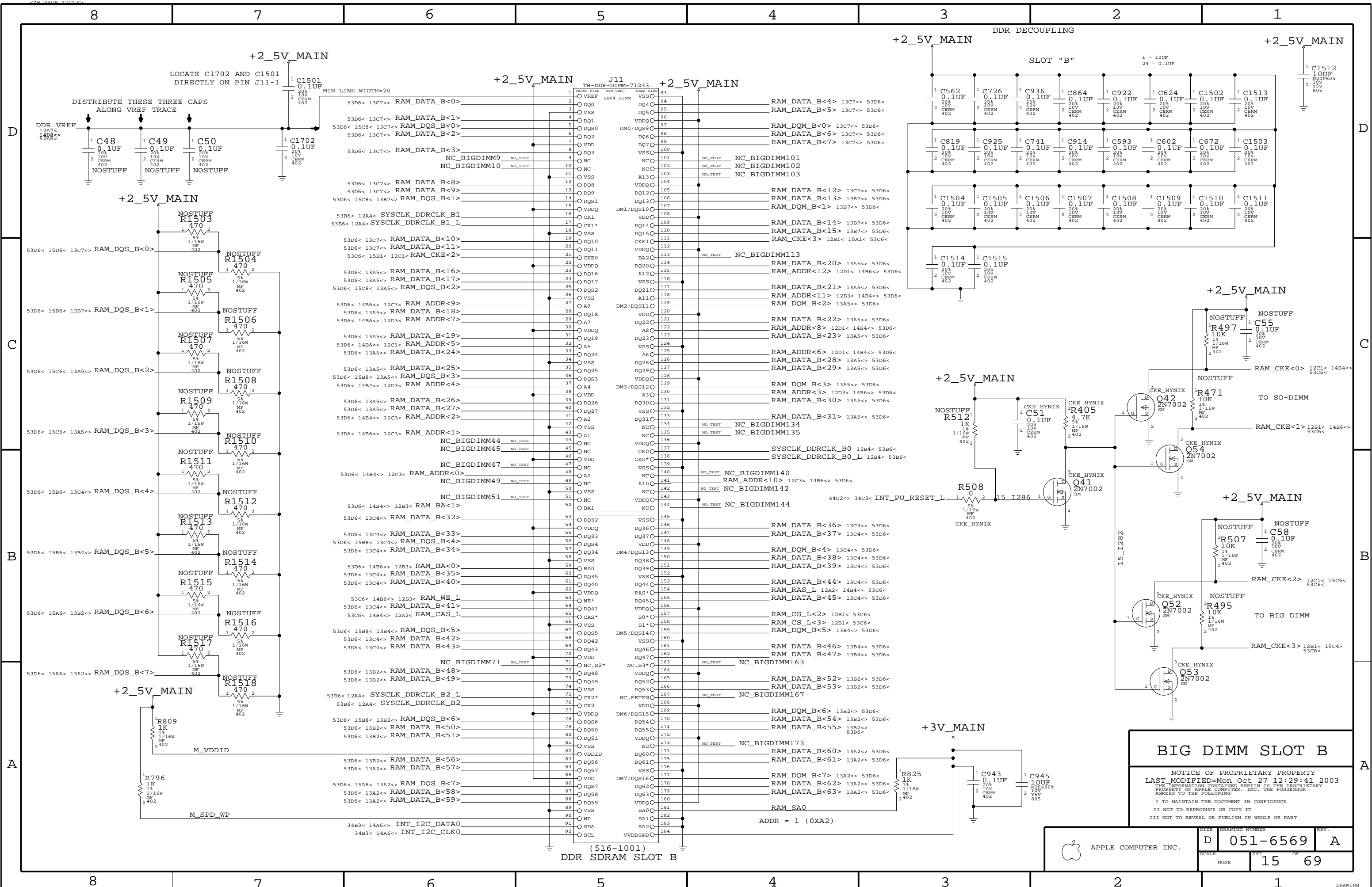
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	SCALE NONE	SHEET OF 14 69

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

DRAWING



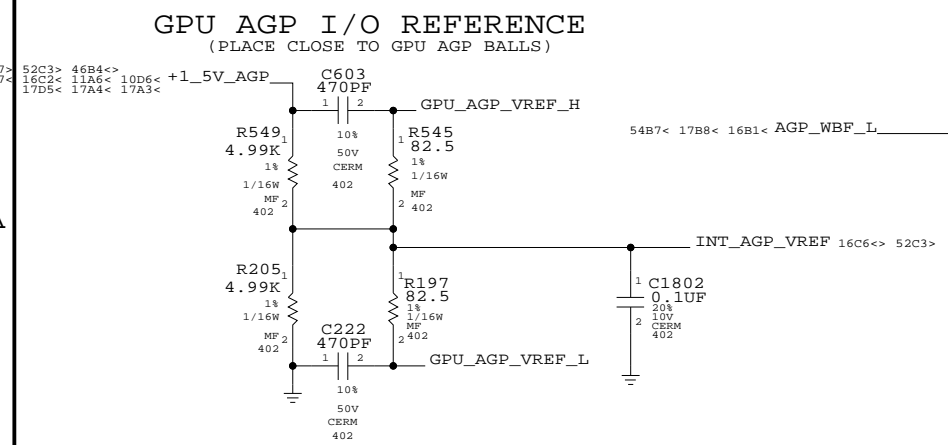
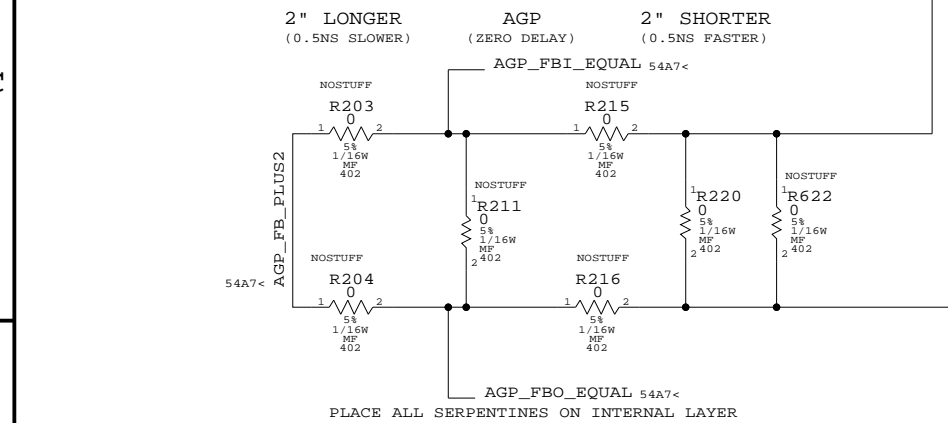
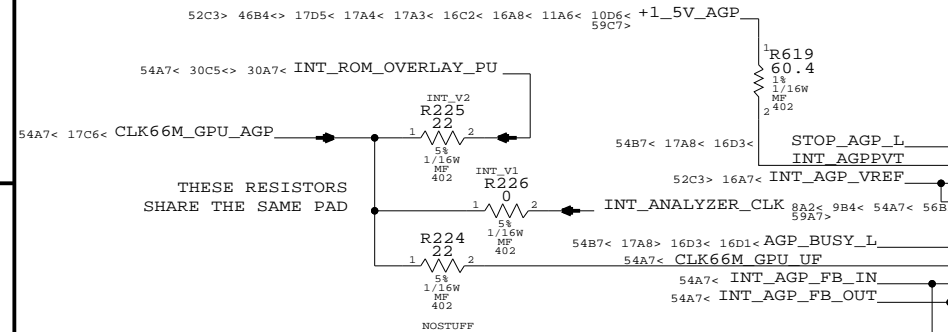
APPLE COMPUTER INC.

D 051-6569 A

SCALE NONE SHEET 15 OF 69

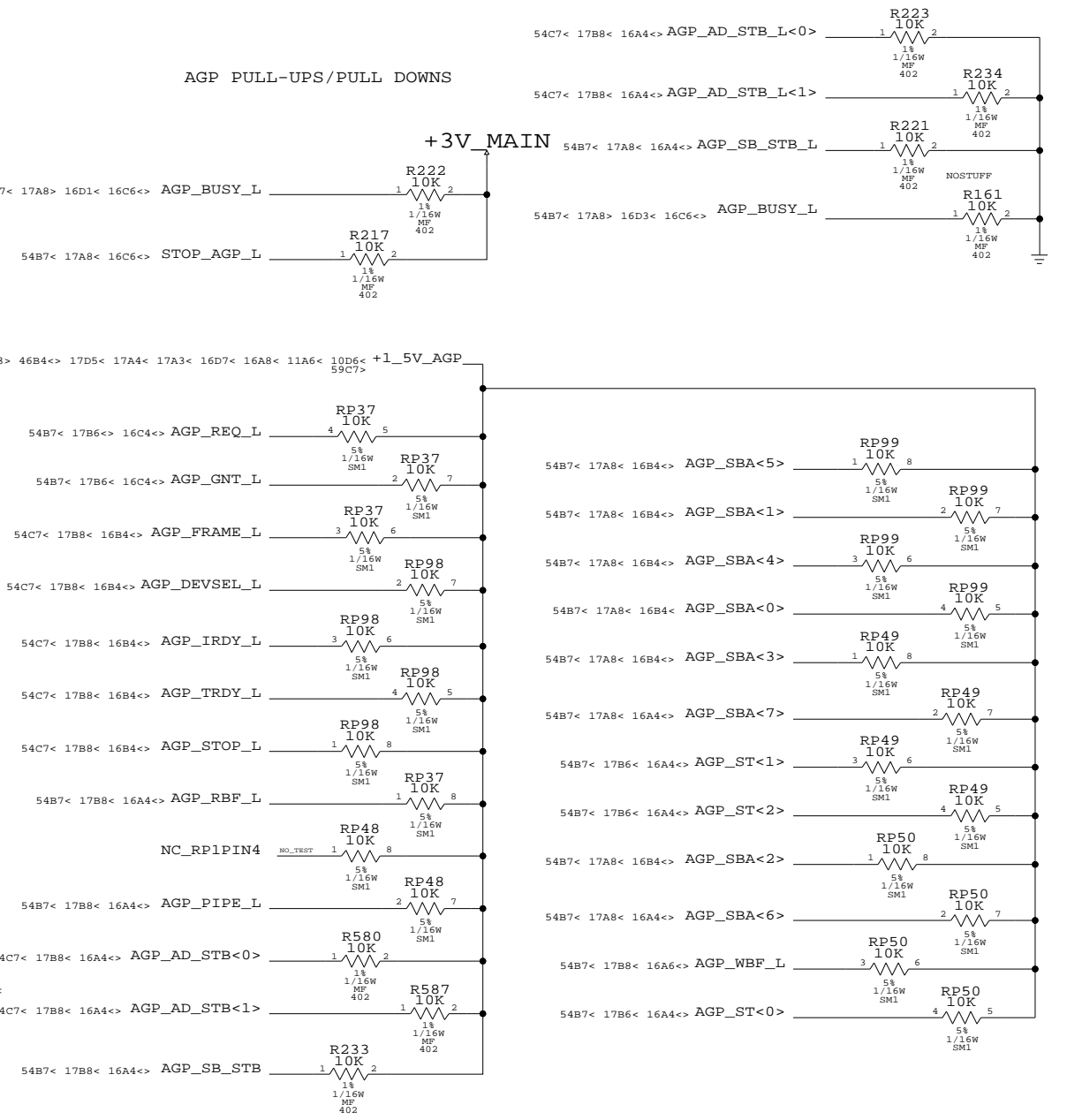
SIZE DRAWING NUMBER REV.

INTREPID AGP CLK IS 1.5V OUT
NEED 3.3V SWING FOR VIDEO CHIPS
VERSION 1 WORKAROUND IS LA CLOCK
VERSION 2 WORKAROUND IS UNUSED PIN



U25 INTREPID BGA (3 OF 9) (ON PAGE 12)

AGPREQ	AT33	AGP_REQ_L	16C3< 17B6<	54B7<
AGPGNT	AM29	AGP_GNT_L	16C3< 17B6<	54B7<
AGPAD0	AR19	AGP_AD<0>	17D8< 54C7<	
AGPAD1	AM19	AGP_AD<1>	17D8< 54C7<	
AGPAD2	AT20	AGP_AD<2>	17D8< 54C7<	
AGPAD3	AR20	AGP_AD<3>	17D8< 54C7<	
AGPAD4	AT21	AGP_AD<4>	17D8< 54C7<	
AGPAD5	AN20	AGP_AD<5>	17D8< 54C7<	
AGPAD6	AR21	AGP_AD<6>	17D8< 54C7<	
AGPAD7	AN21	AGP_AD<7>	17D8< 54C7<	
AGPAD8	AM21	AGP_AD<8>	17D8< 54C7<	
AGPAD9	AT22	AGP_AD<9>	17D8< 54C7<	
AGPAD10	AR22	AGP_AD<10>	17D8< 54C7<	
AGPAD11	AN22	AGP_AD<11>	17D8< 54C7<	
AGPAD12	AM22	AGP_AD<12>	17D8< 54C7<	
AGPAD13	AT23	AGP_AD<13>	17D8< 54C7<	
AGPAD14	AR23	AGP_AD<14>	17D8< 54C7<	
AGPAD15	AT24	AGP_AD<15>	17D8< 54C7<	
AGPAD16	AM23	AGP_AD<16>	17C8< 54C7<	
AGPAD17	AR24	AGP_AD<17>	17C8< 54C7<	
AGPAD18	AT25	AGP_AD<18>	17C8< 54C7<	
AGPAD19	AM24	AGP_AD<19>	17C8< 54C7<	
AGPAD20	AN24	AGP_AD<20>	17C8< 54C7<	
AGPAD21	AR25	AGP_AD<21>	17C8< 54C7<	
AGPAD22	AL24	AGP_AD<22>	17C8< 54C7<	
AGPAD23	AR26	AGP_AD<23>	17C8< 54C7<	
AGPAD24	AT26	AGP_AD<24>	17C8< 54C7<	
AGPAD25	AM25	AGP_AD<25>	17C8< 54C7<	
AGPAD26	AN26	AGP_AD<26>	17C8< 54C7<	
AGPAD27	AM26	AGP_AD<27>	17C8< 54C7<	
AGPAD28	AR27	AGP_AD<28>	17C8< 54C7<	
AGPAD29	AT27	AGP_AD<29>	17C8< 54C7<	
AGPAD30	AR28	AGP_AD<30>	17C8< 54C7<	
AGPAD31	AN27	AGP_AD<31>	17C8< 54C7<	
AGPCBE_0	AM20	AGP_CBE<0>	17C8< 54C7<	
AGPCBE_1	AT23	AGP_CBE<1>	17C8< 54C7<	
AGPCBE_2	AN24	AGP_CBE<2>	17C8< 54C7<	
AGPCBE_3	AL25	AGP_CBE<3>	17C8< 54C7<	
AGPPAR	AT29	AGP_PAR	17B8< 54B7<	
AGPFRAME	AN28	AGP_FRAME_L	16C3< 17B8<	54C7<
AGPTRDY	AR29	AGP_TRDY_L	16B3< 17B8<	54C7<
AGPIRDY	AT28	AGP_IRDY_L	16C3< 17B8<	54C7<
AGPSTOP	AM28	AGP_STOP_L	16B3< 17B8<	54C7<
AGPDEVSEL	AM27	AGP_DEVSEL_L	16C3< 17B8<	54C7<
AGP_SBA0	AT32	AGP_SBA<0>	16C1< 17A8<	54B7<
AGP_SBA1	AR32	AGP_SBA<1>	16C1< 17A8<	54B7<
AGP_SBA2	AM31	AGP_SBA<2>	16B1< 17A8<	54B7<
AGP_SBA3	AN31	AGP_SBA<3>	16C1< 17A8<	54B7<
AGP_SBA4	AR31	AGP_SBA<4>	16C1< 17A8<	54B7<
AGP_SBA5	AT31	AGP_SBA<5>	16C1< 17A8<	54B7<
AGP_SBA6	AM30	AGP_SBA<6>	16B1< 17A8<	54B7<
AGP_SBA7	AN30	AGP_SBA<7>	16B1< 17A8<	54B7<
AGP_SB_STB_P	AN25	AGP_SB_STB	16B3< 17B8<	54B7<
AGP_SB_STB_N	AG25	AGP_SB_STB_L	16D1< 17A8<	54B7<
AGP_ST0	AN29	AGP_ST<0>	16B1< 17B6<	54B7<
AGP_ST1	AT30	AGP_ST<1>	16B1< 17B6<	54B7<
AGP_ST2	AR30	AGP_ST<2>	16B1< 17B6<	54B7<
AGP_AD_STB0_P	AK20	AGP_AD_STB<0>	16B3< 17B8<	54C7<
AGP_AD_STB0_N	AK19	AGP_AD_STB_L<0>	16D1< 17B8<	54C7<
AGP_AD_STB1_P	AK21	AGP_AD_STB<1>	16B3< 17B8<	54C7<
AGP_AD_STB1_N	AK22	AGP_AD_STB_L<1>	16D1< 17B8<	54C7<
AGPIPE	AL29	AGP_PIPE_L	16B3< 17B8<	54B7<
AGPRBF	AK24	AGP_RBF_L	16B3< 17B8<	54B7<

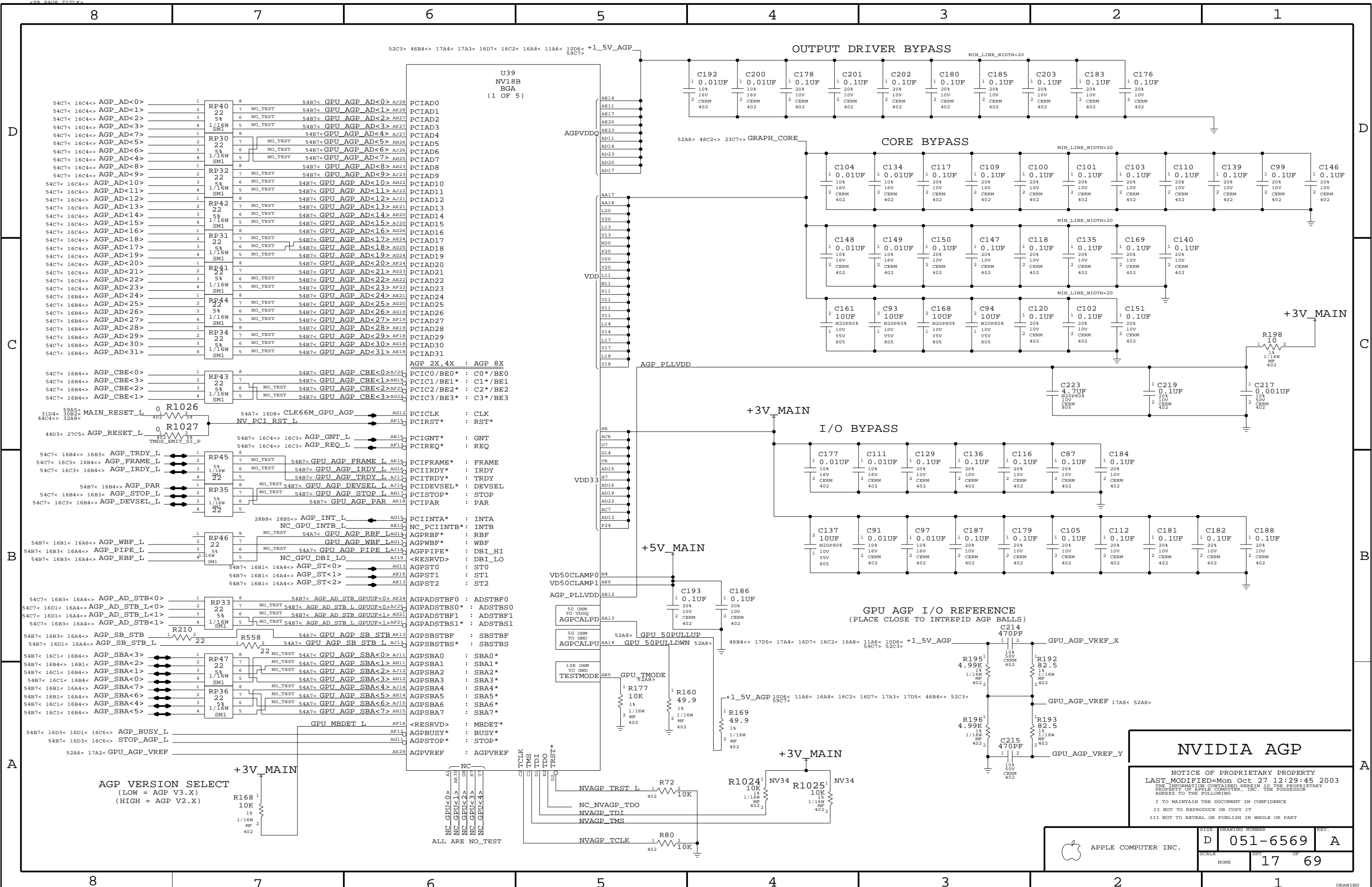


INTREPID AGP

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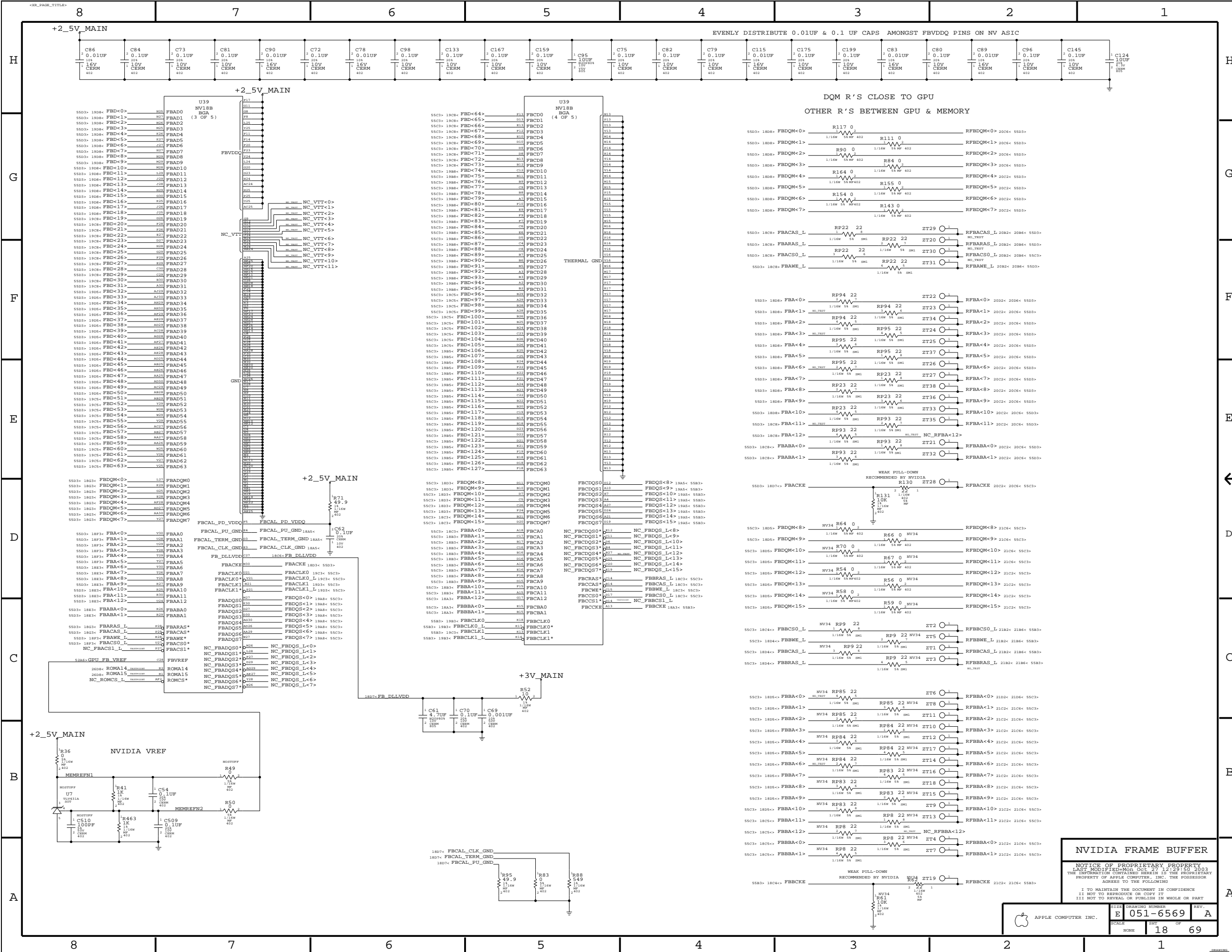
NVIDIA AGP

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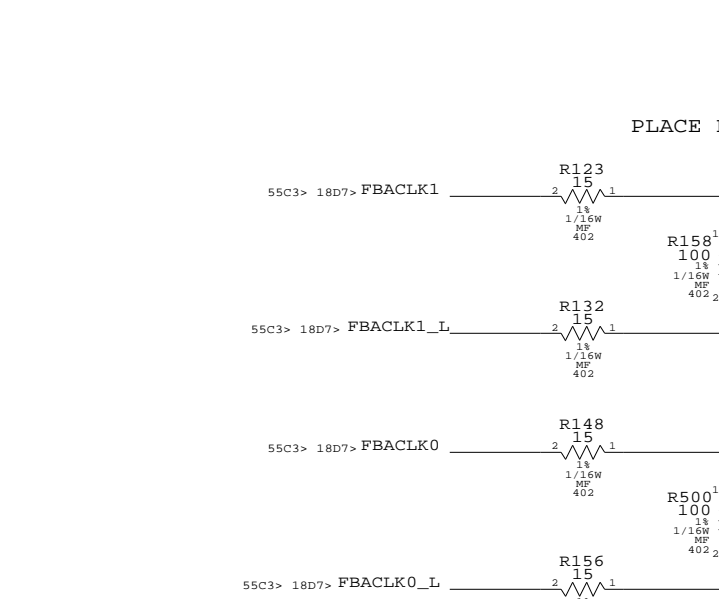
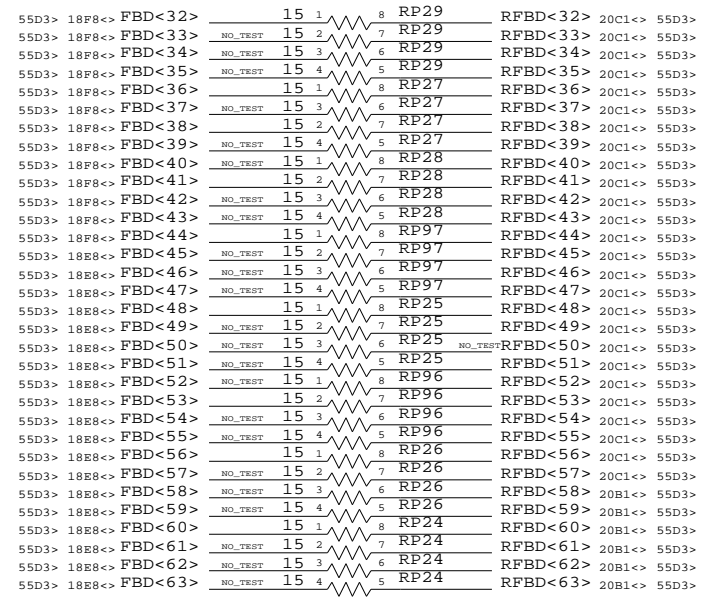
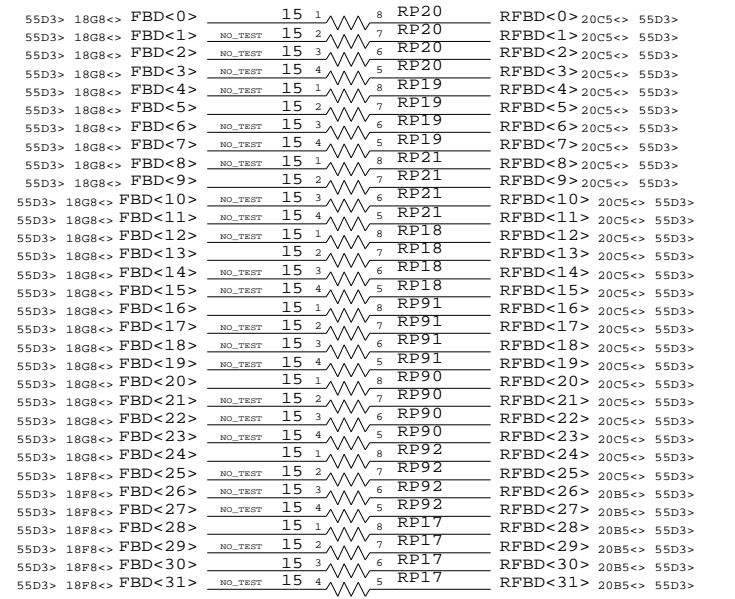


NVIDIA FRAME BUFFER

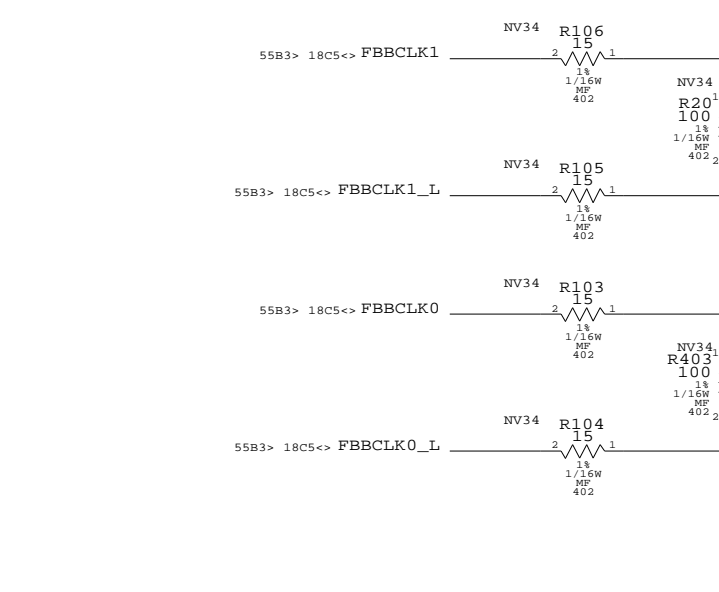
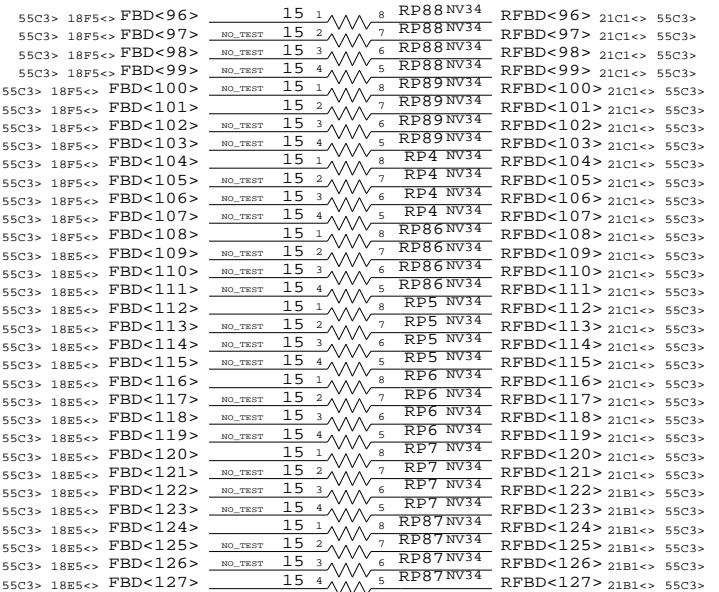
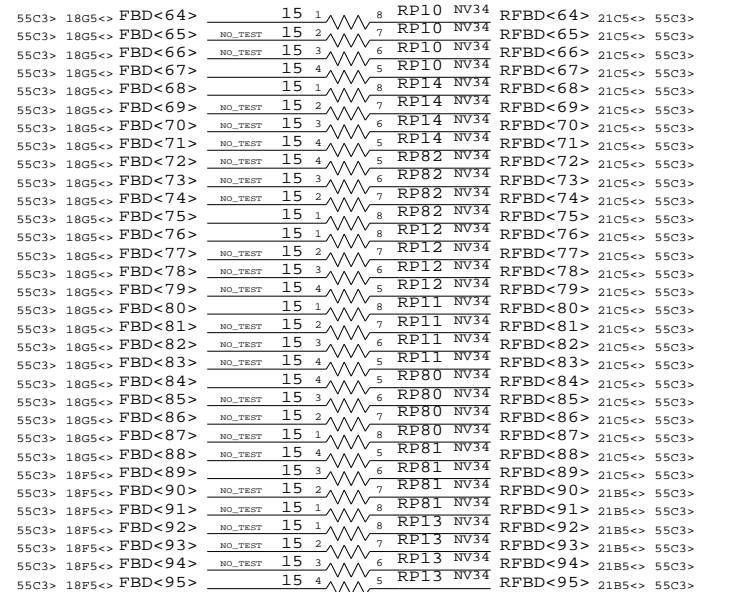
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PLACE R'S BETWEEN GPU & MEMORY



PLACE R'S CLOSE TO GPU



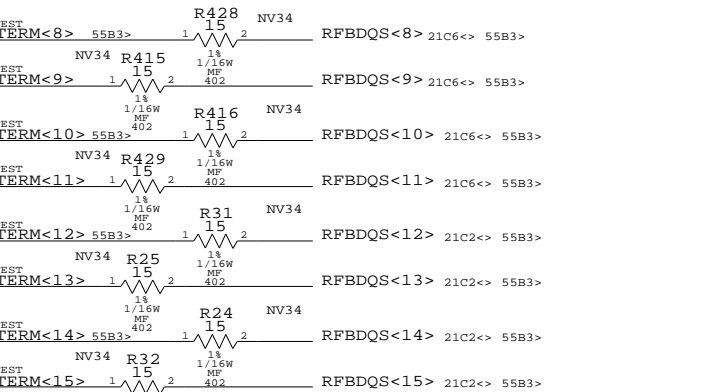
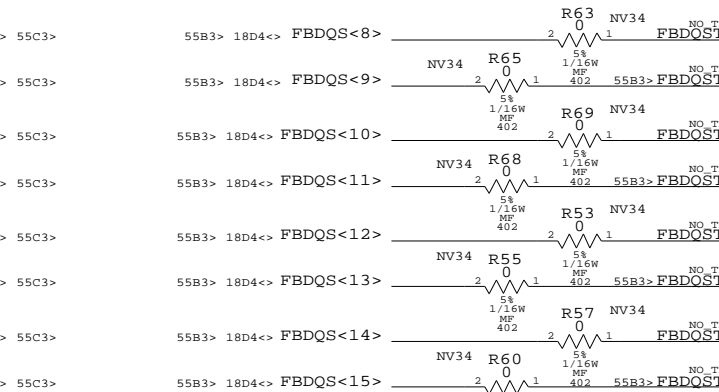
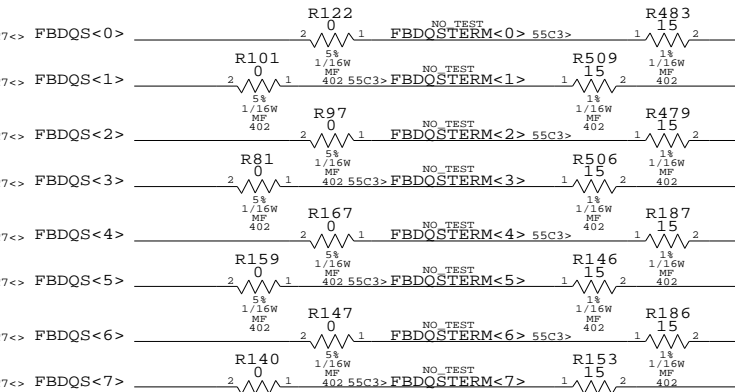
PLACE R'S CLOSE TO GPU

PLACE THESE R CLOSE TO GPU

PLACE THESE R CLOSE TO SGRAM

PLACE THESE R CLOSE TO GPU

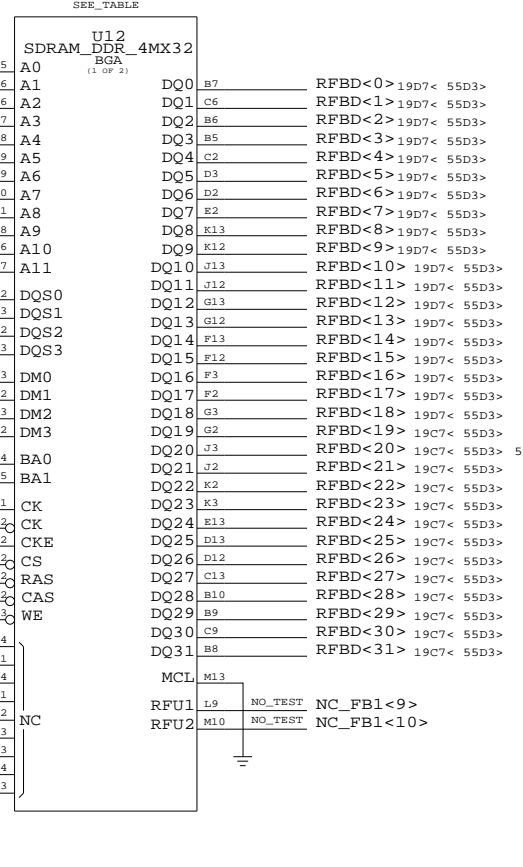
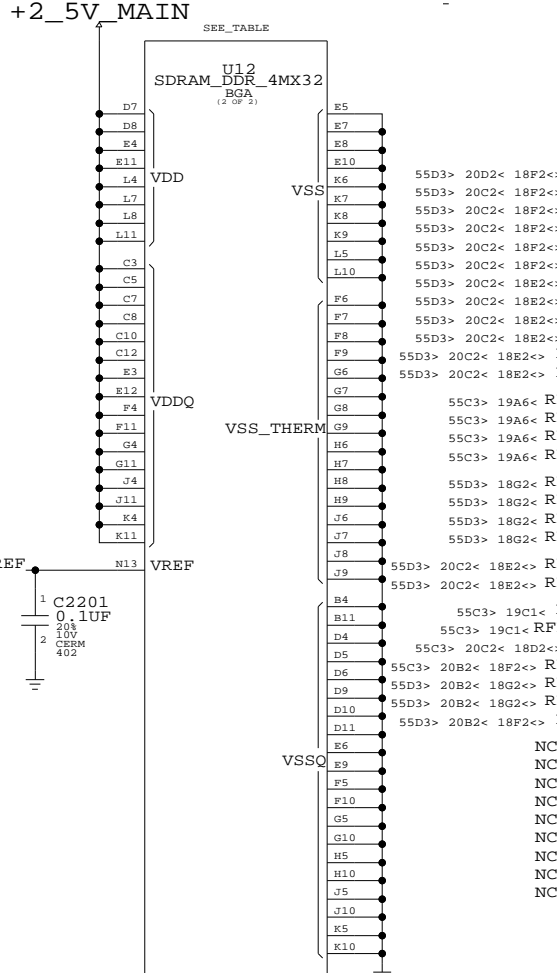
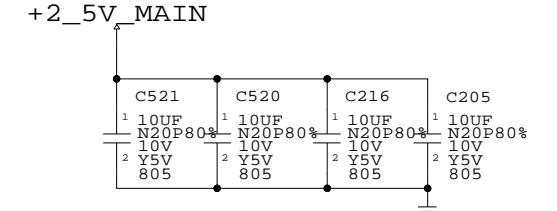
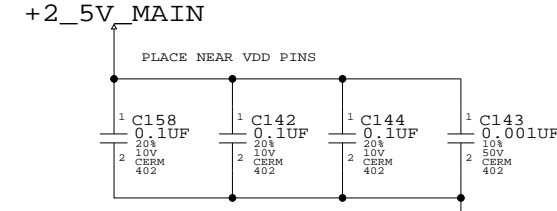
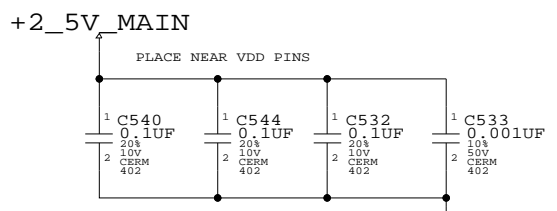
PLACE THESE R CLOSE TO SGRAM



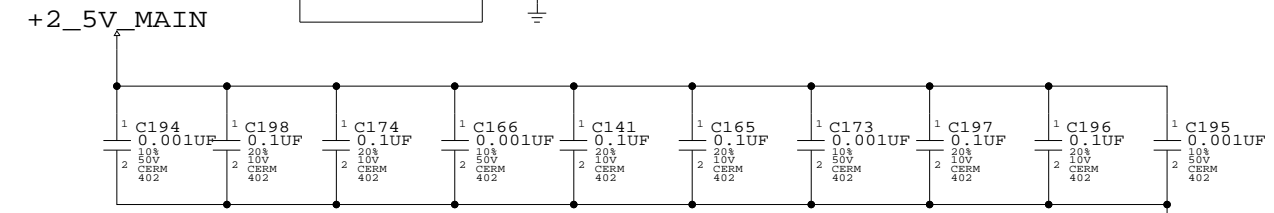
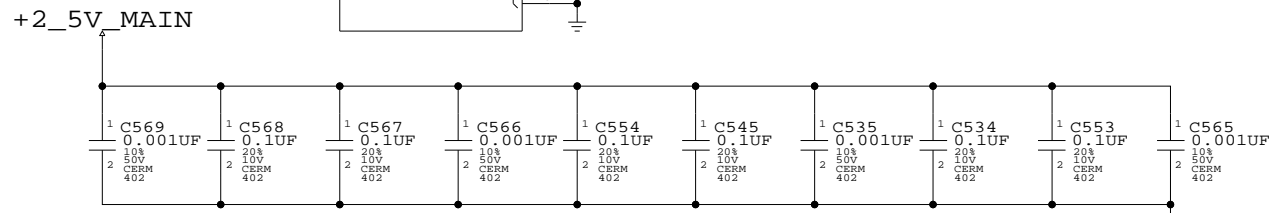
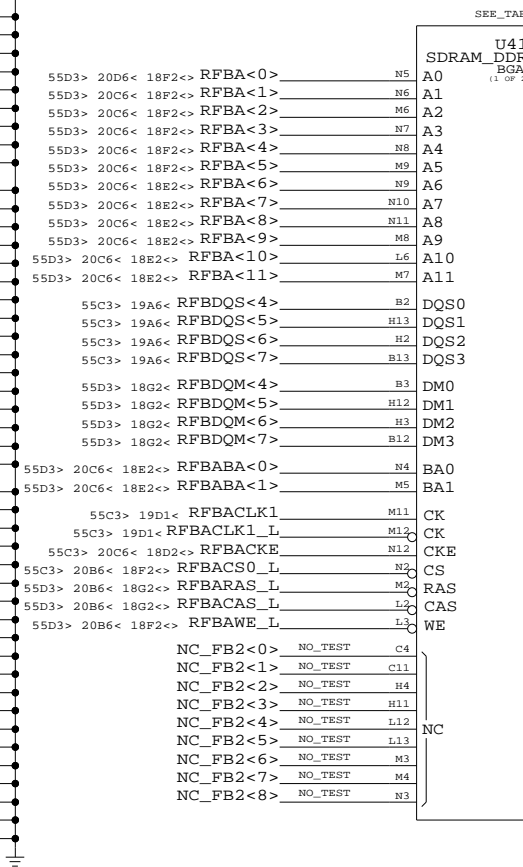
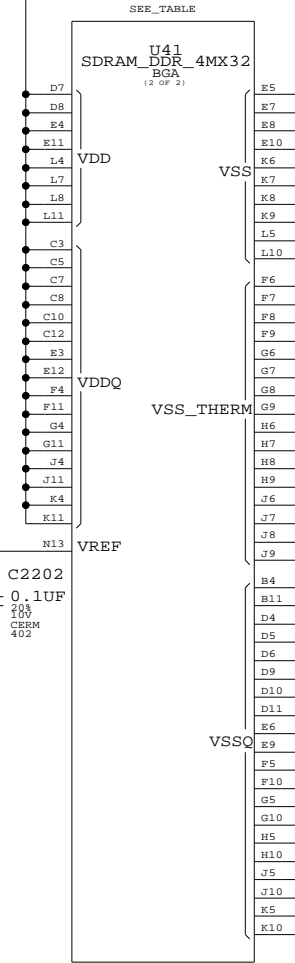
FB TERMINATION

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+2_5V MAIN



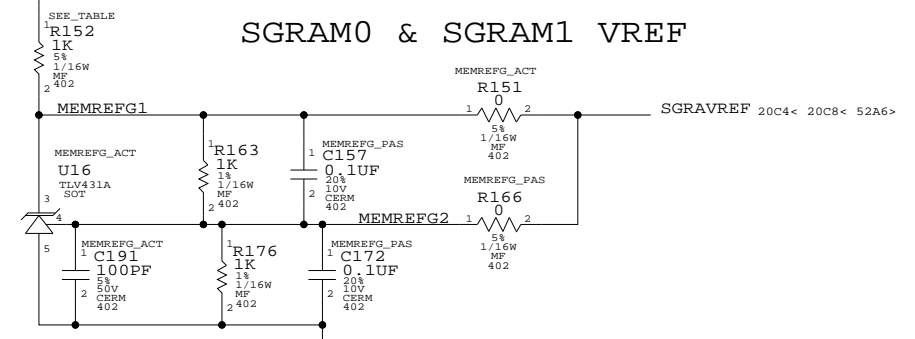
+2_5V MAIN

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	SAMSUNG_275_32M
333S0250	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	HYNIX_275_32M
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	SAMSUNG_300_32M
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	HYNIX_300_32M

SGRAM0 & SGRAM1 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R152	CRITICAL	MEMREFG_ACT
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R152		MEMREFG_PAS



SGRAM0 & SGRAM1

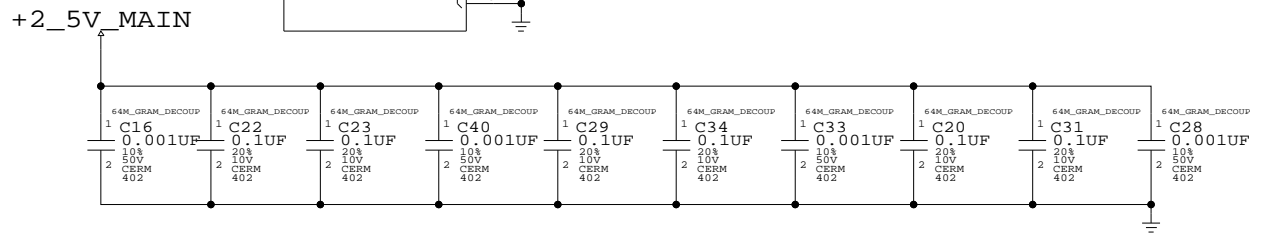
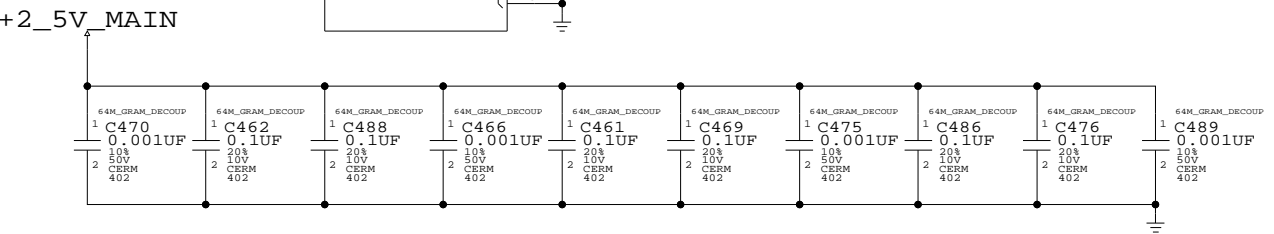
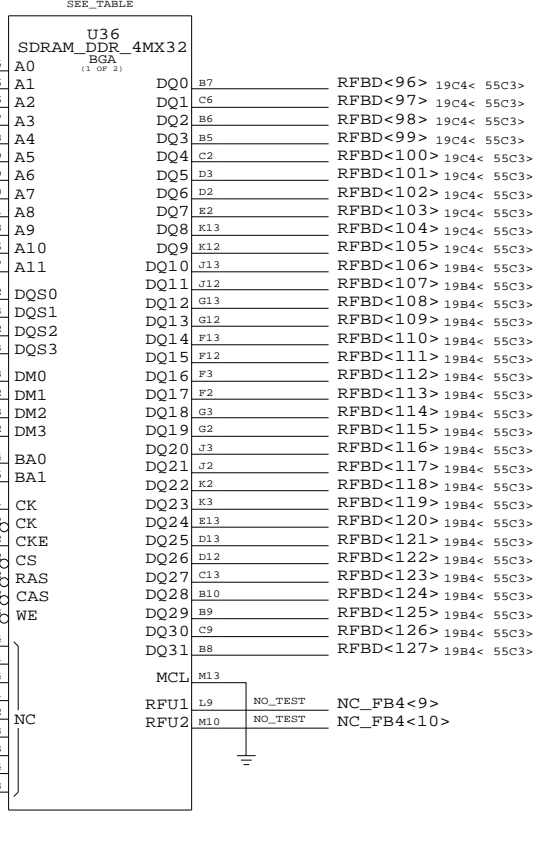
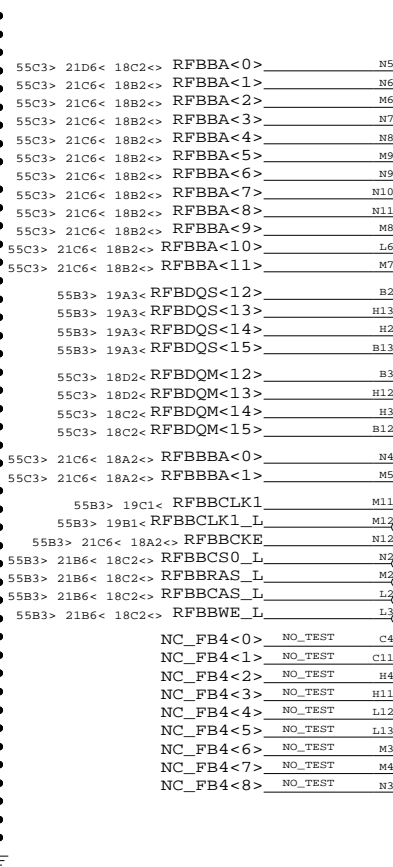
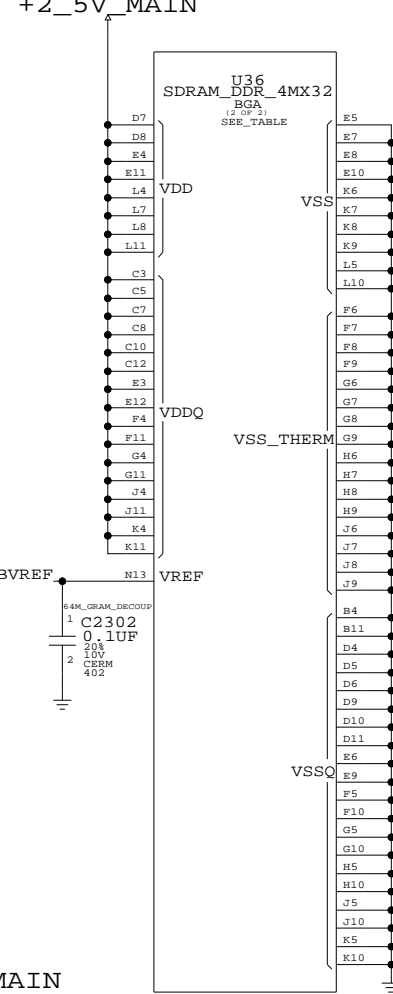
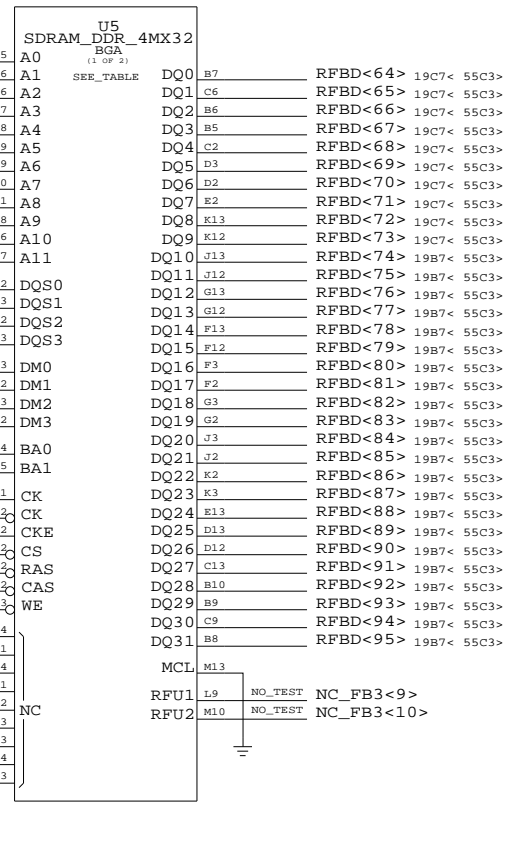
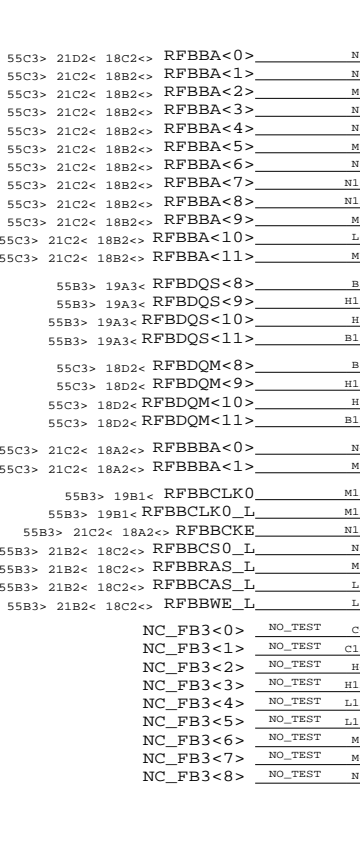
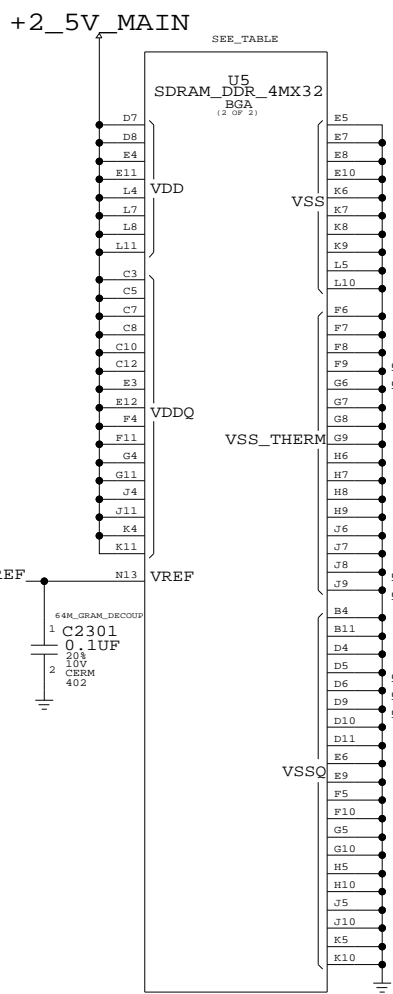
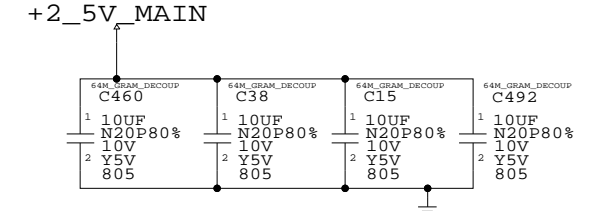
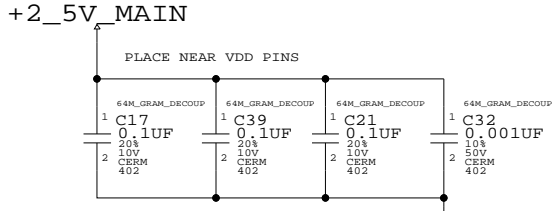
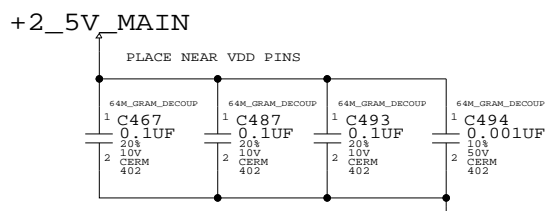
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SCALE: NONE SHEET 20 OF 69

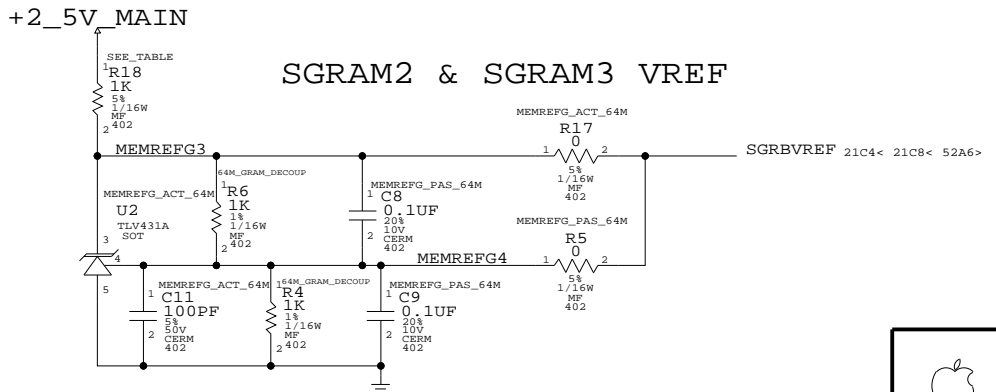


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM, 4MX32, DDR, 275MHZ	U5,U36	CRITICAL	SAMSUNG_275_64M
333S0250	2	SDRAM, 4MX32, DDR, 275MHZ	U5,U36	CRITICAL	HYNIX_275_64M
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5,U36	CRITICAL	SAMSUNG_300_64M
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5,U36	CRITICAL	HYNIX_300_64M

SGRAM2 & SGRAM3 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R18	CRITICAL	MEMREFG_ACT_64M
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R18		MEMREFG_PAS_64M



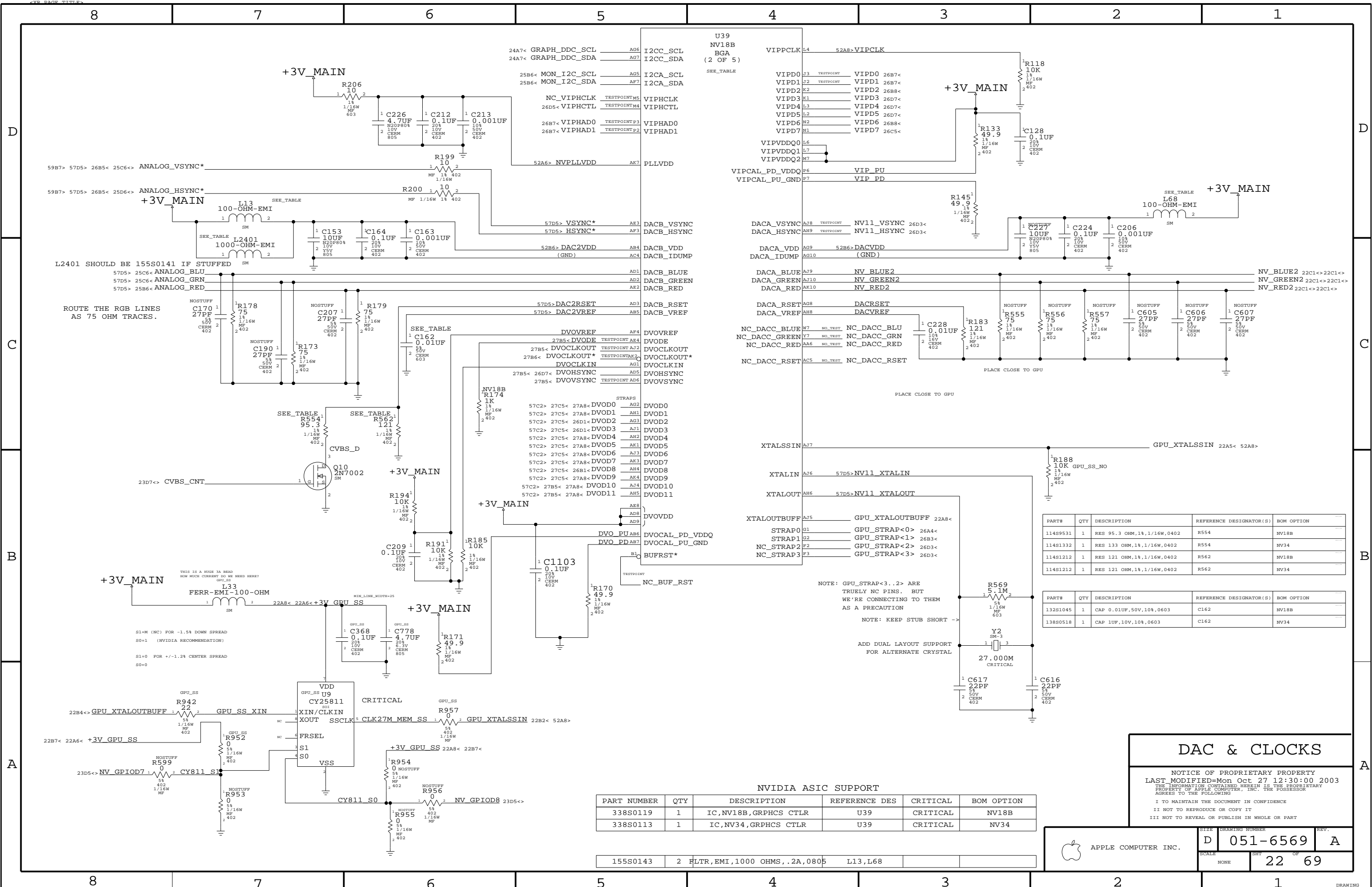
SGRAM2 & SGRAM3

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NONE	21	69



NVIDIA ASIC SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0119	1	IC, NV18B, GRPHCS CTLR	U39	CRITICAL	NV18B
338S0113	1	IC, NV34, GRPHCS CTLR	U39	CRITICAL	NV34

155S0143	2	FLTR, EMI, 1000 OHMS, .2A, 0805	L13, L68		
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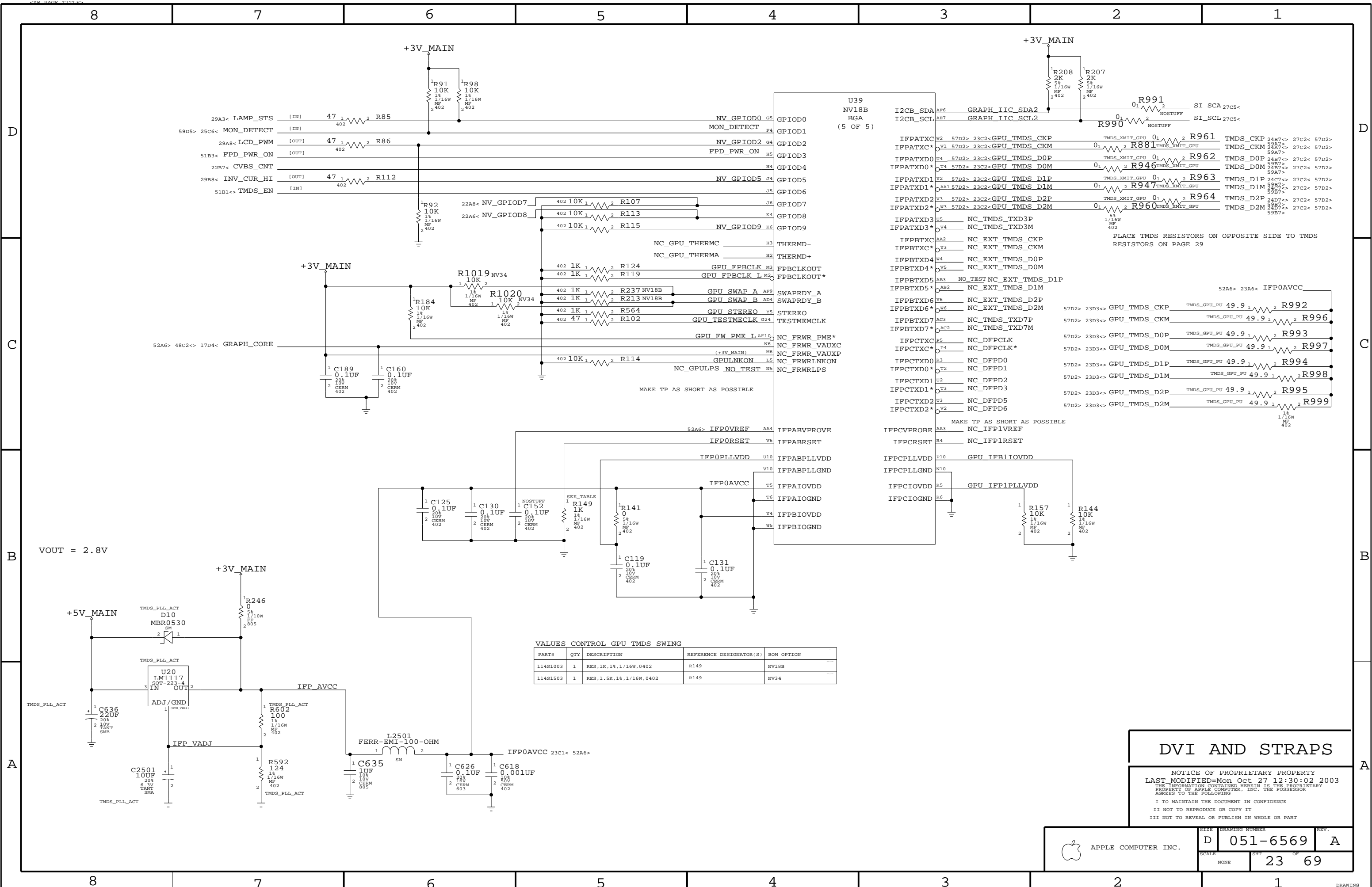
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11489531	1	RES 95.3 OHM, 1%, 1/16W, 0402	R554	NV18B
11481332	1	RES 133 OHM, 1%, 1/16W, 0402	R554	NV34
11481212	1	RES 121 OHM, 1%, 1/16W, 0402	R562	NV18B
11481212	1	RES 121 OHM, 1%, 1/16W, 0402	R562	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13281045	1	CAP 0.01UF, 50V, 10%, 0603	C162	NV18B
13880518	1	CAP 1UF, 10V, 10%, 0603	C162	NV34

DAC & CLOCKS

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VALUES CONTROL GPU TMS SWING

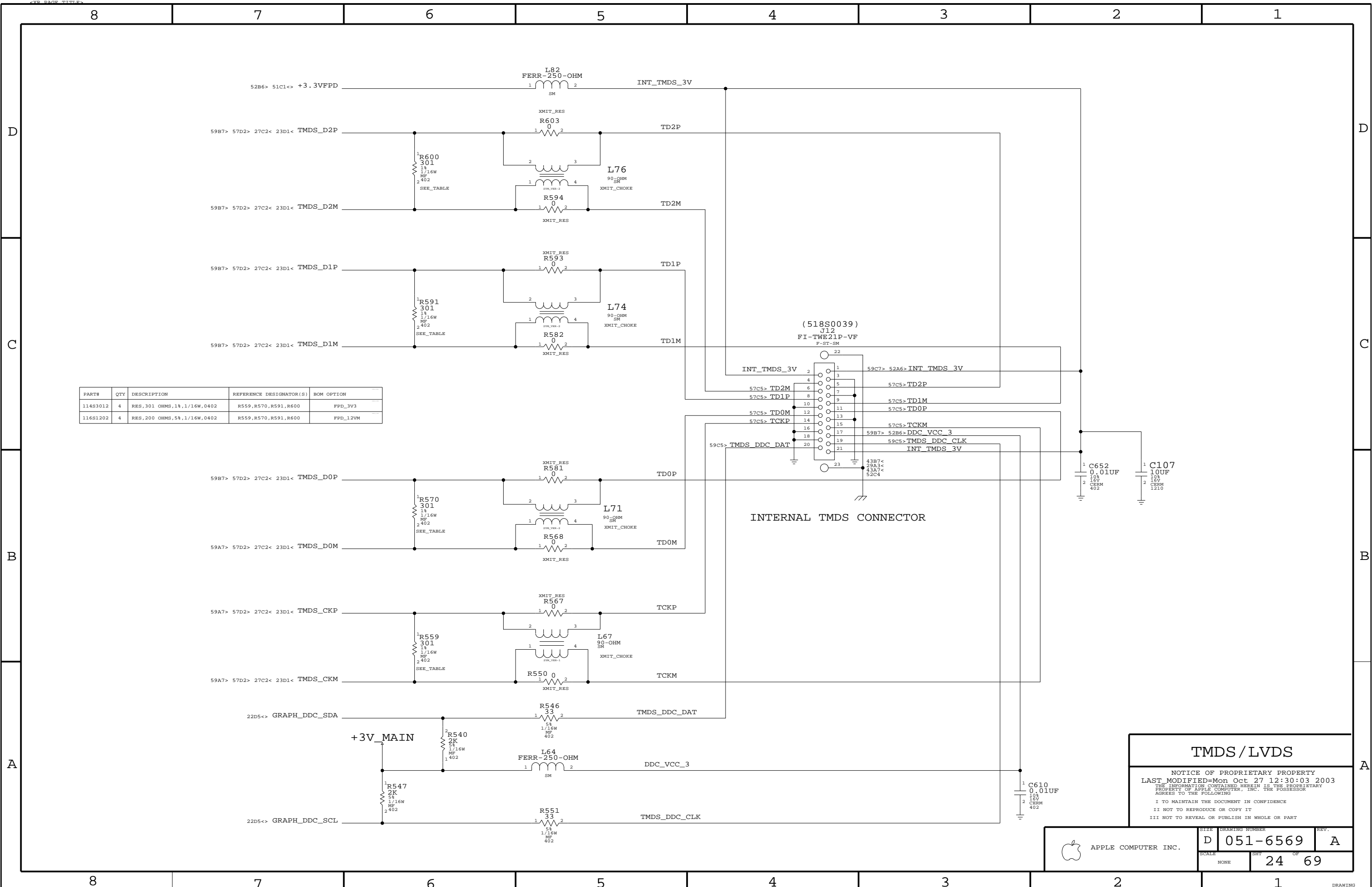
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481003	1	RES,1K,1%,1/16W,0402	R149	NV18B
11481503	1	RES,1.5K,1%,1/16W,0402	R149	NV34

DVI AND STRAPS

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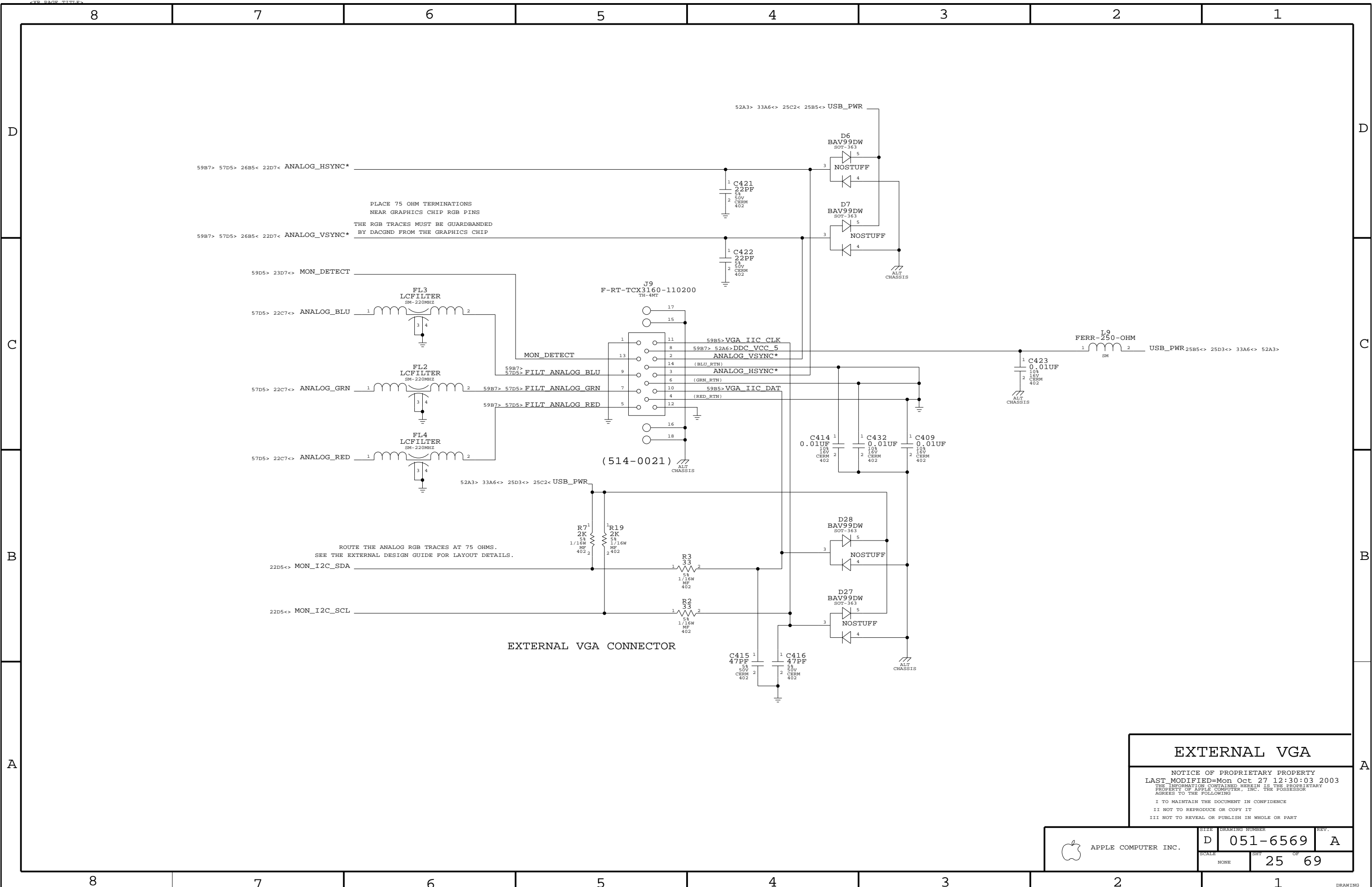


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483012	4	RES, 301 OHMS, 1%, 1/16W, 0402	R559, R570, R591, R600	FPD_3V3
11681202	4	RES, 200 OHMS, 5%, 1/16W, 0402	R559, R570, R591, R600	FPD_12VM

TMDS/LVDS

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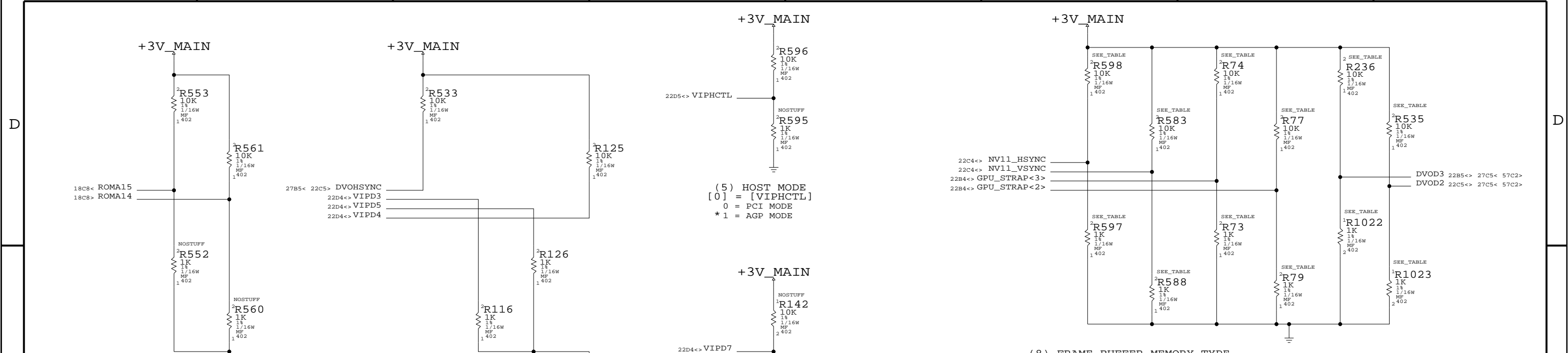


EXTERNAL VGA

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NONE		25 OF 69	



(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
 [1..0] = [ROMA15,ROMA14]
 00 = PARALLEL
 01 = SERIAL AT25F
 10 = SERIAL SST45VF
 * 11 = SERIAL FUTURE

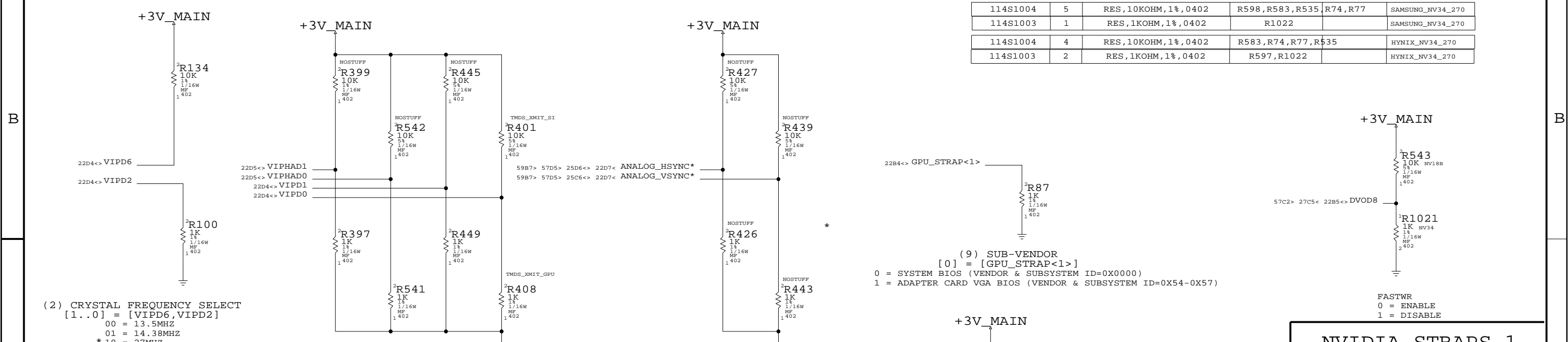
(3) PCI DEVICE ID
 [3..0] = [DVOHSYNC, VIPD3, VIPD5, VIPD4]
 0010 = 0X112 GEFORCE2 GO
 0011 = 0X113 QUADRO2 GO
 0100 = 0X114 NV17M
 0000 = 0X110 GEFORCE2GO MX (NV11B)
 * 1001 = NV18B, NV31, NV34

(6) AGP SIDEBAND
 [0] = [VIPD7]
 * 0 = ENABLE AGP SIDEBAND
 1 = DISABLE AGP SIDEBAND

(8) FRAME BUFFER MEMORY TYPE
 [3..0] = [NV11_HSYNC, NV11_VSYNC, GPU_STRAP<3>, GPU_STRAP<2>]
 1111 = 222MHZ
 1101 = 275MHZ SAMSUNG
 1100 = 275MHZ HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S1004	5	RES,10KOHM,1%,0402	R598,R583,R77,R236,R535		SAMSUNG_NV18B_270
114S1003	1	RES,1KOHM,1%,0402	R73		SAMSUNG_NV18B_270
114S1004	4	RES,10KOHM,1%,0402	R598,R583,R236,R535		HYNIX_NV18B_270
114S1003	2	RES,1KOHM,1%,0402	R73,R79		HYNIX_NV18B_270

114S1004	5	RES,10KOHM,1%,0402	R598,R583,R535	R74,R77	SAMSUNG_NV34_270
114S1003	1	RES,1KOHM,1%,0402	R1022		SAMSUNG_NV34_270
114S1004	4	RES,10KOHM,1%,0402	R583,R74,R77,R535		HYNIX_NV34_270
114S1003	2	RES,1KOHM,1%,0402	R597,R1022		HYNIX_NV34_270



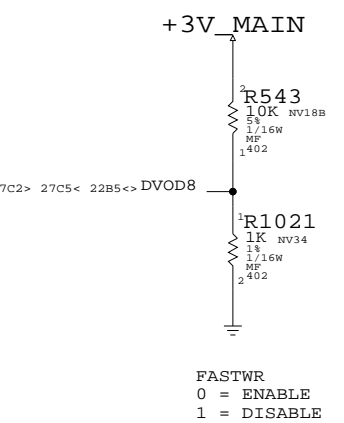
(2) CRYSTAL FREQUENCY SELECT
 [1..0] = [VIPD6, VIPD2]
 00 = 13.5MHZ
 01 = 14.38MHZ
 * 10 = 27MHZ
 11 = {UNDEFINED}

(4) USER DEFINED STRAPS
 [3..0] = [VIPHAD1, VIPHAD0, VIPD1, VIPD0]
 THESE BITS ARE UNDEFINED BUT THEY
 MUST BE KEPT LOW DURING RESET

(7) TV MODE
 [1..0] = [ANALOG_HSYNC*, ANALOG_VSYNC*]
 00 = SECAM
 01 = NTSC
 10 = PAL
 * 11 = DISABLED
 (THESE RESISTORS ARE ALL NOSTUFF)

(9) SUB-VENDOR
 [0] = [GPU_STRAP<1>]
 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
 1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)

(10) PCI ADDRESS BUS
 [0] = [GPU_STRAP<0>]
 0 = REVERSED
 * 1 = NORMAL



NVIDIA STRAPS 1

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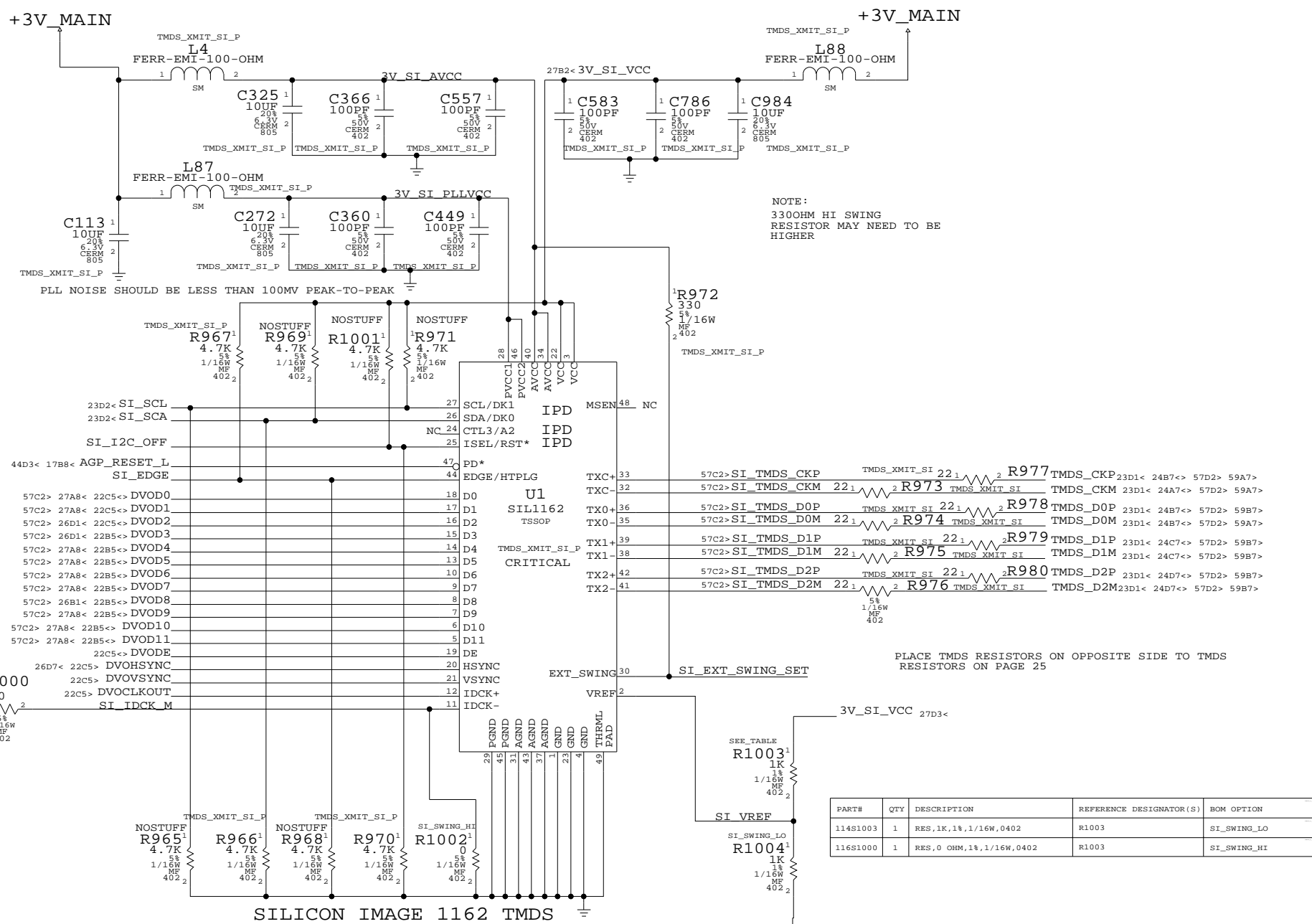
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D

C

B

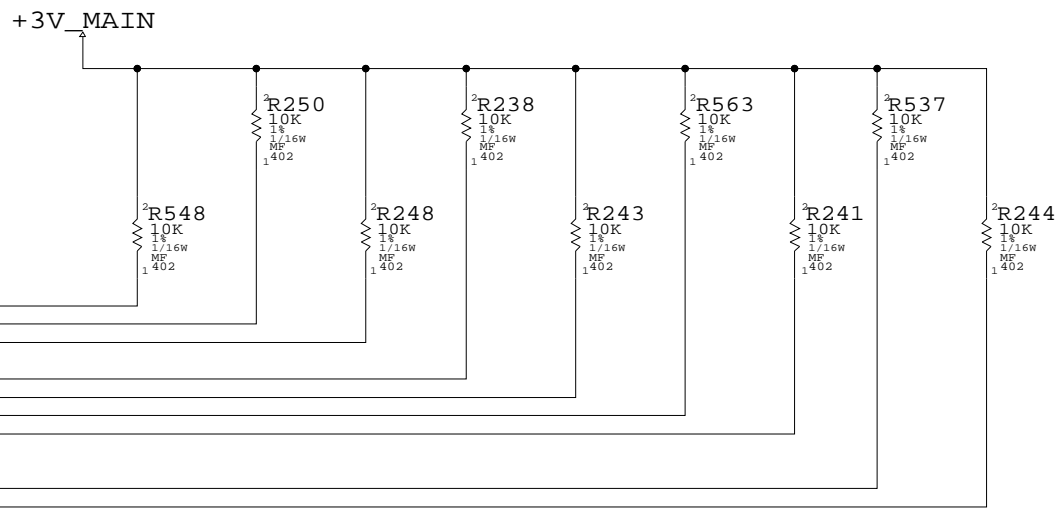
A



NOTE:
330OHM HI SWING
RESISTOR MAY NEED TO BE
HIGHER

PLACE TMD5 RESISTORS ON OPPOSITE SIDE TO TMD5
RESISTORS ON PAGE 25

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481003	1	RES,1K,1%,1/16W,0402	R1003	SI_SWING_LO
11681000	1	RES,0 OHM,1%,1/16W,0402	R1003	SI_SWING_HI

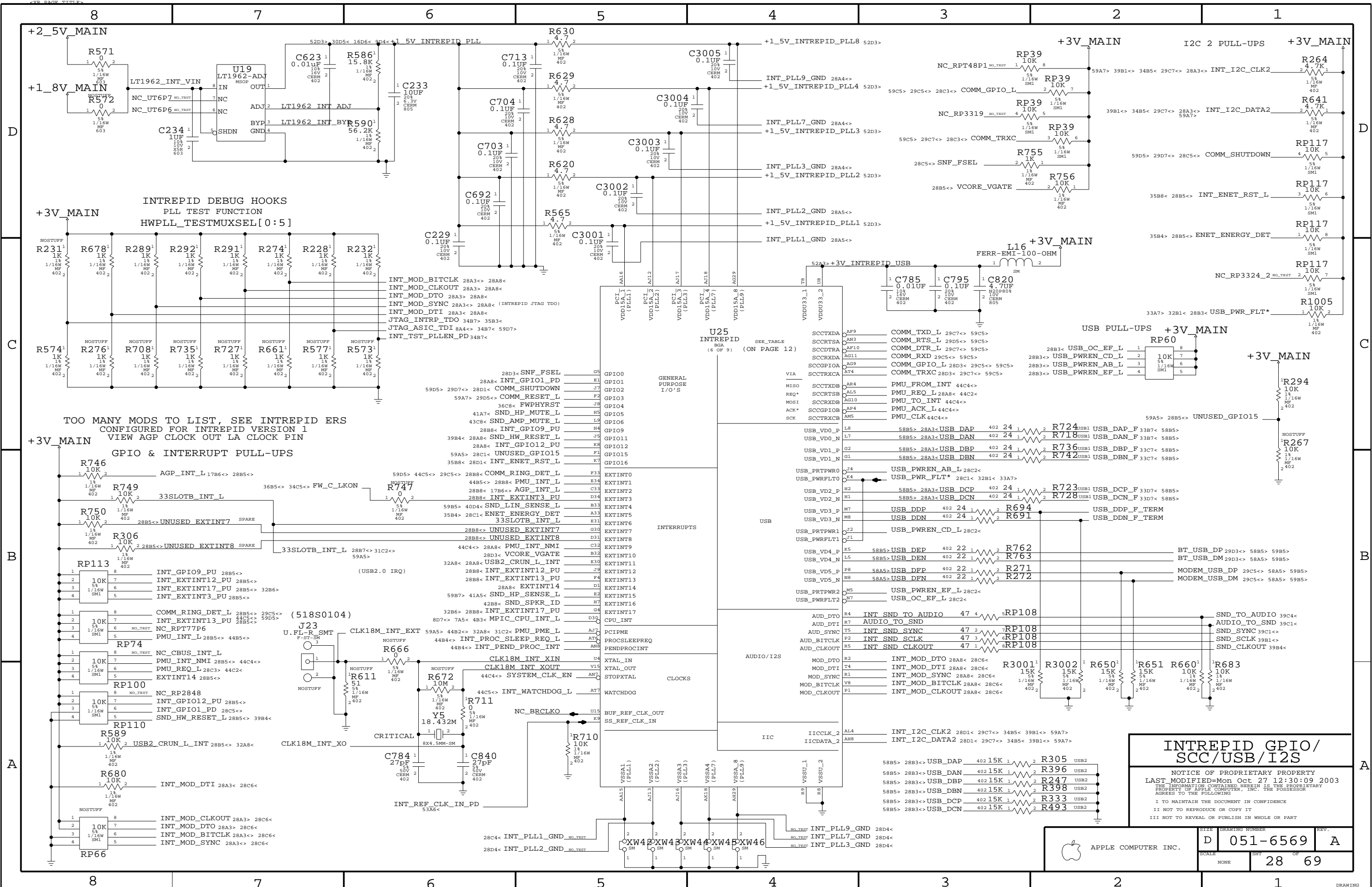


UNDEFINED RESET CONFIGURATION STRAPS

NVIDIA STRAPS 2

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SCALE	NONE	SHT	27 OF 69



INTREPID DEBUG HOOKS
PLL TEST FUNCTION
HWPLL_TESTMUXSEL[0:5]

TOO MANY MODS TO LIST, SEE INTREPID ERS
CONFIGURED FOR INTREPID VERSION 1
VIEW AGP CLOCK OUT LA CLOCK PIN

GPIO & INTERRUPT PULL-UPS

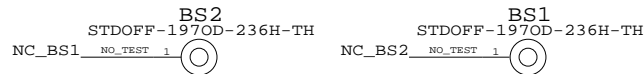
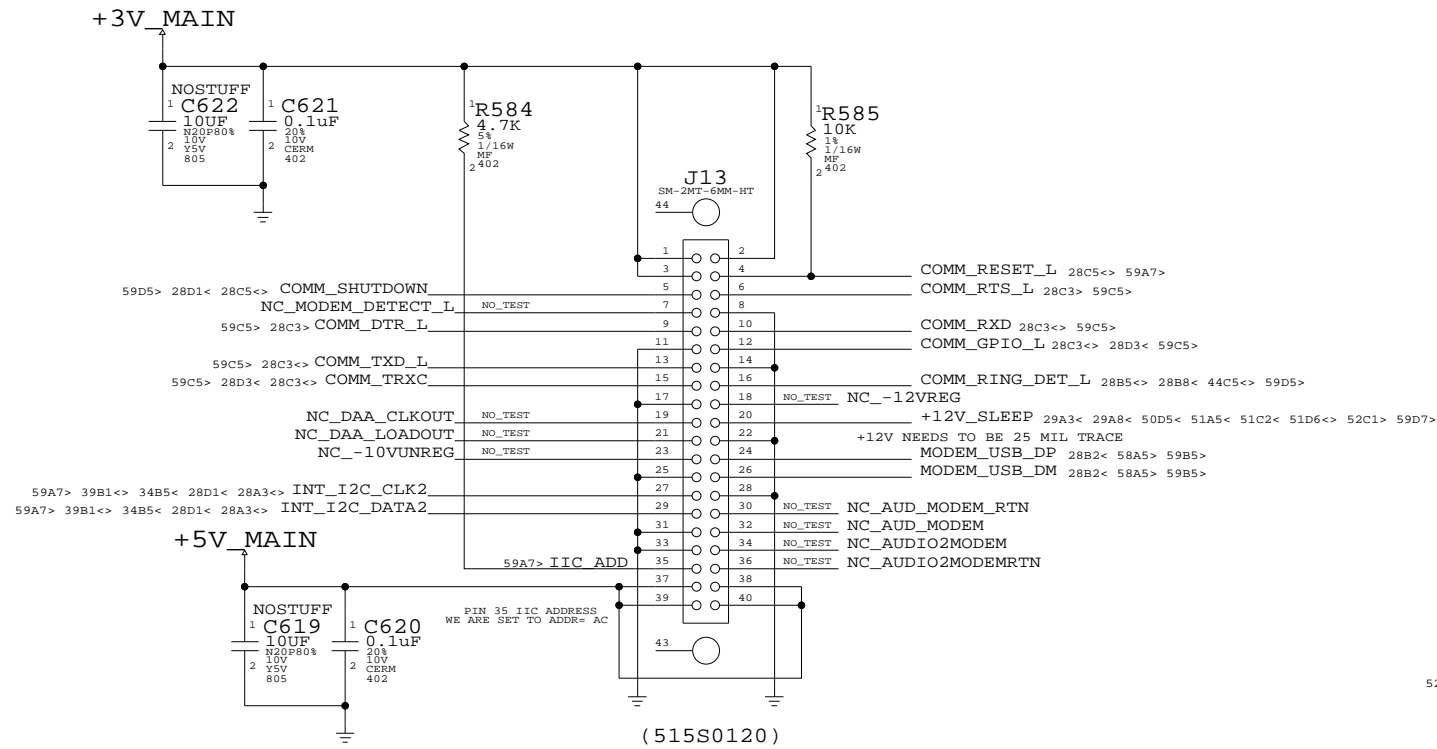
INTREPID GPIO/ SCC/USB/I2S

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NONE	28	69

MODEM BOARD CONNECTOR

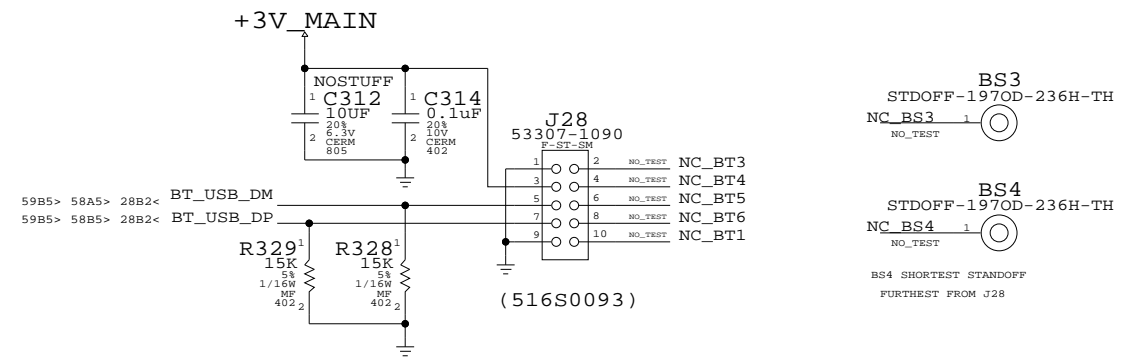
(DASH II)



MODEM STANDOFF SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1034	2	STDOFF-19709-236H-TH	BS1, BS2		

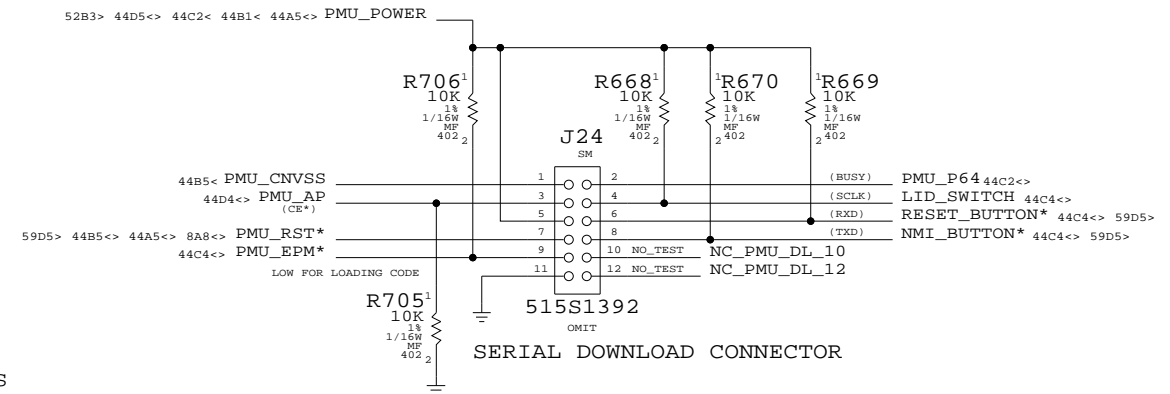
BLUETOOTH CONNECTOR



BLUETOOTH CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-0170	1	STDOFF, BLUETOOTH, SHORT	BS4		
860-0171	1	STDOFF, BLUETOOTH, LONG	BS3		

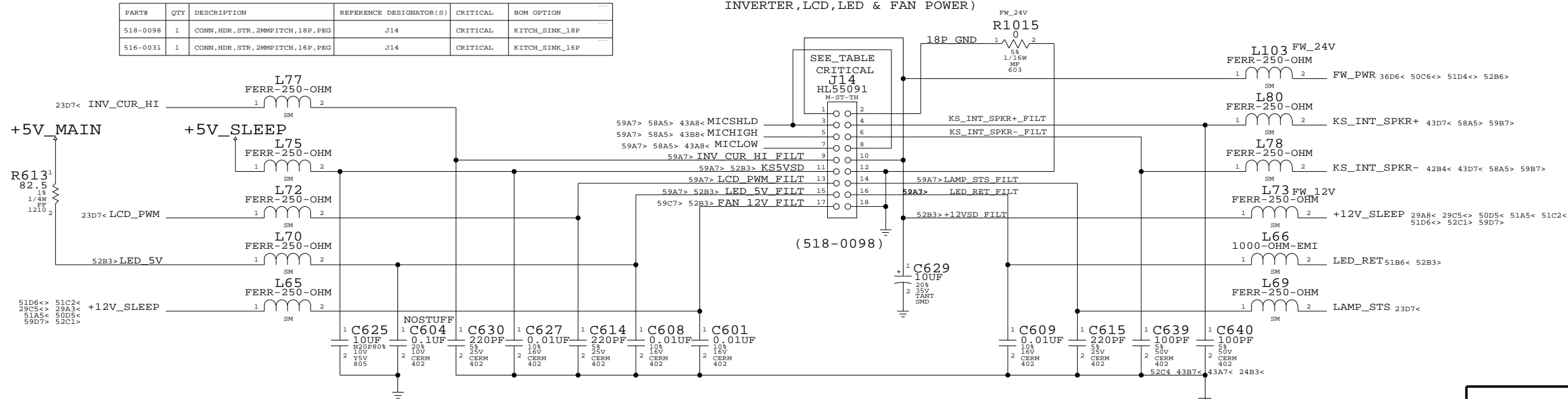
SERIAL DOWNLOAD INTERFACE



SERIAL DOWNLOAD CONNECTOR

'KITCHEN SINK' CONNECTOR
(MICROPHONE, INTERNAL SPEAKER CONNECTIONS
INVERTER, LCD, LED & FAN POWER)

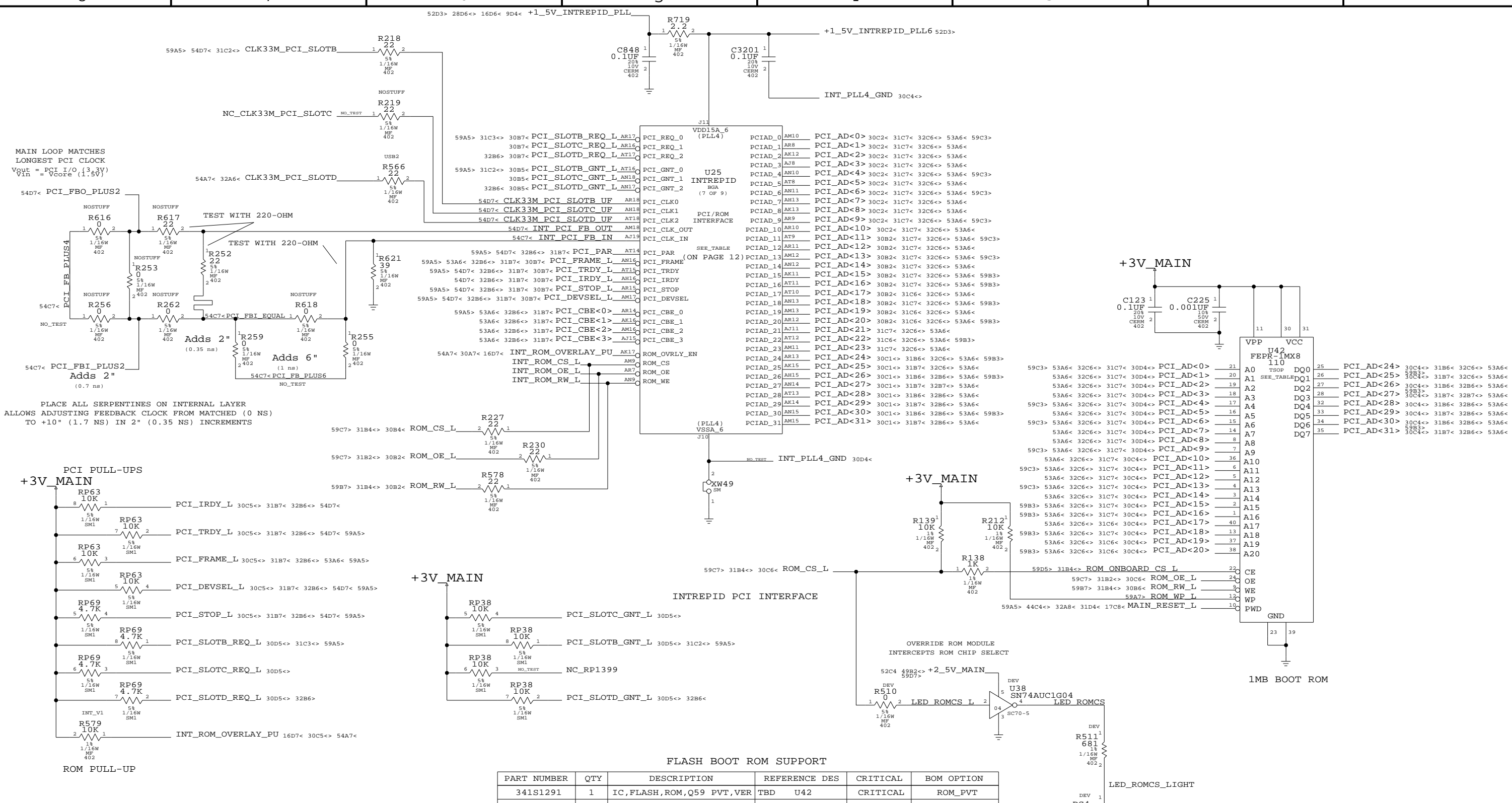
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0098	1	CONN, HDR, STR, 2MMPITCH, 18P, PEG	J14	CRITICAL	KITCH_SINK_18P
516-0031	1	CONN, HDR, STR, 2MMPITCH, 16P, PEG	J14	CRITICAL	KITCH_SINK_16P



MODEM, BLUETOOTH,
KITCHEN SINK
& SERIAL DOWNLOAD

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NONE	29	69	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1291	1	IC, FLASH, ROM, Q59 PVT, VER	TBD U42	CRITICAL	ROM_PVT
341S1289	1	IC, FLASH, ROM, Q59 EVT, VER	TBD U42	CRITICAL	ROM_EVT
341S1290	1	IC, FLASH, ROM, Q59 DVT, 4.7	4B0 U42	CRITICAL	ROM_DVT
341T1292	1	IC, FLASH, ROM, Q59 PROD, VER	TBD U42	CRITICAL	ROM_PROD_T
341S1280	1	IC, FLASH, ROM, Q59 DEV, VER	TBD U42	CRITICAL	ROM_DEV
009-6525	1	IC, FEPR, FLASH ROM, DEV	U42		OMIT
335S0350	1	IC, FLASH ROM, 1MB, BLANK	U42		OMIT
341S1372	1	IC, FLASH, ROM, Q59 PROD, VER	TBD U42	CRITICAL	ROM_PROD
009-6588	1	IC, FEPR, FLASH ROM, PROD	U42		OMIT
335S0350	1	IC, FLASH ROM, 1MB, BLANK	U42		OMIT

RFA STRUCTURE AT PVT REPORTING TO 341T1292

RFA STRUCTURE ONCE ROM IS FINAL REPORTING TO 341T1292

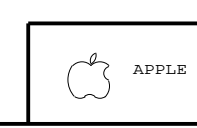
INTREPID PCI & BOOT ROM

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D	051-6569	A
SCALE	SHT	OF
NONE	30	69

DRAWING



D

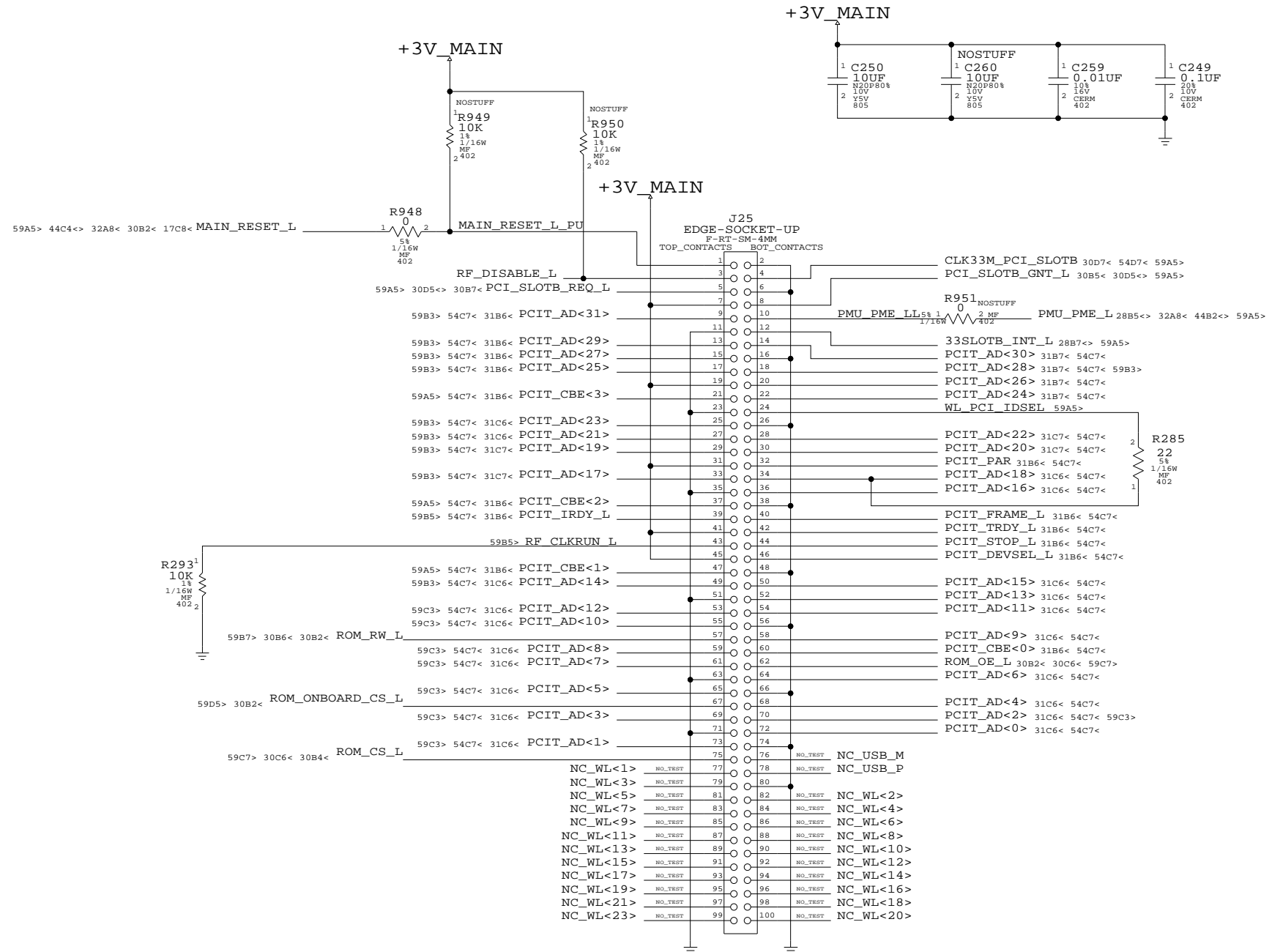
C

B

A

PLACE RP'S NEAR WIRELESS CONNECTOR

59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<0>	1	RP77	8	PCIT_AD<0>	31B2<>	54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<1>	2	RP73	7	NO_TEST	PCIT_AD<1>	31B3<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<2>	3	RP73	6	NO_TEST	PCIT_AD<2>	31B2<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<3>	4	RP73	5	NO_TEST	PCIT_AD<3>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<4>	1	RP75	8	PCIT_AD<4>	31B2<>	54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<5>	2	RP75	7	NO_TEST	PCIT_AD<5>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<6>	3	RP75	6	NO_TEST	PCIT_AD<6>	31B2<> 54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<7>	4	RP75	5	NO_TEST	PCIT_AD<7>	31B3<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<8>	1	RP73	8	PCIT_AD<8>	31B3<>	54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<9>	2	RP73	7	NO_TEST	PCIT_AD<9>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30C2< PCI_AD<10>	3	RP73	6	NO_TEST	PCIT_AD<10>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<11>	4	RP73	5	NO_TEST	PCIT_AD<11>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30B2< PCI_AD<12>	1	RP72	8	PCIT_AD<12>	31B3<>	54C7< 59C3>
59C3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<13>	2	RP72	7	NO_TEST	PCIT_AD<13>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30B2< PCI_AD<14>	3	RP72	6	NO_TEST	PCIT_AD<14>	31C3<> 54C7< 59B3>
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<15>	4	RP72	5	NO_TEST	PCIT_AD<15>	31C2<> 54C7<
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<16>	1	RP59	8	PCIT_AD<16>	31C2<>	54C7<
59B3> 54C7< 31C3<> PCIT_AD<17>	2	RP59	7	NO_TEST	PCIT_AD<17>	30B2< 30C4<> 32C6<> 53A6<
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<18>	3	RP59	6	NO_TEST	PCIT_AD<18>	31C2<> 54C7<
59B3> 54C7< 31C3<> PCIT_AD<19>	4	RP59	5	NO_TEST	PCIT_AD<19>	30B2< 30C4<> 32C6<> 53A6<
53A6< 32C6<> 30C4<> PCI_AD<23>	1	RP58	8	PCIT_AD<23>	31C3<>	54C7< 59B3>
53A6< 32C6<> 30C4<> PCI_AD<21>	2	RP58	7	NO_TEST	PCIT_AD<21>	31C3<> 54C7< 59B3>
54C7< 31C2<> PCIT_AD<22>	3	RP58	6	NO_TEST	PCIT_AD<22>	30C4<> 32C6<> 53A6< 59B3>
54C7< 31C2<> PCIT_AD<20>	4	RP58	5	NO_TEST	PCIT_AD<20>	30B2< 30C4<> 32C6<> 53A6< 59B3>
53A6< 32B7<> 30C4<> 30C1<> PCI_AD<27>	1	RP56	8	PCIT_AD<27>	31C3<>	54C7< 59B3>
53A6< 32C6<> 30C4<> 30C1<> PCI_AD<25>	2	RP56	7	NO_TEST	PCIT_AD<25>	31C3<> 54C7< 59B3>
54C7< 31C2<> PCIT_AD<26>	3	RP56	6	NO_TEST	PCIT_AD<26>	30C1<> 30C4<> 32B6<> 53A6< 59B3>
54C7< 31C2<> PCIT_AD<24>	4	RP56	5	NO_TEST	PCIT_AD<24>	30C1<> 30C4<> 32C6<> 53A6< 59B3>
59B3> 54C7< 31C2<> PCIT_AD<28>	1	RP54	8	PCIT_AD<28>	30C1<>	30C4<> 32B6<> 53A6<
54C7< 31C2<> PCIT_AD<30>	2	RP54	7	NO_TEST	PCIT_AD<30>	30C1<> 30C4<> 32B6<> 53A6< 59B3>
53A6< 32B6<> 30C4<> 30C1<> PCI_AD<31>	3	RP54	6	NO_TEST	PCIT_AD<31>	31C3<> 54C7< 59B3>
53A6< 32B6<> 30C4<> 30C1<> PCI_AD<29>	4	RP54	5	NO_TEST	PCIT_AD<29>	31C3<> 54C7< 59B3>
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_FRAME_L	1	RP61	8	PCIT_PAR	31C2<>	54C7<
59A5> 53A6< 32B6<> 30C5<> 30B7< PCI_FRAME_L	2	RP61	7	NO_TEST	PCIT_FRAME_L	31C2<> 54C7<
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_TRDY_L	3	RP61	6	NO_TEST	PCIT_TRDY_L	31C2<> 54C7<
54D7< 32B6<> 30C5<> 30B7< PCI_IRDY_L	4	RP61	5	NO_TEST	PCIT_IRDY_L	31C3<> 54C7< 59B5>
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_STOP_L	1	RP67	8	PCIT_STOP_L	31C2<>	54C7<
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_DEVSEL_L	2	RP67	7	NO_TEST	PCIT_DEVSEL_L	31C2<> 54C7<
53A6< 32B6<> 30C5<> PCI_CBE<1>	3	RP67	6	NO_TEST	PCIT_CBE<1>	31C3<> 54C7< 59A5>
59A5> 53A6< 32B6<> 30C5<> PCI_CBE<0>	4	RP67	5	NO_TEST	PCIT_CBE<0>	31B2<> 54C7<
53A6< 32B6<> 30C5<> PCI_CBE<2>	1	RP64	8	PCIT_CBE<2>	31C3<>	54C7< 59A5>
53A6< 32B6<> 30C5<> PCI_CBE<3>	2	RP64	7	NO_TEST	PCIT_CBE<3>	31C3<> 54C7< 59A5>
NC_PCIR0	NO_TEST	3	5	NO_TEST	NC_PCITR0	
NC_PCIR1	NO_TEST	4	5	NO_TEST	NC_PCITR1	



(516S0046)

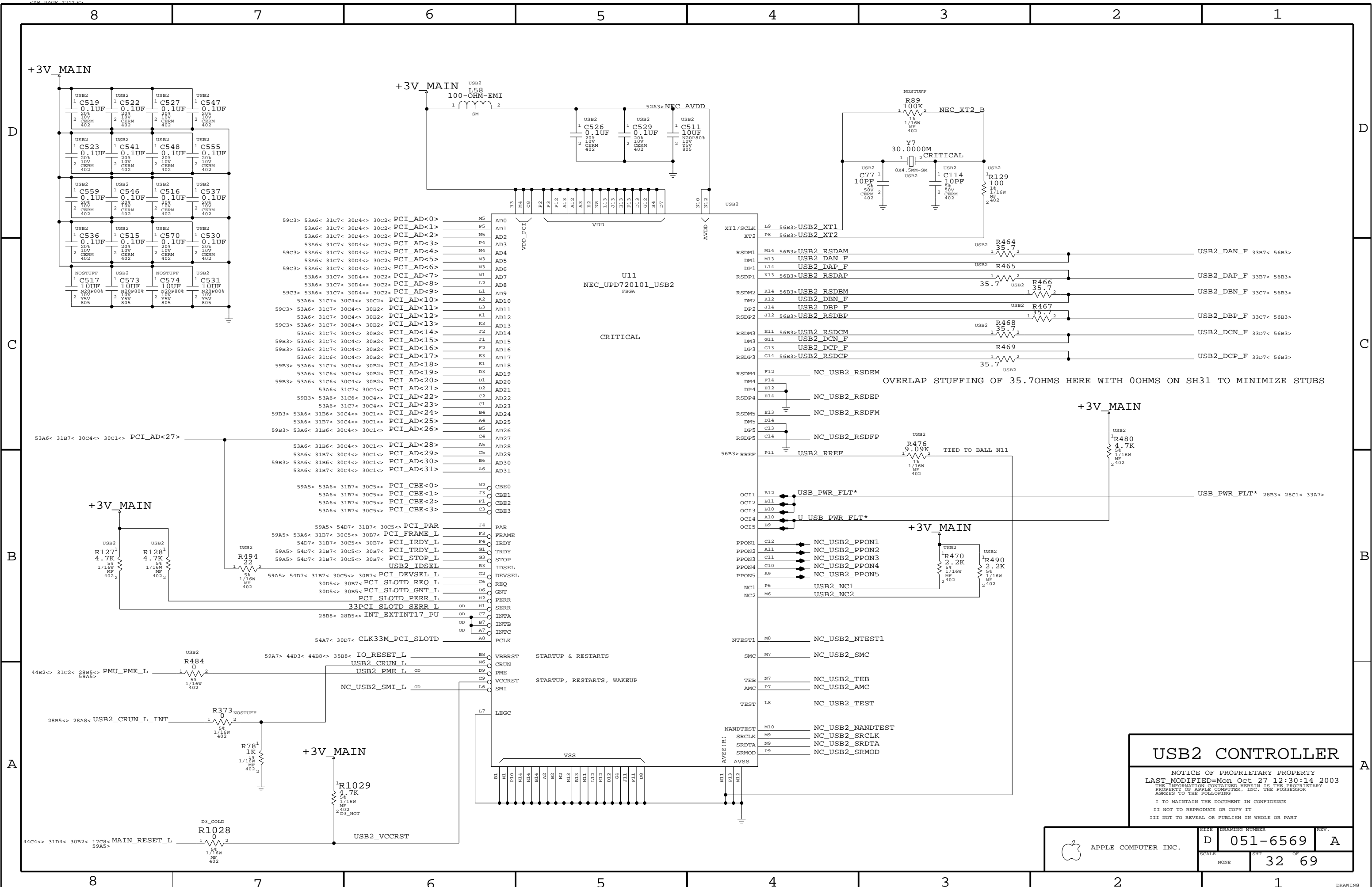
WIRELESS CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
815-7245	1	WIRELESS CARD GUIDE, J25	J251		
452-0411	2	NUT, HEX, M2 X 1.5H, J25	J252, J253		
452-0412	2	SCREW, M2 X 0.4 X 6.0 L, J25	J254, J255		

WIRELESS PCI

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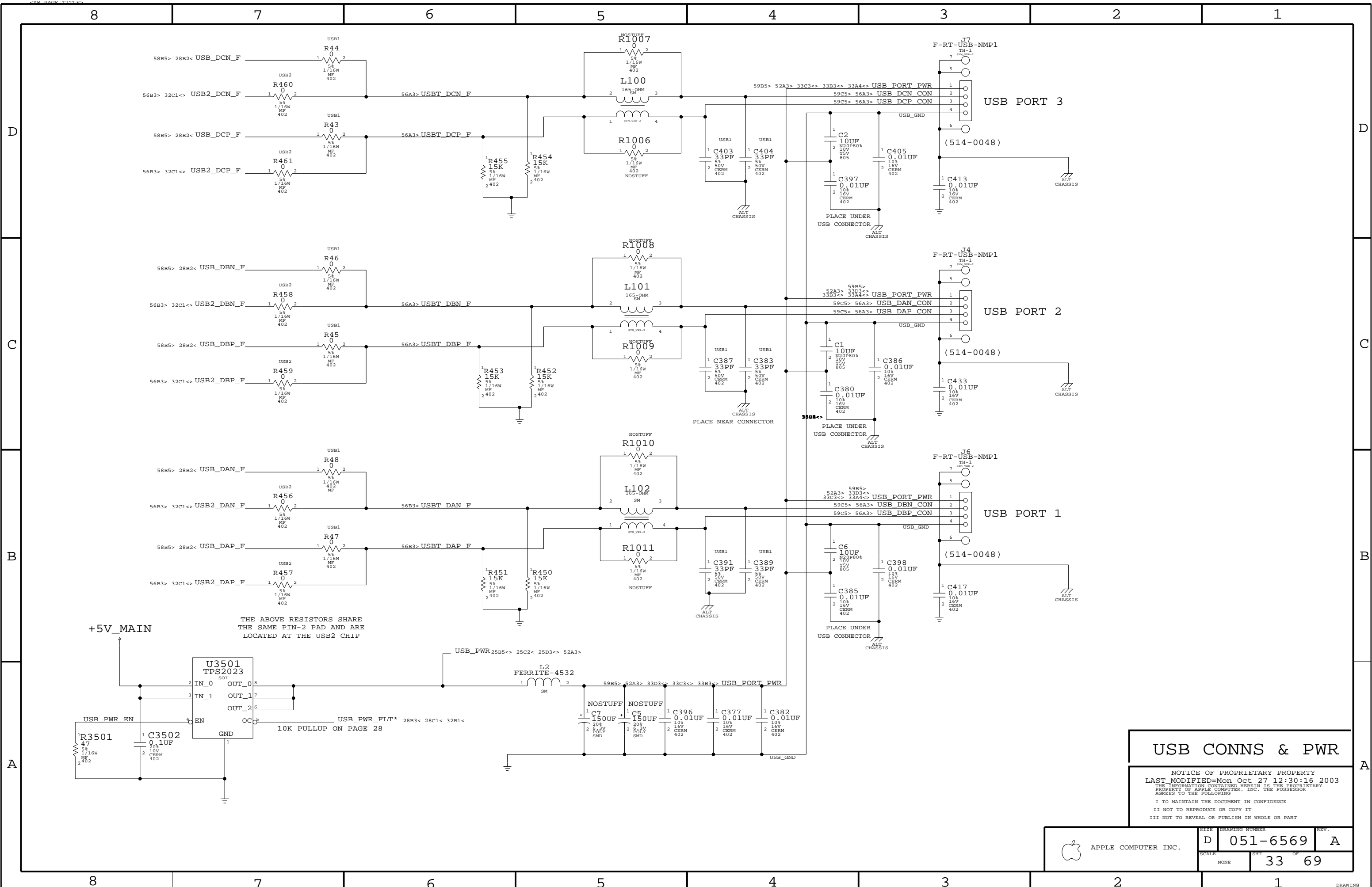
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SCALE	SHT	OF	
NONE	31	69	



USB2 CONTROLLER

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USB CONNS & PWR

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SCALE	SHEET		OF
NONE	33		69

D

C

B

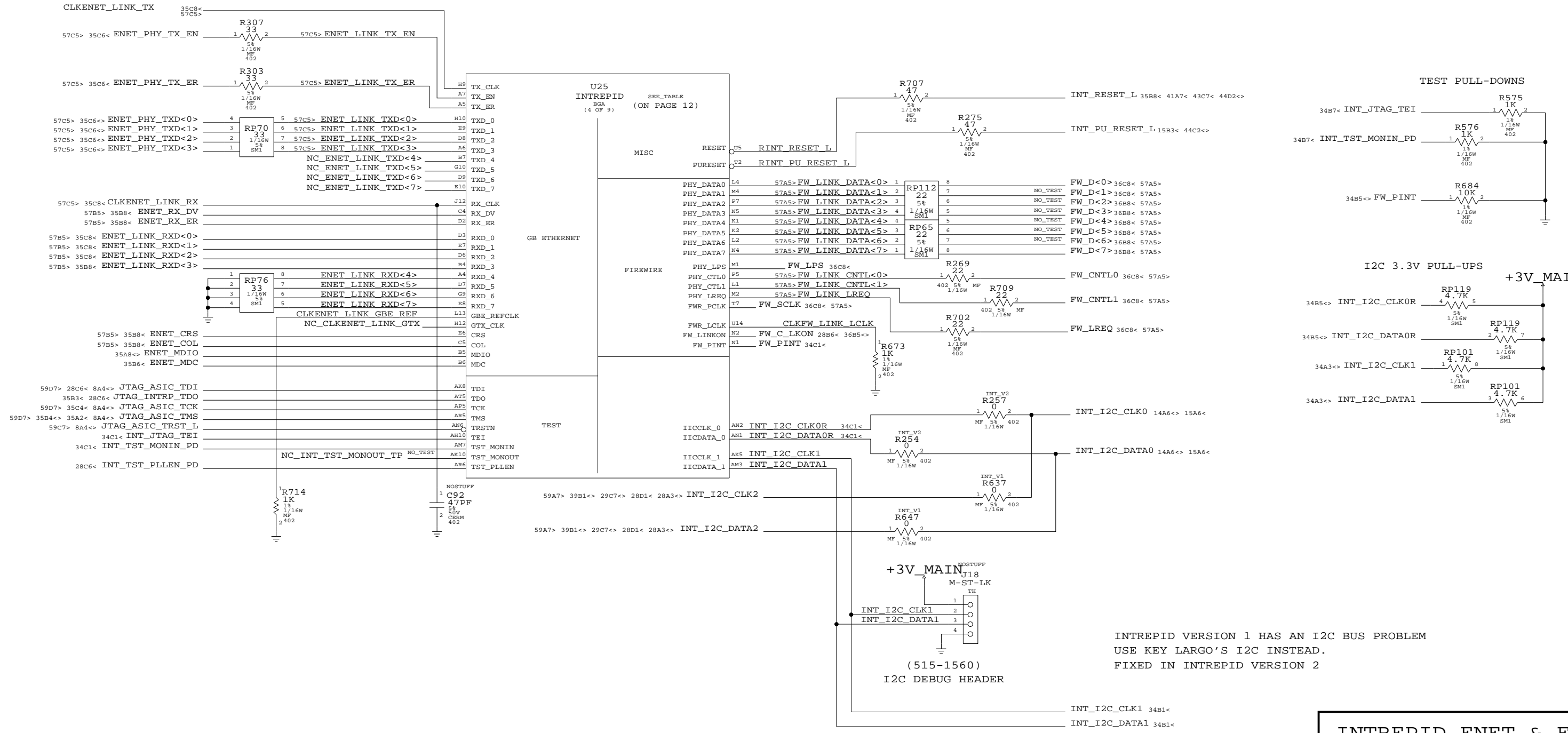
A

D

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B

A

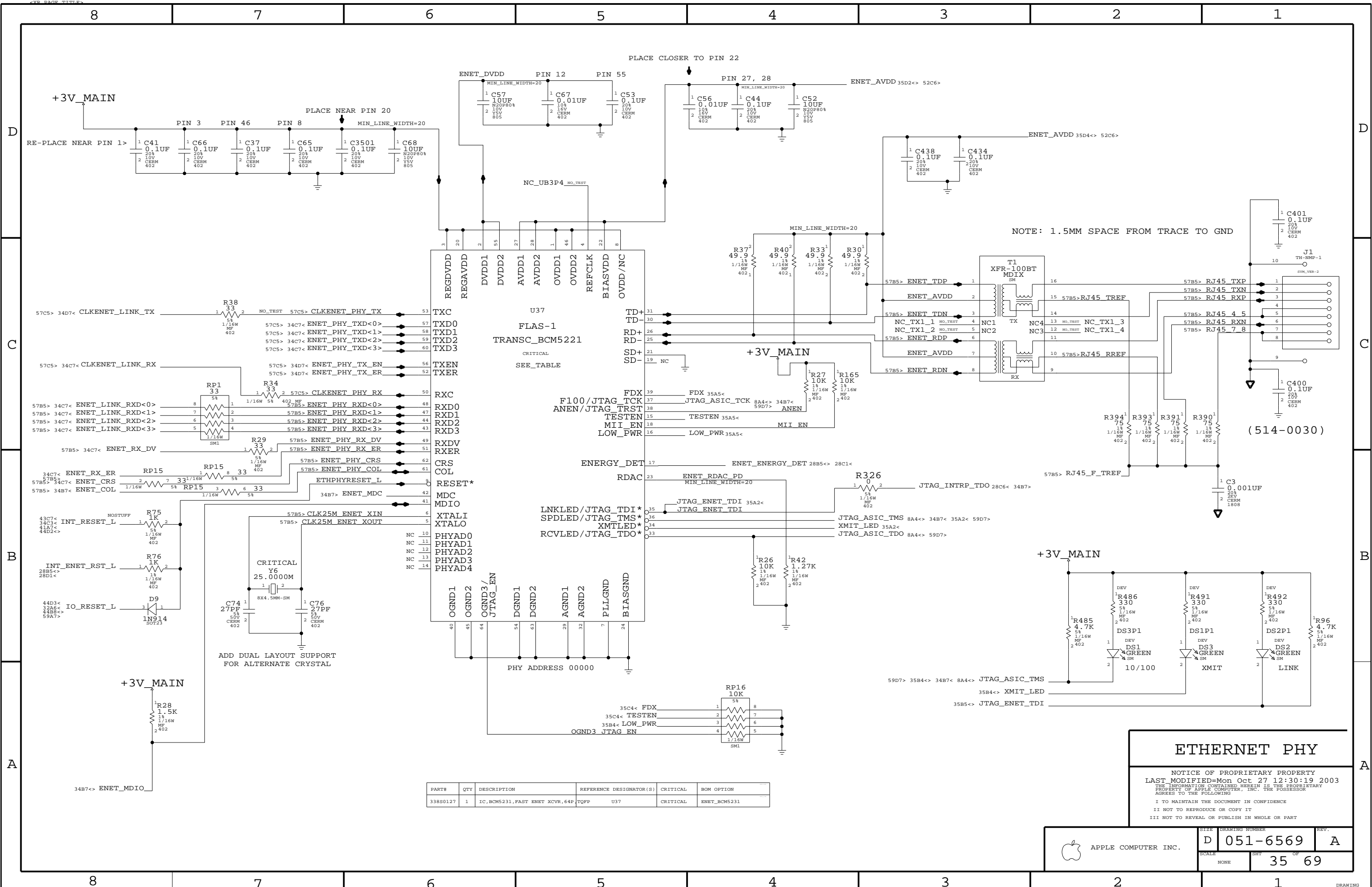


INTREPID ENET & FW

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	D	051-6569	A
SCALE		SHT	OF
NONE		34	69

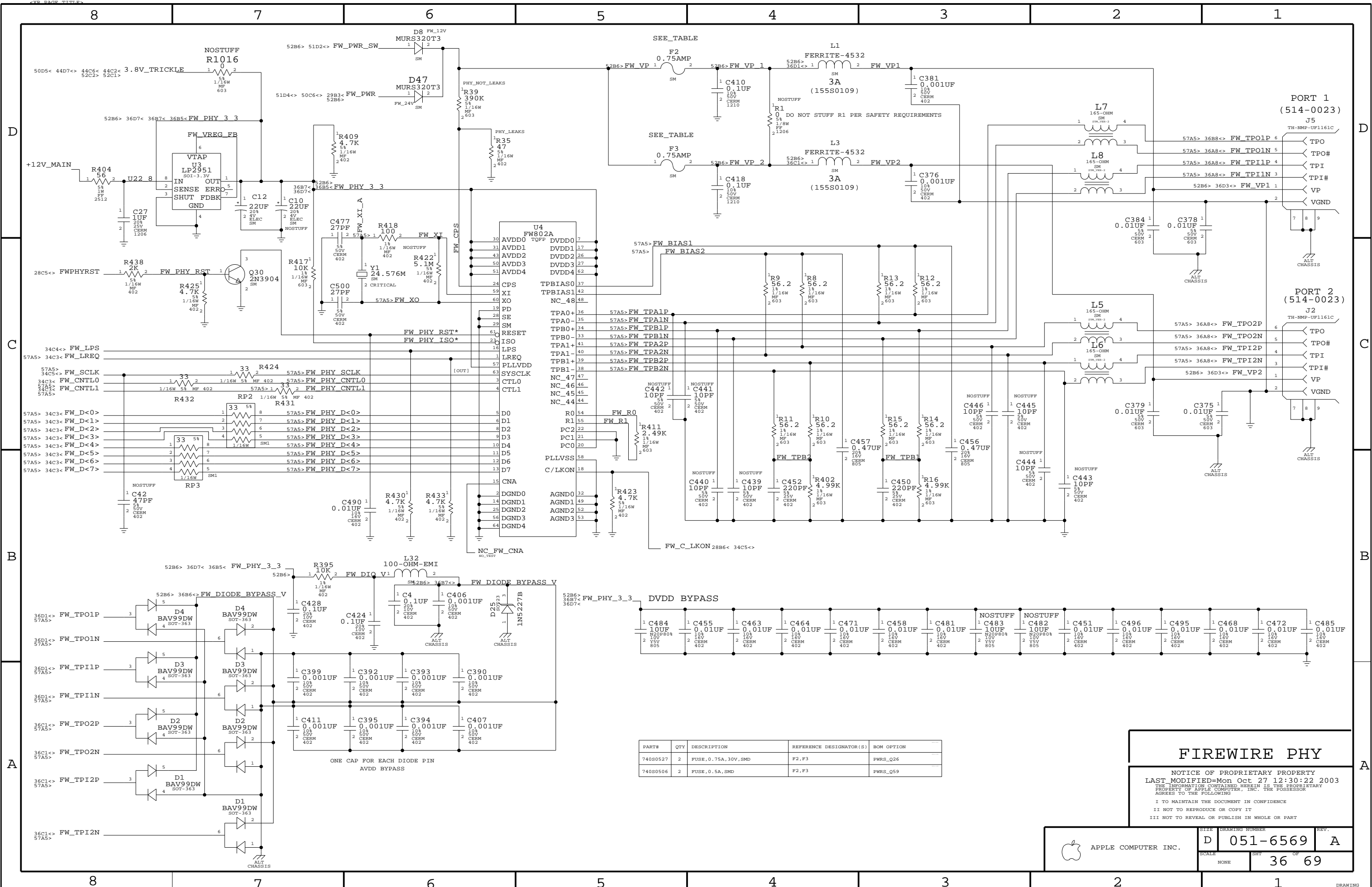


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0127	1	IC, BCM5231, FAST ENET XCVR, 64P, TQFP	U37	CRITICAL	ENET_BCM5231

ETHERNET PHY

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	NONE	D 051-6569	A
SCALE	SHT	OF	
		35	69



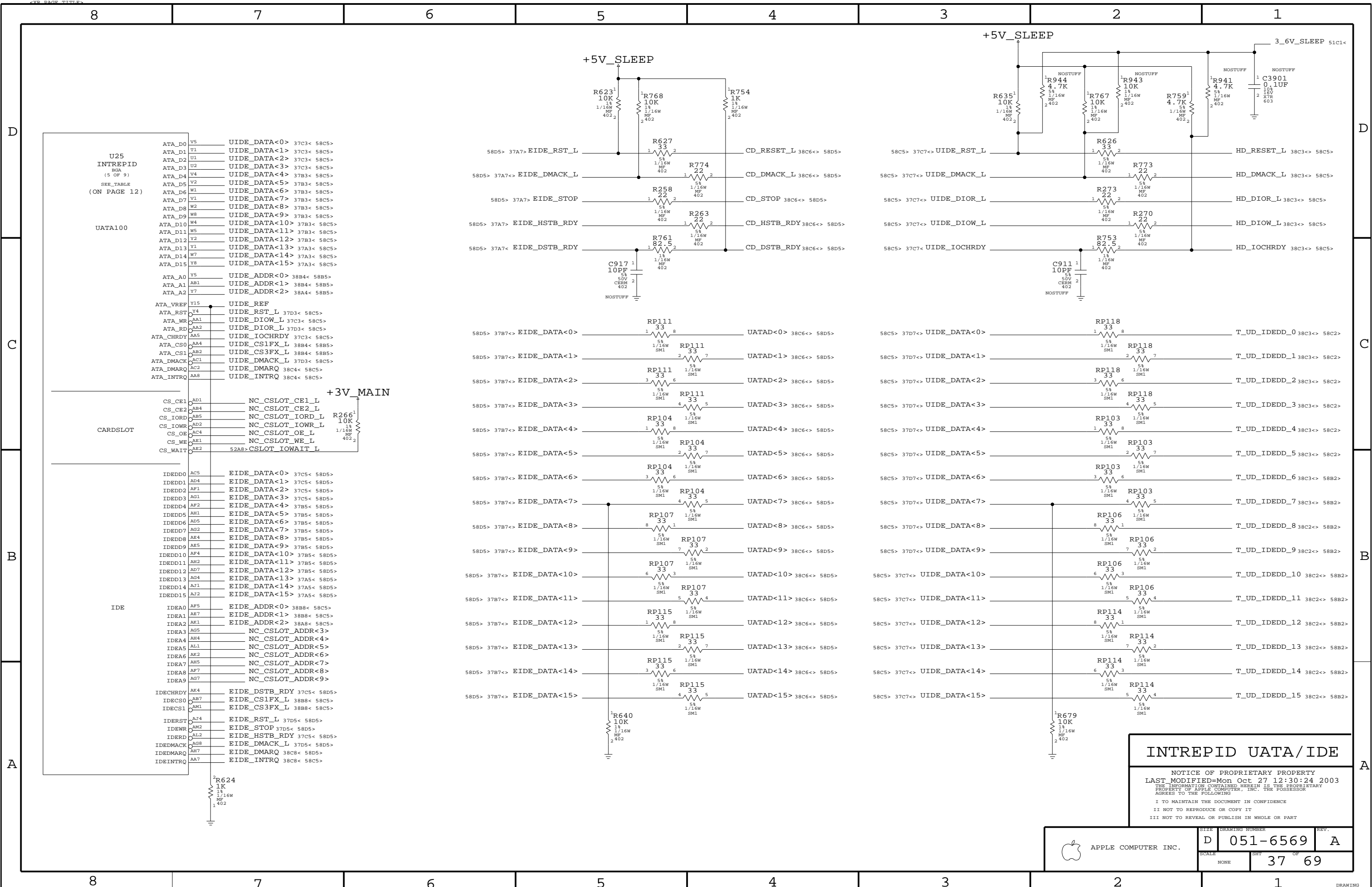
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
740S0527	2	FUSE, 0.75A, 30V, SMD	F2, F3	PWRS_Q26
740S0506	2	FUSE, 0.5A, SMD	F2, F3	PWRS_Q59

FIREWIRE PHY

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	SCALE: NONE	SHEET: 36	OF: 69



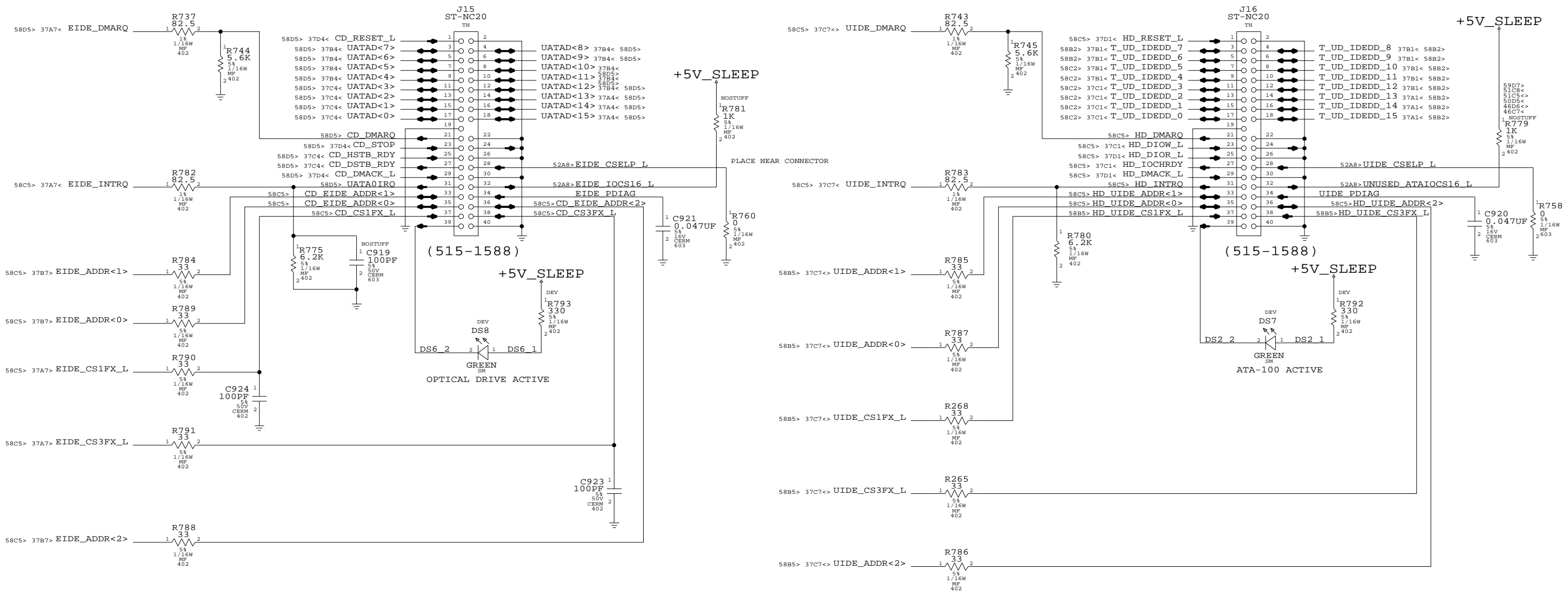
INTREPID UATA/IDE

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	D	051-6569	A
SCALE	SHT	OF	
NONE	37	69	

OPTICAL DRIVE INTERFACE

ATA-100 INTERFACE

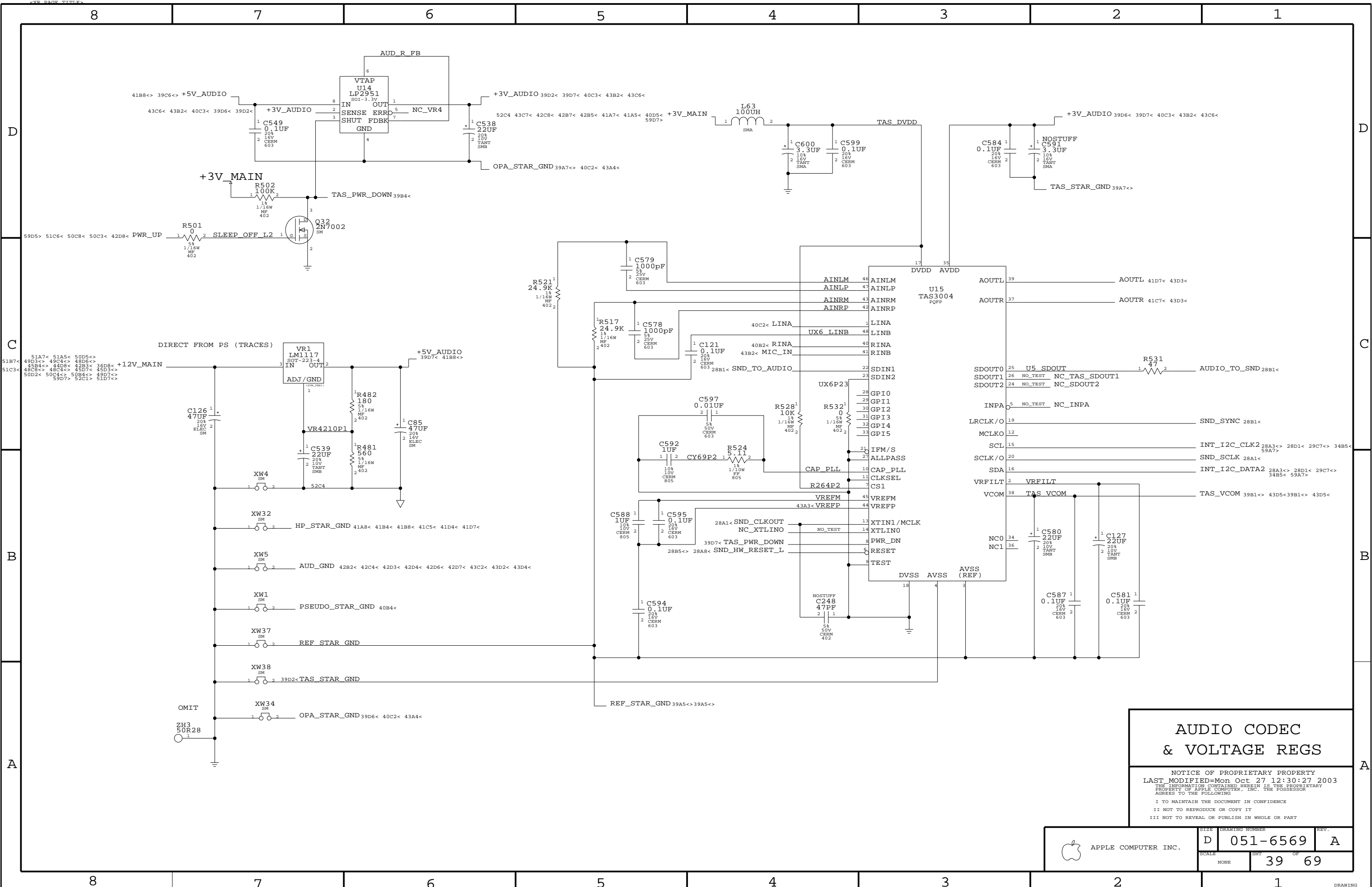


CD/HD CONS

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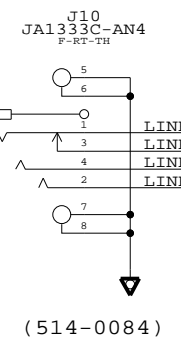
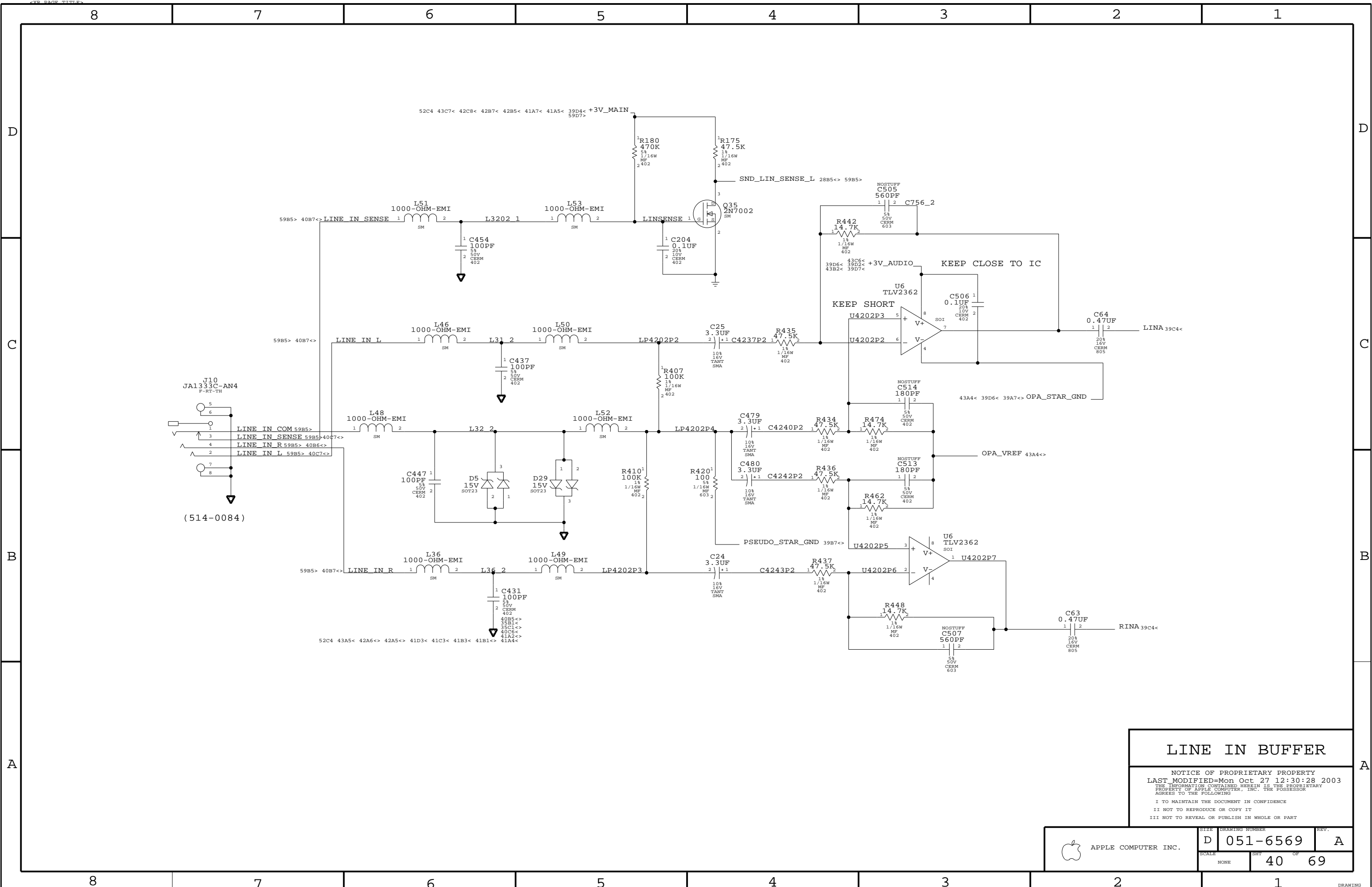
APPLE COMPUTER INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-6569	REV.: A
	SHEETS: 38 OF 69		



AUDIO CODEC & VOLTAGE REGS

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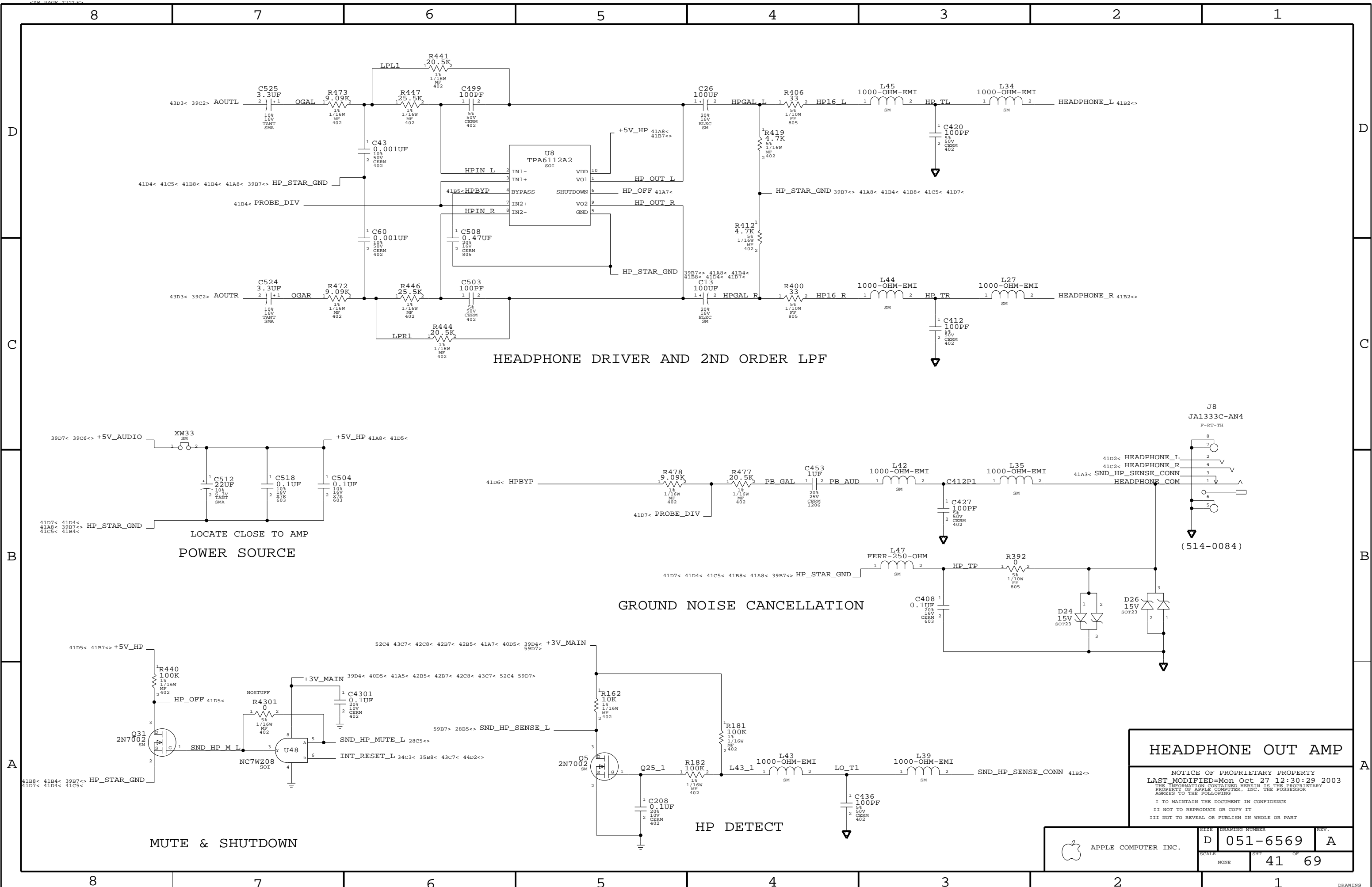
APPLE COMPUTER INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-6569	REV.: A
	SHEET: 39 OF 69		



LINE IN BUFFER

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	DRAWING NUMBER	REV.
	D 051-6569	A
SCALE	SHT	OF
NONE	40	69



HEADPHONE DRIVER AND 2ND ORDER LPF

LOCATE CLOSE TO AMP
POWER SOURCE

GROUND NOISE CANCELLATION

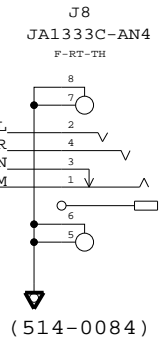
MUTE & SHUTDOWN

HP DETECT

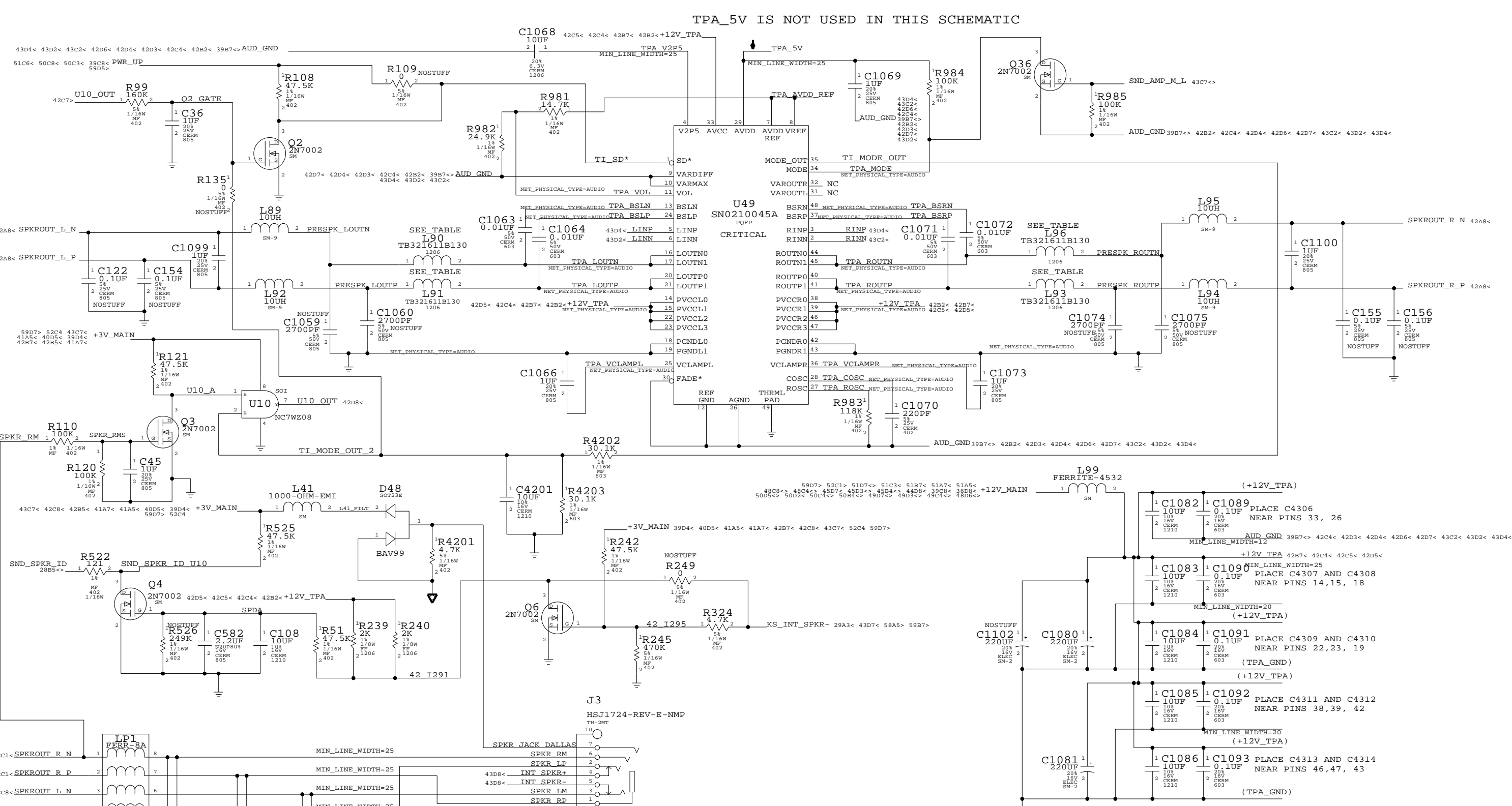
HEADPHONE OUT AMP

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	NONE	051-6569	A
SCALE		SHT	OF
		41	69



(514-0084)



C1061 AND C4261 SHARE PAD 1
 C1062 AND C4262 SHARE PAD 1
 C1065 AND C4265 SHARE PAD 1
 C1067 AND C4267 SHARE PAD 1

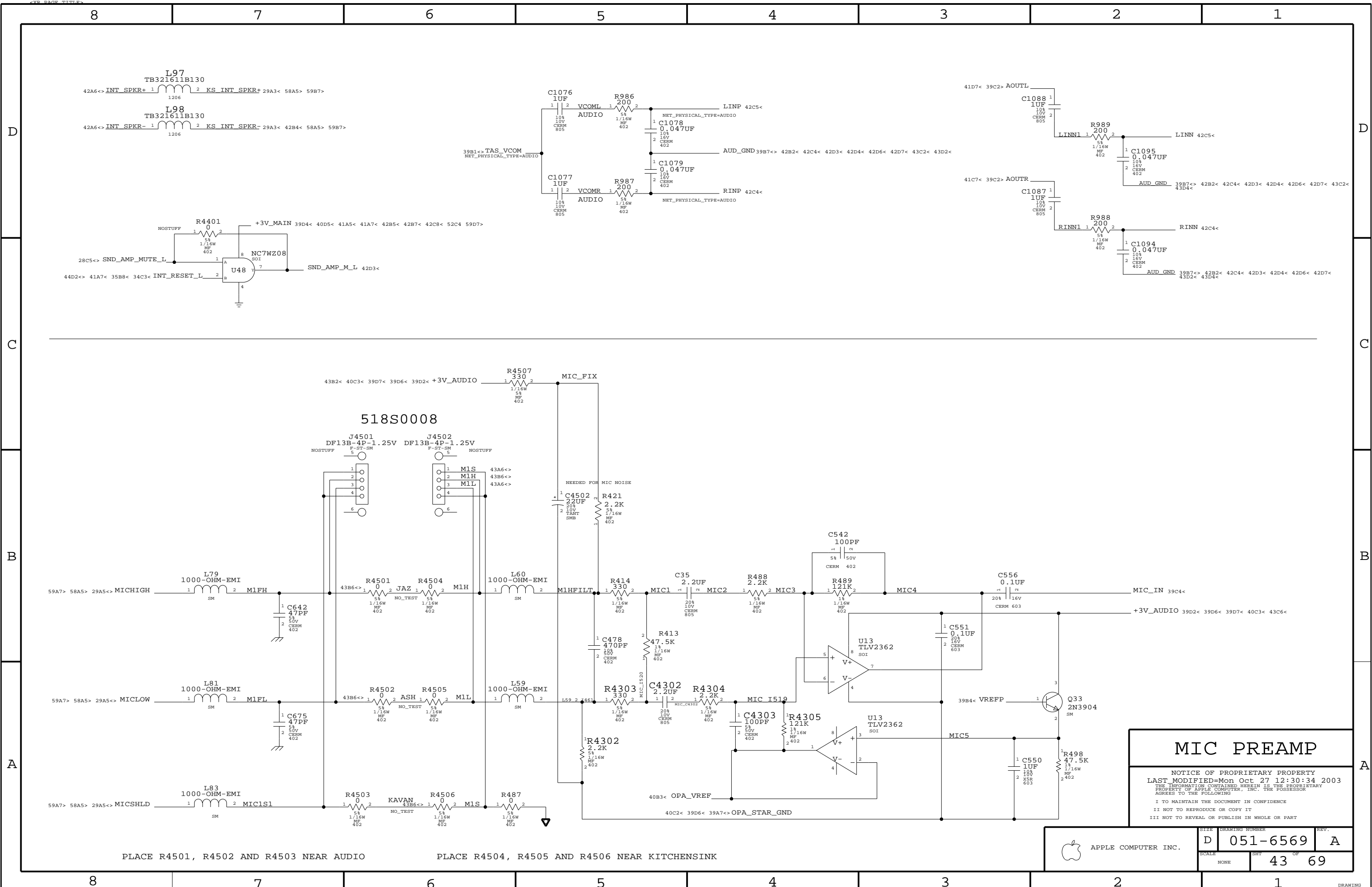
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
101S8000	4	0 OHM, 5%, 1/8W, RES-1206	L90, L91, L93, L96	

PREVIOUS PART NUMBER FOR L90, L91, L93, L96 IS 155S0148

SPEAKER AMP

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6569	A
SCALE	SHEET		OF
NONE	42		69



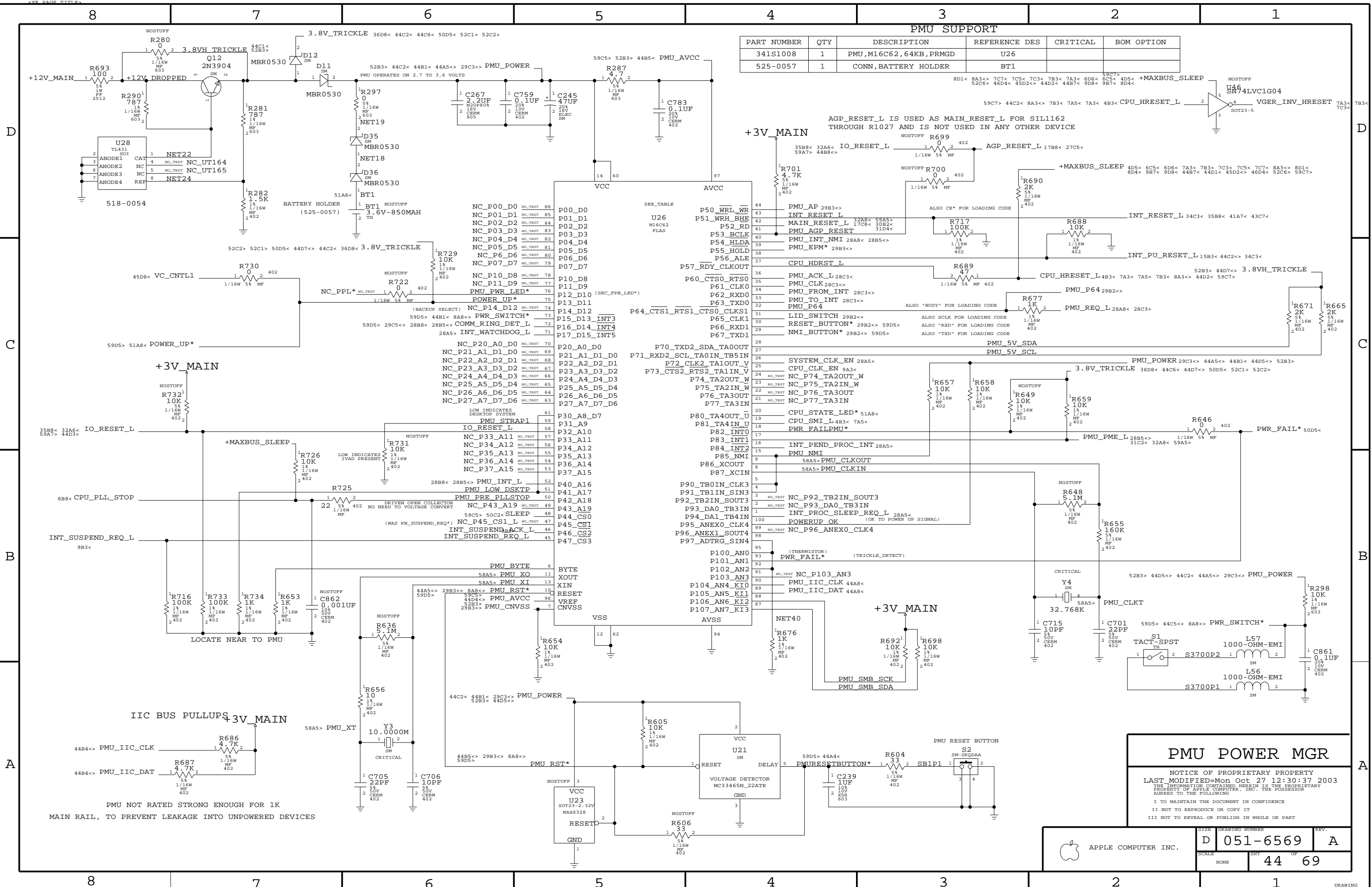
MIC PREAMP

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	D	051-6569	A
SCALE	SHT	OF	
NONE	43	69	

PLACE R4501, R4502 AND R4503 NEAR AUDIO

PLACE R4504, R4505 AND R4506 NEAR KITCHENSINK



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1008	1	PMU, M16C62, 64KB, PRMGD	U26		
525-0057	1	CONN, BATTERY HOLDER	BT1		

Pin	Signal Name	Test Point
86	NC_P00_D0	NO_TEST
85	NC_P01_D1	NO_TEST
84	NC_P02_D2	NO_TEST
83	NC_P03_D3	NO_TEST
82	NC_P04_D4	NO_TEST
81	NC_P05_D5	NO_TEST
80	NC_P06_D6	NO_TEST
79	NC_P07_D7	NO_TEST
78	NC_P10_D8	NO_TEST
77	NC_P11_D9	NO_TEST
76	PMU_PWR_LED*	76
75	POWER_UP*	75
74	NC_P14_D12	NO_TEST
73	NC_P11_D9	NO_TEST
72	COMM_RING_DET_L	72
71	INT_WATCHDOG_L	71
70	NC_P20_A0_D0	NO_TEST
69	NC_P21_A1_D1_D0	NO_TEST
68	NC_P22_A2_D2_D1	NO_TEST
67	NC_P23_A3_D3_D2	NO_TEST
66	NC_P24_A4_D4_D3	NO_TEST
65	NC_P25_A5_D5_D4	NO_TEST
64	NC_P26_A6_D6_D5	NO_TEST
63	NC_P27_A7_D7_D6	NO_TEST
61	PMU STRAP1	59
58	IO_RESET_L	58
57	NC_P33_A11	NO_TEST
56	NC_P34_A12	NO_TEST
55	NC_P35_A13	NO_TEST
54	NC_P36_A14	NO_TEST
53	NC_P37_A15	NO_TEST
52	PMU_INT_L	52
51	PMU_LOW_DSKTP	51
50	PMU_PRE_PLLSTOP	50
49	NC_P43_A19	NO_TEST
48	59C5> 50C2< SLEEP	48
47	NC_P45_CS1_L	NO_TEST
46	INT_SUSPEND_ACK_L	46
45	INT_SUSPEND_REQ_L	45
44	PMU_XO	11
43	PMU_XI	13
42	PMU_RST*	10
41	PMU_AVCC	96
40	PMU_CNVS	7
39	PMU_IIC_CLK	44A8<
38	PMU_IIC_DAT	44A8<
37	PMU_RST*	10
36	PMU_AVCC	96
35	PMU_CNVS	7
34	PMU_RST*	10
33	PMU_AVCC	96
32	PMU_CNVS	7
31	PMU_RST*	10
30	PMU_AVCC	96
29	PMU_CNVS	7
28	PMU_RST*	10
27	PMU_AVCC	96
26	PMU_CNVS	7
25	PMU_RST*	10
24	PMU_AVCC	96
23	PMU_CNVS	7
22	PMU_RST*	10
21	PMU_AVCC	96
20	PMU_CNVS	7
19	PMU_RST*	10
18	PMU_AVCC	96
17	PMU_CNVS	7
16	PMU_RST*	10
15	PMU_AVCC	96
14	PMU_CNVS	7
13	PMU_RST*	10
12	PMU_AVCC	96
11	PMU_CNVS	7
10	PMU_RST*	10
9	PMU_AVCC	96
8	PMU_CNVS	7
7	PMU_RST*	10
6	PMU_AVCC	96
5	PMU_CNVS	7
4	PMU_RST*	10
3	PMU_AVCC	96
2	PMU_CNVS	7
1	PMU_RST*	10

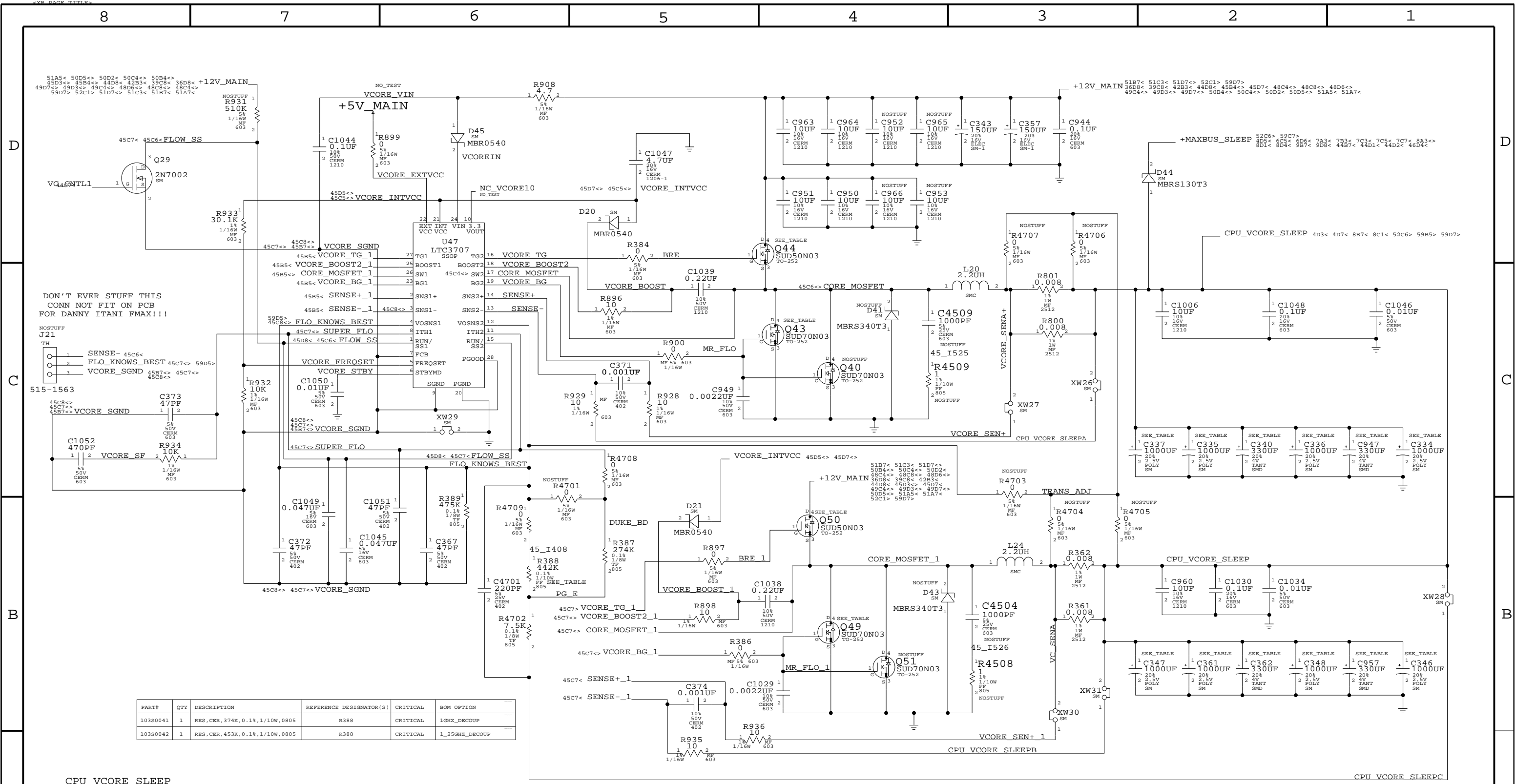
PMU POWER MGR

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SCALE	SHT	OF	
NONE	44	69	

PMU NOT RATED STRONG ENOUGH FOR 1K MAIN RAIL, TO PREVENT LEAKAGE INTO UNPOWERED DEVICES



DON'T EVER STUFF THIS
CONN NOT FIT ON PCB
FOR DANNY ITANI FMAX!!!

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0041	1	RES,CER,374K,0.1%,1/10W,0805	R388	CRITICAL	1GHZ_DECOUP
103S0042	1	RES,CER,453K,0.1%,1/10W,0805	R388	CRITICAL	1_25GHZ_DECOUP

CPU_VCORE_SLEEP
1.0GHZ, 1.5V+30/-130MV, 35W
1.25GHZ, 1.57V+70/-70MV, 35W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	2	MOSFET,N-CH,30V,63A,V30284,TO-252	Q44,Q50	
376S0207	2	MOSFET,N-CH,30V,70A,V30289,TO-252	Q43,Q49	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0012	4	CAP,TANT,POLY,330UF,4.0V,D4	C340,C947,C362,C957	1_25GHZ_DECOUP
128S0410	8	CAP,TANT,POLY,1000UF,2.5V,D4	C337,C335,C336,C334,C347,C361,C48,C346	1_25GHZ_DECOUP
128S0022	12	CAP,EL,POLY,220UF,20%,2V		1GHZ_DECOUP

C337,C335,C336,C334,C347,C361,C348,C346,C340,C947,C362,C957

CPU & AGP VREGS

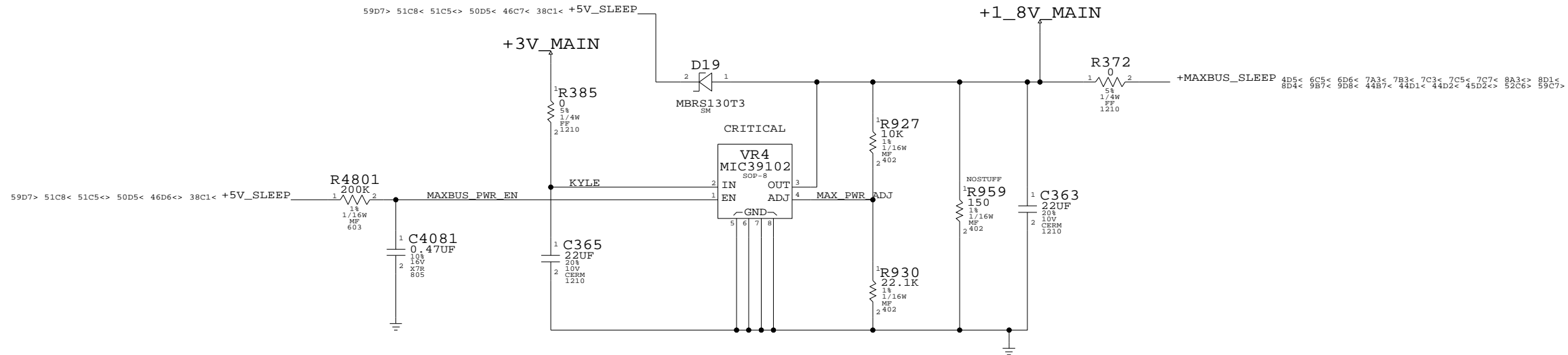
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	NONE	45 OF 69	

INTREPID MAXBUS & CPU OVDD POWER CONVERTER
(OFF DURING SLEEP)

+MAXBUS_SLEEP 1.8V, +/-2%, .606W

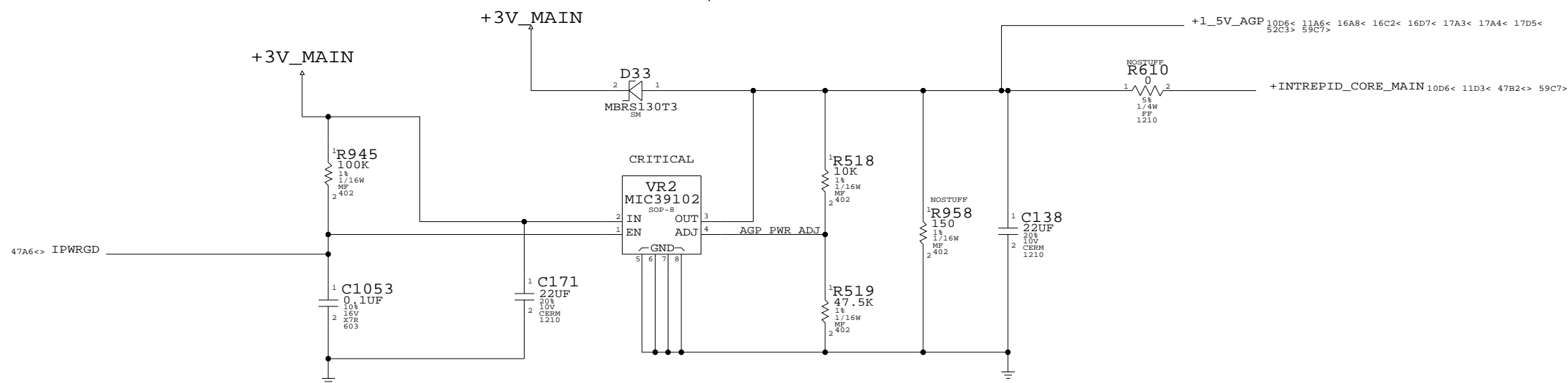


MAXBUS I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES, FF, 47.5K-OHM, 1%	R930		MAXIO_1'50V
114S3014	1	RES, FF, 30.1K-OHM, 1%	R930		MAXIO_1'65V
114S2674	1	RES, FF, 26.7K-OHM, 1%	R930		MAXIO_1'70V
114S2214	1	RES, FF, 22.1K-OHM, 1%	R930		MAXIO_1'80V

+1_5V_AGP 1.5V, +/-5%, .6W

AGP I/O POWER CONVERTER



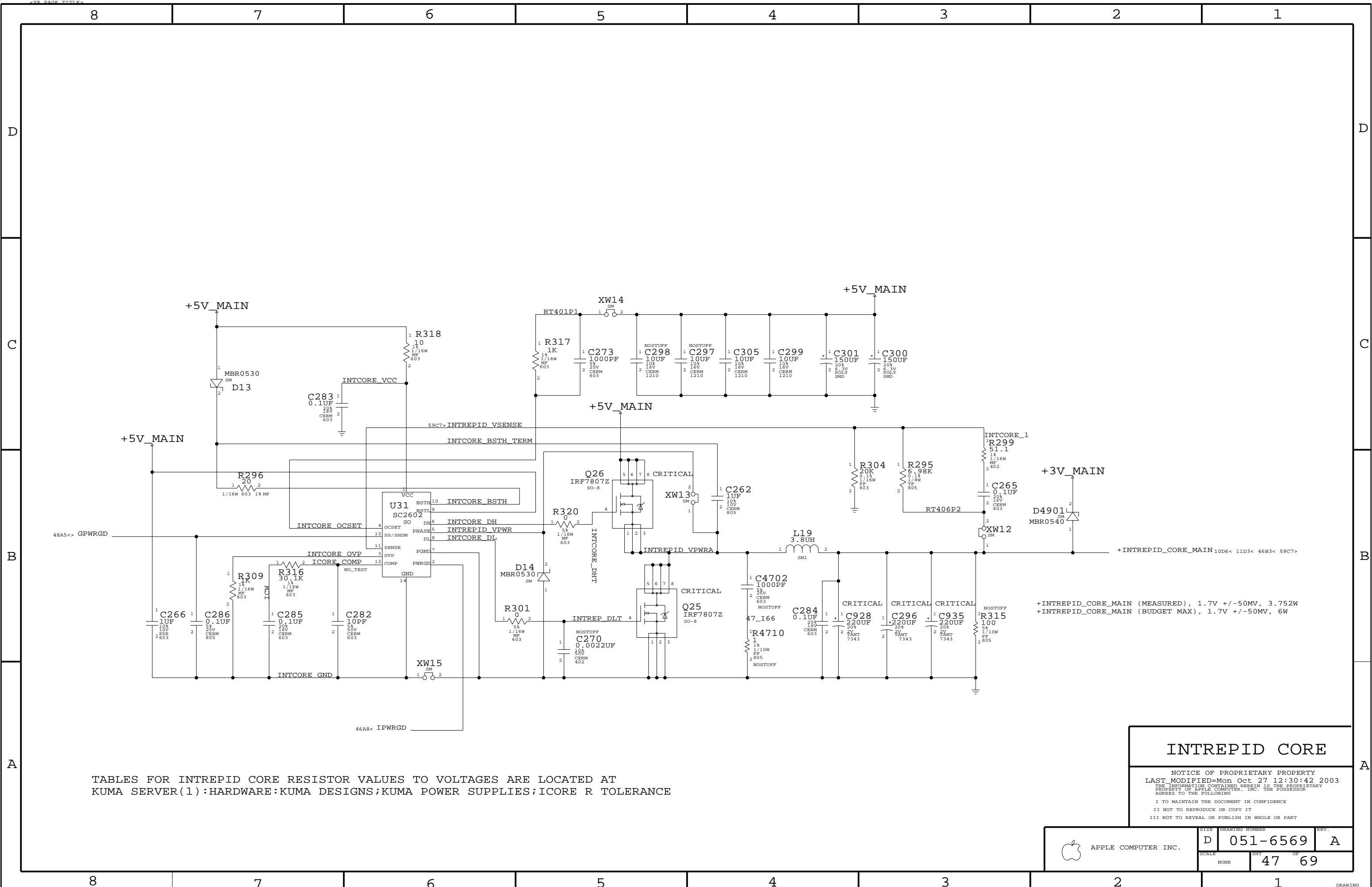
AGP I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES, FF, 47.5K-OHM, 1%	R519		AGPIO_1'50V
114S3014	1	RES, FF, 30.1K-OHM, 1%	R519		AGPIO_1'65V
114S2674	1	RES, FF, 26.7K-OHM, 1%	R519		AGPIO_1'70V
114S2214	1	RES, FF, 22.1K-OHM, 1%	R519		AGPIO_1'80V

CPU & AGP VREGS

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SCALE		SHT	OF
NONE		46	69

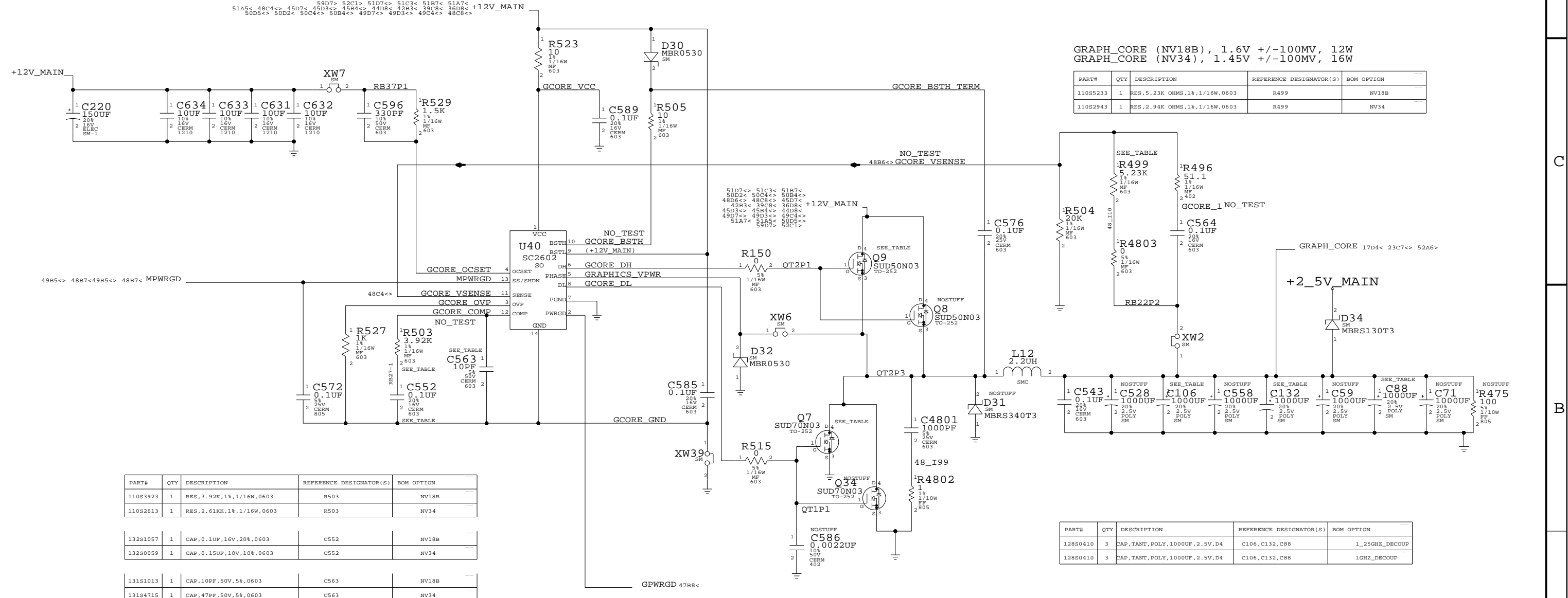


TABLES FOR INTREPID CORE RESISTOR VALUES TO VOLTAGES ARE LOCATED AT
 KUMA SERVER(1):HARDWARE:KUMA DESIGNS;KUMA POWER SUPPLIES;ICORE R TOLERANCE

INTREPID CORE

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APPLE COMPUTER INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-6569	REV.: A
	SHEETS OF 47 69		



GRAPH_CORE (NV18B), 1.6V +/-100MV, 12W
 GRAPH_CORE (NV34), 1.45V +/-100MV, 16W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S233	1	RES,5.23K OHMS,1%,1/16W,0603	R499	NV18B
110S2943	1	RES,2.94K OHMS,1%,1/16W,0603	R499	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S3923	1	RES,3.92K,1%,1/16W,0603	R503	NV18B
110S2613	1	RES,2.61KK,1%,1/16W,0603	R503	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1057	1	CAP,0.1UF,16V,20%,0603	C552	NV18B
132S0059	1	CAP,0.15UF,10V,10%,0603	C552	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S1013	1	CAP,10PF,50V,5%,0603	C563	NV18B
131S4715	1	CAP,47PF,50V,5%,0603	C563	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1_25GHZ_DECOUP
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1GHZ_DECOUP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	1	MOSFET,N-CH,30V,63A,V30284,TO-252	Q9	
376S0207	1	MOSFET,N-CH,30V,70A,V30289,TO-252	Q7	

GRAPHICS CORE

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	SCALE	SHT	OF
	NONE	48	69

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D

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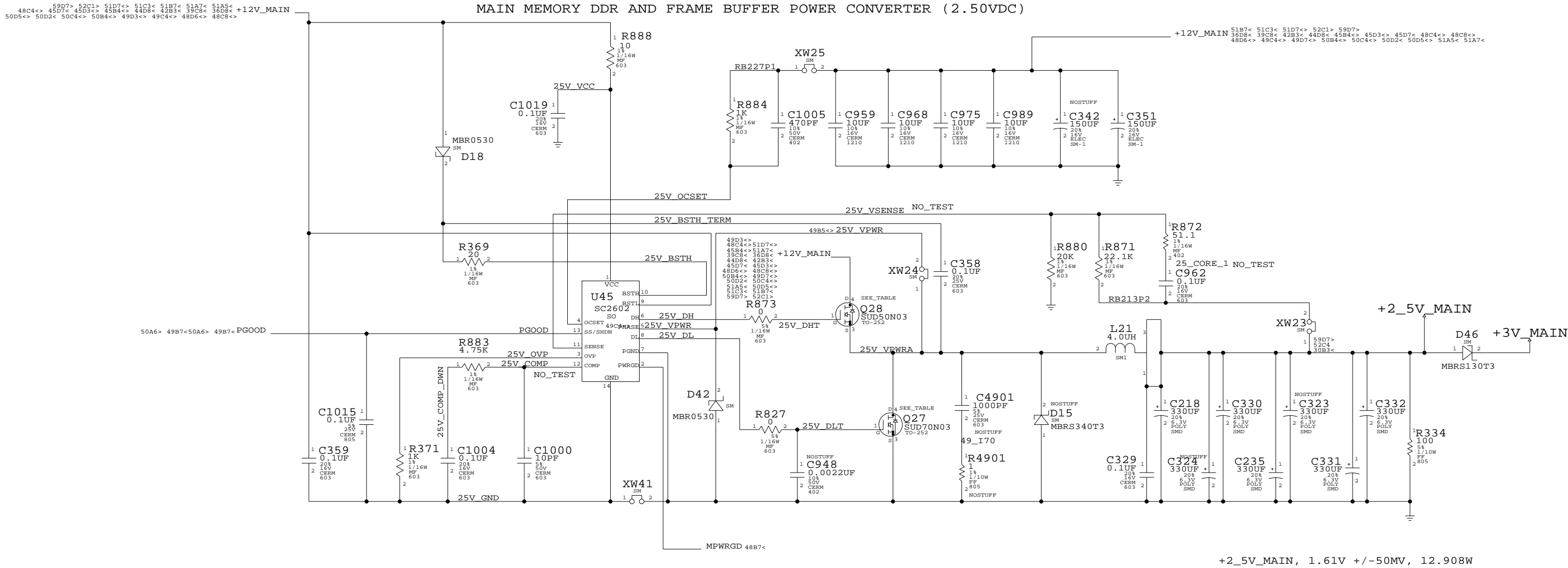
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A



+2_5V_MAIN, 1.61V +/-50MV, 12.908W

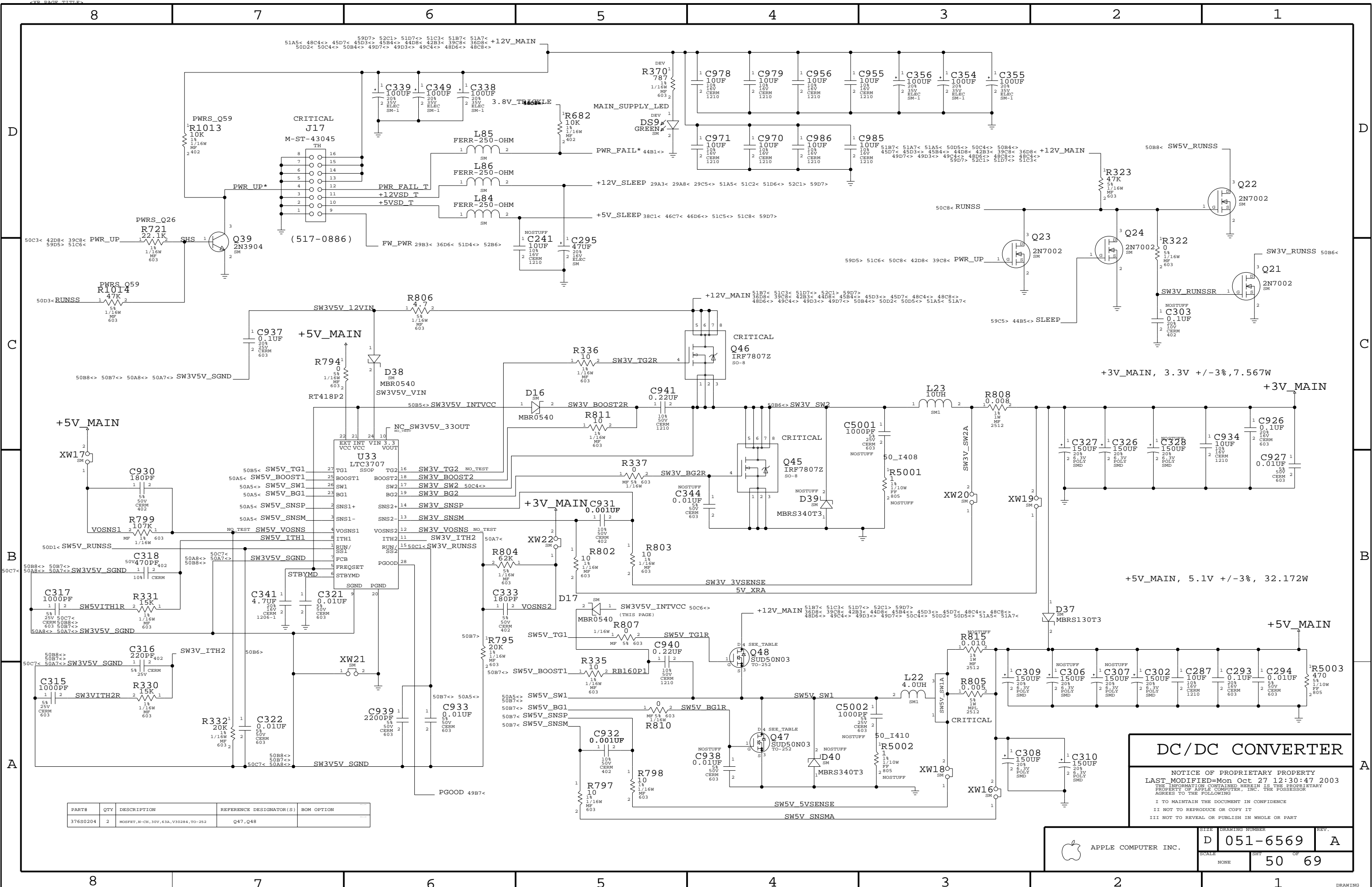
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	1	MOSFET, N-CH, 30V, 63A, V30284, TO-252	Q28	
376S0207	1	MOSFET, N-CH, 30V, 70A, V30289, TO-252	Q27	

MEMORY PS

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SCALE	SHT		OF
NONE	49		69

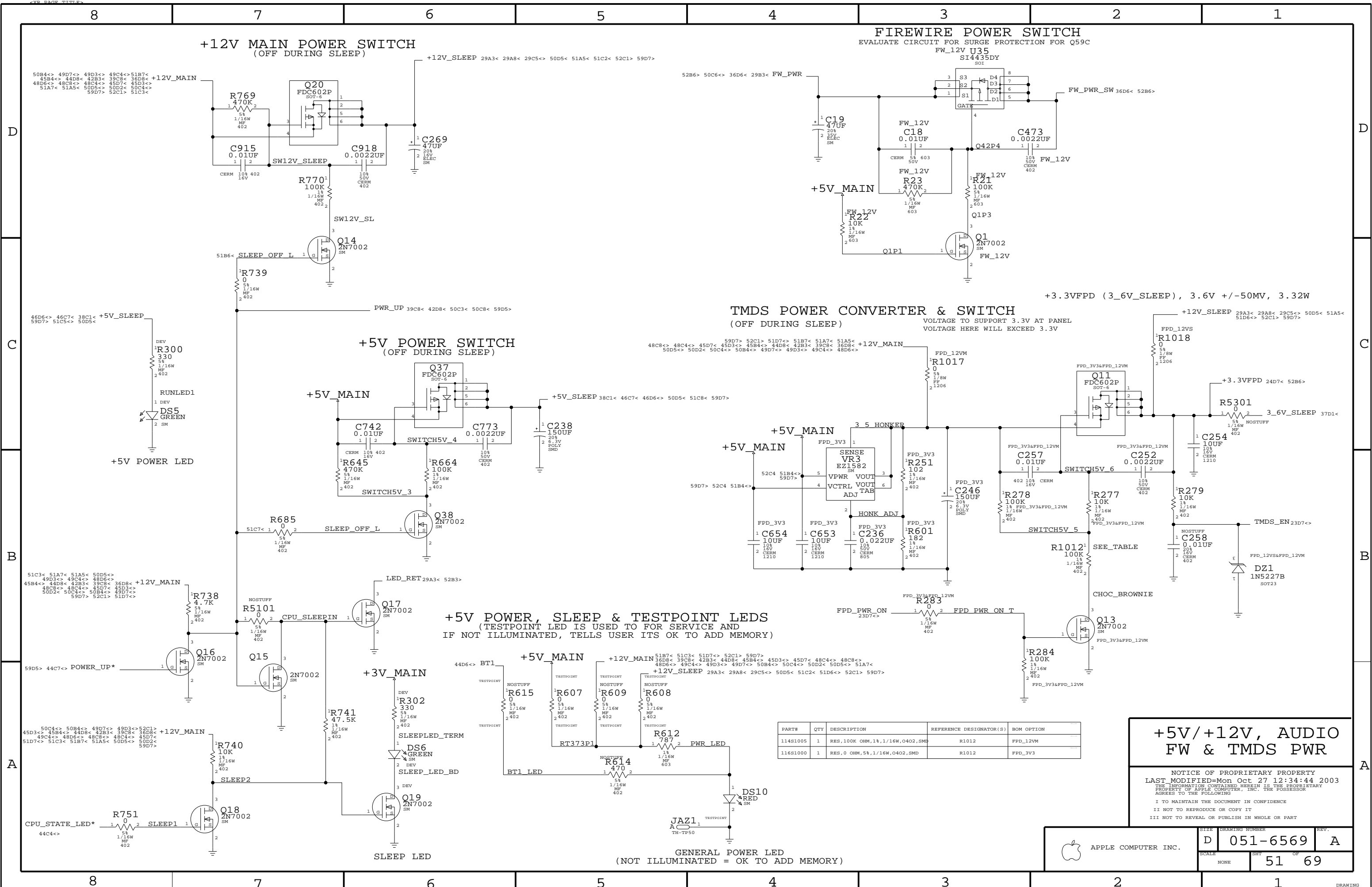


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
37650204	2	MOSFET, N-CH, 30V, 63A, V30204, TO-252	Q47, Q48	

DC/DC CONVERTER

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	SCALE: SHEET OF NONE 50 OF 69



+12V MAIN POWER SWITCH
(OFF DURING SLEEP)

FIREWIRE POWER SWITCH
EVALUATE CIRCUIT FOR SURGE PROTECTION FOR Q59C

+5V POWER SWITCH
(OFF DURING SLEEP)

TMSD POWER CONVERTER & SWITCH
(OFF DURING SLEEP)

+5V POWER, SLEEP & TESTPOINT LEDES
(TESTPOINT LED IS USED FOR SERVICE AND
IF NOT ILLUMINATED, TELLS USER ITS OK TO ADD MEMORY)

**+5V/+12V, AUDIO
FW & TMSD PWR**

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1005	1	RES,100K OHM,1%,1/16W,0402,SMD	R1012	FPD_12VM
116S1000	1	RES,0 OHM,5%,1/16W,0402,SMD	R1012	FPD_3V3

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SCALE		SHT	OF
NONE		51	69

GENERAL POWER LED
(NOT ILLUMINATED = OK TO ADD MEMORY)

CPU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+MAXBUS_SLEEP	10	1.8	20
CPU_AVDD	10	1.85	20
CPU_VCORE_SLEEP	10	1.85	20

4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3< 8D1< 8D4< 9B7< 9D8< 44B7<
 44D1< 44D2< 45D2< 46D4< 59C7>
 4D3< 4D7< 8B7< 8C1< 45D2< 59B5> 59D7>

ETHERNET POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
ENET_AVDD	10	2.5	20

59D7>
 59D7> 49B2<> 30B3<
 43C7< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 39D4<
 59D7>
 59D7> 51B4<>

FIREWIRE POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
FW_DIO_V	10	3.3	20
FW_DIODE_BYPASS_V	10	3.3	20
FW_PWR	10	24	20
FW_PWR_SW	10	24	20
FW_PHY_3_3	10	3.3	20
FW_VGND	10	0	20
FW_VP	10	1.2	20
FW_VP1	10	1.2	20
FW_VP2	10	1.2	20
FW_VP_1	10	1.2	20
FW_VP_2	10	1.2	20

35D2<> 35D4<>
 39B7<>
 41B3< 41B1<> 41A4< 41A2<> 40C6< 40B6< 40B5<> 35C1<> 35B1<
 43A5< 42B6<> 42A5<> 41D3< 41C3<
 36B6<> 36B2< 36A7<> 33D4< 33C4< 32C2< 31B4< 29C3< 29B3<>
 36C1< 36C1<> 36B6<
 43B7< 43A7< 29A3< 24B3<

GRAPHICS POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3.3VFPD	10	3.6	20
DAC2VDD	10	3.3	20
DACVDD	10	3.3	20
DDC_VCC_3	10	3.3	20
DDC_VCC_5	10	5	20
DDR_VREF	10	1.25	20
IFP0AVCC	10	3.8	20
IFP0VREF	10	3.8	20
INT_TMDS_3V	10	3.6	20
GPU_AGP_VREF	10	0.75	20
GPU_FB_VREF	10	1.25	20
GRAPH_CORE	10	1.6	20
NVPLLVD	10	3.3	20
SGRAVREF	10	1.25	20
SGRBVREF	10	1.25	20

36B6<
 36B6<> 36B7<>
 29B3< 36D6< 50C6<> 51D4<>
 36D6< 51D2<>
 36B5< 36B7< 36D7<
 36D5<
 36D1<> 36D3<>
 36C1<> 36D3<>
 36D4<
 36D4<
 24D7< 51C1<>
 22C5<
 22C4<
 24B3<> 59B7>
 25C4< 59B7>
 12A7< 14D2<> 14D8<> 15D8<
 23A6< 23C1<
 23B4<>
 24C3<> 59C7>
 17A2< 17A8<
 18C8<
 17D4< 23C7<> 48C2<>
 22D5<
 20A3< 20C4< 20C8<
 21A3< 21C4< 21C8<

17B5<> GPU_50PULLUP	1.5	
17A5<> GPU_50PULLDOWN	0	
17A5< GPU_TMODE	0	
22B2< 22A5< GPU_XTALSSIN	0	
22D4< VIPCLK	0	
37B7< CSL0T_IOWAIT_L	3.3	
38C6<> EIDE_CSELP_L	0	
38C6<> EIDE_IOCS16_L	5	
38C2<> UIIDE_CSELP_L	0	
38C2<> UNUSED_ATAI0CS16_L	5	

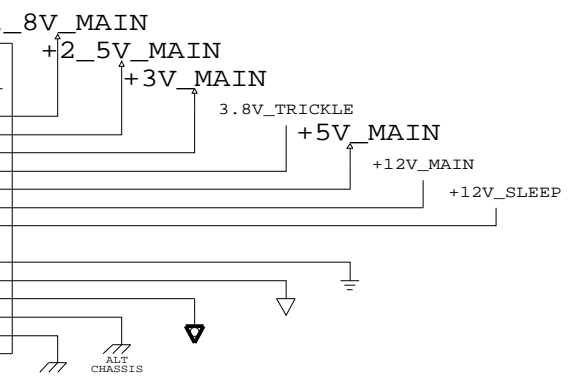
INTREPID POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_5V_INTREPID_PLL	10	1.5	20
+1_5V_INTREPID_PLL1	10	1.5	20
+1_5V_INTREPID_PLL2	10	1.5	20
+1_5V_INTREPID_PLL3	10	1.5	20
+1_5V_INTREPID_PLL4	10	1.5	20
+1_5V_INTREPID_PLL5	10	1.5	20
+1_5V_INTREPID_PLL6	10	1.5	20
+1_5V_INTREPID_PLL7	10	1.5	20
+1_5V_INTREPID_PLL8	10	1.5	20
+1_5V_AGP	10	1.5	20
INT_AGP_VREF	10	0.75	20

9D4< 16D6< 28D6<> 30D5<
 28C4<
 28D4<
 28D4<
 28D4<
 16D5<
 30D4<
 9D2<
 28D4<
 10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17A4< 17D5< 46B4<> 59C7>
 16A7< 16C6<>

MAIN POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_8V_MAIN	10	1.8	20
+2_5V_MAIN	10	2.5	20
+3V_MAIN	10	3.3	20
3.8V_TRICKLE	10	3.8	20
+5V_MAIN	10	5	20
+12V_MAIN	10	12	20
+12V_SLEEP	10	12	20
GND	10	0	20
AGND	10	0	20
ANALOGGND	10	0	20
ALTCGND	10	0	20
CHGND	10	0	20



PMU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
3.8VH_TRICKLE	10	3.8	20
PMU_AVCC	10	3.5	20
PMU_POWER	10	3.5	20

44C1< 44D7<>
 44B5< 44D4<> 59C5>
 29C3<> 44A5<> 44B1< 44C2< 44D5<>

SYSTEM POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+12VSD_FILT	10	12	20
FAN_12V_FILT	10	12	20
KSSVSD	10	5	20
LED_5V	10	5	20
LED_5V_FILT	10	5	20
LED_RET	10	0	20
LED_RET_FILT	10	0	20

29A5<>
 29A5<> 59C7>
 29A5<> 59A7>
 29A8<
 29A5<> 59A7>
 29A3< 51B6<
 29A5<> 59A7>

USB POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3V_INTREPID_USB	10	3.3	20
NEC_AVDD	10	3.3	20
USB_GND	10	0	20
USB_PORT_PWR	10	5	20
USB_PWR	10	5	20

28C4<
 32D5<
 33A4<> 33B3<> 33C3<>
 33B2<> 33B3<> 25D3<> 33A6<>

POWER CONSTRAINTS

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SCALE	SHT	OF	
NONE	52	69	

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SIG_NAME	RATSNEST_SCHEDULE	RELATIVE_PROPAGATION_DELAY	MIN_NECK_WIDTH	MAX_EXPOSED_LENGTH	NO_TEST	FUNC_TEST	PULSE_PARAM
13C4<> 13B6<> 13B3<> 13A6<> 12D8<> 12C8<> 12B8<> MEM_DATA<0..63>	MEM_GROUP0:G:L:S:0:150	8 L:S::1300	3				167 MHZ
13D4<> 13C7<> 13C4<> 13C2<> 13B5<> 13B2<> RAM_DATA_A<0..63>	RAM_GROUP0_A:G:L:S:0:180	8 L:S::1800	3				167 MHZ
14C4<> 14B6<> 14B4<> 14A6<> 14A4<> 13D7<> RAM_DATA_B<0..63>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13B2<> 13A5<> 15D6<> 13A2<> 15A6<> 15B4<> 15B6<> 15C4<> 15C6<> 15D4<>	MEM_GROUP0:G:L:S:0:180	3 L:S::1300	3				167 MHZ
13C8<> 13C4<> 13B3<> 13A6<> 12C6<> MEM_DQS<0..7>	RAM_GROUP0_A:G:L:S:0:180	3 L:S::1700	3				167 MHZ
14A6<> 13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> RAM_DQS_A<0..7>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A8<> 13A5<> RAM_DQS_B<0..7>	MEM_GROUP0:G:L:S:0:180	3 L:S::1300	3				167 MHZ
15D6<> 15C8<> 15C6<> 15C4<> 15B6<> 15B4<> 15A6<> MEM_DQM<0..7>	RAM_GROUP0_A:G:L:S:0:180	3 L:S::1800	3				167 MHZ
13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> 13A5<> RAM_DQM_A<0..7>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A8<> 13A5<> RAM_DQM_B<0..7>							
12D6<> 12D3<> 12D2<> 12C3<> 12C2<> 12B3<> MEM_ADDR<0..12>	MEM_ADDR:G:L:S:0:200	3 L:S::600					
15B4<> 14B6<> 14B4<> 12D3<> 12D1<> 12C3<> 12C1<> 12B3<> RAM_ADDR<0..12>	RAM_ADDR:G:L:S:0:1300	4 L:S::3500	200				
15C6<> 15C4<> 15B6<> 15B4<> 15A6<> 15D4<> 15D2<> 15C6<> 15C4<> 15B6<> 15B4<> 15A6<>	MEM_ADDR:G:L:S:0:1300	3 L:S::600					
15B6<> 14B6<> 14B4<> 12B3<> RAM_BA<0..1>	RAM_ADDR:G:L:S:0:1300	4 L:S::4000	200				
12C6<> 12C2<> 12B2<> MEM_CS_L<0..3>	MEM_ADDR:G:L:S:0:200	3 L:S::600	10 MIL SPACING				
14B6<> 14B4<> 12C1<> RAM_CS_L<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3 L:S:2000:3500	10 MIL SPACING				
15B4<> 12B1<> RAM_CS_L<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2 L:S:2000:3500	10 MIL SPACING				
12C6<> 12A3<> MEM_RAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3 L:S::600 MIL					
12C6<> 12A3<> MEM_CAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3 L:S::600 MIL					
12C6<> 12B3<> MEM_WE_L	MEM_ADDR:G:L:S:0 MIL:280 MIL	3 L:S::600 MIL					
15B6<> 14B4<> 12A2<> RAM_CAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
15B4<> 14B4<> 12A2<> RAM_RAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
15B6<> 14B6<> 12B3<> RAM_WE_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
12C6<> 12C2<> 12B6<> 12B2<> MEM_CKE<0..3>	MEM_ADDR:G:L:S:0:200	3 L:S::600	10 MIL SPACING				
15C1<> 14B6<> 14B4<> 12C1<> 12B1<> RAM_CKE<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3 L:S::2500	10 MIL SPACING				
15C6<> 15C4<> 15B1<> 15A1<> 12C1<> 12B1<> RAM_CKE<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2 L:S::2500	10 MIL SPACING				
12B6<> MEM_MUXSEL_H<0..1>		3 L:S::1000					
12B6<> MEM_MUXSEL_L<0..1>		3 L:S::1000					167 MHZ
13C4<> 13A3<> 12D4<> MUX_SEL_H		4 L:S::2000 MIL	200				167 MHZ
13C8<> 13A6<> 12D4<> MUX_SEL_L		4 L:S::2000 MIL	200				167 MHZ
12B6<> SYSCLK_DDRCLK_A0_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A0_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
14D6<> 12C4<> SYSCLK_DDRCLK_A0	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
14D6<> 12C4<> SYSCLK_DDRCLK_A0_L	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
14A4<> 12C4<> SYSCLK_DDRCLK_A1	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
14A4<> 12B4<> SYSCLK_DDRCLK_A1_L	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_L		3 L:S::750 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15B4<> 12B4<> SYSCLK_DDRCLK_B0	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
12B4<> 15B3<> SYSCLK_DDRCLK_B0_L	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15D6<> 12A4<> SYSCLK_DDRCLK_B1	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
15C6<> 12A4<> SYSCLK_DDRCLK_B1_L	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3 L:S::3200 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15A6<> 12A4<> SYSCLK_DDRCLK_B2	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
15A6<> 12A4<> SYSCLK_DDRCLK_B2_L	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
28A6<> INT_REF_CLK_IN_PD		8 L:S::2500 MIL	10 MIL SPACING	270			66.56 MHZ
31C6<> 31B7<> 31B6<> 30D4<> 30C4<> 30C2<> 30C1<> 30B2<> PCI_AD<31..0>	MIN_DAISSY_CHAIN	6 L:S:6000:8000	500				33 MHZ
59C3<> 59B3<> 31B5<> 31B4<> 31B3<> 31B2<> 31B1<> 31B0<> PCI_CBE<3..0>	MIN_DAISSY_CHAIN	6 L:S:6000:8000	500				33 MHZ
59A5<> 32B6<> 31B7<> 30C5<> 30B7<> PCI_FRAME_L	MIN_DAISSY_CHAIN	L:S:6000 MIL:8000 MIL	500				33 MHZ

DIGITAL SIGNAL CONSTRAINTS

SIGNAL CONSTRAINTS

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	D	051-6569	A
SCALE	SHT		OF
NONE	53		69

D

D

C

C

B

B

A

A

SIG_NAME	RATSNEST_SCHEDULE	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	DIFFERENTIAL_PAIR	FUNC_TEST	PULSE_PARAM
32B6<> 31B7< 30C5<> 30B7< PCI_IRDY_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_TRDY_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_DEVSEL_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_STOP_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> PCI_PAR	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
30D5<> CLK33M_PCI_SLOTB_UF			B:S:600	MIL:10D0	M200		450			33 MHZ
30D5<> CLK33M_PCI_SLOTC_UF			B:S:600	MIL:12D0	M200		450			33 MHZ
30D5<> CLK33M_PCI_SLOTD_UF			B:S:600	MIL:10D0	M200		450			33 MHZ
59A5> 31C2<> 30D7< CLK33M_PCI_SLOTB			I:S:3000	MIL:4000	M200	10 MIL SPACING	450			33 MHZ
30C5<> INT_PCI_FB_OUT			4	L:S::1000	MIL 200		450			33 MHZ
30D8< PCI_FBO_PLUS2			4	L:S::200	MIL 200		450			33 MHZ
30C8< PCI_FB_PLUS4			I4:S:1900	MIL:2000	MIL		450			33 MHZ
30C8< PCI_FBI_PLUS2			I4:S:1900	MIL:2000	M200		450			33 MHZ
30C7< PCI_FBI_EQUAL			I4:S:2000	MIL:3000	M200		450			33 MHZ
30C7< PCI_FB_PLUS6			I4:S:5900	MIL:6000	MIL		450			33 MHZ
30C5< INT_PCI_FB_IN			4	L:S::1080	MIL 200		450			33 MHZ
31C6< 31C3<> 31C2<> 31B7< 31B6< 31B3<> 31B2<> PCIT_AD<31..0>			3	L:S::1000						33 MHZ
59A5> 31C3<> 31B6< 31B2<> PCIT_CBE<31..0>			3	L:S::1000						33 MHZ
31C2<> 31B6< PCIT_FRAME_L			3	L:S::1000	MIL					33 MHZ
59B5> 31C3<> 31B6< PCIT_IRDY_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_TRDY_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_DEVSEL_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_STOP_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_PAR			3	L:S::1000	MIL					33 MHZ
17D8< 17C8< 16C4<> AGP_AD<0..15>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17C8< 16B4<> AGP_CBE<0..1>	AGP_GROUP0:G:L:S:0:330	5	L:S:4500							266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<0>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP0			133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<0>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP0			133 MHZ
17C8< 16C4<> 16B4<> AGP_AD<16..31>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17C8< 16B4<> AGP_CBE<2..3>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<1>	AGP_GROUP0:G:L:S:0 MIL:280	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP1			133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<1>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP1			133 MHZ
17B8< 16C3< 16B4<> AGP_FRAME_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_IRDY_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_TRDY_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_DEVSEL_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_STOP_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_PAR			I:S:4000	MIL:4500	MIL					66 MHZ
17A8< 16C1< 16B4<> 16B4<> 16B1< 16A4<> AGP_SBA<0..7>			5	L:S:4000:4500						AGP_SBSTBB
17B8< 16B3< 16A4<> AGP_SB_STB	AGP_GROUP99:G:L:S:0 MIL:200	MIL	L:S:4500	MIL						AGP_SBSTBB
17A8< 16D1< 16A4<> AGP_SB_STB_L	AGP_GROUP99:G:L:S:0 MIL:200	MIL	L:S:4500	MIL						AGP_SBSTBB
17B6< 16B1< 16A4<> AGP_ST<0..2>			5	L:S:4500:5000						
17B8< 16B3< 16A4<> AGP_PIPE_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B3< 16A4<> AGP_RBF_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B6<> 16C4<> 16C3< AGP_REQ_L			I:S:4500	MIL:5000	MIL					66 MHZ
17B6< 16C4<> 16C3< AGP_GNT_L			I:S:4500	MIL:5000	MIL					66 MHZ
17B8< 16B1< 16A6<> AGP_WBF_L			I:S:4000	MIL:4500	MIL					66 MHZ
17A8> 16D3< 16D1< 16C6<> AGP_BUSY_L			I:S:4500	MIL:5000	MIL					66 MHZ
17A8< 16D3< 16C6<> STOP_AGP_L			I:S:4500	MIL:5000	MIL					66 MHZ
17D7<> 17D6<> 17C6<> GPU_AGP_AD<0..15>	GPU_AGP_GROUP0:G:L:S:0:1003		L:S::600							266 MHZ
17C6<> GPU_AGP_CBE<0..1>	GPU_AGP_GROUP0:G:L:S:0:1003		L:S::600							266 MHZ
AGP_AD_STB_GPU_AGP<0>	GPU_AGP_STB0:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP0			133 MHZ
AGP_AD_STB_L_GPU_AGP<0>	GPU_AGP_STB0:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP0			133 MHZ
17C6<> GPU_AGP_AD<16..31>	GPU_AGP_GROUP1:G:L:S:0:1003		L:S::600							266 MHZ
17C6<> GPU_AGP_CBE<2..3>	GPU_AGP_GROUP1:G:L:S:0:1003		L:S::600							266 MHZ
AGP_AD_STB_GPU_AGP<1>	GPU_AGP_STB1:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP1			133 MHZ
AGP_AD_STB_L_GPU_AGP<1>	GPU_AGP_STB1:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP1			133 MHZ
17B6<> GPU_AGP_FRAME_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_IRDY_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_TRDY_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_DEVSEL_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_STOP_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_PAR			I:S:300	MIL:600	MIL					66 MHZ
17A6<> GPU_AGP_SBA<0..7>			3	L:S:300:600						GPU_SBSTBB
17B6<> GPU_AGP_SB_STB	GPU_AGP_SBSTB:G:L:S:0 MIL:150	MIL	I:S:300	MIL:600	MIL					GPU_SBSTBB
17A6<> GPU_AGP_SB_STB_L	GPU_AGP_SBSTB:G:L:S:0 MIL:150	MIL	I:S:300	MIL:600	MIL					GPU_SBSTBB
17B6<> GPU_AGP_PIPE_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_RBF_L			I:S:300	MIL:600	MIL					66 MHZ
16C6<> CLK66M_GPU_UF			I:S:1000	MIL:1100	MIL	10 MIL SPACING	250			66 MHZ
17C6< 16D8< CLK66M_GPU_AGP			I4:S:3700	MIL:3900	M200	10 MIL SPACING	250			66 MHZ
16C6<> INT_AGP_FB_OUT			I4:S:1400	MIL:1500	M200		250			66 MHZ
16B7< AGP_FBO_EQUAL			B:S:900	MIL:10B0	M200		250			66 MHZ
16B8< AGP_FB_PLUS2			I4:S:1900	MIL:2000	MIL		250			66 MHZ
16C7< AGP_FBI_EQUAL			4	L:S::200	MIL 200		250			66 MHZ
16C6< INT_AGP_FB_IN			4	L:S::1200	MIL 200		250			66 MHZ
30C5<> 30A7< 16D7< INT_ROM_OVERLAY_PU			I:S:600	MIL:800	MIL	10 MIL SPACING	250			66 MHZ
59A7> 56B3> 16C7< 9B4< 8A2< INT_ANALYZER_CLK			3	L:S::2800	MIL	8 MIL SPACING	250			166 MHZ
32A6< 30D7< CLK33M_PCI_SLOTD			I4:S:3000	MIL:3500	M200	8 MIL SPACING	250			33 MHZ

SIGNAL CONSTRAINTS

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	NONE	D 051-6569	A
SCALE		SHT	OF
NONE		54	69

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX EXPOSED LENGTH	PULSE PARAM	
	FBD<0..63>	GPU_FBDDATA_A:G:L:S:0:225		L:S::800				300 MHZ	18E8<> 18F8<> 18G8<> 19C5< 19C8< 19D5< 19D8<
	RFBD<0..63>	RAM_FBDDATA_A:G:L:S:0:300		L:S::1000				300 MHZ	19C4< 19C7< 19D4< 19D7< 20B1<> 20B5<> 20C1<> 20C5<>
	FBDQM<0..7>	GPU_FBDQM_A:G:L:S:0:200		L:S::800				300 MHZ	18D8< 18G3<
	RFBDQM<0..7>	RAM_FBDQM_A:G:L:S:0:200		L:S::1000				300 MHZ	18G2< 20C2< 20C6<
	FBA<0..12>	GPU_FBADDR_A:G:L:S:0:200		L:S::700				300 MHZ	18C8< 18D8< 18E3< 18F3<
	RFBA<0..12>	RAM_FBADDR_A:G:L:S:0:330		L:S::2400	2350			300 MHZ	18E2<> 18F2<> 20C2< 20C6< 20D2< 20D6<
	FBABA<0..1>	GPU_FBADDR_A:G:L:S:0:200		L:S::600				300 MHZ	18C8<> 18E3<
	RFBABA<0..1>	RAM_FBADDR_A:G:L:S:0:330		L:S::2400	50			300 MHZ	18E2<> 20C2< 20C6<
	FBARAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18G3<
	FBACAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18G3<
	FBABE_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18F3<
	FBACSO_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18F3<
	FBACKE_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL			100			300 MHZ	18D3< 18D7<>
	RFBARAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18G2<> 20B2< 20B6<
	RFBACAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18G2<> 20B2< 20B6<
	RFBABE_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACSO_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACKE_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18D2<> 20C2< 20C6<
	FBDQS<0..7>	GPU_FBDQS_A:G:L:S:0:100		L:S::350				300 MHZ	18C7< 19A8<
	FBDOSTERM<0..7>	FB_DQSTERM_A:G:L:S:0:50		L:S::1500		10 MIL SPACING		300 MHZ	19A7<
	RFBDQS<0..7>	RAM_FBDQS_A:G:L:S:0:55		L:S::150		10 MIL SPACING		300 MHZ	19A6< 20C2<> 20C6<>
	FBACLK0	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19C3<
	FBACLK0_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19C3<
	FBACLK1	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19D3<
	FBACLK1_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19D3<
	RFBACLK1	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL:S::2500 MIL					200	300 MHZ	19D1< 20C2<
	RFBACLK1_L	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL:S::2500 MIL					200	300 MHZ	19D1< 20C2<
	RFBACLK0	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL:S::2500 MIL					200	300 MHZ	19C1< 20C6<
	RFBACLK0_L	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL:S::2500 MIL					200	300 MHZ	19C1< 20C6<
	FBD<64..127>	GPU_FBDDATA_B:G:L:S:0:225		L:S::800				300 MHZ	18E5<> 18F5<> 18G5<> 19B5< 19B8< 19C5< 19C8<
	RFBD<64..127>	RAM_FBDDATA_B:G:L:S:0:325		L:S::1000				300 MHZ	19B4< 19B7< 19C4< 19C7< 21B1<> 21B5<> 21C1<> 21C5<>
	FBDQM<8..15>	GPU_FBDQM_B:G:L:S:0:120		L:S::800				300 MHZ	18C3< 18D3< 18D5<
	RFBDQM<8..15>	RAM_FBDQM_B:G:L:S:0:120		L:S::1000				300 MHZ	18C2< 18D2< 21C2< 21C6<
	FBBAA<0..12>	GPU_FBADDR_B:G:L:S:0:220		L:S::600				300 MHZ	18A3< 18B3< 18C3< 18C5<> 18D5<>
	RFBBAA<0..12>	RAM_FBADDR_B:G:L:S:0:370		L:S::2400	50			300 MHZ	18B2<> 18C2<> 21C2< 21C6< 21D2< 21D6<
	FBBBA<0..1>	GPU_FBADDR_B:G:L:S:0:220		L:S::600				300 MHZ	18A3< 18C5<>
	RFBBBA<0..1>	RAM_FBADDR_B:G:L:S:0:370		L:S::2400	50			300 MHZ	18A2<> 21C2< 21C6<
	FBBRAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBCAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBWE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBCSO_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18C4<>
	FBBCKE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL			100			300 MHZ	18A3< 18C4<>
	RFBBRAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBWE_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCSO_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCKE_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18A2<> 21C2< 21C6<
	FBDQS<8..15>	GPU_FBDQS_B:G:L:S:0:190		L:S::350				300 MHZ	18D4<> 19A5<
	FBDOSTERM<8..15>	FB_FBDQSTERM_B:G:L:S:0:60		L:S::1500		10 MIL SPACING		300 MHZ	19A4<
	RFBDQS<8..15>	RAM_FBDQS_B:G:L:S:0:59		L:S::150		10 MIL SPACING		300 MHZ	19A3< 21C2<> 21C6<>
	FBBCLK0	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	FBBCLK0_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	FBBCLK1	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19C3<
	FBBCLK1_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	RFBBCLK1	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19C1< 21C2<
	RFBBCLK1_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C2<
	RFBBCLK0	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C6<
	RFBBCLK0_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C6<

SIGNAL CONSTRAINTS

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	D	051-6569	A
SCALE	SHEET		OF
NONE	55		69

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MIN_LENGTH	PROPAGATION_DELAY	MIN_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MAX_EXPOSED_LENGTH	
MAXBUS	CPU_ADDR<0..31>	CPU_ADDR_GROUP:G:L:S:0	100	250				166 MHZ		4B7<> 4C7<> 8B4<> 8B5<> 8B7<> 8B8<> 8C4<> 8C5<> 8C7<> 8C8<>
	CPU_DATA<0..63>	CPU_DATA_GROUP:G:L:S:0	150	1550				166 MHZ		8C3<> 9D3<> 9D5<> 9D8<>
	CPU BR L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		5B4<> 5B4<> 5D4<> 5D4<> 6C4<> 8C4<> 8C4<> 8C5<> 8C7<> 8C7<> 8C8<>
	CPU BG L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		8D4<> 8D5<> 8D7<> 8D8<> 9A7<> 9B1<> 9B7<> 9C1<> 9C5<> 9C8<> 9D1<>
	CPU TS L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4D7<> 7C7<> 8B4<> 9D3<>
	CPU TT<0..4>	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4D7<> 7C7<> 8B7<> 9D3<>
	CPU TBST L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B7<> 7A7<> 8B4<> 8B5<> 9B3<>
	CPU TSIZ<0..2>	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B7<> 7B7<> 8B4<> 9B3<>
	CPU ARTRY L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B7<> 8B5<> 8B7<> 9B3<>
	CPU AACK L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4A7<> 7C7<> 8B8<> 9B3<>
	CPU GBL L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4A7<> 7B7<> 8B5<> 9B3<>
	CPU INT_GBL L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B8<> 8B5<>
	CPU CI L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B8<> 7B7<> 9C3<>
	CPU HIT L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4A7<> 7A7<> 8C5<> 9C3<>
	CPU DBG L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4A7<> 7C7<> 8B8<> 9B3<>
	CPU DRDY L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<> 7B7<> 8B8<> 9B1<>
	CPU WT L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C2<> 7B7<> 8B5<> 9B1<>
	CPU DRDY L UP	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4B7<> 7A7<> 8B5<> 9B3<>
	CPU DTI<0..2>	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<>
	CPU TA L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<> 8B4<> 8B7<> 9A1<>
	CPU TEA L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<> 7C7<> 8C4<> 9A1<>
	CPU QREQ L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<> 7B7<> 8B5<> 9A1<>
	CPU QACK L	CPU_CNTRL_GROUP:G:L:S:0	10 MIL SPACING	250				166 MHZ		4C3<> 7D5<> 8B7<> 9B3<>
	SYSCLK_CPU UP			2	150			166 MHZ	315	4C3<> 8B4<> 9B3<>
	SYSCLK_CPU			4	2200	2400	200	166 MHZ	315	9A3<>
	INT_CPU_FB_OUT			3	1000	200		166 MHZ	315	4D2<> 9A4<
	CPU_FBO_PLUS1			3	200	200		166 MHZ	315	9B3<>
	CPU_FBI_PLUS1			3	1400	1500	200	166 MHZ	315	9A5<
	CPU_FB_MINUS3			4	900	1000	200	166 MHZ	315	9A5<
	INT_CPU_FB_IN			4	1000	200		166 MHZ	315	9A4<
	CPU_FB_PLUS2			3	900	1000		166 MHZ	315	9B3<
	CPU_FB_PLUS3			3	2900	3000		166 MHZ	315	9A5<
	INT_ANALYZER_CLK			3	300			166 MHZ		9A4<
	SYSCLK_LA			2	2000			166 MHZ		8A2<> 9B4<> 16C7<> 54A7<> 59A7>
	INT_CLOCK_OUT			3	3000			166 MHZ		8A2<> 8D8<>
MIN LINE WIDTH DIFFERENTIAL PAIR										
USB2_XT1			3	1000	100	10 MIL SPACING		30 MHZ		32C4<
USB2_XT2_B			3	1000	100	10 MIL SPACING		30 MHZ		32C4<>
USB2_XT2			3	100	100	10 MIL SPACING		30 MHZ		32B4<>
USB2_RREF			2	100						32C4<>
USB2_RSDAM	USB2_RSDA:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32B4<>
USB2_RSDAP	USB2_RSDA:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32C4<>
USB2_RSDBM	USB2_RSDB:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32C4<>
USB2_RSDBP	USB2_RSDB:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32C4<>
USB2_RSDCM	USB2_RSDB:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32C4<>
USB2_RSDCP	USB2_RSDB:G:L:S:0	0.2MIL	30	500		8 MIL SPACING	3.5	480 MHZ		32C4<>
USB2_DAN_F	USB2_DMA:G:L:S:0	0.1MIL	30	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN DAISY_CHAIN
USB2_DAP_F	USB2_DMA:G:L:S:0	0.1MIL	30	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN DAISY_CHAIN
USB2_DBN_F	USB2_DMB:G:L:S:0	0.1MIL	20	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN DAISY_CHAIN
USB2_DBP_F	USB2_DMB:G:L:S:0	0.1MIL	20	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN DAISY_CHAIN
USB2_DCN_F	USB2_DMC:G:L:S:0	0.1MIL	20	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN DAISY_CHAIN
USB2_DCP_F	USB2_DMC:G:L:S:0	0.1MIL	20	500	50	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN DAISY_CHAIN
USBT_DAN_F	USB2_DMAT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN DAISY_CHAIN
USBT_DAP_F	USB2_DMAT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN DAISY_CHAIN
USBT_DBN_F	USB2_DMBT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN DAISY_CHAIN
USBT_DBP_F	USB2_DMBT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN DAISY_CHAIN
USBT_DCN_F	USB2_DMCT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN DAISY_CHAIN
USBT_DCP_F	USB2_DMCT:G:L:S:0	0.4MIL	60	3000	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN DAISY_CHAIN
USB_DAN_CON	USB2_CONA:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN DAISY_CHAIN
USB_DAP_CON	USB2_CONA:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN DAISY_CHAIN
USB_DBN_CON	USB2_CONB:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN DAISY_CHAIN
USB_DBP_CON	USB2_CONB:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN DAISY_CHAIN
USB_DCN_CON	USB2_CONC:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN DAISY_CHAIN
USB_DCP_CON	USB2_CONC:G:L:S:0	0.2MIL	30	750	50	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN DAISY_CHAIN

SIGNAL CONSTRAINTS

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	D	051-6569	A
SCALE	SHT		OF
NONE	56		69

DIGITAL SIGNALS

DIGITAL SIGNALS

Table with columns: GROUP, SIG_NAME, RELATIVE_PROPAGATION_DELAY, MAX_VIAS, STUB_LENGTH, NET_SPACING_TYPE, MAX_EXPOSED_LENGTH, PULSE_PARAM. Includes signals like VSYNC*, ANALOG_VSYNC*, HSYNC*, ANALOG_HSYNC*, ANALOG_BLU, ANALOG_GRN, ANALOG_RED, FILT_ANALOG_RED, FILT_ANALOG_GRN, FILT_ANALOG_BLU, DAC2RSET, DAC2VREF, NV11_XTALIN, NV11_XTALOUT, TCKP, TCKM, TD0P, TD0M, TD1P, TD1M, TD2P, TD2M, ENET_LINK_TX_EN, ENET_LINK_TX_ER, ENET_LINK_TXD<0..3>, ENET_PHY_TX_EN, ENET_PHY_TX_ER, ENET_PHY_TXD<0..3>, CLKENET_LINK_TX, CLKENET_PHY_TX, CLKENET_LINK_RX, CLKENET_PHY_RX, ENET_PHY_RXD<0..3>, ENET_PHY_RX_DV, ENET_PHY_RX_ER, ENET_PHY_CRS, ENET_PHY_COL, ENET_LINK_RXD<0..3>, ENET_CRS, ENET_COL, ENET_RX_DV, ENET_RX_ER, CLK25M_ENET_XIN, CLK25M_ENET_XOUT, ENET_TDP, ENET_TDN, ENET_RDP, ENET_RDN, RJ45_TXP, RJ45_TXN, RJ45_RXP, RJ45_RXN, RJ45_TREF, RJ45_RREF, RJ45_4_5, RJ45_7_8, RJ45_F_TREF, FW_LINK_DATA<0..7>, FW_LINK_CNTL<0..1>, FW_LINK_LREQ, FW_SCLK, FW_D<0..7>, FW_CNTL0, FW_CNTL1, FW_LREQ, FW_PHY_SCLK, FW_PHY_CNTL0, FW_PHY_CNTL1, FW_PHY_D<0..7>, FW_XI, FW_XO, FW_BIAS1, FW_BIAS2, FW_TPA1P, FW_TPA1N, FW_TPB1P, FW_TPB1N, FW_TPA2P, FW_TPA2N, FW_TPB2P, FW_TPB2N, FW_TPO1P, FW_TPO1N, FW_TPL1P, FW_TPL1N, FW_TPO2P, FW_TPO2N, FW_TPL2P, FW_TPL2N.

Table with columns: GROUP, SIG_NAME, RELATIVE_PROPAGATION_DELAY, MAX_VIAS, STUB_LENGTH, NET_SPACING_TYPE, MAX_EXPOSED_LENGTH, PULSE_PARAM. Includes signals like TMDS_CKP, TMDS_CKM, TMDS_D0P, TMDS_D0M, TMDS_D1P, TMDS_D1M, TMDS_D2P, TMDS_D2M, GPU_TMDS_CKP, GPU_TMDS_CKM, GPU_TMDS_D0P, GPU_TMDS_D0M, GPU_TMDS_D1P, GPU_TMDS_D1M, GPU_TMDS_D2P, GPU_TMDS_D2M, SI_TMDS_CKP, SI_TMDS_CKM, SI_TMDS_D0P, SI_TMDS_D0M, SI_TMDS_D1P, SI_TMDS_D1M, SI_TMDS_D2P, SI_TMDS_D2M, DVOD0, DVOD1, DVOD2, DVOD3, DVOD4, DVOD5, DVOD6, DVOD7, DVOD8, DVOD9, DVOD10, DVOD11.

D

C

B

A

D

C

B

A

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SHEET: 57 OF 69
REV: A

DIGITAL SIGNALS (CONT'D)

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX VIAS	PROPAGATION DELAY	STUB LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM		
CD DRIVE BUS	EIDE_RST_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 37D5<	
	EIDE_DMACK_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7<> 37D5<	
	EIDE_STOP			L:S:5500 MIL				33 MHZ	37A7> 37D5<	
	EIDE_HSTB_RDY			L:S:5500 MIL				33 MHZ	37A7> 37C5<	
	EIDE_DSTB_RDY			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 37C5<	
	EIDE_DATA<0..15>			L:S:3500:5500				33 MHZ	37A5< 37B5< 37B7<> 37C5<	
	CD_RESET_L			L:S:1000 MIL				33 MHZ	37D4< 38C6<>	
	CD_DMACK_L			L:S:4000 MIL				33 MHZ	37D4< 38C6<>	
	CD_STOP			L:S:5000 MIL				33 MHZ	37D4< 38C6<>	
	CD_HSTB_RDY			L:S:5000 MIL				33 MHZ	37C4< 38C6<>	
	CD_DSTB_RDY			L:S:1000 MIL				33 MHZ	37C4< 38C6<>	
	UATAD<0..15>			L:S:1000				33 MHZ	37A4< 37B4< 37C4< 38C6<>	
	CD_DMARQ			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_DMARQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<	
	UATAOIRO			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_INTRO			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<	
	CD_EIDE_ADDR<0..2>			L:S:1000				33 MHZ	38C6<>	
	EIDE_ADDR<0..2>			L:S:3500:5500				33 MHZ	37B7> 38A8< 38B8<	
	CD_CS1FX_L			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_CS1FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<	
	CD_CS3FX_L			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_CS3FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<	
	HD DRIVE BUS	UIDE_RST_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DMACK_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOR_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOW_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<>
		UIDE_IOCHRDY	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<>
		UIDE_DATA<0..15>	HD_DATA:G:L:S:0		L:S:100:6000				100 MHZ	37C3< 37C7<
		HD_RESET_L			L:S:1000 MIL				100 MHZ	37A3< 37B3< 37C3< 37C7<> 37D7<>
		HD_DMACK_L			L:S:1000 MIL				100 MHZ	37D1< 38C3<>
HD_DIOR_L				L:S:5500 MIL				100 MHZ	37D1< 38C3<>	
HD_DIOW_L				L:S:55000 MIL				100 MHZ	37C1< 38C3<>	
HD_IOCHRDY				L:S:1000 MIL				100 MHZ	37C1< 38C3<>	
HD_DMARQ				L:S:1000 MIL				100 MHZ	38C3<>	
UIDE_DMARQ		HD_DATA:G:L:S:0		L:S:5500 MIL:6000 MIL				100 MHZ	37C7<> 38C4<	
HD_INTRO				L:S:1000 MIL				100 MHZ	38C3<>	
UIDE_INTRO		HD_DATA:G:L:S:0		L:S:5500 MIL:6000 MIL				100 MHZ	37C7< 38C4<	
HD_UIDE_ADDR<0..2>				L:S:1000				100 MHZ	38C2<> 38C3<>	
UIDE_ADDR<0..2>		HD_DATA:G:L:S:0		L:S:100:6000				100 MHZ	37C7<> 38A4< 38B4<	
HD_UIDE_CS1FX_L				L:S:6000 MIL				100 MHZ	38C3<>	
UIDE_CS1FX_L		HD_DATA:G:L:S:0		L:S:5500 MIL				100 MHZ	37C7<> 38B4<	
HD_UIDE_CS3FX_L				L:S:6000 MIL				100 MHZ	38C2<>	
UIDE_CS3FX_L		HD_DATA:G:L:S:0		L:S:5500 MIL				100 MHZ	37C7<> 38B4<	
CLK_18M_INT_XOUT			3		L:S:1000 100	8 MIL SPACING		18.432 MHZ	58B5>	
CLK_18M_INT_XOUT			3		L:S:1000 100	8 MIL SPACING		18.432 MHZ	58B5>	
CLK_18M_INT_XOUT			3		L:S:200 50	8 MIL SPACING		18.432 MHZ	58B5>	
USB_DAP		USBA:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DAN		USBA:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DAP_F		USBA_F:G:L:S:0		MIL:500 MIL	100				28B2< 33B7<	
USB_DAN_F		USBA_F:G:L:S:0		MIL:500 MIL	100				28B2< 33B7<	
USB_DBP		USBB:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DBN		USBB:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DBP_F	USBB_F:G:L:S:0		MIL:500 MIL	100				28B2< 33C7<		
USB_DBN_F	USBB_F:G:L:S:0		MIL:500 MIL	100				28B2< 33C7<		
USB_DCP	USBC:G:L:S:0		MIL:500 MIL					28A3< 28B3<>		
USB_DCN	USBC:G:L:S:0		MIL:500 MIL					28A3< 28B3<>		
USB_DCP_F	USBC_F:G:L:S:0		MIL:500 MIL	100				28B2< 33D7<		
USB_DCN_F	USBC_F:G:L:S:0		MIL:500 MIL	100				28B2< 33D7<		
USB_DEP	USBE:G:L:S:0		MIL:500 MIL					28B3<>		
USB_DEN	USBE:G:L:S:0		MIL:500 MIL					28B3<>		
BT_USB_DP	USBE_F:G:L:S:0		MIL:500 MIL	100				28B2< 29D3<> 59B5>		
BT_USB_DM	USBE_F:G:L:S:0		MIL:500 MIL	100				28B2< 29D3<> 59B5>		
USB_DFP	USBF:G:L:S:0		MIL:500 MIL					28B3<>		
USB_DFN	USBF:G:L:S:0		MIL:500 MIL					28B3<>		
MODEM_USB_DP	USBF_F:G:L:S:0		MIL:500 MIL	100				28B2< 29C5<> 59B5>		
MODEM_USB_DM	USBF_F:G:L:S:0		MIL:500 MIL	100				28B2< 29C5<> 59B5>		
PMU_XO		3		L:S:1000 MDD	8 MIL SPACING		10 MHZ	44B5<		
PMU_XI		3		L:S:1000 MDD	8 MIL SPACING		10 MHZ	44B5<		
PMU_XT		3		L:S:300 MDD	8 MIL SPACING		10 MHZ	44A6<		
PMU_CLKOUT		3		L:S:1000 MDD	8 MIL SPACING		32.768 MHZ	44B4<>		
PMU_CLKIN		3		L:S:1000 MDD	8 MIL SPACING		32.768 MHZ	44B4<>		
PMU_CLKT		3		L:S:300 MDD	8 MIL SPACING		32.768 MHZ	44B2<>		
MICSHLD					10 MIL SPACING			29A5<> 43A8< 59A7>		
MICHIGH					10 MIL SPACING			29A5<> 43B8< 59A7>		
MICLOW					10 MIL SPACING			29A5<> 43A8< 59A7>		
KS_INT_SPKR+					10 MIL SPACING			29A3< 43D7< 59B7>		
KS_INT_SPKR-					10 MIL SPACING			29A3< 42B4< 43D7< 59B7>		

SIG_NAME	PROPAGATION_DELAY	PARAM	
T_UD_IDEDD_0	L:S:1000 MIL	100 MHZ	37C1< 38C3<>
T_UD_IDEDD_1	L:S:1000 MIL	100 MHZ	37C1< 38C3<>
T_UD_IDEDD_2	L:S:1000 MIL	100 MHZ	37C1< 38C3<>
T_UD_IDEDD_3	L:S:1000 MIL	100 MHZ	37C1< 38C3<>
T_UD_IDEDD_4	L:S:1000 MIL	100 MHZ	37B1< 38C3<>
T_UD_IDEDD_5	L:S:1000 MIL	100 MHZ	37B1< 38C3<>
T_UD_IDEDD_6	L:S:1000 MIL	100 MHZ	37B1< 38C3<>
T_UD_IDEDD_7	L:S:1000 MIL	100 MHZ	37B1< 38C3<>
T_UD_IDEDD_8	L:S:1000 MIL	100 MHZ	37B1< 38C2<>
T_UD_IDEDD_9	L:S:1000 MIL	100 MHZ	37B1< 38C2<>
T_UD_IDEDD_10	L:S:1000 MIL	100 MHZ	37B1< 38C2<>
T_UD_IDEDD_11	L:S:1000 MIL	100 MHZ	37B1< 38C2<>
T_UD_IDEDD_12	L:S:1000 MIL	100 MHZ	37B1< 38C2<>
T_UD_IDEDD_13	L:S:1000 MIL	100 MHZ	37A1< 38C2<>
T_UD_IDEDD_14	L:S:1000 MIL	100 MHZ	37A1< 38C2<>
T_UD_IDEDD_15	L:S:1000 MIL	100 MHZ	37A1< 38C2<>

SIGNAL CONSTRAINTS

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NONE	58	69	

FUNC_TEST

FUNC_TEST

FUNC_TEST

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52C4	+1_8V_MAIN	52C4
51B7< 51A7< 51A5< 50D5< 50D2< 50C4< 50B4< 50B3< 50B2< 50B1< 45D7< 45D3< 45B4< 44D8< 42B3< 39C8< 36D2< 49D7< 49D3< 49C4< 48B6< 48C8< 48C4< 51D6< 51C2< 51A5< 50D5< 29C5< 29A8< 29A3< 52C1>	+12V_MAIN +12V_SLEEP +12V_SLEEPA +5V_MAIN +5V_SLEEP +2_5V_MAIN +3V_MAIN CPU_VCORE_SLEEP JTAG_ASIC_TCK JTAG_ASIC_TDI JTAG_ASIC_TDO JTAG_ASIC_TMS JTAG_ASIC_TRST_L INT_TMDS_3V +1_5V_AGP FAN_12V_FILT +INTREPID_CORE_MAIN INTREPID_VSENSE OVDJ_ADJ CPU_CHKSTP_OUT_L CPU_CHKSTP_IN_L CPU_HRESET_L JTAG_CPU_TCK JTAG_CPU_TDI JTAG_CPU_TDO JTAG_CPU_TMS JTAG_CPU_TRST_L +MAXBUS_SLEEP ROM_CS_L ROM_OE_L ROM_RW_L DDC_VCC_3 DDC_VCC_5 SND_HP_SENSE_L ANALOG_HSYNC* ANALOG_VSYNC* FILT_ANALOG_BLU FILT_ANALOG_RED FILT_ANALOG_GRN GND KS_INT_SPKR+ KS_INT_SPKR- TMDS_D2P TMDS_D2M TMDS_D1P TMDS_D1M TMDS_D0P TMDS_D0M TMDS_CKP TMDS_CKM INV_CUR_HI_FILT IO_RESET_L KS5VSD INT_I2C_CLK2 INT_I2C_DATA2 INT_ANALYZER_CLK LAMP_STS_FILT LCD_PWM_FILT LED_5V_FILT LED_RET_FILT MICSHLD MICHIGH MICLOW COMM_RESET_L IIC_ADD ROM_WP_L	52C4 51C3< 51B4< 51B3< 51B2< 51B1< 45D7< 45D3< 45B4< 44D8< 42B3< 39C8< 36D2< 49D7< 49D3< 49C4< 48B6< 48C8< 48C4< 51D6< 51C2< 51A5< 50D5< 29C5< 29A8< 29A3< 52C1> 52C4 51B4<> 51C8< 51C5< 50D5< 46D6< 46C7< 38C1< 52C4 49B2<> 30B3< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 39D4< 52C4 43C7< 59B5> 52C6> 45D2<> 8C1< 8B7< 4D7< 4D3< 35C4< 34B7< 8A4<> 34B7< 28C6< 8A4<> 35B4<> 8A4<> 35B4<> 35A2< 34B7< 8A4<> 34B7< 8A4<> 52A6> 24C3<> 17A4< 17A3< 16D7< 16C2< 16A8< 11A6< 10D6< 52C3> 46B4<> 17D5< 52B3> 29A5<> 47B2<> 46B3< 11D3< 10D6< 47C6<> 8D5<> 8A3<> 7B5< 4B3> 7B5< 4B3> 44D2< 44C2< 8A3> 7B3< 7A5< 7A3< 4B3< 8A3<> 7D5< 4C3< 8A3<> 7A5< 4C3< 8A3<> 4C3> 8A3<> 7A5< 4C3< 8A3<> 7C5< 4C3< 8D1< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< 52C6> 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< 8D4< 31B4<> 30C6< 30B4< 31B2<> 30C6< 30B2< 31B4<> 30B6< 30B2< 52B6> 24B3<> 52A6> 25C4< 41A5< 28B5<> 57D5> 26B5< 25D6<> 22D7< 57D5> 26B5< 25C6<> 22D7< 57D5> 25C5< 57D5> 25C5< 57D5> 25C5< 58A5> 43D7< 29A3< 58A5> 43D7< 42B4< 29A3< 57D2> 27C2< 24D7<> 23D1< 57D2> 27C2< 24D7<> 23D1< 57D2> 27C2< 24C7<> 23D1< 57D2> 27C2< 24C7<> 23D1< 57D2> 27C2< 24B7<> 23D1< 57D2> 27C2< 24B7<> 23D1< 57D2> 27C2< 24A7<> 23D1< 29A5<> 44D3< 44B8<> 35B8< 32A6< 52B3> 29A5<> 39B1<> 34B5< 29C7<> 28D1< 28A3<> 39B1<> 34B5< 29C7<> 28D1< 28A3<> 56B3> 54A7< 16C7< 9B4< 8A2< 29A5<> 29A5<> 52B3> 29A5<> 52A3> 29A5<> 58A5> 43A8< 29A5<> 58A5> 43B8< 29A5<> 58A5> 43A8< 29A5<> 29D5<> 28C5<> 29C6<> 30B2<>

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25C6< 23D7<>	MON_DETECT	25C6< 23D7<>
45C8<> 45C7<>	FLO_KNOWS_BEST	45C8<> 45C7<>
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59D5> 44C5<> 44B1< 8A8<>	PWR_SWITCH*	59D5> 44C5<> 44B1< 8A8<>
44B5<> 44A5<> 29B3<> 8A8<>	PMU_RST*	44B5<> 44A5<> 29B3<> 8A8<>
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59D5> 44C5<> 44B1< 8A8<>	PWR_SWITCH*	59D5> 44C5<> 44B1< 8A8<>
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44C5<> 29C5<> 28B8< 28B5<>	COMM_RING_DET_L	44C5<> 29C5<> 28B8< 28B5<>
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29C7<> 28C3<>	COMM_DTR_L	29C7<> 28C3<>
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29C5<> 28D3< 28C3<>	SLEEP	29C5<> 28D3< 28C3<>
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24B3<>	TMDS_DDC_DAT	24B3<>
24B4<>	USB_DCN_CON	24B4<>
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58B5> 29D3<> 28B2<>	BT_USB_DM	58B5> 29D3<> 28B2<>
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40B7<> 40B6<>	LINE_IN_SENSE	40B7<> 40B6<>
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40D4< 28B5<>	OUT_R	40D4< 28B5<>
	LINEOUT_COMM2	
	LINE_OUT_L	
54C7< 31C3<> 31B6<	PCIT_IRDY_L	54C7< 31C3<> 31B6<
31C3<>	RF_CLKRUN_L	31C3<>
	NC_RF_DISABLE_L	
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54D7< 32B6<> 31B7< 30C5<> 30B7<	PCI_STOP_L	54D7< 32B6<> 31B7< 30C5<> 30B7<
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54D7< 32B6<> 31B7< 30C5<>	PCI_PAR	54D7< 32B6<> 31B7< 30C5<>
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31C2<> 28B7<>	PMU_PME_L	31C2<> 28B7<>
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31C3<> 30D5<> 30B7<		31C3<> 30D5<> 30B7<
44C4<> 32A8< 31D4< 30B2< 17C8<	MAIN_RESET_L	44C4<> 32A8< 31D4< 30B2< 17C8<
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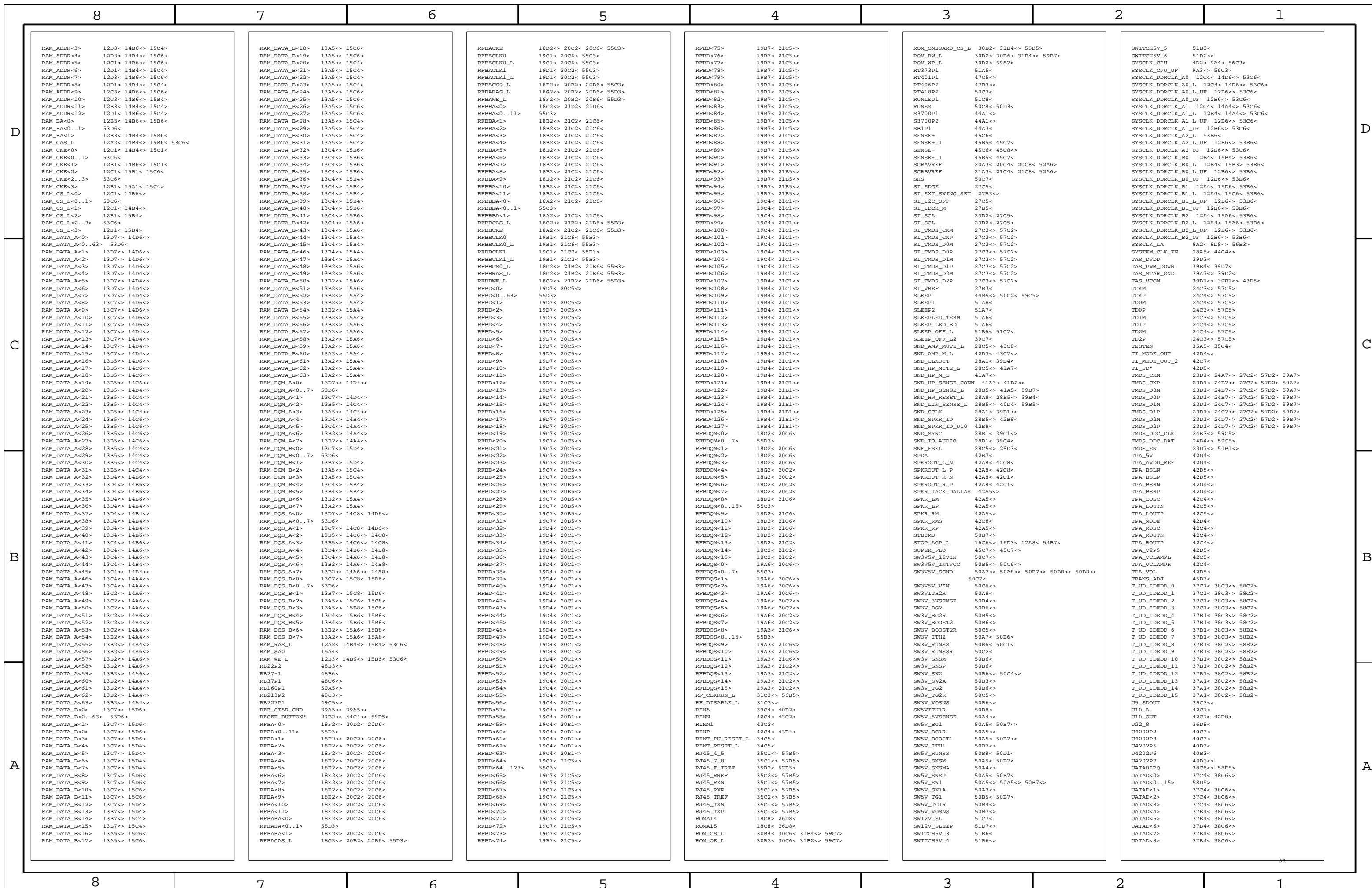
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CONSTRAINT TABLES

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	NONE	59	69



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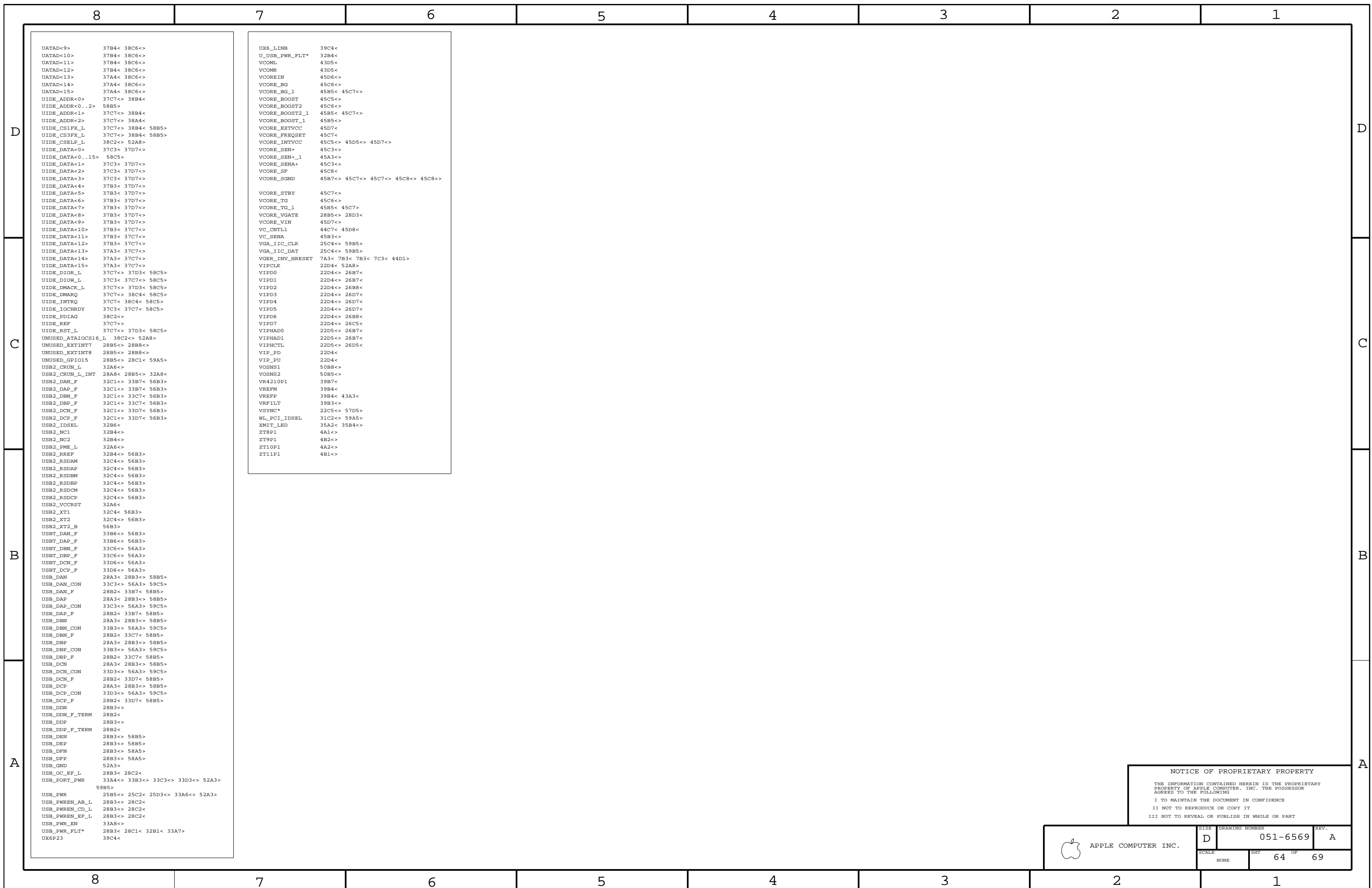
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SCALE	NONE	SHT	64 OF 69

	8	7	6	5	4	3	2	1
D	*** Part Cross-Reference for the entire design ***							
	BS1 PCR_STANDOFF 29B5 BS2 PCR_STANDOFF 29B6 BS3 PCR_STANDOFF 29D1 BS4 PCR_STANDOFF 29D1 BT1 BATTERY 44D6 C1 CAP 33C4 C2 CAP 33D4 C3 CAP 35B1 C4 CAP 36B6 C5 CAP_P 33A5 C6 CAP 33B4 C7 CAP_P 33A5 C8 CAP 21A4 C9 CAP 21A4 C10 CAP_P 36D7 C11 CAP 21A4 C12 CAP_P 36D7 C13 CAP_P 41C4 C14 CAP 12A7 C15 CAP 21D2 C16 CAP 21B4 C17 CAP 21D5 C18 CAP 51D3 C19 CAP_P 51D4 C20 CAP 21B2 C21 CAP 21D5 C22 CAP 21B4 C23 CAP 21B4 C24 CAP_P 40B4 C25 CAP_P 40C4 C26 CAP_P 41D4 C27 CAP 36D8 C28 CAP 21B1 C29 CAP 21B3 C30 CAP 12A6 C31 CAP 21B2 C32 CAP 21D4 C33 CAP 21B2 C34 CAP 21B3 C35 CAP 43B5 C36 CAP 42D7 C37 CAP 35D7 C38 CAP 21D2 C39 CAP 21D5 C40 CAP 21B3 C41 CAP 35D8 C42 CAP 36B8 C43 CAP 41D6 C44 CAP 35D4 C45 CAP 42B8 C46 CAP 14D8 C47 CAP 14D8 C48 CAP 15D8 C49 CAP 15D8 C50 CAP 15D7 C51 CAP 15C3 C52 CAP 35D4 C53 CAP 35D5 C54 CAP 18B8 C55 CAP 15C1 C56 CAP 35D4 C57 CAP 35D6 C58 CAP 15B1 C59 CAP_P 48B2 C60 CAP 41C6 C61 CAP 18B6 C62 CAP 18D6 C63 CAP 40B2 C64 CAP 40C2 C65 CAP 35D7 C66 CAP 35D7 C67 CAP 35D5 C68 CAP 35D6 C69 CAP 18B5 C70 CAP 18B6 C71 CAP_P 48B1 C72 CAP 18H7 C73 CAP 18H7 C74 CAP 35B7 C75 CAP 18H5 C76 CAP 35B7 C77 CAP 32D3 C78 CAP 18H6 C79 CAP 18H4 C80 CAP 18H2 C81 CAP 18H7 C82 CAP 18H4 C83 CAP 18H3 C84 CAP 18H8 C85 CAP_P 39C6 C86 CAP 18H8 C87 CAP 17B2 C88 CAP_P 48B1 C89 CAP 18H2 C90 CAP 18H7 C91 CAP 17B3 C92 CAP 34B6 C93 CAP 17C3 C94 CAP 17C3 C95 CAP 18H5 C96 CAP 18H2 C97 CAP 17B3 C98 CAP 18H6 C99 CAP 17D1 C100 CAP 17D3 C101 CAP 17D2 C102 CAP 17C2 C103 CAP 17D2	C104 CAP 17D4 C105 CAP 17B2 C106 CAP_P 48B2 C107 CAP 24B2 C108 CAP 42B7 C109 CAP 17D3 C110 CAP 17D2 C111 CAP 17B3 C112 CAP 17B2 C113 CAP 27D5 C114 CAP 32D3 C115 CAP 18H3 C116 CAP 17B3 C117 CAP 17D3 C118 CAP 17C3 C119 CAP 23B5 C120 CAP 17C3 C121 CAP 39C4 C122 CAP 42C8 C123 CAP 30C3 C124 CAP 18H1 C125 CAP 23B6 C126 CAP_P 39C7 C127 CAP_P 39B2 C128 CAP 22D3 C129 CAP 17B3 C130 CAP 23B6 C131 CAP 23B4 C132 CAP_P 48B2 C133 CAP 18H6 C134 CAP 17D3 C135 CAP 17C2 C136 CAP 17B3 C137 CAP 17B4 C138 CAP 46B4 C139 CAP 14C1 C140 CAP 17C2 C141 CAP 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38B2 DS8 LED 38B6 DS9 LED 50D5 DS10 LED 51A4 D21 ZENER 51B1 F2 FUSE 36D5 F3 FUSE 36D5 FL2 FILTER_IC 25C6 FL3 FILTER_IC 25C6 FL4 FILTER_IC 25B6 J1 CON_RJ45 35C1 J2 CON_FWVERT_SKT 36C1 J3 CON_F8RT_S_THI 42B5 J4 CON_F4RT_USB_UPRIGHT 33C3 J5 CON_FWVERT_SKT 36D1 J6 CON_F4RT_USB_UPRIGHT 33B3 J7 CON_F4RT_USB_UPRIGHT 33D3	J8 CON_F4RT_S4MT_THI 41C1 J9 CON_F14RT_D4MT_THI 25C5 J10 CON_F4RT_S4MT_THI 40C7 J11 CON_F184ST_DDRDIMM 15D5 J12 CON_F21ST_D2MT_SM 24C4 J13 CON_M40SM_635 29D6 J14 CON_M18ST_D_TH 29B5 J15 CON_M40ST_NC20 38D6 J16 CON_M40ST_NC20 38D2 J17 CON_M16ST_MICROFIT 50D7 J18 CON_M45T_LCK 34B4 J19 CON_37SM_MTOR 8C4 J20 CON_38SM_MTOR 8D7 J21 CON_M35T_LCK 45C8 J22 CON_F20SM_KX 8A4 J23 CON_F15T_S2MT_SM 28B7 J24 CON_M12ST_SM 29B3 J25 CON_F100RT_LP_SM 31D3 J26 CON_F200RT_DDRDIMM_SM2 14D5 J27 CON_F15T_S2MT_SM 8B1 J28 CON_F10ST_D_SMA 29D2 J30 CON_38SM_MTOR 8D4 J31 CON_38SM_MTOR 8C7 J32 CON_F12RT_S2MT_SM 8A8 J4501 CON_F45T_S2MT_SM 43B6 J4502 CON_F45T_S2MT_SM 43B6 JA21 TP 51A5 L1 IND 36D4 L2 IND 33A5 L3 IND 36D4 L4 IND 27D5 L5 FILTER_4P 36C2 L6 FILTER_4P 36C2 L7 FILTER_4P 36D2 L8 FILTER_4P 36D2 L9 IND 25C2 L12 IND 48B3 L13 IND 22D7 L16 IND 28C3 L19 IND 47B4 L20 IND 45C3 L21 IND_3P 49B3 L22 IND_3P 50A3 L23 IND 50C3 L24 IND 45B3 L26 IND 42A6 L27 IND 41C3 L32 IND 36B6 L33 IND 22B7 L34 IND 41D3 L35 IND 41B3 L36 IND 40B6 L39 IND 41A3 L40 IND 42A5 L41 IND 42B7 L42 IND 41B3 L43 IND 41A4 L44 IND 41C3 L45 IND 41D3 L46 IND 40C6 L47 IND 41B3 L48 IND 40C6 L49 IND 40B5 L50 IND 40C5 L51 IND 40D6 L52 IND 40C5 L53 IND 40D5 L56 IND 44A1 L57 IND 44A1 L58 IND 32D6 L59 IND 43A5 L60 IND 43B5 L63 IND 39D4 L64 IND 24A5 L65 IND 29A7 L66 IND 29A3 L67 FILTER_4P 24B5 L68 IND 22D2 L69 IND 29A3 L70 IND 29A7 L71 FILTER_4P 24B5 L72 IND 29A7 L73 IND 29A3 L74 FILTER_4P 24C5 L75 IND 29A7 L76 FILTER_4P 24D5 L77 IND 29B7 L78 IND 29A3 L79 IND 43B7 L80 IND 29B3 L81 IND 43A7 L82 IND 24D5 L83 IND 43A7 L84 IND 50D6 L85 IND 50D6 L86 IND 50D6 L87 IND 27D5 L88 IND 27D2 L89 IND 42D7 L90 IND 42C6 L91 IND 42C6 L92 IND 42C7 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D	L101 FILTER_4P 33C5 L102 FILTER_4P 33B5 L103 IND 29B3 L2401 IND 22C7 L2501 IND 23A6 LP1 LPAK4P 42A8 Q1 TRA_2N7002 51C3 Q2 TRA_2N7002 42D7 Q3 TRA_2N7002 42C7 Q4 TRA_2N7002 42B8 Q5 TRA_2N7002 41A5 Q6 TRA_2N7002 42B6 Q7 TRA_SUD70N03 48B4 Q8 TRA_SUD50N03 48B4 Q9 TRA_SUD50N03 48C4 Q10 TRA_2N7002 22B7 Q11 TRA_FDC602P 51C2 Q12 TRA_2N3904 44D7 Q13 TRA_2N7002 51B2 Q14 TRA_2N7002 51C7 Q15 TRA_2N7002 51A7 Q16 TRA_2N7002 51A7 Q17 TRA_2N7002 51B6 Q18 TRA_2N7002 51A7 Q19 TRA_2N7002 51A6 Q20 TRA_FDC602P 51D7 Q21 TRA_2N7002 50C1 Q22 TRA_2N7002 50D1 Q23 TRA_2N7002 50C2 Q24 TRA_2N7002 50C2 Q25 TRA_IRF7807Z 47B5 Q26 TRA_IRF7807Z 47B5 Q27 TRA_SUD70N03 49B4 Q28 TRA_SUD50N03 49B4 Q29 TRA_2N7002 45D8 Q30 TRA_2N3904 36C7 Q31 TRA_2N7002 41A8 Q32 TRA_2N7002 39C7 Q33 TRA_2N3904 43A2 Q34 TRA_SUD70N03 48B4 Q35 TRA_2N7002 40D4 Q36 TRA_2N7002 42D3 Q37 TRA_FDC602P 51C6 Q38 TRA_2N7002 51B6 Q39 TRA_2N3904 50C7 Q40 TRA_SUD70N03 45C4 Q41 TRA_2N7002 15B2 Q42 TRA_2N7002 15C2 Q43 TRA_SUD70N03 45C4 Q44 TRA_SUD50N03 45C4 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 ZT66 HOLE_VIA 3B1
 ZT67 HOLE_VIA 3B1
 ZT68 HOLE_VIA 3A1

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