1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
01		279015	ENGINEERING RELEASED	06/06/03	?

Dec 09 14:27:01 2003

Q59 MLB CONFIG "C"

TABLE OF CONTENTS

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+2_5V_MAIN	ON	ON	OFF
+3V_MAIN	ON	ON	OFF
+5V_MAIN	ON	ON	OFF
+5V_SLEEP	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12V_SLEEP	ON	OFF	OFF
FW_PWR	ON	ON	OFF
+1.8V_SLEEP	ON	OFF	OFF
+MAXBUS_SLEEP	ON	OFF	OFF

SCHEMATIC AND PCB SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6569	1	SCHEM,MLB,Q59	SCH1	CRITICAL	
820-1599	1	PCB,MLB,IMACG4.A,B,C	PCB1	CRITICAL	
825-2029	1	LBL,SER #,BARCODE	PCB1		
056-1158	1	DESIGN GUIDE,MCO,IMACG4	PCB1	CRITICAL	
057-0085	1	DFM,PNLZN DWG,MLB,Q59	PCB1	CRITICAL	
630-XXXX	1	630-XXXX,PCBA,H,Q59,EEE XXX HYNIX			OMIT
630-XXXX	1	630-XXXX,PCBA,S,Q59,EEE XXX SAMSUNG			OMIT

PCB,UL RECOGNIZED, MIN.130 DEG. C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94. PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, TEMPERATURE RATING AND FLAME RATING.

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

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TITLE: SCHEMATIC,MLB,Q59C
DRAWING NUMBER 051-6569 REV. A
SHT 1 OF 69
DRAWING

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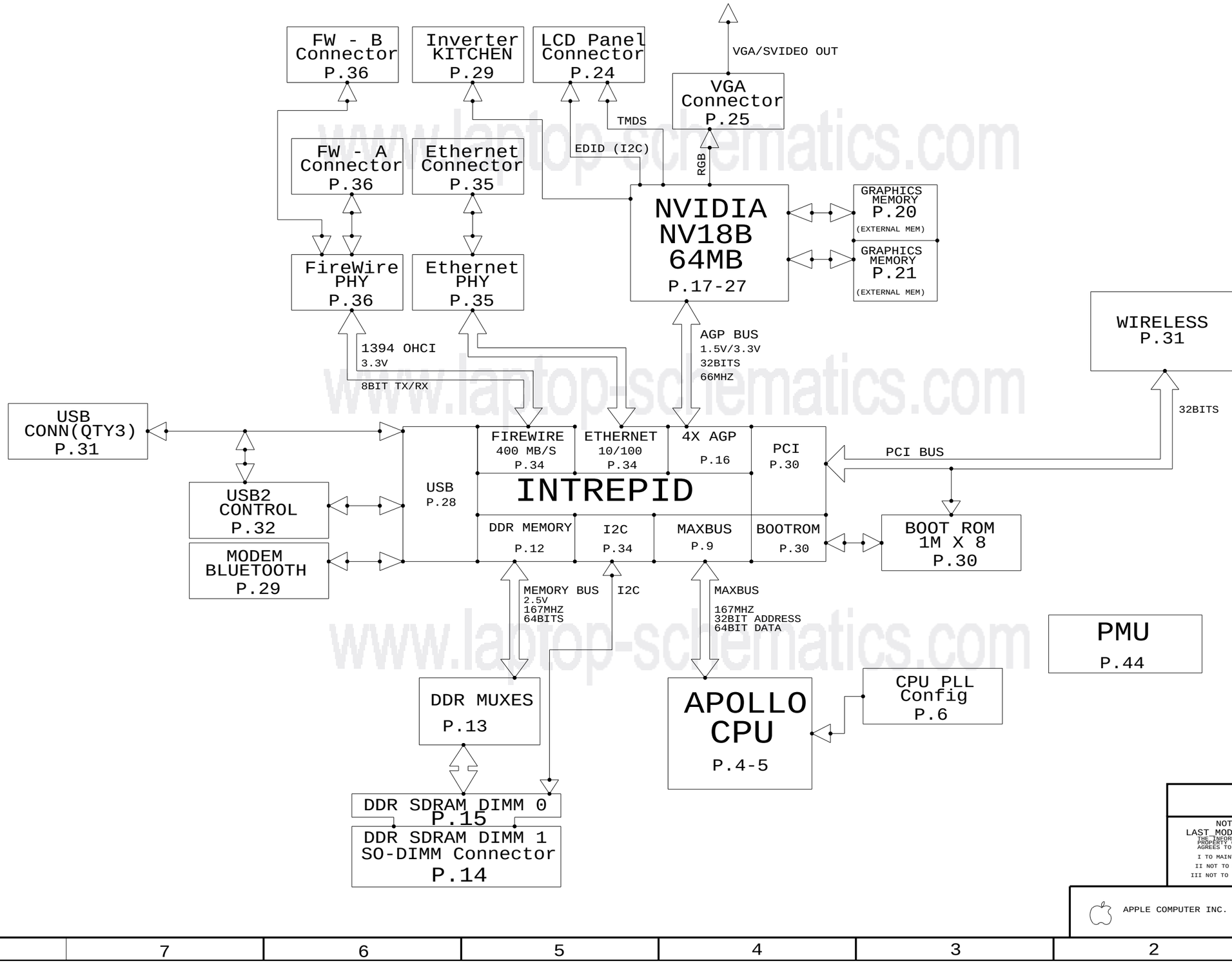

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SYSTEM BLOCK

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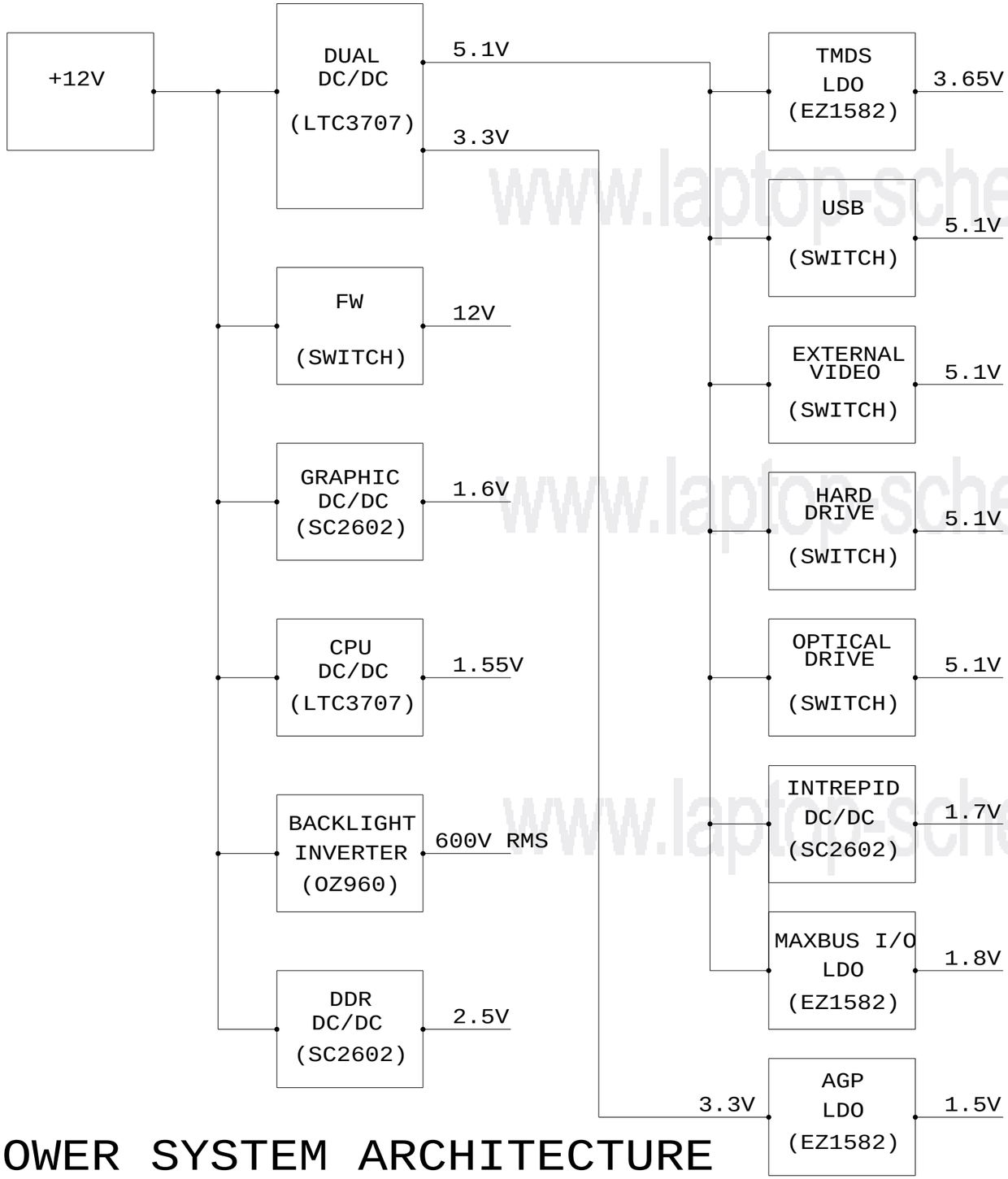
SIZE	DRAWING NUMBER	REV.
D	051-6569	A

SCALE	SHT	OF
NONE	2	69

DRAWING



LAYER	THICKNESS (MILS)	COPPER (OZ)	TRACE WIDTH (MILS)
1 - SIGNAL-TOP	0.7	0.5	4
PREPREG	3	---	
2 - GROUND1	1.4	1	---
PREPREG	3	---	
3 - SIGNAL	0.7	0.5	4
FILLER	17.4	---	
4 - POWER	2.8	2	---
PREPREG	4	---	
5 - POWER	2.8	2	---
FILLER	17.4	---	
6 - SIGNAL	0.7	0.5	4
PREPREG	3	---	
7 - GROUND2	1.4	1	---
PREPREG	3	---	
8 - SIGNAL-BOTTOM	0.7	0.5	4
TOTAL	62.0	---	---

OMIT ZT39 HOLE-VIA-20R10
OMIT ZT46 HOLE-VIA-20R10
OMIT ZT53 HOLE-VIA-20R10
OMIT ZT59 HOLE-VIA-20R10
OMIT ZT64 HOLE-VIA-20R10
OMIT ZT40 HOLE-VIA-20R10
OMIT ZT47 HOLE-VIA-20R10
OMIT ZT54 HOLE-VIA-20R10
OMIT ZT60 HOLE-VIA-20R10
OMIT ZT65 HOLE-VIA-20R10
OMIT ZT41 HOLE-VIA-20R10
OMIT ZT48 HOLE-VIA-20R10
OMIT ZT55 HOLE-VIA-20R10
OMIT ZT61 HOLE-VIA-20R10
OMIT ZT66 HOLE-VIA-20R10
OMIT ZT42 HOLE-VIA-20R10
OMIT ZT49 HOLE-VIA-20R10
OMIT ZT56 HOLE-VIA-20R10
OMIT ZT62 HOLE-VIA-20R10
OMIT ZT67 HOLE-VIA-20R10
OMIT ZT43 HOLE-VIA-20R10
OMIT ZT50 HOLE-VIA-20R10
OMIT ZT57 HOLE-VIA-20R10
OMIT ZT63 HOLE-VIA-20R10
OMIT ZT68 HOLE-VIA-20R10
OMIT ZT44 HOLE-VIA-20R10
OMIT ZT51 HOLE-VIA-20R10
OMIT ZT58 HOLE-VIA-20R10
OMIT ZT45 HOLE-VIA-20R10
OMIT ZT52 HOLE-VIA-20R10

POWER SYSTEM ARCHITECTURE

PWR BLOCK,PCB INFO

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A

SCALE: NONE | SHT 3 OF 69

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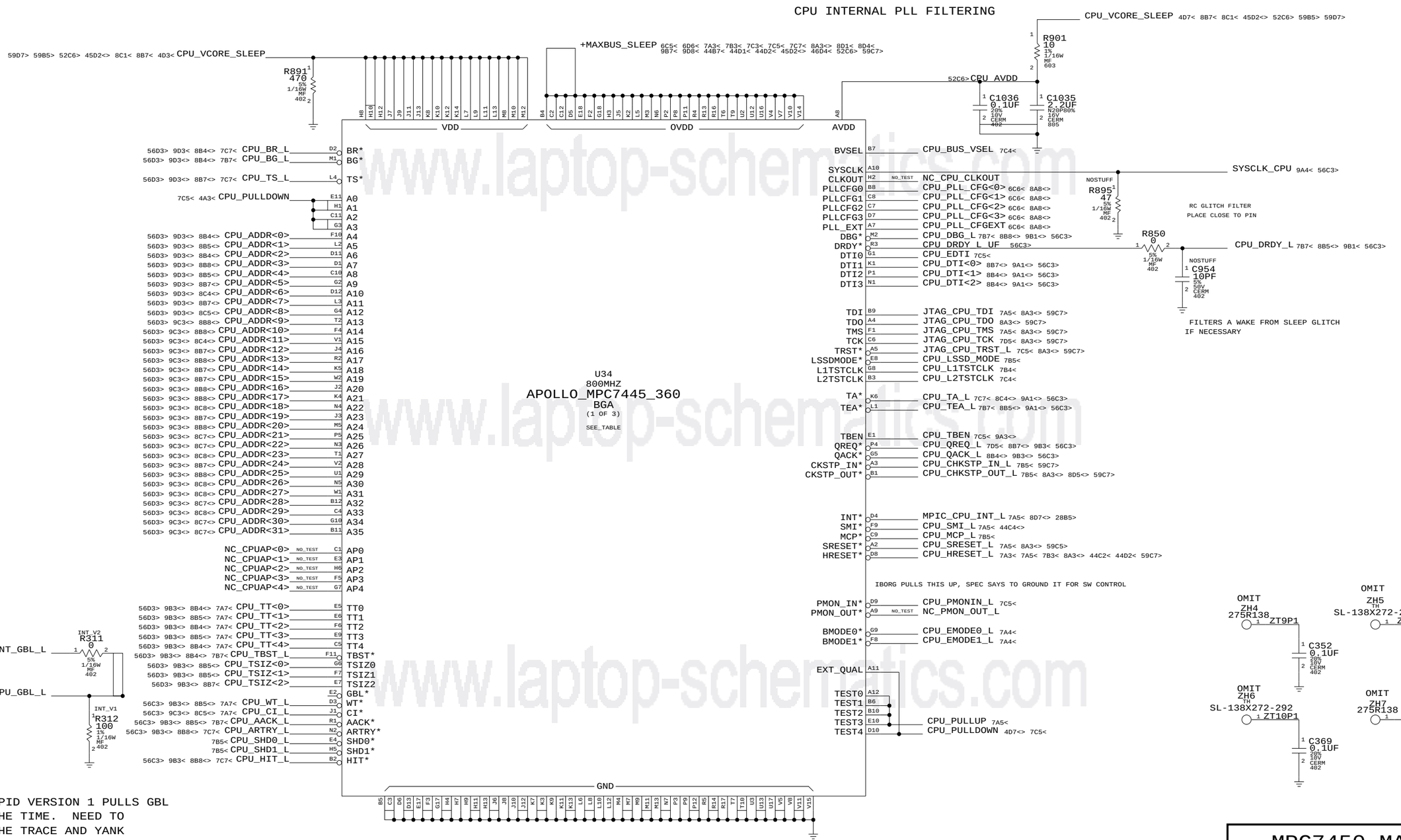
CPU INTERNAL PLL FILTERING



INTREPID VERSION 1 PULLS GBL
ALL THE TIME. NEED TO
CUT THE TRACE AND YANK
DOWN HARD FOR SNOOPING.
FIXED IN INTREPID VERSION 2.

CPU MECHANICAL PARTS SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
875-1475	1	PAD,THERMAL,CPU,U34	U341	?	
870-1113	1	HEAT SINK,CPU,Q26,U34	U342	?	DEV
870-1114	1	CLIP,HEAT SINK,CPU,Q26.U34	U343	?	DEV
412-0042	1	SCREW,MACH,3MM W,8MM L,U34	U344	?	DEV
835-0251	1	NUT,3MM,U34	U345	?	DEV

MPC7450 MAXBUS

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 4 OF 69	

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APOLLO_MPC7445_360

U34
800MHZ
BGA
(3 OF 3)

NC_CPUCRUD<0>	NO_TEST	F18	NC_F18
NC_CPUCRUD<1>	NO_TEST	F17	NC_F17
NC_CPUCRUD<2>	NO_TEST	F19	NC_F19
NC_CPUCRUD<3>	NO_TEST	H19	NC_H19
NC_CPUCRUD<4>	NO_TEST	H18	NC_H18
NC_CPUCRUD<5>	NO_TEST	H17	NC_H17
NC_CPUCRUD<6>	NO_TEST	H16	NC_H16
NC_CPUCRUD<7>	NO_TEST	E19	NC_E19
NC_CPUCRUD<8>	NO_TEST	D18	NC_D18
NC_CPUCRUD<9>	NO_TEST	F16	NC_F16
NC_CPUCRUD<10>	NO_TEST	G16	NC_G16
NC_CPUCRUD<11>	NO_TEST	D19	NC_D19
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NC_CPUCRUD<50>	NO_TEST	D15	NC_D15
NC_CPUCRUD<51>	NO_TEST	G15	NC_G15
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NC_CPUCRUD<53>	NO_TEST	A16	NC_A16
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APOLLO_MPC7445_360

U34
800MHZ
BGA
(2 OF 3)

56D3> 9D1<> 8C4<>	CPU_DATA<0>	R15	D0
56D3> 9D1<> 8C7<>	CPU_DATA<1>	W15	D1
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NC_CPUDP<2>	NO_TEST	T4	DP2
NC_CPUDP<3>	NO_TEST	W9	DP3
NC_CPUDP<4>	NO_TEST	M6	DP4
NC_CPUDP<5>	NO_TEST	V3	DP5
NC_CPUDP<6>	NO_TEST	N8	DP6
NC_CPUDP<7>	NO_TEST	W6	DP7

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 5 OF 69	

DRAWING

BOMOPTIONS FOR UPPER-SET OF RESISTORS

1200@133&1500@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

667@133&833@167&733@133&917@167&800@133&1000@167&1067@133&1333@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1867@133&2333@167&2133@133&2667@167

800@133&1000@167&867@133&1083@167&1067@133&1333@167&1200@133&1500@167&1733@133&2167@167&1867@133&2333@167&2133@133&2667@167

667@133&833@167&933@133&1167@167&1200@133&1500@167&1333@133&1667@167&1600@133&2000@167

667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1200@133&1500@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&2000@133&2500@167&2133@133&2667@167

+MAXBUS_SLEEP 4D5< 6C5< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C7>

SPECIAL CONFIG
R382 10K 1% 1/16W MF 402
R379 10K 1% 1/16W MF 402
R378 10K 1% 1/16W MF 402
R376 10K 1% 1/16W MF 402
R374 10K 1% 1/16W MF 402

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CPU_PLL_CFG<2> 4D3< 8A8<>
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CPU_PLL_CFG<0> 4D3< 8A8<>

SPECIAL CONFIG
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R381 1K 1% 1/16W MF 402
R380 1K 1% 1/16W MF 402
R377 1K 1% 1/16W MF 402
R375 1K 1% 1/16W MF 402

CPU_PLL_STOP 44B8<

NOSTUFF
R879 10K 1% 1/16W MF 402
R878 10K 1% 1/16W MF 402
R889 10K 1% 1/16W MF 402
R866 10K 1% 1/16W MF 402
R874 10K 1% 1/16W MF 402
R877 10K 1% 1/16W MF 402
R875 10K 1% 1/16W MF 402
R867 10K 1% 1/16W MF 402

8D1< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 4D5< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< 8D4< 59C7> 52C6> +MAXBUS_SLEEP

NOSTUFF

667@133&733@133&800@133&867@133&933@133&1000@133&1067@133&1200@133&1333@133&1467@133&1600@133&1733@133&1867@133&2000@133&2133@133

NOSTUFF

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CPU_DATA<45> 5B4<> 8C7<> 9B1<> 56D3>
CPU_DATA<46> 5B4<> 8C4<> 9B1<> 56D3>
CPU_DATA<47> 5B4<> 8C7< 9B1<> 56D3>

R363 4.7K 5% 1/16W MF 402
R364 4.7K 5% 1/16W MF 402
R887 4.7K 5% 1/16W MF 402
R357 4.7K 5% 1/16W MF 402
R368 4.7K 5% 1/16W MF 402
R365 4.7K 5% 1/16W MF 402
R367 4.7K 5% 1/16W MF 402
R356 4.7K 5% 1/16W MF 402

INTREPID BOOT STRAPS
BITS 40 - 47

SPARE
SPARE
PLL4MODESEL_NXT[2:0]
000: 166.4 MHZ
001: 149.76 MHZ
010: 133.12 MHZ
011: 99.84 MHZ
100: 83.20 MHZ
INTERNALSPREADEN 1:: INTERNAL SPREAD ACTIVE
PCI1 SOURCE CLOCK 0:: PLL4 1:: PLL5 (NO SPREAD)
PCI0 SOURCE CLOCK 0:: PLL4 1:: PLL5 (NO SPREAD)

(STUFF FOR 133 AND 167)

833@167&917@167&1000@167&1083@167&1167@167&1250@167&1333@167&1500@167&1667@167&1833@167&2000@167&2167@167&2333@167&2500@167&2667@167

(STUFF FOR 133 AND 167)

933@133&1167@167&1067@133&1333@167&1333@133&1667@167&1867@133&2333@167

733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1067@133&1333@167&1467@133&1833@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

667@133&833@167&733@133&917@167&933@133&1167@167&1000@133&1250@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&2000@133&2500@167

867@133&1083@167&933@133&1167@167&1000@133&1250@167&1200@133&1500@167&1733@133&2167@167&2000@133&2500@167

667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&933@133&1167@167&1000@133&1250@167&1067@133&1333@167

CPU FREQUENCY CONFIGURATION
(SUPPORTED CPU & BUS SPEEDS)

MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ	133MHZ	CPU_PLL_CFG E	0123 HEX
(BUS-TO-CORE)	(MHZ)			
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
9.0X	1500	1200	1	0111 17
10.0X	1667	1333	1	1010 1A
11.0X	1833	1467	1	1001 19
12.0X	2000	1600	1	1011 1B
13.0X	2167	1733	1	0101 15
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D

CPU SPEED & BUS RATIO SUPPORT

THE CONFIGURATION RESISTORS BELOW ARE SELF CONFIGURING WHEN THE ENGINEER SELECTS THE APPROPRIATE CPU AND BUS SPEED BOM OPTION, THE APPROPRIATE RESISTORS ARE ARE AUTOMATICALLY SELECTED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S2799	1	IC,APOLLO6,SICOH,1.0GHZ,1.5V+30/-130MV,28W,85C	U34	CRITICAL	1000@167
337S2801	1	IC,APOLLO6,SICOH,1.25GHZ,1.57V+70/-70MV,35W,85C	U34	CRITICAL	1250@167

CPU BUS RATIO BITS

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BMODE <0>	BMODE <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L	L	1 1	???	01	yes unavail
L	!hr	1 0	Max	01	yes unavail
L	hr	1 1	???	00	yes unavail
L	H	1 0	Max	00	yes unavail
!hr	L	0 1	MB+	01	yes unavail
!hr	!hr	0 0	60x	01	yes unavail
!hr	hr	0 1	MB+	00	yes unavail
!hr	H	0 0	60x	00	yes unavail
hr	L	1 1	???	01	norm unavail
hr	!hr	1 0	Max	01	norm
hr	hr	1 1	???	00	norm unavail
HR	H	1 0	MAX	00	NORM <- DEFAULT
H	L	0 1	MB+	01	norm unavail
H	!hr	0 0	60x	01	norm
H	hr	0 1	MB+	00	norm unavail
H	H	0 0	60x	00	norm

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE
CPU_L3_VSEL	CPU_HRESET_L or L3_OVDD	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE

MAXBUS PULL-UPS

59C7> 52C6> 8D1< 8A3<> 7C5< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< 8D4< +MAXBUS_SLEEP

- 56D3> 9D3<> 8B7<> 4D7<> CPU_TS_L — R347 10K 1% 1/16W MF 402
- 56C3> 9A1<> 8C4<> 4C3< CPU_TA_L — R348 10K 1% 1/16W MF 402
- 56C3> 9B3<> 8B8<> 4A7<> CPU_ARTRY_L — R346 10K 1% 1/16W MF 402
- 56D3> 9D3< 8B4<> 4D7> CPU_BR_L — R841 10K 1% 1/16W MF 402
- 56C3> 9B3< 8B8<> 4A7> CPU_HIT_L — R840 10K 1% 1/16W MF 402
- 56C3> 9B1< 8B5<> 4C2< CPU_DRDY_L — R851 10K 1% 1/16W MF 402
- 56C3> 9A1<> 8B5<> 4C3< CPU_TEA_L — R845 10K 1% 1/16W MF 402
- 56C3> 9B3<> 8B5<> 4A7< CPU_AACK_L — R849 10K 1% 1/16W MF 402
- 56C3> 9B1<> 8B8<> 4C3< CPU_DBG_L — R847 10K 1% 1/16W MF 402
- 56D3> 9D3<> 8B4<> 4D7< CPU_BG_L — R846 10K 1% 1/16W MF 402
- 56D3> 9B3<> 8B4<> 4B7> CPU_TBST_L — R349 10K 1% 1/16W MF 402
- 56C3> 9C3<> 4B8< CPU_INT_GBL_L — R842 10K 1% 1/16W MF 402
- 56C3> 9C3<> 8C5<> 4A7> CPU_CI_L — R844 10K 1% 1/16W MF 402
- 56C3> 9B3<> 8B5<> 4B7> CPU_WT_L — RP78 10K 5% 1/16W SM1 (2-7)
- 56D3> 9B3<> 8B4<> 4B7<> CPU_TT<0> — RP78 10K 5% 1/16W SM1 (1-8)
- 56D3> 9B3<> 8B5<> 4B7<> CPU_TT<1> — RP78 10K 5% 1/16W SM1 (3-6)
- 56D3> 9B3<> 8B4<> 4B7<> CPU_TT<2> — R843 10K 1% 1/16W MF 402
- 56D3> 9B3<> 8B5<> 4B7<> CPU_TT<3> — RP78 10K 5% 1/16W SM1 (4-5)
- 56D3> 9B3<> 8B4<> 4B7<> CPU_TT<4> — R350 10K 1% 1/16W MF 402

- 56C3> 9B3< 8B7<> 4C3> CPU_QREQ_L — R848 10K 1% 1/16W MF 402
- 59C7> 8A3<> 4C3< JTAG_CPU_TCK — R924 10K 1% 1/16W MF 402
- 59C7> 8A3<> 4C3< JTAG_CPU_TRST_L — R925 200 5% 1/16W MF 402
- 4B3< CPU_PMONIN_L — RP79 10K 5% 1/16W SM1 (4-5)
- 4C3< CPU_EDTI — R858 10K 1% 1/16W MF 402
- 4D7<> 4A3< CPU_PULLDOWN — R859 470 5% 1/16W MF 402

MPC7450 PULL-UPS

59C7> 8D4< 8D1< 8A3<> 7C7< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< 52C6> 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< +MAXBUS_SLEEP

- 9A3<> 4C3< CPU_TBEN — R856 10K 1% 1/16W MF 402
- 4A7<> CPU_SHD0_L — R857 10K 1% 1/16W MF 402
- 4A7<> CPU_SHD1_L — R860 10K 1% 1/16W MF 402
- 4B3< CPU_MCP_L — R910 10K 1% 1/16W MF 402
- 4C3< CPU_LSSD_MODE — R911 10K 1% 1/16W MF 402
- 59C7> 8D5<> 8A3<> 4B3> CPU_CHKSTP_OUT_L — NOSTUFF R921 1K 1% 1/16W MF 402
- 59C7> 4B3< CPU_CHKSTP_IN_L — R882 1K 1% 1/16W MF 402
- 4A3< CPU_PULLUP — R909 1K 1% 1/16W MF 402
- 59C7> 44D2< 44C2< 8A3<> 7B3< 7A3< 4B3< CPU_HRESET_L — R922 10K 1% 1/16W MF 402
- 59C5> 8A3<> 4B3< CPU_SRESET_L — RP79 10K 5% 1/16W SM1 (2-7)
- 28B5> 8D7<> 4B3< MPIC_CPU_INT_L — RP79 10K 5% 1/16W SM1 (3-6)
- 44C4<> 4B3< CPU_SMI_L — R912 10K 1% 1/16W MF 402
- 59C7> 8A3<> 4C3< JTAG_CPU_TDI — RP79 10K 5% 1/16W SM1 (1-8)
- 59C7> 8A3<> 4C3< JTAG_CPU_TMS — R923 10K 1% 1/16W MF 402

NOSTUFF R915 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 44D1>

NOSTUFF R913 10K 5% 1/16W MF 402 — +MAXBUS_SLEEP 59C7> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>

4D3< CPU_BUS_VSEL — R914 200 5% 1/16W MF 402

BUS MODE

0V	1.8V BUS MODE
INV_HRESET	1.5V BUS MODE
OVDD	2.5V BUS MODE

4C3< CPU_L2TSTCLK — R918 10K 1% 1/16W MF 402 — +MAXBUS_SLEEP 59C7> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>

NOSTUFF R926 0 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C7>

NOSTUFF R919 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 7C3< 44D1>

NOSTUFF R920 200 5% 1/16W MF 402

DO NOT USE UNLESS FIX INVERTER BUFFER

NOSTUFF R907 10K 5% 1/16W MF 402 — +MAXBUS_SLEEP 4D5< 6C5< 6D6< 7A3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C7>

NOSTUFF R906 0 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C7>

NOSTUFF R916 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 7C3< 44D1>

4C3< CPU_L1TSTCLK — R917 200 5% 1/16W MF 402

CPUBUS_60X R904 1K 5% 1/16W MF 402 — +MAXBUS_SLEEP 59C7> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>

4B3< CPU_EMODE0_L — CPUBUS_MAX R905 200 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C7>

R903 1K 1% 1/16W MF 402 — +MAXBUS_SLEEP 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C7>

4B3< CPU_EMODE1_L — NOSTUFF R902 200 5% 1/16W MF 402 — VGER_INV_HRESET 7B3< 7C3< 44D1>

CPU CONFIG OPTIONS

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<XR_PAGE_TITLE>

MAXBUS LOGIC ANALYZER SUPPORT

NOTE: INTREPID MAXBUS CONFIG STRAPS MUST DROP
TO 1K OR LOGIC ANALYZER MAY AFFECT STRAP VALUES

J20
CON_38SM_MICTOR
SM
OMIT
EPROBE SYM_VER3

	GND	1	2	GND	
	GND	2	1	GND	
56B3> 8A2< SYSCLK_LA	CLK3	3	36	Q1	MPIC_CPU_INT_L 4B3< 7A5< 28B5>
56D3> 9C1< 9B7< 5C4< CPU_DATA<34>	C3_7	4	35	C1_7	CPU_DATA<35> 5C4<> 9B7< 9C1<> 56D3>
56D3> 9B1<> 5B4<> CPU_DATA<56>	C3_6	5	34	C1_6	CPU_DATA<54> 5B4<> 9B1<> 9C8< 56D3>
56D3> 9D5< 9B1<> 5B4<> CPU_DATA<59>	C3_5	6	33	C1_5	CPU_DATA<32> 5C4<> 9B7< 9C1<> 56D3>
56D3> 9C1<> 9B7< 5C4<> CPU_DATA<33>	C3_4	7	32	C1_4	CPU_DATA<40> 5B4<> 6C4< 9C1<> 56D3>
56D3> 9D5< 9B1<> 5B4<> CPU_DATA<60>	C3_3	8	31	C1_3	CPU_DATA<31> 5C4<> 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<28>	C3_2	9	30	C1_2	CPU_DATA<25> 5C4<> 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<29>	C3_1	10	29	C1_1	CPU_DATA<27> 5C4<> 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<23>	C3_0	11	28	C1_0	CPU_DATA<22> 5C4<> 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<21>	C2_7	12	27	C0_7	CPU_DATA<17> 5C4<> 9C1<> 56D3>
56D3> 9D1<> 5C4<> CPU_DATA<14>	C2_6	13	26	C0_6	CPU_DATA<10> 5D4<> 9D1<> 56D3>
56D3> 9D8< 9B1<> 5B4<> CPU_DATA<50>	C2_5	14	25	C0_5	CPU_DATA<13> 5C4<> 9D1<> 56D3>
56D3> 9D1<> 5C4<> CPU_DATA<2>	C2_4	15	24	C0_4	CPU_DATA<1> 5D4<> 9D1<> 56D3>
56D3> 9D1<> 5D4<> CPU_DATA<5>	C2_3	16	23	C0_3	CPU_DATA<4> 5D4<> 9D1<> 56D3>
56D3> 9D8< 9B1<> 5B4<> CPU_DATA<51>	C2_2	17	22	C0_2	CPU_DATA<53> 5B4<> 9B1<> 9C8< 56D3>
56D3> 9D1<> 5D4<> CPU_DATA<7>	C2_1	18	21	C0_1	CPU_DATA<47> 5B4<> 6C4< 9B1<> 56D3>
56D3> 9B1<> 6C4< 5B4<> CPU_DATA<44>	C2_0	19	20	C0_0	CPU_DATA<45> 5B4<> 6C4< 9B1<> 56D3>
	GND			GND	
		39	40 41 42 43 44 45		

J31
CON_38SM_MICTOR
SM
OMIT
APROBE SYM_VER3

	GND	1	2	GND	
	GND	2	1	GND	
	CLK0	3	36	CLK1	
56D3> 9C3<> 4B7<> CPU_ADDR<26>	A3_7	4	35	A1_7	CPU_ADDR<30> 4B7<> 9C3<> 56D3>
56D3> 9C3<> 4B7<> CPU_ADDR<29>	A3_6	5	34	A1_6	CPU_ADDR<31> 4B7<> 9C3<> 56D3>
56D3> 9C3<> 4B7<> CPU_ADDR<27>	A3_5	6	33	A1_5	CPU_ADDR<28> 4B7<> 9C3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<18>	A3_4	7	32	A1_4	CPU_ADDR<22> 4C7<> 9C3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<23>	A3_3	8	31	A1_3	CPU_ADDR<21> 4C7<> 9C3<> 56D3>
56D3> 9C3<> 4B7<> CPU_ADDR<25>	A3_2	9	30	A1_2	CPU_ADDR<24> 4B7<> 9C3<> 56D3>
56C3> 9B1<> 7B7< 4C3< CPU_DBG_L	A3_1	10	29	A1_1	CPU_TS_L 4D7<> 7C7< 9D3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<17>	A3_0	11	28	A1_0	CPU_ADDR<15> 4C7<> 9C3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<20>	A2_7	12	27	A0_7	CPU_ADDR<19> 4C7<> 9C3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<16>	A2_6	13	26	A0_6	CPU_ADDR<14> 4C7<> 9C3<> 56D3>
56C3> 9B3<> 7C7< 4A7> CPU_ARTRY_L	A2_5	14	25	A0_5	CPU_DTI<0> 4C3< 9A1<> 56C3>
56D3> 9C3<> 4C7<> CPU_ADDR<10>	A2_4	15	24	A0_4	CPU_ADDR<7> 4C7<> 9D3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<13>	A2_3	16	23	A0_3	CPU_ADDR<12> 4C7<> 9C3<> 56D3>
56C3> 9B3< 7C7< 4A7> CPU_HIT_L	A2_2	17	22	A0_2	CPU_QREQ_L 4C3> 7D5< 9B3< 56C3>
56D3> 9D3<> 4C7<> CPU_ADDR<3>	A2_1	18	21	A0_1	CPU_TSIZ<2> 4B7> 9B3<> 56D3>
56D3> 9C3<> 4C7<> CPU_ADDR<9>	A2_0	19	20	A0_0	CPU_ADDR<5> 4C7<> 9D3<> 56D3>
	GND			GND	
		39	40 41 42 43 44 45		

(519-0698)

J30
CON_38SM_MICTOR
SM
OMIT
EPROBE SYM_VER3

	GND	1	2	GND	
	GND	2	1	GND	
59C7> 8A3<> 7B5< 4B3> CPU_CHKSTP_OUT_L	Q3	3	36	Q2	
56D3> 9C1<> 5B4<> CPU_DATA<37>	E3_7	4	35	E1_7	CPU_DATA<58> 5B4<> 9B1<> 9D5< 56D3>
56D3> 9C1<> 5B4<> CPU_DATA<39>	E3_6	5	34	E1_6	CPU_DATA<36> 5C4<> 9A7< 9C1<> 56D3>
56D3> 9C1<> 5B4<> CPU_DATA<38>	E3_5	6	33	E1_5	CPU_DATA<62> 5B4<> 9B1<> 9C5< 56D3>
56D3> 9C5< 9B1<> 5A4<> CPU_DATA<63>	E3_4	7	32	E1_4	CPU_DATA<61> 5B4<> 9B1<> 9C5< 56D3>
56D3> 9D5< 9B1<> 5B4<> CPU_DATA<57>	E3_3	8	31	E1_3	CPU_DATA<24> 5C4<> 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<30>	E3_2	9	30	E1_2	CPU_DATA<41> 5B4<> 6C4< 9C1<> 56D3>
56D3> 9C1<> 5C4<> CPU_DATA<26>	E3_1	10	29	E1_1	CPU_DATA<9> 5D4<> 9D1<> 56D3>
56D3> 9D1<> 5D4<> CPU_DATA<8>	E3_0	11	28	E1_0	CPU_DATA<19> 5C4<> 9C1<> 56D3>
56D3> 9D1<> 5C4<> CPU_DATA<15>	E2_7	12	27	E0_7	CPU_DATA<20> 5C4<> 9C1<> 56D3>
56D3> 9C8< 9B1<> 5B4<> CPU_DATA<55>	E2_6	13	26	E0_6	CPU_DATA<16> 5C4<> 9C1<> 56D3>
56D3> 9D1<> 5C4<> CPU_DATA<11>	E2_5	14	25	E0_5	CPU_DATA<18> 5C4<> 9C1<> 56D3>
56D3> 9D1<> 5D4<> CPU_DATA<3>	E2_4	15	24	E0_4	CPU_DATA<49> 5B4<> 9B1<> 9D8< 56D3>
56D3> 9D1<> 5C4<> CPU_DATA<12>	E2_3	16	23	E0_3	CPU_DATA<6> 5D4<> 9D1<> 56D3>
56D3> 9C8< 9B1<> 5B4<> CPU_DATA<52>	E2_2	17	22	E0_2	CPU_DATA<0> 5D4<> 9D1<> 56D3>
56D3> 9B1<> 6C4< 5B4<> CPU_DATA<42>	E2_1	18	21	E0_1	CPU_DATA<43> 5B4<> 6C4< 9B1<> 56D3>
56D3> 9D8< 9B1<> 5B4<> CPU_DATA<48>	E2_0	19	20	E0_0	CPU_DATA<46> 5B4<> 6C4< 9B1<> 56D3>
	GND			GND	
		39	40 41 42 43 44 45		

J19
CON_37SM_MICTOR
F-ST-SM
OMIT
DPROBE SYM_VER3

	GND	1	2	GND	
	GND	2	1	GND	
	Q0	3	36	CLK2	
	D3_7	4	35	D1_7	CPU_ADDR<11> 4C7<> 9C3<> 56D3>
	D3_6	5	34	D1_6	CPU_ADDR<6> 4C7<> 9D3<> 56D3>
	D3_5	6	33	D1_5	CPU_TA_L 4C3< 7C7< 9A1<> 56C3>
	D3_4	7	32	D1_4	CPU_TT<0> 4B7<> 7A7< 9B3<> 56D3>
	D3_3	8	31	D1_3	CPU_ADDR<2> 4C7<> 9D3<> 56D3>
	D3_2	9	30	D1_2	CPU_BR_L 4D7> 7C7< 9D3< 56D3>
	D3_1	10	29	D1_1	CPU_TT<4> 4B7<> 7A7< 9B3<> 56D3>
	D3_0	11	28	D1_0	CPU_ADDR<0> 4C7<> 9D3<> 56D3>
	D2_7	12	27	D0_7	CPU_TBST_L 4B7> 7B7< 9B3<> 56D3>
	D2_6	13	26	D0_6	CPU_DTI<1> 4C3< 9A1<> 56C3>
	D2_5	14	25	D0_5	CPU_TT<2> 4B7<> 7A7< 9B3<> 56D3>
	D2_4	15	24	D0_4	CPU_BG_L 4D7< 7B7< 9D3<> 56D3>
	D2_3	16	23	D0_3	CPU_QACK_L 4C3< 9B3<> 56C3>
	D2_2	17	22	D0_2	CPU_DTI<2> 4C3< 9A1<> 56C3>
	D2_1	18	21	D0_1	
	D2_0	19	20	D0_0	
	GND			GND	
		39	40 41 42 43 44 45		

56D3> 9D3<> 4C7<> CPU_ADDR<8>
56C3> 9C3<> 7A7< 4A7> CPU_CI_L
56D3> 9B3<> 4B7> CPU_TSIZ<1>
56D3> 9D3<> 4C7<> CPU_ADDR<4>
56C3> 9A1<> 7B7< 4C3< CPU_TEA_L
56D3> 9B3<> 7A7< 4B7<> CPU_TT<1>
56D3> 9D3<> 4C7<> CPU_ADDR<1>
56D3> 9B3<> 4B7> CPU_TSIZ<0>
56C3> 9B3<> 7A7< 4B7> CPU_WT_L
56D3> 9B3<> 7A7< 4B7<> CPU_TT<3>
56C3> 9B1< 7B7< 4C2< CPU_DRDY_L
56C3> 4B8<> CPU_GBL_L
56C3> 9B3<> 7B7< 4A7< CPU_AACK_L

+MAXBUS_SLEEP

8D1< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 59C7> 6C5< 4D5<
52C6> 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7<

C350 10UF N20P80% 10V Y5V 805
C958 10UF N20P80% 10V Y5V 805
C983 10UF N20P80% 10V Y5V 805
C992 10UF N20P80% 10V Y5V 805
C969 2.2UF N20P80% 10V CERM 805
C353 2.2UF N20P80% 10V CERM 805

C988 0.1UF 20% 10V CERM 402
C1026 0.1UF 20% 10V CERM 402
C1043 0.1UF 20% 10V CERM 402
C982 0.1UF 20% 10V CERM 402
C1013 0.1UF 20% 10V CERM 402
C999 0.1UF 20% 10V CERM 402
C974 0.1UF 20% 10V CERM 402
C1003 0.1UF 20% 10V CERM 402
C1041 0.1UF 20% 10V CERM 402
C1014 0.1UF 20% 10V CERM 402
C987 0.1UF 20% 10V CERM 402
C998 0.1UF 20% 10V CERM 402
C995 0.1UF 20% 10V CERM 402
C991 0.1UF 20% 10V CERM 402
C977 0.1UF 20% 10V CERM 402

+MAXBUS_SLEEP

8D4< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 59C7> 6C5< 4D5<
52C6> 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7<

C972 0.1UF 20% 10V CERM 402
C981 0.1UF 20% 10V CERM 402
C980 0.1UF 20% 10V CERM 402
C973 0.1UF 20% 10V CERM 402
C993 0.1UF 20% 10V CERM 402
C990 0.1UF 20% 10V CERM 402
C994 0.1UF 20% 10V CERM 402
C1007 0.1UF 20% 10V CERM 402
C961 0.1UF 20% 10V CERM 402
C1020 0.1UF 20% 10V CERM 402
C1021 0.1UF 20% 10V CERM 402
C967 0.1UF 20% 10V CERM 402

CPU_VCORE_SLEEP

59D7> 59B5> 52C6> 45D2<> 8B7< 4D7< 4D3<

C1040 10UF N20P80% 10V Y5V 805
C976 10UF N20P80% 10V Y5V 805
C1037 10UF N20P80% 10V Y5V 805
C1033 10UF N20P80% 10V Y5V 805
C1032 10UF N20P80% 10V Y5V 805
C1042 10UF N20P80% 10V Y5V 805
C1016 10UF N20P80% 10V Y5V 805
C364 10UF N20P80% 10V Y5V 805
C1911 10UF N20P80% 10V Y5V 805
C1912 10UF N20P80% 10V Y5V 805
C1913 10UF N20P80% 10V Y5V 805
C1914 10UF N20P80% 10V Y5V 805
C598 10UF N20P80% 10V Y5V 805
C1054 10UF N20P80% 10V Y5V 805
C1055 10UF N20P80% 10V Y5V 805
C1056 10UF N20P80% 10V Y5V 805
C1057 10UF N20P80% 10V Y5V 805
C1058 10UF N20P80% 10V Y5V 805

INTREPID CLOCK OUTPUT

NOSTUFF J27 U.FL-R_SMT F-ST-SM
NOSTUFF R314 0 5% 1/16W MF 402
56B3> INT_CLOCK_OUT
NOSTUFF R308 47 5% 1/16W MF 402
PLACE BOTH RESISTORS CLOSE TO INTREPID
NOSTUFF R313 22 5% 1/16W MF 402
59A7> 56B3> 54A7< 16C7< 9B4< INT_ANALYZER_CLK
SYSCLK_LA 8D8<> 56B3>

(518S0104)

CPU CORE DECOUPLING

59D7> 59B5> 52C6> 45D2<> 8C1< 4D7< 4D3< CPU_VCORE_SLEEP

C1022 1UF 10% 6.3V CERM 402
C1027 1UF 10% 6.3V CERM 402
C1011 1UF 10% 6.3V CERM 402
C1008 1UF 10% 6.3V CERM 402
C1010 1UF 10% 6.3V CERM 402
C1025 1UF 10% 6.3V CERM 402
C1098 1UF 10% 6.3V CERM 402
C1009 1UF 10% 6.3V CERM 402
C1002 1UF 10% 6.3V CERM 402
C1023 1UF 10% 6.3V CERM 402
C1017 1UF 10% 6.3V CERM 402
C1031 1UF 10% 6.3V CERM 402
C997 1UF 10% 6.3V CERM 402
C996 1UF 10% 6.3V CERM 402
C1012 1UF 10% 6.3V CERM 402
C1024 1UF 10% 6.3V CERM 402
C1001 1UF 10% 6.3V CERM 402
C1028 1UF 10% 6.3V CERM 402
C1018 1UF 10% 6.3V CERM 402
C1096 1UF 10% 6.3V CERM 402
C1097 1UF 10% 6.3V CERM 402
C1901 0.1UF 20% 10V CERM 402
C1902 0.1UF 20% 10V CERM 402
C1903 0.1UF 20% 10V CERM 402
C1904 0.1UF 20% 10V CERM 402
C1910 0.1UF 20% 10V CERM 402

CPU CORE DECOUPLING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0013	21	CAP,CER,.22UF,20%,6.3V,0402,X5R		1GHZ_DECOUP
		C1022,C1027,C1011,C1008,C1010,C1025,C1009,C1002,C1023,C1017,C1031,C997,C996,C1012,C1024,C1001,C1028,C1018,C1096,C1097,C1098		
138S0541	21	CAP,CER,1UF,10%,6.3V,0402,X5R		1_25GHZ_DECOUP
		C1022,C1027,C1011,C1008,C1010,C1025,C1009,C1002,C1023,C1017,C1031,C997,C996,C1012,C1024,C1001,C1028,C1018,C1096,C1097,C1098		

PULLDOWN ON TRST* STRONGER TO OVERCOME POSSIBLE LEAKAGE

FMAX DEBUG CONNECTOR

NOSTUFF J32 SM12B-SRSS-TB F-RT-SM

	14		
1			CPU_PLL_CFG<0> 4D3< 6C6<
2			CPU_PLL_CFG<1> 4D3< 6C6<
3			CPU_PLL_CFG<2> 4D3< 6C6<
4			CPU_PLL_CFG<3> 4C3< 6C6<
5			CPU_PLL_CFGEXT 4C3< 6C6<
6			
7	NO_TEST		NC_FMAX7
8	NO_TEST		NC_FMAX8
9			PWR_SWITCH* 44B1< 44C5<> 59D5>
10			PMU_RST* 29B3<> 44A5<> 44B5<> 59D5>
11	NO_TEST		NC_RESET_BUTTON_L
12			
	13		

(518S0105)

+3V_MAIN

R937 10K 1% 1/16W MF 402

NOSTUFF J22 SM-1

		1	2	+MAXBUS_SLEEP 52C6> 59C7> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2< 46D4<
NC_TESTMODE	NO_TEST	3	4	CPU_CHKSTP_OUT_L 4B3> 7B5< 8D5<> 59C7>
NC_LCENABLE	NO_TEST	5	6	CPU_HRESET_L 4B3< 7A3< 7A5< 7B3< 44C2< 44D2< 59C7>
NC_JTAG7	NO_TEST	7	8	CPU_SRESET_L 4B3< 7A5< 59C5>
		9	10	NO_TEST NC_JTAG10
JTAG_ASIC_TMS 59D7> 35B4<> 35A2< 34B7<		11	12	JTAG_CPU_TMS 4C3< 7A5< 59C7>
JTAG_ASIC_TDI 59D7> 34B7< 28C6<		13	14	JTAG_CPU_TDI 4C3< 7A5< 59C7>
JTAG_ASIC_TDO 59D7> 35B4<>		15	16	JTAG_CPU_TDO 4C3> 59C7>
JTAG_ASIC_TCK 59D7> 35C4< 34B7<		17	18	JTAG_CPU_TCK 4C3< 7D5< 59C7>
JTAG_ASIC_TRST_L 59C7> 34B7<		19	20	JTAG_CPU_TRST_L 4C3< 7C5< 59C7>

R939 10K 1% 1/16W MF 402
R940 1K 1% 1/16W MF 402

(511S0018)

LA CONS & ESP

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 8 OF 69	

DRAWING

INTREPID BOOT STRAPS

BITS 48 - 63

52C6> 46D4< 45D2<> 8D4< 8D1< 8A3<> 7A3< 6D6< 6C5< 4D5< +MAXBUS_SLEEP 7C7< 7B3< 7A3< 8D4< 6C5< 4D5< 7C7< 7C5< 7B3< 44D2< 44D1< 44B7< 9B7< 59C7>

R890 10K	R868 10K	R892 10K	R832 10K	R863 10K	R339 10K	R340 10K	R864 10K	R876 10K	R865 10K	R885 10K	R855 10K	R869 10K	R894 4.7K	R355 4.7K	R893 4.7K	R343 4.7K
R360 4.7K	R352 4.7K	R338 4.7K	R341 4.7K	R359 4.7K	R366 4.7K	R358 4.7K	R886 4.7K	R354 4.7K	R351 4.7K	R870 4.7K						

56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<48>
56D3> 9B1<> 8C4<> 5B4<> CPU_DATA<49>
56D3> 9B1<> 8C8<> 5B4<> CPU_DATA<50>
56D3> 9B1<> 8D8<> 5B4<> CPU_DATA<51>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<52>
56D3> 9B1<> 8C7<> 5B4<> CPU_DATA<53>
56D3> 9B1<> 8D7<> 5B4<> CPU_DATA<54>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<55>
CPU_DATA<57> 5B4<> 8D5<> 9B1<>
CPU_DATA<58> 5B4<> 8D4<> 9B1<>
CPU_DATA<59> 5B4<> 8D8<> 9B1<>
CPU_DATA<60> 5B4<> 8D8<> 9B1<>
CPU_DATA<61> 5B4<> 8D4<> 9B1<>
CPU_DATA<62> 5B4<> 8D4<> 9B1<>
CPU_DATA<63> 5A4<> 8D5<> 9B1<> 56D3>

0:: BUF_REF_CLK_OUTENABLE_H ACTIVE
1:: INACTIVE

1:: SEL_PLL_4EXTSRC EXTERNAL SOURCE

0:: EN_PCI_ROM_P BOOTROM ON PCI1
1:: BOOTROM ON IDE/CARDSLOT

0:: TI 1394B WORKAROUND NORMAL 1394B
1:: TI PHY WORKAROUND

MAXBUS OUTPUT IMPEDANCE
111: 28.6 OHM
011: 33.3 OHM
101: 40 OHM
001: 50 OHM
110: 66.6 OHM
010: 100 OHM
100: 200 OHM
000: 200 OHM

SPARE
SPARE

0:: 0-1 IDE / 2-3 PCI1
1:: ROM_Ovrly_Rng

0:: REQ/GNT GPIOS
1:: PCI1_REQ2_L / PCI1_GNT2_L GPIOS

0:: REQ/GNT GPIOS
1:: PCI1_REQ1_L / PCI1_GNT1_L GPIOS

0:: REQ/GNT GPIOS
1:: PCI1_REQ0_L / PCI1_GNT0_L GPIOS

0:: LEGACY INTERFACE
1:: B-MODE INTERFACE
FIREWIRE PHY INTERFACE

0:: MAX BUS (G4)
1:: 60X BUS (G3)
PROCESSOR BUS MODE

BITS 32 - 39

45D2<> 44D2< 44D1< 44B7< 7C5< 7B3< 7A3< 8D4< 6C5< 4D5< +MAXBUS_SLEEP 9D8< 8D4< 8D1< 8A3<> 7C7< 7C5< 59C7> 52C6> 46D4<

R833 10K	R852 10K	R862 10K	R854 10K	R853 10K	R342 4.7K	R345 4.7K	R861 4.7K	R353 4.7K	R344 4.7K

56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<32>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<33>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<34>
56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<35>
56D3> 9C1<> 8D4<> 5C4<> CPU_DATA<36>

0:: TDI OUTPUT(JTAG)
1:: TDI OUTPUT

0:: ACTIVE
1:: ANALYZERCLK_EN_H ACTIVE

0:: DDR_TPDEN_POL ACTIVE HIGH
1:: DDR_TPDEN_POL ACTIVE LOW

0:: ACTIVE HIGH
1:: EXTPLL_SDWN_POL ACTIVE LOW

SPARE

DDR_TPDMODEENABLE_H

INTREPID V1.1 IS 133MHZ ONLY

52D3> 30D5< 28D6<> 16D6< +1_5V_INTREPID_PLL — R720 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7 52D3>

C854 0.1UF 20% 10V CERM 402 (1 to 2)
C1101 0.1UF 20% 10V CERM 402 (1 to 2)

9A2<> INT_PLL6_GND

H26 VDD15A_7 (PLL6)

U25 INTREPID BGA SEE_TABLE (ON PAGE 12) (1 OF 9)

56D3> 8B4<> 7C7< 4D7> CPU_BR_L	E29	BR
56D3> 8B4<> 7B7< 4D7< CPU_BG_L	E26	BG
56D3> 8B7<> 7C7< 4D7<> CPU_TS_L	B27	TS
56D3> 8B4<> 4C7<> CPU_ADDR<0>	D24	A_0
56D3> 8B5<> 4C7<> CPU_ADDR<1>	D25	A_1
56D3> 8B4<> 4C7<> CPU_ADDR<2>	A27	A_2
56D3> 8B8<> 4C7<> CPU_ADDR<3>	E24	A_3
56D3> 8B5<> 4C7<> CPU_ADDR<4>	G23	A_4
56D3> 8B7<> 4C7<> CPU_ADDR<5>	B26	A_5
56D3> 8C4<> 4C7<> CPU_ADDR<6>	A26	A_6
56D3> 8B7<> 4C7<> CPU_ADDR<7>	D23	A_7
56D3> 8C5<> 4C7<> CPU_ADDR<8>	A25	A_8
56D3> 8B8<> 4C7<> CPU_ADDR<9>	E23	A_9
56D3> 8B8<> 4C7<> CPU_ADDR<10>	J22	A_10
56D3> 8C4<> 4C7<> CPU_ADDR<11>	B25	A_11
56D3> 8B7<> 4C7<> CPU_ADDR<12>	H22	A_12
56D3> 8B8<> 4C7<> CPU_ADDR<13>	G22	A_13
56D3> 8B7<> 4C7<> CPU_ADDR<14>	D22	A_14
56D3> 8B7<> 4C7<> CPU_ADDR<15>	B24	A_15
56D3> 8B8<> 4C7<> CPU_ADDR<16>	B23	A_16
56D3> 8B8<> 4C7<> CPU_ADDR<17>	E22	A_17
56D3> 8C8<> 4C7<> CPU_ADDR<18>	J21	A_18
56D3> 8B7<> 4C7<> CPU_ADDR<19>	G21	A_19
56D3> 8B8<> 4C7<> CPU_ADDR<20>	E21	A_20
56D3> 8C7<> 4C7<> CPU_ADDR<21>	A24	A_21
56D3> 8C7<> 4C7<> CPU_ADDR<22>	D21	A_22
56D3> 8C8<> 4C7<> CPU_ADDR<23>	A23	A_23
56D3> 8B7<> 4B7<> CPU_ADDR<24>	H20	A_24
56D3> 8B8<> 4B7<> CPU_ADDR<25>	B22	A_25
56D3> 8C8<> 4B7<> CPU_ADDR<26>	H21	A_26
56D3> 8C8<> 4B7<> CPU_ADDR<27>	A22	A_27
56D3> 8C7<> 4B7<> CPU_ADDR<28>	E20	A_28
56D3> 8C8<> 4B7<> CPU_ADDR<29>	B21	A_29
56D3> 8C7<> 4B7<> CPU_ADDR<30>	D20	A_30
56D3> 8C7<> 4B7<> CPU_ADDR<31>	A21	A_31
56C3> 8C5<> 7A7< 4A7> CPU_CI_L	G26	CI
56C3> 7B7< 4B8< CPU_INT_GBL_L	A29	GBL
56D3> 8B4<> 7B7< 4B7> CPU_TBST_L	A28	TBST
56D3> 8B5<> 4B7> CPU_TSIZ<0>	G24	TSIZ_0
56D3> 8B5<> 4B7> CPU_TSIZ<1>	H24	TSIZ_1
56D3> 8B7< 4B7> CPU_TSIZ<2>	D26	TSIZ_2
56D3> 8B4<> 7A7< 4B7<> CPU_TT<0>	E25	TT_0
56D3> 8B5<> 7A7< 4B7<> CPU_TT<1>	G25	TT_1
56D3> 8B4<> 7A7< 4B7<> CPU_TT<2>	B28	TT_2
56D3> 8B5<> 7A7< 4B7<> CPU_TT<3>	D27	TT_3
56D3> 8B4<> 7A7< 4B7<> CPU_TT<4>	J25	TT_4
56C3> 8B5<> 7A7< 4B7> CPU_WT_L	D28	WT
56C3> 8B5<> 7B7< 4A7< CPU_AACK_L	B29	AACK
56C3> 8B8<> 7C7< 4A7<> CPU_ARTRY_L	H23	ARTRY
56C3> 8B8<> 7C7< 4A7> CPU_HIT_L	B31	HIT
56C3> 8B7<> 7D5< 4C3> CPU_QREQ_L	A32	QREQ
56C3> 8B4<> 4C3< CPU_QACK_L	G27	QACK
44B8<> INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
44B5<> INT_SUSPEND_ACK_L	AM8	SUSPENDACK
56C3> INT_CPU_FB_IN	J24	CPU_FB_IN
56C3> INT_CPU_FB_OUT	H16	CPU_FB_OUT
INT_ANALYZER_CLKA	G8	ANALYZER_CLK
44C4<> CPU_CLK_EN	AH9	STOPCPUCLK
INTREPID_ACS_REF	H13	ACS_REF
56C3> SYSCLK_CPU_UF	J15	CPU_CLK
7C5< 4C3<> CPU_TBEN	A31	TBEN

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0> 5D4<> 8C4<> 56D3>
D_1	G12	CPU_DATA<1> 5D4<> 8C7<> 56D3>
D_2	E11	CPU_DATA<2> 5D4<> 8C8<> 56D3>
D_3	H11	CPU_DATA<3> 5D4<> 8C5<> 56D3>
D_4	B9	CPU_DATA<4> 5D4<> 8C7<> 56D3>
D_5	B8	CPU_DATA<5> 5D4<> 8C8<> 56D3>
D_6	A9	CPU_DATA<6> 5D4<> 8C4<> 56D3>
D_7	A8	CPU_DATA<7> 5D4<> 8C8<> 56D3>
D_8	E12	CPU_DATA<8> 5D4<> 8C5<> 56D3>
D_9	D11	CPU_DATA<9> 5D4<> 8C4<> 56D3>
D_10	B10	CPU_DATA<10> 5D4<> 8C7<> 56D3>
D_11	J13	CPU_DATA<11> 5C4<> 8C5<> 56D3>
D_12	A10	CPU_DATA<12> 5C4<> 8C5<> 56D3>
D_13	D12	CPU_DATA<13> 5C4<> 8C7<> 56D3>
D_14	E13	CPU_DATA<14> 5C4<> 8C8<> 56D3>
D_15	G13	CPU_DATA<15> 5C4<> 8C5<> 56D3>
D_16	B11	CPU_DATA<16> 5C4<> 8C4<> 56D3>
D_17	D13	CPU_DATA<17> 5C4<> 8C7<> 56D3>
D_18	A11	CPU_DATA<18> 5C4<> 8C4<> 56D3>
D_19	G14	CPU_DATA<19> 5C4<> 8C4<> 56D3>
D_20	H14	CPU_DATA<20> 5C4<> 8C4<> 56D3>
D_21	E14	CPU_DATA<21> 5C4<> 8C8<> 56D3>
D_22	B12	CPU_DATA<22> 5C4<> 8C7<> 56D3>
D_23	G15	CPU_DATA<23> 5C4<> 8C8<> 56D3>
D_24	B13	CPU_DATA<24> 5C4<> 8D4<> 56D3>
D_25	H15	CPU_DATA<25> 5C4<> 8D7<> 56D3>
D_26	D14	CPU_DATA<26> 5C4<> 8C5<> 56D3>
D_27	B14	CPU_DATA<27> 5C4<> 8C7<> 56D3>
D_28	A12	CPU_DATA<28> 5C4<> 8D8<> 56D3>
D_29	G16	CPU_DATA<29> 5C4<> 8C8<> 56D3>
D_30	E15	CPU_DATA<30> 5C4<> 8C5<> 56D3>
D_31	J16	CPU_DATA<31> 5C4<> 8D7<> 56D3>
D_32	D15	CPU_DATA<32> 5C4<> 8D7<> 9B7< 56D3>
D_33	A14	CPU_DATA<33> 5C4<> 8D8<> 9B7< 56D3>
D_34	A13	CPU_DATA<34> 5C4<> 8D8<> 9B7< 56D3>
D_35	D16	CPU_DATA<35> 5C4<> 8D7<> 9B7< 56D3>
D_36	E16	CPU_DATA<36> 5C4<> 8D4<> 9A7< 56D3>
D_37	G17	CPU_DATA<37> 5B4<> 8D5<> 56D3>
D_38	B15	CPU_DATA<38> 5B4<> 8D5<> 56D3>
D_39	H17	CPU_DATA<39> 5B4<> 8D5<> 56D3>
D_40	A15	CPU_DATA<40> 5B4<> 6C4< 8D7<> 56D3>
D_41	B16	CPU_DATA<41> 5B4<> 6C4< 8C4<> 56D3>
D_42	E17	CPU_DATA<42> 5B4<> 6C4< 8C5<> 56D3>
D_43	A16	CPU_DATA<43> 5B4<> 6C4< 8C4< 56D3>
D_44	J18	CPU_DATA<44> 5B4<> 6C4< 8C8<> 56D3>
D_45	H18	CPU_DATA<45> 5B4<> 6C4< 8C7<> 56D3>
D_46	D17	CPU_DATA<46> 5B4<> 6C4< 8C4<> 56D3>
D_47	G18	CPU_DATA<47> 5B4<> 6C4< 8C7< 56D3>
D_48	A17	CPU_DATA<48> 5B4<> 8C5<> 9D8< 56D3>
D_49	B17	CPU_DATA<49> 5B4<> 8C4<> 9D8< 56D3>
D_50	E18	CPU_DATA<50> 5B4<> 8C8<> 9D8< 56D3>
D_51	B18	CPU_DATA<51> 5B4<> 8C8<> 9D8< 56D3>
D_52	D18	CPU_DATA<52> 5B4<> 8C5<> 9C8< 56D3>
D_53	A18	CPU_DATA<53> 5B4<> 8C7<> 9C8< 56D3>
D_54	A19	CPU_DATA<54> 5B4<> 8D7<> 9C8< 56D3>
D_55	H19	CPU_DATA<55> 5B4<> 8C5<> 9C8< 56D3>
D_56	B19	CPU_DATA<56> 5B4<> 8D8<> 56D3>
D_57	J19	CPU_DATA<57> 5B4<> 8D5<> 9D5< 56D3>
D_58	A20	CPU_DATA<58> 5B4<> 8D4<> 9D5< 56D3>
D_59	D19	CPU_DATA<59> 5B4<> 8D8<> 9D5< 56D3>
D_60	E19	CPU_DATA<60> 5B4<> 8D8<> 9D5< 56D3>
D_61	G19	CPU_DATA<61> 5B4<> 8D4<> 9C5< 56D3>
D_62	B20	CPU_DATA<62> 5B4<> 8D4<> 9C5< 56D3>
D_63	G20	CPU_DATA<63> 5A4<> 8D5<> 9C5< 56D3>
DBG	A30	CPU_DBG_L 4C3< 7B7< 8B8<> 56C3>
DRDY	G28	CPU_DRDY_L 4C2< 7B7< 8B5<> 56C3>
DTI_0	K25	CPU_DTI<0> 4C3< 8B7<> 56C3>
DTI_1	D29	CPU_DTI<1> 4C3< 8B4<> 56C3>
DTI_2	B30	CPU_DTI<2> 4C3< 8B4<> 56C3>
TA	E27	CPU_TA_L 4C3< 7C7< 8C4<> 56C3>
TEA	E28	CPU_TEA_L 4C3< 7B7< 8B5<> 56C3>

VIN = INTREPID VCORE (1.7V)
VOUT = MAXBUS RAIL (1.8V)

56C3> 4D2< SYSCLK_CPU — R713 0 5% 1/16W MF 402 — 56C3> SYSCLK_CPU_UF

56B3> CPU_FB_PLUS3

ADDS 2" (0.35 NS) ADDS 1" (0.17 NS) ADDS 3" (0.5 NS)

56C3> CPU_FBI_PLUS1

R772 0 NOSTUFF — R766 0 NOSTUFF — R321 0 NOSTUFF — R777 0 — R310 0 — R752 470

56C3> CPU_FB_MINUS3

R776 0 — R757 0 NOSTUFF — R319 0 NOSTUFF — R765 0

56C3> CPU_FB_PLUS2

56C3> CPU_FBO_PLUS1

MAIN LOOP IS 3" (0.5 NS) SHORTER THAN MAXBUS CLOCK

ALLOWS ADJUSTING FB CLOCK FROM -3" (0.5 NS) TO +2" (0.35 NS) IN 1" (0.17 NS) INCREMENTS
PLACE ALL SERPENTINES ON INTERNAL LAYER

59A7> 56B3> 54A7< 16C7< 8A2< INT_ANALYZER_CLK — R764 10 5% 1/16W MF 402 — INT_V1

R712 1K 1% 1/16W MF 402 (9D3< INT_PLL6_GND)

XW47 SM (NO_TEST) — VSSA_7 (PLL6) H25

INTREPID MAX

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DRAWING

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INTREPID 1.1 SHOULD ALLOW MAXBUS
RAIL TO TURN OFF IN SLEEP

52C3> 46B4<> 17D5< 17A4< 17A3< 16D7< 16C2< 16A8< 11A6< 59C7> +1_5V_AGP

59C7> 47B2<> 46B3< 11D3< +INTREPID_CORE_MAIN

+1_8V_MAIN

+2_5V_MAIN

+3V_MAIN

U25
INTREPID
BGA
(8 OF 9)
SEE_TABLE

VDD1.8/CPUVIO

VDD2.5

POWER/GROUND

VSS

VSS

U25
INTREPID
BGA
(9 OF 9)
SEE_TABLE

POWER

VDD1.5

VDD3.3

GROUND

VSS

VSS

AGP_IO_VDD

VDD3.3

AGP_IO_VSS

SP1 CLIP-SM EMI-SPRING SEE_TABLE

SP2 CLIP-SM EMI-SPRING SEE_TABLE

SP3 CLIP-SM EMI-SPRING SEE_TABLE

SP4 CLIP-SM EMI-SPRING SEE_TABLE

CLIPS TO ATTACH INTREPID
HEATSINK TO GND AT THE
FOUR CORNERS

INTREPID EMI CLIP SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1125	4	INTREPID EMI CLIP	SP1,SP2,SP3,SP4	?	

INTREPID VERSION SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0198	1	IC,ASIC,INTREPID,V1.X	U25		INT_V1
343S0211	1	IC,ASIC,INTREPID,V2.1	U25	CRITICAL	INT_V2

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INTREPID POWER

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SCALE: NONE

SHT 10 OF 69

DRAWING

+1_8V_MAIN — INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
36 X 0.1UF (0402)

C289 10UF N20P80% 10V Y5V 805
C291 10UF N20P80% 10V Y5V 805
C288 10UF N20P80% 10V Y5V 805
C290 10UF N20P80% 10V Y5V 805
C890 0.1UF 20% 10V CERM 402
C832 0.1UF 20% 10V CERM 402
C900 0.1UF 20% 10V CERM 402
C888 0.1UF 20% 10V CERM 402
C891 0.1UF 20% 10V CERM 402
C844 0.1UF 20% 10V CERM 402
C824 0.1UF 20% 10V CERM 402
C872 0.1UF 20% 10V CERM 402
C874 0.1UF 20% 10V CERM 402
C899 0.1UF 20% 10V CERM 402
C901 0.1UF 20% 10V CERM 402
C823 0.1UF 20% 10V CERM 402
C845 0.1UF 20% 10V CERM 402
C871 0.1UF 20% 10V CERM 402
C834 0.1UF 20% 10V CERM 402
C884 0.1UF 20% 10V CERM 402
C896 0.1UF 20% 10V CERM 402
C898 0.1UF 20% 10V CERM 402
C886 0.1UF 20% 10V CERM 402
C846 0.1UF 20% 10V CERM 402
C885 0.1UF 20% 10V CERM 402
C887 0.1UF 20% 10V CERM 402
C870 0.1UF 20% 10V CERM 402
C897 0.1UF 20% 10V CERM 402
C889 0.1UF 20% 10V CERM 402
C842 0.1UF 20% 10V CERM 402
C895 0.1UF 20% 10V CERM 402
C869 0.1UF 20% 10V CERM 402
C873 0.1UF 20% 10V CERM 402
C902 0.1UF 20% 10V CERM 402
C843 0.1UF 20% 10V CERM 402
C278 0.1UF 20% 10V CERM 402
C849 0.1UF 20% 10V CERM 402
C281 0.1UF 20% 10V CERM 402
C280 0.1UF 20% 10V CERM 402
C279 0.1UF 20% 10V CERM 402

INTREPID CORE DECOUPLING

59C7> 47B2<> 46B3< 10D6< +INTREPID_CORE_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.1UF (0402)

C702 10UF N20P80% 10V Y5V 805
C727 10UF N20P80% 10V Y5V 805
C292 10UF N20P80% 10V Y5V 805
C841 10UF N20P80% 10V Y5V 805
C787 0.1UF 20% 10V CERM 402
C789 0.1UF 20% 10V CERM 402
C749 0.1UF 20% 10V CERM 402
C797 0.1UF 20% 10V CERM 402
C719 0.1UF 20% 10V CERM 402
C800 0.1UF 20% 10V CERM 402
C810 0.1UF 20% 10V CERM 402
C766 0.1UF 20% 10V CERM 402
C731 0.1UF 20% 10V CERM 402
C732 0.1UF 20% 10V CERM 402
C764 0.1UF 20% 10V CERM 402
C831 0.1UF 20% 10V CERM 402
C833 0.1UF 20% 10V CERM 402
C765 0.1UF 20% 10V CERM 402
C808 0.1UF 20% 10V CERM 402
C763 0.1UF 20% 10V CERM 402
C780 0.1UF 20% 10V CERM 402
C798 0.1UF 20% 10V CERM 402
C779 0.1UF 20% 10V CERM 402
C790 0.1UF 20% 10V CERM 402
C746 0.1UF 20% 10V CERM 402
C730 0.1UF 20% 10V CERM 402
C721 0.1UF 20% 10V CERM 402
C788 0.1UF 20% 10V CERM 402
C734 0.1UF 20% 10V CERM 402
C748 0.1UF 20% 10V CERM 402
C811 0.1UF 20% 10V CERM 402
C747 0.1UF 20% 10V CERM 402
C799 0.1UF 20% 10V CERM 402

+2_5V_MAIN — INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.1UF (0402)

C277 10UF N20P80% 10V Y5V 805
C271 10UF N20P80% 10V Y5V 805
C240 10UF N20P80% 10V Y5V 805
C641 10UF N20P80% 10V Y5V 805
C700 0.1UF 20% 10V CERM 402
C878 0.1UF 20% 10V CERM 402
C725 0.1UF 20% 10V CERM 402
C836 0.1UF 20% 10V CERM 402
C817 0.1UF 20% 10V CERM 402
C839 0.1UF 20% 10V CERM 402
C857 0.1UF 20% 10V CERM 402
C794 0.1UF 20% 10V CERM 402
C855 0.1UF 20% 10V CERM 402
C880 0.1UF 20% 10V CERM 402
C837 0.1UF 20% 10V CERM 402
C877 0.1UF 20% 10V CERM 402
C688 0.1UF 20% 10V CERM 402
C767 0.1UF 20% 10V CERM 402
C793 0.1UF 20% 10V CERM 402
C815 0.1UF 20% 10V CERM 402
C904 0.1UF 20% 10V CERM 402
C827 0.1UF 20% 10V CERM 402
C876 0.1UF 20% 10V CERM 402
C698 0.1UF 20% 10V CERM 402
C856 0.1UF 20% 10V CERM 402
C735 0.1UF 20% 10V CERM 402
C722 0.1UF 20% 10V CERM 402
C750 0.1UF 20% 10V CERM 402
C753 0.1UF 20% 10V CERM 402
C687 0.1UF 20% 10V CERM 402
C792 0.1UF 20% 10V CERM 402
C668 0.1UF 20% 10V CERM 402
C714 0.1UF 20% 10V CERM 402
C736 0.1UF 20% 10V CERM 402
C801 0.1UF 20% 10V CERM 402
C825 0.1UF 20% 10V CERM 402
C838 0.1UF 20% 10V CERM 402
C723 0.1UF 20% 10V CERM 402
C803 0.1UF 20% 10V CERM 402
C791 0.1UF 20% 10V CERM 402
C755 0.1UF 20% 10V CERM 402
C818 0.1UF 20% 10V CERM 402
C802 0.1UF 20% 10V CERM 402
C813 0.1UF 20% 10V CERM 402
C699 0.1UF 20% 10V CERM 402
C751 0.1UF 20% 10V CERM 402
C826 0.1UF 20% 10V CERM 402
C752 0.1UF 20% 10V CERM 402
C768 0.1UF 20% 10V CERM 402
C816 0.1UF 20% 10V CERM 402
C814 0.1UF 20% 10V CERM 402
C754 0.1UF 20% 10V CERM 402
C724 0.1UF 20% 10V CERM 402
C781 0.1UF 20% 10V CERM 402
C782 0.1UF 20% 10V CERM 402

+3V_MAIN — INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
66 X 0.1UF (0402)

C655 10UF N20P80% 10V Y5V 805
C264 10UF N20P80% 10V Y5V 805
C892 10UF N20P80% 10V Y5V 805
C637 10UF N20P80% 10V Y5V 805
C745 0.1UF 20% 10V CERM 402
C830 0.1UF 20% 10V CERM 402
C775 0.1UF 20% 10V CERM 402
C717 0.1UF 20% 10V CERM 402
C829 0.1UF 20% 10V CERM 402
C806 0.1UF 20% 10V CERM 402
C691 0.1UF 20% 10V CERM 402
C762 0.1UF 20% 10V CERM 402
C777 0.1UF 20% 10V CERM 402
C796 0.1UF 20% 10V CERM 402
C867 0.1UF 20% 10V CERM 402
C866 0.1UF 20% 10V CERM 402
C863 0.1UF 20% 10V CERM 402
C868 0.1UF 20% 10V CERM 402
C812 0.1UF 20% 10V CERM 402
C821 0.1UF 20% 10V CERM 402
C822 0.1UF 20% 10V CERM 402
C893 0.1UF 20% 10V CERM 402
C720 0.1UF 20% 10V CERM 402
C728 0.1UF 20% 10V CERM 402
C809 0.1UF 20% 10V CERM 402
C680 0.1UF 20% 10V CERM 402
C894 0.1UF 20% 10V CERM 402
C643 0.1UF 20% 10V CERM 402
C656 0.1UF 20% 10V CERM 402
C689 0.1UF 20% 10V CERM 402
C774 0.1UF 20% 10V CERM 402
C828 0.1UF 20% 10V CERM 402
C850 0.1UF 20% 10V CERM 402
C743 0.1UF 20% 10V CERM 402
C761 0.1UF 20% 10V CERM 402
C707 0.1UF 20% 10V CERM 402
C883 0.1UF 20% 10V CERM 402
C807 0.1UF 20% 10V CERM 402
C776 0.1UF 20% 10V CERM 402
C744 0.1UF 20% 10V CERM 402
C718 0.1UF 20% 10V CERM 402
C712 0.1UF 20% 10V CERM 402
C835 0.1UF 20% 10V CERM 402
C729 0.1UF 20% 10V CERM 402
C881 0.1UF 20% 10V CERM 402
C676 0.1UF 20% 10V CERM 402
C716 0.1UF 20% 10V CERM 402
C805 0.1UF 20% 10V CERM 402
C644 0.1UF 20% 10V CERM 402
C645 0.1UF 20% 10V CERM 402
C865 0.1UF 20% 10V CERM 402
C882 0.1UF 20% 10V CERM 402
C708 0.1UF 20% 10V CERM 402
C681 0.1UF 20% 10V CERM 402
C678 0.1UF 20% 10V CERM 402
C682 0.1UF 20% 10V CERM 402
C879 0.1UF 20% 10V CERM 402
C903 0.1UF 20% 10V CERM 402
C673 0.1UF 20% 10V CERM 402
C679 0.1UF 20% 10V CERM 402
C677 0.1UF 20% 10V CERM 402
C660 0.1UF 20% 10V CERM 402
C657 0.1UF 20% 10V CERM 402
C851 0.1UF 20% 10V CERM 402
C875 0.1UF 20% 10V CERM 402
C659 0.1UF 20% 10V CERM 402
C690 0.1UF 20% 10V CERM 402
C658 0.1UF 20% 10V CERM 402
C852 0.1UF 20% 10V CERM 402
C646 0.1UF 20% 10V CERM 402

+1_5V_AGP — INTREPID AGP I/O DECOUPLING

52C3> 46B4<> 17D5< 17A4< 17A3< 16D7< 16C2< 16A8< 10D6< 59C7>

21 Balls
4 X 10UF (0805)
24 X 0.1UF (0402)

C231 10UF N20P80% 10V Y5V 805
C232 10UF N20P80% 10V Y5V 805
C638 10UF N20P80% 10V Y5V 805
C628 10UF N20P80% 10V Y5V 805
C697 0.1UF 20% 10V CERM 402
C693 0.1UF 20% 10V CERM 402
C684 0.1UF 20% 10V CERM 402
C686 0.1UF 20% 10V CERM 402
C709 0.1UF 20% 10V CERM 402
C649 0.1UF 20% 10V CERM 402
C667 0.1UF 20% 10V CERM 402
C694 0.1UF 20% 10V CERM 402
C695 0.1UF 20% 10V CERM 402
C664 0.1UF 20% 10V CERM 402
C733 0.1UF 20% 10V CERM 402
C650 0.1UF 20% 10V CERM 402
C647 0.1UF 20% 10V CERM 402
C710 0.1UF 20% 10V CERM 402
C685 0.1UF 20% 10V CERM 402
C683 0.1UF 20% 10V CERM 402
C665 0.1UF 20% 10V CERM 402
C696 0.1UF 20% 10V CERM 402
C666 0.1UF 20% 10V CERM 402
C651 0.1UF 20% 10V CERM 402
C662 0.1UF 20% 10V CERM 402
C661 0.1UF 20% 10V CERM 402
C648 0.1UF 20% 10V CERM 402
C674 0.1UF 20% 10V CERM 402
C711 0.1UF 20% 10V CERM 402
C663 0.1UF 20% 10V CERM 402

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INTREPID BYPASS

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SCALE: NONE	SHT 11 OF 69	

DRAWING

DDR MUX CONNECTIONS

0-ohm resistors to allow rewiring if necessary

SERIES RESISTORS FOR CONTROL SIGNALS

U25 INTREPID BGA (2 OF 9) SEE_TABLE (ON PAGE 12)

DDR MEMORY INTERFACE

'0'S ARE SAME POLARITY (ACTIVE LO)
'1'S ARE SAME POLARITY (ACTIVE HI)
SEL = 0; HOST=B PORT, A PORT = 100 OHMGND
SEL = 1; HOST=A PORT, B PORT = 100 OHMGND

LOCATE 2 DECOUPLING CAPS DIRECTLY AT DDR_VREF_X BALLS (U25-Y22 & T22)

LOCATE THESE RESISTORS NEAR INTREPID

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INTREPID DDR CNTRL

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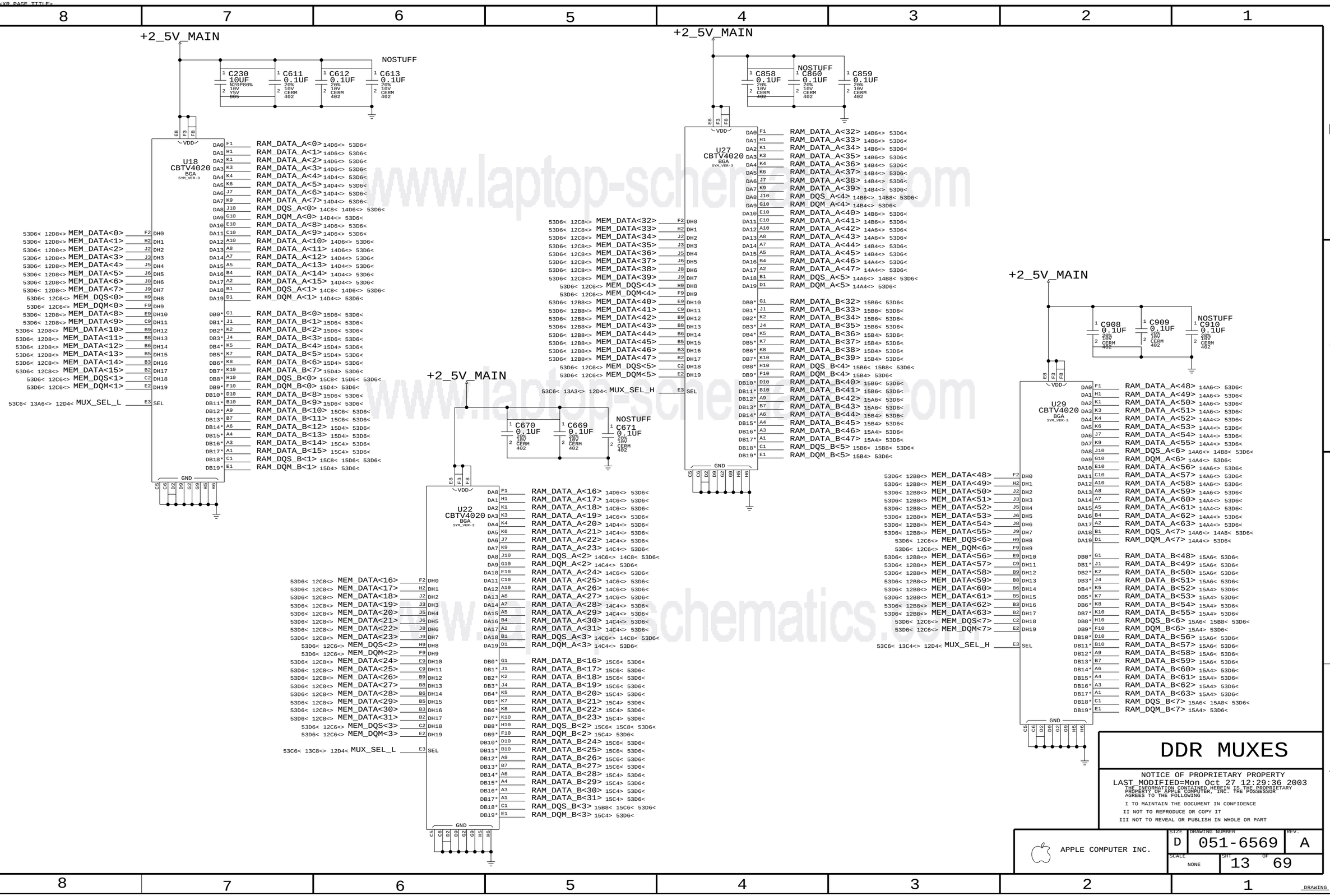
DRAWING


+2_5V_MAIN
C230 10UF N20P80% 10V 10V 805
C611 0.1UF 20% 10V CERM 402
C612 0.1UF 20% 10V CERM 402
C613 0.1UF 20% 10V CERM 402
NOSTUFF
U18 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<0> 14D6<> 53D6<
RAM_DATA_A<1> 14D6<> 53D6<
RAM_DATA_A<2> 14D6<> 53D6<
RAM_DATA_A<3> 14D6<> 53D6<
RAM_DATA_A<4> 14D4<> 53D6<
RAM_DATA_A<5> 14D4<> 53D6<
RAM_DATA_A<6> 14D4<> 53D6<
RAM_DATA_A<7> 14D4<> 53D6<
RAM_DQS_A<0> 14C8< 14D6<> 53D6<
RAM_DQM_A<0> 14D4<> 53D6<
RAM_DATA_A<8> 14D6<> 53D6<
RAM_DATA_A<9> 14D6<> 53D6<
RAM_DATA_A<10> 14D6<> 53D6<
RAM_DATA_A<11> 14D6<> 53D6<
RAM_DATA_A<12> 14D4<> 53D6<
RAM_DATA_A<13> 14D4<> 53D6<
RAM_DATA_A<14> 14D4<> 53D6<
RAM_DATA_A<15> 14D4<> 53D6<
RAM_DQS_A<1> 14C8< 14D6<> 53D6<
RAM_DQM_A<1> 14D4<> 53D6<
MEM_DATA<0> MEM_DATA<1> MEM_DATA<2> MEM_DATA<3> MEM_DATA<4> MEM_DATA<5> MEM_DATA<6> MEM_DATA<7>
MEM_DQS<0> MEM_DQM<0> MEM_DATA<8> MEM_DATA<9> MEM_DATA<10> MEM_DATA<11> MEM_DATA<12> MEM_DATA<13> MEM_DATA<14> MEM_DATA<15>
MEM_DQS<1> MEM_DQM<1> MUX_SEL_L
RAM_DATA_B<0> 15D6< 53D6<
RAM_DATA_B<1> 15D6< 53D6<
RAM_DATA_B<2> 15D6< 53D6<
RAM_DATA_B<3> 15D6< 53D6<
RAM_DATA_B<4> 15D4> 53D6<
RAM_DATA_B<5> 15D4> 53D6<
RAM_DATA_B<6> 15D4> 53D6<
RAM_DATA_B<7> 15D4> 53D6<
RAM_DQS_B<0> 15C8< 15D6< 53D6<
RAM_DQM_B<0> 15D4> 53D6<
RAM_DATA_B<8> 15D6< 53D6<
RAM_DATA_B<9> 15D6< 53D6<
RAM_DATA_B<10> 15C6< 53D6<
RAM_DATA_B<11> 15C6< 53D6<
RAM_DATA_B<12> 15D4> 53D6<
RAM_DATA_B<13> 15D4> 53D6<
RAM_DATA_B<14> 15C4> 53D6<
RAM_DATA_B<15> 15C4> 53D6<
RAM_DQS_B<1> 15C8< 15D6< 53D6<
RAM_DQM_B<1> 15D4> 53D6<
GND
+2_5V_MAIN
C858 0.1UF 20% 10V CERM 402
C860 0.1UF 20% 10V CERM 402
C859 0.1UF 20% 10V CERM 402
NOSTUFF
U27 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<32> 14B6<> 53D6<
RAM_DATA_A<33> 14B6<> 53D6<
RAM_DATA_A<34> 14B6<> 53D6<
RAM_DATA_A<35> 14B6<> 53D6<
RAM_DATA_A<36> 14B4<> 53D6<
RAM_DATA_A<37> 14B4<> 53D6<
RAM_DATA_A<38> 14B4<> 53D6<
RAM_DATA_A<39> 14B4<> 53D6<
RAM_DQS_A<4> 14B6<> 14B8< 53D6<
RAM_DQM_A<4> 14B4<> 53D6<
RAM_DATA_A<40> 14B6<> 53D6<
RAM_DATA_A<41> 14B6<> 53D6<
RAM_DATA_A<42> 14A6<> 53D6<
RAM_DATA_A<43> 14A6<> 53D6<
RAM_DATA_A<44> 14B4<> 53D6<
RAM_DATA_A<45> 14B4<> 53D6<
RAM_DATA_A<46> 14A4<> 53D6<
RAM_DATA_A<47> 14A4<> 53D6<
RAM_DQS_A<5> 14A6<> 14B8< 53D6<
RAM_DQM_A<5> 14A4<> 53D6<
MEM_DATA<32> MEM_DATA<33> MEM_DATA<34> MEM_DATA<35> MEM_DATA<36> MEM_DATA<37> MEM_DATA<38> MEM_DATA<39>
MEM_DQS<4> MEM_DQM<4> MEM_DATA<40> MEM_DATA<41> MEM_DATA<42> MEM_DATA<43> MEM_DATA<44> MEM_DATA<45> MEM_DATA<46> MEM_DATA<47>
MEM_DQS<5> MEM_DQM<5> MUX_SEL_H
RAM_DATA_B<32> 15B6< 53D6<
RAM_DATA_B<33> 15B6< 53D6<
RAM_DATA_B<34> 15B6< 53D6<
RAM_DATA_B<35> 15B6< 53D6<
RAM_DATA_B<36> 15B4> 53D6<
RAM_DATA_B<37> 15B4> 53D6<
RAM_DATA_B<38> 15B4> 53D6<
RAM_DATA_B<39> 15B4> 53D6<
RAM_DQS_B<4> 15B6< 15B8< 53D6<
RAM_DQM_B<4> 15B4> 53D6<
RAM_DATA_B<40> 15B6< 53D6<
RAM_DATA_B<41> 15B6< 53D6<
RAM_DATA_B<42> 15A6< 53D6<
RAM_DATA_B<43> 15A6< 53D6<
RAM_DATA_B<44> 15B4> 53D6<
RAM_DATA_B<45> 15B4> 53D6<
RAM_DATA_B<46> 15A4> 53D6<
RAM_DATA_B<47> 15A4> 53D6<
RAM_DQS_B<5> 15B6< 15B8< 53D6<
RAM_DQM_B<5> 15B4> 53D6<
MEM_DATA<48> MEM_DATA<49> MEM_DATA<50> MEM_DATA<51> MEM_DATA<52> MEM_DATA<53> MEM_DATA<54> MEM_DATA<55> MEM_DATA<56> MEM_DATA<57> MEM_DATA<58> MEM_DATA<59> MEM_DATA<60> MEM_DATA<61> MEM_DATA<62> MEM_DATA<63>
MEM_DQS<6> MEM_DQM<6> MEM_DQS<7> MEM_DQM<7> MUX_SEL_H
+2_5V_MAIN
C908 0.1UF 20% 10V CERM 402
C909 0.1UF 20% 10V CERM 402
C910 0.1UF 20% 10V CERM 402
NOSTUFF
U29 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<48> 14A6<> 53D6<
RAM_DATA_A<49> 14A6<> 53D6<
RAM_DATA_A<50> 14A6<> 53D6<
RAM_DATA_A<51> 14A6<> 53D6<
RAM_DATA_A<52> 14A4<> 53D6<
RAM_DATA_A<53> 14A4<> 53D6<
RAM_DATA_A<54> 14A4<> 53D6<
RAM_DATA_A<55> 14A4<> 53D6<
RAM_DQS_A<6> 14A6<> 14B8< 53D6<
RAM_DQM_A<6> 14A4<> 53D6<
RAM_DATA_A<56> 14A6<> 53D6<
RAM_DATA_A<57> 14A6<> 53D6<
RAM_DATA_A<58> 14A6<> 53D6<
RAM_DATA_A<59> 14A6<> 53D6<
RAM_DATA_A<60> 14A4<> 53D6<
RAM_DATA_A<61> 14A4<> 53D6<
RAM_DATA_A<62> 14A4<> 53D6<
RAM_DATA_A<63> 14A4<> 53D6<
RAM_DQS_A<7> 14A6<> 14A8< 53D6<
RAM_DQM_A<7> 14A4<> 53D6<
RAM_DATA_B<48> 15A6< 53D6<
RAM_DATA_B<49> 15A6< 53D6<
RAM_DATA_B<50> 15A6< 53D6<
RAM_DATA_B<51> 15A6< 53D6<
RAM_DATA_B<52> 15A4> 53D6<
RAM_DATA_B<53> 15A4> 53D6<
RAM_DATA_B<54> 15A4> 53D6<
RAM_DATA_B<55> 15A4> 53D6<
RAM_DQS_B<6> 15A6< 15B8< 53D6<
RAM_DQM_B<6> 15A4> 53D6<
RAM_DATA_B<56> 15A6< 53D6<
RAM_DATA_B<57> 15A6< 53D6<
RAM_DATA_B<58> 15A6< 53D6<
RAM_DATA_B<59> 15A6< 53D6<
RAM_DATA_B<60> 15A4> 53D6<
RAM_DATA_B<61> 15A4> 53D6<
RAM_DATA_B<62> 15A4> 53D6<
RAM_DATA_B<63> 15A4> 53D6<
RAM_DQS_B<7> 15A6< 15A8< 53D6<
RAM_DQM_B<7> 15A4> 53D6<
+2_5V_MAIN
C670 0.1UF 20% 10V CERM 402
C669 0.1UF 20% 10V CERM 402
C671 0.1UF 20% 10V CERM 402
NOSTUFF
U22 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<16> 14C6<> 53D6<
RAM_DATA_A<17> 14C6<> 53D6<
RAM_DATA_A<18> 14C6<> 53D6<
RAM_DATA_A<19> 14C6<> 53D6<
RAM_DATA_A<20> 14D4<> 53D6<
RAM_DATA_A<21> 14C4<> 53D6<
RAM_DATA_A<22> 14C4<> 53D6<
RAM_DATA_A<23> 14C4<> 53D6<
RAM_DQS_A<2> 14C6<> 14C8< 53D6<
RAM_DQM_A<2> 14C4<> 53D6<
RAM_DATA_A<24> 14C6<> 53D6<
RAM_DATA_A<25> 14C6<> 53D6<
RAM_DATA_A<26> 14C6<> 53D6<
RAM_DATA_A<27> 14C6<> 53D6<
RAM_DATA_A<28> 14C4<> 53D6<
RAM_DATA_A<29> 14C4<> 53D6<
RAM_DATA_A<30> 14C4<> 53D6<
RAM_DATA_A<31> 14C4<> 53D6<
RAM_DQS_A<3> 14C6<> 14C8< 53D6<
RAM_DQM_A<3> 14C4<> 53D6<
MEM_DATA<16> MEM_DATA<17> MEM_DATA<18> MEM_DATA<19> MEM_DATA<20> MEM_DATA<21> MEM_DATA<22> MEM_DATA<23>
MEM_DQS<2> MEM_DQM<2> MEM_DATA<24> MEM_DATA<25> MEM_DATA<26> MEM_DATA<27> MEM_DATA<28> MEM_DATA<29> MEM_DATA<30> MEM_DATA<31>
MEM_DQS<3> MEM_DQM<3> MUX_SEL_L
RAM_DATA_B<16> 15C6< 53D6<
RAM_DATA_B<17> 15C6< 53D6<
RAM_DATA_B<18> 15C6< 53D6<
RAM_DATA_B<19> 15C6< 53D6<
RAM_DATA_B<20> 15C4> 53D6<
RAM_DATA_B<21> 15C4> 53D6<
RAM_DATA_B<22> 15C4> 53D6<
RAM_DATA_B<23> 15C4> 53D6<
RAM_DQS_B<2> 15C6< 15C8< 53D6<
RAM_DQM_B<2> 15C4> 53D6<
RAM_DATA_B<24> 15C6< 53D6<
RAM_DATA_B<25> 15C6< 53D6<
RAM_DATA_B<26> 15C6< 53D6<
RAM_DATA_B<27> 15C6< 53D6<
RAM_DATA_B<28> 15C4> 53D6<
RAM_DATA_B<29> 15C4> 53D6<
RAM_DATA_B<30> 15C4> 53D6<
RAM_DATA_B<31> 15C4> 53D6<
RAM_DQS_B<3> 15B8< 15C6< 53D6<
RAM_DQM_B<3> 15C4> 53D6<
DDR MUXES
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+2_5V_MAIN

DISTRIBUTE THESE TWO CAPS
ALONG VREF TRACE

LOCATE C1601 AND C1401
DIRECTLY ON PIN AT J26-1

15D8< 12A7< 14D2<> 52A6> DDR_VREF

C1401 0.1UF 20% 10V CERM 402

C46 0.1UF 20% 10V CERM 402 NOSTUFF

C47 0.1UF 20% 10V CERM 402 NOSTUFF

C1601 0.1UF 20% 10V CERM 402

+2_5V_MAIN

NOSTUFF R1403 470 5% 1/16W MF 402
53D6< 14D6<> 13D7<> RAM_DQS_A<0>

NOSTUFF R1404 470 5% 1/16W MF 402

NOSTUFF R1405 470 5% 1/16W MF 402
53D6< 14D6<> 13C7<> RAM_DQS_A<1>

NOSTUFF R1406 470 5% 1/16W MF 402

NOSTUFF R1407 470 5% 1/16W MF 402
53D6< 14C6<> 13B5<> RAM_DQS_A<2>

NOSTUFF R1408 470 5% 1/16W MF 402

NOSTUFF R1409 470 5% 1/16W MF 402
53D6< 14C6<> 13B5<> RAM_DQS_A<3>

NOSTUFF R1410 470 5% 1/16W MF 402

NOSTUFF R1411 470 5% 1/16W MF 402
53D6< 14B6<> 13D4<> RAM_DQS_A<4>

NOSTUFF R1412 470 5% 1/16W MF 402

NOSTUFF R1413 470 5% 1/16W MF 402
53D6< 14A6<> 13C4<> RAM_DQS_A<5>

NOSTUFF R1414 470 5% 1/16W MF 402

NOSTUFF R1415 470 5% 1/16W MF 402
53D6< 14A6<> 13B2<> RAM_DQS_A<6>

NOSTUFF R1416 470 5% 1/16W MF 402

NOSTUFF R1417 470 5% 1/16W MF 402
53D6< 14A6<> 13B2<> RAM_DQS_A<7>

NOSTUFF R1418 470 5% 1/16W MF 402

+3V_MAIN

C319 10UF N20P80% 10V Y5V 805

C929 0.1UF 20% 10V CERM 402

+2_5V_MAIN

NC_SODIMM201 NO_TEST

J26 AS0A42-D2R F-RT-SM

MIN_LINE_WIDTH=20

53D6< 13D7<>	RAM_DATA_A<0>	53D6< 13D7<>	RAM_DATA_A<4>
53D6< 13D7<>	RAM_DATA_A<1>	53D6< 13D7<>	RAM_DATA_A<5>
53D6< 14C8< 13D7<>	RAM_DQS_A<0>	53D6< 13D7<>	RAM_DQM_A<0>
53D6< 13D7<>	RAM_DATA_A<2>	53D6< 13D7<>	RAM_DATA_A<6>
53D6< 13D7<>	RAM_DATA_A<3>	53D6< 13C7<>	RAM_DATA_A<7>
53D6< 13C7<>	RAM_DATA_A<8>	53D6< 13C7<>	RAM_DATA_A<12>
53D6< 13C7<>	RAM_DATA_A<9>	53D6< 13C7<>	RAM_DATA_A<13>
53D6< 14C8< 13C7<>	RAM_DQS_A<1>	53D6< 13C7<>	RAM_DQM_A<1>
53D6< 13C7<>	RAM_DATA_A<10>	53D6< 13C7<>	RAM_DATA_A<14>
53D6< 13C7<>	RAM_DATA_A<11>	53D6< 13C7<>	RAM_DATA_A<15>
53C6< 12C4<	SYSCLK_DDRCLK_A0		
53C6< 12C4<	SYSCLK_DDRCLK_A0_L		
53D6< 13B5<>	RAM_DATA_A<16>	53D6< 13B5<>	RAM_DATA_A<20>
53D6< 13B5<>	RAM_DATA_A<17>	53D6< 13B5<>	RAM_DATA_A<21>
53D6< 14C8< 13B5<>	RAM_DQS_A<2>	53D6< 13B5<>	RAM_DQM_A<2>
53D6< 13B5<>	RAM_DATA_A<18>	53D6< 13B5<>	RAM_DATA_A<22>
53D6< 13B5<>	RAM_DATA_A<19>	53D6< 13B5<>	RAM_DATA_A<23>
53D6< 13B5<>	RAM_DATA_A<24>	53D6< 13B5<>	RAM_DATA_A<28>
53D6< 13B5<>	RAM_DATA_A<25>	53D6< 13B5<>	RAM_DATA_A<29>
53D6< 14C8< 13B5<>	RAM_DQS_A<3>	53D6< 13A5<>	RAM_DQM_A<3>
53D6< 13B5<>	RAM_DATA_A<26>	53D6< 13B5<>	RAM_DATA_A<30>
53D6< 13B5<>	RAM_DATA_A<27>	53D6< 13B5<>	RAM_DATA_A<31>
NC_SODIMM71	NO_TEST	NC_SODIMM72	NO_TEST
NC_SODIMM73	NO_TEST	NC_SODIMM74	NO_TEST
NC_SODIMM77	NO_TEST	NC_SODIMM78	NO_TEST
NC_SODIMM79	NO_TEST	NC_SODIMM80	NO_TEST
NC_SODIMM83	NO_TEST	NC_SODIMM84	NO_TEST
NC_SODIMM85	NO_TEST	NC_SODIMM86	NO_TEST
NC_SODIMM89	NO_TEST		
NC_SODIMM91	NO_TEST		
53C6< 15C1< 12B1<	RAM_CKE<1>	RAM_CKE<0>	12C1< 15C1< 53C6>
NC_SODIMM97	NO_TEST	NC_SODIMM98	NO_TEST
53D6< 15C4> 12D1<	RAM_ADDR<12>	RAM_ADDR<11>	12B3< 15C4> 53D6>
53D6< 15C6< 12C3<	RAM_ADDR<9>	RAM_ADDR<8>	12D1< 15C4> 53D6>
53D6< 15C6< 12D3<	RAM_ADDR<7>	RAM_ADDR<6>	12D1< 15C4> 53D6>
53D6< 15C6< 12C1<	RAM_ADDR<5>	RAM_ADDR<4>	12D3< 15C6< 53D6>
53D6< 15C4< 12D3<	RAM_ADDR<3>	RAM_ADDR<2>	12C3< 15C6< 53D6>
53D6< 15B6< 12C3<	RAM_ADDR<1>	RAM_ADDR<0>	12C3< 15B6< 53D6>
53D6< 15B4> 12C3<	RAM_ADDR<10>	RAM_BA<1>	12B3< 15B6< 53D6>
53D6< 15B6< 12B3<	RAM_BA<0>	RAM_RAS_L	12A2< 15B4> 53C6>
53C6< 15B6< 12B3<	RAM_WE_L	RAM_CAS_L	12A2< 15B6< 53C6>
53C6< 12C1<	RAM_CS_L<0>	RAM_CS_L<1>	12C1< 53C6>
NC_SODIMM123	NO_TEST	NC_SODIMM124	NO_TEST
53D6< 13D4<>	RAM_DATA_A<32>	53D6< 13D4<>	RAM_DATA_A<36>
53D6< 13D4<>	RAM_DATA_A<33>	53D6< 13D4<>	RAM_DATA_A<37>
53D6< 14B8< 13D4<>	RAM_DQS_A<4>	53D6< 13D4<>	RAM_DQM_A<4>
53D6< 13D4<>	RAM_DATA_A<34>	53D6< 13D4<>	RAM_DATA_A<38>
53D6< 13D4<>	RAM_DATA_A<35>	53D6< 13D4<>	RAM_DATA_A<39>
53D6< 13D4<>	RAM_DATA_A<40>	53D6< 13C4<>	RAM_DATA_A<44>
53D6< 13C4<>	RAM_DATA_A<41>	53D6< 13C4<>	RAM_DATA_A<45>
53D6< 14B8< 13C4<>	RAM_DQS_A<5>	53D6< 13C4<>	RAM_DQM_A<5>
53D6< 13C4<>	RAM_DATA_A<42>	53D6< 13C4<>	RAM_DATA_A<46>
53D6< 13C4<>	RAM_DATA_A<43>	53D6< 13C4<>	RAM_DATA_A<47>
		SYSCLK_DDRCLK_A1_L	12B4< 53C6<
		SYSCLK_DDRCLK_A1	12C4< 53C6<
53D6< 13C2<>	RAM_DATA_A<48>	53D6< 13C2<>	RAM_DATA_A<52>
53D6< 13C2<>	RAM_DATA_A<49>	53D6< 13C2<>	RAM_DATA_A<53>
53D6< 14B8< 13B2<>	RAM_DQS_A<6>	53D6< 13B2<>	RAM_DQM_A<6>
53D6< 13C2<>	RAM_DATA_A<50>	53D6< 13B2<>	RAM_DATA_A<54>
53D6< 13C2<>	RAM_DATA_A<51>	53D6< 13B2<>	RAM_DATA_A<55>
53D6< 13B2<>	RAM_DATA_A<56>	53D6< 13B2<>	RAM_DATA_A<60>
53D6< 13B2<>	RAM_DATA_A<57>	53D6< 13B2<>	RAM_DATA_A<61>
53D6< 14A8< 13B2<>	RAM_DQS_A<7>	53D6< 13B2<>	RAM_DQM_A<7>
53D6< 13B2<>	RAM_DATA_A<58>	53D6< 13B2<>	RAM_DATA_A<62>
53D6< 13B2<>	RAM_DATA_A<59>	53D6< 13B2<>	RAM_DATA_A<63>
34B3< 15A6<	INT_I2C_DATA0		
34B3< 15A6<	INT_I2C_CLK0		
NC_SODIMM199	NO_TEST		
NC_SODIMM202	NO_TEST		

ADDR=0 (0xA0)

(516S0029)

+2_5V_MAIN

C1602 0.1UF 20% 10V CERM 402

C1402 0.1UF 20% 10V CERM 402

DDR_VREF 12A7< 14D8<> 15D8< 52A6>

LOCATE C1602 AND C1402
DIRECTLY ON PIN AT J26-2

DDR DECOUPLING
SLOT "A"

+2_5V_MAIN

1 - 10UF
24 - 0.1UF

C244 0.1UF 20% 10V CERM 402
C263 0.1UF 20% 10V CERM 402
C320 0.1UF 20% 10V CERM 402
C243 0.1UF 20% 10V CERM 402
C255 0.1UF 20% 10V CERM 402
C256 0.1UF 20% 10V CERM 402
C1403 0.1UF 20% 10V CERM 402
C1404 0.1UF 20% 10V CERM 402

C313 0.1UF 20% 10V CERM 402
C242 0.1UF 20% 10V CERM 402
C275 0.1UF 20% 10V CERM 402
C276 0.1UF 20% 10V CERM 402
C304 0.1UF 20% 10V CERM 402
C261 0.1UF 20% 10V CERM 402
C311 0.1UF 20% 10V CERM 402
C1405 0.1UF 20% 10V CERM 402

C1406 0.1UF 20% 10V CERM 402
C1407 0.1UF 20% 10V CERM 402
C1408 0.1UF 20% 10V CERM 402
C1409 0.1UF 20% 10V CERM 402
C1410 0.1UF 20% 10V CERM 402
C1411 0.1UF 20% 10V CERM 402
C1412 0.1UF 20% 10V CERM 402
C1413 0.1UF 20% 10V CERM 402

C1415 0.1UF 20% 10V CERM 402
C1416 0.1UF 20% 10V CERM 402
C1417 0.1UF 20% 10V CERM 402
C1418 0.1UF 20% 10V CERM 402
C1419 0.1UF 20% 10V CERM 402
C1420 0.1UF 20% 10V CERM 402
C1421 0.1UF 20% 10V CERM 402

+2_5V_MAIN

C1414 10UF N20P80% 10V Y5V 805

+2_5V_MAIN

R1401 100 1% 1/16W MF 402

MIN_LINE_WIDTH=25

INT_MEM_VREF 12A8<>

LOCATE THESE RESISTORS BETWEEN DIMMS

R1402 100 1% 1/16W MF 402

SO-DIMM SLOT A

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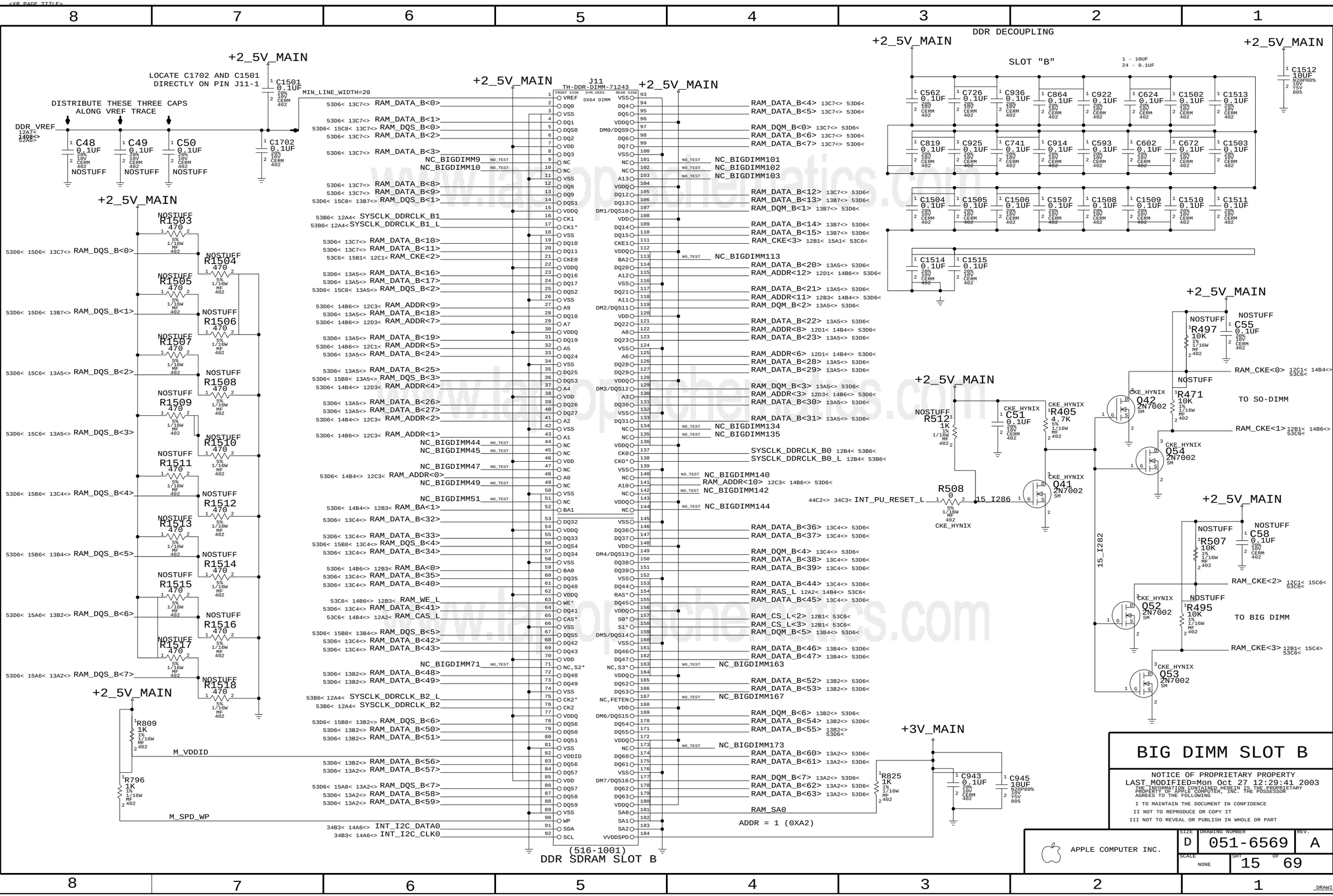

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INTREPID AGP CLK IS 1.5V OUT
NEED 3.3V SWING FOR VIDEO CHIPS
VERSION 1 WORKAROUND IS LA CLOCK
VERSION 2 WORKAROUND IS UNUSED PIN

52D3> 30D5< 28D6<> 9D4< +1_5V_INTREPID_PLL
R667 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL5 52D3>
C760 0.1UF 20% 10V CERM 402
C1801 0.1UF 20% 10V CERM 402
INT_PLL5_GND 16A5<>

52C3> 46B4<> 17D5< 17A4< 17A3< 16C2< 16A8< 11A6< 10D6< 59C7> +1_5V_AGP
R619 60.4 1% 1/16W MF 402
54A7< 30C5<> 30A7< INT_ROM_OVERLAY_PU
54A7< 17C6< CLK66M_GPU_AGP
R225 22 5% 1/16W MF 402 (INT_V2)
R226 0 5% 1/16W MF 402 (INT_V1)
THESE RESISTORS SHARE THE SAME PAD
R224 22 5% 1/16W MF 402 NOSTUFF
54B7< 17A8< 16D3< STOP_AGP_L
INT_AGPPVT
52C3> 16A7< INT_AGP_VREF
INT_ANALYZER_CLK 8A2< 9B4< 54A7< 56B3> 59A7>
54B7< 17A8< 16D3< 16D1< AGP_BUSY_L
54A7< CLK66M_GPU_UF
54A7< INT_AGP_FB_IN
54A7< INT_AGP_FB_OUT

V14 VDD15A_5 (PLL5)

U25 INTREPID BGA (3 OF 9) SEE_TABLE (ON PAGE 12)

AN19	STP_AGP	
AJ24	AGPPVT	
AB20	AGPVREF0	
AB21	AGPVREF1	
AT19	AGP_BUSY	
AK28	AGP_CLK	
AK27	AGP_FB_IN	
AK25	AGP_FB_OUT	

2" LONGER (0.5NS SLOWER) AGP (ZERO DELAY) 2" SHORTER (0.5NS FASTER)

AGP_FBI_EQUAL 54A7<
R203 0 NOSTUFF
R215 0 NOSTUFF
R211 0 NOSTUFF
R220 0 NOSTUFF
R622 0 NOSTUFF
54A7< AGP_FB_PLUS2
R204 0 NOSTUFF
R216 0 NOSTUFF
AGP_FBO_EQUAL 54A7<
PLACE ALL SERPENTINES ON INTERNAL LAYER

AGP INTERFACES

VOUT = AGPIO (1.5V)
VIN = VCORE (1.5V)

AT33	AGPREQ	AGP_REQ_L 16C3< 17B6<> 54B7<
AM29	AGPGNT	AGP_GNT_L 16C3< 17B6< 54B7<
AR19	AGPAD0	AGP_AD<0> 17D8< 54C7<
AM19	AGPAD1	AGP_AD<1> 17D8< 54C7<
AT20	AGPAD2	AGP_AD<2> 17D8< 54C7<
AR20	AGPAD3	AGP_AD<3> 17D8< 54C7<
AT21	AGPAD4	AGP_AD<4> 17D8< 54C7<
AN20	AGPAD5	AGP_AD<5> 17D8< 54C7<
AR21	AGPAD6	AGP_AD<6> 17D8< 54C7<
AN21	AGPAD7	AGP_AD<7> 17D8< 54C7<
AM21	AGPAD8	AGP_AD<8> 17D8< 54C7<
AT22	AGPAD9	AGP_AD<9> 17D8< 54C7<
AR22	AGPAD10	AGP_AD<10> 17D8< 54C7<
AN22	AGPAD11	AGP_AD<11> 17D8< 54C7<
AM22	AGPAD12	AGP_AD<12> 17D8< 54C7<
AN23	AGPAD13	AGP_AD<13> 17D8< 54C7<
AR23	AGPAD14	AGP_AD<14> 17D8< 54C7<
AT24	AGPAD15	AGP_AD<15> 17C8< 54C7<
AM23	AGPAD16	AGP_AD<16> 17C8< 54C7<
AR24	AGPAD17	AGP_AD<17> 17C8< 54C7<
AT25	AGPAD18	AGP_AD<18> 17C8< 54C7<
AR25	AGPAD19	AGP_AD<19> 17C8< 54C7<
AM24	AGPAD20	AGP_AD<20> 17C8< 54C7<
AN25	AGPAD21	AGP_AD<21> 17C8< 54C7<
AL24	AGPAD22	AGP_AD<22> 17C8< 54C7<
AR26	AGPAD23	AGP_AD<23> 17C8< 54C7<
AT26	AGPAD24	AGP_AD<24> 17C8< 54C7<
AM25	AGPAD25	AGP_AD<25> 17C8< 54C7<
AN26	AGPAD26	AGP_AD<26> 17C8< 54C7<
AM26	AGPAD27	AGP_AD<27> 17C8< 54C7<
AR27	AGPAD28	AGP_AD<28> 17C8< 54C7<
AT27	AGPAD29	AGP_AD<29> 17C8< 54C7<
AR28	AGPAD30	AGP_AD<30> 17C8< 54C7<
AN27	AGPAD31	AGP_AD<31> 17C8< 54C7<
AM20	AGPCBE_0	AGP_CBE<0> 17C8< 54C7<
AT23	AGPCBE_1	AGP_CBE<1> 17C8< 54C7<
AN24	AGPCBE_2	AGP_CBE<2> 17C8< 54C7<
AL25	AGPCBE_3	AGP_CBE<3> 17C8< 54C7<
AT29	AGPPAR	AGP_PAR 17B8< 54B7<
AN28	AGPFRAME	AGP_FRAME_L 16C3< 17B8< 54C7<
AR29	AGPTRDY	AGP_TRDY_L 16B3< 17B8< 54C7<
AT28	AGPIRDY	AGP_IRDY_L 16C3< 17B8< 54C7< 54C7< 17B8< 16A4<> AGP_AD_STB<0>
AM28	AGPSTOP	AGP_STOP_L 16B3< 17B8< 54C7<
AM27	AGPDEVSEL	AGP_DEVSEL_L 16C3< 17B8< 54C7<
AT32	AGP_SBA0	AGP_SBA<0> 16C1< 17A8< 54B7< 54C7< 17B8< 16A4<> AGP_AD_STB<1>
AR32	AGP_SBA1	AGP_SBA<1> 16C1< 17A8< 54B7<
AM31	AGP_SBA2	AGP_SBA<2> 16B1< 17A8< 54B7<
AN31	AGP_SBA3	AGP_SBA<3> 16C1< 17A8< 54B7<
AR31	AGP_SBA4	AGP_SBA<4> 16C1< 17A8< 54B7<
AT31	AGP_SBA5	AGP_SBA<5> 16C1< 17A8< 54B7<
AM30	AGP_SBA6	AGP_SBA<6> 16B1< 17A8< 54B7<
AN30	AGP_SBA7	AGP_SBA<7> 16B1< 17A8< 54B7<
AH25	AGP_SB_STB_P	AGP_SB_STB 16B3< 17B8< 54B7<
AG25	AGP_SB_STB_N	AGP_SB_STB_L 16D1< 17A8< 54B7<
AN29	AGP_ST0	AGP_ST<0> 16B1< 17B6< 54B7<
AT30	AGP_ST1	AGP_ST<1> 16B1< 17B6< 54B7<
AR30	AGP_ST2	AGP_ST<2> 16B1< 17B6< 54B7<
AK20	AGP_AD_STB0_P	AGP_AD_STB<0> 16B3< 17B8< 54C7<
AK19	AGP_AD_STB0_N	AGP_AD_STB_L<0> 16D1< 17B8< 54C7<
AK21	AGP_AD_STB1_P	AGP_AD_STB<1> 16B3< 17B8< 54C7<
AK22	AGP_AD_STB1_N	AGP_AD_STB_L<1> 16D1< 17B8< 54C7<
AJ29	AGPPIPE	AGP_PIPE_L 16B3< 17B8< 54B7<
AK24	AGPRBF	AGP_RBF_L 16B3< 17B8< 54B7<

54B7< 17B8< 16B1< AGP_WBF_L — AK30 — AGP_WBF

VSSA_5 (PLL5) V13
NO_TEST INT_PLL5_GND 16D5<
OMIT XW48 SM

AGP PULL-UPS/PULL DOWNS

+3V_MAIN
54B7< 17A8< 16D1< 16C6<> AGP_BUSY_L
R222 10K 1% 1/16W MF 402
54B7< 17A8< 16C6<> STOP_AGP_L
R217 10K 1% 1/16W MF 402

52C3> 46B4<> 17D5< 17A4< 17A3< 16D7< 16A8< 11A6< 10D6< 59C7> +1_5V_AGP

54B7< 17B6<> 16C4<>	AGP_REQ_L	RP37 10K
54B7< 17B6< 16C4<>	AGP_GNT_L	RP37 10K
54C7< 17B8< 16B4<>	AGP_FRAME_L	RP37 10K
54C7< 17B8< 16B4<>	AGP_DEVSEL_L	RP98 10K
54C7< 17B8< 16B4<>	AGP_IRDY_L	RP98 10K
54C7< 17B8< 16B4<>	AGP_TRDY_L	RP98 10K
54C7< 17B8< 16B4<>	AGP_STOP_L	RP98 10K
54B7< 17B8< 16A4<>	AGP_RBF_L	RP37 10K
NC_RP1PIN4		RP48 10K NO_TEST
54B7< 17B8< 16A4<>	AGP_PIPE_L	RP48 10K
54B7< 17B8< 16A4<>	AGP_AD_STB<0>	R580 10K 1% 1/16W MF 402
54C7< 17B8< 16A4<>	AGP_AD_STB<1>	R587 10K 1% 1/16W MF 402
54B7< 17B8< 16A4<>	AGP_SB_STB	R233 10K 1% 1/16W MF 402

54C7< 17B8< 16A4<>	AGP_AD_STB_L<0>	R223 10K
54C7< 17B8< 16A4<>	AGP_AD_STB_L<1>	R234 10K
54B7< 17A8< 16A4<>	AGP_SB_STB_L	R221 10K
54B7< 17A8< 16D3< 16C6<>	AGP_BUSY_L	R161 10K NOSTUFF

54B7< 17A8< 16B4<>	AGP_SBA<5>	RP99 10K
54B7< 17A8< 16B4<>	AGP_SBA<1>	RP99 10K
54B7< 17A8< 16B4<>	AGP_SBA<4>	RP99 10K
54B7< 17A8< 16B4<	AGP_SBA<0>	RP99 10K
54B7< 17A8< 16B4<	AGP_SBA<3>	RP49 10K
54B7< 17A8< 16A4<>	AGP_SBA<7>	RP49 10K
54B7< 17B6< 16A4<>	AGP_ST<1>	RP49 10K
54B7< 17B6< 16A4<>	AGP_ST<2>	RP49 10K
54B7< 17A8< 16B4<>	AGP_SBA<2>	RP50 10K
54B7< 17A8< 16A4<>	AGP_SBA<6>	RP50 10K
54B7< 17B8< 16A6<	AGP_WBF_L	RP50 10K
54B7< 17B6< 16A4<>	AGP_ST<0>	RP50 10K

GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)

59C7> 52C3> 46B4<> 16D7< 16C2< 11A6< 10D6< 17D5< 17A4< 17A3< +1_5V_AGP
C603 470PF 10% 50V CERM 402
GPU_AGP_VREF_H
R549 4.99K 1% 1/16W MF 402
R545 82.5 1% 1/16W MF 402
INT_AGP_VREF 16C6<> 52C3>
R205 4.99K 1% 1/16W MF 402
R197 82.5 1% 1/16W MF 402
C1802 0.1UF 20% 10V CERM 402
C222 470PF 10% 50V CERM 402
GPU_AGP_VREF_L

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INTREPID AGP

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 16 OF 69	

DRAWING

U39
NV18B
BGA
(1 OF 5)

+1_5V_AGP

AGP_AD<0> AGP_AD<1> AGP_AD<2> AGP_AD<3> AGP_AD<7> AGP_AD<5> AGP_AD<6> AGP_AD<4> AGP_AD<8> AGP_AD<9> AGP_AD<10> AGP_AD<11> AGP_AD<12> AGP_AD<13> AGP_AD<14> AGP_AD<15> AGP_AD<16> AGP_AD<18> AGP_AD<17> AGP_AD<19> AGP_AD<20> AGP_AD<21> AGP_AD<22> AGP_AD<23> AGP_AD<24> AGP_AD<25> AGP_AD<26> AGP_AD<27> AGP_AD<28> AGP_AD<29> AGP_AD<30> AGP_AD<31>

RP40 RP30 RP32 RP42 RP31 RP41 RP44 RP34 22 5% 1/16W SM1

GPU_AGP_AD<0> AJ28 … GPU_AGP_AD<31> AE18

PCIAD0 … PCIAD31

AGP_CBE<0> AGP_CBE<3> AGP_CBE<2> AGP_CBE<1>

RP43 22 5% 1/16W SM1

GPU_AGP_CBE<0> AJ24 … GPU_AGP_CBE<3> AB22

PCIC0/BE0* : C0*/BE0
PCIC1/BE1* : C1*/BE1
PCIC2/BE2* : C2*/BE2
PCIC3/BE3* : C3*/BE3

MAIN_RESET_L — R1026 0 402 5%

AGP_RESET_L — R1027 0 402 5% TMDS_XMIT_SI_P

CLK66M_GPU_AGP — AG12
NV_PCI_RST_L — AF15

PCICLK : CLK
PCIRST* : RST*

AGP_GNT_L — AE15
AGP_REQ_L — AF13

PCIGNT* : GNT
PCIREQ* : REQ

AGP_TRDY_L AGP_FRAME_L AGP_IRDY_L AGP_PAR AGP_STOP_L AGP_DEVSEL_L

RP45 RP35 22 5% 1/16W SM1

GPU_AGP_FRAME_L AK16 … GPU_AGP_DEVSEL_L AJ16

PCIFRAME* : FRAME
PCIIRDY* : IRDY
PCITRDY* : TRDY
PCIDEVSEL* : DEVSEL
PCISTOP* : STOP
PCIPAR : PAR

AGP_INT_L — AG15
NC_GPU_INTB_L — AE10

PCIINTA* : INTA
NC_PCIINTB* : INTB

AGP_WBF_L AGP_PIPE_L AGP_RBF_L

RP46 22 5% 1/16W SM1

GPU_AGP_RBF_L AG14 … NC_GPU_DBI_LO AJ19

AGPRBF* : RBF
AGPWBF* : WBF
AGPPIPE* : DBI_HI
<RESRVD> : DBI_LO

AGP_ST<0> AGP_ST<1> AGP_ST<2>

AGPST0 : ST0
AGPST1 : ST1
AGPST2 : ST2

AGP_AD_STB<0> AGP_AD_STB_L<0> AGP_AD_STB_L<1> AGP_AD_STB<1>

RP33 22 5% 1/16W SM1

GPU_AGP_AD_STB_GPUUF<0> AK24 … GPU_AGP_AD_STB_GPUUF<1> AF21

AGPADSTBF0 : ADSTBF0
AGPADSTBS0* : ADSTBS0
AGPADSTBF1 : ADSTBF1
AGPADSTBS1* : ADSTBS1

AGP_SB_STB — R210 22 — R558 22 — GPU_AGP_SB_STB AK13
AGP_SB_STB_L — GPU_AGP_SB_STB_L AJ13

AGPSBSTBF : SBSTBF
AGPSBSTBS* : SBSTBS

AGP_SBA<3> AGP_SBA<2> AGP_SBA<1> AGP_SBA<0> AGP_SBA<7> AGP_SBA<6> AGP_SBA<4> AGP_SBA<5>

RP47 RP36 22 5% 1/16W SM1

GPU_AGP_SBA<0> AJ11 … GPU_AGP_SBA<7> AH15

AGPSBA0 : SBA0*
AGPSBA1 : SBA1*
AGPSBA2 : SBA2*
AGPSBA3 : SBA3*
AGPSBA4 : SBA4*
AGPSBA5 : SBA5*
AGPSBA6 : SBA6*
AGPSBA7 : SBA7*

GPU_MBDET_L — AF16

<RESRVD> : MBDET*

AGP_BUSY_L — AF12
STOP_AGP_L — AG11

AGPBUSY* : BUSY*
AGPSTOP* : STOP*

GPU_AGP_VREF — AK29

AGPVREF : AGPVREF

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

+3V_MAIN — R168 10K 1% 1/16W MF 402

NC_GPU<0> NC_GPU<1> NC_GPU<2> NC_GPU<3> NC_GPU<4> — ALL ARE NO_TEST

AGPVDDQ: AE14 AE11 AE17 AE20 AE23 AD11 AD14 AD23 AD20 AD17

VDD: AA17 AA18 L20 Y20 L13 Y13 N20 P20 U20 V20 L11 N11 P11 U11 V11 Y11 L14 Y14 L17 Y17 L18 Y18

VDD33: H6 AC6 U7 G14 U6 AD15 H7 AD16 AD19 AD22 AC7 AD12 P24

VD50CLAMP0 N4
VD50CLAMP1 AE9
AGP_PLLVDD AE12

50 OHM TO VDDQ — AGPCALPD AA13
50 OHM TO GND — AGPCALPU AA14

10K OHM TO GND — TESTMODE AE5 — GPU_TMODE 52A8>

R177 10K 1% 1/16W MF 402
R160 49.9 1% 1/16W MF 402
R169 49.9 1% 1/16W MF 402

+1_5V_AGP 10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17D5< 46B4<> 52C3> 59C7>

+5V_MAIN
C193 0.1UF 20% 10V CERM 402
C186 0.1UF 20% 10V CERM 402

GPU_50PULLUP 52A8>
GPU_50PULLDWN 52A8>

46B4<> 17D5< 17A4< 16D7< 16C2< 16A8< 11A6< 10D6< 59C7> 52C3>

TCLK TMS TDI TDO TRST*

NVAGP_TRST_L — R72 10K
NC_NVAGP_TDO
NVAGP_TDI
NVAGP_TMS
NVAGP_TCLK — R80 10K

+3V_MAIN
R1024 10K 1% 1/16W MF 402 — NV34
R1025 10K 1% 1/16W MF 402 — NV34

OUTPUT DRIVER BYPASS

MIN_LINE_WIDTH=20

C192 0.01UF, C200 0.01UF, C178 0.1UF, C201 0.1UF, C202 0.1UF, C180 0.1UF, C185 0.1UF, C203 0.1UF, C183 0.1UF, C176 0.1UF
10% 16V CERM 402

CORE BYPASS

52A6> 48C2<> 23C7<> GRAPH_CORE

MIN_LINE_WIDTH=20

C104 0.01UF, C134 0.01UF, C117 0.1UF, C109 0.1UF, C100 0.1UF, C101 0.1UF, C103 0.1UF, C110 0.1UF, C139 0.1UF, C99 0.1UF, C146 0.1UF
10% 16V CERM 402

MIN_LINE_WIDTH=20

C148 0.01UF, C149 0.01UF, C150 0.1UF, C147 0.1UF, C118 0.1UF, C135 0.1UF, C169 0.1UF, C140 0.1UF
10% 16V CERM 402

MIN_LINE_WIDTH=20

C161 10UF, C93 10UF, C168 10UF, C94 10UF
N20P80% 10V Y5V 805

C120 0.1UF, C102 0.1UF, C151 0.1UF
20% 10V CERM 402

+3V_MAIN
R198 10 1% 1/16W MF 402

AGP_PLLVDD

C223 4.7UF N20P80% 10V CERM 805
C219 0.1UF 20% 10V CERM 402
C217 0.001UF 10% 50V CERM 402

I/O BYPASS

+3V_MAIN

C177 0.01UF, C111 0.01UF, C129 0.1UF, C136 0.1UF, C116 0.1UF, C87 0.1UF, C184 0.1UF
10% 16V CERM 402

C137 10UF N20P80% 10V Y5V 805

C91 0.01UF, C97 0.01UF, C187 0.1UF, C179 0.1UF, C105 0.1UF, C112 0.1UF, C181 0.1UF, C182 0.1UF, C188 0.1UF
10% 16V CERM 402

GPU AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

+1_5V_AGP — C214 470PF 10% 50V CERM 402 — GPU_AGP_VREF_X

R195 4.99K 1% 1/16W MF 402 — R192 82.5 1% 1/16W MF 402
GPU_AGP_VREF 17A8< 52A6>
R196 4.99K 1% 1/16W MF 402 — R193 82.5 1% 1/16W MF 402

C215 470PF 10% 50V CERM 402 — GPU_AGP_VREF_Y

NVIDIA AGP

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+2_5V_MAIN

EVENLY DISTRIBUTE 0.01UF & 0.1 UF CAPS AMONGST FBVDDQ PINS ON NV ASIC

C86 0.01UF 10% 16V CERM 402
C84 0.1UF 10% 16V CERM 402
C73 0.1UF 10% 16V CERM 402
C81 0.1UF 10% 16V CERM 402
C90 0.01UF 10% 16V CERM 402
C72 0.1UF 10% 16V CERM 402
C78 0.01UF 10% 16V CERM 402
C98 0.1UF 10% 16V CERM 402
C133 0.1UF 10% 16V CERM 402
C167 0.1UF 10% 16V CERM 402
C159 0.1UF 10% 16V CERM 402
C95 10UF 20% 16V TANT 3528
C75 0.1UF 10% 16V CERM 402
C82 0.1UF 10% 16V CERM 402
C79 0.1UF 10% 16V CERM 402
C115 0.01UF 10% 16V CERM 402
C175 0.1UF 10% 16V CERM 402
C199 0.1UF 10% 16V CERM 402
C83 0.01UF 10% 16V CERM 402
C80 0.1UF 10% 16V CERM 402
C89 0.01UF 10% 16V CERM 402
C96 0.1UF 10% 16V CERM 402
C145 0.1UF 10% 16V CERM 402
C124 10UF 20% 6.3V TANT 805

+2_5V_MAIN

U39 NV18B BGA (3 OF 5)

55D3> 19D8< FBD<0> … FBD<63>
FBADQ0 … FBADQ63
FBVDDQ
NC_VTT
GND
NC_TEST
NC_VTT<0> … NC_VTT<11>
GPU_FB_VREF
FBVREF
ROMA14 ROMA15 ROMCS*

55D3> 18D3< FBDQM<0> … FBDQM<7>
FBADQM0 … FBADQM7

55D3> 18F3< FBA<0> … FBA<12>
FBAA0 … FBAA12

55D3> 18E3< FBABA<0> FBABA<1>
FBABA0 FBABA1

55D3> 18G3< FBARAS_L FBACAS_L FBAWE_L FBACS0_L
NC_FBACS1_L
FBARAS* FBACAS* FBAWE* FBACS0* FBACS1*

FCAL_PD_VDDQ FCAL_PU_GND FCAL_TERM_GND FCAL_CLK_GND FB_DLLVDD
18A5< 18A5< 18A5< 18C6<

R71 49.9 1% 1/16W MF 402
C62 0.1UF 10% 16V CERM 402

FBACKE 18D3< 55D3>
FBACLK0 19C3< 55C3>
FBACLK0_L 19C3< 55C3>
FBACLK1 19D3< 55C3>
FBACLK1_L 19D3< 55C3>
FBDQS0 … FBDQS7 19A5< 55C3>
NC_FBDQS0 … NC_FBDQS7

+2_5V_MAIN

U39 NV18B BGA (4 OF 5)

55C3> 19C8< FBD<64> … FBD<127>
FBDCD0 … FBDCD63

55C3> 18D3< FBDQM<8> … FBDQM<15>
FBDCDQM0 … FBDCDQM7

55C3> 18C3< FBA<0> … FBA<8>
FBA0 … FBA8

55C3> 18B3< FBA<9> … FBA<12>
FBA9 FBA10 FBA11 FBA12

55C3> 18A3< FBABA<0> FBABA<1>
FBCBA0 FBCBA1

55B3> 19B3< FBBCLK0 FBBCLK0_L FBBCLK1 FBBCLK1_L
FBBCLK0 FBBCLK0* FBBCLK1 FBBCLK1*

FBCDQS0 … FBCDQS7
FBDQS<8> … FBDQS<15> 19A5< 55B3>
NC_FBCDQS0 … NC_FBCDQS7
NC_FBDQS_L<8> … NC_FBDQS_L<15>

FBCRAS* FBCCAS* FBCWE* FBCCS0* FBCCS1* FBCCKE
FBBRAS_L FBBCAS_L FBBWE_L FBBCS0_L NC_FBBCS1_L FBBCKE
1BC3< 55C3>
1BC3< 55C3>
1BC3< 55C3>
1BC3< 55C3>
1BA3< 55B3>

THERMAL GND

+3V_MAIN

R52 10 1% 1/16W MF 402
18D7< FB_DLLVDD
C61 4.7UF 20% 6.3V TANT 3528
C70 0.1UF 10% 16V CERM 402
C69 0.001UF 10% 50V CERM 402

18D7< FBCAL_CLK_GND
18D7< FBCAL_TERM_GND
18D7< FBCAL_PU_GND
R95 49.9 1% 1/16W MF 402
R83 0 1% 1/16W MF 402
R88 549 1% 1/16W MF 402

+2_5V_MAIN

NVIDIA VREF

R36 0 1% 1/16W MF 402
MEMREFN1
U7 TLV431A SOT
R41 1K 1% 1/16W MF 402
C54 0.1UF 10% 16V CERM 402
MEMREFN2
R50 0 1% 1/16W MF 402
R49 0 1% 1/16W MF 402
NOSTUFF
C510 100PF 5% 25V CERM 402
R463 1K 1% 1/16W MF 402
C509 0.1UF 10% 16V CERM 402

DQM R'S CLOSE TO GPU

OTHER R'S BETWEEN GPU & MEMORY

55D3> 18D8> FBDQM<0> … FBDQM<7>
R117 0 R111 0 R90 0 R84 0 R164 0 R155 0 R154 0 R143 0
1/16W 5% MF 402
RFBDQM<0> … RFBDQM<7> 20C6< 55D3>

55D3> 18C8> FBACAS_L FBARAS_L FBACS0_L FBAWE_L
RP22 22 1/16W 5% SM1
ZT29 ZT20 ZT30 ZT31
RFBACAS_L RFBARAS_L RFBACS0_L RFBAWE_L 20B2< 20B6< 55D3>
NO_TEST

55D3> 18D8> FBA<0> … FBA<12>
RP94 22 RP95 22 RP23 22 RP93 22 RP84 22 RP83 22 RP8 22 1/16W 5% SM1
ZT22 … ZT32
RFBA<0> … RFBA<11> 20D2< 20D6< 55D3>
NO_TEST
NC_RFBA<12>

55D3> 18C8> FBABA<0> FBABA<1>
RP93 22 1/16W 5% SM1
ZT21 ZT32
RFBABA<0> RFBABA<1> 20C2< 20C6< 55D3>

WEAK PULL-DOWN
RECOMMENDED BY NVIDIA
55D3> 18D7<> FBACKE
R130 22 1/16W 5% SM1
ZT28
RFBACKE 20C2< 20C6< 55C3>
R131 10K 1% 1/16W MF 402

55C3> 18D5> FBDQM<8> … FBDQM<15>
R64 0 R66 0 R70 0 R67 0 R54 0 R56 0 R58 0 R59 0
NV34
1/16W 5% MF 402
RFBDQM<8> … RFBDQM<15> 21C6< 55C3>

55C3> 18C4<> FBBCS0_L FBBWE_L FBBCAS_L FBBRAS_L
RP9 22 1/16W 5% SM1
ZT2 ZT5 ZT1 ZT3
RFBBCS0_L RFBBWE_L RFBBCAS_L RFBBRAS_L 21B2< 21B6< 55B3>
NO_TEST

55C3> 18D5<> FBBA<0> … FBBA<12>
RP85 22 RP84 22 RP83 22 RP8 22 1/16W 5% SM1
ZT6 … ZT32
RFBBA<0> … RFBBA<11> 21D2< 21D6< 55C3>
NO_TEST
NC_RFBBA<12>

55B3> 18C4<> FBBCKE
WEAK PULL-DOWN
RECOMMENDED BY NVIDIA
R132 22 1/16W 5% SM1
ZT19
RFBBCKE 21C2< 21C6< 55B3>
R61 10K 1% 1/16W MF 402

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NVIDIA FRAME BUFFER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
E	051-6569	A
SCALE	SHT	OF
NONE	18	69

DRAWING

PLACE R'S BETWEEN GPU & MEMORY

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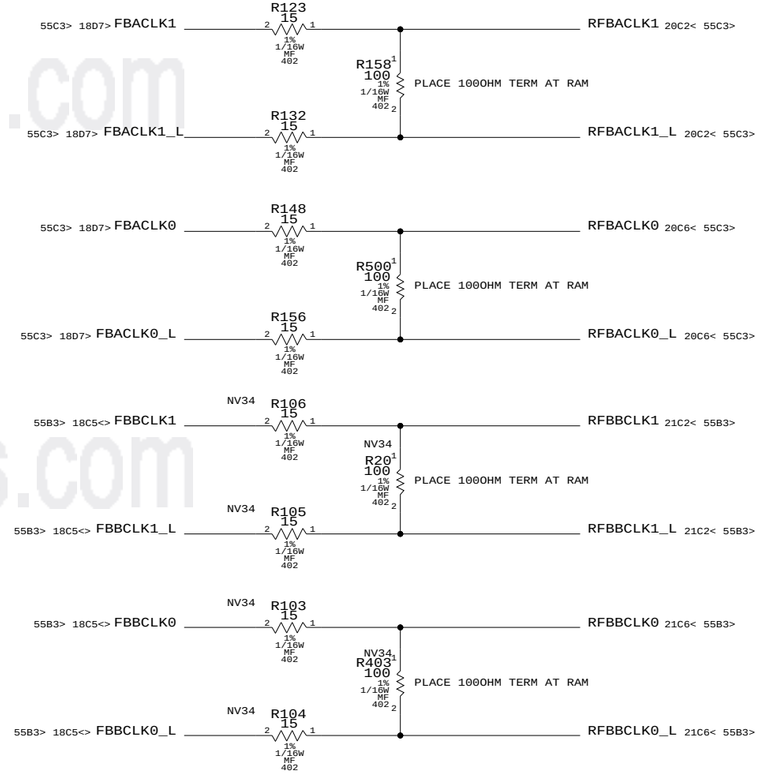
PLACE R'S CLOSE TO GPU



PLACE THESE R CLOSE TO GPU — PLACE THESE R CLOSE TO SGRAM

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FB TERMINATION

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A

SCALE	SHT	OF
NONE	19	69

DRAWING

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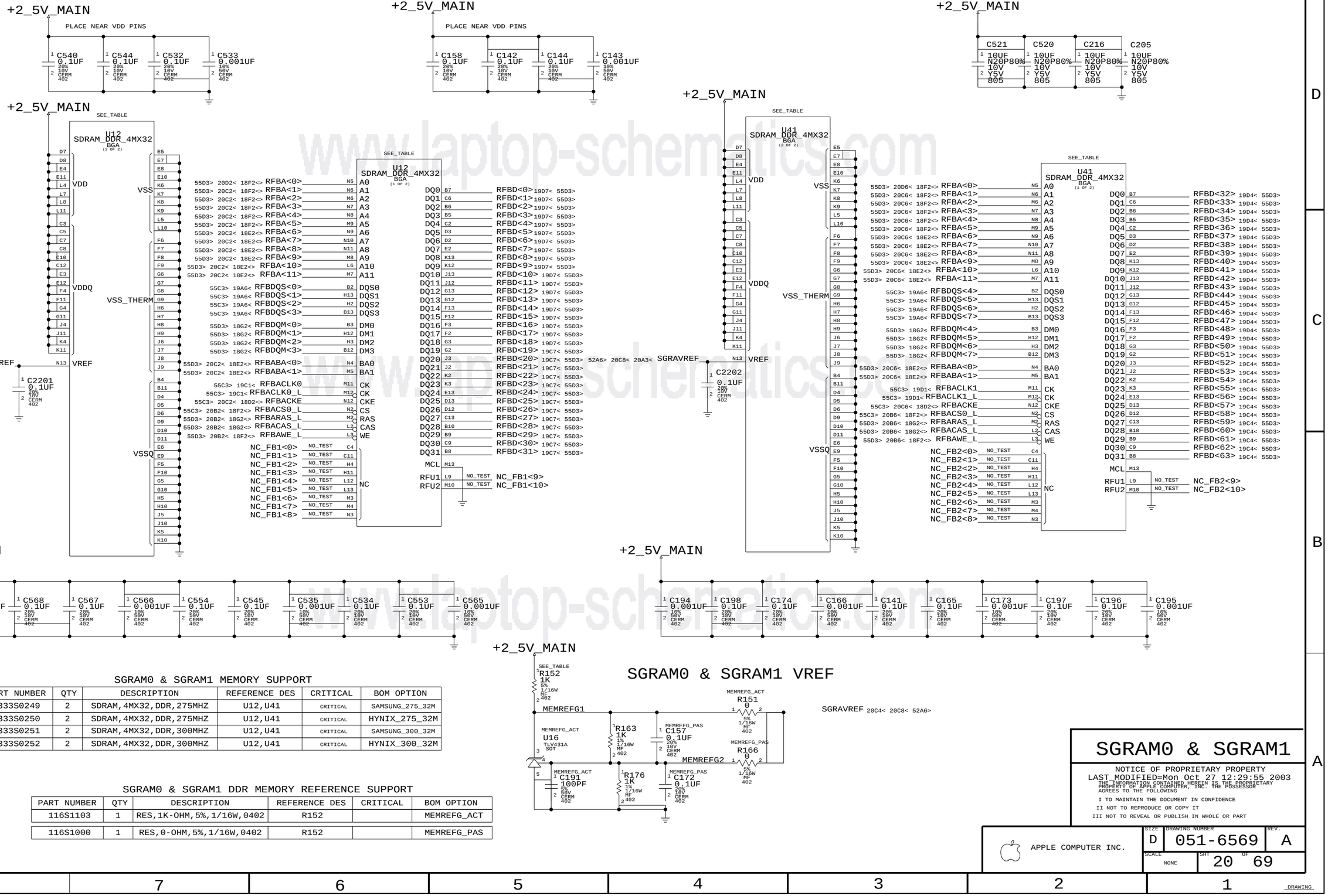

SGRAM0 & SGRAM1 VREF

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM,4MX32,DDR,275MHZ	U12,U41	CRITICAL	SAMSUNG_275_32M
333S0250	2	SDRAM,4MX32,DDR,275MHZ	U12,U41	CRITICAL	HYNIX_275_32M
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U12,U41	CRITICAL	SAMSUNG_300_32M
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U12,U41	CRITICAL	HYNIX_300_32M

SGRAM0 & SGRAM1 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES,1K-OHM,5%,1/16W,0402	R152		MEMREFG_ACT
116S1000	1	RES,0-OHM,5%,1/16W,0402	R152		MEMREFG_PAS

SGRAM0 & SGRAM1

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE	SHT	OF
NONE	20	69

DRAWING

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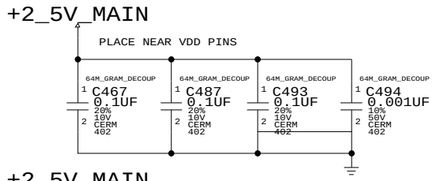
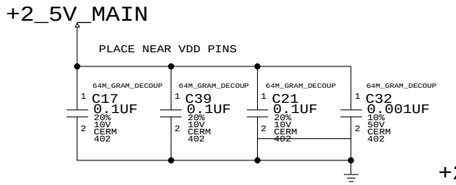
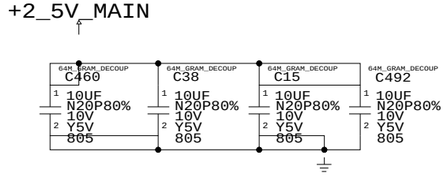
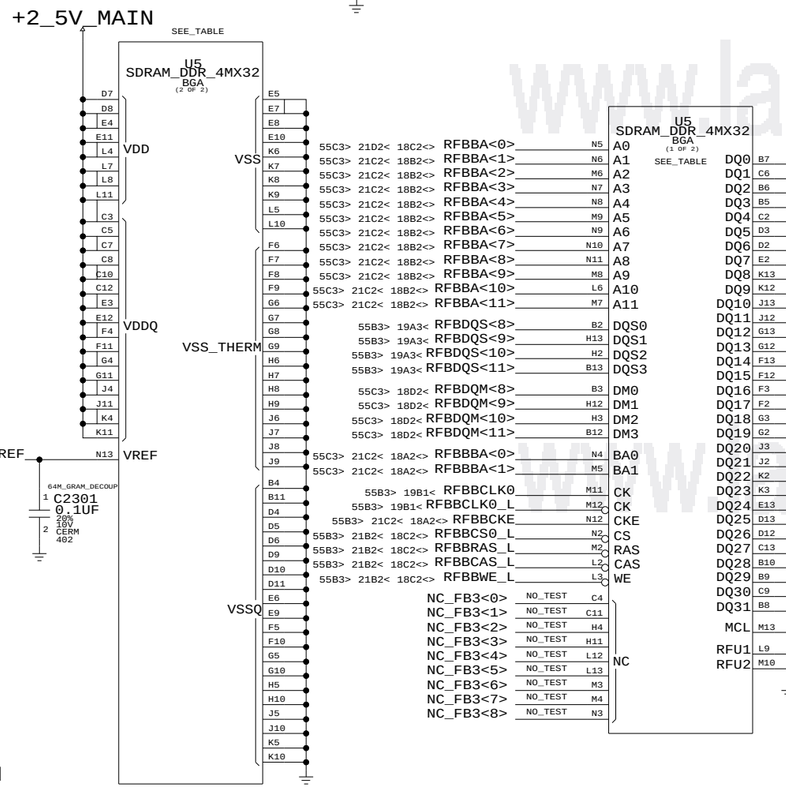
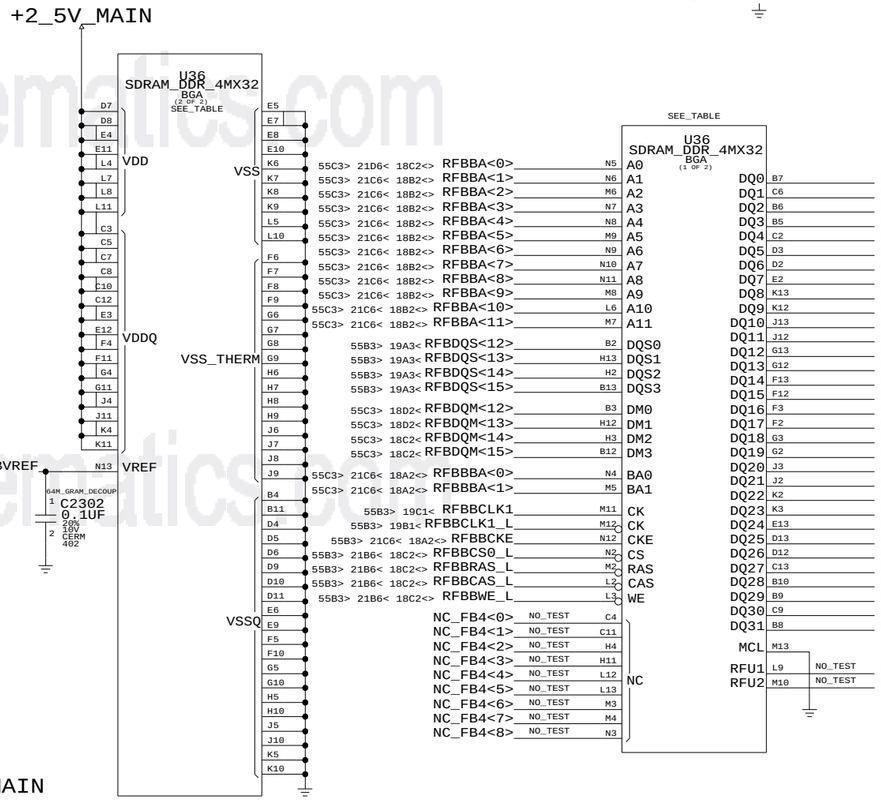
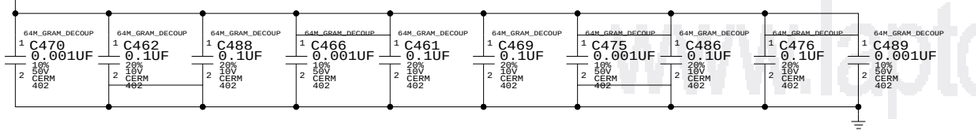


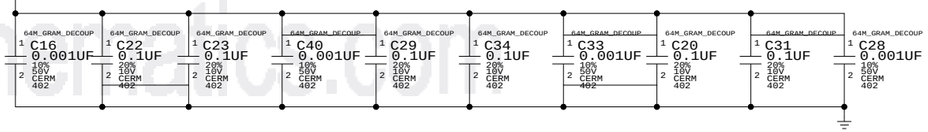










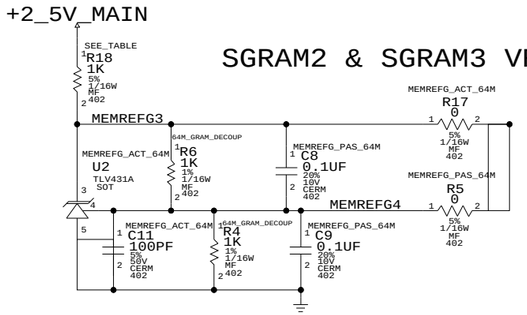


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM,4MX32,DDR,275MHZ	U5,U36	CRITICAL	SAMSUNG_275_64M
333S0250	2	SDRAM,4MX32,DDR,275MHZ	U5,U36	CRITICAL	HYNIX_275_64M
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5,U36	CRITICAL	SAMSUNG_300_64M
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5,U36	CRITICAL	HYNIX_300_64M

SGRAM2 & SGRAM3 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES,1K-OHM,5%,1/16W,0402	R18		MEMREFG_ACT_64M
116S1000	1	RES,0-OHM,5%,1/16W,0402	R18		MEMREFG_PAS_64M



SGRAM2 & SGRAM3 VREF

SGRBVREF 21C4< 21C8< 52A6>

SGRAM2 & SGRAM3

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
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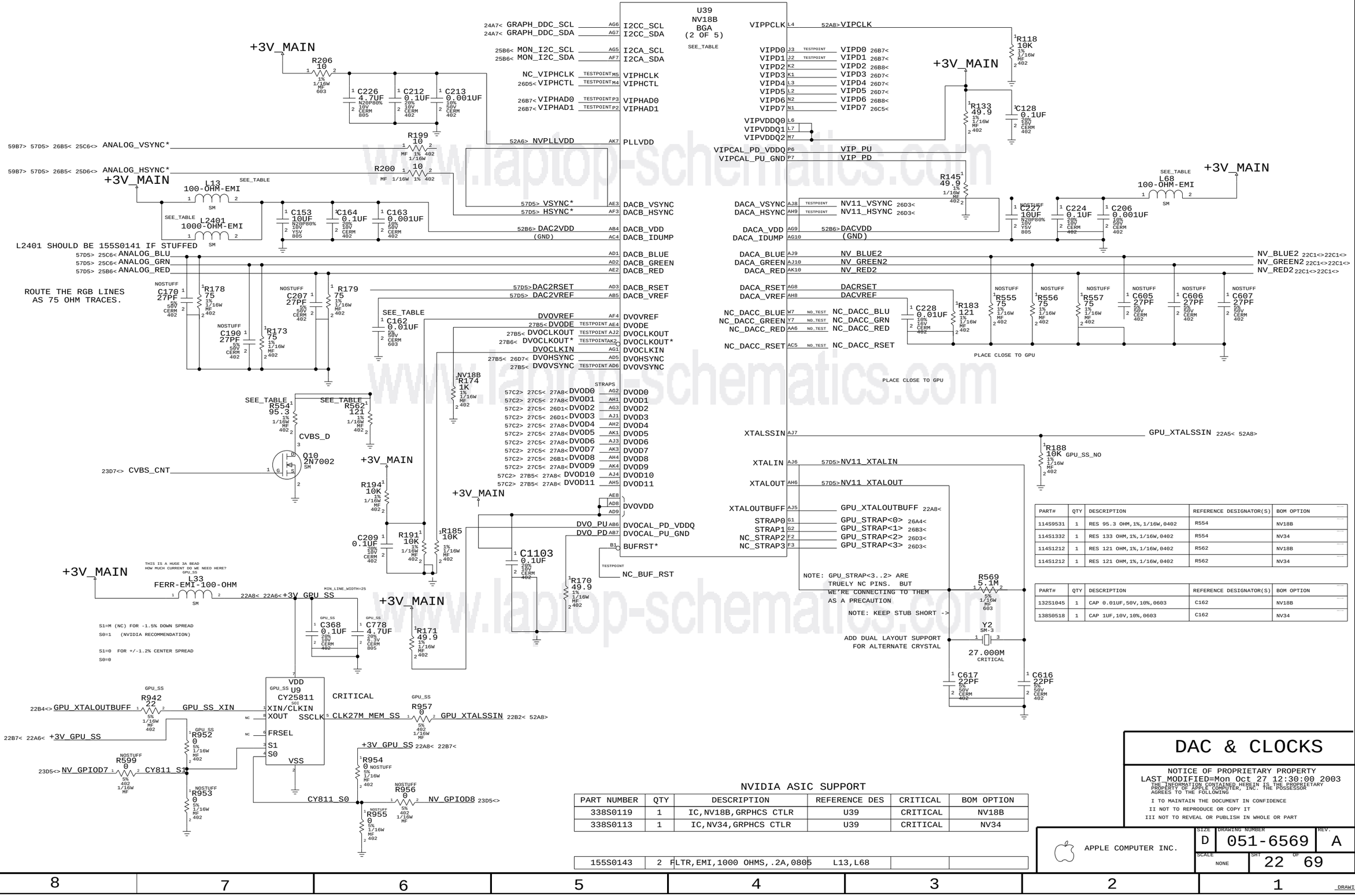
DRAWING



NVIDIA ASIC SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0119	1	IC,NV18B,GRPHCS CTLR	U39	CRITICAL	NV18B
338S0113	1	IC,NV34,GRPHCS CTLR	U39	CRITICAL	NV34

155S0143	2	FLTR,EMI,1000 OHMS,.2A,0805	L13,L68		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S9531	1	RES 95.3 OHM,1%,1/16W,0402	R554	NV18B
114S1332	1	RES 133 OHM,1%,1/16W,0402	R554	NV34
114S1212	1	RES 121 OHM,1%,1/16W,0402	R562	NV18B
114S1212	1	RES 121 OHM,1%,1/16W,0402	R562	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1045	1	CAP 0.01UF,50V,10%,0603	C162	NV18B
138S0518	1	CAP 1UF,10V,10%,0603	C162	NV34

DAC & CLOCKS

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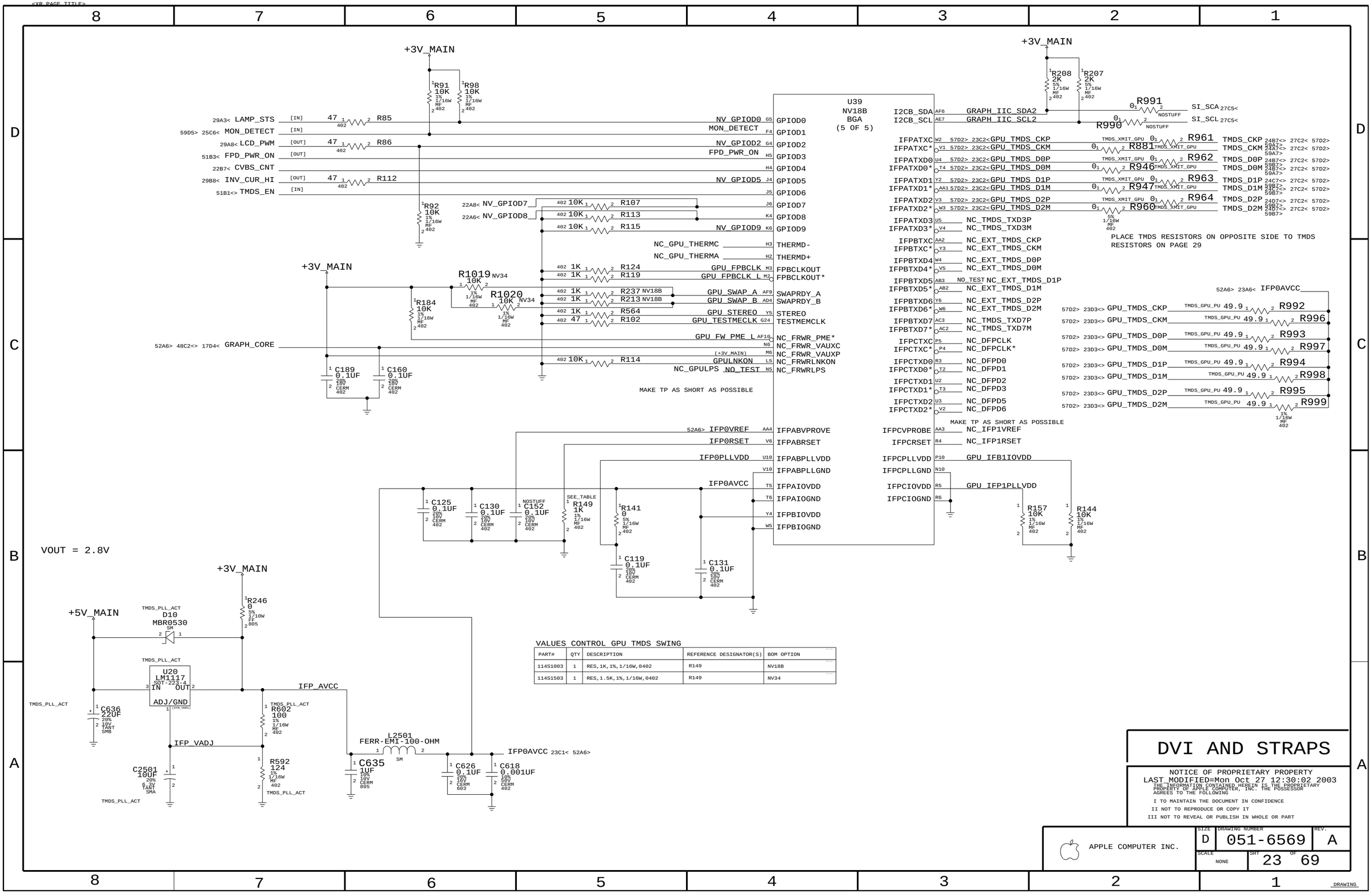
+3V_MAIN
R91 10K 1% 1/16W MF 402
R98 10K 1% 1/16W MF 402
29A3< LAMP_STS [IN] 47 R85
59D5> 25C6< MON_DETECT [IN]
29A8< LCD_PWM [OUT] 47 R86
51B3< FPD_PWR_ON [OUT]
22B7< CVBS_CNT
29B8< INV_CUR_HI [OUT] 47 R112
51B1<> TMDS_EN [IN]
R92 10K 1% 1/16W MF 402
22A8< NV_GPIOD7 10K R107
22A6< NV_GPIOD8 10K R113
10K R115
NV_GPIOD0 G5
MON_DETECT F4
NV_GPIOD2 G4
FPD_PWR_ON H5
H4
NV_GPIOD5 J4
J5
J6
K4
NV_GPIOD9 K6
NC_GPU_THERMC H3
NC_GPU_THERMA H2
U39
NV18B
BGA
(5 OF 5)
GPIOD0
GPIOD1
GPIOD2
GPIOD3
GPIOD4
GPIOD5
GPIOD6
GPIOD7
GPIOD8
GPIOD9
THERMD-
THERMD+
+3V_MAIN
R1019 10K NV34
R1020 10K NV34
R184 10K 1% 1/16W MF 402
1K R124
1K R119
1K R237 NV18B
1K R213 NV18B
1K R564
47 R102
GPU_FPBCLK M3
GPU_FPBCLK_L M2
GPU_SWAP_A AF9
GPU_SWAP_B AD4
GPU_STEREO Y5
GPU_TESTMECLK G24
FPBCLKOUT
FPBCLKOUT*
SWAPRDY_A
SWAPRDY_B
STEREO
TESTMEMCLK
GPU_FW_PME_L AF10
NC_FRWR_PME*
NC_FRWR_VAUXC
NC_FRWR_VAUXP
NC_FRWRLNKON
NC_FRWRLPS
52A6> 48C2<> 17D4< GRAPH_CORE
C189 0.1UF 20% 10V CERM 402
C160 0.1UF 20% 10V CERM 402
(+3V_MAIN) M6
GPULNKON L5
10K R114
NC_GPULPS NO_TEST N5
N6
MAKE TP AS SHORT AS POSSIBLE
52A6> IFP0VREF AA4
IFP0RSET V6
IFP0PLLVDD U10
V10
IFP0AVCC T5
T6
Y4
W5
IFPABVPROVE
IFPABRSET
IFPABPLLVDD
IFPABPLLGND
IFPAIOVDD
IFPAIOGND
IFPBIOVDD
IFPBIOGND
C125 0.1UF 20% 10V CERM 402
C130 0.1UF 20% 10V CERM 402
NOSTUFF C152 0.1UF 20% 10V CERM 402
SEE_TABLE R149 1K 1% 1/16W MF 402
R141 0 5% 1/16W MF 402
C119 0.1UF 20% 10V CERM 402
C131 0.1UF 20% 10V CERM 402
+3V_MAIN
R208 2K 5% 1/16W MF 402
R207 2K 5% 1/16W MF 402
I2CB_SDA AF6 GRAPH_IIC_SDA2
I2CB_SCL AE7 GRAPH_IIC_SCL2
R991 NOSTUFF SI_SCA 27C5<
R990 NOSTUFF SI_SCL 27C5<
IFPATXC W2 57D2> 23C2< GPU_TMDS_CKP R961 TMDS_CKP 24B7<> 27C2< 57D2>
IFPATXC* V1 57D2> 23C2< GPU_TMDS_CKM R881 TMDS_CKM 24A7<> 27C2< 57D2>
IFPATXD0 U4 57D2> 23C2< GPU_TMDS_D0P R962 TMDS_D0P 24B7<> 27C2< 57D2>
IFPATXD0* T4 57D2> 23C2< GPU_TMDS_D0M R946 TMDS_D0M 24B7<> 27C2< 57D2>
IFPATXD1 Y2 57D2> 23C2< GPU_TMDS_D1P R963 TMDS_D1P 24C7<> 27C2< 57D2>
IFPATXD1* AA1 57D2> 23C2< GPU_TMDS_D1M R947 TMDS_D1M 24C7<> 27C2< 57D2>
IFPATXD2 V3 57D2> 23C2< GPU_TMDS_D2P R964 TMDS_D2P 24D7<> 27C2< 57D2>
IFPATXD2* W3 57D2> 23C2< GPU_TMDS_D2M R960 TMDS_D2M 24D7<> 27C2< 57D2>
IFPATXD3 U5 NC_TMDS_TXD3P
IFPATXD3* V4 NC_TMDS_TXD3M
IFPBTXC AA2 NC_EXT_TMDS_CKP
IFPBTXC* Y3 NC_EXT_TMDS_CKM
IFPBTXD4 W4 NC_EXT_TMDS_D0P
IFPBTXD4* V5 NC_EXT_TMDS_D0M
IFPBTXD5 AB3 NO_TEST NC_EXT_TMDS_D1P
IFPBTXD5* AB2 NC_EXT_TMDS_D1M
IFPBTXD6 Y6 NC_EXT_TMDS_D2P
IFPBTXD6* W6 NC_EXT_TMDS_D2M
IFPBTXD7 AC3 NC_TMDS_TXD7P
IFPBTXD7* AC2 NC_TMDS_TXD7M
IFPCTXC P5 NC_DFPCLK
IFPCTXC* P4 NC_DFPCLK*
IFPCTXD0 R3 NC_DFPD0
IFPCTXD0* T2 NC_DFPD1
IFPCTXD1 U2 NC_DFPD2
IFPCTXD1* T3 NC_DFPD3
IFPCTXD2 U3 NC_DFPD5
IFPCTXD2* V2 NC_DFPD6
IFPCVPROBE AA3 NC_IFP1VREF
IFPCRSET R4 NC_IFP1RSET
IFPCPLLVDD P10 GPU_IFB1IOVDD
IFPCPLLGND N10
IFPCIOVDD R5 GPU_IFP1PLLVDD
IFPCIOGND R6
MAKE TP AS SHORT AS POSSIBLE
R157 10K 1% 1/16W MF 402
R144 10K 1% 1/16W MF 402
PLACE TMDS RESISTORS ON OPPOSITE SIDE TO TMDS RESISTORS ON PAGE 29
52A6> 23A6< IFP0AVCC
57D2> 23D3<> GPU_TMDS_CKP TMDS_GPU_PU 49.9 R992
57D2> 23D3<> GPU_TMDS_CKM TMDS_GPU_PU 49.9 R996
57D2> 23D3<> GPU_TMDS_D0P TMDS_GPU_PU 49.9 R993
57D2> 23D3<> GPU_TMDS_D0M TMDS_GPU_PU 49.9 R997
57D2> 23D3<> GPU_TMDS_D1P TMDS_GPU_PU 49.9 R994
57D2> 23D3<> GPU_TMDS_D1M TMDS_GPU_PU 49.9 R998
57D2> 23D3<> GPU_TMDS_D2P TMDS_GPU_PU 49.9 R995
57D2> 23D3<> GPU_TMDS_D2M TMDS_GPU_PU 49.9 R999
VOUT = 2.8V
+3V_MAIN
+5V_MAIN
TMDS_PLL_ACT D10 MBR0530 SM
R246 0 5% 1/10W FF 805
U20 LM1117 SOT-223-4 IN OUT ADJ/GND (SYM_VER1)
IFP_AVCC
C636 2.2UF 20% 10V TANT SMB
IFP_VADJ
C2501 10UF 20% 6.3V TANT SMA
R602 100 1% 1/16W MF 402
R592 124 1% 1/16W MF 402
L2501 FERR-EMI-100-OHM SM
C635 1UF 10% 10V CERM 805
C626 0.1UF 10% 50V CERM 603
C618 0.001UF 10% 50V CERM 402
IFP0AVCC 23C1< 52A6>
VALUES CONTROL GPU TMDS SWING
PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION
114S1003 | 1 | RES,1K,1%,1/16W,0402 | R149 | NV18B
114S1503 | 1 | RES,1.5K,1%,1/16W,0402 | R149 | NV34
DVI AND STRAPS
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DRAWING NUMBER 051-6569
REV: A
SCALE NONE
SHT 23 OF 69
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3012	4	RES,301 OHMS,1%,1/16W,0402	R559,R570,R591,R600	FPD_3V3
116S1202	4	RES,200 OHMS,5%,1/16W,0402	R559,R570,R591,R600	FPD_12VM

52B6> 51C1<> +3.3VFPD — L82 FERR-250-OHM SM — INT_TMDS_3V

59B7> 57D2> 27C2< 23D1< TMDS_D2P — R603 0 XMIT_RES — TD2P

R600 301 1% 1/16W MF 402 SEE_TABLE — L76 90-OHM SM XMIT_CHOKE

59B7> 57D2> 27C2< 23D1< TMDS_D2M — R594 0 XMIT_RES — TD2M

59B7> 57D2> 27C2< 23D1< TMDS_D1P — R593 0 XMIT_RES — TD1P

R591 301 1% 1/16W MF 402 SEE_TABLE — L74 90-OHM SM XMIT_CHOKE

59B7> 57D2> 27C2< 23D1< TMDS_D1M — R582 0 XMIT_RES — TD1M

(518S0039) J12 FI-TWE21P-VF F-ST-SM

INT_TMDS_3V
57C5> TD2M
57C5> TD1P
57C5> TD0M
57C5> TCKP
59C5> TMDS_DDC_DAT

59C7> 52A6> INT_TMDS_3V
57C5> TD2P
57C5> TD1M
57C5> TD0P
57C5> TCKM
59B7> 52B6> DDC_VCC_3
59C5> TMDS_DDC_CLK
INT_TMDS_3V
43B7< 29A3< 43A7< 52C4

INTERNAL TMDS CONNECTOR

C652 0.01UF 10% 16V CERM 402

C107 10UF 10% 16V CERM 1210

59B7> 57D2> 27C2< 23D1< TMDS_D0P — R581 0 XMIT_RES — TD0P

R570 301 1% 1/16W MF 402 SEE_TABLE — L71 90-OHM SM XMIT_CHOKE

59A7> 57D2> 27C2< 23D1< TMDS_D0M — R568 0 XMIT_RES — TD0M

59A7> 57D2> 27C2< 23D1< TMDS_CKP — R567 0 XMIT_RES — TCKP

R559 301 1% 1/16W MF 402 SEE_TABLE — L67 90-OHM SM XMIT_CHOKE

59A7> 57D2> 27C2< 23D1< TMDS_CKM — R550 0 XMIT_RES — TCKM

22D5<> GRAPH_DDC_SDA — R546 33 5% 1/16W MF 402 — TMDS_DDC_DAT

+3V_MAIN — R540 2K 5% 1/16W MF 402

L64 FERR-250-OHM SM — DDC_VCC_3

C610 0.01UF 10% 16V CERM 402

R547 2K 5% 1/16W MF 402

22D5<> GRAPH_DDC_SCL — R551 33 5% 1/16W MF 402 — TMDS_DDC_CLK

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TMDS/LVDS

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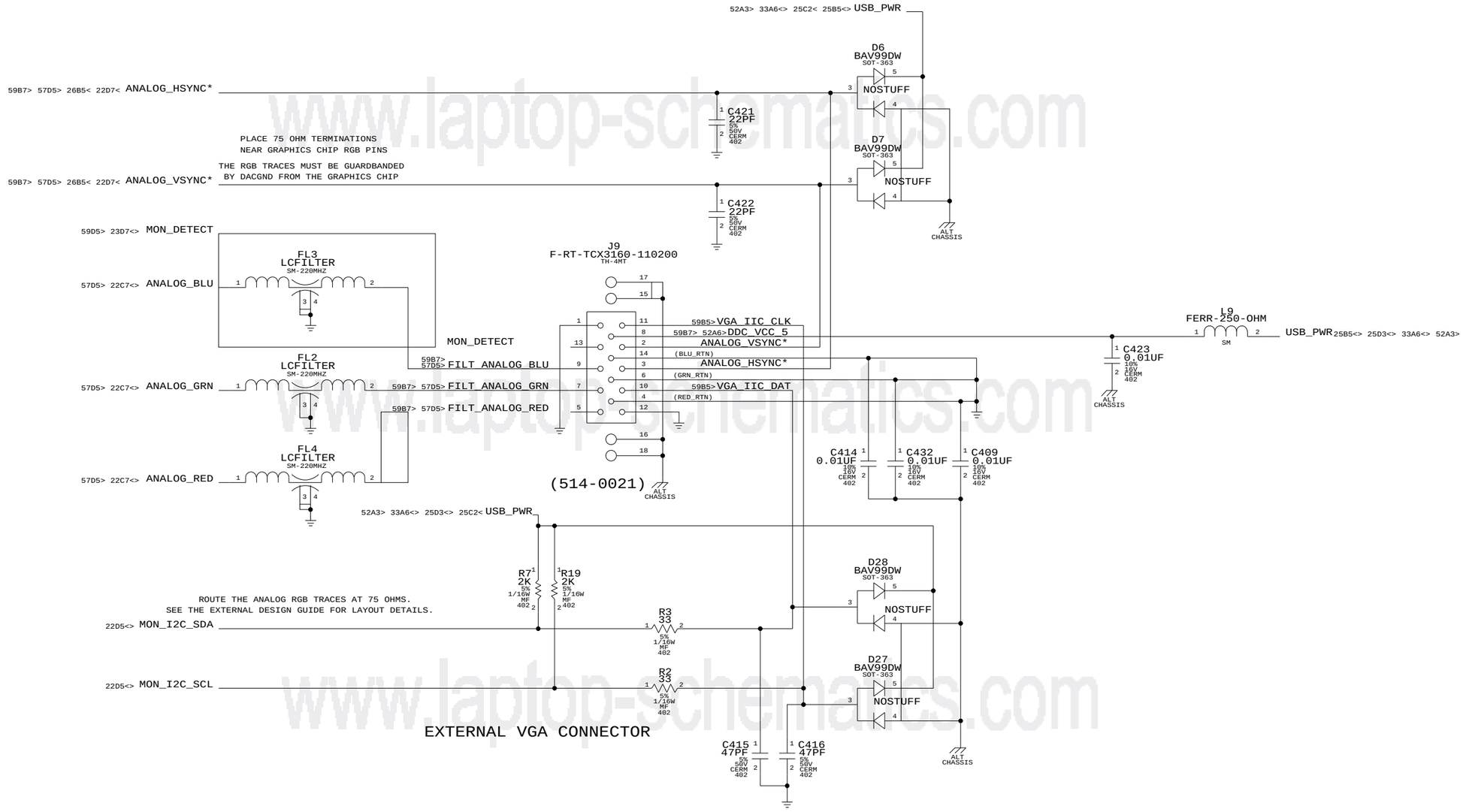

EXTERNAL VGA CONNECTOR

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EXTERNAL VGA

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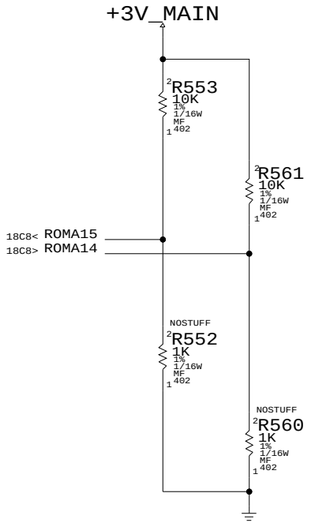
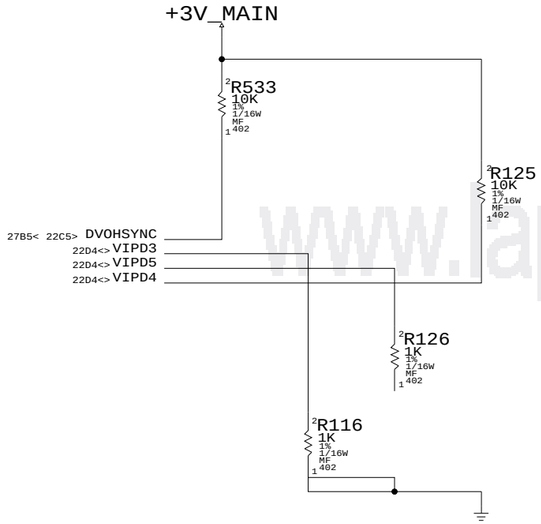
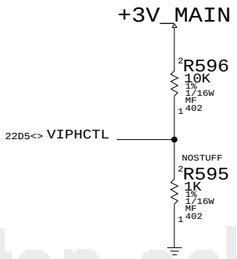


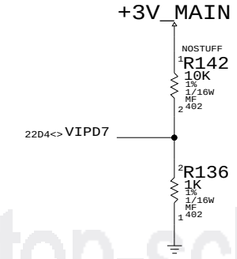
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
[1..0] = [ROMA15,ROMA14]
00 = PARALLEL
01 = SERIAL AT25F
10 = SERIAL SST45VF
* 11 = SERIAL FUTURE



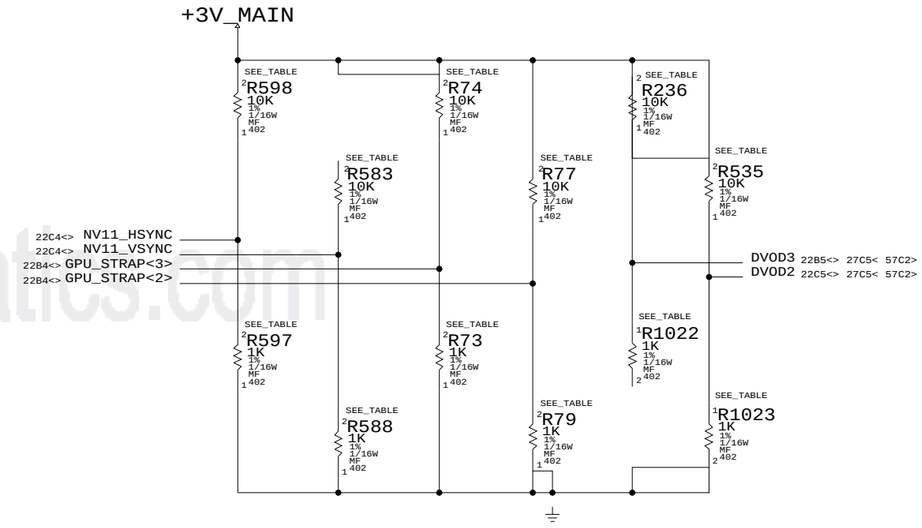
(3) PCI DEVICE ID
[3..0] = [DVOHSYNC,VIPD3,VIPD5,VIPD4]
0010 = 0X112 GEFORCE2 GO
0011 = 0X113 QUADRO2 GO
0100 = 0X114 NV17M
0000 = 0X110 GEFORCE2GO MX (NV11B)
* 1001 = NV18B,NV31,NV34



(5) HOST MODE
[0] = [VIPHCTL]
0 = PCI MODE
* 1 = AGP MODE



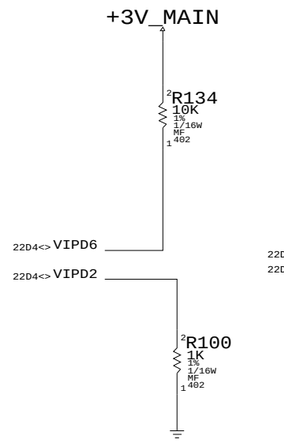
(6) AGP SIDEBAND
[0] = [VIPD7]
* 0 = ENABLE AGP SIDEBAND
1 = DISABLE AGP SIDEBAND



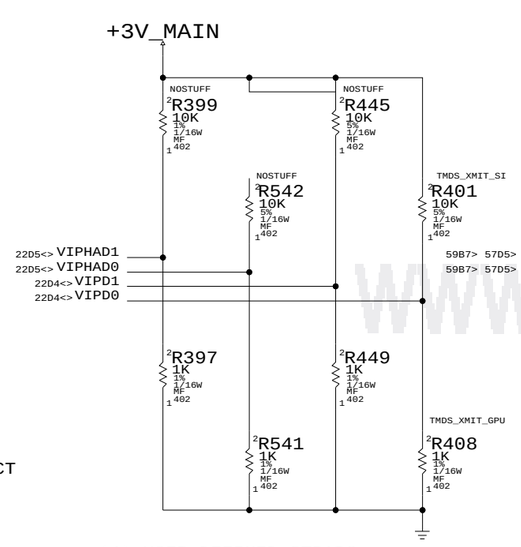
(8) FRAME BUFFER MEMORY TYPE
[3..0] = [NV11_HSYNC,NV11_VSYNC,GPU_STRAP<3>,GPU_STRAP<2>]
1111 = 222MHZ
1101 = 275MHZ SAMSUNG
1100 = 275MHZ HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S1004	5	RES,10KOHM,1%,0402	R598,R583,R77,R236,R535		SAMSUNG_NV18B_270
114S1003	1	RES,1KOHM,1%,0402	R73		SAMSUNG_NV18B_270
114S1004	4	RES,10KOHM,1%,0402	R598,R583,R236,R535		HYNIX_NV18B_270
114S1003	2	RES,1KOHM,1%,0402	R73,R79		HYNIX_NV18B_270

114S1004	5	RES,10KOHM,1%,0402	R598,R583,R535,R74,R77		SAMSUNG_NV34_270
114S1003	1	RES,1KOHM,1%,0402	R1022		SAMSUNG_NV34_270
114S1004	4	RES,10KOHM,1%,0402	R583,R74,R77,R535		HYNIX_NV34_270
114S1003	2	RES,1KOHM,1%,0402	R597,R1022		HYNIX_NV34_270

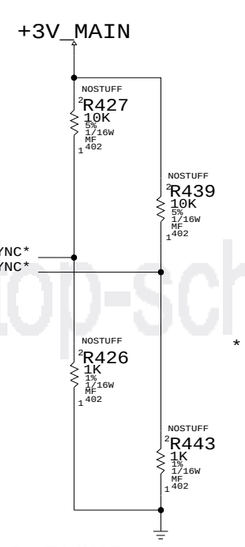


(2) CRYSTAL FREQUENCY SELECT
[1..0] = [VIPD6,VIPD2]
00 = 13.5MHZ
01 = 14.38MHZ
* 10 = 27MHZ
11 = {UNDEFINED}



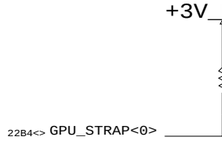
(4) USER DEFINED STRAPS
[3..0] = [VIPHAD1,VIPHAD0,VIPD1,VIPD0]

THESE BITS ARE UNDEFINED BUT THEY
MUST BE KEPT LOW DURING RESET

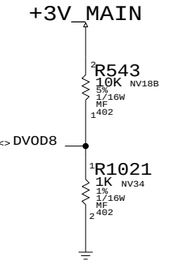


(7) TV MODE
[1..0] = [ANALOG_HSYNC*,ANALOG_VSYNC*]
00 = SECAM
01 = NTSC
10 = PAL
* 11 = DISABLED
(THESE RESISTORS ARE ALL NOSTUFF)

(9) SUB-VENDOR
[0] = [GPU_STRAP<1>]
0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)



(10) PCI ADDRESS BUS
[0] = [GPU_STRAP<0>]
0 = REVERSED
* 1 = NORMAL



FASTWR
0 = ENABLE
1 = DISABLE

NVIDIA STRAPS 1

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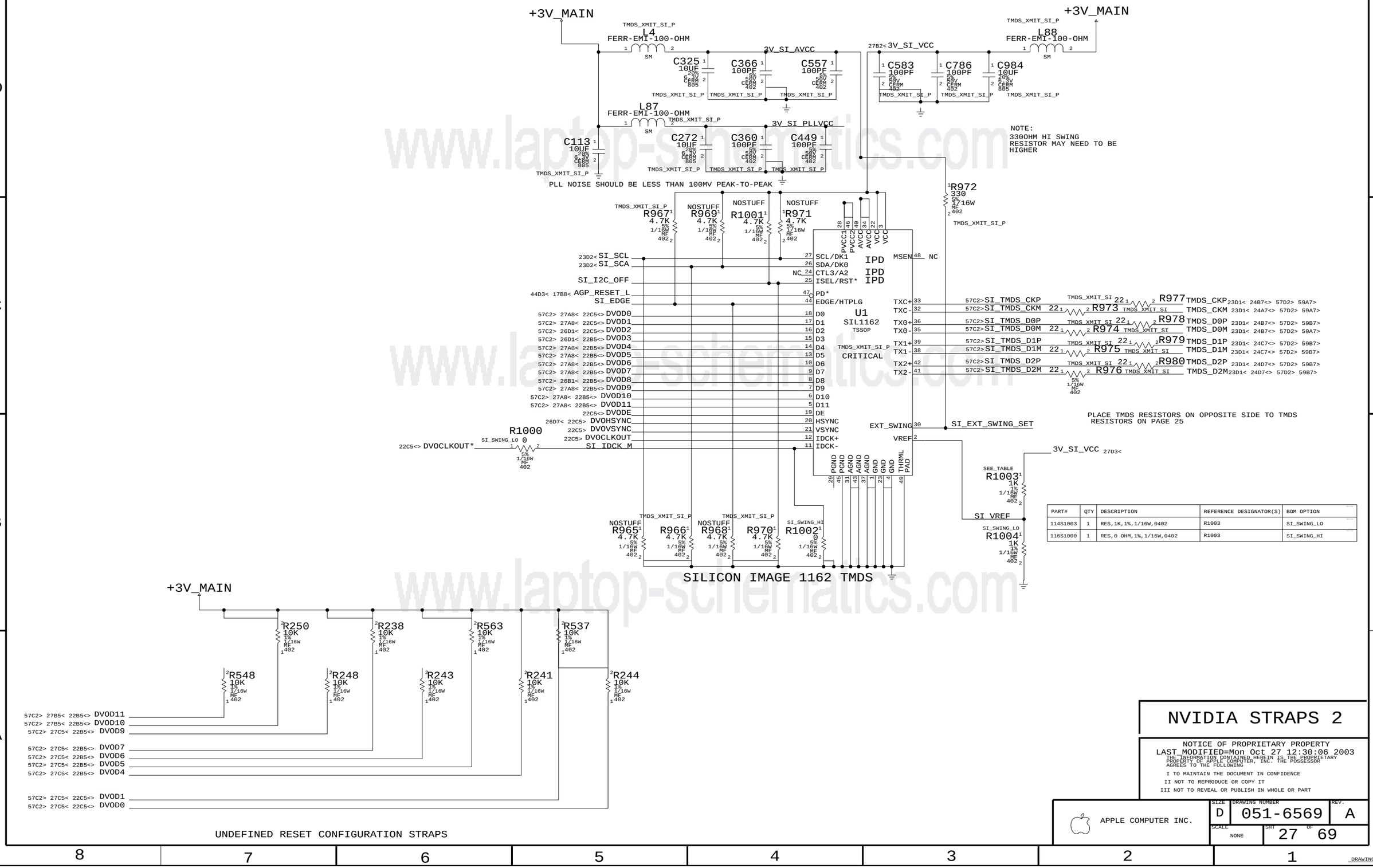

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1003	1	RES,1K,1%,1/16W,0402	R1003	SI_SWING_LO
116S1000	1	RES,0 OHM,1%,1/16W,0402	R1003	SI_SWING_HI

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NVIDIA STRAPS 2

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+2_5V_MAIN
+1_8V_MAIN
R571 0 1/16W MF 603
R572 0 1/16W MF 603
U19 LT1962-ADJ MSOP
IN OUT NC NC ADJ BYP GND SHDN
LT1962_INT_VIN
NC_UT6P7 NO_TEST
NC_UT6P6 NO_TEST
LT1962_INT_ADJ
LT1962_INT_BYP
C623 0.01UF 10% 16V X5R 402
R586 15.8K 1% 1/16W MF 402
C233 10UF 20% 6.3V CERM 805
C234 1UF 10% 10V X5R 603
52D3> 30D5< 16D6< 9D4< +1_5V_INTREPID_PLL

R630 4.7 5% 1/16W MF 402
C713 0.1UF 20% 10V CERM 402
C3005 0.1UF 20% 10V CERM 402
+1_5V_INTREPID_PLL8 52D3>
R629 4.7
INT_PLL9_GND 28A4<>
C704 0.1UF
C3004 0.1UF
+1_5V_INTREPID_PLL4 52D3>
R628 4.7
INT_PLL7_GND 28A4<>
C703 0.1UF
C3003 0.1UF
+1_5V_INTREPID_PLL3 52D3>
R620 4.7
INT_PLL3_GND 28A4<>
C692 0.1UF
C3002 0.1UF
+1_5V_INTREPID_PLL2 52D3>
R565 4.7
INT_PLL2_GND 28A5<>
C229 0.1UF
C3001 0.1UF
+1_5V_INTREPID_PLL1 52D3>
INT_PLL1_GND 28A5<>

+3V_MAIN
NC_RPT48P1 NO_TEST
RP39 10K 5% 1/16W SM1
59C5> 29C5<> 28C3<> COMM_GPIO_L
NC_RP3319 NO_TEST
59C5> 29C7<> 28C3<> COMM_TRXC
28C5<> SNF_FSEL
R755 1K 1% 1/16W MF 402
R756 10K
28B5<> VCORE_VGATE

I2C 2 PULL-UPS
+3V_MAIN
59A7> 39B1<> 34B5< 29C7<> 28A3<> INT_I2C_CLK2
R264 4.7K 5% 1/16W MF 402
39B1<> 34B5< 29C7<> 28A3<> 59A7> INT_I2C_DATA2
R641 4.7K
59D5> 29D7<> 28C5<> COMM_SHUTDOWN
RP117 10K 5% 1/16W SM1
35B8< 28B5<> INT_ENET_RST_L
RP117 10K
35B4> 28B5<> ENET_ENERGY_DET
RP117 10K
NC_RP3324_2 NO_TEST
RP117 10K
33A7> 32B1< 28B3< USB_PWR_FLT*
R1005 10K 1% 1/16W MF 402

INTREPID DEBUG HOOKS
PLL TEST FUNCTION
HWPLL_TESTMUXSEL[0:5]
+3V_MAIN
NOSTUFF
R231 1K 1% 1/16W MF 402
R678 1K
R289 1K
R292 1K
R291 1K
R274 1K
R228 1K
R232 1K
INT_MOD_BITCLK 28A3<> 28A8<
INT_MOD_CLKOUT 28A3> 28A8<
INT_MOD_DTO 28A3> 28A8<
INT_MOD_SYNC 28A3<> 28A8< (INTREPID JTAG TDO)
INT_MOD_DTI 28A3< 28A8<
JTAG_INTRP_TDO 34B7> 35B3<
JTAG_ASIC_TDI 8A4<> 34B7< 59D7>
INT_TST_PLLEN_PD 34B7<
R574 1K NOSTUFF
R276 1K NOSTUFF
R708 1K NOSTUFF
R735 1K NOSTUFF
R727 1K NOSTUFF
R661 1K NOSTUFF
R577 1K NOSTUFF
R573 1K NOSTUFF

TOO MANY MODS TO LIST, SEE INTREPID ERS
CONFIGURED FOR INTREPID VERSION 1
VIEW AGP CLOCK OUT LA CLOCK PIN
+3V_MAIN
GPIO & INTERRUPT PULL-UPS
R746 10K 1% 1/16W MF 402
AGP_INT_L 17B6<> 28B5<>
R749 10K
33SLOTB_INT_L
R750 10K
28B5<> UNUSED_EXTINT7 SPARE
R306 10K
28B5<> UNUSED_EXTINT8 SPARE
RP113 10K 5% 1/16W SM1
INT_GPIO9_PU 28B5<>
INT_EXTINT12_PU 28B5<>
INT_EXTINT17_PU 28B5<> 32B6>
INT_EXTINT3_PU 28B5<>
COMM_RING_DET_L 28B5<> 29C5<>
INT_EXTINT13_PU 28B5<> 59D5>
NC_RPT77P6 NO_TEST
PMU_INT_L 28B5<> 44B5<>
RP74 10K
NC_CBUS_INT_L NO_TEST
PMU_INT_NMI 28B5<> 44C4<>
PMU_REQ_L 28C3> 44C2<
EXTINT14 28B5<>
RP100 10K
NC_RP2848 NO_TEST
INT_GPIO12_PU 28B5<>
INT_GPIO1_PD 28C5<>
SND_HW_RESET_L 28B5<> 39B4<
RP110 10K
R589 10K 1% 1/16W MF 402
USB2_CRUN_L_INT 28B5<> 32A8<
R680 10K 1% 1/16W MF 402
INT_MOD_DTI 28A3< 28C6<
INT_MOD_CLKOUT 28A3> 28C6<
INT_MOD_DTO 28A3> 28C6<
INT_MOD_BITCLK 28A3<> 28C6<
INT_MOD_SYNC 28A3<> 28C6<
RP66 10K NOSTUFF

(518S0104)
J23 U.FL-R_SMT F-ST-SM
CLK18M_INT_EXT 59A5> 44B2<> 32A8< 31C2< PMU_PME_L
R666 0 NOSTUFF
R611 51 1% NOSTUFF
CLK18M_INT_XIN
CLK18M_INT_XOUT
44C4<> SYSTEM_CLK_EN
R672 10M NOSTUFF
44C5<> INT_WATCHDOG_L
R711 0
NC_BRCLKO
Y5 18.432M CRITICAL 8X4.5MM-SM
R710 10K 1%
CLK18M_INT_XO
C784 27PF 5% 50V CERM 402
C840 27PF 5% 50V CERM 402
INT_REF_CLK_IN_PD 53A6<

L16 FERR-EMI-100-OHM SM
+3V_MAIN
52A3> +3V_INTREPID_USB
C785 0.01UF 20% 16V CERM 402
C795 0.1UF 20% 10V CERM 402
C820 4.7UF N20P80% 10V CERM 805

U25 INTREPID BGA (6 OF 9) SEE_TABLE (ON PAGE 12)
VDDU33_1 T8
VDDU33_2 U8
PCI VDD15A_1 (PLL1) AA16
PCI VDD15A_2 (PLL2) AJ12
PCI VDD15A_3 (PLL3) AJ17
PCI VDD15A_7 (PLL7) AJ18
PCI VDD15A_8 (PLL9) AG29

GENERAL PURPOSE I/O'S
28D3< SNF_FSEL G5 GPIO0
28A8< INT_GPIO1_PD E1 GPIO1
59D5> 29D7<> 28D1< COMM_SHUTDOWN J7 GPIO2
59A7> 29D5<> COMM_RESET_L F2 GPIO3
36C8< FWPHYRST J8 GPIO4
41A7< SND_HP_MUTE_L H5 GPIO5
43C8< SND_AMP_MUTE_L L9 GPIO6
28B8< INT_GPIO9_PU H4 GPIO9
39B4< 28A8< SND_HW_RESET_L J5 GPIO11
28A8< INT_GPIO12_PU K8 GPIO12
59A5> 28C1< UNUSED_GPIO15 F1 GPIO15
35B8< 28D1< INT_ENET_RST_L K7 GPIO16

59D5> 44C5> 29C5<> 28B8< COMM_RING_DET_L F33 EXTINT0
44B5<> 28B8< PMU_INT_L E34 EXTINT1
28B8< 17B6<> AGP_INT_L C33 EXTINT2
28B8< INT_EXTINT3_PU D34 EXTINT3
59B5> 40D4< SND_LIN_SENSE_L B33 EXTINT4
35B4> 28C1< ENET_ENERGY_DET A33 EXTINT5
33SLOTB_INT_L E31 EXTINT6
28B8<> UNUSED_EXTINT7 G30 EXTINT7
28B8<> UNUSED_EXTINT8 D31 EXTINT8
44C4<> 28A8< PMU_INT_NMI C32 EXTINT9
28D3< VCORE_VGATE B32 EXTINT10
32A8< 28A8< USB2_CRUN_L_INT E30 EXTINT11
28B8< INT_EXTINT12_PU J9 EXTINT12
28B8< INT_EXTINT13_PU F4 EXTINT13
28A8< INT_EXTINT14 D1 EXTINT14
59B7> 41A5< SND_HP_SENSE_L E2 EXTINT15
42B8< SND_SPKR_ID H7 EXTINT16
32B6> 28B8< INT_EXTINT17_PU G4 EXTINT17
8D7<> 7A5< 4B3< MPIC_CPU_INT_L D38 CPU_INT
INTERRUPTS

59A5> 44B2<> 32A8< 31C2< PMU_PME_L A37 PCIPME
44B4<> INT_PROC_SLEEP_REQ_L AT6 PROCSLEEPREQ
44B4<> INT_PEND_PROC_INT AN8 PENDPROCINT

CLK18M_INT_XIN U4 XTAL_IN
CLK18M_INT_XOUT V15 XTAL_OUT
44C4<> SYSTEM_CLK_EN AN7 STOPXTAL
AT7 WATCHDOG
U15 BUF_REF_CLK_OUT
K9 SS_REF_CLK_IN
CLOCKS

USB
SCCTXDA AF9 COMM_TXD_L 29C7<> 59C5>
SCCRTSA AN3 COMM_RTS_L 29D5<> 59C5>
SCCDTRA AF10 COMM_DTR_L 29C7<> 59C5>
SCCRXDA AG11 COMM_RXD 29C5<> 59C5>
SCCGPIOA AG9 COMM_GPIO_L 28D3< 29C5<> 59C5>
VIA SCCTRXCA AT4 COMM_TRXC 28D3< 29C7<> 59C5>
MISO SCCTXDB AR4 PMU_FROM_INT 44C4<>
REQ* SCCRTSB AL5 PMU_REQ_L 28A8< 44C2<
MOSI SCCRXDB AG10 PMU_TO_INT 44C4<>
ACK* SCCGPIOB AP4 PMU_ACK_L 44C4<>
SCK SCCTRXCB AM5 PMU_CLK 44C4<>

USB_VD0_P L8 58B5> 28A3< USB_DAP 402 24 R724 USB1 USB_DAP_F 33B7< 58B5>
USB_VD0_N L7 58B5> 28A3< USB_DAN 402 24 R718 USB1 USB_DAN_F 33B7< 58B5>
USB_VD1_P G2 58B5> 28A3< USB_DBP 402 24 R736 USB1 USB_DBP_F 33C7< 58B5>
USB_VD1_N G1 58B5> 28A3< USB_DBN 402 24 R742 USB1 USB_DBN_F 33C7< 58B5>
USB_PRTPWR0 J4 USB_PWREN_AB_L 28C2<
USB_PWRFLT0 K4 USB_PWR_FLT* 28C1< 32B1< 33A7>
USB_VD2_P H2 58B5> 28A3< USB_DCP 402 24 R723 USB1 USB_DCP_F 33D7< 58B5>
USB_VD2_N H1 58B5> 28A3< USB_DCN 402 24 R728 USB1 USB_DCN_F 33D7< 58B5>
USB_VD3_P M7 USB_DDP 402 24 R694 USB_DDP_F_TERM
USB_VD3_N M8 USB_DDN 402 24 R691 USB_DDN_F_TERM
USB_PRTPWR1 J2 USB_PWREN_CD_L 28C2<
USB_PWRFLT1 J1
USB_VD4_P K5 58B5> USB_DEP 402 22 R762 BT_USB_DP 29D3<> 58B5> 59B5>
USB_VD4_N L5 58B5> USB_DEN 402 22 R763 BT_USB_DM 29D3<> 58A5> 59B5>
USB_VD5_P P8 58A5> USB_DFP 402 22 R271 MODEM_USB_DP 29C5<> 58A5> 59B5>
USB_VD5_N N8 58A5> USB_DFN 402 22 R272 MODEM_USB_DM 29C5<> 58A5> 59B5>
USB_PRTPWR2 M5 USB_PWREN_EF_L 28C2<
USB_PWRFLT2 N7 USB_OC_EF_L 28C2<

USB PULL-UPS
+3V_MAIN
RP60 10K
28B3< USB_OC_EF_L
28B3<> USB_PWREN_CD_L
28B3<> USB_PWREN_AB_L
28B3<> USB_PWREN_EF_L

+3V_MAIN
59A5> 28B5<> UNUSED_GPIO15
R294 10K 1% 1/16W MF 402
NOSTUFF R267 10K

AUDIO/I2S
AUD_DTO R4 INT_SND_TO_AUDIO 47 4 RP108 SND_TO_AUDIO 39C4<
AUD_DTI R7 AUDIO_TO_SND AUDIO_TO_SND 39C1<
AUD_SYNC T5 INT_SND_SYNC 47 2 RP108 SND_SYNC 39C1<>
AUD_BITCLK P2 INT_SND_SCLK 47 3 RP108 SND_SCLK 39B1<>
AUD_CLKOUT R5 INT_SND_CLKOUT 47 1 RP108 SND_CLKOUT 39B4<
MOD_DTO R2 INT_MOD_DTO 28A8< 28C6<
MOD_DTI T4 INT_MOD_DTI 28A8< 28C6<
MOD_SYNC R1 INT_MOD_SYNC 28A8< 28C6<
MOD_BITCLK V8 INT_MOD_BITCLK 28A8< 28C6<
MOD_CLKOUT P1 INT_MOD_CLKOUT 28A8< 28C6<
R3001 15K R3002 15K R650 15K R651 15K R660 10K R683 10K

IIC
IICCLK_2 AL4 INT_I2C_CLK2 28D1< 29C7<> 34B5< 39B1<> 59A7>
IICDATA_2 AH8 INT_I2C_DATA2 28D1< 29C7<> 34B5< 39B1<> 59A7>

58B5> 28B3<> USB_DAP 402 15K R305 USB2
58B5> 28B3<> USB_DAN 402 15K R396 USB2
58B5> 28B3<> USB_DBP 402 15K R247 USB2
58B5> 28B3<> USB_DBN 402 15K R398 USB2
58B5> 28B3<> USB_DCP 402 15K R333 USB2
58B5> 28B3<> USB_DCN 402 15K R493 USB2

VSSA1 (PLL1) AA15
VSSA2 (PLL2) AJ13
VSSA3 (PLL3) AJ16
VSSA4 (PLL7) AK18
VSSA_8 (PLL9) AH20
VSSU_1 R9
VSSU_2 R8
XW42 XW43 XW44 XW45 XW46
28C4< INT_PLL1_GND NO_TEST
28D4< INT_PLL2_GND NO_TEST
NO_TEST INT_PLL9_GND 28D4<
NO_TEST INT_PLL7_GND 28D4<
NO_TEST INT_PLL3_GND 28D4<

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INTREPID GPIO/ SCC/USB/I2S

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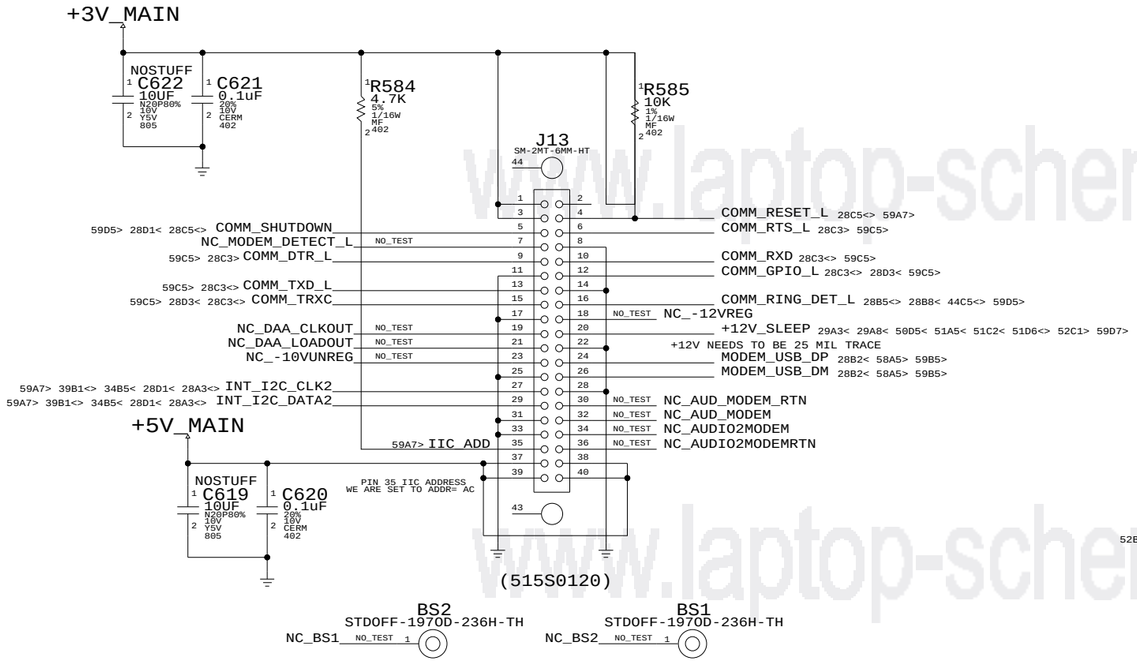
DRAWING

MODEM BOARD CONNECTOR

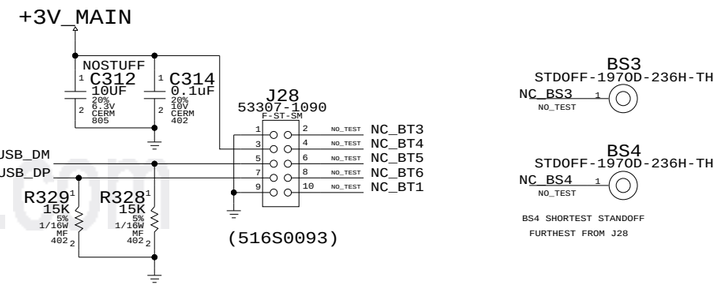
(DASH II)



MODEM STANDOFF SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1034	2	STDOFF-19709-236H-TH	BS1,BS2		

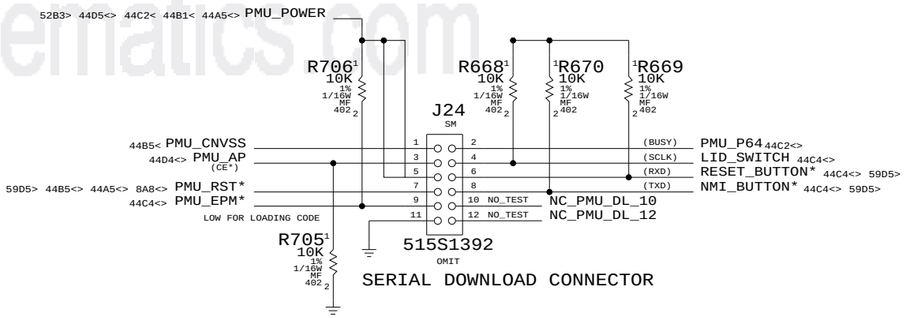
BLUETOOTH CONNECTOR



BLUETOOTH CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-0170	1	STDOFF,BLUETOOTH,SHORT	BS4		
860-0171	1	STDOFF,BLUETOOTH,LONG	BS3		

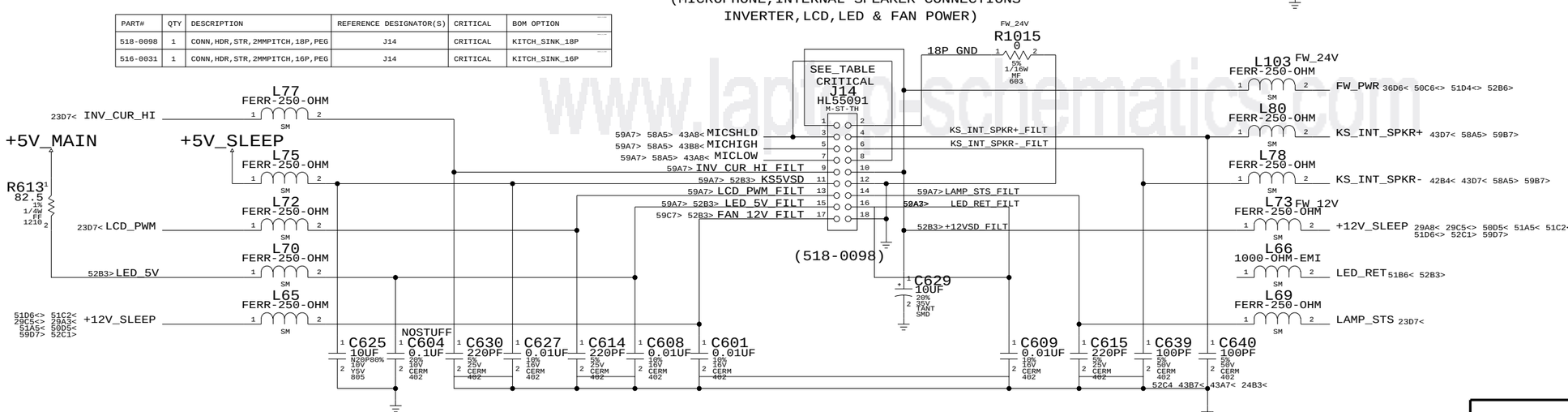
SERIAL DOWNLOAD INTERFACE



'KITCHEN SINK' CONNECTOR

(MICROPHONE,INTERNAL SPEAKER CONNECTIONS
INVERTER,LCD,LED & FAN POWER)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0098	1	CONN,HDR,STR,2MMPITCH,18P,PEG	J14	CRITICAL	KITCH_SINK_18P
516-0031	1	CONN,HDR,STR,2MMPITCH,16P,PEG	J14	CRITICAL	KITCH_SINK_16P



MODEM, BLUETOOTH, KITCHEN SINK & SERIAL DOWNLOAD

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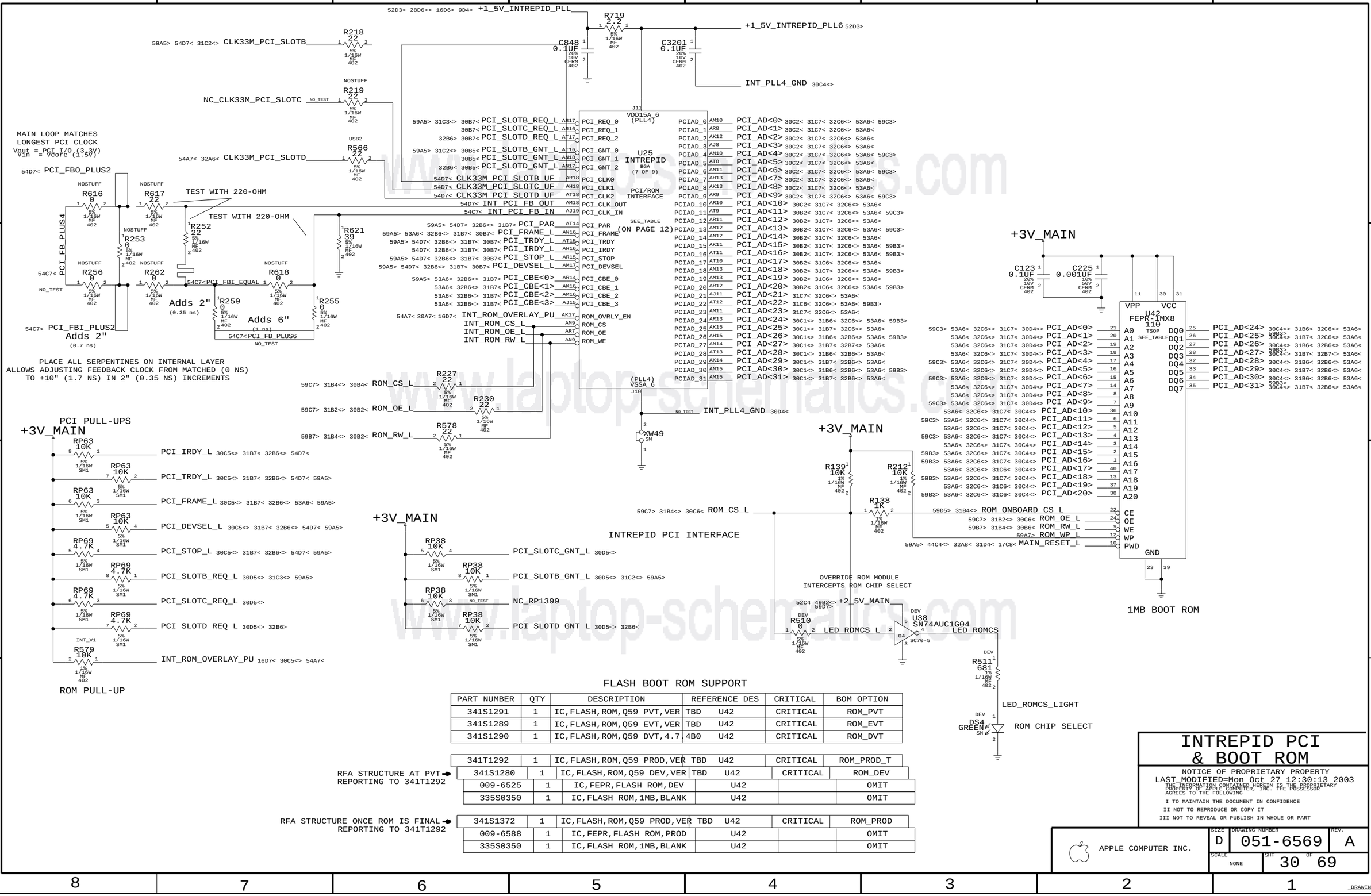

FLASH BOOT ROM SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1291	1	IC,FLASH,ROM,Q59 PVT,VER	TBD U42	CRITICAL	ROM_PVT
341S1289	1	IC,FLASH,ROM,Q59 EVT,VER	TBD U42	CRITICAL	ROM_EVT
341S1290	1	IC,FLASH,ROM,Q59 DVT,4.7	4B0 U42	CRITICAL	ROM_DVT
341T1292	1	IC,FLASH,ROM,Q59 PROD,VER	TBD U42	CRITICAL	ROM_PROD_T
341S1280	1	IC,FLASH,ROM,Q59 DEV,VER	TBD U42	CRITICAL	ROM_DEV
009-6525	1	IC,FEPR,FLASH ROM,DEV	U42		OMIT
335S0350	1	IC,FLASH ROM,1MB,BLANK	U42		OMIT
341S1372	1	IC,FLASH,ROM,Q59 PROD,VER	TBD U42	CRITICAL	ROM_PROD
009-6588	1	IC,FEPR,FLASH ROM,PROD	U42		OMIT
335S0350	1	IC,FLASH ROM,1MB,BLANK	U42		OMIT

RFA STRUCTURE AT PVT
REPORTING TO 341T1292

RFA STRUCTURE ONCE ROM IS FINAL
REPORTING TO 341T1292

INTREPID PCI & BOOT ROM

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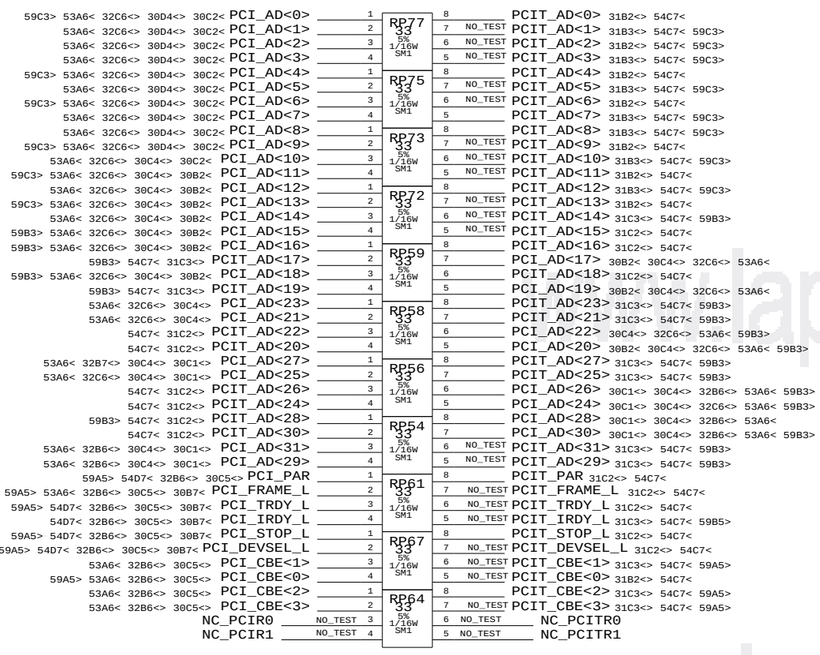
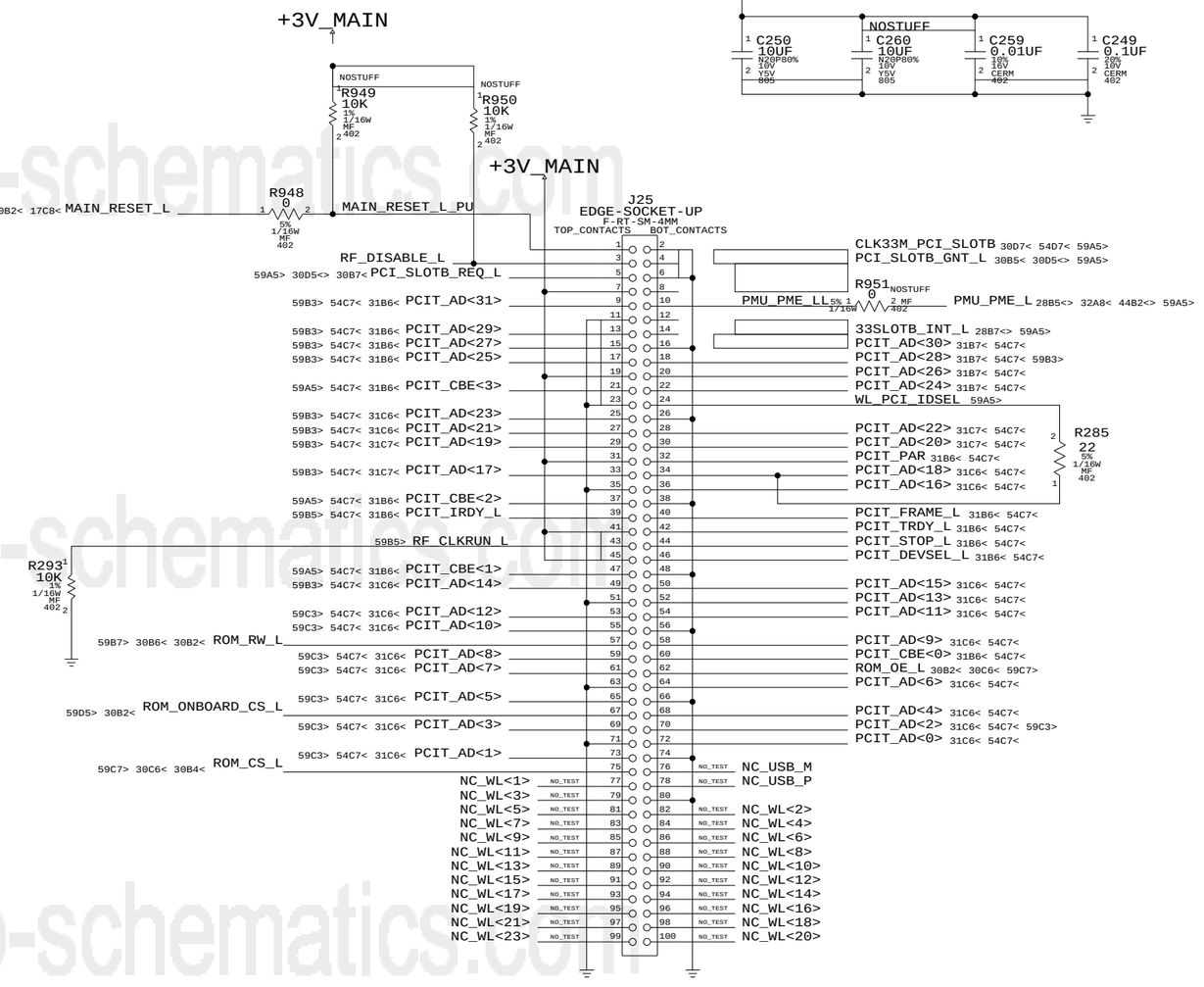
PLACE RP'S NEAR WIRELESS CONNECTOR





(516S0046)

WIRELESS CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
815-7245	1	WIRELESS CARD GUIDE,J25	J251		
452-0411	2	NUT,HEX,M2 X 1.5H, J25	J252,J253		
452-0412	2	SCREW,M2 X 0.4 X 6.0 L,J25	J254,J255		

WIRELESS PCI

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DRAWING

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+3V_MAIN

USB2 C519 0.1UF 20% 10V CERM 402
USB2 C522 0.1UF 20% 10V CERM 402
USB2 C527 0.1UF 20% 10V CERM 402
USB2 C547 0.1UF 20% 10V CERM 402
USB2 C523 0.1UF 20% 10V CERM 402
USB2 C541 0.1UF 20% 10V CERM 402
USB2 C548 0.1UF 20% 10V CERM 402
USB2 C555 0.1UF 20% 10V CERM 402
USB2 C559 0.1UF 20% 10V CERM 402
USB2 C546 0.1UF 20% 10V CERM 402
USB2 C516 0.1UF 20% 10V CERM 402
USB2 C537 0.1UF 20% 10V CERM 402
USB2 C536 0.1UF 20% 10V CERM 402
USB2 C515 0.1UF 20% 10V CERM 402
USB2 C570 0.1UF 20% 10V CERM 402
USB2 C530 0.1UF 20% 10V CERM 402
NOSTUFF C517 10UF N20P80% 10V Y5V 805
USB2 C573 10UF N20P80% 10V Y5V 805
NOSTUFF C574 10UF N20P80% 10V Y5V 805
USB2 C531 10UF N20P80% 10V Y5V 805

+3V_MAIN

USB2 L58 100-OHM-EMI SM

52A3> NEC_AVDD

USB2 C526 0.1UF 20% 10V CERM 402
USB2 C529 0.1UF 20% 10V CERM 402
USB2 C511 10UF N20P80% 10V Y5V 805

NOSTUFF R89 100K 1% 1/16W MF 402

NEC_XT2_B

Y7 30.0000M CRITICAL 8X4.5MM-SM USB2

USB2 C77 10PF 5% 50V CERM 402
USB2 C114 10PF 5% 50V CERM 402

USB2 R129 100 1% 1/16W MF 402

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 N12 — AVDD
USB2

VDD_PCI

59C3> 53A6< 31C7< 30D4<> 30C2< PCI_AD<0> M5 AD0
53A6< 31C7< 30D4<> 30C2< PCI_AD<1> P5 AD1
53A6< 31C7< 30D4<> 30C2< PCI_AD<2> N5 AD2
53A6< 31C7< 30D4<> 30C2< PCI_AD<3> P4 AD3
59C3> 53A6< 31C7< 30D4<> 30C2< PCI_AD<4> N4 AD4
53A6< 31C7< 30D4<> 30C2< PCI_AD<5> M3 AD5
59C3> 53A6< 31C7< 30D4<> 30C2< PCI_AD<6> N3 AD6
53A6< 31C7< 30D4<> 30C2< PCI_AD<7> M1 AD7
53A6< 31C7< 30D4<> 30C2< PCI_AD<8> L2 AD8
59C3> 53A6< 31C7< 30D4<> 30C2< PCI_AD<9> L1 AD9
53A6< 31C7< 30C4<> 30C2< PCI_AD<10> K2 AD10
59C3> 53A6< 31C7< 30C4<> 30B2< PCI_AD<11> L3 AD11
53A6< 31C7< 30C4<> 30B2< PCI_AD<12> K1 AD12
59C3> 53A6< 31C7< 30C4<> 30B2< PCI_AD<13> K3 AD13
53A6< 31C7< 30C4<> 30B2< PCI_AD<14> J2 AD14
59B3> 53A6< 31C7< 30C4<> 30B2< PCI_AD<15> J1 AD15
59B3> 53A6< 31C7< 30C4<> 30B2< PCI_AD<16> F2 AD16
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53A6< 31C6< 30C4<> 30B2< PCI_AD<19> D3 AD19
59B3> 53A6< 31C6< 30C4<> 30B2< PCI_AD<20> D1 AD20
53A6< 31C7< 30C4<> PCI_AD<21> D2 AD21
59B3> 53A6< 31C6< 30C4<> PCI_AD<22> C2 AD22
53A6< 31C7< 30C4<> PCI_AD<23> C1 AD23
59B3> 53A6< 31B6< 30C4<> 30C1<> PCI_AD<24> B4 AD24
53A6< 31B7< 30C4<> 30C1<> PCI_AD<25> A4 AD25
59B3> 53A6< 31B6< 30C4<> 30C1<> PCI_AD<26> B5 AD26
53A6< 31B7< 30C4<> 30C1<> PCI_AD<27> C4 AD27
53A6< 31B6< 30C4<> 30C1<> PCI_AD<28> A5 AD28
53A6< 31B7< 30C4<> 30C1<> PCI_AD<29> C5 AD29
59B3> 53A6< 31B6< 30C4<> 30C1<> PCI_AD<30> B6 AD30
53A6< 31B7< 30C4<> 30C1<> PCI_AD<31> A6 AD31

59A5> 53A6< 31B7< 30C5<> PCI_CBE<0> M2 CBE0
53A6< 31B7< 30C5<> PCI_CBE<1> J3 CBE1
53A6< 31B7< 30C5<> PCI_CBE<2> F1 CBE2
53A6< 31B7< 30C5<> PCI_CBE<3> C3 CBE3

59A5> 54D7< 31B7< 30C5<> PCI_PAR J4 PAR
59A5> 53A6< 31B7< 30C5<> 30B7< PCI_FRAME_L F3 FRAME
54D7< 31B7< 30C5<> 30B7< PCI_IRDY_L F4 IRDY
59A5> 54D7< 31B7< 30C5<> 30B7< PCI_TRDY_L G1 TRDY
59A5> 54D7< 31B7< 30C5<> 30B7< PCI_STOP_L G3 STOP
USB2 IDSEL B3 IDSEL
59A5> 54D7< 31B7< 30C5<> 30B7< PCI_DEVSEL_L G2 DEVSEL
30D5<> 30B7< PCI_SLOTD_REQ_L C6 REQ
30D5<> 30B5< PCI_SLOTD_GNT_L D6 GNT
PCI_SLOTD_PERR_L H2 PERR
33PCI_SLOTD_SERR_L OD H1 SERR
28B8< 28B5<> INT_EXTINT17_PU OD C7 INTA
OD B7 INTB
OD A7 INTC
54A7< 30D7< CLK33M_PCI_SLOTD A8 PCLK

59A7> 44D3< 44B8<> 35B8< IO_RESET_L B8 VBBRST — STARTUP & RESTARTS
USB2_CRUN_L N6 CRUN
USB2_PME_L OD D9 PME
C9 VCCRST — STARTUP, RESTARTS, WAKEUP
NC_USB2_SMI_L OD L6 SMI
L7 LEGC

VSS — B1 N1 P10 N14 H14 B14 A2 B2 N2 M13 B13 M11 L12 H12 D12 G4 J11 F11 D8

U11
NEC_UPD720101_USB2
FBGA

CRITICAL

XT1/SCLK L9 56B3> USB2_XT1
XT2 P8 56B3> USB2_XT2

RSDM1 M14 56B3> USB2_RSDAM — R464 35.7 — USB2_DAN_F 33B7< 56B3>
DM1 M13 USB2_DAN_F
DP1 L14 USB2_DAP_F — R465 35.7 — USB2_DAP_F 33B7< 56B3>
RSDP1 K13 56B3> USB2_RSDAP
RSDM2 K14 56B3> USB2_RSDBM — R466 35.7 — USB2_DBN_F 33C7< 56B3>
DM2 K12 USB2_DBN_F
DP2 J14 USB2_DBP_F — R467 35.7 — USB2_DBP_F 33C7< 56B3>
RSDP2 J12 56B3> USB2_RSDBP
RSDM3 H11 56B3> USB2_RSDCM — R468 35.7 — USB2_DCN_F 33D7< 56B3>
DM3 G11 USB2_DCN_F
DP3 G13 USB2_DCP_F — R469 35.7 — USB2_DCP_F 33D7< 56B3>
RSDP3 G14 56B3> USB2_RSDCP
RSDM4 F12 NC_USB2_RSDEM
DP4 E12
RSDP4 E14 NC_USB2_RSDEP
RSDM5 E13 NC_USB2_RSDFM
DM5 D14
DP5 C13
RSDP5 C14 NC_USB2_RSDFP

OVERLAP STUFFING OF 35.7OHMS HERE WITH 0OHMS ON SH31 TO MINIMIZE STUBS

56B3> RREF P11 USB2_RREF — R476 9.09K 1% 1/16W MF 402 — TIED TO BALL N11

OCI1 B12 USB_PWR_FLT*
OCI2 B11
OCI3 B10
OCI4 A10 U_USB_PWR_FLT*
OCI5 B9

USB_PWR_FLT* 28B3< 28C1< 33A7>

PPON1 C12 NC_USB2_PPON1
PPON2 A11 NC_USB2_PPON2
PPON3 C11 NC_USB2_PPON3
PPON4 C10 NC_USB2_PPON4
PPON5 A9 NC_USB2_PPON5

R470 2.2K 5% 1/16W MF 402
R490 2.2K 5% 1/16W MF 402

NC1 P6 USB2_NC1
NC2 M6 USB2_NC2

NTEST1 M8 NC_USB2_NTEST1
SMC M7 NC_USB2_SMC
TEB N7 NC_USB2_TEB
AMC P7 NC_USB2_AMC
TEST L8 NC_USB2_TEST
NANDTEST M10 NC_USB2_NANDTEST
SRCLK M9 NC_USB2_SRCLK
SRDTA N9 NC_USB2_SRDTA
SRMOD P9 NC_USB2_SRMOD

AVSS(R) — AVSS — N11 P13 M12

+3V_MAIN

R480 4.7K 5% 1/16W MF 402

+3V_MAIN

R127 4.7K 5% 1/16W MF 402
R128 4.7K 5% 1/16W MF 402
R494 22 5% 1/16W MF 402 — USB2_IDSEL

44B2<> 31C2< 28B5<> 59A5> PMU_PME_L — R484 0 5% 1/16W 402 — USB2_PME_L

28B5<> 28A8< USB2_CRUN_L_INT — R373 NOSTUFF 0 5% 1/16W 402 — USB2_CRUN_L

R78 1K 1% 1/16W MF 402

+3V_MAIN

R1029 4.7K 5% 1/16W MF 402 — D3_HOT

D3_COLD
44C4<> 31D4< 30B2< 17C8< 59A5> MAIN_RESET_L — R1028 0 5% 1/16W MF 402 — USB2_VCCRST

USB2 CONTROLLER

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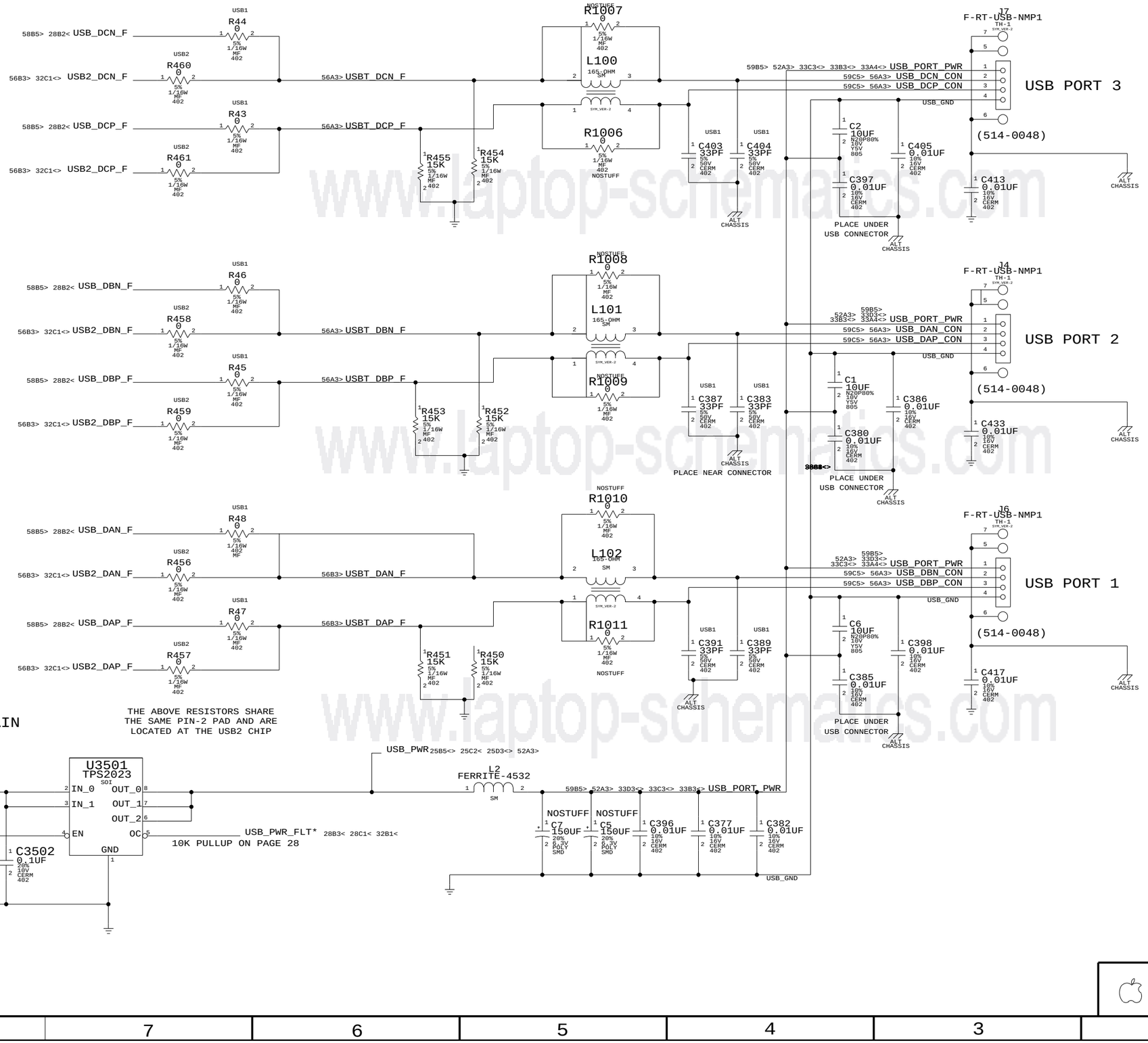
SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 32 OF 69	

DRAWING



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USB CONNS & PWR

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D	051-6569	A
SCALE: NONE	SHT 33 OF 69	

DRAWING

CLKENET_LINK_TX

R307 33 5% 1/16W MF 402
R303 33 5% 1/16W MF 402
RP70 33 1/16W 5% SM1
RP76 33 1/16W 5% SM1

U25 INTREPID BGA (4 OF 9)
SEE_TABLE (ON PAGE 12)

GB ETHERNET
FIREWIRE
MISC
TEST

R714 1K 1% 1/16W MF 402
C92 47PF 5% 50V CERM 402 NOSTUFF

R707 47 5% 1/16W MF 402
R275 47 5% 1/16W MF 402
RP112 22 5% 1/16W SM1
RP65 22 5% 1/16W SM1
R269 22 5% 1/16W MF
R709 22 5% 1/16W MF
R702 22 5% 1/16W MF 402
R673 1K 1% 1/16W MF 402

R257 0 MF 5% 1/16W 402 INT_V2
R254 0 MF 5% 1/16W 402 INT_V2
R637 0 MF 5% 1/16W 402 INT_V1
R647 0 MF 5% 1/16W 402 INT_V1

TEST PULL-DOWNS

R575 1K 1% 1/16W MF 402
R576 1K 1% 1/16W MF 402
R684 10K 1% 1/16W MF 402

I2C 3.3V PULL-UPS

+3V_MAIN

RP119 4.7K 5% 1/16W SM1
RP101 4.7K 5% 1/16W SM1

+3V_MAIN NOSTUFF J18 M-ST-LK TH

(515-1560)
I2C DEBUG HEADER

INTREPID VERSION 1 HAS AN I2C BUS PROBLEM
USE KEY LARGO'S I2C INSTEAD.
FIXED IN INTREPID VERSION 2

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INTREPID ENET & FW

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SIZE	DRAWING NUMBER	REV.
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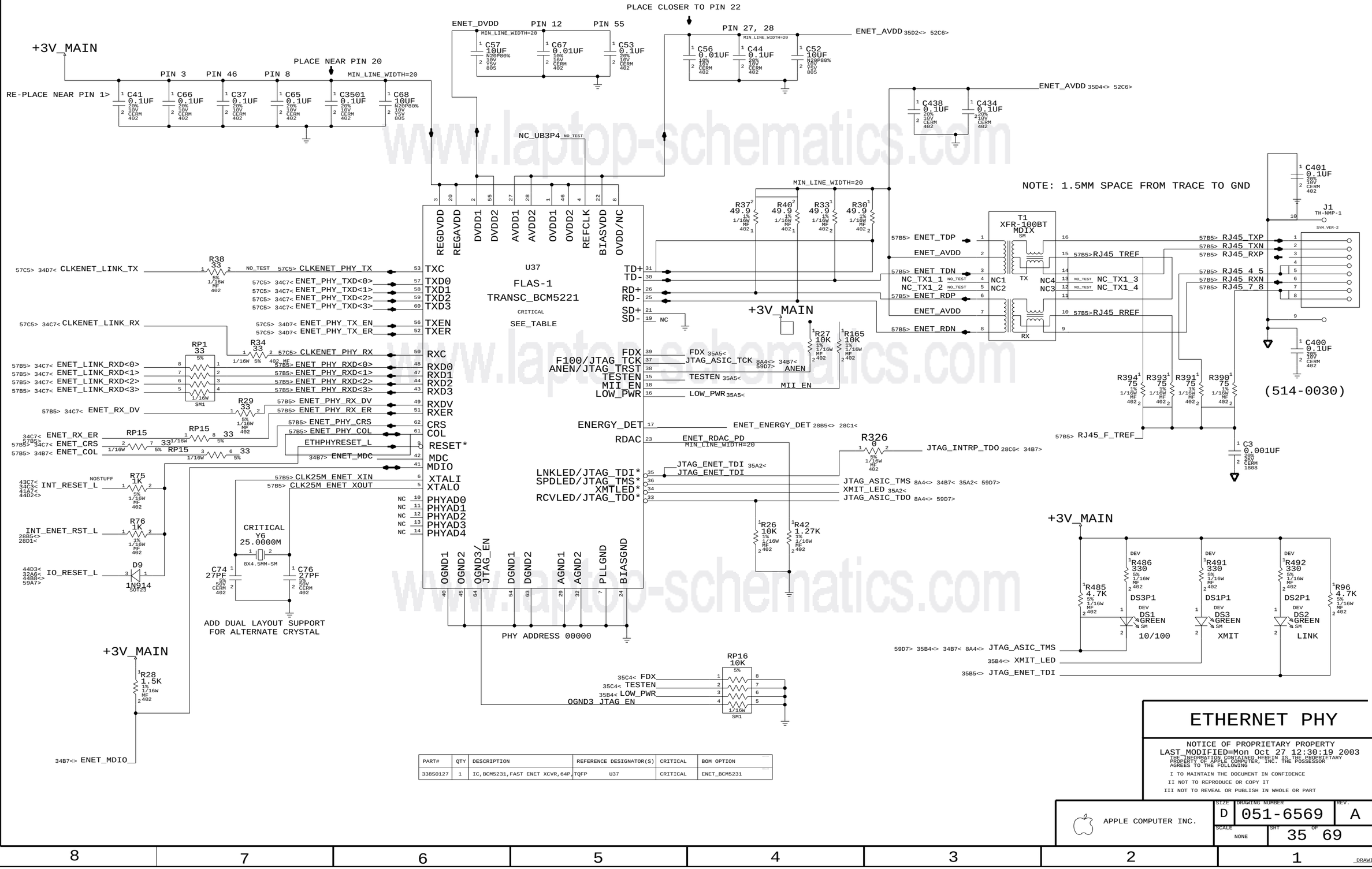
SCALE: NONE
SHT 34 OF 69



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0127	1	IC,BCM5231,FAST ENET XCVR,64P,TQFP	U37	CRITICAL	ENET_BCM5231

ETHERNET PHY

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 35 OF 69	

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
740S0527	2	FUSE,0.75A,30V,SMD	F2,F3	PWRS_Q26
740S0506	2	FUSE,0.5A,SMD	F2,F3	PWRS_Q59

FIREWIRE PHY

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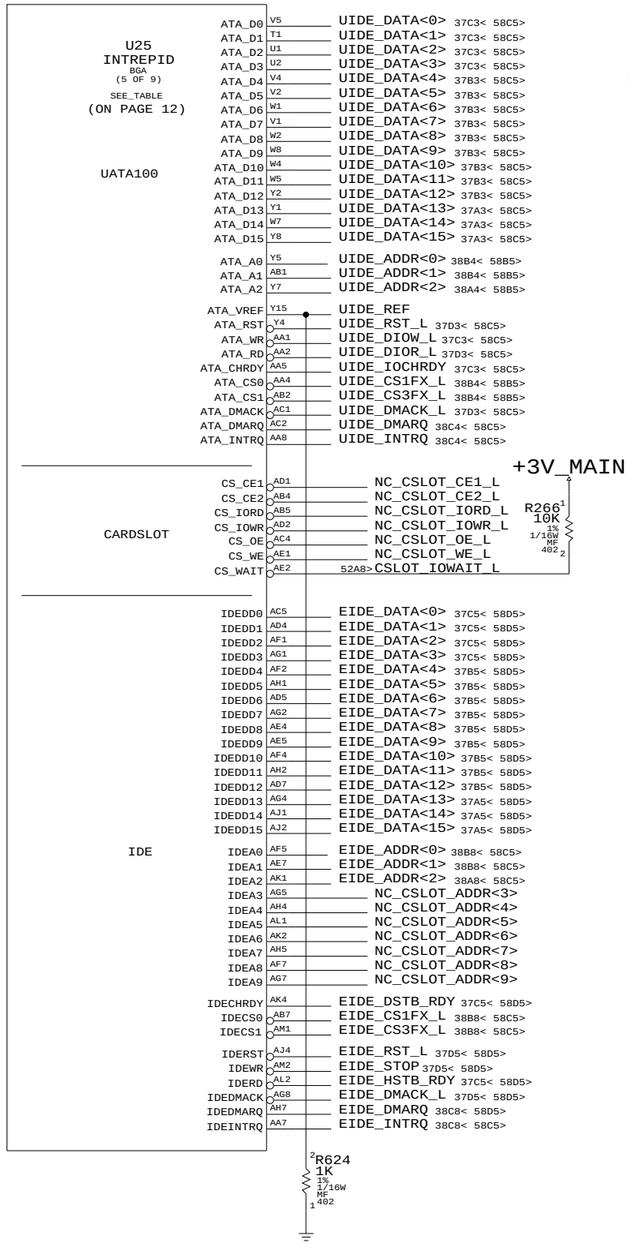
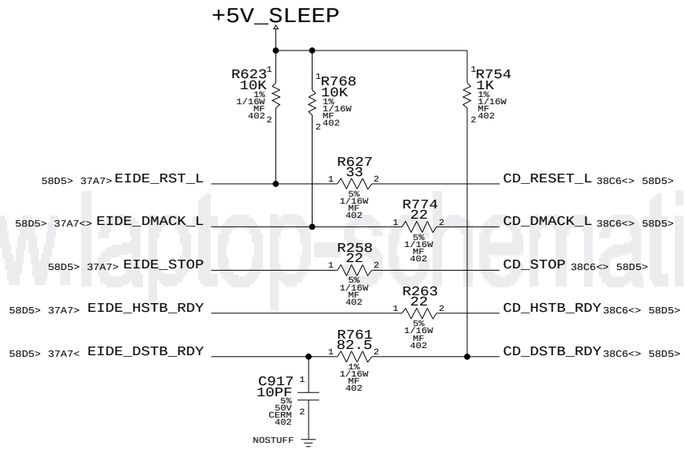
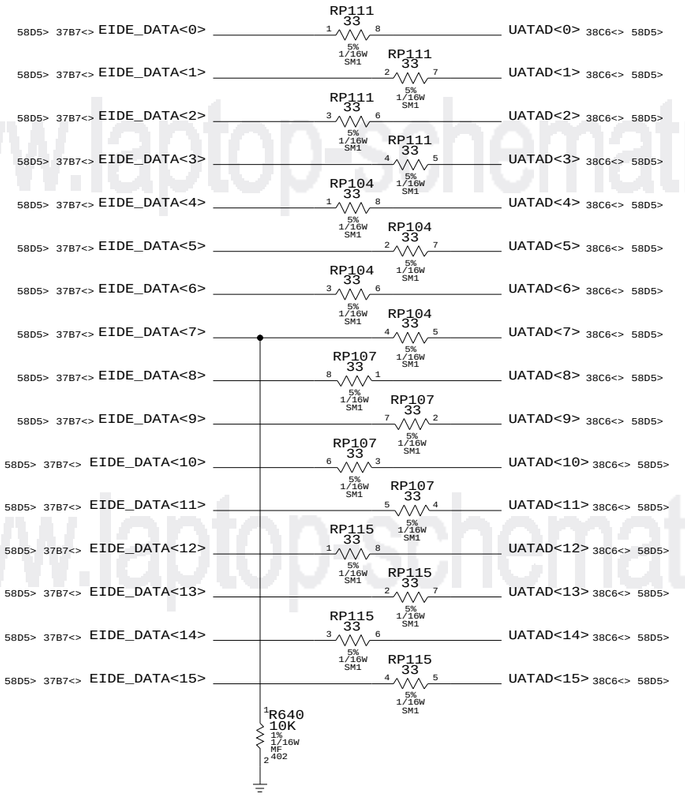
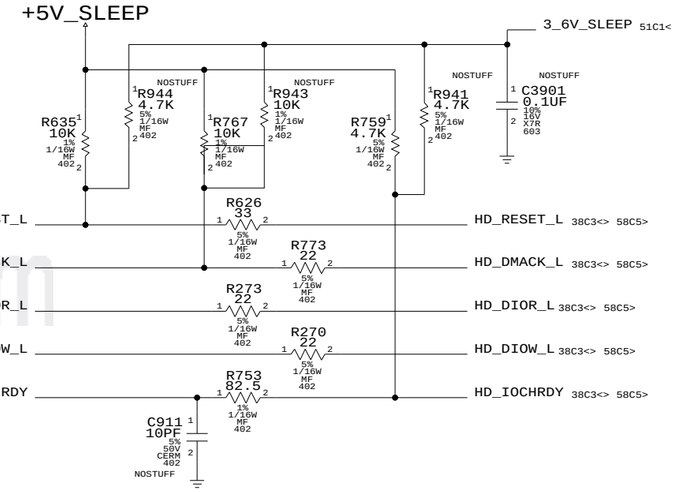
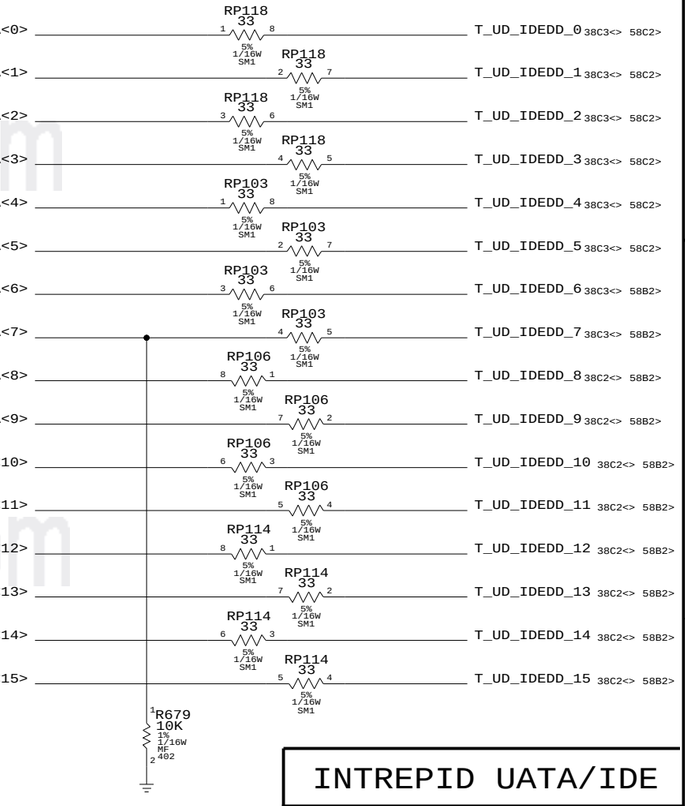
SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 36 OF 69	











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INTREPID UATA/IDE

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D	051-6569	A
SCALE: NONE	SHT 37 OF 69	

DRAWING

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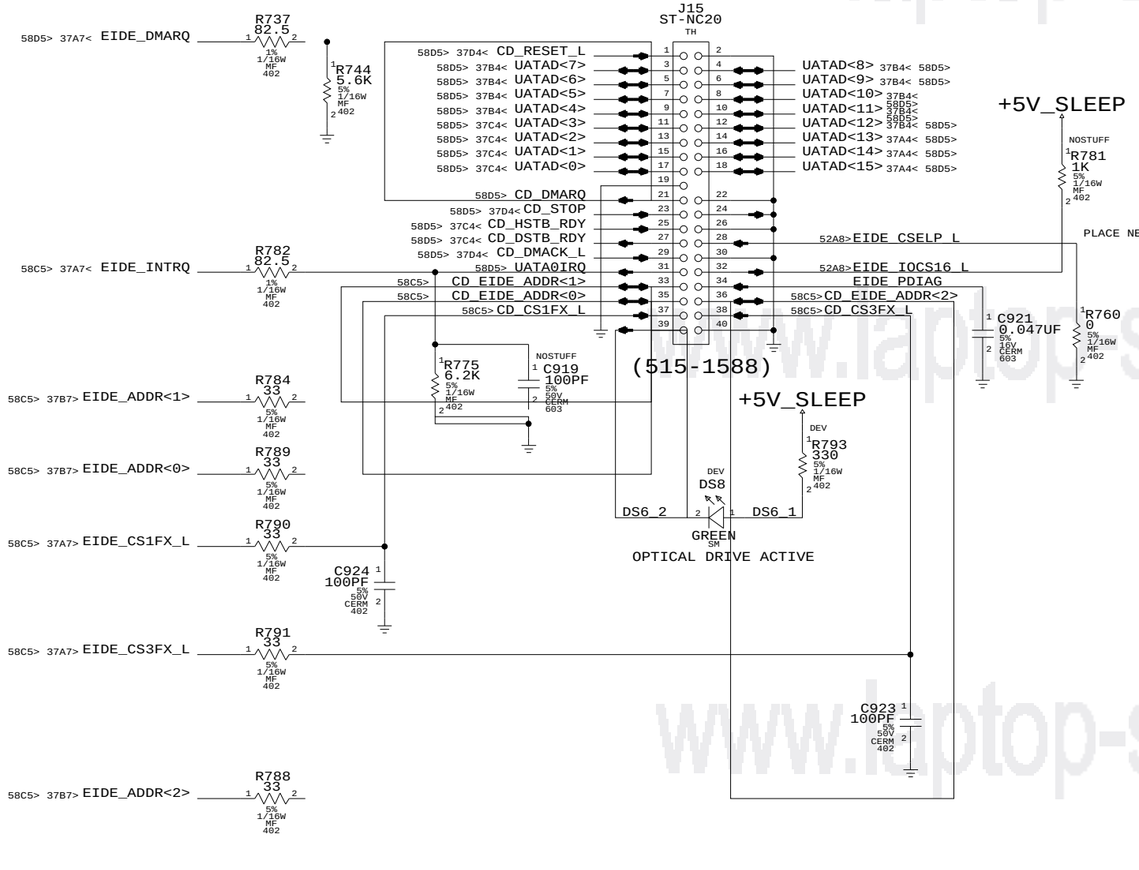
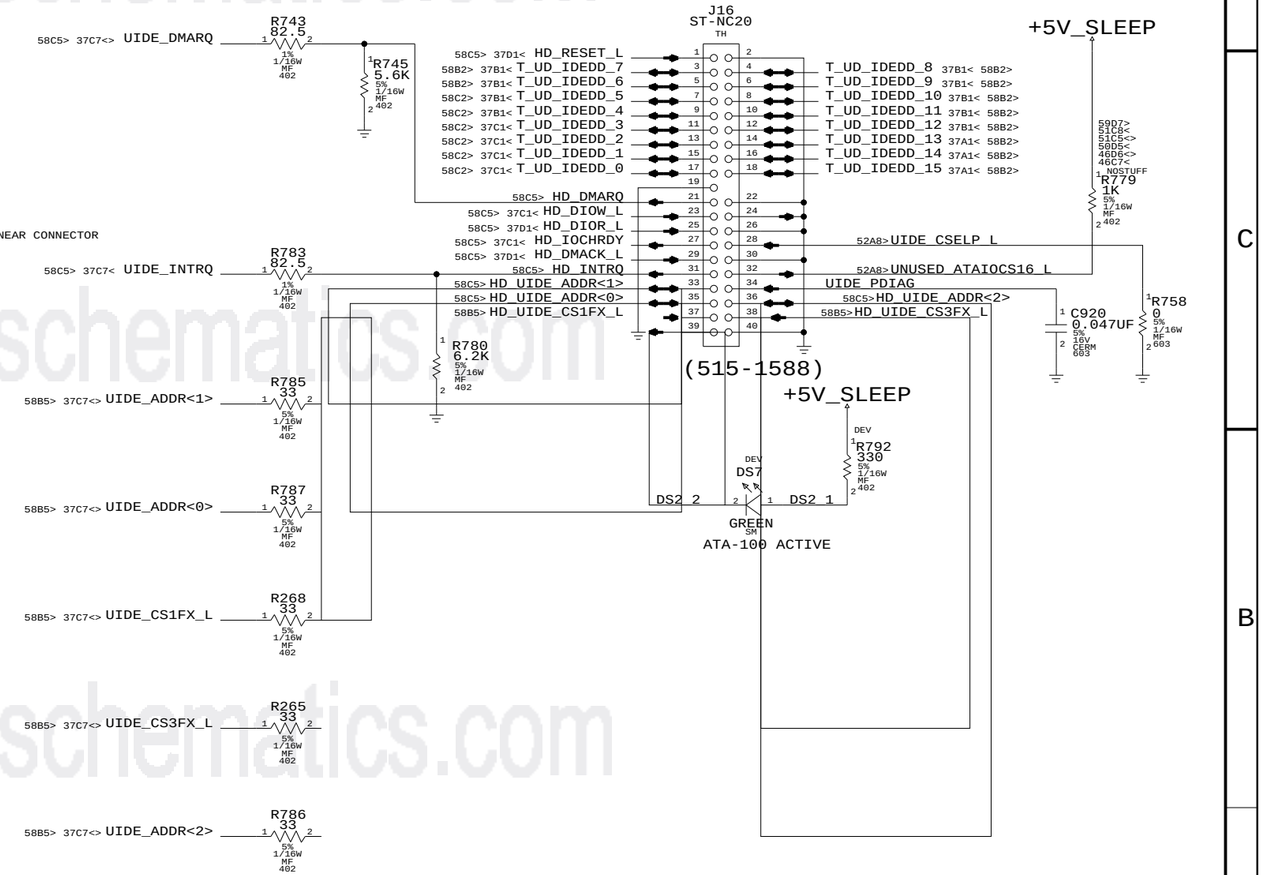
OPTICAL DRIVE INTERFACE



ATA-100 INTERFACE



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CD/HD CONS

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	SCALE NONE	SHT 38 OF 69	

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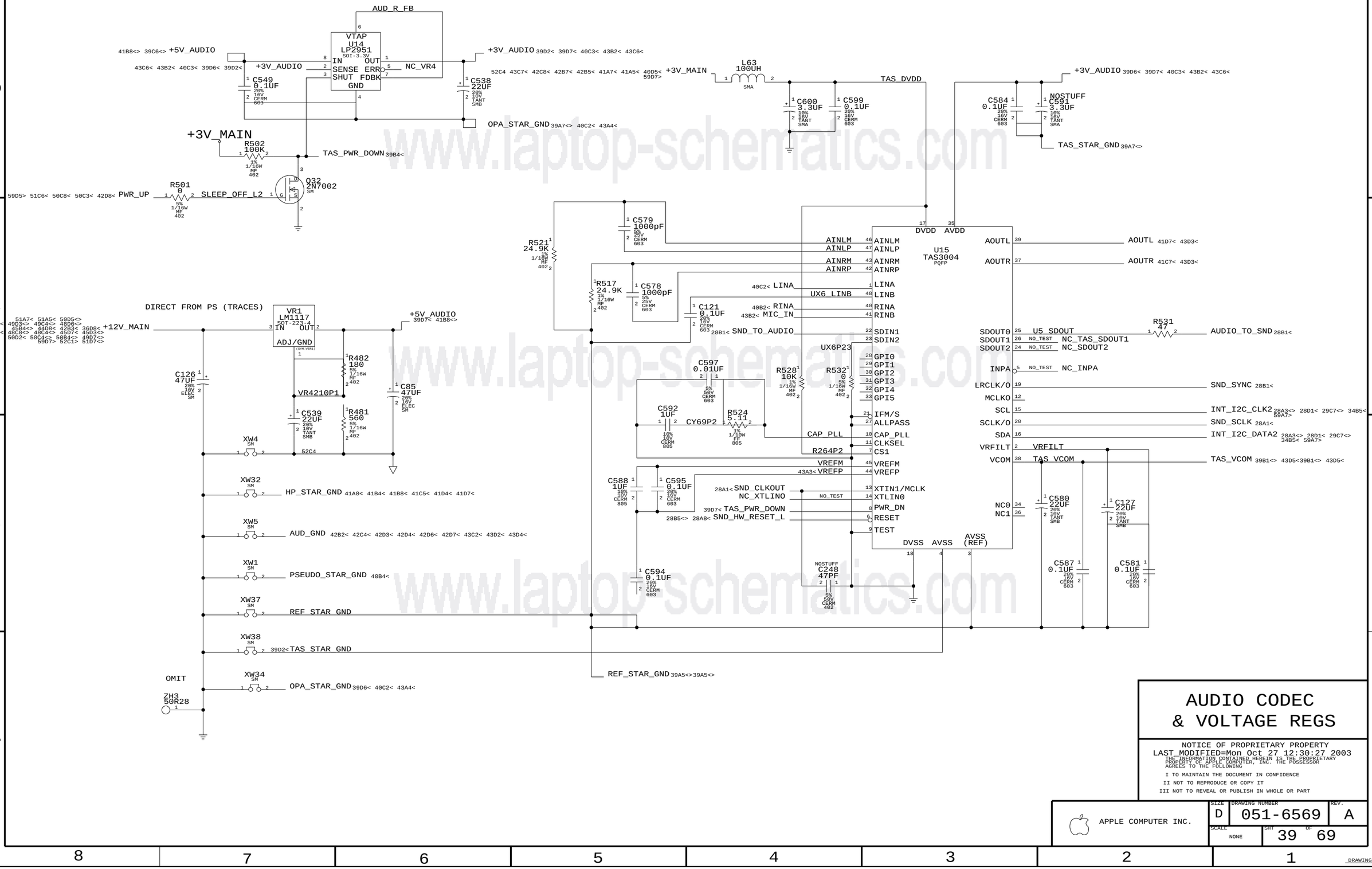

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AUDIO CODEC & VOLTAGE REGS

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D	051-6569	A
SCALE: NONE	SHT 39 OF 69	

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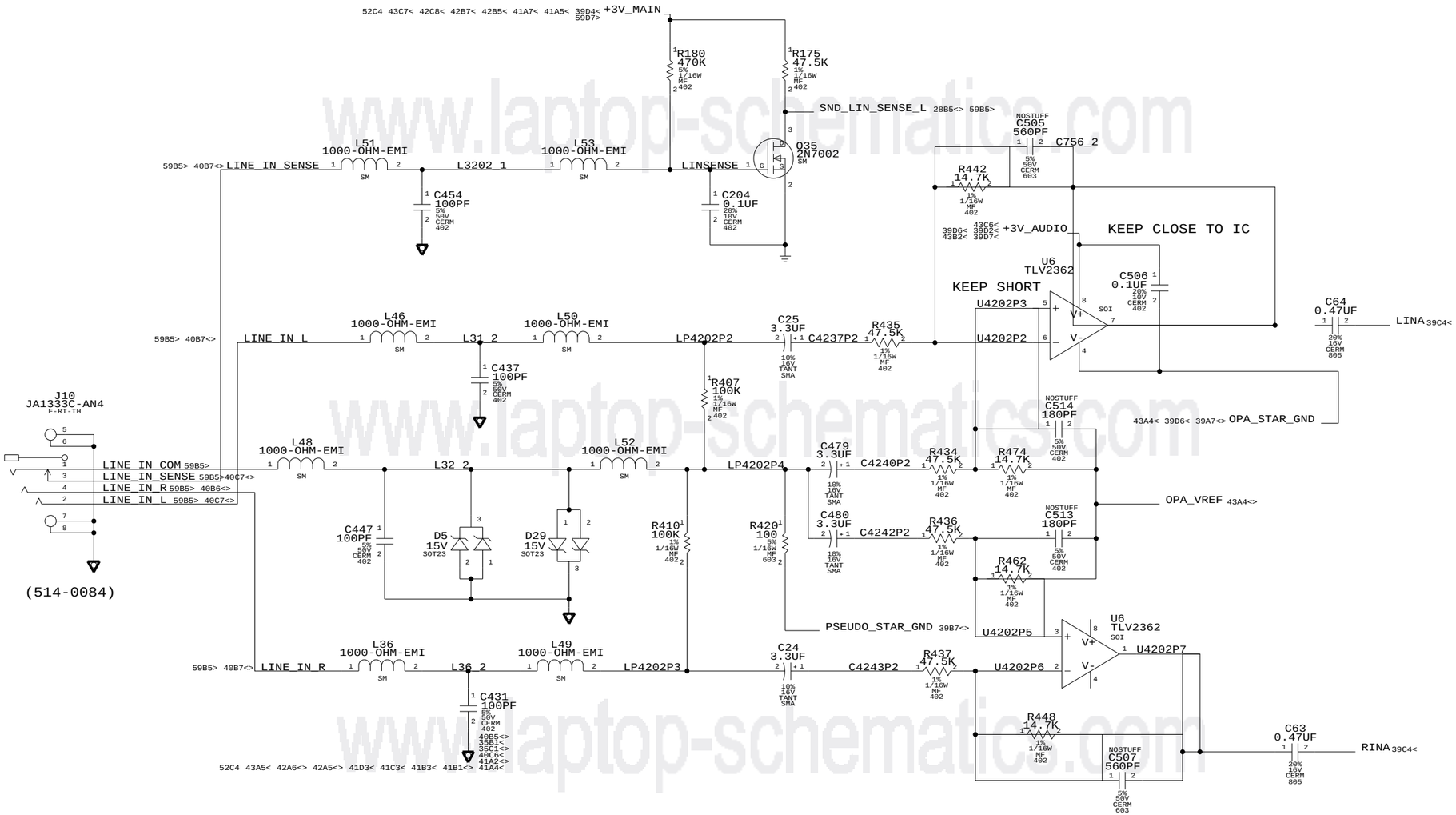

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LINE IN BUFFER

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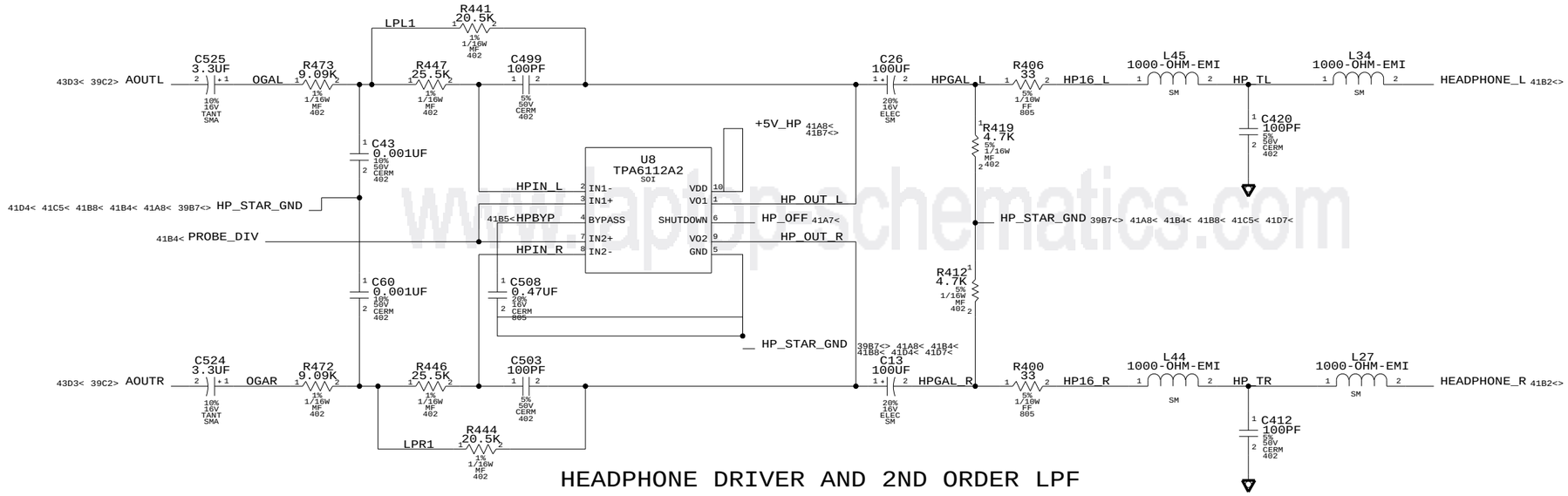
SIZE	DRAWING NUMBER	REV.
D	051-6569	A

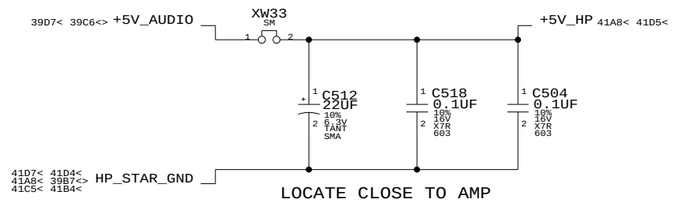
SCALE: NONE

SHT 40 OF 69

DRAWING

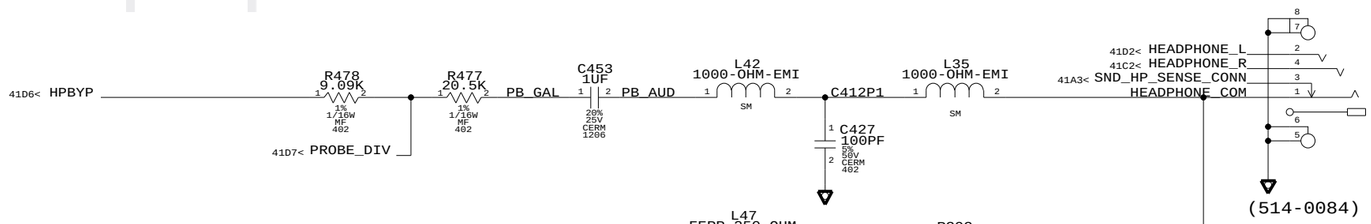


HEADPHONE DRIVER AND 2ND ORDER LPF

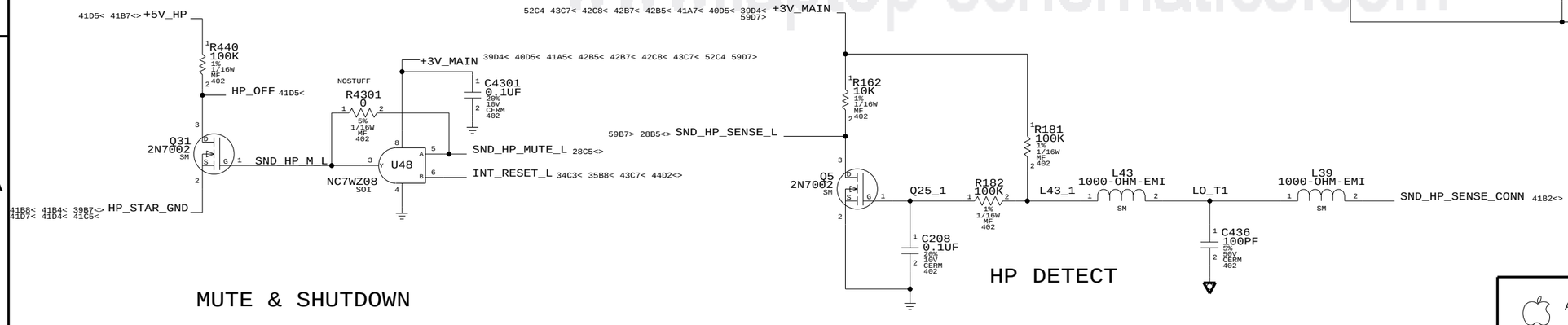


LOCATE CLOSE TO AMP

POWER SOURCE



GROUND NOISE CANCELLATION



MUTE & SHUTDOWN

HP DETECT

HEADPHONE OUT AMP

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SCALE: NONE	SHT 41 OF 69	

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TPA_5V IS NOT USED IN THIS SCHEMATIC

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
101S8000	4	0 OHM,5%,1/8W,RES-1206	L90,L91,L93,L96	

PREVIOUS PART NUMBER FOR L90,L91,L93,L96 IS 155S0148

C1061 AND C4261 SHARE PAD 1
C1062 AND C4262 SHARE PAD 1
C1065 AND C4265 SHARE PAD 1
C1067 AND C4267 SHARE PAD 1

SPEAKER AMP

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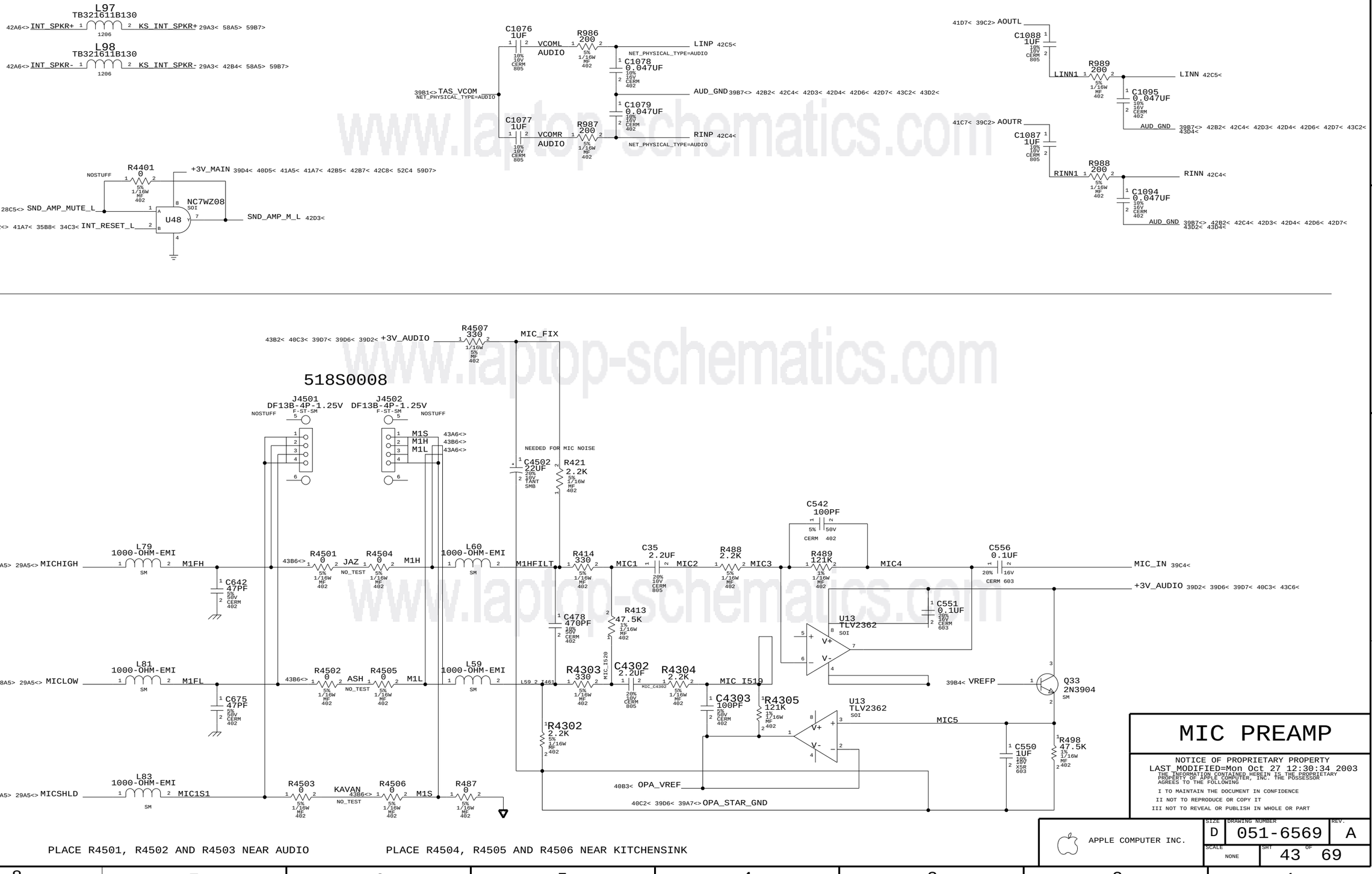
SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 42 OF 69	

DRAWING



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MIC PREAMP

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D	051-6569	A
SCALE: NONE	SHT 43 OF 69	

DRAWING

<XR_PAGE_TITLE>

PMU SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1008	1	PMU,M16C62,64KB,PRMGD	U26		
525-0057	1	CONN,BATTERY HOLDER	BT1		

AGP_RESET_L IS USED AS MAIN_RESET_L FOR SIL1162
THROUGH R1027 AND IS NOT USED IN ANY OTHER DEVICE

IIC BUS PULLUPS

PMU NOT RATED STRONG ENOUGH FOR 1K
MAIN RAIL, TO PREVENT LEAKAGE INTO UNPOWERED DEVICES

LOCATE NEAR TO PMU

PMU POWER MGR

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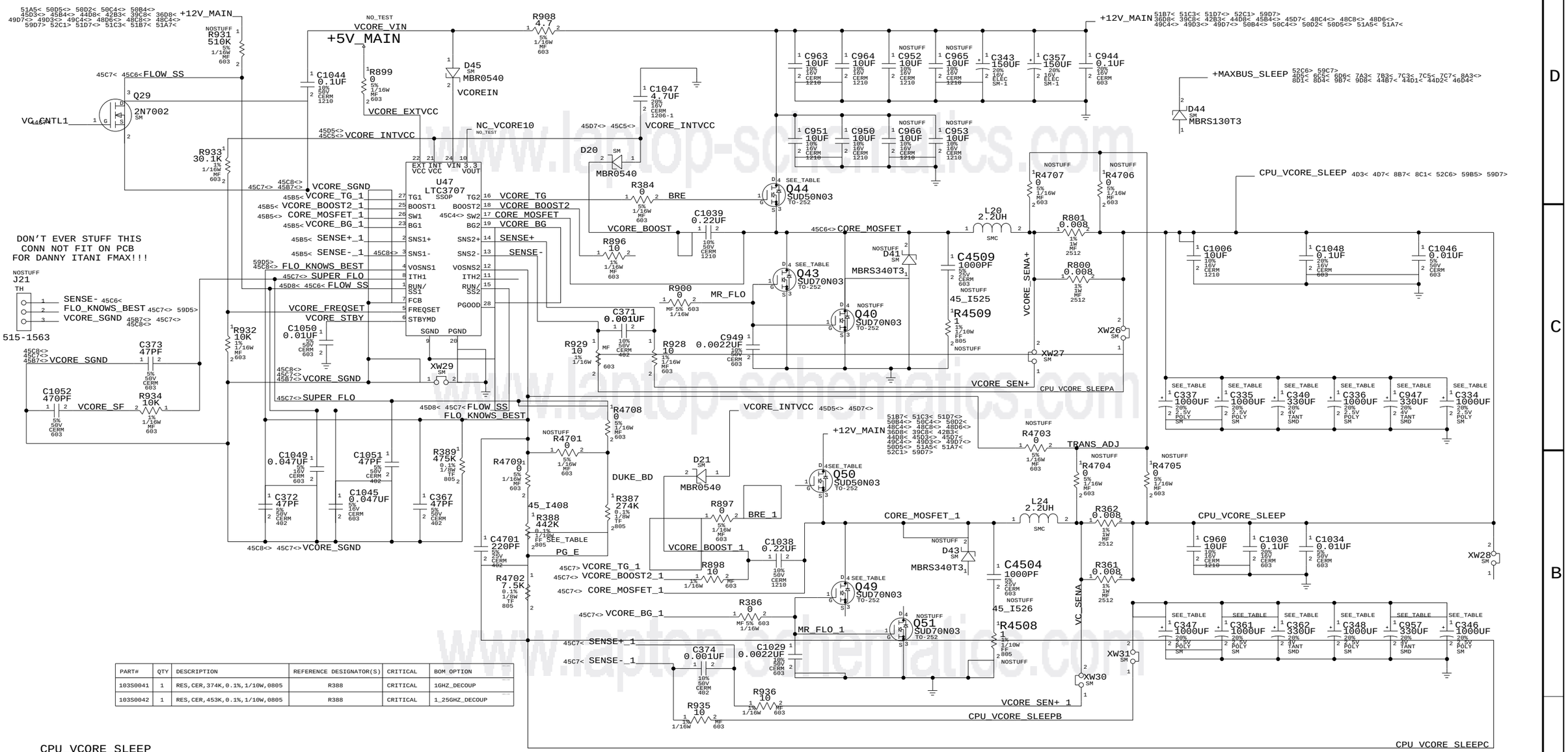

DON'T EVER STUFF THIS
CONNECTOR NOT FIT ON PCB
FOR DANNY ITANI FMAX!!!

CPU_VCORE_SLEEP
1.0GHZ,1.5V+30/-130MV,35W
1.25GHZ,1.57V+70/-70MV,35W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0041	1	RES,CER,374K,0.1%,1/10W,0805	R388	CRITICAL	1GHZ_DECOUP
103S0042	1	RES,CER,453K,0.1%,1/10W,0805	R388	CRITICAL	1_25GHZ_DECOUP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	2	MOSFET,N-CH,30V,63A,V30284,TO-252	Q44,Q50	
376S0207	2	MOSFET,N-CH,30V,70A,V30289,TO-252	Q43,Q49	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0012	4	CAP,TANT,POLY,330UF,4.0V,D4	C340,C947,C362,C957	1_25GHZ_DECOUP
128S0410	8	CAP,TANT,POLY,1000UF,2.5V,D4	C337,C335,C336,C334,C347,C361,C348,C346	1_25GHZ_DECOUP
128S0022	12	CAP,EL,POLY,220UF,20%,2V	C337,C335,C336,C334,C347,C361,C348,C346,C340,C947,C362,C957	1GHZ_DECOUP

CPU & AGP VREGS

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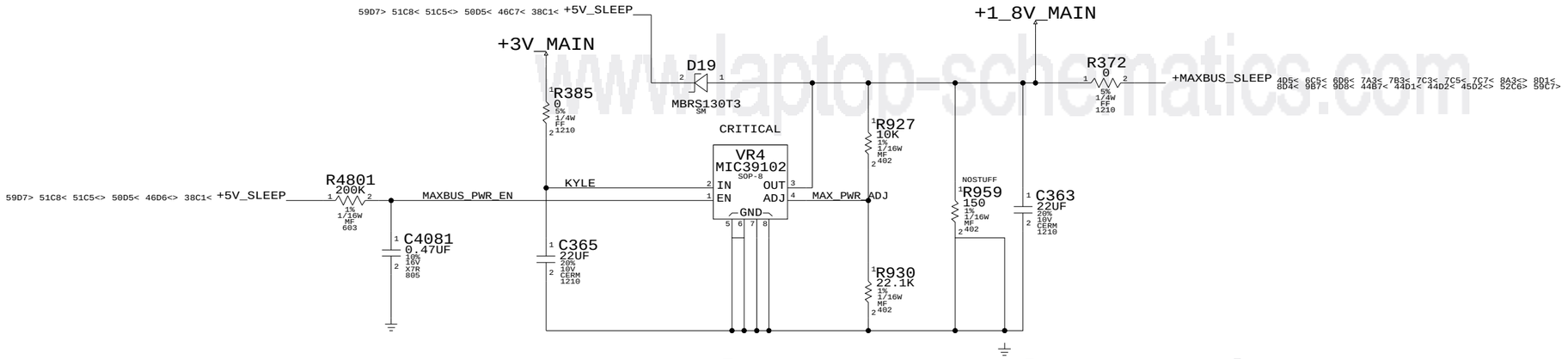
INTREPID MAXBUS & CPU OVDD POWER CONVERTER

(OFF DURING SLEEP)

+MAXBUS_SLEEP 1.8V,+/-2%,.606W

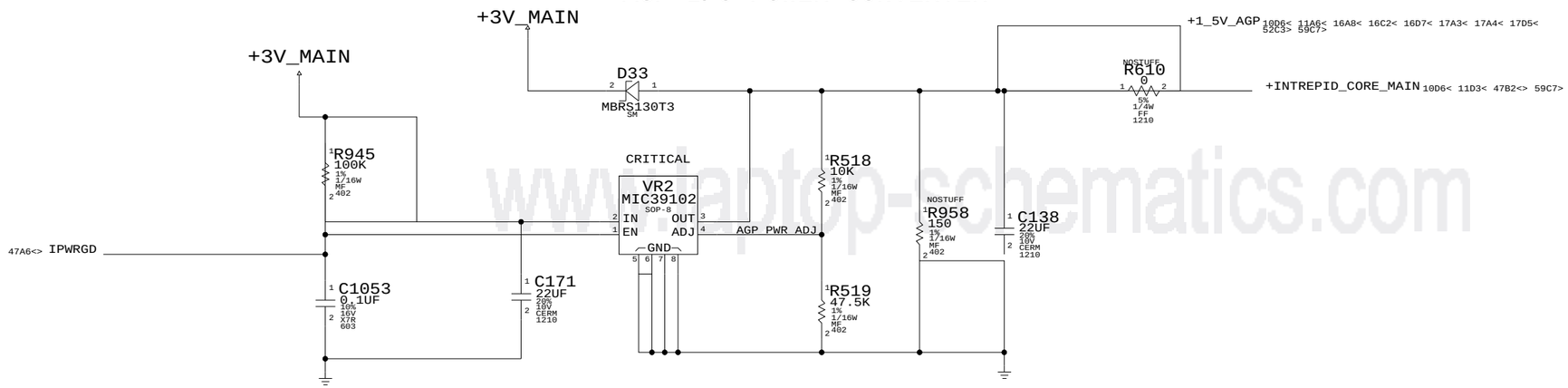


MAXBUS I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES,FF,47.5K-OHM,1%	R930		MAXIO_1'50V
114S3014	1	RES,FF,30.1K-OHM,1%	R930		MAXIO_1'65V
114S2674	1	RES,FF,26.7K-OHM,1%	R930		MAXIO_1'70V
114S2214	1	RES,FF,22.1K-OHM,1%	R930		MAXIO_1'80V *

+1_5V_AGP 1.5V,+/-5%,.6W

AGP I/O POWER CONVERTER



AGP I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES,FF,47.5K-OHM,1%	R519		AGPIO_1'50V *
114S3014	1	RES,FF,30.1K-OHM,1%	R519		AGPIO_1'65V
114S2674	1	RES,FF,26.7K-OHM,1%	R519		AGPIO_1'70V
114S2214	1	RES,FF,22.1K-OHM,1%	R519		AGPIO_1'80V

CPU & AGP VREGS

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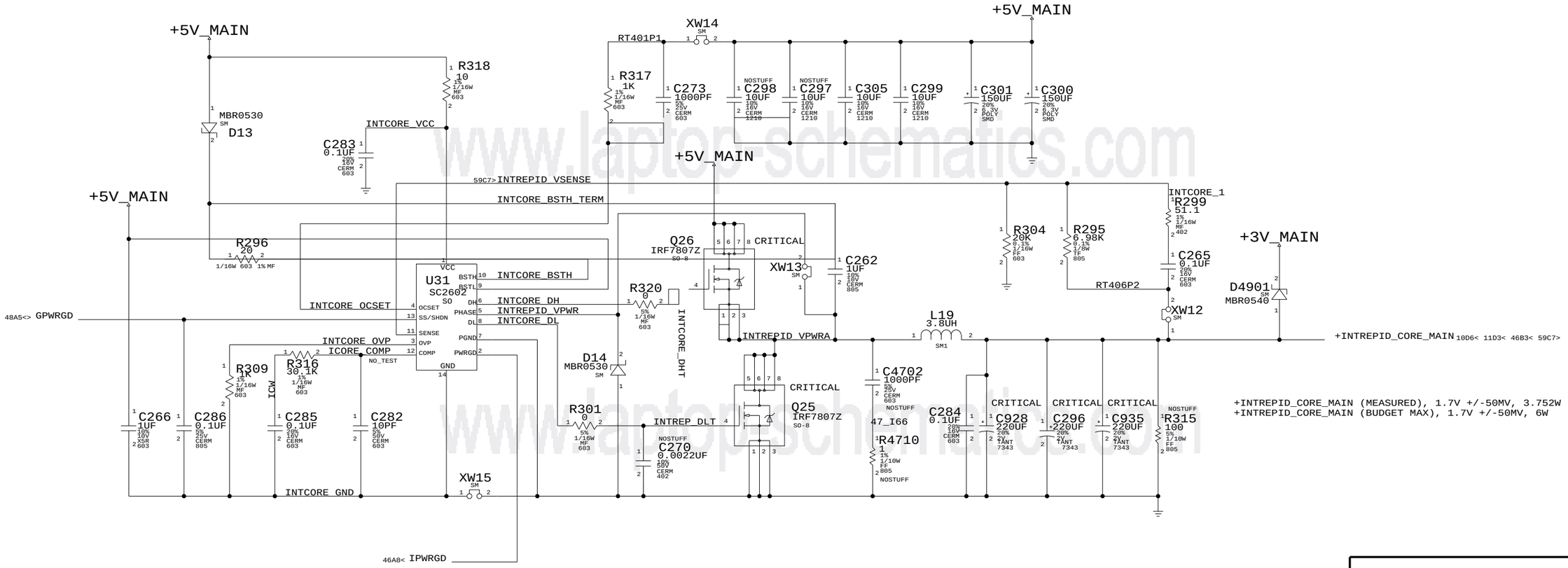

TABLES FOR INTREPID CORE RESISTOR VALUES TO VOLTAGES ARE LOCATED AT
KUMA SERVER(1):HARDWARE:KUMA DESIGNS;KUMA POWER SUPPLIES;ICORE R TOLERANCE

INTREPID CORE

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SIZE	DRAWING NUMBER	REV.
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SCALE: NONE | SHT 47 OF 69

DRAWING

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59D7> 52C1> 51D7<> 51C3< 51B7< 51A7<
51A5< 48C4<> 45D7< 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8<
50D5<> 50D2< 50C4<> 50B4<> 49D7<> 49D3<> 49C4<> 48C8<> +12V_MAIN

+12V_MAIN

XW7 SM

RB37P1

C220 150UF 20% 16V ELEC SM-1

C634 10UF 10% 16V CERM 1210

C633 10UF 10% 16V CERM 1210

C631 10UF 10% 16V CERM 1210

C632 10UF 10% 16V CERM 1210

C596 330PF 10% 16V CERM 603

R529 1.5K 1% 1/16W MF 603

R523 10 1% 1/16W MF 603

D30 MBR0530 SM

GCORE_VCC

C589 0.1UF 20% 16V CERM 603

R505 10 1% 1/16W MF 603

GCORE_BSTH_TERM

NO_TEST
48B6<> GCORE_VSENSE

GRAPH_CORE (NV18B), 1.6V +/-100MV, 12W
GRAPH_CORE (NV34), 1.45V +/-100MV, 16W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S5233	1	RES,5.23K OHMS,1%,1/16W,0603	R499	NV18B
110S2943	1	RES,2.94K OHMS,1%,1/16W,0603	R499	NV34

51D7<> 51C3< 51B7<
50D2< 50C4<> 50B4<>
48D8<> 48C8<> 45D7<
42B3< 39C8< 36D8< +12V_MAIN
45D3<> 45B4<> 44D8<
49D7<> 49D3<> 49C4<>
51A7< 51A9< 50D5<>
59D7> 52C1>

R150 0 5% 1/16W MF 603

QT2P1

Q9 SUD50N03 TO-252 (SEE_TABLE)

Q8 SUD50N03 TO-252 (NOSTUFF)

XW6 SM

D32 SM MBR0530

QT2P3

L12 2.2UH SMC

D31 SM MBRS340T3 (NOSTUFF)

C576 0.1UF 20% 16V CERM 603

R504 20K 1% 1/16W MF 603

R499 5.23K 1% 1/16W MF 603 (SEE_TABLE)

R4803 0 5% 1/16W MF 603

48_I10

R496 51.1 1% 1/16W MF 402

GCORE_1 NO_TEST

C564 0.1UF 20% 16V CERM 603

RB22P2

XW2 SM

GRAPH_CORE 17D4< 23C7<> 52A6>

+2_5V_MAIN

D34 SM MBRS130T3

C543 0.1UF 20% 16V CERM 603

C528 1000UF 20% 2.5V POLY SM (NOSTUFF)

C106 1000UF 20% 2.5V POLY SM (SEE_TABLE)

C558 1000UF 20% 2.5V POLY SM (NOSTUFF)

C132 1000UF 20% 2.5V POLY SM (SEE_TABLE)

C59 1000UF 20% 2.5V POLY SM (NOSTUFF)

C88 1000UF 20% 2.5V POLY SM (SEE_TABLE)

C71 1000UF 20% 2.5V POLY SM (NOSTUFF)

R475 100 5% 1/10W FF 805 (NOSTUFF)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1_25GHZ_DECOUP
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1GHZ_DECOUP

U40 SC2602 SO

VCC	1		
BSTH	10	NO_TEST	
BSTL	9	GCORE_BSTH	
DH	6	(+12V_MAIN)	
PHASE	5	GCORE_DH	
DL	8	GRAPHICS_VPWR	
PGND	7	GCORE_DL	
GND	14		
PWRGD	2		
OCSET	4	GCORE_OCSET	
SS/SHDN	13	MPWRGD	49B5<> 48B7<49B5<> 48B7< MPWRGD
SENSE	11	GCORE_VSENSE	48C4<>
OVP	3	GCORE_OVP	
COMP	12	GCORE_COMP	
		NO_TEST	

GPWRGD 47B8<

R527 1K 1% 1/16W MF 603

R503 3.92K 1% 1/16W MF 603 (SEE_TABLE)

RB27-1

C563 10PF 5% 50V CERM 603 (SEE_TABLE)

C572 0.1UF 20% 16V CERM 805

C552 0.1UF 20% 16V CERM 603 (SEE_TABLE)

C585 0.1UF 20% 16V CERM 603

GCORE_GND

XW39 SM

R515 0 5% 1/16W MF 603

Q7 SUD70N03 TO-252 (SEE_TABLE)

Q34 SUD70N03 TO-252 (NOSTUFF)

QT1P1

C4801 1000PF 5% 25V CERM 603

48_I99

R4802 1 1% 1/10W FF 805

C586 0.0022UF 10% 50V CERM 402 (NOSTUFF)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S3923	1	RES,3.92K,1%,1/16W,0603	R503	NV18B
110S2613	1	RES,2.61KK,1%,1/16W,0603	R503	NV34

132S1057	1	CAP,0.1UF,16V,20%,0603	C552	NV18B
132S0059	1	CAP,0.15UF,10V,10%,0603	C552	NV34

131S1013	1	CAP,10PF,50V,5%,0603	C563	NV18B
131S4715	1	CAP,47PF,50V,5%,0603	C563	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	1	MOSFET,N-CH,30V,63A,V30284,TO-252	Q9	
376S0207	1	MOSFET,N-CH,30V,70A,V30289,TO-252	Q7	

GRAPHICS CORE

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DRAWING

MAIN MEMORY DDR AND FRAME BUFFER POWER CONVERTER (2.50VDC)

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+12V_MAIN

25V_VCC

C1019 0.1UF 20% 16V CERM 603

R888 10 1% 1/16W MF 603

MBR0530 SM D18

XW25 SM RB227P1

R884 1K 1% 1/16W MF 603

C1005 470PF 10% 50V CERM 402

C959 10UF 10% 16V CERM 1210

C968 10UF 10% 16V CERM 1210

C975 10UF 10% 16V CERM 1210

C989 10UF 10% 16V CERM 1210

NOSTUFF C342 150UF 20% 16V ELEC SM-1

C351 150UF 20% 16V ELEC SM-1

25V_OCSET

25V_BSTH_TERM

25V_VSENSE NO_TEST

49B5<> 25V_VPWR

R369 20 1% 1/16W MF 603

25V_BSTH

U45 SC2602 SO 49C4

VCC BSTH BSTL DH PHASE DL PGND OCSET SS/SHDN SENSE OVP COMP PWRGD GND

25V_DH

25V_VPWR

25V_DL

R873 0 5% 1/16W MF 603

25V_DHT

Q28 SUD50N03 TO-252 SEE_TABLE

XW24 SM C358 0.1UF 20% 25V CERM 603

R880 20K 1% 1/16W MF 603

R871 22.1K 1% 1/16W MF 603

R872 51.1 1% 1/16W MF 402

25_CORE_1 NO_TEST

C962 0.1UF 20% 16V CERM 603

RB213P2

50A6> 49B7<50A6> 49B7< PGOOD

R883 4.75K 1% 1/16W MF 603

25V_OVP

25V_COMP

NO_TEST

25V_COMP_DWN

C1015 0.1UF 50V 25V CERM 805

C359 0.1UF 20% 16V CERM 603

R371 1K 1% 1/16W MF 603

C1004 0.1UF 20% 16V CERM 603

C1000 10PF 5% 50V CERM 603

25V_GND

D42 SM MBR0530

XW41 SM

MPWRGD 48B7<

R827 0 5% 1/16W MF 603

25V_DLT

Q27 SUD70N03 TO-252 SEE_TABLE

NOSTUFF C948 0.0022UF 10% 50V CERM 402

C4901 1000PF 5% 25V CERM 603

NOSTUFF R4901 1 1% 1/10W FF 805

NOSTUFF D15 SM MBRS340T3

L21 4.0UH SM1

+2_5V_MAIN

XW23 SM

D46 SM MBRS130T3 +3V_MAIN

C218 330UF 20% 6.3V POLY SMD

C330 330UF 20% 6.3V POLY SMD

NOSTUFF C323 330UF 20% 6.3V POLY SMD

C332 330UF 20% 6.3V POLY SMD

C329 0.1UF 20% 16V CERM 603

NOSTUFF C324 330UF 20% 6.3V POLY SMD

C235 330UF 20% 6.3V POLY SMD

C331 330UF 20% 6.3V POLY SMD

R334 100 5% 1/10W FF 805

+2_5V_MAIN, 1.61V +/-50MV, 12.908W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	1	MOSFET,N-CH,30V,63A,V30284,TO-252	Q28	
376S0207	1	MOSFET,N-CH,30V,70A,V30289,TO-252	Q27	

MEMORY PS

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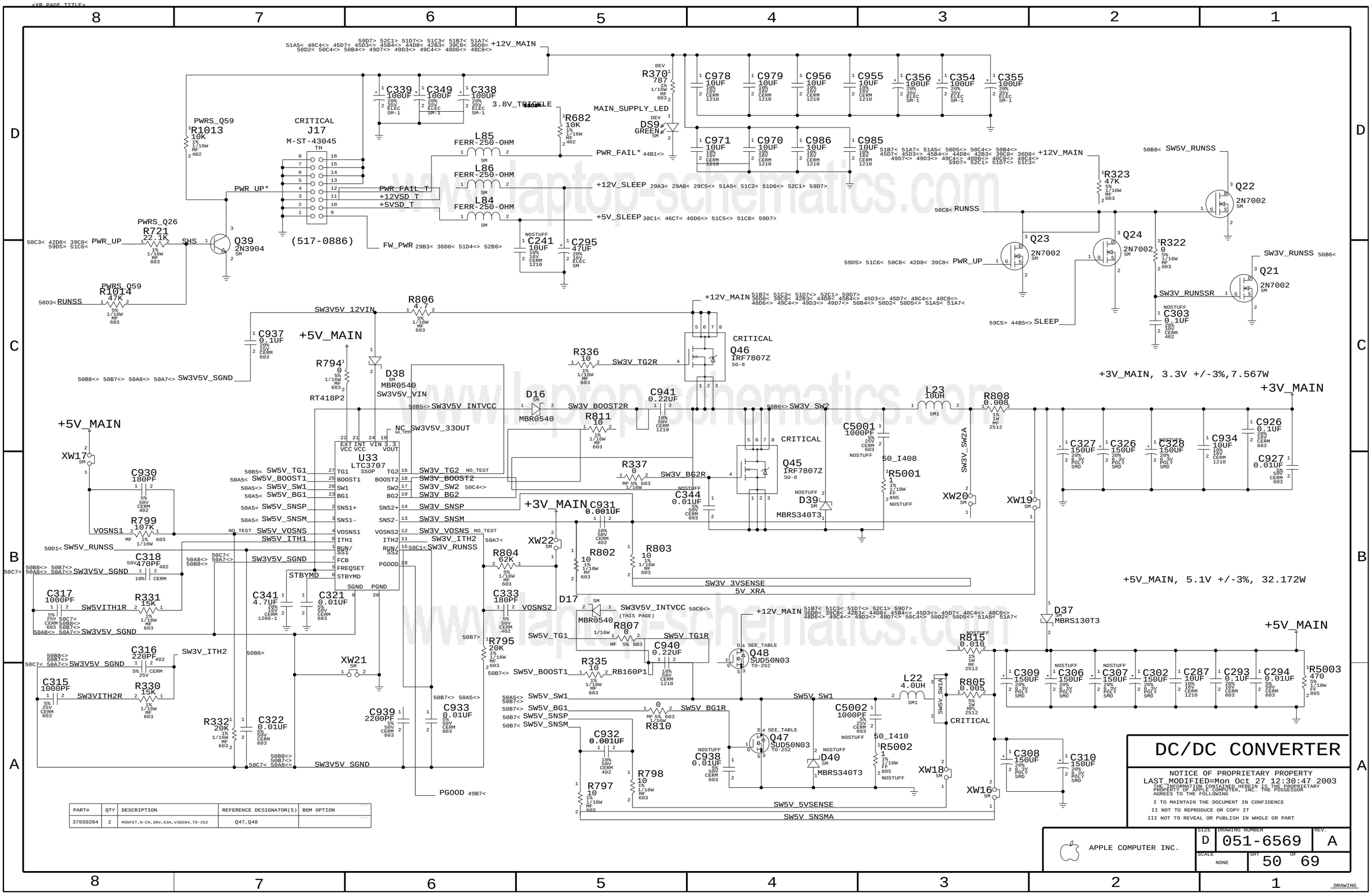

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	2	MOSFET,N-CH,30V,63A,V30284,TO-252	Q47,Q48	

DC/DC CONVERTER

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D	051-6569	A
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DRAWING

+12V MAIN POWER SWITCH
(OFF DURING SLEEP)

50B4<> 49D7<> 49D3<> 49C4<> 51B7< 45B4<> 44D8< 42B3< 39C8< 36D8< 48D6<> 48C8<> 48C4<> 45D7< 45D3<> 51A7< 51A5< 50D5<> 50D2< 50C4<> 59D7> 52C1> 51C3< +12V_MAIN

R769 470K 5% 1/16W MF 402

Q20 FDC602P SOT-6

+12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51A5< 51C2< 52C1> 59D7>

C269 47UF 20% 16V ELEC SM

C915 0.01UF CERM 10% 16V 402

C918 0.0022UF 10% 50V CERM 402

SW12V_SLEEP

R770 100K 1% 1/16W MF 402

SW12V_SL

51B6< SLEEP_OFF_L

Q14 2N7002 SM

R739 0 5% 1/16W MF 402

PWR_UP 39C8< 42D8< 50C3< 50C8< 59D5>

+5V POWER SWITCH
(OFF DURING SLEEP)

+5V_MAIN

Q37 FDC602P SOT-6

C742 0.01UF CERM 10% 16V 402

C773 0.0022UF 10% 50V CERM 402

+5V_SLEEP 38C1< 46C7< 46D6<> 50D5< 51C8< 59D7>

C238 150UF 20% 6.3V POLY SMD

SWITCH5V_4

R645 470K 5% 1/16W MF 402

R664 100K 1% 1/16W MF 402

SWITCH5V_3

R685 0 5% 1/16W MF 402

51C7<

SLEEP_OFF_L

Q38 2N7002 SM

46D6<> 46C7< 38C1< +5V_SLEEP 59D7> 51C5<> 50D5<

R300 330 5% 1/16W MF 402

RUNLED1

DS5 GREEN SM DEV

+5V POWER LED

FIREWIRE POWER SWITCH
EVALUATE CIRCUIT FOR SURGE PROTECTION FOR Q59C

FW_12V U35 SI4435DY SOI

52B6> 50C6<> 36D6< 29B3< FW_PWR

C19 47UF 20% 25V ELEC SM

FW_12V

C18 0.01UF CERM 5% 50V 603

Q42P4

C473 0.0022UF 10% 50V CERM 402

FW_PWR_SW 36D6< 52B6>

+5V_MAIN

R23 470K 5% 1/16W MF 603

R21 100K 5% 1/16W MF 603

Q1P3

R22 10K 1% 1/16W MF 603

Q1P1

Q1 2N7002 SM

TMDS POWER CONVERTER & SWITCH
(OFF DURING SLEEP)

VOLTAGE TO SUPPORT 3.3V AT PANEL
VOLTAGE HERE WILL EXCEED 3.3V

+3.3VFPD (3_6V_SLEEP), 3.6V +/-50MV, 3.32W

59D7> 52C1> 51D7<> 51B7< 51A7< 51A5< 48C8<> 48C4<> 45D7< 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8< 50D5<> 50D2< 50C4<> 50B4<> 49D7<> 49D3<> 49C4<> 48D6<> +12V_MAIN

FPD_12VM R1017 0 5% 1/8W FF 1206

+12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51A5< 51D6<> 52C1> 59D7>

FPD_12VS R1018 0 5% 1/8W FF 1206

FPD_3V3&FPD_12VM Q11 FDC602P SOT-6

+3.3VFPD 24D7< 52B6>

R5301 0 5% 1/16W MF 402 NOSTUFF

3_6V_SLEEP 37D1<

C254 10UF 10% 16V CERM 1210

+5V_MAIN

3_5 HONKER

+5V_MAIN

FPD_3V3

SENSE VR3 EZ1582 SM

VPWR VOUT VCTRL VOUT ADJ TAB

52C4 51B4<> 59D7>

59D7> 52C4 51B4<>

HONK_ADJ

R251 102 1% 1/16W MF 402

C246 150UF 20% 6.3V POLY SMD

FPD_3V3&FPD_12VM C257 0.01UF 402 10% 16V CERM

C252 0.0022UF 10% 50V CERM 402

SWITCH5V_6

R278 100K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

R277 10K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

R279 10K 1% 1/16W MF 402

TMDS_EN 23D7<>

C654 10UF 10% 16V CERM 1210

C653 10UF 10% 16V CERM 1210

C236 0.022UF 10% 50V CERM 805

R601 182 1% 1/16W MF 402

SWITCH5V_5

R1012 100K 1% 1/16W MF 402 SEE_TABLE

NOSTUFF C258 0.01UF 20% 16V CERM 402

FPD_12VS&FPD_12VM DZ1 1N5227B SOT23

CHOC_BROWNIE

FPD_3V3&FPD_12VM R283 0 5% 1/16W MF 402

FPD_PWR_ON 23D7<>

FPD_PWR_ON_T

Q13 2N7002 SM FPD_3V3&FPD_12VM

R284 100K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

+5V POWER, SLEEP & TESTPOINT LEDS
(TESTPOINT LED IS USED TO FOR SERVICE AND
IF NOT ILLUMINATED, TELLS USER ITS OK TO ADD MEMORY)

51C3< 51A7< 51A5< 50D5<> 49D3<> 49C4<> 48D6<> 45B4<> 44D8< 42B3< 39C8< 36D8< 48C8<> 48C4<> 45D7< 45D3<> 50D2< 50C4<> 50B4<> 49D7<> 52C1> 51D7<> +12V_MAIN

R738 4.7K 5% 1/16W MF 402

NOSTUFF R5101 0 5% 1/16W MF 402

CPU_SLEEPIN

LED_RET 29A3< 52B3>

Q17 2N7002 SM

59D5> 44C7<> POWER_UP*

Q16 2N7002 SM

Q15 2N7002 SM

R741 47.5K 1% 1/8W 402

50C4<> 50B4<> 49D7<> 49D3<> 52C1> 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8< 49C4<> 48D6<> 48C8<> 48C4<> 45D7< 51D7<> 51C3< 51B7< 51A5< 50D5<> 50D2< 59D7> +12V_MAIN

R740 10K 1% 1/16W MF 402

SLEEP2

CPU_STATE_LED* 44C4<>

R751 0 5% 1/16W MF 402

SLEEP1

Q18 2N7002 SM

+3V_MAIN

R302 330 5% 1/16W MF 402 DEV

SLEEPLED_TERM

DS6 GREEN SM DEV

SLEEP_LED_BD

Q19 2N7002 SM

SLEEP LED

44D6<> BT1

+5V_MAIN

+12V_MAIN

51B7< 51C3< 51D7<> 52C1> 59D7> 36D8< 39C8< 42B3< 44D8< 45B4<> 45D3<> 45D7< 48C4<> 48C8<> 50B4<> 50C4<> 50D2< 50D5<> 51A7< +12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51C2< 51D6<> 52C1> 59D7>

NOSTUFF R615 0 5% 1/16W MF 402

NOSTUFF R607 0 5% 1/16W MF 402

NOSTUFF R609 0 5% 1/16W MF 402

NOSTUFF R608 0 5% 1/16W MF 402

TESTPOINT

RT373P1

R612 787 1% 1/16W MF 603

PWR_LED

BT1_LED

NOSTUFF R614 470 5% 1/16W MF 402

DS10 RED SM

JAZ1 A TH-TP50

GENERAL POWER LED
(NOT ILLUMINATED = OK TO ADD MEMORY)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1005	1	RES,100K OHM,1%,1/16W,0402,SMD	R1012	FPD_12VM
116S1000	1	RES,0 OHM,5%,1/16W,0402,SMD	R1012	FPD_3V3

+5V/+12V, AUDIO FW & TMDS PWR

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 51 OF 69	

DRAWING

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CPU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+MAXBUS_SLEEP	10	1.8	20
CPU_AVDD	10	1.85	20
CPU_VCORE_SLEEP	10	1.85	20

4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7<
4D1< 44D2< 45D2<> 46D4< 59C7>
4D3<
4D3< 4D7< 8B7< 8C1< 45D2<> 59B5> 59D7>

ETHERNET POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
ENET_AVDD	10	2.5	20

35D2<> 35D4<>

FIREWIRE POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
FW_DIO_V	10	3.3	20
FW_DIODE_BYPASS_V	10	3.3	20
FW_PWR	10	24	20
FW_PWR_SW	10	24	20
FW_PHY_3_3	10	3.3	20
FW_VGND	10	0	20
FW_VP	10	12	20
FW_VP1	10	12	20
FW_VP2	10	12	20
FW_VP_1	10	12	20
FW_VP_2	10	12	20

36B6<
36B6<> 36B7<>
29B3< 36D6< 50C6<> 51D4<>
36D6< 51D2<>
36B5< 36B7< 36D7<

36D5<
36D1<> 36D3<>
36C1<> 36D3<>
36D4<
36D4<

GRAPHICS POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3.3VFPD	10	3.6	20
DAC2VDD	10	3.3	20
DACVDD	10	3.3	20
DDC_VCC_3	10	3.3	20
DDC_VCC_5	10	5	20
DDR_VREF	10	1.25	20
IFP0AVCC	10	3.8	20
IFP0VREF	10	3.8	20
INT_TMDS_3V	10	3.6	20
GPU_AGP_VREF	10	0.75	20
GPU_FB_VREF	10	1.25	20
GRAPH_CORE	10	1.6	20
NVPLLVDD	10	3.3	20
SGRAVREF	10	1.25	20
SGRBVREF	10	1.25	20

24D7< 51C1<>
22C5<
22C4<
24B3<> 59B7>
25C4< 59B7>
12A7< 14D2<> 14D8<> 15D8<
23A6< 23C1<
23B4<>
24C3<> 59C7>
17A2< 17A8<
18C8<
17D4< 23C7<> 48C2<>
22D5<
20A3< 20C4< 20C8<
21A3< 21C4< 21C8<

17B5<>	GPU_50PULLUP	1.5	OUT
17A5<>	GPU_50PULLDWN	0	OUT
17A5<	GPU_TMODE	0	OUT
22B2< 22A5<	GPU_XTALSSIN	0	OUT
22D4<	VIPCLK	0	OUT
37B7<	CSLOT_IOWAIT_L	3.3	OUT
38C6<>	EIDE_CSELP_L	0	OUT
38C6<>	EIDE_IOCS16_L	5	OUT
38C2<>	UIDE_CSELP_L	0	OUT
38C2<>	UNUSED_ATAIOCS16_L	5	OUT

INTREPID POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_5V_INTREPID_PLL	10	1.5	20
+1_5V_INTREPID_PLL1	10	1.5	20
+1_5V_INTREPID_PLL2	10	1.5	20
+1_5V_INTREPID_PLL3	10	1.5	20
+1_5V_INTREPID_PLL4	10	1.5	20
+1_5V_INTREPID_PLL5	10	1.5	20
+1_5V_INTREPID_PLL6	10	1.5	20
+1_5V_INTREPID_PLL7	10	1.5	20
+1_5V_INTREPID_PLL8	10	1.5	20
+1_5V_AGP	10	1.5	20
INT_AGP_VREF	10	0.75	20

9D4< 16D6< 28D6<> 30D5<
28C4<
28D4<
28D4<
28D4<
16D5<
30D4<
9D2<
28D4<
10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17A4< 17D5< 46B4<> 59C7>
16A7< 16C6<>

MAIN POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_8V_MAIN	10	1.8	20
+2_5V_MAIN	10	2.5	20
+3V_MAIN	10	3.3	20
3.8V_TRICKLE	10	3.8	20
+5V_MAIN	10	5	20
+12V_MAIN	10	12	20
+12V_SLEEP	10	12	20
GND	10	0	20
AGND	10	0	20
ANALOGGND	10	0	20
ALTCHGND	10	0	20
CHGND	10	0	20

59D7>
59D7> 49B2<> 30B3<
43C7< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 39D4<
59D7>
59D7> 51B4<>

39B7<>
41B3< 41B1<> 41A4< 41A2<> 40C6< 40B6< 40B5<> 35C1<> 35B1<
43A5< 42A6<> 42A5<> 41D3< 41C3<
36B6<> 36B2< 36A7<> 33D4< 33C4< 33C2< 33B4< 25C3< 25B3<>
36C1< 36C1<> 36B6<
43B7< 43A7< 29A3< 24B3<

+1_8V_MAIN
+2_5V_MAIN
+3V_MAIN
3.8V_TRICKLE
+5V_MAIN
+12V_MAIN
+12V_SLEEP

ALT CHASSIS

PMU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
3.8VH_TRICKLE	10	3.8	20
PMU_AVCC	10	3.5	20
PMU_POWER	10	3.5	20

44C1< 44D7<>
44B5< 44D4<> 59C5>
29C3<> 44A5<> 44B1< 44C2< 44D5<>

SYSTEM POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+12VSD_FILT	10	12	20
FAN_12V_FILT	10	12	20
KS5VSD	10	5	20
LED_5V	10	5	20
LED_5V_FILT	10	5	20
LED_RET	10	0	20
LED_RET_FILT	10	0	20

29A5<>
29A5<> 59C7>
29A5<> 59A7>
29A8<
29A5<> 59A7>
29A3< 51B6<
29A5<> 59A7>

USB POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3V_INTREPID_USB	10	3.3	20
NEC_AVDD	10	3.3	20
USB_GND	10	0	20
USB_PORT_PWR	10	5	20
USB_PWR	10	5	20

28C4<
32D5<
33A4<> 33B3<> 33C3<>
32D3<> 59B3>
25B5<> 25C2< 25D3<> 33A6<>

POWER CONSTRAINTS

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SIZE D | DRAWING NUMBER 051-6569 | REV. A
SCALE NONE | SHT 52 OF 69

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SIG_NAME	RATSNEST_SCHEDULE RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	MIN_NECK_WIDTH NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	NO_TEST	FUNC_TEST	PULSE_PARAM
13C4<> 13B6<> 13B3<> 13A6<> 12D8<> 12C8<> 12B8< MEM_DATA<0..63>	MEM_GROUP0:G:L:S:0:150	8	L:S::1300		3				167 MHZ
13C8<> 14D6<> 14D4<> 14C6<> 13D4<> 13C7<> 13C4<> 13C2<> 13B5<> 13B2<> RAM_DATA_A<0..63>	RAM_GROUP0_A:G:L:S:0:180	8	L:S::1800		3				167 MHZ
14C4<> 14B6<> 14B4<> 14A6<> 14A4<> 13D7<> 13B2<> 13A5<> 15D6< 13A2<> 15A6< 15B4< 15B6< 15C4< 15C6< 15D4< RAM_DATA_B<0..63>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
13C8<> 13C4<> 13B3<> 13A6<> 12C6<> MEM_DQS<0..7>	MEM_GROUP0:G:L:S:0:180	3	L:S::1300		3				167 MHZ
14A6<> 13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> RAM_DQS_A<0..7>	RAM_GROUP0_A:G:L:S:0:180	3	L:S::1700		3				167 MHZ
14D6<> 14C6<> 14C4<> 14B2<> 14B5<> 14A2<> 13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A5<> RAM_DQS_B<0..7>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
15D6< 15C8<> 15C6<> 15B8<> 15B6<> 15A6<> 15A2<> 14C8<> 13A4<> 13B6<> 12C6<> MEM_DQM<0..7>	MEM_GROUP0:G:L:S:0:180	3	L:S::1300		3				167 MHZ
13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> 13A5<> RAM_DQM_A<0..7>	RAM_GROUP0_A:G:L:S:0:180	3	L:S::1800		3				167 MHZ
13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A5<> 15D4> 15C4> 15B4> 15A4> RAM_DQM_B<0..7>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
12D6<> 12D3< 12D2< 12C3< 12C2< 12B3< MEM_ADDR<0..12>	MEM_ADDR:G:L:S:0:200	3	L:S::600						
15B4> 14B6<> 14B4<> 12D3< 12D1< 12C3< 12C1< 12B3< RAM_ADDR<0..12>	RAM_ADDR:G:L:S:0:1300	4	L:S::3500	200					
15C6< 15C4> 15B6< 12D6<> 12B3< MEM_BA<0..1>	MEM_ADDR:G:L:S:0:1300	3	L:S::600						
15B6< 14B6<> 14B4<> 12B3< RAM_BA<0..1>	RAM_ADDR:G:L:S:0:1300	4	L:S::4000	200					
12C6<> 12C2< 12B2< MEM_CS_L<0..3>	MEM_ADDR:G:L:S:0:200	3	L:S::600		10 MIL SPACING				
14B6<> 14B4<> 12C1< RAM_CS_L<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3	L:S:2000:3500		10 MIL SPACING				
15B4> 12B1< RAM_CS_L<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2	L:S:2000:3500		10 MIL SPACING				
12C6<> 12A3< MEM_RAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3	L:S::600 MIL						
12C6<> 12A3< MEM_CAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3	L:S::600 MIL						
12C6<> 12B3< MEM_WE_L	MEM_ADDR:G:L:S:0 MIL:280 MIL	3	L:S::600 MIL						
15B6< 14B4<> 12A2< RAM_CAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
15B4> 14B4<> 12A2< RAM_RAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
15B6< 14B6<> 12B3< RAM_WE_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
12C6<> 12C2< 12B6<> 12B2< MEM_CKE<0..3>	MEM_ADDR:G:L:S:0:200	3	L:S::600		10 MIL SPACING				
15C1< 14B6<> 14B4<> 12C1< 12B1< RAM_CKE<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3	L:S::2500		10 MIL SPACING				
15C6< 15C4> 15B1< 15A1< 12C1< 12B1< RAM_CKE<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2	L:S::2500		10 MIL SPACING				
12B6<> MEM_MUXSEL_H<0..1>		3	L:S::1000						
12B6<> MEM_MUXSEL_L<0..1>		3	L:S::1000						167 MHZ
13C4<> 13A3<> 12D4< MUX_SEL_H		4	L:S::2000 MIL	200					167 MHZ
13C8<> 13A6<> 12D4< MUX_SEL_L		4	L:S::2000 MIL	200					167 MHZ
12B6<> SYSCLK_DDRCLK_A0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A0_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
14D6<> 12C4< SYSCLK_DDRCLK_A0	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
14D6<> 12C4< SYSCLK_DDRCLK_A0_L	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
14A4<> 12C4< SYSCLK_DDRCLK_A1	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
14A4<> 12B4< SYSCLK_DDRCLK_A1_L	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A2_L		3	L:S::750 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
15B4> 12B4< SYSCLK_DDRCLK_B0	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
12B4< 15B3> SYSCLK_DDRCLK_B0_L	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
15D6< 12A4< SYSCLK_DDRCLK_B1	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
15C6< 12A4< SYSCLK_DDRCLK_B1_L	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3	L:S::3200 MIL	200	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_L_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
15A6< 12A4< SYSCLK_DDRCLK_B2	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
15A6< 12A4< SYSCLK_DDRCLK_B2_L	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
28A6< INT_REF_CLK_IN_PD		8	L:S::2500 MIL		10 MIL SPACING	270			66.56 MHZ
31C6< 31B7< 31B6< 30D4<> 30C4<> 30C2< 30C1<> 30B2< PCI_AD<31..0>	MIN_DAISY_CHAIN	6	L:S:6000:8000	500					33 MHZ
59C3> 59B3> 32C6<> 32B7<> 32B6<> 31C7<> 59A5> 32B6<> 31B7< 30C5<> PCI_CBE<3..0>	MIN_DAISY_CHAIN	6	L:S:6000:8000	500					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_FRAME_L	MIN_DAISY_CHAIN	L7	S:6000 MIL:8000 MIL	500					33 MHZ

DIGITAL SIGNAL CONSTRAINTS

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SIGNAL CONSTRAINTS

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 53 OF 69	

DRAWING

SIG_NAME	RATSNEST_SCHEDULE RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	DIFFERENTIAL_PAIR MAX_EXPOSED_LENGTH	DIFFERENTIAL_PAIR FUNC_TEST	PULSE_PARAM
32B6<> 31B7< 30C5<> 30B7< PCI_IRDY_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	100				33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_TRDY_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	100				33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_DEVSEL_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	100				33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_STOP_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	100				33 MHZ
59A5> 32B6<> 31B7< 30C5<> PCI_PAR	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	100				33 MHZ
30D5<> CLK33M_PCI_SLOTB_UF		8	S:600 MIL:1000 MIL	200		450		33 MHZ
30D5<> CLK33M_PCI_SLOTC_UF		8	S:600 MIL:1200 MIL	200		450		33 MHZ
30D5<> CLK33M_PCI_SLOTD_UF		8	S:600 MIL:1000 MIL	200		450		33 MHZ
59A5> 31C2<> 30D7< CLK33M_PCI_SLOTB		5	S:3000 MIL:4000 MIL	200	10 MIL SPACING	450		33 MHZ
30C5<> INT_PCI_FB_OUT		4	L:S::1000 MIL	200		450		33 MHZ
30D8< PCI_FBO_PLUS2		4	L:S::200 MIL	200		450		33 MHZ
30C8< PCI_FB_PLUS4		4	S:1900 MIL:2000 MIL			450		33 MHZ
30C8< PCI_FBI_PLUS2		4	S:1900 MIL:2000 MIL	200		450		33 MHZ
30C7< PCI_FBI_EQUAL		4	S:2600 MIL:3000 MIL	200		450		33 MHZ
30C7< PCI_FB_PLUS6		4	S:5900 MIL:6000 MIL			450		33 MHZ
30C5< INT_PCI_FB_IN		4	L:S::1080 MIL	200		450		33 MHZ
31C6< 31C3<> 31C2<> 31B7< 31B6< 31B3<> 31B2<> PCIT_AD<31..0>		3	L:S::1000					33 MHZ
59C3> 59B3> 31C7< 59A5> 31C3<> 31B6< 31B2<> PCIT_CBE<31..0>		3	L:S::1000					33 MHZ
31C2<> 31B6< PCIT_FRAME_L		3	L:S::1000 MIL					33 MHZ
59B5> 31C3<> 31B6< PCIT_IRDY_L		3	L:S::1000 MIL					33 MHZ
31C2<> 31B6< PCIT_TRDY_L		3	L:S::1000 MIL					33 MHZ
31C2<> 31B6< PCIT_DEVSEL_L		3	L:S::1000 MIL					33 MHZ
31C2<> 31B6< PCIT_STOP_L		3	L:S::1000 MIL					33 MHZ
31C2<> 31B6< PCIT_PAR		3	L:S::1000 MIL					33 MHZ
17D8< 17C8< 16C4<> AGP_AD<0..15>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500					266 MHZ
17C8< 16B4<> AGP_CBE<0..1>	AGP_GROUP0:G:L:S:0:330	5	L:S::4500					266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<0>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP0	133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<0>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP0	133 MHZ
17C8< 16C4<> 16B4<> AGP_AD<16..31>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500					266 MHZ
17C8< 16B4<> AGP_CBE<2..3>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500					266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<1>	AGP_GROUP0:G:L:S:0 MIL:280 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP1	133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<1>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP1	133 MHZ
17B8< 16C3< 16B4<> AGP_FRAME_L		5	S:4000 MIL:4500 MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_IRDY_L		5	S:4000 MIL:4500 MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_TRDY_L		5	S:4000 MIL:4500 MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_DEVSEL_L		5	S:4000 MIL:4500 MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_STOP_L		5	S:4000 MIL:4500 MIL					66 MHZ
17B8< 16B4<> AGP_PAR		5	S:4000 MIL:4500 MIL					66 MHZ
17A8< 16C1< 16B4< 16B4<> 16B1< 16A4<> AGP_SBA<0..7>		5	L:S:4000:4500					
17B8< 16B3< 16A4<> AGP_SB_STB	AGP_GROUP99:G:L:S:0 MIL:200 MIL	3	L:S::4500 MIL				AGP_SBSTBB	
17A8< 16D1< 16A4<> AGP_SB_STB_L	AGP_GROUP99:G:L:S:0 MIL:200 MIL	3	L:S::4500 MIL				AGP_SBSTBB	
17B6< 16B1< 16A4<> AGP_ST<0..2>		5	L:S:4500:5000					
17B8< 16B3< 16A4<> AGP_PIPE_L		5	S:4000 MIL:4500 MIL					
17B8< 16B3< 16A4<> AGP_RBF_L		5	S:4000 MIL:4500 MIL					
17B6<> 16C4<> 16C3< AGP_REQ_L		5	S:4500 MIL:5000 MIL					
17B6< 16C4<> 16C3< AGP_GNT_L		5	S:4500 MIL:5000 MIL					
17B8< 16B1< 16A6<> AGP_WBF_L		5	S:4000 MIL:4500 MIL					
17A8> 16D3< 16D1< 16C6<> AGP_BUSY_L		5	S:4500 MIL:5000 MIL					
17A8< 16D3< 16C6<> STOP_AGP_L		5	S:4500 MIL:5000 MIL					
17D7<> 17D6<> 17C6<> GPU_AGP_AD<0..15>	GPU_AGP_GROUP0:G:L:S:0:100	3	L:S::600					266 MHZ
17C6<> GPU_AGP_CBE<0..1>	GPU_AGP_GROUP0:G:L:S:0:100	3	L:S::600					266 MHZ
AGP_AD_STB_GPU_UF<0>	GPU_AGP_STB0:G:L:S:0 MIL:50 MIL	3	L:S::450 MIL		8 MIL SPACING	500	GPU_ADSTBDP0	133 MHZ
AGP_AD_STB_L_GPU_UF<0>	GPU_AGP_STB0:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP0	133 MHZ
17C6<> GPU_AGP_AD<16..31>	GPU_AGP_GROUP1:G:L:S:0:100	3	L:S::600					266 MHZ
17C6<> GPU_AGP_CBE<2..3>	GPU_AGP_GROUP1:G:L:S:0:100	3	L:S::600					266 MHZ
AGP_AD_STB_GPU_UF<1>	GPU_AGP_STB1:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP1	133 MHZ
AGP_AD_STB_L_GPU_UF<1>	GPU_AGP_STB1:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP1	133 MHZ
17B6<> GPU_AGP_FRAME_L		3	S:300 MIL:600 MIL					66 MHZ
17B6<> GPU_AGP_IRDY_L		3	S:300 MIL:600 MIL					66 MHZ
17B6<> GPU_AGP_TRDY_L		3	S:300 MIL:600 MIL					66 MHZ
17B6<> GPU_AGP_DEVSEL_L		3	S:300 MIL:600 MIL					66 MHZ
17B6<> GPU_AGP_STOP_L		3	S:300 MIL:600 MIL					66 MHZ
17B6<> GPU_AGP_PAR		3	S:300 MIL:600 MIL					66 MHZ
17A6<> GPU_AGP_SBA<0..7>		3	L:S:300:600					
17B6<> GPU_AGP_SB_STB	GPU_AGP_SBSTB:G:L:S:0 MIL:50 MIL	3	S:300 MIL:600 MIL				GPU_SBSTBB	
17A6<> GPU_AGP_SB_STB_L	GPU_AGP_SBSTB:G:L:S:0 MIL:50 MIL	3	S:300 MIL:600 MIL				GPU_SBSTBB	
17B6<> GPU_AGP_PIPE_L		3	S:300 MIL:600 MIL					
17B6<> GPU_AGP_RBF_L		3	S:300 MIL:600 MIL					
16C6<> CLK66M_GPU_UF		3	S:1000 MIL:1100 MIL		10 MIL SPACING	250		66 MHZ
17C6< 16D8< CLK66M_GPU_AGP		4	S:3700 MIL:3900 MIL	200	10 MIL SPACING	250		66 MHZ
16C6<> INT_AGP_FB_OUT		4	S:1400 MIL:1500 MIL	200		250		66 MHZ
16B7< AGP_FBO_EQUAL		4	S:900 MIL:1080 MIL	200		250		66 MHZ
16B8< AGP_FB_PLUS2		4	S:1900 MIL:2000 MIL			250		66 MHZ
16C7< AGP_FBI_EQUAL		4	L:S::200 MIL	200		250		66 MHZ
16C6< INT_AGP_FB_IN		4	L:S::1200 MIL	200		250		66 MHZ
30C5<> 30A7< 16D7< INT_ROM_OVERLAY_PU		3	S:600 MIL:800 MIL		10 MIL SPACING	250		66 MHZ
59A7> 56B3> 16C7> 9B4< 8A2< INT_ANALYZER_CLK		3	L:S::2800 MIL		8 MIL SPACING	250		166 MHZ
32A6< 30D7< CLK33M_PCI_SLOTD		4	S:3000 MIL:3500 MIL	200	8 MIL SPACING	250		33 MHZ

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DIGITAL SIGNALS

RATSNEST_SCHEDULE

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX EXPOSED LENGTH	PULSE PARAM	
	FBD<0..63>	GPU_FBDATA_A:G:L:S:0:225	2	L:S::800				300 MHZ	18E8<> 18F8<> 18G8<> 19C5< 19C8< 19D5< 19D8<
	RFBD<0..63>	RAM_FBDATA_A:G:L:S:0:300	2	L:S::1000				300 MHZ	19C4< 19C7< 19D4< 19D7< 20B1<> 20B5<> 20C1<> 20C5<>
	FBDQM<0..7>	GPU_FBDQM_A:G:L:S:0:200	2	L:S::800				300 MHZ	18D8> 18G3<
	RFBDQM<0..7>	RAM_FBDQM_A:G:L:S:0:200	2	L:S::1000				300 MHZ	18G2< 20C2< 20C6<
	FBA<0..12>	GPU_FBADDR_A:G:L:S:0:200	2	L:S::700				300 MHZ	18C8> 18D8> 18E3< 18F3<
	RFBA<0..11>	RAM_FBADDR_A:G:L:S:0:330	2	L:S::2400	2350			300 MHZ	18E2<> 18F2<> 20C2< 20C6< 20D2< 20D6<
	FBABA<0..1>	GPU_FBADDR_A:G:L:S:0:200	2	L:S::600				300 MHZ	18C8<> 18E3<
	RFBABA<0..1>	RAM_FBADDR_A:G:L:S:0:330	2	L:S::2400	50			300 MHZ	18E2<> 20C2< 20C6<
	FBARAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	2	L:S::400 MIL				300 MHZ	18C8> 18G3<
	FBACAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	2	L:S::400 MIL				300 MHZ	18C8> 18G3<
	FBAWE_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	2	L:S::400 MIL				300 MHZ	18C8> 18F3<
	FBACS0_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	2	L:S::400 MIL				300 MHZ	18C8> 18F3<
	FBACKE	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	2	L:S::400 MIL	100			300 MHZ	18D3< 18D7<>
	RFBARAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MIL	2	L:S::2700 MIL	50			300 MHZ	18G2<> 20B2< 20B6<
	RFBACAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18G2<> 20B2< 20B6<
	RFBAWE_L	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACS0_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MIL	2	L:S::2700 MIL	50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACKE	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18D2<> 20C2< 20C6<
	FBDQS<0..7>	GPU_FBDQS_A:G:L:S:0:100	2	L:S::350				300 MHZ	18C7<> 19A8<
	FBDQSTERM<0..7>	FB_DQSTERM_A:G:L:S:0:80	2	L:S::1500		10 MIL SPACING		300 MHZ	19A7<
	RFBDQS<0..7>	RAM_FBDQS_A:G:L:S:0:55	2	L:S::150		10 MIL SPACING		300 MHZ	19A6< 20C2<> 20C6<>
	FBACLK0	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18D7> 19C3<
	FBACLK0_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18D7> 19C3<
	FBACLK1	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18D7> 19D3<
	FBACLK1_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18D7> 19D3<
	RFBACLK1	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL	2	L:S::2500 MIL			200	300 MHZ	19D1< 20C2<
	RFBACLK1_L	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL	2	L:S::2500 MIL			200	300 MHZ	19D1< 20C2<
	RFBACLK0	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL	2	L:S::2500 MIL			200	300 MHZ	19C1< 20C6<
	RFBACLK0_L	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL	2	L:S::2500 MIL			200	300 MHZ	19C1< 20C6<
	FBD<64..127>	GPU_FBDATA_B:G:L:S:0:225	2	L:S::800				300 MHZ	18E5<> 18F5<> 18G5<> 19B5< 19B8< 19C5< 19C8<
	RFBD<64..127>	RAM_FBDATA_B:G:L:S:0:325	2	L:S::1000				300 MHZ	19B4< 19B7< 19C4< 19C7< 21B1<> 21B5<> 21C1<> 21C5<>
	FBDQM<8..15>	GPU_FBDQM_B:G:L:S:0:120	2	L:S::800				300 MHZ	18C3< 18D3< 18D5>
	RFBDQM<8..15>	RAM_FBDQM_B:G:L:S:0:120	2	L:S::1000				300 MHZ	18C2< 18D2< 21C2< 21C6<
	FBBA<0..12>	GPU_FBADDR_B:G:L:S:0:120	2	L:S::600				300 MHZ	18A3< 18B3< 18C3< 18C5<> 18D5<>
	RFBBA<0..11>	RAM_FBADDR_B:G:L:S:0:370	2	L:S::2400	50			300 MHZ	18B2<> 18C2<> 21C2< 21C6< 21D2< 21D6<
	FBBBA<0..1>	GPU_FBADDR_B:G:L:S:0:120	2	L:S::600				300 MHZ	18A3< 18C5<>
	RFBBBA<0..1>	RAM_FBADDR_B:G:L:S:0:370	2	L:S::2400	50			300 MHZ	18A2<> 21C2< 21C6<
	FBBRAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	2	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBCAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	2	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBWE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	2	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBCS0_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	2	L:S::400 MIL				300 MHZ	18A3< 18C4<>
	FBBCKE	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	2	L:S::400 MIL	100			300 MHZ	18C3< 18C4<>
	RFBBRAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	2	L:S::3500 MIL	3550			300 MHZ	18A3< 18C4<>
	RFBBCAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	2	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBWE_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	2	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCS0_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	2	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCKE	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	2	L:S::3500 MIL	3550			300 MHZ	18A2<> 21C2< 21C6<
	FBDQS<8..15>	GPU_FBDQS_B:G:L:S:0:100	2	L:S::350		10 MIL SPACING		300 MHZ	18D4<> 19A5<
	FBDQSTERM<8..15>	FB_FBDQSTERM_B:G:L:S:0:60	2	L:S::1500		10 MIL SPACING		300 MHZ	19A4<
	RFBDQS<8..15>	RAM_FBDQS_B:G:L:S:0:50	2	L:S::150		10 MIL SPACING		300 MHZ	19A3< 21C2<> 21C6<>
	FBBCLK0	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18C5<> 19B3<
	FBBCLK0_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18C5> 19B3<
	FBBCLK1	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18C5> 19C3<
	FBBCLK1_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	2	L:S::150 MIL			200	300 MHZ	18C5> 19B3<
	RFBBCLK1	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	2	L:S::2500 MIL			200	300 MHZ	19C1< 21C2<
	RFBBCLK1_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	2	L:S::2500 MIL			200	300 MHZ	19B1< 21C2<
	RFBBCLK0	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	2	L:S::2500 MIL			200	300 MHZ	19B1< 21C6<
	RFBBCLK0_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	2	L:S::2500 MIL			200	300 MHZ	19B1< 21C6<

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GROUP	SIG_NAME	RELATIVE_PROPAGATION_NAME	VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MAX_EXPOSED_LENGTH	
MAXBUS	CPU_ADDR<0..31>	CPU_ADDR_GROUP:G:L:S:0:MIL:30:MIL	7	:::5000	250			166 MHZ		4B7<> 4C7<> 8B4<> 8B5<> 8B7<> 8B8<> 8C4<> 8C5<> 8C7<> 8C8<> 9C3<> 9D3<> 9D5<> 9D8<>
	CPU_DATA<0..63>	CPU_DATA_GROUP:G:L:S:0:MIL:30:MIL	7	:::1400	1550			166 MHZ		9A3<> 9B4<> 9C4<> 9D4<> 6C4< 8C4<> 8C4< 8C5<> 8C7<> 8C7< 8C8<> 9D4<> 8D5<> 8D7<> 8D8<> 9A7< 9B1<> 9B7< 9C1<> 9C5< 9C8< 9D1<>
	CPU_BR_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4D7> 7C7< 8B4<> 9D3<>
	CPU_BG_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1000	250	10 MIL SPACING		166 MHZ		4D7< 7B7< 8B4<> 9D3<>
	CPU_TS_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4D7<> 7C7< 8B7<> 9D3<>
	CPU_TT<0..4>	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1350	250	10 MIL SPACING		166 MHZ		4B7<> 7A7< 8B4<> 8B5<> 9B3<>
	CPU_TBST_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4B7> 7B7< 8B4<> 9B3<>
	CPU_TSIZ<0..2>	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1250	250	10 MIL SPACING		166 MHZ		4B7> 8B5<> 8B7< 9B3<>
	CPU_ARTRY_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7<> 7C7< 8B8<> 9B3<>
	CPU_AACK_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7< 7B7< 8B5<> 9B3<>
	CPU_GBL_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1000	250	10 MIL SPACING		166 MHZ		4B8<> 8B5<>
	CPU_INT_GBL_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	6	:::3500	250	10 MIL SPACING		166 MHZ		4B8< 7B7< 9C3<>
	CPU_CI_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7> 7A7< 8C5<> 9C3<>
	CPU_HIT_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7> 7C7< 8B8<> 9B3<
	CPU_DBG_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::3500	250	10 MIL SPACING		166 MHZ		4C3< 7B7< 8B8<> 9B1<>
	CPU_DRDY_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	6	:::1500	250	10 MIL SPACING		166 MHZ		4C2< 7B7< 8B5<> 9B1<
	CPU_WT_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4B7> 7A7< 8B5<> 9B3<>
	CPU_DRDY_L_UF		2	:::5000	250	10 MIL SPACING		166 MHZ		4C3<>
	CPU_DTI<0..2>	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1500	250	10 MIL SPACING		166 MHZ		4C3< 8B4<> 8B7<> 9A1<>
	CPU_TA_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4C3< 7C7< 8C4<> 9A1<>
	CPU_TEA_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4C3< 7B7< 8B5<> 9A1<>
	CPU_QREQ_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::1000	250	10 MIL SPACING		166 MHZ		4C3> 7D5< 8B7<> 9B3<
	CPU_QACK_L	CPU_CNTL_GROUP:G:L:S:0:MIL:20:MIL	7	:::4000	250	10 MIL SPACING		166 MHZ		4C3< 8B4<> 9B3<>
	SYSCLK_CPU_UF		2	:::150		10 MIL SPACING		166 MHZ	315	9A3<>
	SYSCLK_CPU		4	::2200:2400	200	10 MIL SPACING		166 MHZ	315	4D2< 9A4<
	INT_CPU_FB_OUT		3	:::1000	200			166 MHZ	315	9B3<>
	CPU_FBO_PLUS1		3	:::200	200			166 MHZ	315	9A5<
	CPU_FBI_PLUS1		3	::1400:1500	200			166 MHZ	315	9A5<
	CPU_FB_MINUS3		4	::900:1000	200			166 MHZ	315	9A4<
	INT_CPU_FB_IN		4	:::1000	200			166 MHZ	315	9B3<
	CPU_FB_PLUS2		3	::900:1000				166 MHZ	315	9A5<
	CPU_FB_PLUS3		3	::2900:3000				166 MHZ	315	9A4<
	INT_ANALYZER_CLK		3	:::300				166 MHZ		8A2< 9B4< 16C7< 54A7< 59A7>
	SYSCLK_LA		2	:::2000				166 MHZ		8A2< 8D8<>
	INT_CLOCK_OUT		3	:::3000				166 MHZ		8B2<>

					MIN_LINE_WIDTH	DIFFERENTIAL_PAIR			
	USB2_XT1		3	:::1000	100	10 MIL SPACING	30 MHZ		32C4<
	USB2_XT2_B		3	:::1000	100	10 MIL SPACING	30 MHZ		
	USB2_XT2		3	:::100	100	10 MIL SPACING	30 MHZ		32C4<>
	USB2_RREF		2	:::100					32B4<>
	USB2_RSDAM	USB2_RSDA:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<>
	USB2_RSDAP	USB2_RSDA:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<>
	USB2_RSDBM	USB2_RSDB:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<>
	USB2_RSDBP	USB2_RSDB:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<>
	USB2_RSDCM	USB2_RSDC:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<> RATSNEST_SCEDULE
	USB2_RSDCP	USB2_RSDC:G:L:S:02MIL:20:MIL	3	:::600		8 MIL SPACING 3.5	480 MHZ		32C4<>
	USB2_DAN_F	USB2_DMA:G:L:S:0 MIL:30:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMA_DP MIN_DAISY_CHAIN	32C1<> 33B7<
	USB2_DAP_F	USB2_DMA:G:L:S:0 MIL:30:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMA_DP MIN_DAISY_CHAIN	32C1<> 33B7<
	USB2_DBN_F	USB2_DMB:G:L:S:0 MIL:20:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMB_DP MIN_DAISY_CHAIN	32C1<> 33C7<
	USB2_DBP_F	USB2_DMB:G:L:S:0 MIL:20:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMB_DP MIN_DAISY_CHAIN	32C1<> 33C7<
	USB2_DCN_F	USB2_DMC:G:L:S:0 MIL:20:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMC_DP MIN_DAISY_CHAIN	32C1<> 33D7<
	USB2_DCP_F	USB2_DMC:G:L:S:0 MIL:20:MIL	7	:::1500	50	8 MIL SPACING 3.5	480 MHZ	USB2_DMC_DP MIN_DAISY_CHAIN	32C1<> 33D7<
	USBT_DAN_F	USB2_DMAT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMAT_DP MIN_DAISY_CHAIN	33B6<>
	USBT_DAP_F	USB2_DMAT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMAT_DP MIN_DAISY_CHAIN	33B6<>
	USBT_DBN_F	USB2_DMBT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMBT_DP MIN_DAISY_CHAIN	33C6<>
	USBT_DBP_F	USB2_DMBT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMBT_DP MIN_DAISY_CHAIN	33C6<>
	USBT_DCN_F	USB2_DMCT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMCT_DP MIN_DAISY_CHAIN	33D6<>
	USBT_DCP_F	USB2_DMCT:G:L:S:04MIL:60:MIL	7	:::4000	2000	8 MIL SPACING 3.5	480 MHZ	USB2_DMCT_DP MIN_DAISY_CHAIN	33D6<>
	USB_DAN_CON	USB2_CONA:G:L:S:02MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONA_DP MIN_DAISY_CHAIN	33C3<> 59C5>
	USB_DAP_CON	USB2_CONA:G:L:S:02MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONA_DP MIN_DAISY_CHAIN	33C3<> 59C5>
	USB_DBN_CON	USB2_CONB:G:L:S:02MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONB_DP MIN_DAISY_CHAIN	33B3<> 59C5>
	USB_DBP_CON	USB2_CONB:G:L:S:02MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONB_DP MIN_DAISY_CHAIN	33B3<> 59C5>
	USB_DCN_CON	USB2_CONC:G:L:S:02MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONC_DP MIN_DAISY_CHAIN	33D3<> 59C5>
	USB_DCP_CON	USB2_CONC:G:L:S:0 MIL:30:MIL	3	:::750	50	8 MIL SPACING 3.5	480 MHZ	USB2_CONC_DP MIN_DAISY_CHAIN	33D3<> 59C5>

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DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MIN_LINE_WIDTH MAX_EXPOSED_LENGTH	PULSE_PARAM	
NEW STUFF HERE	VSYNC*		3	L:S::1000 MIL					22C5<>
	ANALOG_VSYNC*		4	L:S::3500 MIL					22D7< 25C6<> 26B5< 59B7>
	HSYNC*		3	L:S::1000 MIL					22C5<>
	ANALOG_HSYNC*		5	L:S::3500 MIL					22D7< 25D6<> 26B5< 59B7>
	ANALOG_BLU		4	L:S::4000 MIL	2400	10 MIL SPACING	5.8		22C7<> 25C6<
	ANALOG_GRN		4	L:S::4000 MIL	2400	10 MIL SPACING	5.8		22C7<> 25C6<
	ANALOG_RED		4	L:S::4000 MIL	2400	10 MIL SPACING	5.8		22C7<> 25B6<
	FILT_ANALOG_RED		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B7>
	FILT_ANALOG_GRN		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B7>
	FILT_ANALOG_BLU		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B7>
	DAC2RSET			L:S::1000 MIL		10 MIL SPACING			22C5<>
	DAC2VREF			L:S::1000 MIL		10 MIL SPACING			22C5<>
	NV11_XTALIN		4	L:S::1000 MIL	100	8 MIL SPACING		27 MHZ	22B4<>
	NV11_XTALOUT		4	L:S::1000 MIL	100	8 MIL SPACING		27 MHZ	22B4<>
	TCKP	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_CLK		24C4<>
	TCKM	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_CLK		24C3<>
	TD0P	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D0		24C3<>
	TD0M	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D0		24C4<>
	TD1P	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D1		24C4<>
	TD1M	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D1		24C3<>
	TD2P	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D2		24C3<>
	TD2M	TMDSFILT:G:L:S:0 2MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D2		24C4<>
	ENET_LINK_TX_EN		4	L:S::1000 MIL				25 MHZ	34D6<>
	ENET_LINK_TX_ER		4	L:S::1000 MIL				25 MHZ	34D6<>
	ENET_LINK_TXD<0..3>		4	L:S::1000				25 MHZ	34C6<>
	ENET_PHY_TX_EN		4	L:S::5600 MIL				25 MHZ	34D7< 35C6<
	ENET_PHY_TX_ER		4	L:S::5600 MIL				25 MHZ	34D7< 35C6<
	ENET_PHY_TXD<0..3>		4	L:S:4600:5600				25 MHZ	34C7< 35C6<
	CLKENET_LINK_TX		4	L:S:4600 MIL:5600 MIL				25 MHZ	34D7< 35C8<
	CLKENET_PHY_TX		4	L:S::1000 MIL				25 MHZ	35C6<>
	CLKENET_LINK_RX		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35C8<
	CLKENET_PHY_RX		4	L:S::1000 MIL				25 MHZ	35C6<>
	ENET_PHY_RXD<0..3>		4	L:S::1000				25 MHZ	35B6<> 35C6<>
	ENET_PHY_RX_DV		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_RX_ER		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_CRS		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_COL		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_LINK_RXD<0..3>		4	L:S:4600:5600				25 MHZ	34C7< 35B8< 35C8<
	ENET_CRS		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	ENET_COL		4	L:S:4600 MIL:5600 MIL				25 MHZ	34B7< 35B8<
	ENET_RX_DV		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	ENET_RX_ER		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	CLK25M_ENET_XIN		3	L:S::1000 MIL	400	8 MIL SPACING		25 MHZ	35B6<
	CLK25M_ENET_XOUT		3	L:S::1000 MIL	400	8 MIL SPACING		25 MHZ	35B6<>
	ENET_TDP	ETHTD:G:L:S:0 MIL:70 MIL	3	L:S::4000 MIL	3150	10 MIL SPACING	ETH_TXD	100 MHZ	35C3<>
	ENET_TDN	ETHTD:G:L:S:0 MIL:70 MIL	3	L:S::4000 MIL	3150	10 MIL SPACING	ETH_TXD	100 MHZ	35C3<>
	ENET_RDP	ETHRD:G:L:S:0 MIL:70 MIL	3	L:S::4000 MIL	3150	10 MIL SPACING	ETH_RXD	100 MHZ	35C3<>
	ENET_RDN	ETHRD:G:L:S:0 MIL:70 MIL	3	L:S::4000 MIL	3150	10 MIL SPACING	ETH_RXD	100 MHZ	35C3<>
	RJ45_TXP	RJTXD:G:L:S:0 MIL:70 MIL	2	L:S::750 MIL		2KV_ISO	RJ45_TXD	100 MHZ	35C1<>
	RJ45_TXN	RJTXD:G:L:S:0 MIL:70 MIL	2	L:S::750 MIL		2KV_ISO	RJ45_TXD	100 MHZ	35C1<>
	RJ45_RXP	RJRXD:G:L:S:0 MIL:70 MIL	2	L:S::750 MIL		2KV_ISO	RJ45_RXD	100 MHZ	35C1<>
	RJ45_RXN	RJRXD:G:L:S:0 MIL:70 MIL	2	L:S::750 MIL		2KV_ISO	RJ45_RXD	100 MHZ	35C1<>
	RJ45_TREF					2KV_ISO			35C2<>
	RJ45_RREF					2KV_ISO			35C2<>
	RJ45_4_5					2KV_ISO			35C1<>
	RJ45_7_8					2KV_ISO			35C1<>
	RJ45_F_TREF					2KV_ISO			35B2<
	FW_LINK_DATA<0..7>		4	L:S::1000					34C4<>
	FW_LINK_CNTL<0..1>		4	L:S::1000				49.152 MHZ	34C4<>
	FW_LINK_LREQ		4	L:S::1000 MIL				49.152 MHZ	34C4<>
	FW_SCLK		4	L:S:3500 MIL:4500 MIL				49.152 MHZ	34C5<> 36C8<
	FW_D<0..7>		4	L:S:3700:4700				49.152 MHZ	34C3< 36B8< 36C8<
	FW_CNTL0		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_CNTL1		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_LREQ		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_PHY_SCLK		4	L:S::500 MIL				49.152 MHZ	36C7<>
	FW_PHY_CNTL0		4	L:S::1000 MIL				49.152 MHZ	36C7<>
	FW_PHY_CNTL1		4	L:S::1000 MIL				49.152 MHZ	36C7<>
	FW_PHY_D<0..7>		4	L:S::1000				49.152 MHZ	36B7<> 36C7<>
	FW_XI		3	L:S::1000 MIL	100	8 MIL SPACING		24.576 MHZ	36C6<
	FW_XO		3	L:S::1000 MIL	100	8 MIL SPACING		24.576 MHZ	36C6<>
	FW_BIAS1								36C5<>
	FW_BIAS2								36C5<>
	FW_TPA1P	FWTPA1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPA1	400 MHZ	36C5<>
	FW_TPA1N	FWTPA1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPA1	400 MHZ	36C5<>
	FW_TPB1P	FWTPB1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPB1	400 MHZ	36C5<>
	FW_TPB1N	FWTPB1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPB1	400 MHZ	36C5<>
	FW_TPA2P	FWTPA2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPA2	400 MHZ	36C5<>
	FW_TPA2N	FWTPA2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPA2	400 MHZ	36C5<>
	FW_TPB2P	FWTPB2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPB2	400 MHZ	36C5<>
	FW_TPB2N	FWTPB2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPB2	400 MHZ	36C5<>
	FW_TPO1P	FWTPO1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPO1	400 MHZ	36B8<> 36D1<>
	FW_TPO1N	FWTPO1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPO1	400 MHZ	36A8<> 36D1<>
	FW_TPI1P	FWTPL1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPL1	400 MHZ	36A8<> 36D1<>
	FW_TPI1N	FWTPL1:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPL1	400 MHZ	36A8<> 36D1<>
	FW_TPO2P	FWTPO2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPO2	400 MHZ	36A8<> 36C1<>
	FW_TPO2N	FWTPO2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPO2	400 MHZ	36A8<> 36C1<>
	FW_TPI2P	FWTPL2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPL2	400 MHZ	36A8<> 36C1<>
	FW_TPI2N	FWTPL2:G:L:S:0 MIL:50 MIL	1	L:S::1220 MIL	5000		FW_TPL2	400 MHZ	36A8<> 36C1<>

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	STUB_LENGTH	NET_SPACING_TYPE	MIN_LINE_WIDTH MAX_EXPOSED_LENGTH	PULSE_PARAM	
NEW STUFF HERE	TMDS_CKP	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_CLK		23D1< 24B7<> 27C2< 59A7>
	TMDS_CKM	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_CLK		23D1< 24A7<> 27C2< 59A7>
	TMDS_D0P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D0		23D1< 24B7<> 27C2< 59B7>
	TMDS_D0M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D0		23D1< 24B7<> 27C2< 59A7>
	TMDS_D1P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D1		23D1< 24C7<> 27C2< 59B7>
	TMDS_D1M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D1		23D1< 24C7<> 27C2< 59B7>
	TMDS_D2P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D2		23D1< 24D7<> 27C2< 59B7>
	TMDS_D2M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D2		23D1< 24D7<> 27C2< 59B7>
	GPU_TMDS_CKP	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_CLK		23C2< 23D3<>
	GPU_TMDS_CKM	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_CLK		23C2< 23D3<>
	GPU_TMDS_D0P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D0		23C2< 23D3<>
	GPU_TMDS_D0M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D0		23C2< 23D3<>
	GPU_TMDS_D1P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D1		23C2< 23D3<>
	GPU_TMDS_D1M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D1		23C2< 23D3<>
	GPU_TMDS_D2P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D2		23C2< 23D3<>
	GPU_TMDS_D2M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D2		23C2< 23D3<>
	SI_TMDS_CKP	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_CLK		27C3<>
	SI_TMDS_CKM	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_CLK		27C3<>
	SI_TMDS_D0P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D0		27C3<>
	SI_TMDS_D0M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D0		27C3<>
	SI_TMDS_D1P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D1		27C3<>
	SI_TMDS_D1M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D1		27C3<>
	SI_TMDS_D2P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D2		27C3<>
	SI_TMDS_D2M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D2		27C3<>
	DVOD0	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 27A8< 27C5<
	DVOD1	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 27A8< 27C5<
	DVOD2	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 26D1< 27C5<
	DVOD3	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 26D1< 27C5<
	DVOD4	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD5	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD6	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD7	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD8	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 26B1< 27C5<
	DVOD9	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD10	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27B5<
	DVOD11	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27B5<

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DIGITAL SIGNALS (CONT'D)

	GROUP	SIG_NAME	RELATIVE_PROPAGATION	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM	
	CD DRIVE BUS	EIDE_RST_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 37D5<
		EIDE_DMACK_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7<> 37D5<
		EIDE_STOP			L:S::5500 MIL				33 MHZ	37A7> 37D5<
		EIDE_HSTB_RDY			L:S::5500 MIL				33 MHZ	37A7> 37C5<
		EIDE_DSTB_RDY			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 37C5<
		EIDE_DATA<0..15>			L:S:3500:5500				33 MHZ	37A5< 37B5< 37B7<> 37C5<
		CD_RESET_L			L:S::1000 MIL				33 MHZ	37D4< 38C6<>
		CD_DMACK_L			L:S::4000 MIL				33 MHZ	37D4< 38C6<>
		CD_STOP			L:S::5000 MIL				33 MHZ	37D4< 38C6<>
		CD_HSTB_RDY			L:S::5000 MIL				33 MHZ	37C4< 38C6<>
		CD_DSTB_RDY			L:S::1000 MIL				33 MHZ	37C4< 38C6<>
		UATAD<0..15>			L:S::1000				33 MHZ	37A4< 37B4< 37C4< 38C6<>
		CD_DMARQ			L:S::1000 MIL				33 MHZ	38C6<>
		EIDE_DMARQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<
		UATA0IRQ			L:S::1000 MIL				33 MHZ	38C6<>
		EIDE_INTRQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<
		CD_EIDE_ADDR<0..2>			L:S::1000				33 MHZ	38C6<>
		EIDE_ADDR<0..2>			L:S:3500:5500				33 MHZ	37B7> 38A8< 38B8<
		CD_CS1FX_L			L:S::1000 MIL				33 MHZ	38C6<>
		EIDE_CS1FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<
		CD_CS3FX_L			L:S::1000 MIL				33 MHZ	38C6<>
		EIDE_CS3FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<
	HD DRIVE BUS									
		UIDE_RST_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DMACK_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOR_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOW_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S::55000 MIL				100 MHZ	37C3< 37C7<>
		UIDE_IOCHRDY	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<
		UIDE_DATA<0..15>	HD_DATA:G:L:S:0:5500		L:S::100:6000				100 MHZ	37A3< 37B3< 37C3< 37C7<> 37D7<>
		HD_RESET_L			L:S::1000 MIL				100 MHZ	37D1< 38C3<>
		HD_DMACK_L			L:S::1000 MIL				100 MHZ	37D1< 38C3<>
		HD_DIOR_L			L:S::55000 MIL				100 MHZ	37D1< 38C3<>
		HD_DIOW_L			L:S::55000 MIL				100 MHZ	37C1< 38C3<>
		HD_IOCHRDY			L:S::1000 MIL				100 MHZ	37C1< 38C3<>
		HD_DMARQ			L:S::1000 MIL				100 MHZ	38C3<>
		UIDE_DMARQ	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 38C4<
		HD_INTRQ			L:S::1000 MIL				100 MHZ	38C3<>
		UIDE_INTRQ	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7< 38C4<
		HD_UIDE_ADDR<0..2>			L:S::1000				100 MHZ	38C2<> 38C3<>
		UIDE_ADDR<0..2>	HD_DATA:G:L:S:0:5500		L:S::100:6000				100 MHZ	37C7<> 38A4< 38B4<
		HD_UIDE_CS1FX_L			L:S::6000 MIL				100 MHZ	38C3<>
		UIDE_CS1FX_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S::6000 MIL				100 MHZ	37C7<> 38B4<
		HD_UIDE_CS3FX_L			L:S::6000 MIL				100 MHZ	38C2<>
		UIDE_CS3FX_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S::6000 MIL				100 MHZ	37C7<> 38B4<
		CLK_18M_INT_XOUT	3		L:S::1000	100	8 MIL SPACING		18.432 MHZ	58B5>
		CLK_18M_INT_XOUT	3		L:S::1000	100	8 MIL SPACING		18.432 MHZ	58B5>
		CLK_18M_INT_XOUT	3		L:S::200	50	8 MIL SPACING		18.432 MHZ	58B5>
		USB_DAP	USBA:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DAN	USBA:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DAP_F	USBA_F:G:L:S:0 MIL:500 MIL			100				28B2< 33B7<
		USB_DAN_F	USBA_F:G:L:S:0 MIL:500 MIL			100				28B2< 33B7<
		USB_DBP	USBB:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DBN	USBB:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DBP_F	USBB_F:G:L:S:0 MIL:500 MIL			100				28B2< 33C7<
		USB_DBN_F	USBB_F:G:L:S:0 MIL:500 MIL			100				28B2< 33C7<
		USB_DCP	USBC:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DCN	USBC:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
		USB_DCP_F	USBC_F:G:L:S:0 MIL:500 MIL			100				28B2< 33D7<
		USB_DCN_F	USBC_F:G:L:S:0 MIL:500 MIL			100				28B2< 33D7<
		USB_DEP	USBE:G:L:S:0 MIL:500 MIL							28B3<>
		USB_DEN	USBE:G:L:S:0 MIL:500 MIL							28B3<>
		BT_USB_DP	USBE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29D3<> 59B5>
		BT_USB_DM	USBE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29D3<> 59B5>
		USB_DFP	USBF:G:L:S:0 MIL:500 MIL							28B3<>
		USB_DFN	USBF:G:L:S:0 MIL:500 MIL							28B3<>
		MODEM_USB_DP	USBF_F:G:L:S:0 MIL:500 MIL			100				28B2< 29C5<> 59B5>
		MODEM_USB_DM	USFE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29C5<> 59B5>
		PMU_XO		3	L:S::1000 MIL	100	8 MIL SPACING		10 MHZ	44B5<
		PMU_XI		3	L:S::1000 MIL	100	8 MIL SPACING		10 MHZ	44B5<
		PMU_XT		3	L:S::300 MIL	50	8 MIL SPACING		10 MHZ	44A6<
		PMU_CLKOUT		3	L:S::1000 MIL	100	8 MIL SPACING		32.768 MHZ	44B4<>
		PMU_CLKIN		3	L:S::1000 MIL	100	8 MIL SPACING		32.768 MHZ	44B4<>
		PMU_CLKT		3	L:S::300 MIL	50	8 MIL SPACING		32.768 MHZ	44B2<>
		MICSHLD					10 MIL SPACING			29A5<> 43A8< 59A7>
		MICHIGH					10 MIL SPACING			29A5<> 43B8< 59A7>
		MICLOW					10 MIL SPACING			29A5<> 43A8< 59A7>
		KS_INT_SPKR+					10 MIL SPACING			29A3< 43D7< 59B7>
		KS_INT_SPKR-					10 MIL SPACING			29A3< 42B4< 43D7< 59B7>

	SIG_NAME	PROPAGATION_DELAY	PULSE_PARAM	
	T_UD_IDEDD_0	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
	T_UD_IDEDD_1	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
	T_UD_IDEDD_2	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
	T_UD_IDEDD_3	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
	T_UD_IDEDD_4	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
	T_UD_IDEDD_5	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
	T_UD_IDEDD_6	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
	T_UD_IDEDD_7	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
	T_UD_IDEDD_8	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
	T_UD_IDEDD_9	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
	T_UD_IDEDD_10	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
	T_UD_IDEDD_11	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
	T_UD_IDEDD_12	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
	T_UD_IDEDD_13	L:S::1000 MIL	100 MHZ	37A1< 38C2<>
	T_UD_IDEDD_14	L:S::1000 MIL	100 MHZ	37A1< 38C2<>
	T_UD_IDEDD_15	L:S::1000 MIL	100 MHZ	37A1< 38C2<>

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SIGNAL CONSTRAINTS

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FUNC_TEST

+1_8V_MAIN
+12V_MAIN
+12V_SLEEP
+12V_SLEEPA
+5V_MAIN
+5V_SLEEP
+2_5V_MAIN
+3V_MAIN
CPU_VCORE_SLEEP
JTAG_ASIC_TCK
JTAG_ASIC_TDI
JTAG_ASIC_TDO
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
INT_TMDS_3V
+1_5V_AGP
FAN_12V_FILT
+INTREPID_CORE_MAIN
INTREPID_VSENSE
OVDD_ADJ
CPU_CHKSTP_OUT_L
CPU_CHKSTP_IN_L
CPU_HRESET_L
JTAG_CPU_TCK
JTAG_CPU_TDI
JTAG_CPU_TDO
JTAG_CPU_TMS
JTAG_CPU_TRST_L
+MAXBUS_SLEEP
ROM_CS_L
ROM_OE_L
ROM_RW_L
DDC_VCC_3
DDC_VCC_5
SND_HP_SENSE_L
ANALOG_HSYNC*
ANALOG_VSYNC*
FILT_ANALOG_BLU
FILT_ANALOG_RED
FILT_ANALOG_GRN
GND
KS_INT_SPKR+
KS_INT_SPKR-
TMDS_D2P
TMDS_D2M
TMDS_D1P
TMDS_D1M
TMDS_D0P
TMDS_D0M
TMDS_CKP
TMDS_CKM
INV_CUR_HI_FILT
IO_RESET_L
KS5VSD
INT_I2C_CLK2
INT_I2C_DATA2
INT_ANALYZER_CLK
LAMP_STS_FILT
LCD_PWM_FILT
LED_5V_FILT
LED_RET_FILT
MICSHLD
MICHIGH
MICLOW
COMM_RESET_L
IIC_ADD
ROM_WP_L

FUNC_TEST

COMM_SHUTDOWN
MON_DETECT
FLO_KNOWS_BEST
NMI_BUTTON*
PWR_SWITCH*
PMU_RST*
PMURESETBUTTON*
PWR_SWITCH*
PWR_UP
POWER_UP*
RESET_BUTTON*
COMM_RING_DET_L
ROM_ONBOARD_CS_L
COMM_DTR_L
COMM_TXD_L
COMM_TRXC
COMM_RTS_L
COMM_RXD
COMM_GPIO_L
SLEEP
CPU_SRESET_L
PMU_AVCC
TMDS_DDC_CLK
TMDS_DDC_DAT
USB_DCN_CON
USB_DCP_CON
USB_DBN_CON
USB_DBP_CON
USB_DAN_CON
USB_DAP_CON
BT_USB_DP
BT_USB_DM
MODEM_USB_DP
MODEM_USB_DM
USB_PORT_PWR
VGA_IIC_CLK
VGA_IIC_DAT
CPU_VCORE_SLEEP
LINE_IN_COM
LINE_IN_R
LINE_IN_SENSE
LINE_IN_L
SND_LIN_SENSE_L
OUT_R FUNC_TEST
LINEOUT_COMM2 FUNC_TEST
LINE_OUT_L FUNC_TEST
PCIT_IRDY_L
RF_CLKRUN_L
NC_RF_DISABLE_L FUNC_TEST
PCI_DEVSEL_L
PCI_STOP_L
PCI_TRDY_L
PCI_FRAME_L
PCI_PAR
WL_PCI_IDSEL
33SLOTB_INT_L
PMU_PME_L
PCI_SLOTB_GNT_L
CLK33M_PCI_SLOTB
PCI_SLOTB_REQ_L
MAIN_RESET_L
PCI_CBE<0>
PCIT_CBE<1>
PCIT_CBE<2>
PCIT_CBE<3>
UNUSED_GPIO15

FUNC_TEST

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PCI_AD<4>
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PCIT_AD<29>
PCI_AD<30>
PCIT_AD<31>

CONSTRINT TABLES

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 59 OF 69	

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*** Signal Cross-Reference for the entire design ***

+1_5V_AGP 10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17A4< 17D5< 46B4<> 52C3> 59C7>

+1_5V_INTREPID_PLL 9D4< 16D6< 28D6<> 30D5< 52D3>
+1_5V_INTREPID_PLL1 28C4< 52D3>
+1_5V_INTREPID_PLL2 28D4< 52D3>
+1_5V_INTREPID_PLL3 28D4< 52D3>
+1_5V_INTREPID_PLL4 28D4< 52D3>
+1_5V_INTREPID_PLL5 16D5< 52D3>
+1_5V_INTREPID_PLL6 30D4< 52D3>
+1_5V_INTREPID_PLL7 9D2< 52D3>
+1_5V_INTREPID_PLL8 28D4< 52D3>
+1_8V_MAIN 52C4 59D7>
+2_5V_MAIN 30B3< 49B2<> 52C4 59D7>
+3.3VFPD 24D7< 51C1<> 52B6>
+3V_AUDIO 39D2< 39D6< 39D7< 40C3< 43B2< 43C6<
+3V_GPU_SS 22A6< 22A8< 22B7<
+3V_INTREPID_USB 28C4< 52A3>
+3V_MAIN 39D4< 40D5< 41A5< 41A7< 42B5< 42B7< 42C8< 43C7< 52C4 59D7>
+5VSD_T 50D6<>
+5V_AUDIO 39C6<> 39D7< 41B6<>
+5V_HP 41A8< 41B7<> 41D5<
+5V_MAIN 51B4<> 51B4<> 52C4 59D7>
+5V_SLEEP 38C1< 46C7< 46D6<> 50D5< 51C5<> 51C8< 59D7>
+12VSD_FILT 29A5<> 52B3>
+12VSD_T 50D6<>
+12V_DROPPED 44D8<
+12V_MAIN 36D8< 39C8< 42B3< 44D8< 45B4<> 45D3<> 45D7< 48C4<> 48C8<> 48D6<> 49C4<> 49D3<> 49D7<> 50B4<> 50C4<> 50D2< 50D5<> 51A5< 51A7< 51B7< 51C3< 51D7<> 52C1> 52C1> 59D7>
+12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51A5< 51C2< 51D6<> 52C1> 52C1> 59D7>
+12V_SLEEPA 59D7>
+12V_TPA 42B2< 42B7< 42C4< 42C5< 42D5<
+INTREPID_CORE_MAIN 10D6< 11D3< 46B3< 47B2<> 59C7>

+MAXBUS_SLEEP 4D5< 6C5< 6D6< 7A3< 7A3< 7B3< 7C3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C7>
3.8VH_TRICKLE 44C1< 44D7<> 52B3>
3.8V_TRICKLE 36D8< 44C2< 44C6< 44D7<> 50D5< 52C1> 52C2>
3V_SI_AVCC 27D4<
3V_SI_PLLVCC 27D4<
3V_SI_VCC 27B2< 27D3<
3_5_HONKER 51C4<>
3_6V_SLEEP 37D1< 51C1<
5V_XRA 50B4<>
15_I282 15B2<
15_I286 15B3<
18P_GND 29B5<>
25V_BSTH 49C5<>
25V_BSTH_TERM 49C5<>
25V_COMP 49B6<
25V_COMP_DWN 49B6<
25V_DH 49B5<>
25V_DHT 49B5<>
25V_DL 49B5<>
25V_DLT 49B4<>
25V_GND 49B6<>
25V_OCSET 49C5<>
25V_OVP 49B6<>
25V_VCC 49C6<
25V_VPWR 49B5<> 49C4<>
25V_VPWRA 49B4<>
25V_VSENSE 49C4<>
25_CORE_1 49C3<
33PCI_SLOTD_SERR_L 32B6<>
33SLOTB_INT_L 28B7<> 28B7<> 28B7<> 31C2<> 59A5>
42_I291 42B6<
42_I295 42B5<
45_I408 45B6<
45_I525 45C4<
45_I526 45B3<
47_I66 47B4<
48_I10 48C3<
48_I99 48B4<
49_I70 49B4<
50_I408 50B3<
50_I410 50A3<
AGND 39B7<> 52C4
AGP_AD<0> 16C4<> 17D8<
AGP_AD<0..15> 54C7<
AGP_AD<1> 16C4<> 17D8<
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AGP_AD<31> 16B4<> 17C8<
AGP_AD_STB<0> 16A4<> 16B3< 17B8< 54C7<
AGP_AD_STB<1> 16A4<> 16B3< 17B8< 54C7<
AGP_AD_STB_GPUUF<0> 17B6< 54B7<
AGP_AD_STB_GPUUF<1> 17B6< 54B7<
AGP_AD_STB_L<0> 16A4<> 16D1< 17B8< 54C7<
AGP_AD_STB_L<1> 16A4<> 16D1< 17B8< 54C7<
AGP_AD_STB_L_GPUUF<0> 17B6< 54B7<
AGP_AD_STB_L_GPUUF<1> 17B6< 54B7<
AGP_BUSY_L 16C6<> 16D1< 16D3< 17A8> 54B7<
AGP_CBE<0> 16B4<> 17C8<
AGP_CBE<0..1> 54C7<
AGP_CBE<1> 16B4<> 17C8<
AGP_CBE<2> 16B4<> 17C8<
AGP_CBE<2..3> 54C7<
AGP_CBE<3> 16B4<> 17C8<
AGP_DEVSEL_L 16B4<> 16C3< 17B8< 54C7<
AGP_FBI_EQUAL 16C7< 54A7<
AGP_FBO_EQUAL 16B7< 54A7<
AGP_FB_PLUS2 16B8< 54A7<
AGP_FRAME_L 16B4<> 16C3< 17B8< 54C7<
AGP_GNT_L 16C3< 16C4<> 17B6< 54B7<
AGP_INT_L 17B6<> 28B5<> 28B8<
AGP_IRDY_L 16B4<> 16C3< 17B8< 54C7<
AGP_PAR 16B4<> 17B8< 54B7<
AGP_PIPE_L 16A4<> 16B3< 17B8< 54B7<
AGP_PLLVDD 17C5<
AGP_PWR_ADJ 46A5<>
AGP_RBF_L 16A4<> 16B3< 17B8< 54B7<
AGP_REQ_L 16C3< 16C4<> 17B6<> 54B7<
AGP_RESET_L 17B8< 27C5< 44D3<
AGP_SBA<0> 16B4< 16C1< 17A8<
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AGP_SBA<1> 16B4<> 16C1< 17A8<
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AGP_TRDY_L 16B3< 16B4<> 17B8< 54C7<
AGP_WBF_L 16A6<> 16B1< 17B8< 54B7<
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AINLP 39C4<
AINRM 39C4<
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ANALOG_GRN 22C7<> 25C6< 57D5>
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ANALOG_RED 22C7<> 25B6< 57D5>
ANALOG_VSYNC* 22D7< 25C6<> 26B5< 57D5> 59B7>
ANEN 35C4<
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ASH 43A6<
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BRE_1 45B5<>
BT1 44D6<> 51A6<
BT1_LED 51A6<
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CD_CS3FX_L 38C6<> 58C5>
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CD_DMARQ 38C6<> 58D5>
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CD_EIDE_ADDR<1> 38C6<>
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CD_RESET_L 37D4< 38C6<> 58D5>
CD_STOP 37D4< 38C6<> 58D5>
CHGND 24B3< 29A3< 43A7< 43B7< 52C4
CHOC_BROWNIE 51B2<
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CLK33M_PCI_SLOTB_UF 30D5<> 54D7<
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COMM_GPIO_L 28C3<> 28D3< 29C5<> 59C5>
COMM_RESET_L 28C5<> 29D5<> 59A7>
COMM_RING_DET_L 28B5<> 28B8< 29C5<> 44C5<> 59D5>
COMM_RTS_L 28C3> 29D5<> 59C5>
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COMM_SHUTDOWN 28C5<> 28D1< 29D7<> 59D5>
COMM_TRXC 28C3<> 28D3< 29C7<> 59C5>
COMM_TXD_L 28C3<> 29C7<> 59C5>
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CORE_MOSFET_1 45B5<> 45C7<>
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ENET_RDN 35C3<> 57B5>
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FBBCKE 18A3< 18C4<> 55B3>
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INT_PU_RESET_L   15B3< 34C3< 44C2<> 44C2<>
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INT_RESET_L      34C3< 35B8< 41A7< 43C7< 44D2<>
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INT_ROM_OE_L     30C5<>
INT_ROM_OVERLAY_PU  16D7< 30A7< 30C5<> 54A7<
INT_ROM_RW_L     30C5<>
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INT_SND_SCLK     28A3<>
INT_SND_SYNC     28B3<>
INT_SND_TO_AUDIO  28B3<>
INT_SPKR+        42A6<> 43D8<
INT_SPKR-        42A6<> 43D8<
INT_SUSPEND_ACK_L  9B3> 44B5<>
INT_SUSPEND_REQ_L  9B3< 44B8<>
INT_TMDS_3V      24C3<> 52A6> 59C7>
INT_TST_MONIN_PD  34B7< 34C1<
INT_TST_PLLEN_PD  28C6< 34B7<
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INV_CUR_HI       23D7< 29B8<
INV_CUR_HI_FIT   29A5<> 59A7>
IO_RESET_L       32A6< 35B8< 44B8<> 44D3< 59A7>
IPWRGD           46A8< 47A6<>
JAZ              43B6<
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JTAG_ASIC_TDO    8A4<> 35B4<> 59D7>
JTAG_ASIC_TMS    8A4<> 34B7< 35A2< 35B4<> 59D7>
JTAG_ASIC_TRST_L  8A4<> 34B7< 59C7>
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JTAG_CPU_TDI     4C3< 7A5< 8A3<> 59C7>
JTAG_CPU_TDO     4C3> 8A3<> 59C7>
JTAG_CPU_TMS     4C3< 7A5< 8A3<> 59C7>
JTAG_CPU_TRST_L  4C3< 7C5< 8A3<> 59C7>
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JTAG_INTRP_TDO   28C6< 34B7> 35B3<
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KS_INT_SPKR-     29A3< 42B4< 43D7< 58A5> 59B7>
KS_INT_SPKR-_FILT  29A5<>
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L32_2            40B6<>
L36_2            40B6<
L41_FILT         42B7<>
L43_1            41A4<
L59_2_I461       43A5<
L3202_1          40C6<
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LCD_PWM_FILT     29A5<> 59A7>
LED_5V           29A8< 52B3>
LED_5V_FILT      29A5<> 52B3> 59A7>
LED_RET          29A3< 51B6< 52B3>
LED_RET_FILT     29A5<> 52A3> 59A7>
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LINA             39C4< 40C2<
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LINE_IN_COM      40B7<> 59B5>
LINE_IN_L        40B7<> 40C7<> 59B5>
LINE_IN_R        40B6<> 40B7<> 59B5>
LINE_IN_SENSE    40B7<> 40C7<> 59B5>
LINE_OUT_L       59B5>
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LINP             42C5< 43D4<
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LO_T1            41A4<
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LPR1             41C6<
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M1L              43A6<> 43B6<>
M1S              43A6<> 43B6<>
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                 59A5>
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MAX_PWR_ADJ      46C5<>
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MEM_WE_L         12B3< 12C6<> 53C6<
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MIC2            43B4<
MIC3            43B4<
MIC4            43B3<>
MIC5            43A3<
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MR_FLO_1        45B4<>
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RF_DISABLE_L	31C3<>
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RINN	42C4< 43C2<
RINN1	43C2<
RINP	42C4< 43D4<
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RINT_RESET_L	34C5<
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RJ45_7_8	35C1<> 57B5>
RJ45_F_TREF	35B2< 57B5>
RJ45_RREF	35C2<> 57B5>
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RJ45_RXP	35C1<> 57B5>
RJ45_TREF	35C2<> 57B5>
RJ45_TXN	35C1<> 57B5>
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ROMA15	18C8< 26D8<
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ROM_OE_L	30B2< 30C6< 31B2<> 59C7>
ROM_ONBOARD_CS_L	30B2< 31B4<> 59D5>
ROM_RW_L	30B2< 30B6< 31B4<> 59B7>
ROM_WP_L	30B2< 59A7>
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RT401P1	47C5<>
RT406P2	47B3<>
RT418P2	50C7<
RUNLED1	51C8<
RUNSS	50C8< 50D3<
S3700P1	44A1<>
S3700P2	44A1<>
SB1P1	44A3<
SENSE+	45C6<
SENSE+_1	45B5< 45C7<
SENSE-	45C6< 45C8<>
SENSE-_1	45B5< 45C7<
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SGRBVREF	21A3< 21C4< 21C8< 52A6>
SHS	50C7<
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SI_SCL	23D2< 27C5<
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SI_TMDS_CKP	27C3<> 57C2>
SI_TMDS_D0M	27C3<> 57C2>
SI_TMDS_D0P	27C3<> 57C2>
SI_TMDS_D1M	27C3<> 57C2>
SI_TMDS_D1P	27C3<> 57C2>
SI_TMDS_D2M	27C3<> 57C2>
SI_TMDS_D2P	27C3<> 57C2>
SI_VREF	27B3<
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SND_AMP_M_L	42D3< 43C7<>
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SND_HP_M_L	41A7<>
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SND_HP_SENSE_L	28B5<> 41A5< 59B7>
SND_HW_RESET_L	28A8< 28B5<> 39B4<
SND_LIN_SENSE_L	28B5<> 40D4< 59B5>
SND_SCLK	28A1< 39B1<>
SND_SPKR_ID	28B5<> 42B8<
SND_SPKR_ID_U10	42B8<
SND_SYNC	28B1< 39C1<>
SND_TO_AUDIO	28B1< 39C4<
SNF_FSEL	28C5<> 28D3<
SPDA	42B7<
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SPKROUT_L_P	42A8< 42C8<
SPKROUT_R_N	42A8< 42C1<
SPKROUT_R_P	42A8< 42C1<
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SPKR_LM	42A5<>
SPKR_LP	42A5<>
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SW3V5V_INTVCC	50B5<> 50C6<>
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SYSCLK_CPU_UF	9A3<> 56C3>
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SYSCLK_DDRCLK_A0_L	12C4< 14D6<> 53C6<
SYSCLK_DDRCLK_A0_L_UF	12B6<> 53C6<
SYSCLK_DDRCLK_A0_UF	12B6<> 53C6<
SYSCLK_DDRCLK_A1	12C4< 14A4<> 53C6<
SYSCLK_DDRCLK_A1_L	12B4< 14A4<> 53C6<
SYSCLK_DDRCLK_A1_L_UF	12B6<> 53C6<
SYSCLK_DDRCLK_A1_UF	12B6<> 53C6<
SYSCLK_DDRCLK_A2_L	53B6<
SYSCLK_DDRCLK_A2_L_UF	12B6<> 53B6<
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SYSCLK_DDRCLK_B0	12B4< 15B4> 53B6<
SYSCLK_DDRCLK_B0_L	12B4< 15B3> 53B6<
SYSCLK_DDRCLK_B0_L_UF	12B6<> 53B6<
SYSCLK_DDRCLK_B0_UF	12B6<> 53B6<
SYSCLK_DDRCLK_B1	12A4< 15D6< 53B6<
SYSCLK_DDRCLK_B1_L	12A4< 15C6< 53B6<
SYSCLK_DDRCLK_B1_L_UF	12B6<> 53B6<
SYSCLK_DDRCLK_B1_UF	12B6<> 53B6<
SYSCLK_DDRCLK_B2	12A4< 15A6< 53B6<
SYSCLK_DDRCLK_B2_L	12A4< 15A6< 53B6<
SYSCLK_DDRCLK_B2_L_UF	12B6<> 53B6<
SYSCLK_DDRCLK_B2_UF	12B6<> 53B6<
SYSCLK_LA	8A2< 8D8<> 56B3>
SYSTEM_CLK_EN	28A5< 44C4<>
TAS_DVDD	39D3<
TAS_PWR_DOWN	39B4< 39D7<
TAS_STAR_GND	39A7<> 39D2<
TAS_VCOM	39B1<> 39B1<> 43D5<
TCKM	24C3<> 57C5>
TCKP	24C4<> 57C5>
TD0M	24C4<> 57C5>
TD0P	24C3<> 57C5>
TD1M	24C3<> 57C5>
TD1P	24C4<> 57C5>
TD2M	24C4<> 57C5>
TD2P	24C3<> 57C5>
TESTEN	35A5< 35C4<
TI_MODE_OUT	42D4<>
TI_MODE_OUT_2	42C7<
TI_SD*	42D5<
TMDS_CKM	23D1< 24A7<> 27C2< 57D2> 59A7>
TMDS_CKP	23D1< 24B7<> 27C2< 57D2> 59A7>
TMDS_D0M	23D1< 24B7<> 27C2< 57D2> 59A7>
TMDS_D0P	23D1< 24B7<> 27C2< 57D2> 59B7>
TMDS_D1M	23D1< 24C7<> 27C2< 57D2> 59B7>
TMDS_D1P	23D1< 24C7<> 27C2< 57D2> 59B7>
TMDS_D2M	23D1< 24D7<> 27C2< 57D2> 59B7>
TMDS_D2P	23D1< 24D7<> 27C2< 57D2> 59B7>
TMDS_DDC_CLK	24B3<> 59C5>
TMDS_DDC_DAT	24B4<> 59C5>
TMDS_EN	23D7<> 51B1<>
TPA_5V	42D4<
TPA_AVDD_REF	42D4<
TPA_BSLN	42D5<>
TPA_BSLP	42D5<>
TPA_BSRN	42D4<>
TPA_BSRP	42D4<>
TPA_COSC	42C4<>
TPA_LOUTN	42C5<>
TPA_LOUTP	42C5<>
TPA_MODE	42D4<
TPA_ROSC	42C4<>
TPA_ROUTN	42C4<>
TPA_ROUTP	42C4<>
TPA_V2P5	42D5<
TPA_VCLAMPL	42C5<
TPA_VCLAMPR	42C4<
TPA_VOL	42D5<
TRANS_ADJ	45B3<
T_UD_IDEDD_0	37C1< 38C3<> 58C2>
T_UD_IDEDD_1	37C1< 38C3<> 58C2>
T_UD_IDEDD_2	37C1< 38C3<> 58C2>
T_UD_IDEDD_3	37C1< 38C3<> 58C2>
T_UD_IDEDD_4	37B1< 38C3<> 58C2>
T_UD_IDEDD_5	37B1< 38C3<> 58C2>
T_UD_IDEDD_6	37B1< 38C3<> 58B2>
T_UD_IDEDD_7	37B1< 38C3<> 58B2>
T_UD_IDEDD_8	37B1< 38C2<> 58B2>
T_UD_IDEDD_9	37B1< 38C2<> 58B2>
T_UD_IDEDD_10	37B1< 38C2<> 58B2>
T_UD_IDEDD_11	37B1< 38C2<> 58B2>
T_UD_IDEDD_12	37B1< 38C2<> 58B2>
T_UD_IDEDD_13	37A1< 38C2<> 58B2>
T_UD_IDEDD_14	37A1< 38C2<> 58B2>
T_UD_IDEDD_15	37A1< 38C2<> 58B2>
U5_SDOUT	39C3<>
U10_A	42C7<
U10_OUT	42C7> 42D8<
U22_8	36D8<
U4202P2	40C3<
U4202P3	40C3<
U4202P5	40B3<
U4202P6	40B3<
U4202P7	40B3<>
UATA0IRQ	38C6<> 58D5>
UATAD<0>	37C4< 38C6<>
UATAD<0..15>	58D5>
UATAD<1>	37C4< 38C6<>
UATAD<2>	37C4< 38C6<>
UATAD<3>	37C4< 38C6<>
UATAD<4>	37B4< 38C6<>
UATAD<5>	37B4< 38C6<>
UATAD<6>	37B4< 38C6<>
UATAD<7>	37B4< 38C6<>
UATAD<8>	37B4< 38C6<>

UATAD<9>	37B4< 38C6<>	
UATAD<10>	37B4< 38C6<>	
UATAD<11>	37B4< 38C6<>	
UATAD<12>	37B4< 38C6<>	
UATAD<13>	37A4< 38C6<>	
UATAD<14>	37A4< 38C6<>	
UATAD<15>	37A4< 38C6<>	
UIDE_ADDR<0>	37C7<> 38B4<	
UIDE_ADDR<0..2>	58B5>	
UIDE_ADDR<1>	37C7<> 38B4<	
UIDE_ADDR<2>	37C7<> 38A4<	
UIDE_CS1FX_L	37C7<> 38B4< 58B5>	
UIDE_CS3FX_L	37C7<> 38B4< 58B5>	
UIDE_CSELP_L	38C2<> 52A8>	
UIDE_DATA<0>	37C3< 37D7<>	
UIDE_DATA<0..15>	58C5>	
UIDE_DATA<1>	37C3< 37D7<>	
UIDE_DATA<2>	37C3< 37D7<>	
UIDE_DATA<3>	37C3< 37D7<>	
UIDE_DATA<4>	37B3< 37D7<>	
UIDE_DATA<5>	37B3< 37D7<>	
UIDE_DATA<6>	37B3< 37D7<>	
UIDE_DATA<7>	37B3< 37D7<>	
UIDE_DATA<8>	37B3< 37D7<>	
UIDE_DATA<9>	37B3< 37D7<>	
UIDE_DATA<10>	37B3< 37C7<>	
UIDE_DATA<11>	37B3< 37C7<>	
UIDE_DATA<12>	37B3< 37C7<>	
UIDE_DATA<13>	37A3< 37C7<>	
UIDE_DATA<14>	37A3< 37C7<>	
UIDE_DATA<15>	37A3< 37C7<>	
UIDE_DIOR_L	37C7<> 37D3< 58C5>	
UIDE_DIOW_L	37C3< 37C7<> 58C5>	
UIDE_DMACK_L	37C7<> 37D3< 58C5>	
UIDE_DMARQ	37C7<> 38C4< 58C5>	
UIDE_INTRQ	37C7< 38C4< 58C5>	
UIDE_IOCHRDY	37C3< 37C7< 58C5>	
UIDE_PDIAG	38C2<>	
UIDE_REF	37C7<>	
UIDE_RST_L	37C7<> 37D3< 58C5>	
UNUSED_ATAIOCS16_L	38C2<> 52A8>	
UNUSED_EXTINT7	28B5<> 28B8<>	
UNUSED_EXTINT8	28B5<> 28B8<>	
UNUSED_GPIO15	28B5<> 28C1< 59A5>	
USB2_CRUN_L	32A6<>	
USB2_CRUN_L_INT	28A8< 28B5<> 32A8<	
USB2_DAN_F	32C1<> 33B7< 56B3>	
USB2_DAP_F	32C1<> 33B7< 56B3>	
USB2_DBN_F	32C1<> 33C7< 56B3>	
USB2_DBP_F	32C1<> 33C7< 56B3>	
USB2_DCN_F	32C1<> 33D7< 56B3>	
USB2_DCP_F	32C1<> 33D7< 56B3>	
USB2_IDSEL	32B6<	
USB2_NC1	32B4<>	
USB2_NC2	32B4<>	
USB2_PME_L	32A6<>	
USB2_RREF	32B4<> 56B3>	
USB2_RSDAM	32C4<> 56B3>	
USB2_RSDAP	32C4<> 56B3>	
USB2_RSDBM	32C4<> 56B3>	
USB2_RSDBP	32C4<> 56B3>	
USB2_RSDCM	32C4<> 56B3>	
USB2_RSDCP	32C4<> 56B3>	
USB2_VCCRST	32A6<	
USB2_XT1	32C4< 56B3>	
USB2_XT2	32C4<> 56B3>	
USB2_XT2_B	56B3>	
USBT_DAN_F	33B6<> 56B3>	
USBT_DAP_F	33B6<> 56B3>	
USBT_DBN_F	33C6<> 56A3>	
USBT_DBP_F	33C6<> 56A3>	
USBT_DCN_F	33D6<> 56A3>	
USBT_DCP_F	33D6<> 56A3>	
USB_DAN	28A3< 28B3<> 58B5>	
USB_DAN_CON	33C3<> 56A3> 59C5>	
USB_DAN_F	28B2< 33B7< 58B5>	
USB_DAP	28A3< 28B3<> 58B5>	
USB_DAP_CON	33C3<> 56A3> 59C5>	
USB_DAP_F	28B2< 33B7< 58B5>	
USB_DBN	28A3< 28B3<> 58B5>	
USB_DBN_CON	33B3<> 56A3> 59C5>	
USB_DBN_F	28B2< 33C7< 58B5>	
USB_DBP	28A3< 28B3<> 58B5>	
USB_DBP_CON	33B3<> 56A3> 59C5>	
USB_DBP_F	28B2< 33C7< 58B5>	
USB_DCN	28A3< 28B3<> 58B5>	
USB_DCN_CON	33D3<> 56A3> 59C5>	
USB_DCN_F	28B2< 33D7< 58B5>	
USB_DCP	28A3< 28B3<> 58B5>	
USB_DCP_CON	33D3<> 56A3> 59C5>	
USB_DCP_F	28B2< 33D7< 58B5>	
USB_DDN	28B3<>	
USB_DDN_F_TERM	28B2<	
USB_DDP	28B3<>	
USB_DDP_F_TERM	28B2<	
USB_DEN	28B3<> 58B5>	
USB_DEP	28B3<> 58B5>	
USB_DFN	28B3<> 58A5>	
USB_DFP	28B3<> 58A5>	
USB_GND	52A3>	
USB_OC_EF_L	28B3< 28C2<	
USB_PORT_PWR	33A4<> 33B3<> 33C3<> 33D3<> 52A3> 59B5>	
USB_PWR	25B5<> 25C2< 25D3<> 33A6<> 52A3>	
USB_PWREN_AB_L	28B3<> 28C2<	
USB_PWREN_CD_L	28B3<> 28C2<	
USB_PWREN_EF_L	28B3<> 28C2<	
USB_PWR_EN	33A8<>	
USB_PWR_FLT*	28B3< 28C1< 32B1< 33A7>	
UX6P23	39C4<	

UX6_LINB	39C4<	
U_USB_PWR_FLT*	32B4<	
VCOML	43D5<	
VCOMR	43D5<	
VCOREIN	45D6<>	
VCORE_BG	45C6<>	
VCORE_BG_1	45B5< 45C7<>	
VCORE_BOOST	45C5<>	
VCORE_BOOST2	45C6<>	
VCORE_BOOST2_1	45B5< 45C7<>	
VCORE_BOOST_1	45B5<>	
VCORE_EXTVCC	45D7<	
VCORE_FREQSET	45C7<	
VCORE_INTVCC	45C5<> 45D5<> 45D7<>	
VCORE_SEN+	45C3<>	
VCORE_SEN+_1	45A3<>	
VCORE_SENA+	45C3<>	
VCORE_SF	45C8<	
VCORE_SGND	45B7<> 45C7<> 45C7<> 45C8<> 45C8<>	
VCORE_STBY	45C7<>	
VCORE_TG	45C6<>	
VCORE_TG_1	45B5< 45C7>	
VCORE_VGATE	28B5<> 28D3<	
VCORE_VIN	45D7<>	
VC_CNTL1	44C7< 45D8<	
VC_SENA	45B3<>	
VGA_IIC_CLK	25C4<> 59B5>	
VGA_IIC_DAT	25C4<> 59B5>	
VGER_INV_HRESET	7A3< 7B3< 7B3< 7C3< 44D1>	
VIPCLK	22D4< 52A8>	
VIPD0	22D4<> 26B7<	
VIPD1	22D4<> 26B7<	
VIPD2	22D4<> 26B8<	
VIPD3	22D4<> 26D7<	
VIPD4	22D4<> 26D7<	
VIPD5	22D4<> 26D7<	
VIPD6	22D4<> 26B8<	
VIPD7	22D4<> 26C5<	
VIPHAD0	22D5<> 26B7<	
VIPHAD1	22D5<> 26B7<	
VIPHCTL	22D5<> 26D5<	
VIP_PD	22D4<	
VIP_PU	22D4<	
VOSNS1	50B8<>	
VOSNS2	50B5<>	
VR4210P1	39B7<	
VREFM	39B4<	
VREFP	39B4< 43A3<	
VRFILT	39B3<>	
VSYNC*	22C5<> 57D5>	
WL_PCI_IDSEL	31C2<> 59A5>	
XMIT_LED	35A2< 35B4<>	
ZT8P1	4A1<>	
ZT9P1	4B2<>	
ZT10P1	4A2<>	
ZT11P1	4B1<>	

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SIZE	DRAWING NUMBER	REV.
D	051-6569	A
SCALE: NONE	SHT 64 OF 69	

*** Part Cross-Reference for the entire design ***

BS1	PCB_STANDOFF	29B5
BS2	PCB_STANDOFF	29B6
BS3	PCB_STANDOFF	29D1
BS4	PCB_STANDOFF	29D1
BT1	BATTERY	44D6
C1	CAP	33C4
C2	CAP	33D4
C3	CAP	35B1
C4	CAP	36B6
C5	CAP_P	33A5
C6	CAP	33B4
C7	CAP_P	33A5
C8	CAP	21A4
C9	CAP	21A4
C10	CAP_P	36D7
C11	CAP	21A4
C12	CAP_P	36D7
C13	CAP_P	41C4
C14	CAP	12A7
C15	CAP	21D2
C16	CAP	21B4
C17	CAP	21D5
C18	CAP	51D3
C19	CAP_P	51D4
C20	CAP	21B2
C21	CAP	21D5
C22	CAP	21B4
C23	CAP	21B4
C24	CAP_P	40B4
C25	CAP_P	40C4
C26	CAP_P	41D4
C27	CAP	36D8
C28	CAP	21B1
C29	CAP	21B3
C30	CAP	12A6
C31	CAP	21B2
C32	CAP	21D4
C33	CAP	21B2
C34	CAP	21B3
C35	CAP	43B5
C36	CAP	42D7
C37	CAP	35D7
C38	CAP	21D2
C39	CAP	21D5
C40	CAP	21B3
C41	CAP	35D8
C42	CAP	36B8
C43	CAP	41D6
C44	CAP	35D4
C45	CAP	42B8
C46	CAP	14D8
C47	CAP	14D8
C48	CAP	15D8
C49	CAP	15D8
C50	CAP	15D7
C51	CAP	15C3
C52	CAP	35D4
C53	CAP	35D5
C54	CAP	18B8
C55	CAP	15C1
C56	CAP	35D4
C57	CAP	35D6
C58	CAP	15B1
C59	CAP_P	48B2
C60	CAP	41C6
C61	CAP	18B6
C62	CAP	18D6
C63	CAP	40B2
C64	CAP	40C2
C65	CAP	35D7
C66	CAP	35D7
C67	CAP	35D5
C68	CAP	35D6
C69	CAP	18B5
C70	CAP	18B6
C71	CAP_P	48B1
C72	CAP	18H7
C73	CAP	18H7
C74	CAP	35B7
C75	CAP	18H5
C76	CAP	35B7
C77	CAP	32D3
C78	CAP	18H6
C79	CAP	18H4
C80	CAP	18H2
C81	CAP	18H7
C82	CAP	18H4
C83	CAP	18H3
C84	CAP	18H8
C85	CAP_P	39C6
C86	CAP	18H8
C87	CAP	17B2
C88	CAP_P	48B1
C89	CAP	18H2
C90	CAP	18H7
C91	CAP	17B3
C92	CAP	34B6
C93	CAP	17C3
C94	CAP	17C3
C95	CAP	18H5
C96	CAP	18H2
C97	CAP	17B3
C98	CAP	18H6
C99	CAP	17D1
C100	CAP	17D3
C101	CAP	17D2
C102	CAP	17C2
C103	CAP	17D2
C104	CAP	17D4
C105	CAP	17B2
C106	CAP_P	48B2
C107	CAP	24B2
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C109	CAP	17D3
C110	CAP	17D2
C111	CAP	17B3
C112	CAP	17B2
C113	CAP	27D5
C114	CAP	32D3
C115	CAP	18H3
C116	CAP	17B3
C117	CAP	17D3
C118	CAP	17C3
C119	CAP	23B5
C120	CAP	17C3
C121	CAP	39C4
C122	CAP	42C8
C123	CAP	30C3
C124	CAP	18H1
C125	CAP	23B6
C126	CAP_P	39C7
C127	CAP_P	39B2
C128	CAP	22D3
C129	CAP	17B3
C130	CAP	23B6
C131	CAP	23B4
C132	CAP_P	48B2
C133	CAP	18H6
C134	CAP	17D3
C135	CAP	17C2
C136	CAP	17B3
C137	CAP	17B4
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C140	CAP	17C2
C141	CAP	20B3
C142	CAP	20D5
C143	CAP	20D5
C144	CAP	20D5
C145	CAP	18H2
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C147	CAP	17C3
C148	CAP	17C4
C149	CAP	17C3
C150	CAP	17C3
C151	CAP	17C2
C152	CAP	23B5
C153	CAP	22C7
C154	CAP	42C8
C155	CAP	42C1
C156	CAP	42C1
C157	CAP	20A4
C158	CAP	20D5
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C160	CAP	23C6
C161	CAP	17C4
C162	CAP	22C6
C163	CAP	22C6
C164	CAP	22C6
C165	CAP	20B3
C166	CAP	20B3
C167	CAP	18H5
C168	CAP	17C3
C169	CAP	17C2
C170	CAP	22C7
C171	CAP	46A6
C172	CAP	20A4
C173	CAP	20B2
C174	CAP	20B4
C175	CAP	18H3
C176	CAP	17D2
C177	CAP	17B4
C178	CAP	17D4
C179	CAP	17B3
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C184	CAP	17B2
C185	CAP	17D3
C186	CAP	17B4
C187	CAP	17B3
C188	CAP	17B1
C189	CAP	23C7
C190	CAP	22C7
C191	CAP	20A5
C192	CAP	17D4
C193	CAP	17B5
C194	CAP	20B4
C195	CAP	20B1
C196	CAP	20B2
C197	CAP	20B2
C198	CAP	20B4
C199	CAP	18H3
C200	CAP	17D4
C201	CAP	17D4
C202	CAP	17D3
C203	CAP	17D2
C204	CAP	40C5
C205	CAP	20D2
C206	CAP	22C2
C207	CAP	22C7
C208	CAP	41A5
C209	CAP	22B6
C212	CAP	22D6
C213	CAP	22D6
C214	CAP	17B3
C215	CAP	17A3
C216	CAP	20D2
C217	CAP	17C1
C218	CAP_P	49B3
C219	CAP	17C2
C220	CAP_P	48C8
C222	CAP	16A8
C223	CAP	17C2
C224	CAP	22C2
C225	CAP	30C2
C226	CAP	22D6
C227	CAP	22C3
C228	CAP	22C3
C229	CAP	28C6
C230	CAP	13D7
C231	CAP	11A6
C232	CAP	11A6
C233	CAP	28D6
C234	CAP	28D7
C235	CAP_P	49B2
C236	CAP	51B3
C238	CAP_P	51C5
C239	CAP	44A4
C240	CAP	11C8
C241	CAP	50C5
C242	CAP	14C2
C243	CAP	14C2
C244	CAP	14C3
C245	CAP_P	44D5
C246	CAP_P	51B3
C248	CAP	39B4
C249	CAP	31D1
C250	CAP	31D2
C252	CAP	51B2
C254	CAP	51B1
C255	CAP	14C2
C256	CAP	14C1
C257	CAP	51B2
C258	CAP	51B2
C259	CAP	31D1
C260	CAP	31D2
C261	CAP	14C1
C262	CAP	47B4
C263	CAP	14C2
C264	CAP	11C4
C265	CAP	47B3
C266	CAP	47B8
C267	CAP	44D6
C269	CAP_P	51D6
C270	CAP	47A5
C271	CAP	11C8
C272	CAP	27D4
C273	CAP	47C5
C275	CAP	14C2
C276	CAP	14C2
C277	CAP	11C8
C278	CAP	11C6
C279	CAP	11C5
C280	CAP	11C6
C281	CAP	11C6
C282	CAP	47B6
C283	CAP	47C7
C284	CAP	47B4
C285	CAP	47B7
C286	CAP	47B7
C287	CAP	50A2
C288	CAP	11D8
C289	CAP	11D8
C290	CAP	11D8
C291	CAP	11D8
C292	CAP	11D4
C293	CAP	50A1
C294	CAP	50A1
C295	CAP_P	50C5
C296	CAP_P	47B3
C297	CAP	47C4
C298	CAP	47C5
C299	CAP	47C4
C300	CAP_P	47C3
C301	CAP_P	47C4
C302	CAP_P	50A2
C303	CAP	50C2
C304	CAP	14C2
C305	CAP	47C4
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C307	CAP_P	50A2
C308	CAP_P	50A3
C309	CAP_P	50A3
C310	CAP_P	50A2
C311	CAP	14C1
C312	CAP	29D3
C313	CAP	14C3
C314	CAP	29D3
C315	CAP	50A8
C316	CAP	50A8
C317	CAP	50B8
C318	CAP	50B8
C319	CAP	14A7
C320	CAP	14C2
C321	CAP	50B7
C322	CAP	50A7
C323	CAP_P	49B2
C324	CAP_P	49B2
C325	CAP	27D4
C326	CAP_P	50B2
C327	CAP_P	50B2
C328	CAP_P	50B2
C329	CAP	49B3
C330	CAP_P	49B2
C331	CAP_P	49B2
C332	CAP_P	49B2
C333	CAP	50B6
C334	CAP_P	45C1
C335	CAP_P	45C2
C336	CAP_P	45C2
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C1502	CAP	15D1	
C1503	CAP	15D1	
C1504	CAP	15D3	
C1505	CAP	15D3	
C1506	CAP	15D3	
C1507	CAP	15D2	
C1508	CAP	15D2	
C1509	CAP	15D2	
C1510	CAP	15D1	
C1511	CAP	15D1	
C1512	CAP	15D1	
C1513	CAP	15D1	
C1514	CAP	15C3	
C1515	CAP	15C3	
C1601	CAP	14D7	
C1602	CAP	14D3	
C1702	CAP	15D7	
C1801	CAP	16D5	
C1802	CAP	16A7	
C1901	CAP	8A7	
C1902	CAP	8A6	

C1903	CAP	8A6	
C1904	CAP	8A6	
C1910	CAP	8A6	
C1911	CAP	8C2	
C1912	CAP	8C1	
C1913	CAP	8C1	
C1914	CAP	8C1	
C2201	CAP	20C8	
C2202	CAP	20C4	
C2301	CAP	21C8	
C2302	CAP	21C4	
C2501	CAP_P	23A8	
C3001	CAP	28C5	
C3002	CAP	28D5	
C3003	CAP	28D5	
C3004	CAP	28D4	
C3005	CAP	28D4	
C3201	CAP	30D4	
C3501	CAP	35D6	
C3502	CAP	33A8	
C3901	CAP	37D1	
C4081	CAP	46C7	
C4201	CAP	42B6	
C4261	CAP	42A7	
C4262	CAP	42A7	
C4265	CAP	42A7	
C4267	CAP	42A6	
C4301	CAP	41A6	
C4302	CAP	43A5	
C4303	CAP	43A4	
C4502	CAP_P	43B5	
C4504	CAP	45B3	
C4509	CAP	45C4	
C4701	CAP	45B6	
C4702	CAP	47B4	
C4801	CAP	48B4	
C4901	CAP	49B4	
C5001	CAP	50C3	
C5002	CAP	50A3	
D1	DIODE_DUAL_6P	36A7	
D2	DIODE_DUAL_6P	36A7	
D3	DIODE_DUAL_6P	36A7	
D4	DIODE_DUAL_6P	36B7	
D5	ZENER_MMBZ15VDLT1	40B6	
D6	DIODE_DUAL_6P	25D4	
D7	DIODE_DUAL_6P	25D4	
D8	DIODE	36D6	
D9	DIODE	35B8	
D10	DIODE_SCHOT	23B8	
D11	DIODE_SCHOT	44D7	
D12	DIODE_SCHOT	44D7	
D13	DIODE_SCHOT	47C7	
D14	DIODE_SCHOT	47B5	
D15	DIODE_SCHOT	49B3	
D16	DIODE_SCHOT	50C5	
D17	DIODE_SCHOT	50B5	
D18	DIODE_SCHOT	49C6	
D19	DIODE_SCHOT	46D6	
D20	DIODE_SCHOT	45D5	
D21	DIODE_SCHOT	45B5	
D23	DIODE_SCHOT_3P	42A6	
D24	ZENER_MMBZ15VDLT1	41B2	
D25	ZENER	36B6	
D26	ZENER_MMBZ15VDLT1	41B2	
D27	DIODE_DUAL_6P	25B4	
D28	DIODE_DUAL_6P	25B4	
D29	ZENER_MMBZ15VDLT1	40B5	
D30	DIODE_SCHOT	48C5	
D31	DIODE_SCHOT	48B3	
D32	DIODE_SCHOT	48B5	
D33	DIODE_SCHOT	46B6	
D34	DIODE_SCHOT	48B2	
D35	DIODE_SCHOT	44D6	
D36	DIODE_SCHOT	44D6	
D37	DIODE_SCHOT	50B2	
D38	DIODE_SCHOT	50C6	
D39	DIODE_SCHOT	50B4	
D40	DIODE_SCHOT	50A4	
D41	DIODE_SCHOT	45C4	
D42	DIODE_SCHOT	49B5	
D43	DIODE_SCHOT	45B4	
D44	DIODE_SCHOT	45D2	
D45	DIODE_SCHOT	45D6	
D46	DIODE_SCHOT	49B1	
D47	DIODE	36D6	
D48	DIODE_DUAL_SWI	42B6	
D4901	DIODE_SCHOT	47B2	
DS1	LED	35A2	
DS2	LED	35A1	
DS3	LED	35A1	
DS4	LED	30A3	
DS5	LED	51C8	
DS6	LED	51A6	
DS7	LED	38B2	
DS8	LED	38B6	
DS9	LED	50D5	
DS10	LED	51A4	
DZ1	ZENER	51B1	
F2	FUSE	36D5	
F3	FUSE	36D5	
FL2	FILTER_LC	25C6	
FL3	FILTER_LC	25C6	
FL4	FILTER_LC	25B6	
J1	CON_RJ45	35C1	
J2	CON_FWVERT_SKT	36C1	
J3	CON_F8RT_S_TH1	42B5	
J4	CON_F4RT_USB_UPRIGHT	33C3	
J5	CON_FWVERT_SKT	36D1	
J6	CON_F4RT_USB_UPRIGHT	33B3	
J7	CON_F4RT_USB_UPRIGHT	33D3	

J8	CON_F4RT_S4MT_TH1	41C1	
J9	CON_F14RT_D4MT_TH1	25C5	
J10	CON_F4RT_S4MT_TH1	40C7	
J11	CON_F184ST_DDRDIMM	15D5	
J12	CON_F21ST_D2MT_SM	24C4	
J13	CON_M40SM_635	29D6	
J14	CON_M18ST_D_TH	29B5	
J15	CON_M40ST_NC20	38D6	
J16	CON_M40ST_NC20	38D2	
J17	CON_M16ST_MICROFIT	50D7	
J18	CON_M4ST_LCK	34B4	
J19	CON_37SM_MTOR	8C4	
J20	CON_38SM_MTOR	8D7	
J21	CON_M3ST_LCK	45C8	
J22	CON_F20SM_KX	8A4	
J23	CON_F1ST_S2MT_SM	28B7	
J24	CON_M12ST_SM	29B3	
J25	CON_F100RT_LP_SM	31D3	
J26	CON_F200RT_DDRDIMM_SM2	14D5	
J27	CON_F1ST_S2MT_SM	8B1	
J28	CON_F10ST_D_SMA	29D2	
J30	CON_38SM_MTOR	8D4	
J31	CON_38SM_MTOR	8C7	
J32	CON_F12RT_S2MT_SM	8A8	
J4501	CON_F4ST_S2MT_SM	43B6	
J4502	CON_F4ST_S2MT_SM	43B6	
JAZ1	TP	51A5	
L1	IND	36D4	
L2	IND	33A5	
L3	IND	36D4	
L4	IND	27D5	
L5	FILTER_4P	36C2	
L6	FILTER_4P	36C2	
L7	FILTER_4P	36D2	
L8	FILTER_4P	36D2	
L9	IND	25C2	
L12	IND	48B3	
L13	IND	22D7	
L16	IND	28C3	
L19	IND	47B4	
L20	IND	45C3	
L21	IND_3P	49B3	
L22	IND_3P	50A3	
L23	IND	50C3	
L24	IND	45B3	
L26	IND	42A6	
L27	IND	41C3	
L32	IND	36B6	
L33	IND	22B7	
L34	IND	41D3	
L35	IND	41B3	
L36	IND	40B6	
L39	IND	41A3	
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L44	IND	41C3	
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L60	IND	43B5	
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L92	IND	42C7	
L93	IND	42C3	
L94	IND	42C2	
L95	IND	42D2	
L96	IND	42C3	
L97	IND	43D7	
L98	IND	43D7	
L99	IND	42B3	
L100	FILTER_4P	33D5	

L101	FILTER_4P	33C5	
L102	FILTER_4P	33B5	
L103	IND	29B3	
L2401	IND	22C7	
L2501	IND	23A6	
LP1	LPAK4P	42A8	
Q1	TRA_2N7002	51C3	
Q2	TRA_2N7002	42D7	
Q3	TRA_2N7002	42C7	
Q4	TRA_2N7002	42B8	
Q5	TRA_2N7002	41A5	
Q6	TRA_2N7002	42B6	
Q7	TRA_SUD70N03	48B4	
Q8	TRA_SUD50N03	48B4	
Q9	TRA_SUD50N03	48C4	
Q10	TRA_2N7002	22B7	
Q11	TRA_FDC602P	51C2	
Q12	TRA_2N3904	44D7	
Q13	TRA_2N7002	51B2	
Q14	TRA_2N7002	51C7	
Q15	TRA_2N7002	51A7	
Q16	TRA_2N7002	51A7	
Q17	TRA_2N7002	51B6	
Q18	TRA_2N7002	51A7	
Q19	TRA_2N7002	51A6	
Q20	TRA_FDC602P	51D7	
Q21	TRA_2N7002	50C1	
Q22	TRA_2N7002	50D1	
Q23	TRA_2N7002	50C2	
Q24	TRA_2N7002	50C2	
Q25	TRA_IRF7807Z	47B5	
Q26	TRA_IRF7807Z	47B5	
Q27	TRA_SUD70N03	49B4	
Q28	TRA_SUD50N03	49B4	
Q29	TRA_2N7002	45D8	
Q30	TRA_2N3904	36C7	
Q31	TRA_2N7002	41A8	
Q32	TRA_2N7002	39C7	
Q33	TRA_2N3904	43A2	
Q34	TRA_SUD70N03	48B4	
Q35	TRA_2N7002	40D4	
Q36	TRA_2N7002	42D3	
Q37	TRA_FDC602P	51C6	
Q38	TRA_2N7002	51B6	
Q39	TRA_2N3904	50C7	
Q40	TRA_SUD70N03	45C4	
Q41	TRA_2N7002	15B2	
Q42	TRA_2N7002	15C2	
Q43	TRA_SUD70N03	45C4	
Q44	TRA_SUD50N03	45C4	
Q45	TRA_IRF7807Z	50B4	
Q46	TRA_IRF7807Z	50C4	
Q47	TRA_SUD50N03	50A4	
Q48	TRA_SUD50N03	50A4	
Q49	TRA_SUD70N03	45B4	
Q50	TRA_SUD50N03	45B4	
Q51	TRA_SUD50N03	45B4	
Q52	TRA_SUD70N03	45B4	
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Q54	TRA_2N7002	15B2	
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RP60	RPAK4P	28C2
RP61	RPAK4P	31B7
RP62	RPAK4P	12C3
RP63	RPAK4P	30B8
RP64	RPAK4P	31B7
RP65	RPAK4P	34C4
RP66	RPAK4P	28A8
RP67	RPAK4P	31B7
RP68	RPAK4P	12D3
RP69	RPAK4P	30B8
RP70	RPAK4P	34C7
RP71	RPAK4P	12C2 12D2
RP72	RPAK4P	31C7
RP73	RPAK4P	31C7
RP74	RPAK4P	28A8
RP75	RPAK4P	31C7
RP76	RPAK4P	34C7
RP77	RPAK4P	31C7
RP78	RPAK4P	7A7
RP79	RPAK4P	7A5 7C5
RP80	RPAK4P	19B7
RP81	RPAK4P	19B7
RP82	RPAK4P	19B7 19C7 19C7
RP83	RPAK4P	18B2 18B3 18B3
RP84	RPAK4P	18B2 18B2 18B3
RP85	RPAK4P	18B3 18C2 18C3
RP86	RPAK4P	19B5
RP87	RPAK4P	19B5
RP88	RPAK4P	19C5
RP89	RPAK4P	19C5
RP90	RPAK4P	19C7
RP91	RPAK4P	19C7 19D7
RP92	RPAK4P	19C7
RP93	RPAK4P	18E2 18E3
RP94	RPAK4P	18F2 18F3
RP95	RPAK4P	18F2 18F2 18F3
RP96	RPAK4P	19C5
RP97	RPAK4P	19D5
RP98	RPAK4P	16B3 16C3 16C3
RP99	RPAK4P	16C1
RP100	RPAK4P	28A8
RP101	RPAK4P	34B1
RP102	RPAK4P	12C5
RP103	RPAK4P	37B2 37C2
RP104	RPAK4P	37B4 37B5 37C5
RP105	RPAK4P	12B5
RP106	RPAK4P	37B2
RP107	RPAK4P	37B4 37B4 37B5
RP108	RPAK4P	28A3 28B3
RP109	RPAK4P	12A5
RP110	RPAK4P	28A8
RP111	RPAK4P	37C4 37C4 37C5 37C5
RP112	RPAK4P	34C4
RP113	RPAK4P	28B8
RP114	RPAK4P	37A2 37B2
RP115	RPAK4P	37A4 37A5 37B4 37B5
RP116	RPAK4P	12B3

RP117	RPAK4P	28C1 28C1 28D1 28D1
RP118	RPAK4P	37C2
RP119	RPAK4P	34C1
S1	SWI_TACT_2P1	44B2
S2	SWI_TACT	44A3
SP1	SPRING_CLIP_1P_EMI	10D2
SP2	SPRING_CLIP_1P_EMI	10D2
SP3	SPRING_CLIP_1P_EMI	10D1
SP4	SPRING_CLIP_1P_EMI	10D1
T1	XFR_100BT_MDIX	35C3
U1	SIL1162	27C3
U2	SHNTREG_TLV431A	21A4
U3	VREG_LP2951	36D7
U4	FW802A	36C5
U5	SDRAM_DDR_4MX32	21D6 21D7
U6	OPAMP_TLV2362	40B3 40C3
U7	SHNTREG_TLV431A	18B8
U8	AMP_TPA6112A2	41D5
U9	CLK_GEN_CY25811	22A7
U10	NC7WZ08	42C7
U11	UPD720101_FBGA	32C5
U12	SDRAM_DDR_4MX32	20D6 20D7
U13	OPAMP_TLV2362	43A3
U14	VREG_LP2951	39D6
U15	TAS3004	39C3
U16	SHNTREG_TLV431A	20A5
U18	CBTV4020	13D7
U19	VREG_LT1962	28D7
U20	VREG_LM1117	23A8
U21	VDET_MC33465N_22ATR	44A4
U22	CBTV4020	13B6
U23	MAX6328	44A5
U25	INTREPID	9D2 10D5 10D7 12D7 16D5 28C4 30D5 34C5 37D8
U26	M16C62	44C5
U27	CBTV4020	13D4
U28	VREG_TL431	44D8
U29	CBTV4020	13C2
U31	DCDC_SC2602	47B6
U33	LTC3707	50B6
U34	APOLLO_MPC7445_360	4C5 5D3 5D6
U35	TRA_SI4435DY	51D3
U36	SDRAM_DDR_4MX32	21D2 21D3
U37	TRANSCEIVER_BCM5221	35C5
U38	SN74AUC1G04	30B3
U39	NV18B	17D6 18G5 18G7 22D4 23D4
U40	DCDC_SC2602	48C6
U41	SDRAM_DDR_4MX32	20D2 20D3
U42	FEPR_1MX8	30C2
U45	DCDC_SC2602	49C5
U46	SN74LVC1G04	44D1
U47	LTC3707	45C6
U48	NC7WZ08	41A7 43C7
U49	AMP_SN02100045A	42D5
U3501	SWI_TPS2023	33A7
VR1	VREG_LM1117	39C7
VR2	VREG_MIC39102	46B6
VR3	VREG_EZ1582	51B4
VR4	VREG_MIC39102	46C5
XW1	SHORT	39B7
XW2	SHORT8L25_WITH_ALTS	48B2
XW4	SHORT	39B7
XW5	SHORT	39B7
XW6	SHORT8L25_WITH_ALTS	48B4
XW7	SHORT8L25_WITH_ALTS	48C7
XW12	SHORT8L25_WITH_ALTS	47B3
XW13	SHORT8L25_WITH_ALTS	47B4
XW14	SHORT8L25_WITH_ALTS	47C5
XW15	SHORT8L25_WITH_ALTS	47A6
XW16	SHORT8L25_WITH_ALTS	50A3
XW17	SHORT8L25_WITH_ALTS	50B8
XW18	SHORT8L25_WITH_ALTS	50A3
XW19	SHORT8L25_WITH_ALTS	50B2
XW20	SHORT8L25_WITH_ALTS	50B3
XW21	SHORT8L25_WITH_ALTS	50A6
XW22	SHORT8L25_WITH_ALTS	50B5
XW23	SHORT8L25_WITH_ALTS	49B2
XW24	SHORT8L25_WITH_ALTS	49C4
XW25	SHORT8L25_WITH_ALTS	49C4
XW26	SHORT8L25_WITH_ALTS	45C3
XW27	SHORT8L25_WITH_ALTS	45C3
XW28	SHORT8L25_WITH_ALTS	45B1
XW29	SHORT8L25_WITH_ALTS	45C6
XW30	SHORT8L25_WITH_ALTS	45A3
XW31	SHORT8L25_WITH_ALTS	45B3
XW32	SHORT	39B7
XW33	SHORT	41B7
XW34	SHORT	39A7
XW37	SHORT	39B7
XW38	SHORT	39A7
XW39	SHORT8L25_WITH_ALTS	48B5
XW41	SHORT8L25_WITH_ALTS	49B5
XW42	SHORT	28A5
XW43	SHORT	28A5
XW44	SHORT	28A5
XW45	SHORT	28A4
XW46	SHORT	28A4
XW47	SHORT	9A2
XW48	SHORT	16A5
XW49	SHORT	30B5
Y1	CRYSTAL	36C6
Y2	CRYSTAL_4PIN	22B3
Y3	CRYSTAL	44A6
Y4	CRYSTAL_4PIN	44B2
Y5	CRYSTAL	28A6
Y6	CRYSTAL	35B7
Y7	CRYSTAL	32D3
ZH3	MTGHOLE	39A7
ZH4	MTGHOLE	4B2
ZH5	SLOT	4B1

ZH6	SLOT	4B2
ZH7	MTGHOLE	4B1
ZT1	HOLE_VIA	18C2
ZT2	HOLE_VIA	18C2
ZT3	HOLE_VIA	18C2
ZT4	HOLE_VIA	18A2
ZT5	HOLE_VIA	18C2
ZT6	HOLE_VIA	18C2
ZT7	HOLE_VIA	18A2
ZT8	HOLE_VIA	18C2
ZT9	HOLE_VIA	18B2
ZT10	HOLE_VIA	18B2
ZT11	HOLE_VIA	18B2
ZT12	HOLE_VIA	18B2
ZT13	HOLE_VIA	18B2
ZT14	HOLE_VIA	18B2
ZT15	HOLE_VIA	18B2
ZT16	HOLE_VIA	18B2
ZT17	HOLE_VIA	18B2
ZT18	HOLE_VIA	18B2
ZT19	HOLE_VIA	18A2
ZT20	HOLE_VIA	18G2
ZT21	HOLE_VIA	18E2
ZT22	HOLE_VIA	18F2
ZT23	HOLE_VIA	18F2
ZT24	HOLE_VIA	18F2
ZT25	HOLE_VIA	18F2
ZT26	HOLE_VIA	18F2
ZT27	HOLE_VIA	18E2
ZT28	HOLE_VIA	18D2
ZT29	HOLE_VIA	18G2
ZT30	HOLE_VIA	18F2
ZT31	HOLE_VIA	18F2
ZT32	HOLE_VIA	18E2
ZT33	HOLE_VIA	18E2
ZT34	HOLE_VIA	18F2
ZT35	HOLE_VIA	18E2
ZT36	HOLE_VIA	18E2
ZT37	HOLE_VIA	18F2
ZT38	HOLE_VIA	18E2
ZT39	HOLE_VIA	3B3
ZT40	HOLE_VIA	3B3
ZT41	HOLE_VIA	3B3
ZT42	HOLE_VIA	3B3
ZT43	HOLE_VIA	3A3
ZT44	HOLE_VIA	3A3
ZT45	HOLE_VIA	3A3
ZT46	HOLE_VIA	3B3
ZT47	HOLE_VIA	3B3
ZT48	HOLE_VIA	3B3
ZT49	HOLE_VIA	3B3
ZT50	HOLE_VIA	3A3
ZT51	HOLE_VIA	3A3
ZT52	HOLE_VIA	3A3
ZT53	HOLE_VIA	3B2
ZT54	HOLE_VIA	3B2
ZT55	HOLE_VIA	3B2
ZT56	HOLE_VIA	3B2
ZT57	HOLE_VIA	3A2
ZT58	HOLE_VIA	3A2
ZT59	HOLE_VIA	3B2
ZT60	HOLE_VIA	3B2
ZT61	HOLE_VIA	3B2
ZT62	HOLE_VIA	3B2
ZT63	HOLE_VIA	3A2
ZT64	HOLE_VIA	3B1
ZT65	HOLE_VIA	3B1
ZT66	HOLE_VIA	3B1
ZT67	HOLE_VIA	3B1
ZT68	HOLE_VIA	3A1

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