

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

|         |  |     |      |        |                       |          |          |
|---------|--|-----|------|--------|-----------------------|----------|----------|
| DRAWING |  | REV | ZONE | ECN    | DESCRIPTION OF CHANGE | CK APPD  | ENG APPD |
|         |  |     |      |        |                       | DATE     | DATE     |
|         |  | C   |      | 329994 | PRODUCTION RELEASED   | 05/27/04 |          |

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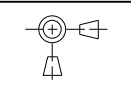
# SCHEM, MLB, PB15

Thu May 27 14:58:03 2004

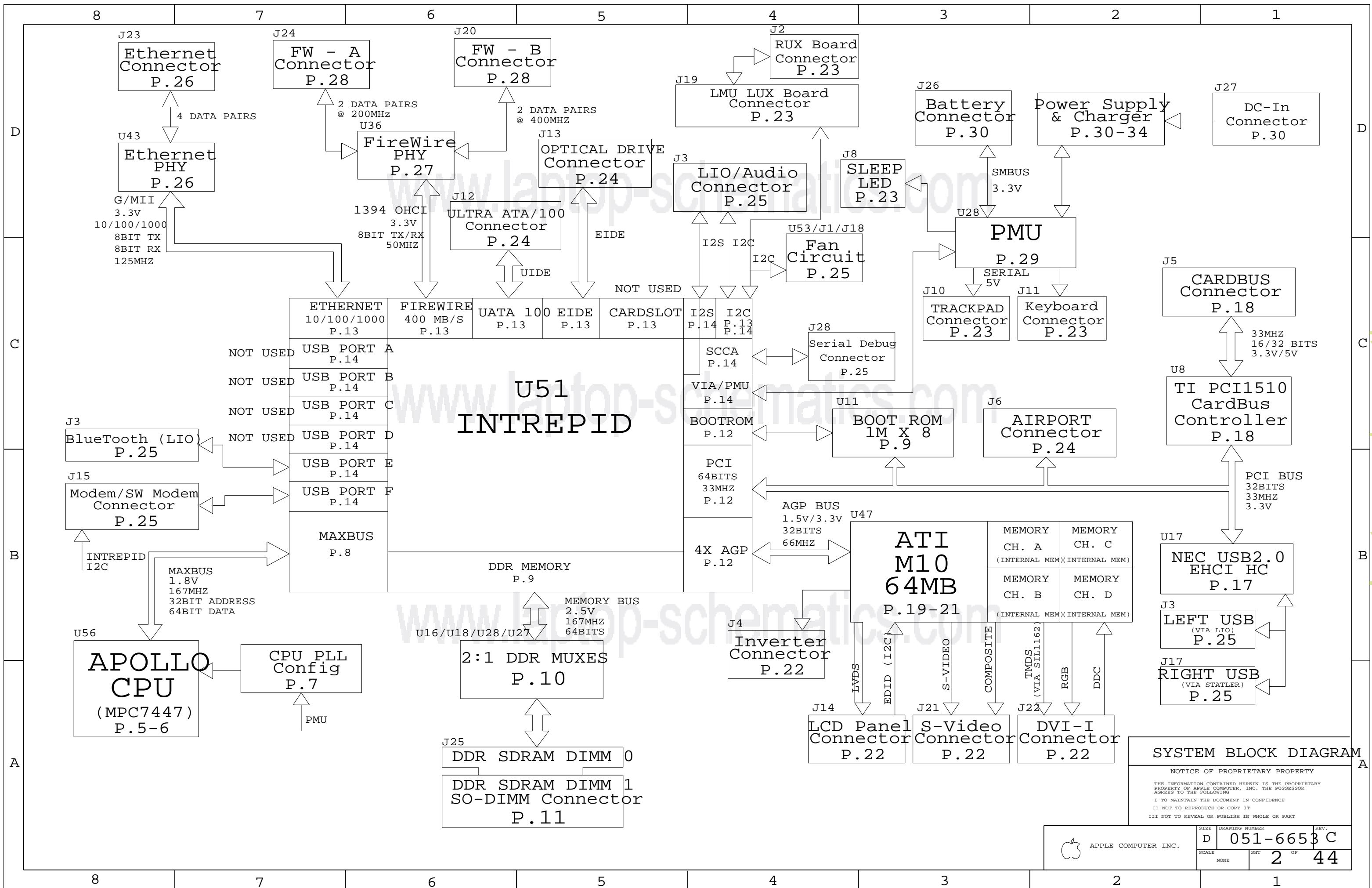
### BOM OPTIONS (IN COMMON PARTS)

| STUFF          | NO STUFF     |
|----------------|--------------|
| 1_8V_MAXBUS    | 1_5V_MAXBUS  |
| NO_SSCG        | SSCG         |
| 5V_HD_LOGIC    | 3V_HD_LOGIC  |
| NO_BBANG       | BBANG        |
| INT_2_5V_COLD  | INT_2_5V_HOT |
| ATI_MEMIO_HI   | ATI_MEMIO_LO |
| SOFT_MODEM     | USB_MODEM    |
| GPU_PWRMSR     | EXT_TMDS     |
| GPU_SS         |              |
| VGA_BUFFER_RES |              |
| INT_TMDS       |              |

| PART#    | QTY | DESCRIPTION    | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|----------------|-------------------------|------------|
| 051-6653 | 1   | SCHEM,MLB,PB15 | SCH1                    |            |
| B20-1600 | 1   | PCBF,MLB,PB15  | PCB1                    |            |

|   |  |                                     |           |   |                         |
|---|--|-------------------------------------|-----------|---|-------------------------|
| DIMENSIONS ARE IN MILLIMETERS   |  | METRIC                              |           | Apple Computer Inc.   |                         |
| xx : _____  |  | DRAPTR                              | DESIGN CK | NOTICE OF PROPRIETARY PROPERTY<br>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:<br>I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE<br>II. NOT TO REPRODUCE OR COPY IT<br>III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART |                         |
| x.xx : _____  |  | ENG APPD                            | MFG APPD  |   |                         |
| x.xxx : _____   |  | QA APPD                             | DESIGNER  |   |                         |
| ANGLES : _____  |  | RELEASE                             | SCALE     |   |                         |
| DO NOT SCALE DRAWING  |  | SCALE NONE                          |           | TITLE   |                         |
| <br>THIRD ANGLE PROJECTION |  | MATERIAL/FINISH NOTED AS APPLICABLE |           | SIZE D  | DRAWING NUMBER 051-6653 |
|   |  |                                     |           | REV. C  | SHT 1 OF 44             |

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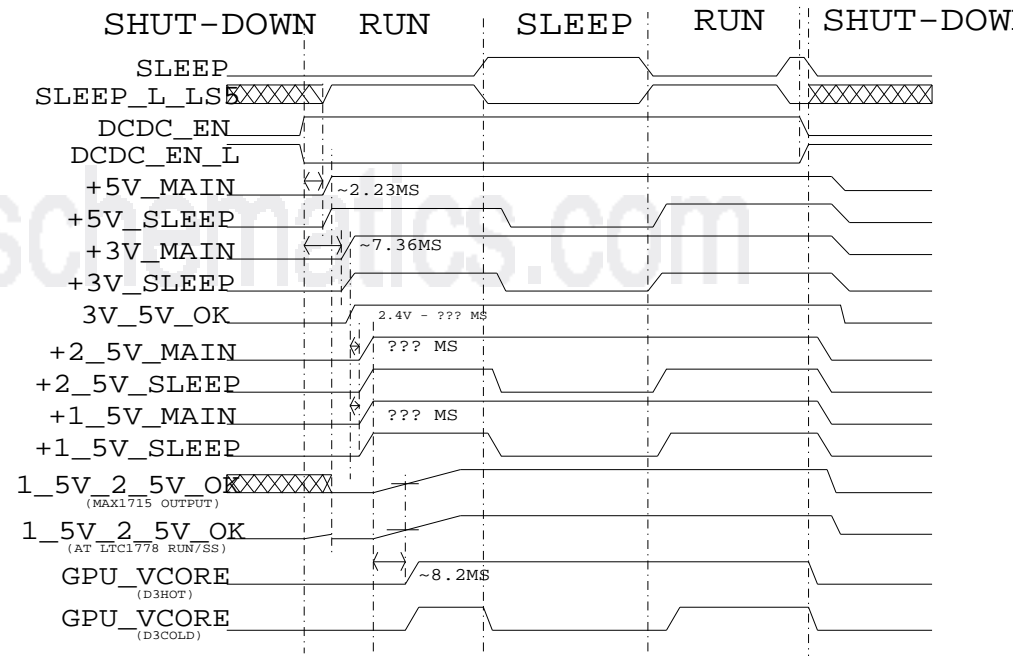
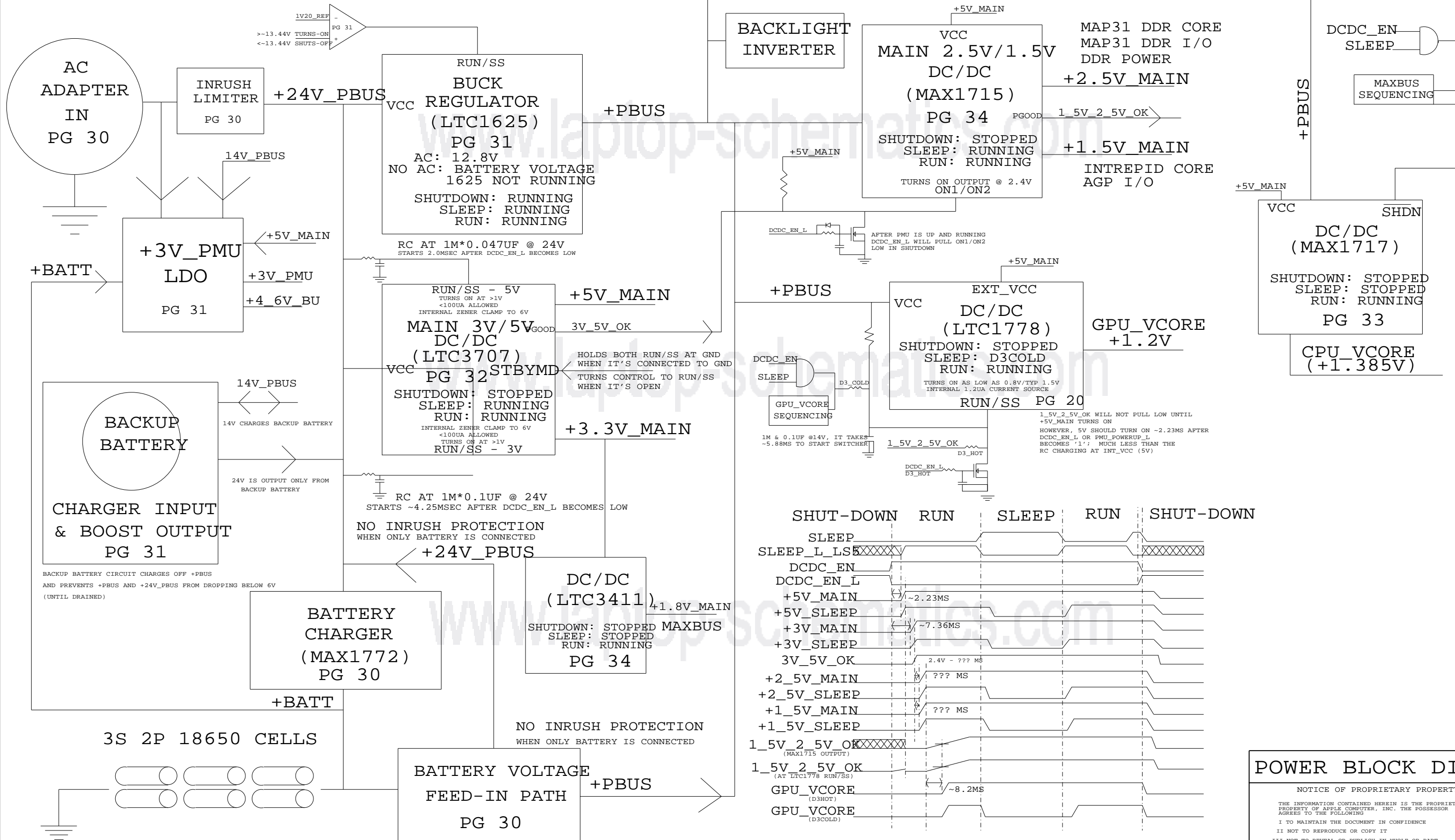


**SYSTEM BLOCK DIAGRAM**

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# POWER SYSTEM ARCHITECTURE



**POWER BLOCK DIAGRAM**

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# PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
 1/2 OZ CU THICKNESS: 0.7 MILS  
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
 DIELECTRIC: FR-4  
 LAYER COUNT: 10  
 SIGNAL TRACE WIDTH: 4 MILS  
 SIGNAL TRACE SPACING: 4 MILS  
 PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

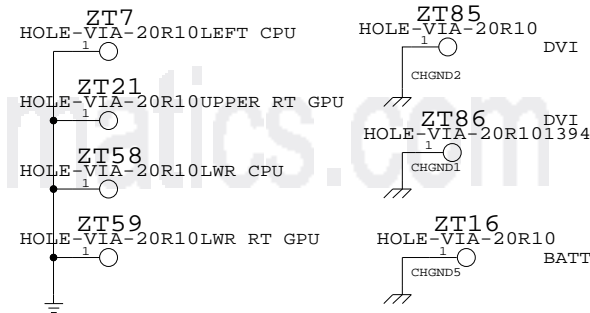
## BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

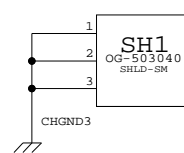
| Layer | Material | Thickness               | Notes                            |
|-------|----------|-------------------------|----------------------------------|
| 1     | SIGNAL   | 1/2 OZ + COPPER PLATING |                                  |
| 2     | PREPREG  | 3 MIL                   | SIGNAL (1/2 OZ)                  |
| 3     | PREPREG  | 3 MIL                   | GROUND (1/2 OZ)                  |
| 4     | CORE     | 3 MIL                   | SIGNAL (1/2 OZ)                  |
| 5     | PREPREG  | 5 MIL                   | CUT POWER PLANE (1 OZ)           |
| 6     | CORE     | 5 MIL                   | CUT POWER PLANE (1 OZ)           |
| 7     | PREPREG  | 5 MIL                   | SIGNAL (1/2 OZ)                  |
| 8     | CORE     | 3 MIL                   | GROUND (1/2 OZ)                  |
| 9     | PREPREG  | 3 MIL                   | SIGNAL (1/2 OZ)                  |
| 10    | PREPREG  | 3 MIL                   | SIGNAL (1/2 OZ + COPPER PLATING) |

## BOARD HOLES CHASSIS MOUNTS

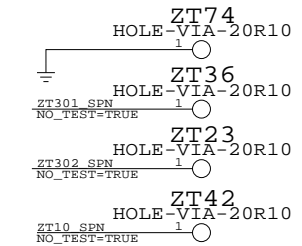
### ASICS HEATSINK MOUNTS I/O AREA



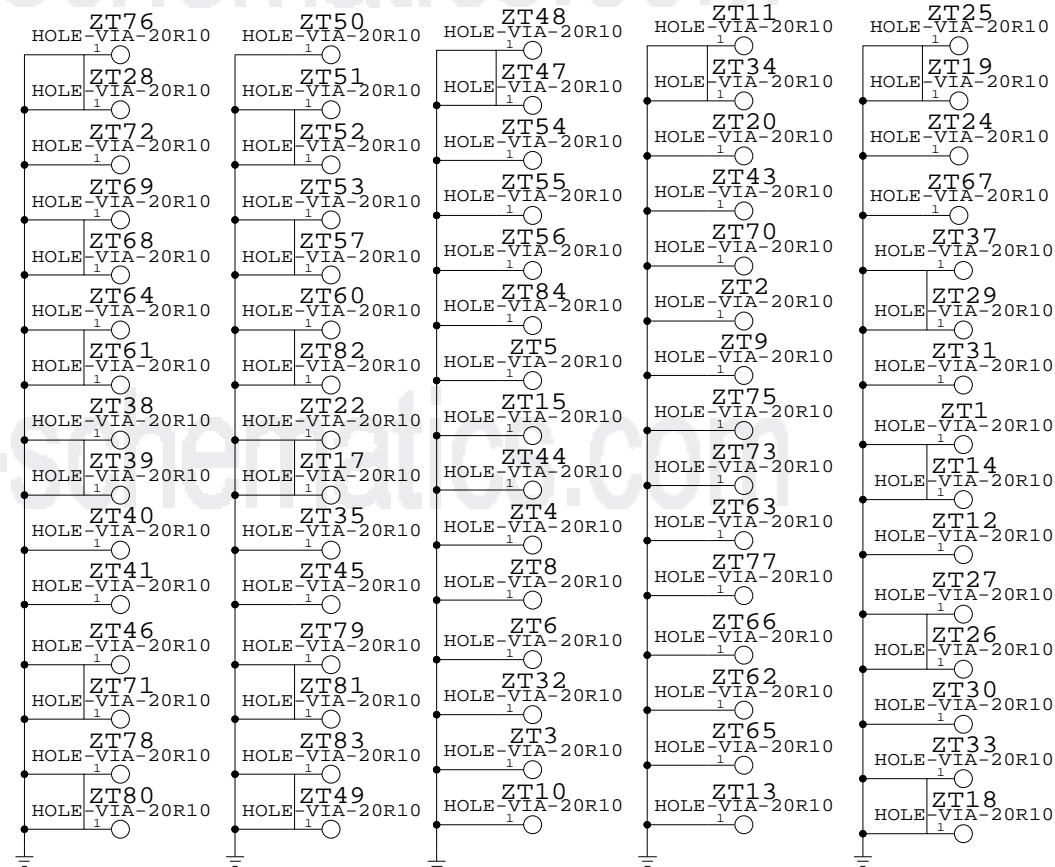
### INVERTER



### MECH. HOLES



## GROUND VIAS

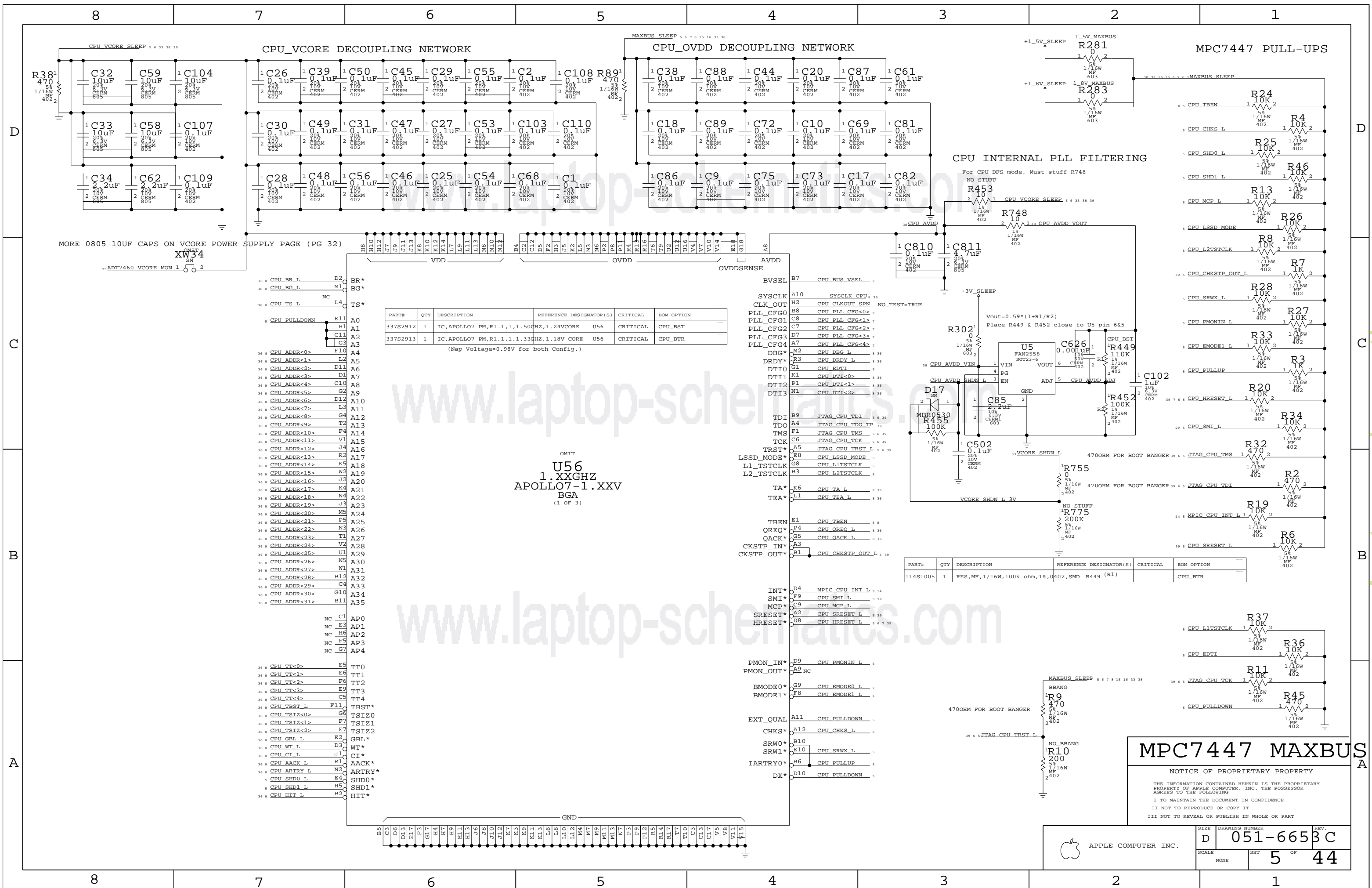


## BOARD INFORMATION

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|                     | SCALE | NONE | SHT            | 4        | OF   | 44 |

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**U56**  
**1.XXGHZ**  
**APOLLO7-1.XXV**  
 BGA  
 (1 OF 3)

| PART#    | QTY | DESCRIPTION                                     | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---|-------------------------|----------|------------|
| 337S2912 | 1   | IC, APOLLO7 FM, R1.1.1, 1.50GHZ, 1.24VCORE U56  |                         | CRITICAL | CPU_BST    |
| 337S2913 | 1   | IC, APOLLO7 FM, R1.1.1, 1.33GHZ, 1.18V CORE U56 |                         | CRITICAL | CPU_BTR    |

(Nap Voltage=0.98V for both Config.)

| PART#    | QTY | DESCRIPTION                                       | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---|-------------------------|----------|------------|
| 114S1005 | 1   | RES, MF, 1/16W, 100k ohm, 1%, 0402, SMD R449 (R1) |                         |          | CPU_BTR    |

### MPC7447 MAXBUS

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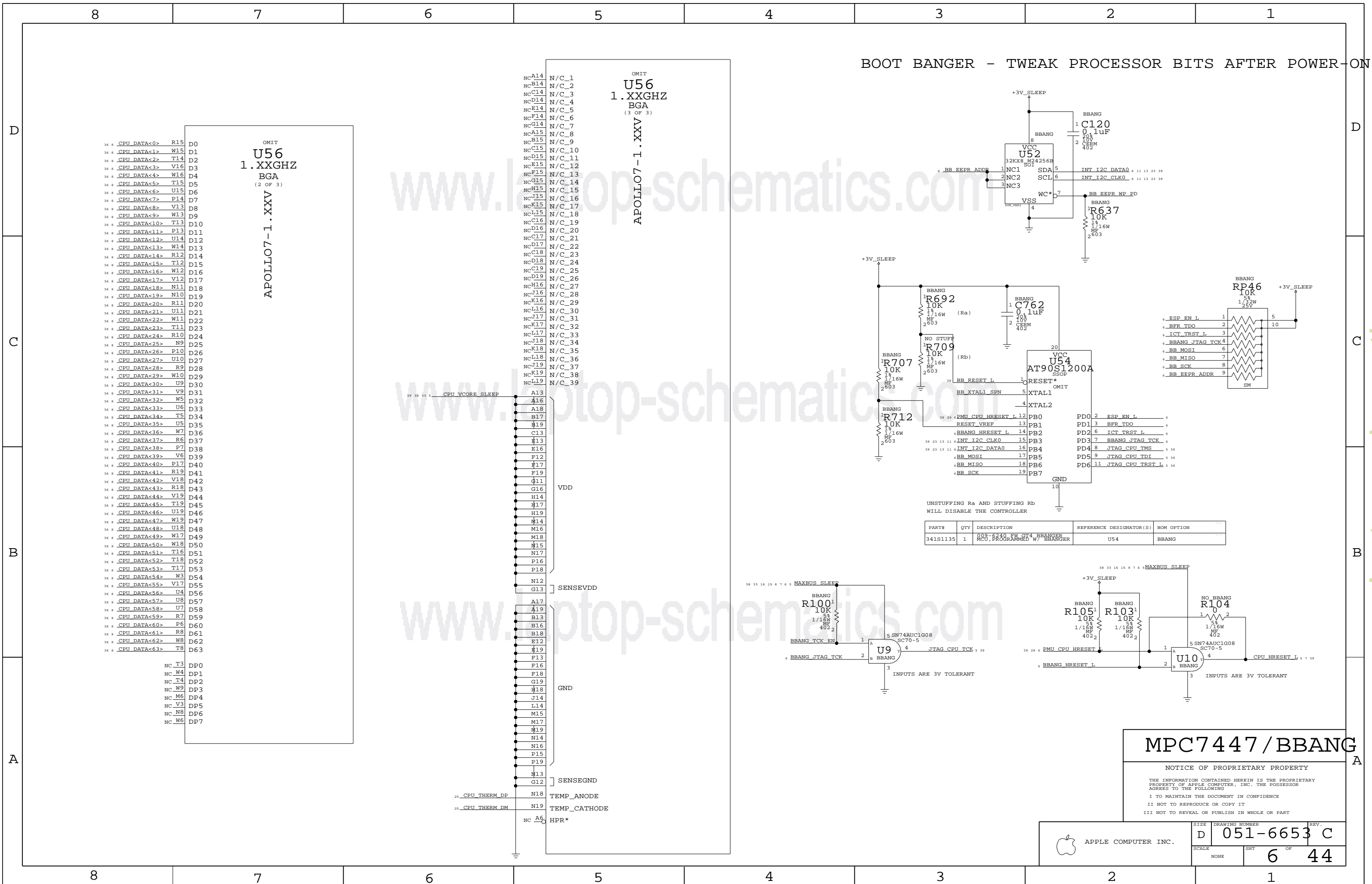
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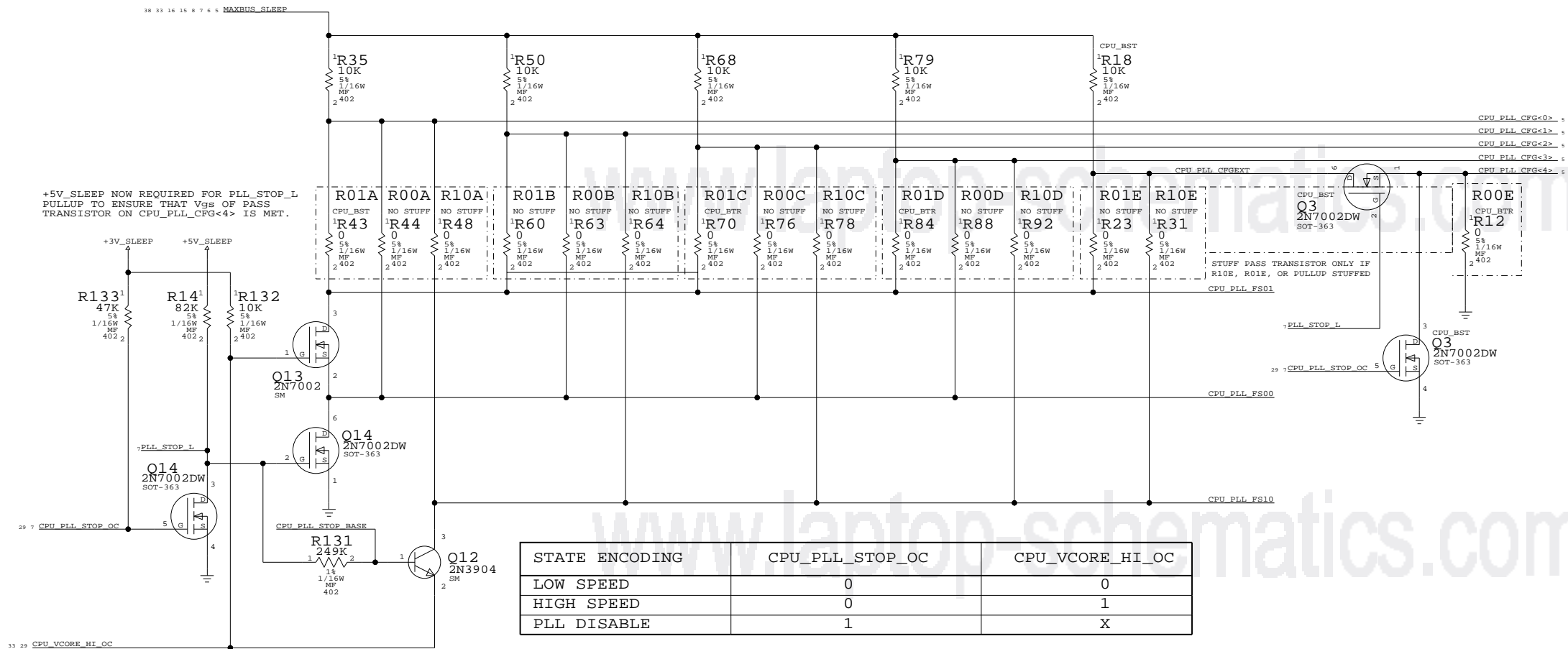
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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|-------------------------|------|----------------|------|
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| NONE                    | 5    | 44             |      |



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### CPU PLL CONFIG CIRCUITRY



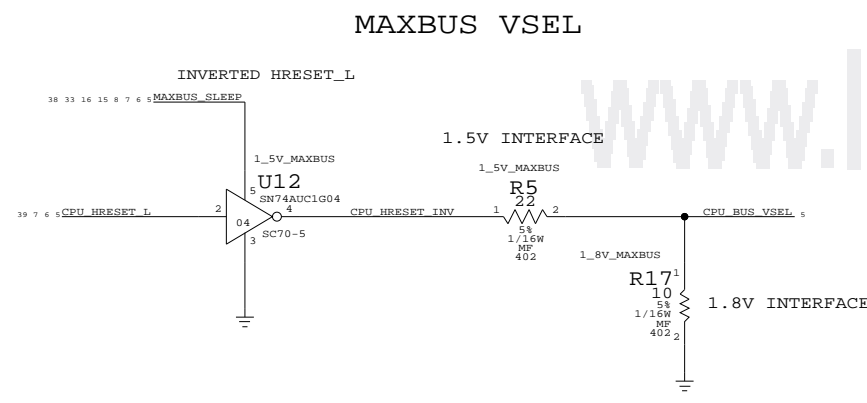
| STATE ENCODING | CPU_PLL_STOP_OC | CPU_VCORE_HI_OC |
|----------------|-----------------|-----------------|
| LOW SPEED      | 0               | 0               |
| HIGH SPEED     | 0               | 1               |
| PLL DISABLE    | 1               | X               |

### CPU FREQUENCY CONFIGURATION

APOLLO 7

| MULTIPLIER<br>(Bus-to-Core) | CORE FREQUENCY<br>(AT BUS FREQUENCY) |        | CPU_PLL_CFG |                  |
|-----------------------------|--------------------------------------|--------|-------------|------------------|
|                             | 167MHZ                               | 133MHZ | 4<br>E      | 0123<br>ABCD HEX |
| 0.0X                        | PLL OFF                              |        | 0           | 1111 0F          |
| 1.0X                        | PLL BYPASS                           |        | 0           | 0011 03          |
| 2.0X                        | 333                                  | 267    | 0           | 0100 04          |
| 3.0X                        | 500                                  | 400    | 0           | 1000 08          |
| 4.0X                        | 667                                  | 533    | 0           | 1010 0A          |
| 5.0X                        | 833                                  | 667    | 0           | 1011 0B          |
| 5.5X                        | 917                                  | 733    | 0           | 1001 09          |
| 6.0X                        | 1000                                 | 800    | 0           | 1101 0D          |
| 6.5X                        | 1083                                 | 867    | 0           | 0101 05          |
| 7.0X                        | 1167                                 | 933    | 0           | 0010 02          |
| 7.5X                        | 1250                                 | 1000   | 0           | 0001 01          |
| 8.0X                        | 1333                                 | 1067   | 0           | 1100 0C          |
| 8.5X                        | 1417                                 | 1133   | 0           | 0110 06          |
| 9.0X                        | 1500                                 | 1200   | 1           | 0111 17          |
| 9.5X                        | 1583                                 | 1267   | 0           | 0111 07          |
| 10.0X                       | 1667                                 | 1333   | 1           | 1010 1A          |
| 10.5X                       | 1750                                 | 1400   | 1           | 1000 18          |
| 11.0X                       | 1833                                 | 1467   | 1           | 1001 19          |
| 11.5X                       | 1917                                 | 1533   | 0           | 0000 00          |
| 12.0X                       | 2000                                 | 1600   | 1           | 1011 1B          |
| 12.5X                       | 2083                                 | 1667   | 1           | 1111 1F          |
| 13.0X                       | 2167                                 | 1733   | 1           | 0101 15          |
| 13.5X                       | 2250                                 | 1800   | 0           | 1110 0E          |
| 14.0X                       | 2333                                 | 1867   | 1           | 1100 1C          |
| 15.0X                       | 2500                                 | 2000   | 1           | 0001 11          |
| 16.0X                       | 2667                                 | 2133   | 1           | 1101 1D          |
| 17.0X                       | 2833                                 | 2267   | 1           | 0000 10          |
| 18.0X                       | 3000                                 | 2400   | 1           | 0010 12          |
| 20.0X                       | 3333                                 | 2667   | 1           | 0011 13          |
| 21.0X                       | 3500                                 | 2800   | 1           | 0100 14          |
| 24.0X                       | 4000                                 | 3200   | 1           | 0110 16          |
| 28.0X                       | 4667                                 | 3733   | 1           | 1110 1E          |

### CPU CONFIGURATION



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET\_L  
NEED TO CHARACTERIZE

| SIGNAL                   | TIED           | APPLICATION    |
|--------------------------|----------------|----------------|
| CPU_EMODE0_L (PROCESSOR) | HIGH           | 60X BUS MODE   |
|                          | CPU_HRESET_L   | MAX BUS MODE   |
| CPU_BUS_VSEL (PROCESSOR) | CPU_HRESET_L   | 2.5V INTERFACE |
|                          | LOW            | 1.8V INTERFACE |
|                          | CPU_HRESET_INV | 1.5V INTERFACE |

### CPU CONFIGURATION

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| SCALE | SHT            | 7 OF 44 |
| NONE  |                |         |

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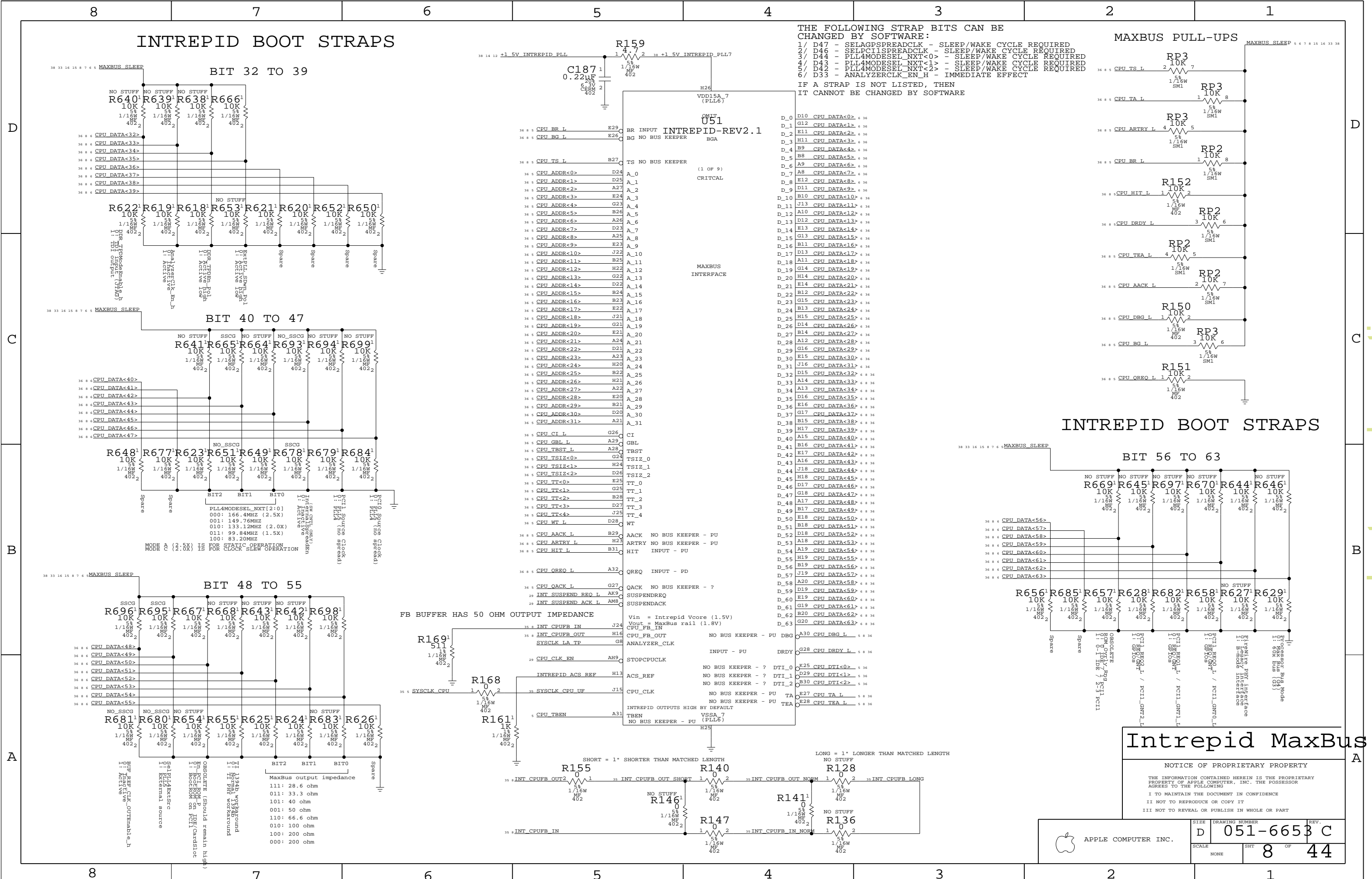
# INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

- 1/ D47 - SELAGPSREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D45 - PLL4MODESEL\_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL\_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL\_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL\_NXT<3> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK\_EN\_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

# MAXBUS PULL-UPS



# INTREPID BOOT STRAPS

# Intrepid MaxBus

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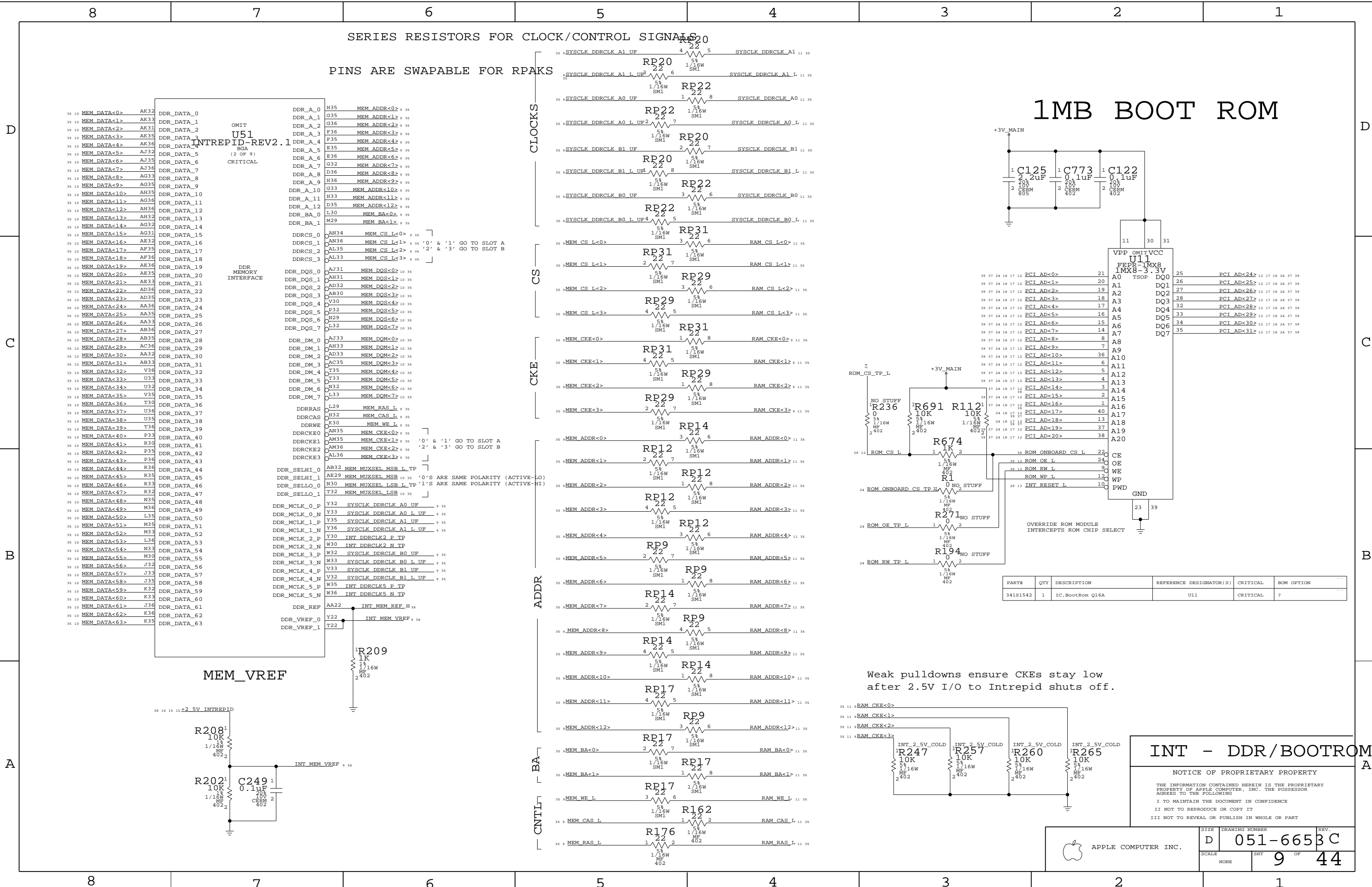
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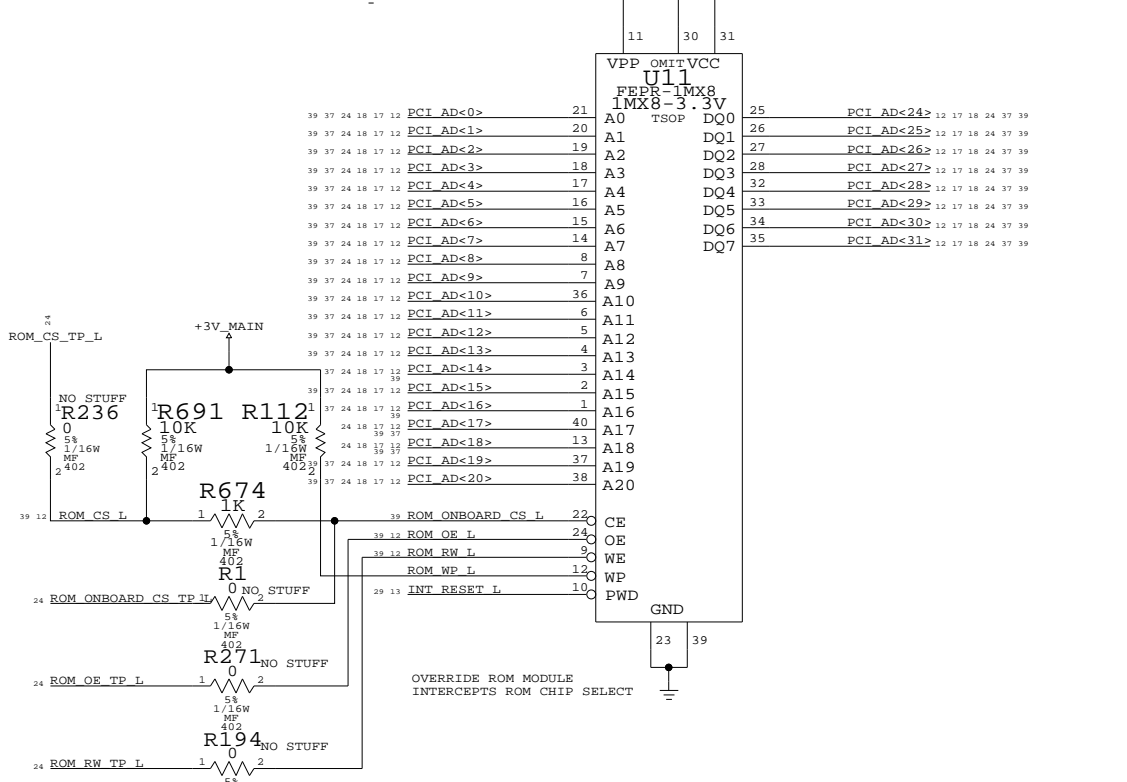
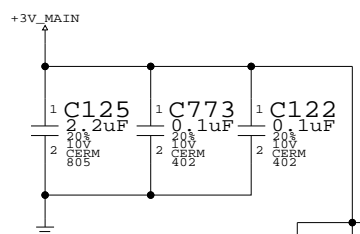
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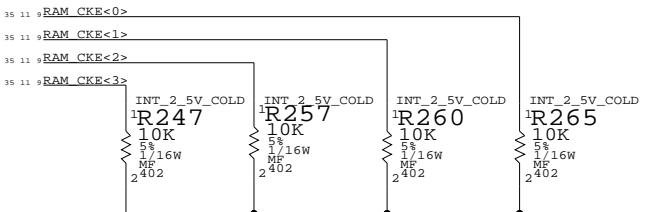
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS  
PINS ARE SWAPABLE FOR RPAKS

1MB BOOT ROM



| PART#    | QTY | DESCRIPTION      | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|------------------|-------------------------|----------|------------|
| 341S1542 | 1   | IC, BootRom Q16A | U11                     | CRITICAL | ?          |

Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.

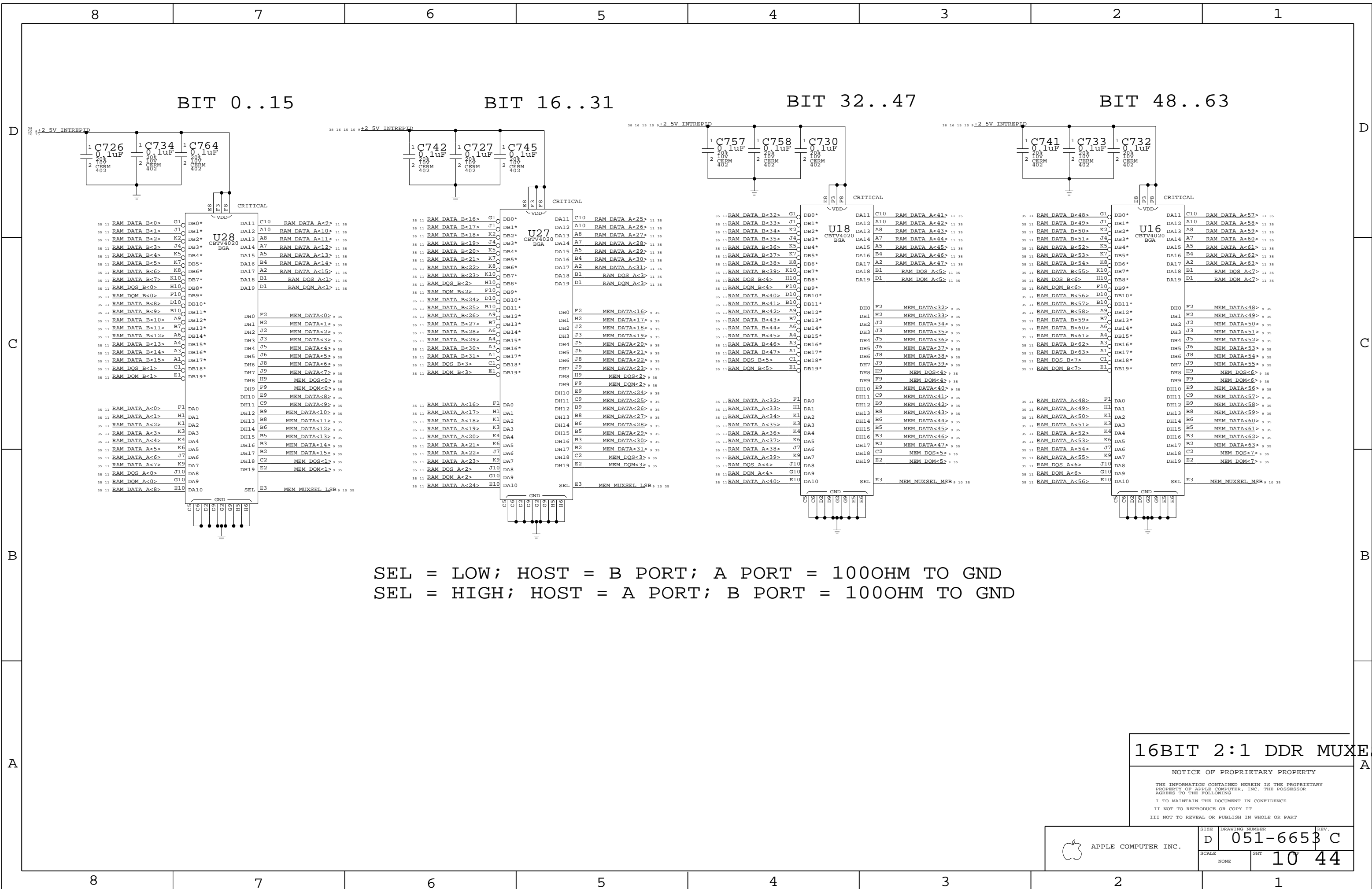


INT - DDR/BOOTROM

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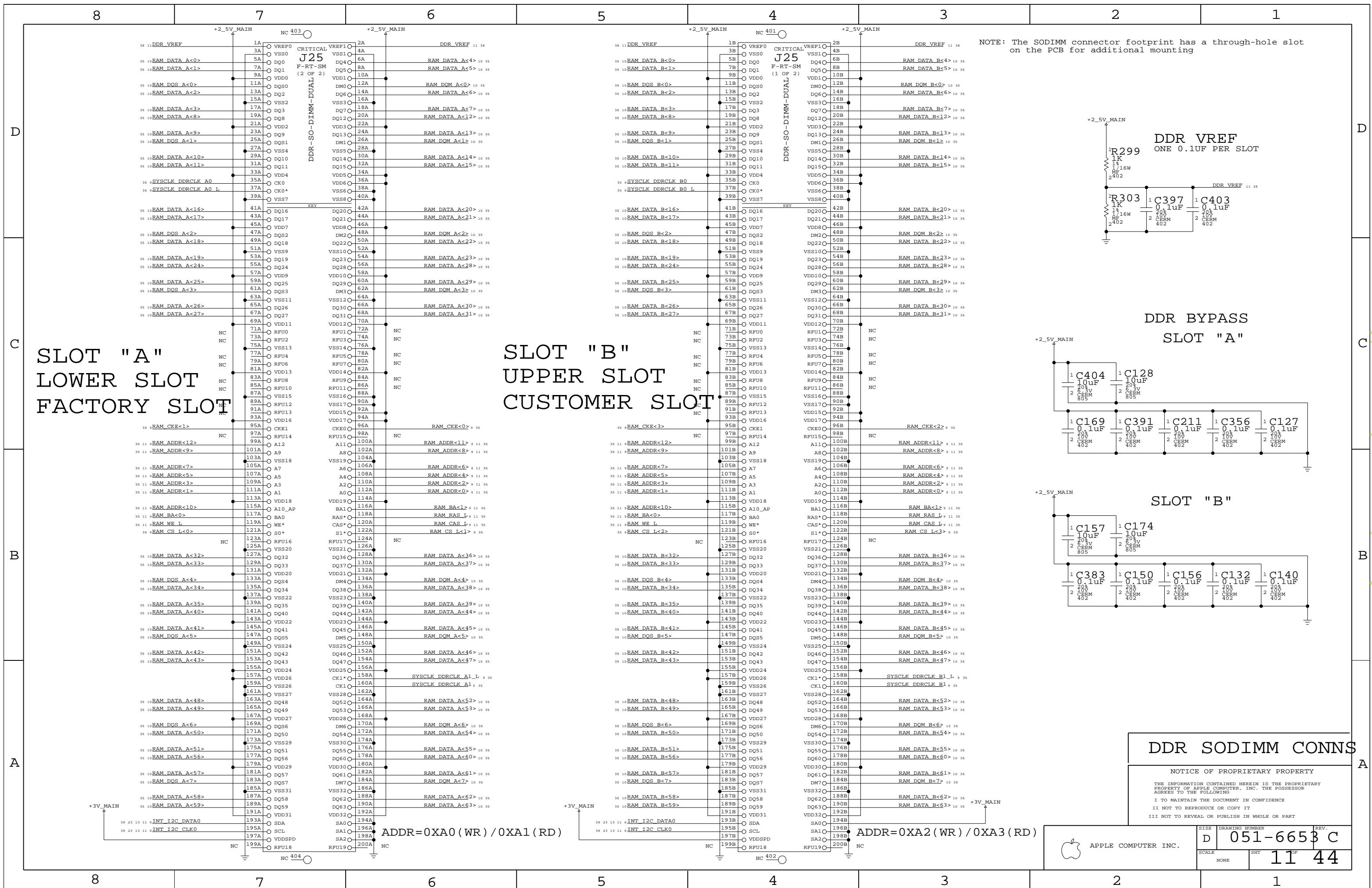


SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND  
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

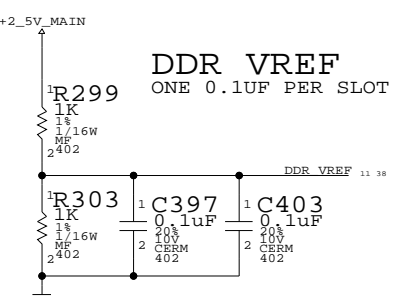
16BIT 2:1 DDR MUXES

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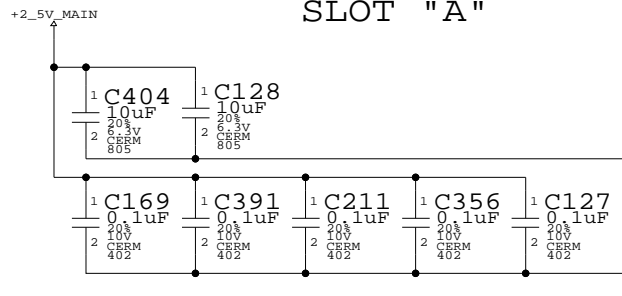
|                     |      |                |       |
|---------------------|------|----------------|-------|
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|                     | D    | 051-6653       | C     |
| SCALE               | NONE | SHT            | 10 44 |



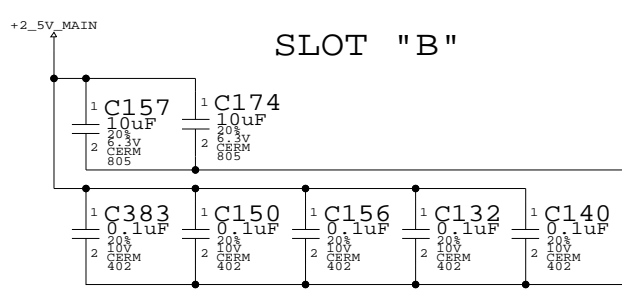
NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting



DDR VREF  
ONE 0.1uF PER SLOT



DDR BYPASS  
SLOT "A"



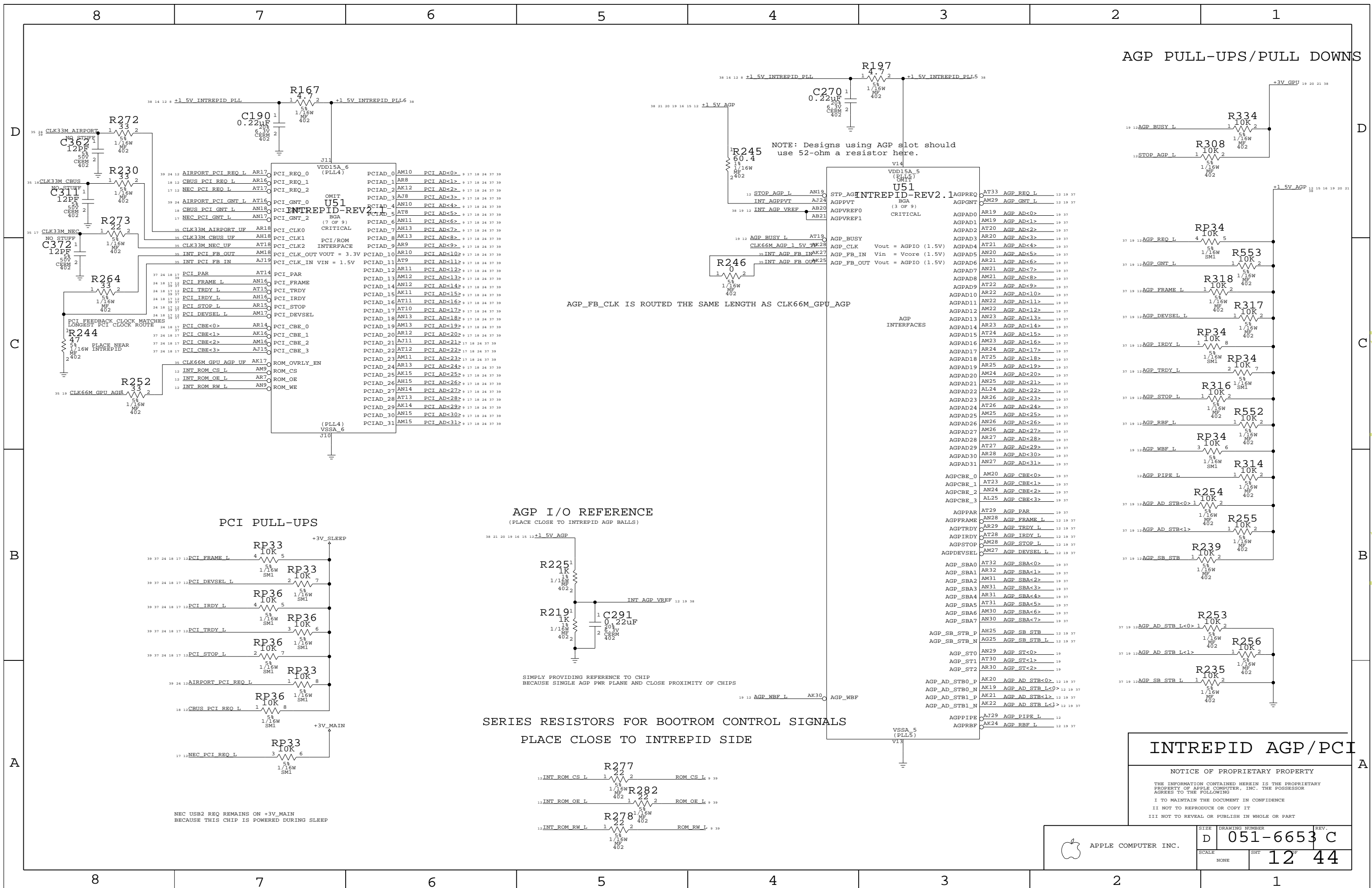
DDR BYPASS  
SLOT "B"

DDR SODIMM CONNS

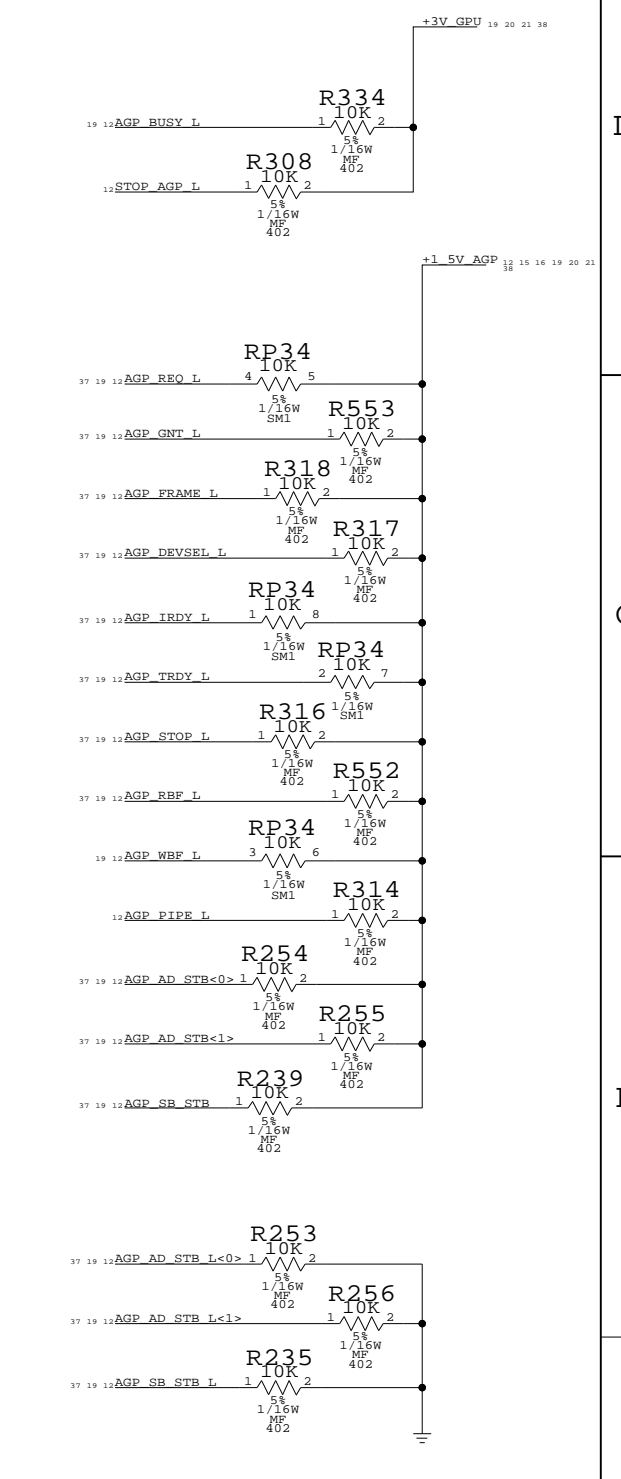
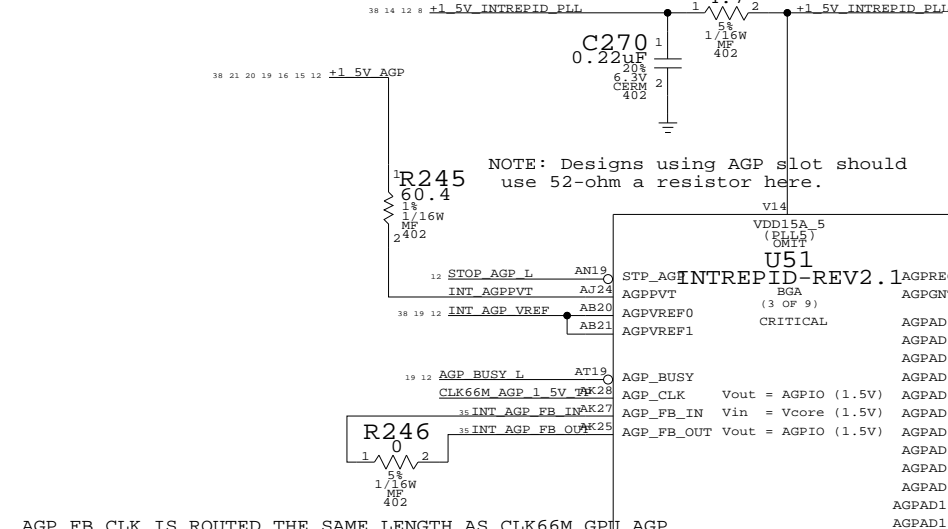
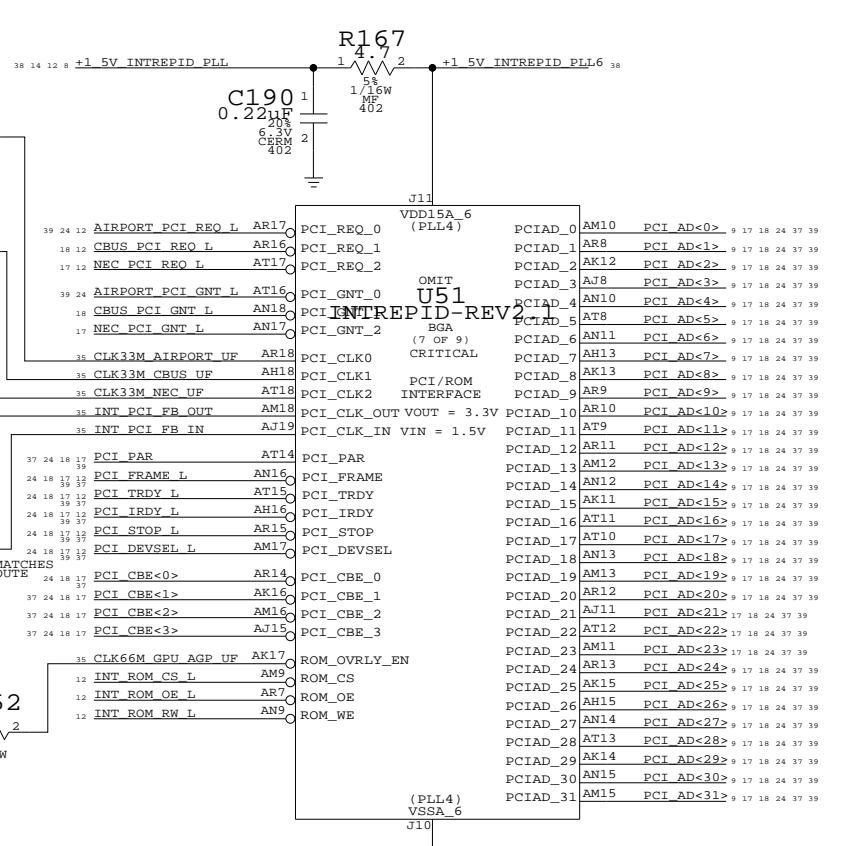
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-6653       | C    |
| SCALE               | SHT  | 11             | 44   |
| NONE                |      |                |      |

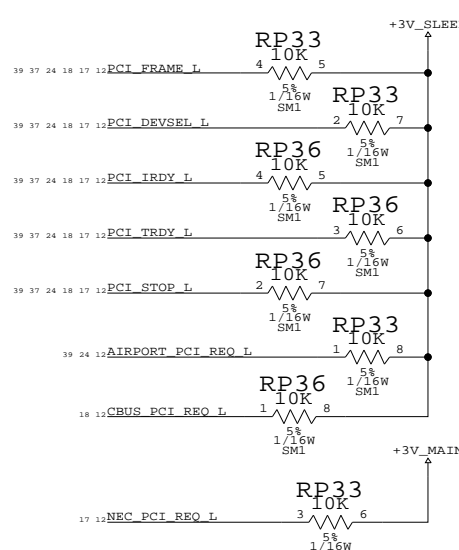
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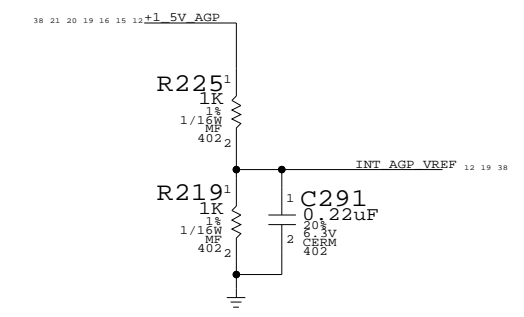
AGP PULL-UPS/PULL DOWNS



PCI PULL-UPS

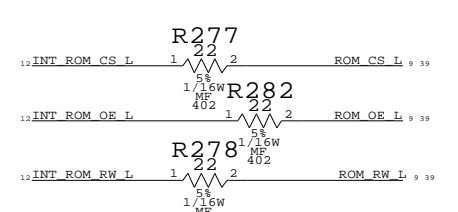


AGP I/O REFERENCE  
(PLACE CLOSE TO INTREPID AGP BALLS)



SIMPLY PROVIDING REFERENCE TO CHIP BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS  
PLACE CLOSE TO INTREPID SIDE



NEC USB2 REQ REMAINS ON +3V\_MAIN BECAUSE THIS CHIP IS POWERED DURING SLEEP

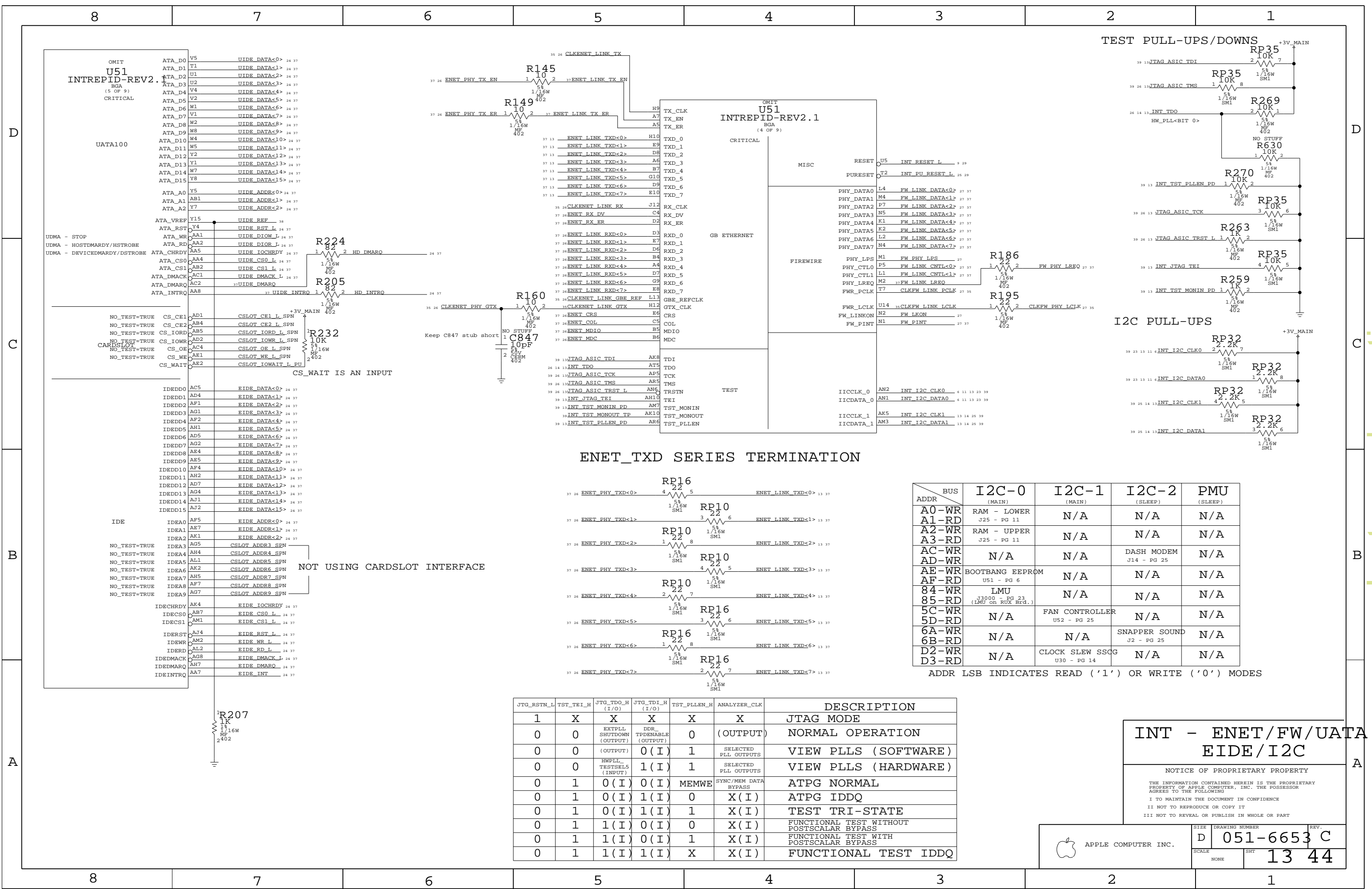
INTREPID AGP/PCI

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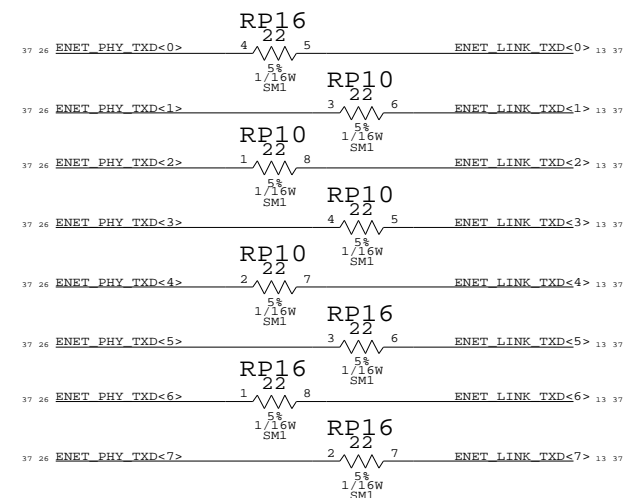
APPLE COMPUTER INC.

|       |      |                |            |      |    |
|-------|------|----------------|------------|------|----|
| SIZE  | D    | DRAWING NUMBER | 051-6653 C | REV. | C  |
| SCALE | NONE | SHT            | 12         | OF   | 44 |

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ENET\_TXD SERIES TERMINATION



| BUS ADDR | I2C-0 (MAIN)                    | I2C-1 (MAIN)    | I2C-2 (SLEEP) | PMU (SLEEP) |
|----------|---------------------------------|-----------------|---------------|-------------|
| A0-WR    | RAM - LOWER                     | N/A             | N/A           | N/A         |
| A1-RD    | J25 - PG 11                     | N/A             | N/A           | N/A         |
| A2-WR    | RAM - UPPER                     | N/A             | N/A           | N/A         |
| A3-RD    | J25 - PG 11                     | N/A             | N/A           | N/A         |
| AC-WR    | N/A                             | N/A             | DASH MODEM    | N/A         |
| AD-WR    | N/A                             | N/A             | J14 - PG 25   | N/A         |
| AE-WR    | BOOTBANG EEPROM                 | N/A             | N/A           | N/A         |
| AF-RD    | U51 - PG 6                      | N/A             | N/A           | N/A         |
| 84-WR    | LMU                             | N/A             | N/A           | N/A         |
| 85-RD    | J3000 - PG 23 (LMU on RUX Brd.) | N/A             | N/A           | N/A         |
| 5C-WR    | N/A                             | FAN CONTROLLER  | N/A           | N/A         |
| 5D-RD    | N/A                             | U52 - PG 25     | N/A           | N/A         |
| 6A-WR    | N/A                             | N/A             | SNAPPER SOUND | N/A         |
| 6B-RD    | N/A                             | N/A             | J2 - PG 25    | N/A         |
| D2-WR    | N/A                             | CLOCK SLEW SSCG | N/A           | N/A         |
| D3-RD    | N/A                             | U30 - PG 14     | N/A           | N/A         |

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

| JTG_RSTN_L | TST_TEL_H | JTG_TDO_H (I/O)          | JTG_TDI_H (I/O)        | TST_PLEN_H | ANALYZER_CLK         | DESCRIPTION                               |
|------------|-----------|--------------------------|------------------------|------------|----------------------|---|
| 1          | X         | X                        | X                      | X          | X                    | JTAG MODE                                 |
| 0          | 0         | EXTPLL SHUTDOWN (OUTPUT) | DDR_TPDENABLE (OUTPUT) | 0          | (OUTPUT)             | NORMAL OPERATION                          |
| 0          | 0         | (OUTPUT)                 | 0(I)                   | 1          | SELECTED PLL OUTPUTS | VIEW PLLS (SOFTWARE)                      |
| 0          | 0         | HWPLL_TESTSELS (INPUT)   | 1(I)                   | 1          | SELECTED PLL OUTPUTS | VIEW PLLS (HARDWARE)                      |
| 0          | 1         | 0(I)                     | 0(I)                   | MEMWE      | SYNC/MEM DATA BYPASS | ATPG NORMAL                               |
| 0          | 1         | 0(I)                     | 1(I)                   | 0          | X(I)                 | ATPG IDDQ                                 |
| 0          | 1         | 0(I)                     | 1(I)                   | 1          | X(I)                 | TEST TRI-STATE                            |
| 0          | 1         | 1(I)                     | 0(I)                   | 0          | X(I)                 | FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS |
| 0          | 1         | 1(I)                     | 0(I)                   | 1          | X(I)                 | FUNCTIONAL TEST WITH POSTSCALAR BYPASS    |
| 0          | 1         | 1(I)                     | 1(I)                   | X          | X(I)                 | FUNCTIONAL TEST IDDQ                      |

INT - ENET/FW/UATA EIDE/I2C

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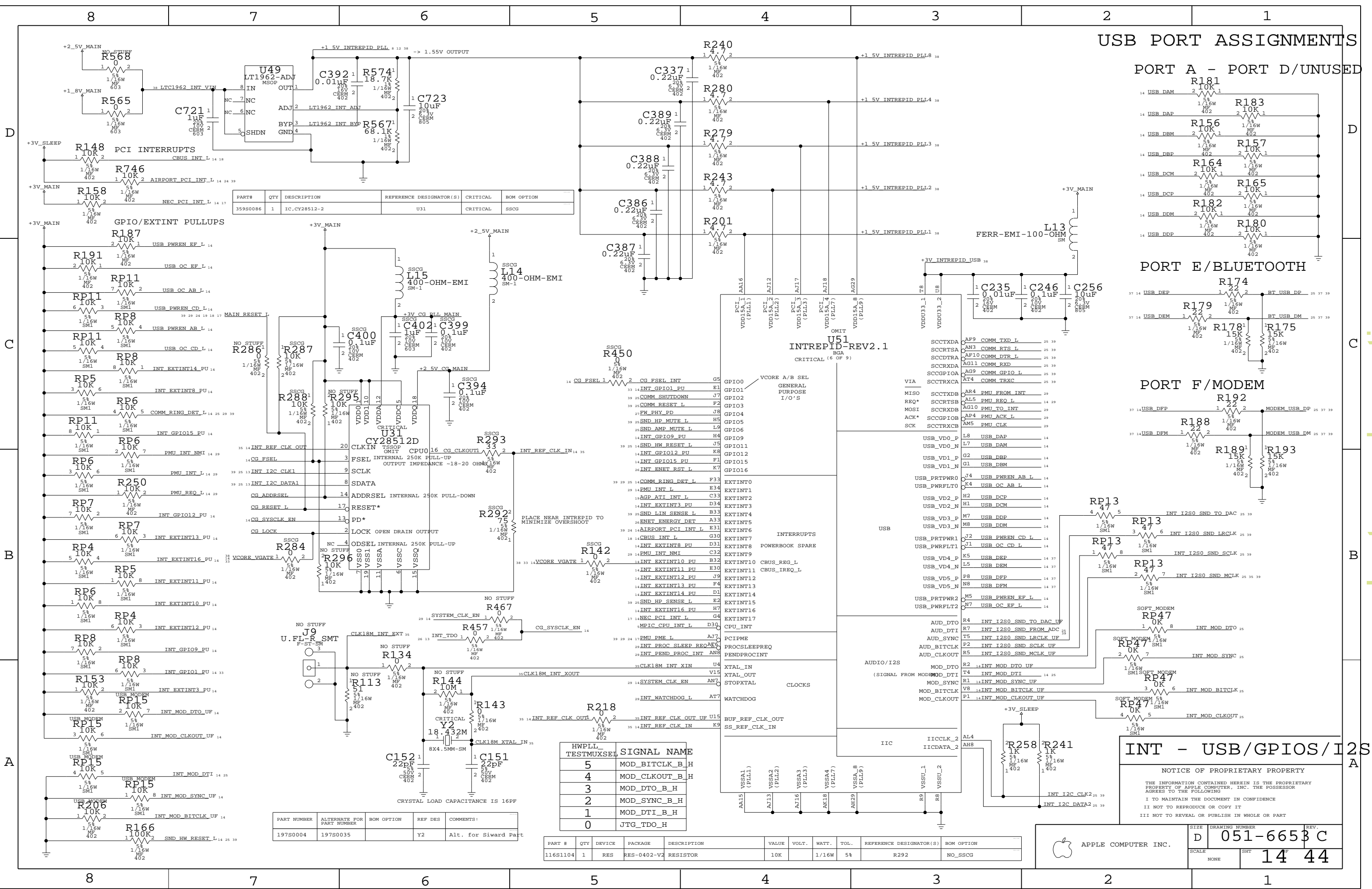
APPLE COMPUTER INC.

SIZE: D, DRAWING NUMBER: 051-6653, REV. C

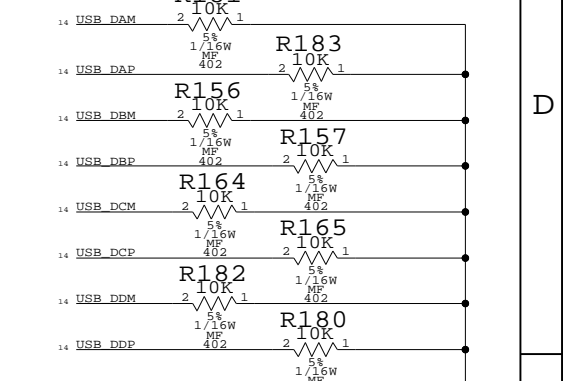
SCALE: NONE, SHEET: 13 OF 44

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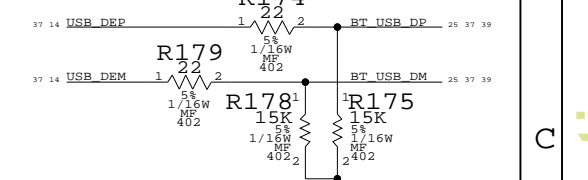
# USB PORT ASSIGNMENTS



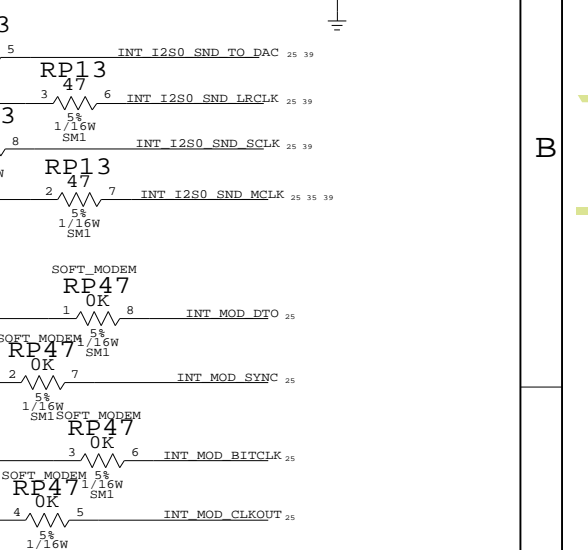
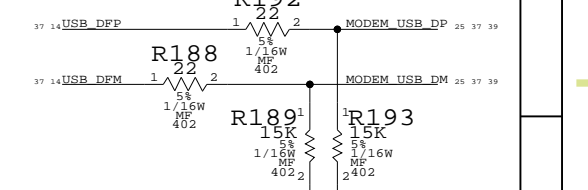
PORT A - PORT D/UNUSED



PORT E/BLUETOOTH



PORT F/MODEM



INT - USB/GPIOS/I2S

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| PART#    | QTY | DESCRIPTION  | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------|-------------------------|----------|------------|
| 359S0086 | 1   | IC,CY28512-2 | U31                     | CRITICAL | SSCG       |

| HWPLL TESTMUXSEL | SIGNAL NAME    |
|------------------|----------------|
| 5                | MOD_BITCLK_B_H |
| 4                | MOD_CLKOUT_B_H |
| 3                | MOD_DTO_B_H    |
| 2                | MOD_SYNC_B_H   |
| 1                | MOD_DTI_B_H    |
| 0                | JTG_TDO_H      |

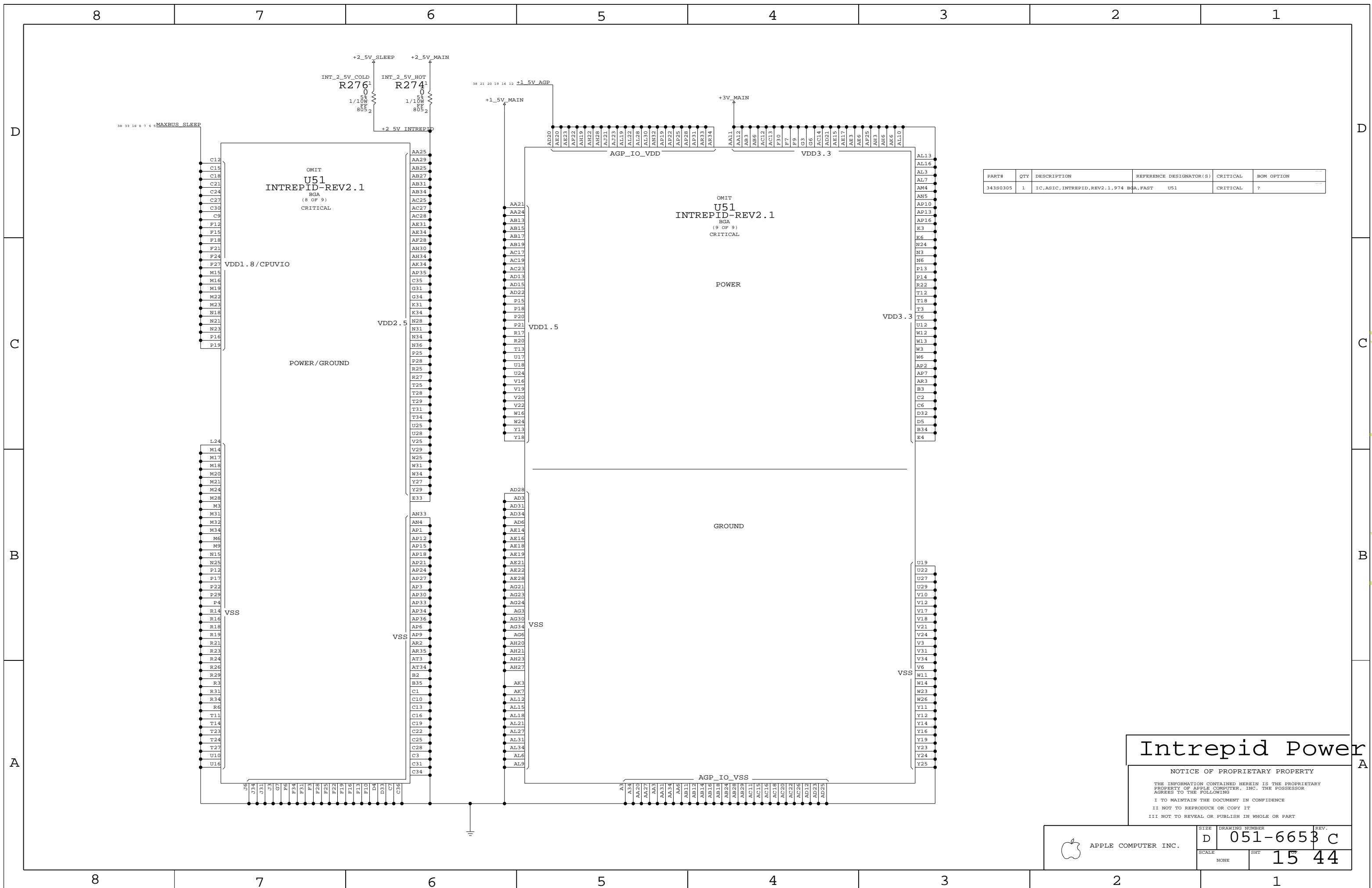
| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:           |
|-------------|---------------------------|------------|---------|---------------------|
| 197S0004    | 197S0035                  |            | Y2      | Alt. for Sward Part |

| PART #   | QTY | DEVICE | PACKAGE     | DESCRIPTION | VALUE | VOLT. | WATT. | TOL. | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|--------|-------------|-------------|-------|-------|-------|------|-------------------------|------------|
| 116S1104 | 1   | RES    | RES-0402-V2 | RESISTOR    | 10K   |       | 1/16W | 5%   | R292                    | NO_SSCG    |

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SIZE: D  
 DRAWING NUMBER: 051-6653 C  
 SCALE: NONE  
 SHEET: 14 OF 44

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| PART#    | QTY | DESCRIPTION                          | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------------|-------------------------|----------|------------|
| 34380305 | 1   | IC,ASIC,INTREPID,REV2.1,974 BGA,FAST | U51                     | CRITICAL | ?          |

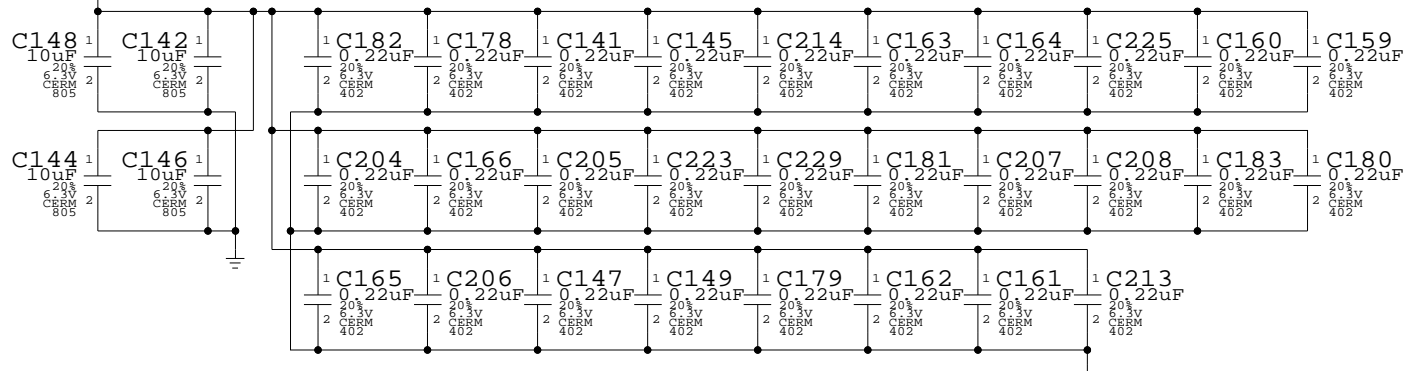
# Intrepid Power

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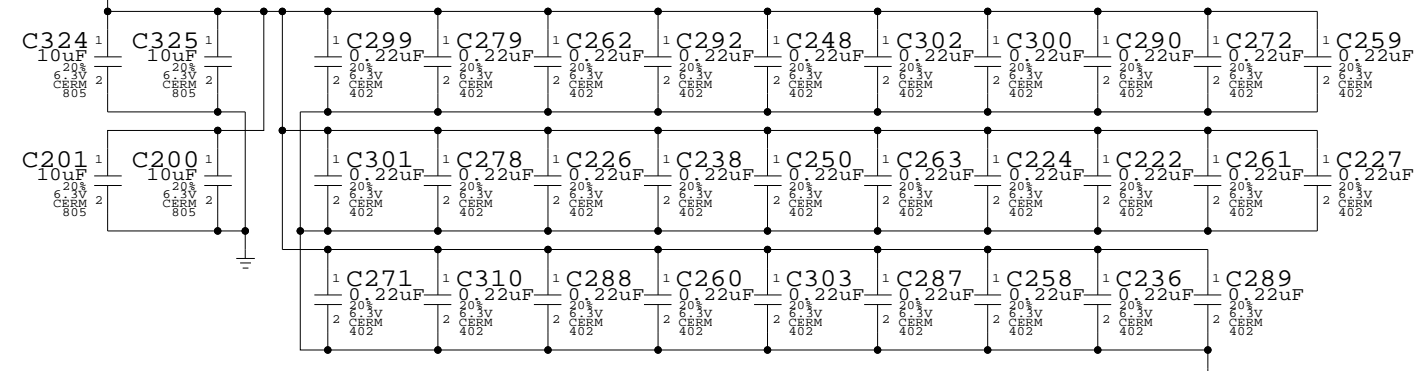
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | NONE | 051-6653       | C    |
| SCALE               |      | SHT            |      |
| NONE                |      | 15             | 44   |

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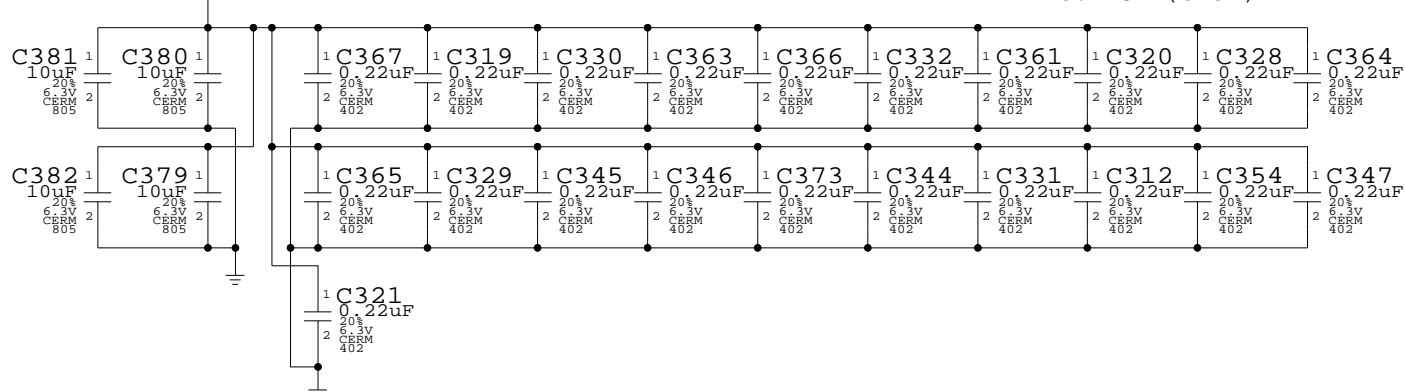
INTREPID MAXBUS DECOUPLING



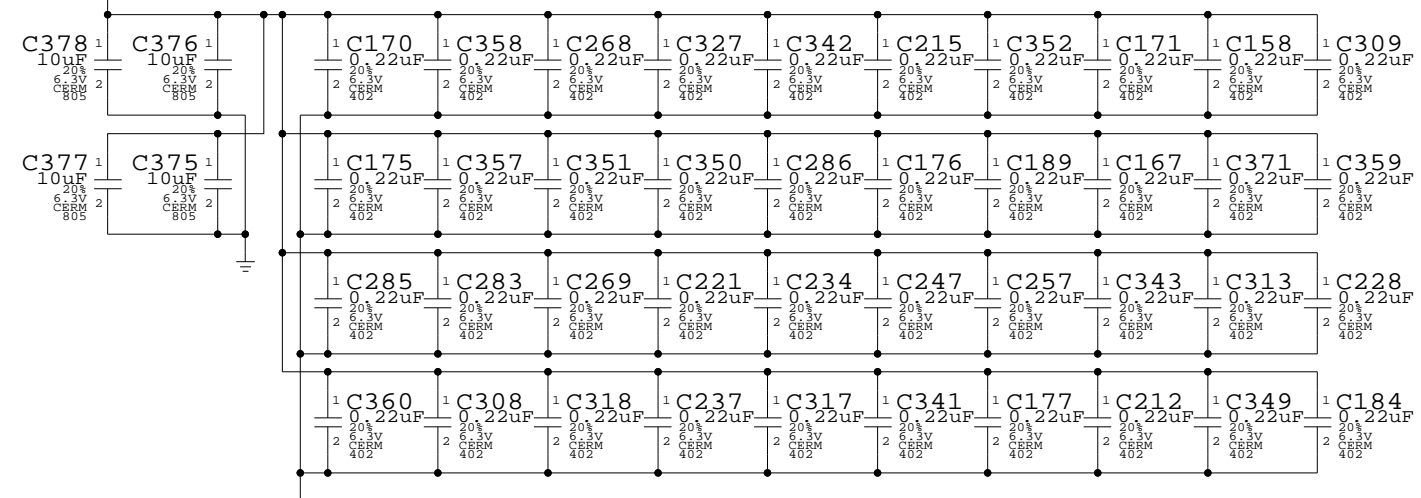
INTREPID CORE DECOUPLING



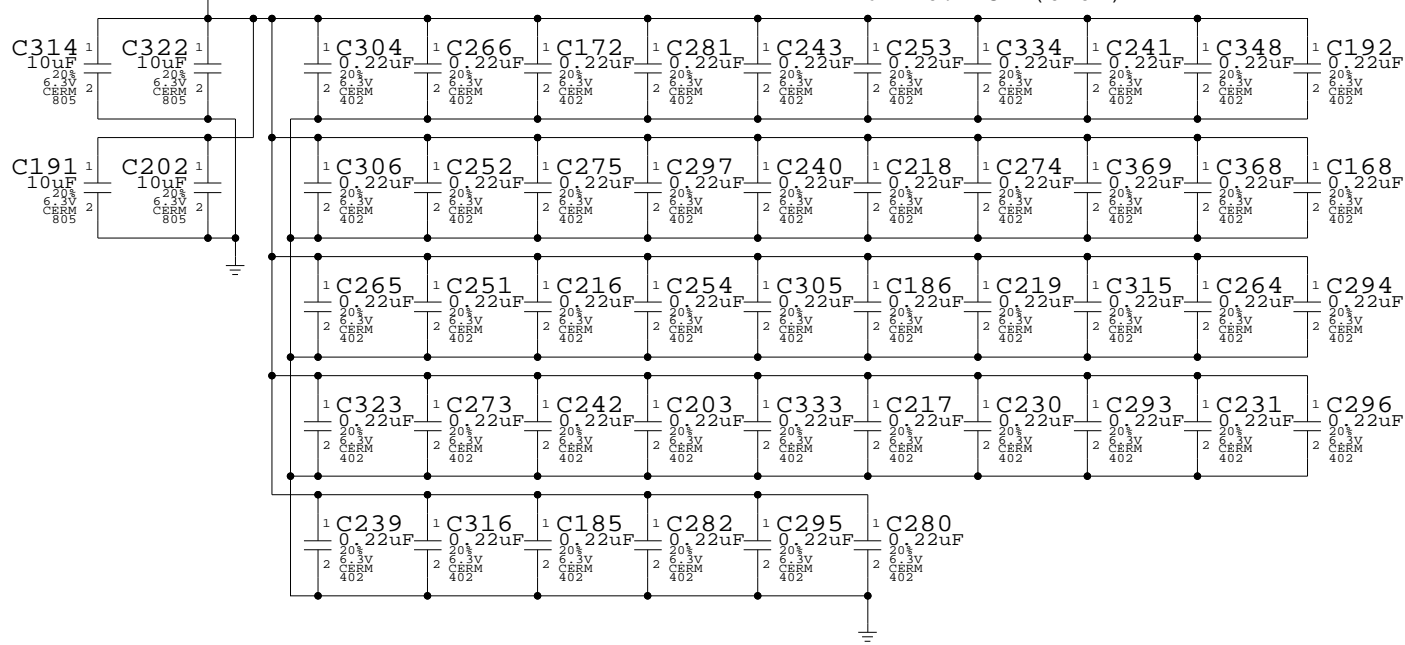
INTREPID AGP I/O DECOUPLING



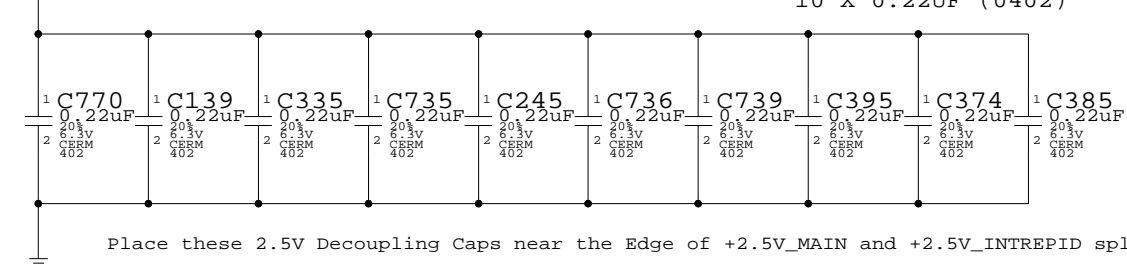
INTREPID 3.3V DECOUPLING



INTREPID DDR DECOUPLING



INTREPID/MAIN 2.5V DECOUPLING



Place these 2.5V Decoupling Caps near the Edge of +2.5V\_MAIN and +2.5V\_INTREPID split

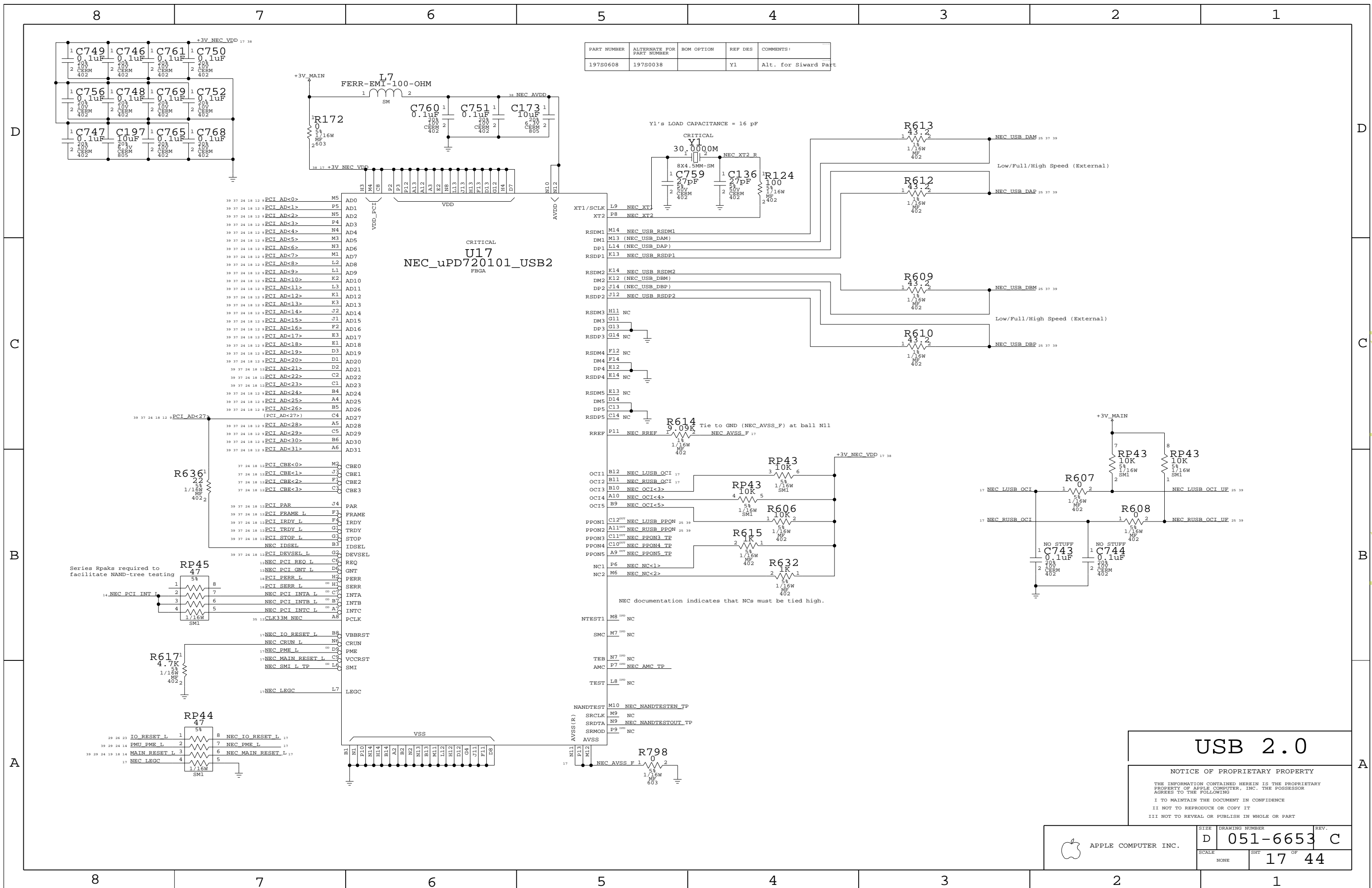
Intrepid Decoupling

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|---------------------|-------|----------------|------|
| APPLE COMPUTER INC. | SIZE  | DRAWING NUMBER | REV. |
|                     | D     | 051-6653 C     |      |
|                     | SCALE | SHEET          |      |
|                     | NONE  | 16             | 44   |

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| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS             |
|-------------|---------------------------|------------|---------|----------------------|
| 197S0608    | 197S0038                  |            | Y1      | Alt. for Siward Part |

Y1's LOAD CAPACITANCE = 16 pF

CRITICAL  
Y1  
30.0000M  
NEC XT2 R

R614  
9 09K  
1/16W  
402  
Tie to GND (NEC\_AVSS\_F) at ball N11

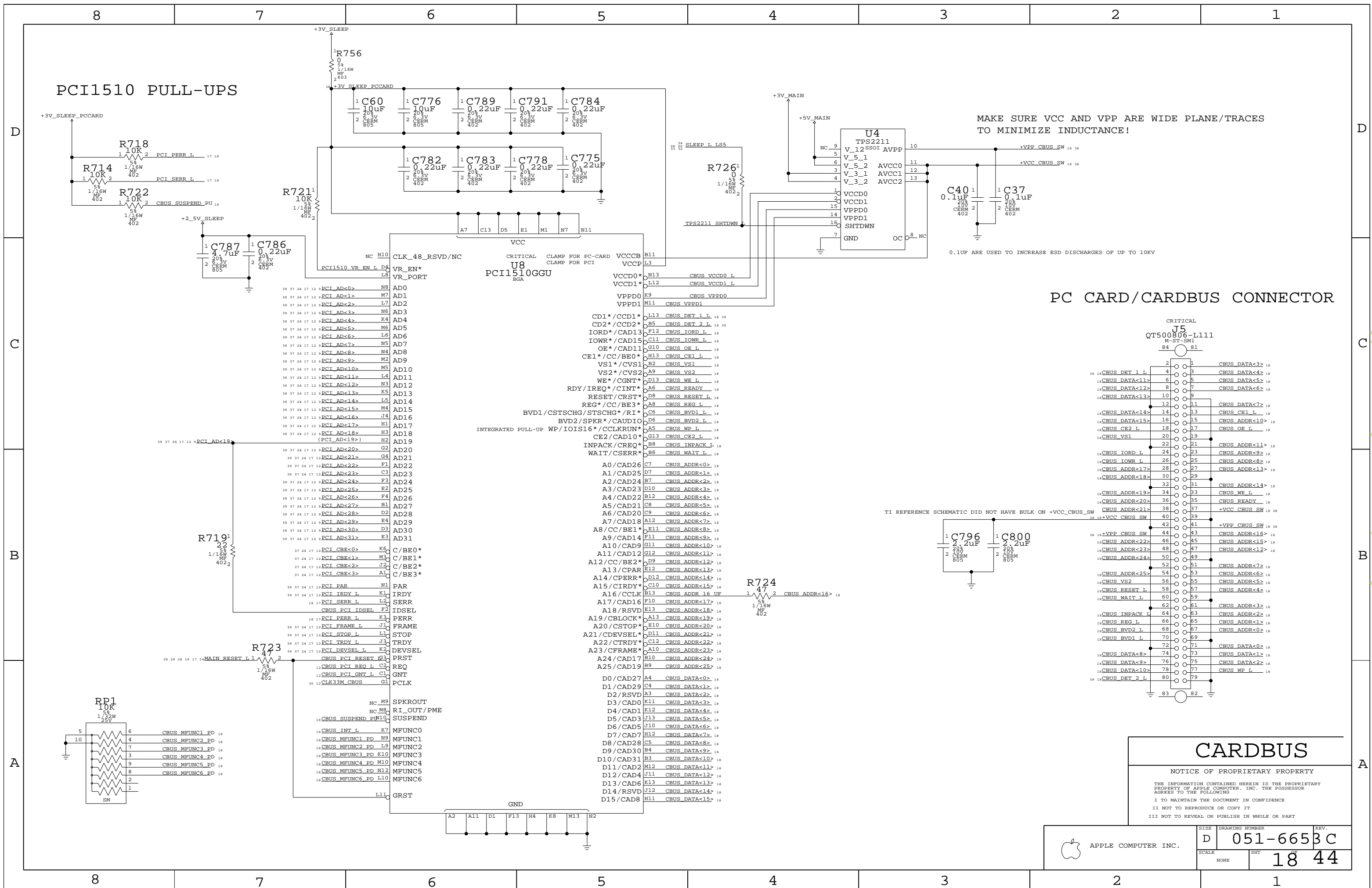
NEC documentation indicates that NCs must be tied high.

# USB 2.0

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|---------------------|------|----------------|----------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.     |
|                     | D    | 051-6653       | C        |
| SCALE               | NONE | SHT            | 17 OF 44 |

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PCI1510 PULL-UPS

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

PC CARD/CARDBUS CONNECTOR

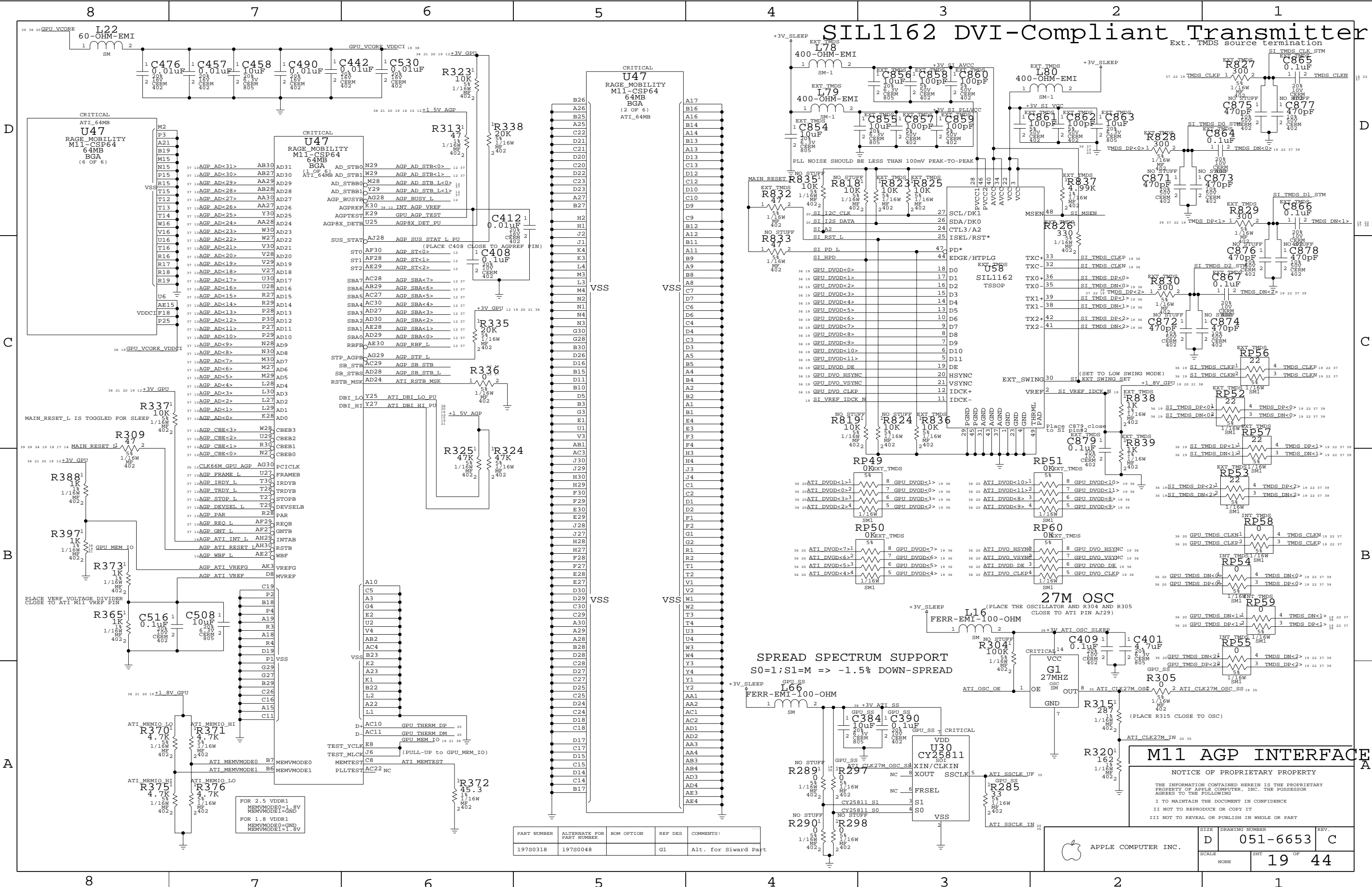
CARDBUS

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|                     |               |                             |                    |
|---------------------|---------------|-----------------------------|--------------------|
| APPLE COMPUTER INC. | SIZE<br>D     | DRAWING NUMBER<br>051-6653C | REV.<br>C          |
|                     | SCALE<br>NONE | SHEET<br>18                 | TOTAL SHEETS<br>44 |

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# SIL1162 DVI-Compliant Transmitter



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS            |
|-------------|---------------------------|------------|---------|---------------------|
| 197S0318    | 197S0048                  |            | G1      | Alt. for Sward Part |

**M11 AGP INTERFACE**

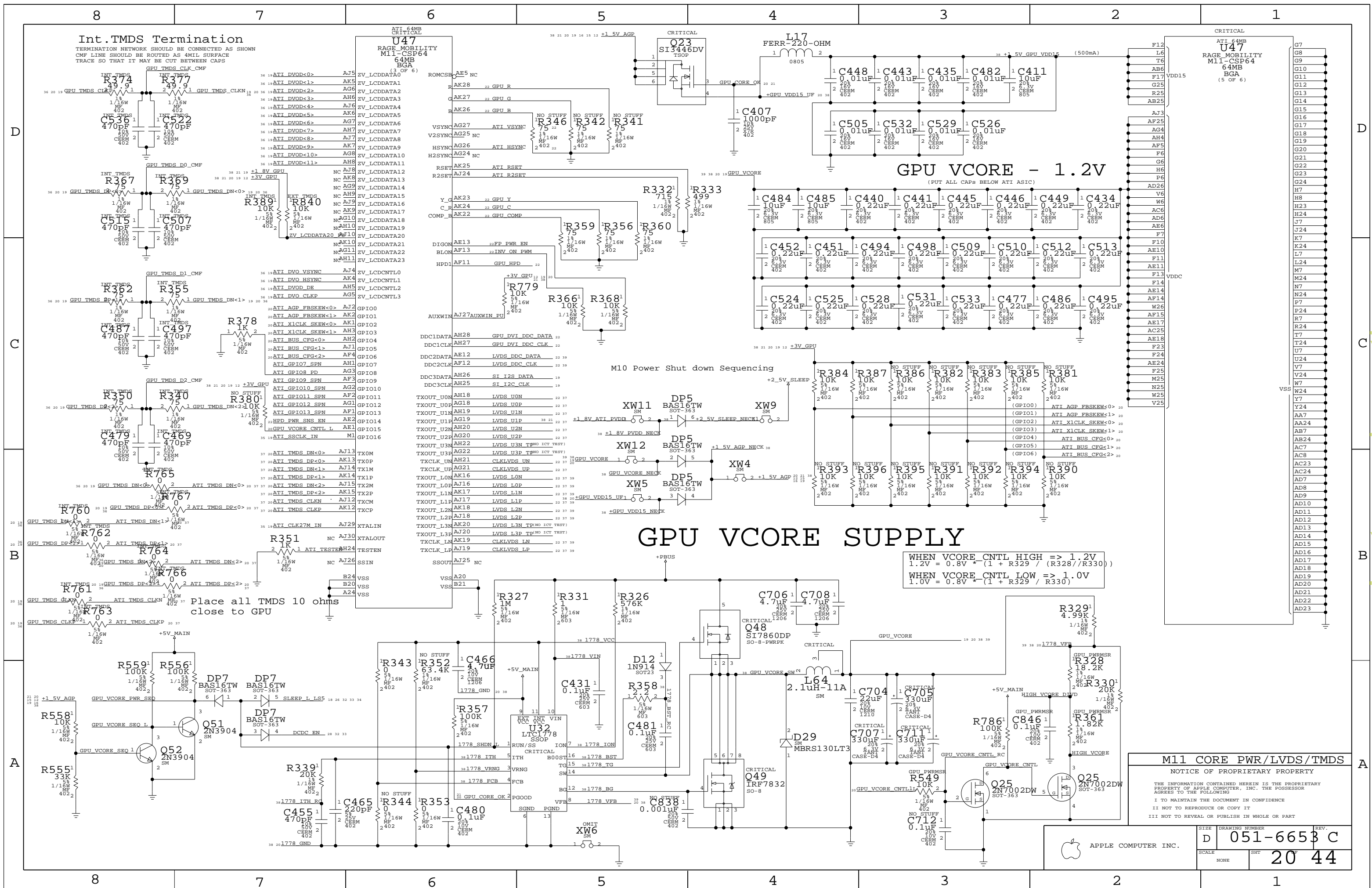
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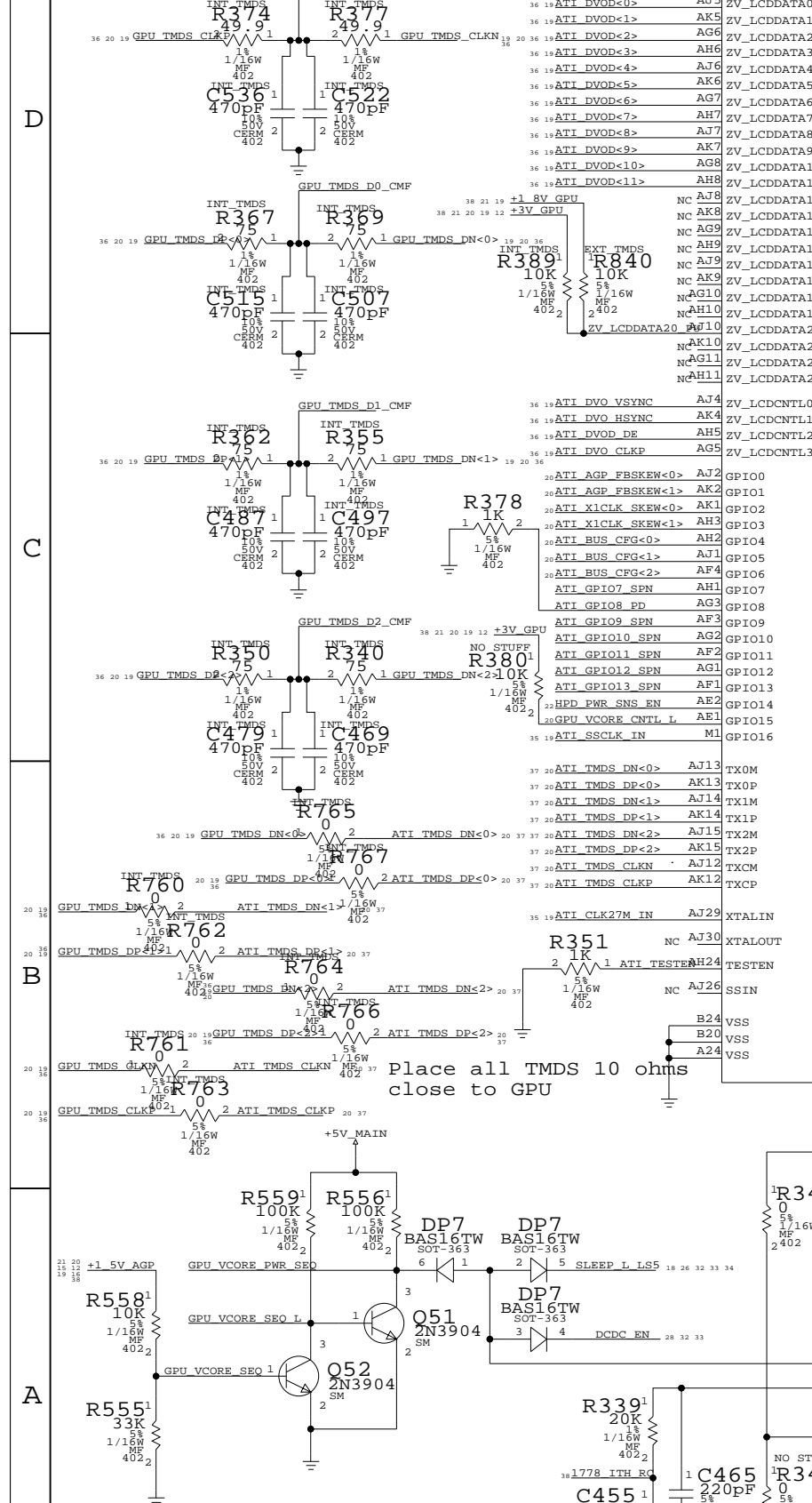
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|---------------------|-------|------|----------------|----------|------|----|
| APPLE COMPUTER INC. | SIZE  | D    | DRAWING NUMBER | 051-6653 | REV. | C  |
|                     | SCALE | NONE | SHT            | 19       | OF   | 44 |

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**Int. TMDS Termination**

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN  
 CMP LINE SHOULD BE ROUTED AS 4MIL SURFACE  
 TRACE SO THAT IT MAY BE CUT BETWEEN CAPS



Place all TMDS 10 ohms close to GPU

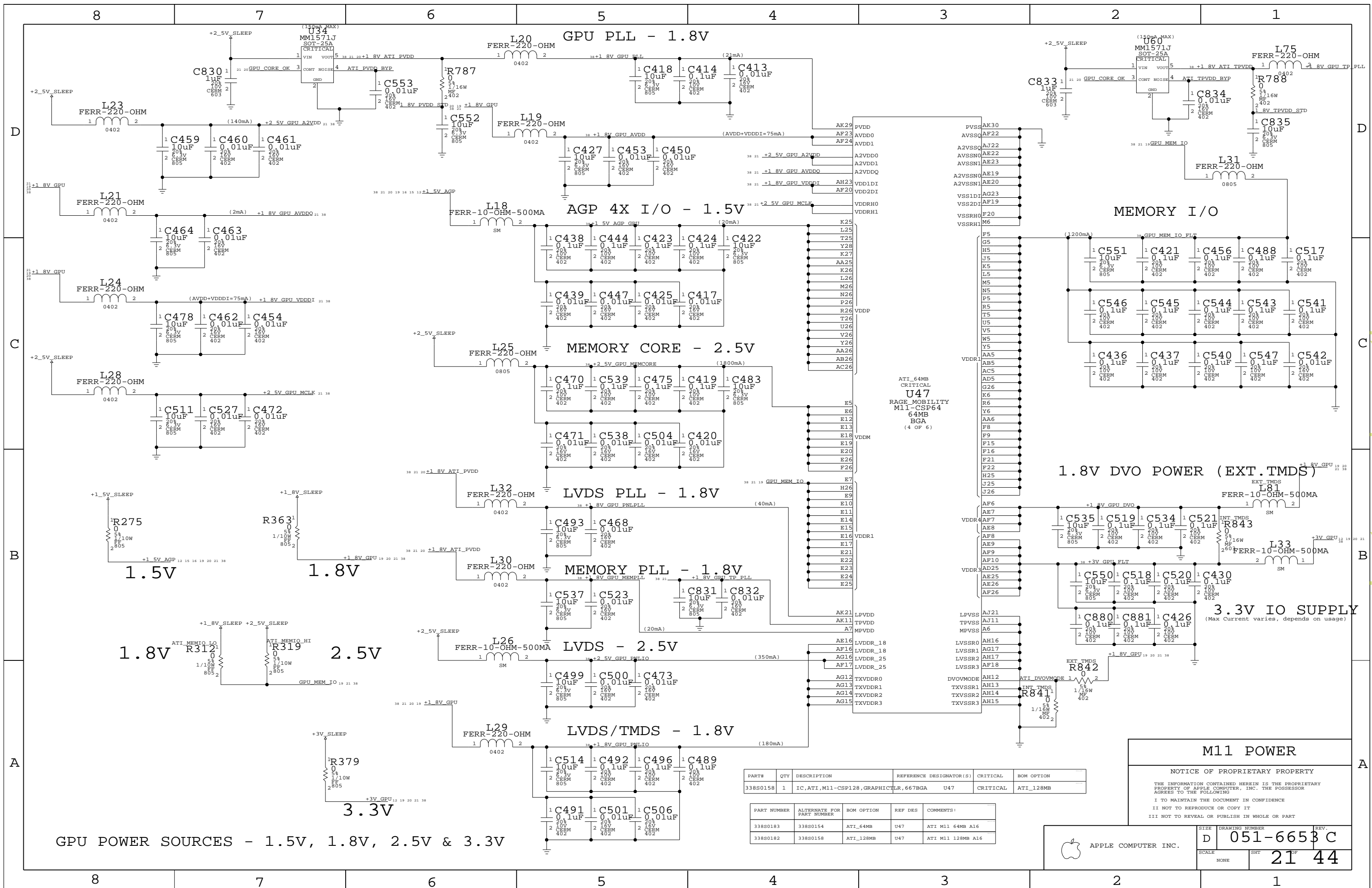
**GPU VCORE SUPPLY**

WHEN VCORE\_CNTL HIGH => 1.2V  
 $1.2V = 0.8V * (1 + R329 / (R328 // R330))$   
 WHEN VCORE\_CNTL LOW => 1.0V  
 $1.0V = 0.8V * (1 + R329 / R330)$

|                     |  |   |
|---------------------|--|---|
| APPLE COMPUTER INC. |  | SIZE: D<br>DRAWING NUMBER: 051-6653 C<br>REV.: 44 |
|---------------------|--|---|

**M11 CORE PWR/LVDS/TMDS**  
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GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

| PART#    | QTY | DESCRIPTION                          | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------------|-------------------------|----------|------------|
| 338S0158 | 1   | IC,ATI,M11-CSP128,GRAPHIC,TLR,667BGA | U47                     | CRITICAL | ATI_128MB  |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:         |
|-------------|---------------------------|------------|---------|-------------------|
| 338S0183    | 338S0154                  | ATI_64MB   | U47     | ATI M11 64MB A16  |
| 338S0182    | 338S0158                  | ATI_128MB  | U47     | ATI M11 128MB A16 |

**M11 POWER**

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SIZE: D

DRAWING NUMBER: 051-6653 C

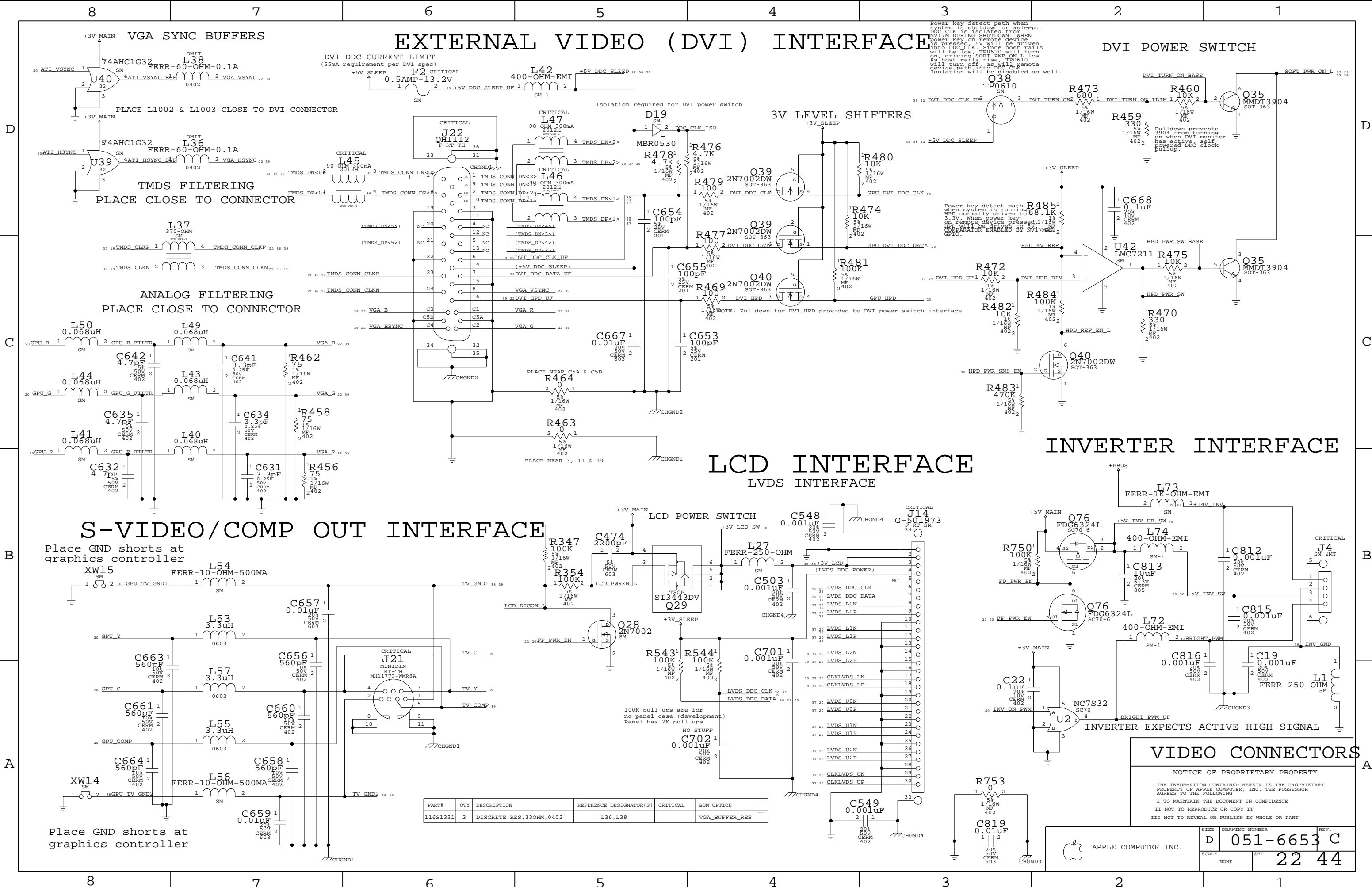
SCALE: NONE

SHT: 21

REV: 44

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# EXTERNAL VIDEO (DVI) INTERFACE



| PART#    | QTY | DESCRIPTION                | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION     |
|----------|-----|----------------------------|-------------------------|----------|----------------|
| 116S1331 | 2   | DISCRETE, RES, 330HM, 0402 | L36, L38                |          | VGA_BUFFER_RES |

## VIDEO CONNECTORS

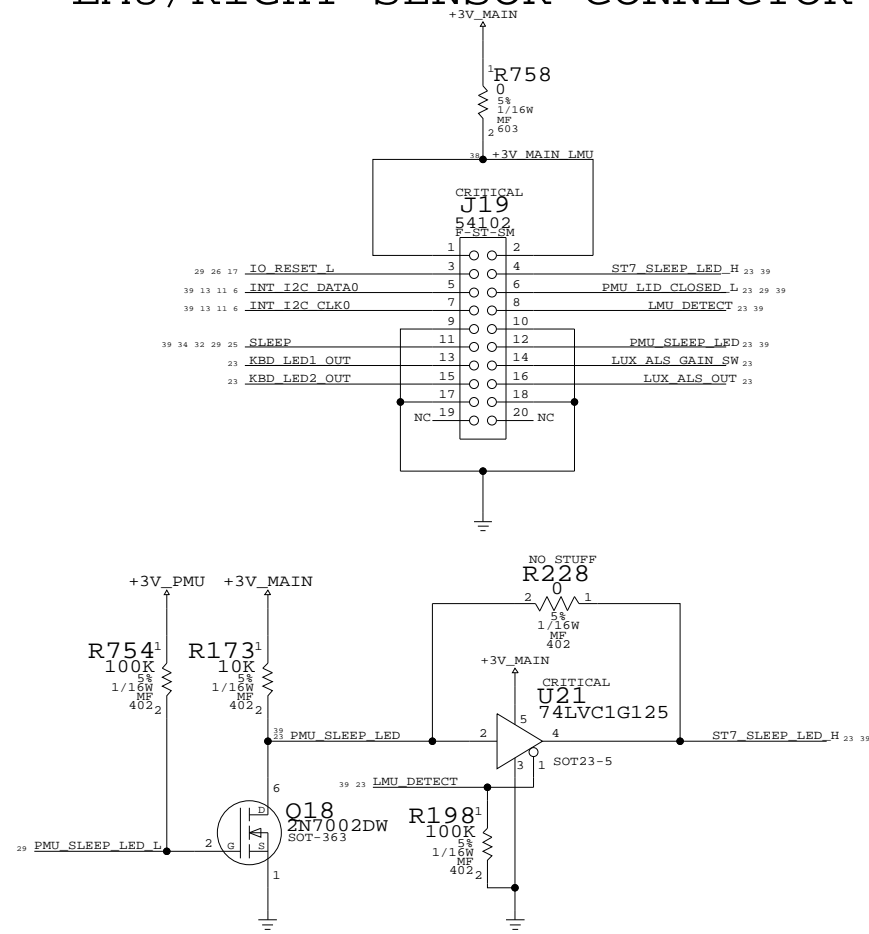
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APPLE COMPUTER INC.

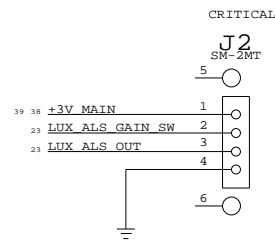
|       |      |                |          |      |   |
|-------|------|----------------|----------|------|---|
| SIZE  | D    | DRAWING NUMBER | 051-6653 | REV. | C |
| SCALE | NONE | SHT            | 22       | 44   |   |

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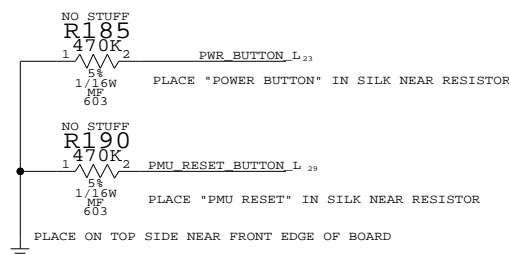
# LMU/RIGHT SENSOR CONNECTOR



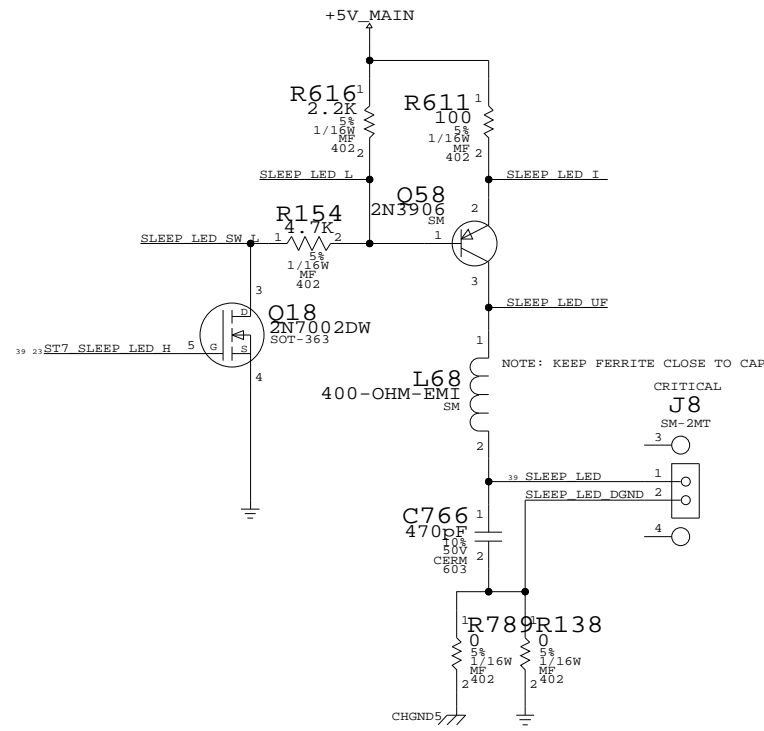
# LEFT LIGHT SENSOR CONNECTOR



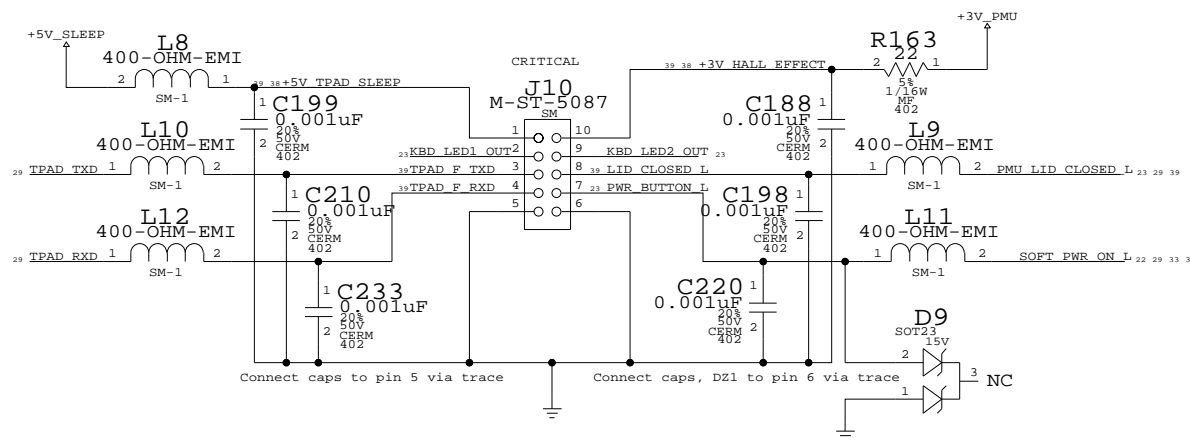
# DEBUG HELPERS



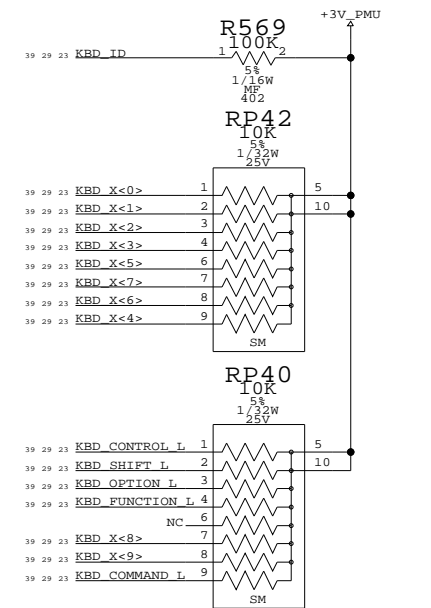
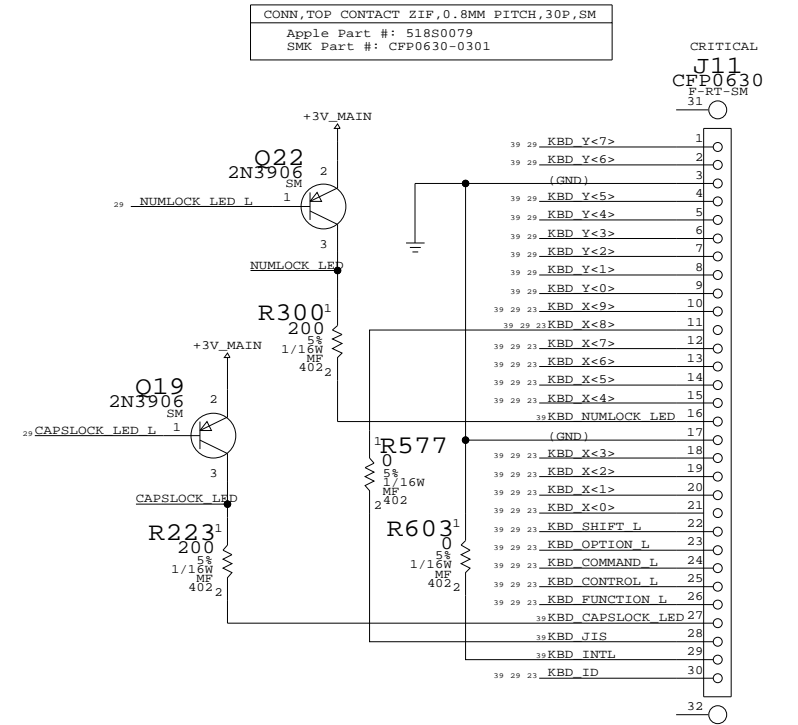
# SLEEP LED



# TRACKPAD/PWR BTN CONN



# TOP CONTACT ZIF KEYBOARD CONN



# KEYBOARD PULLUPS

# KEYBOARD/TPAD/SLEEP LED

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|                     |      |                |       |
|---------------------|------|----------------|-------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.  |
|                     | D    | 051-6653       | C     |
| SCALE               | NONE | SHT            | 23 44 |

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8

7

6

5

4

3

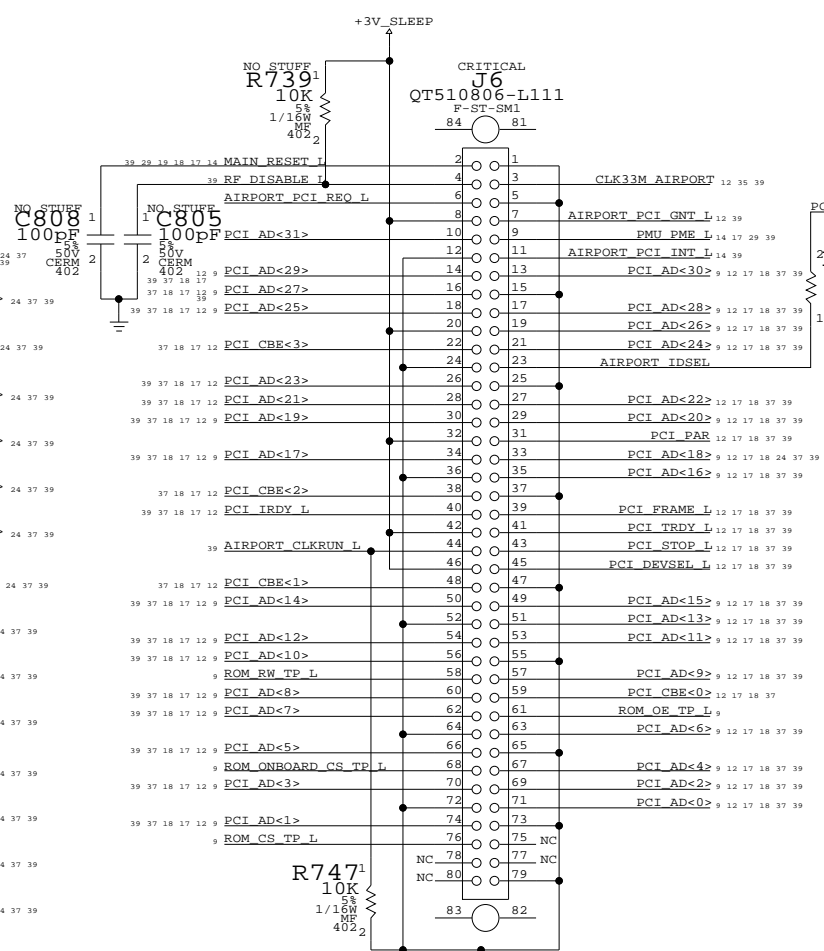
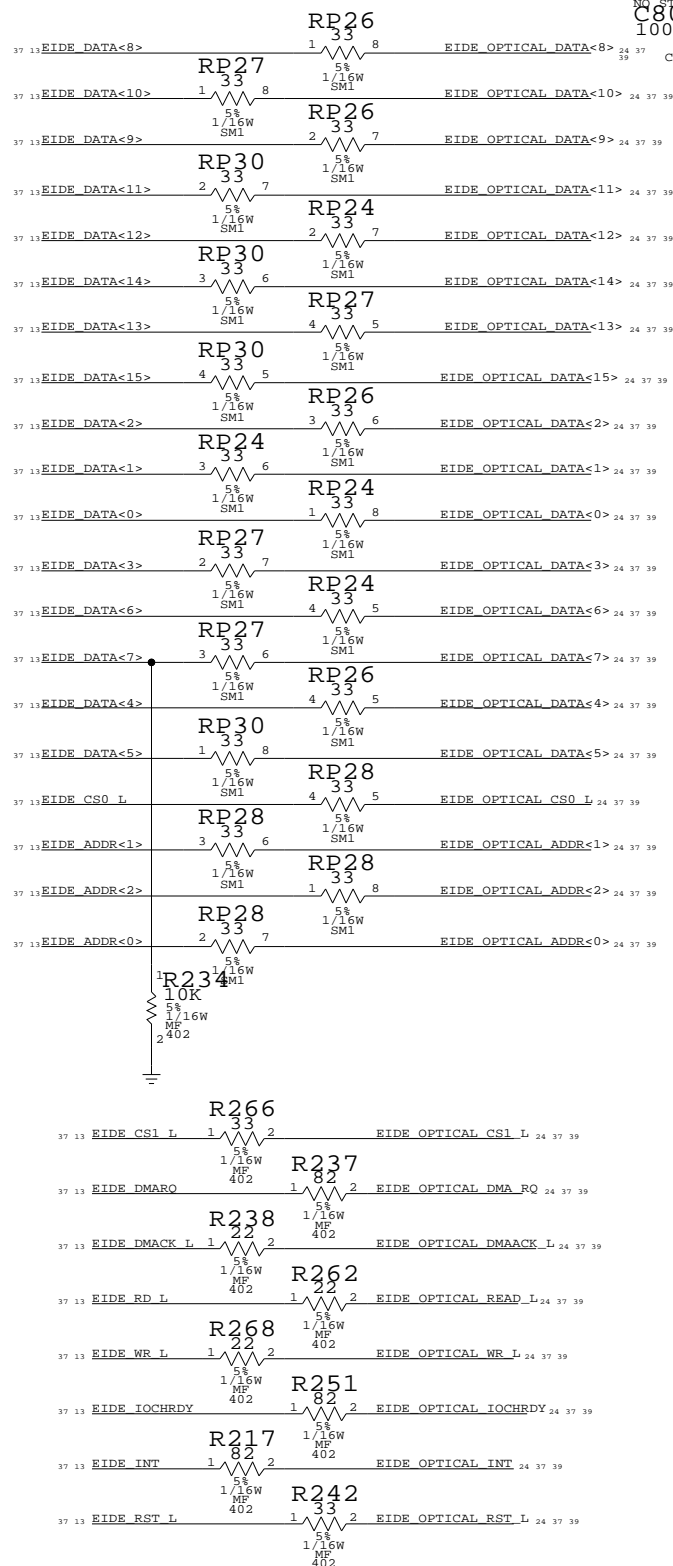
2

1

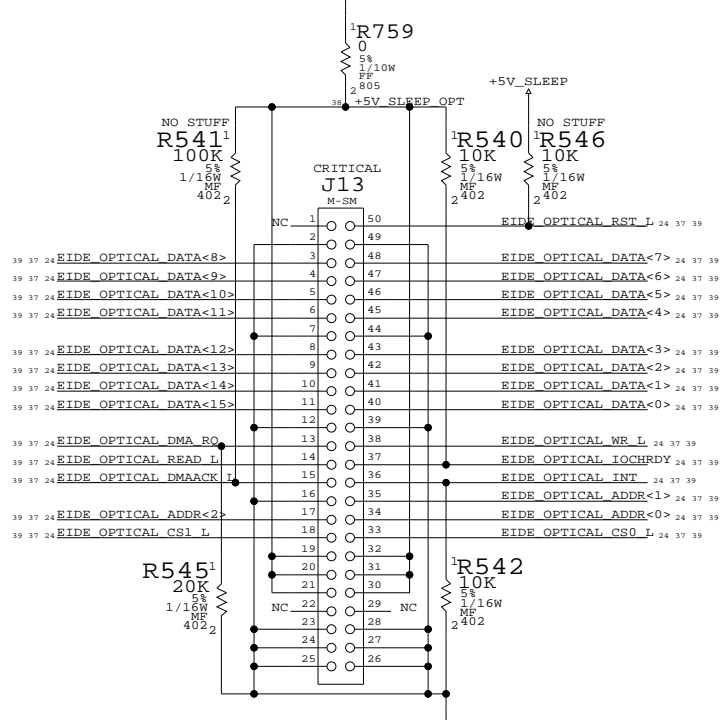
### WIRELESS INTERFACE

### HARD DRIVE INTERFACE (UATA100)

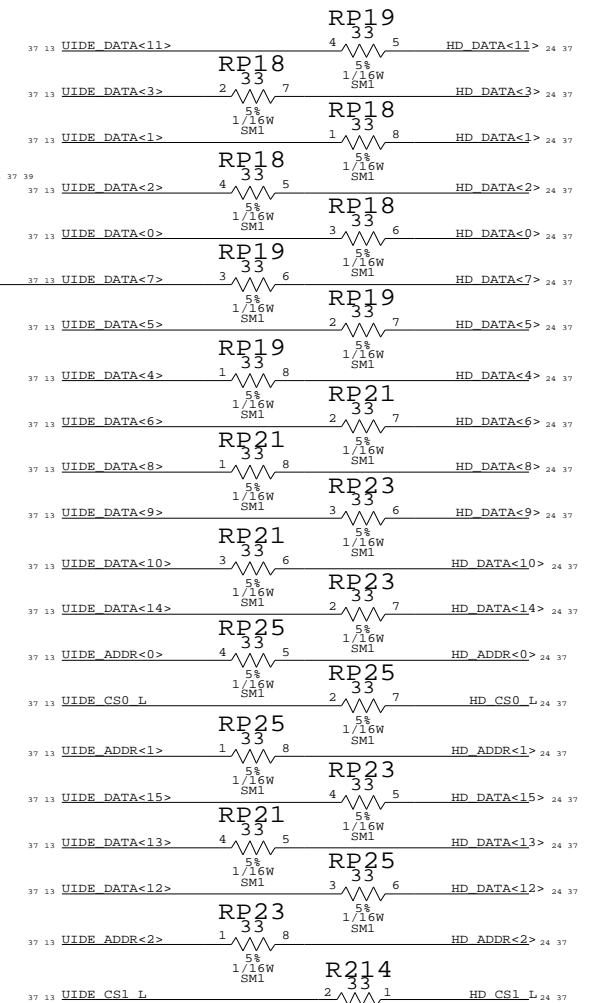
#### EIDE SERIES TERMINATION PLACE TERMINATORS NEAR INTREPID



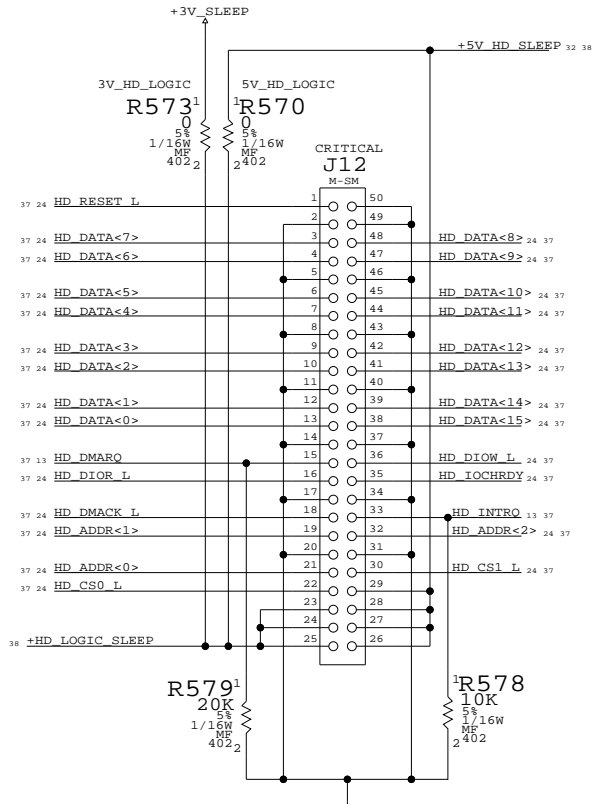
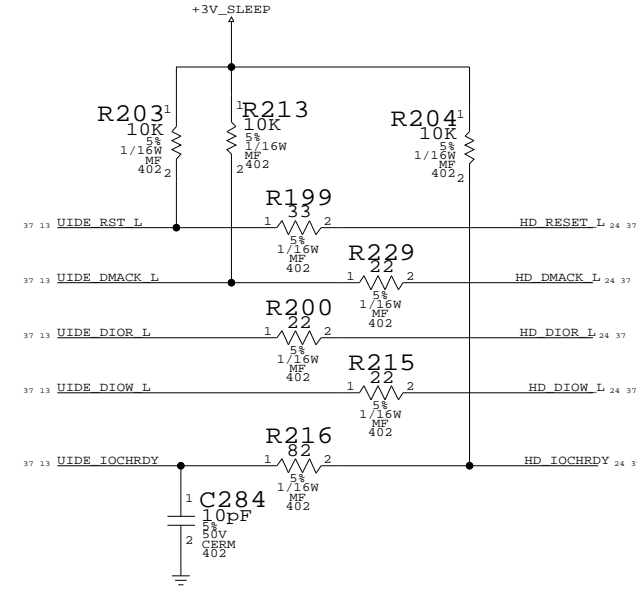
#### OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID



ANY SEQUENCING REQUIREMENT BETWEEN +5V\_HD\_SLEEP AND +3V\_SLEEP

#### INTERNAL I/O CONNECTORS

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IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

8

7

6

5

4

3

2

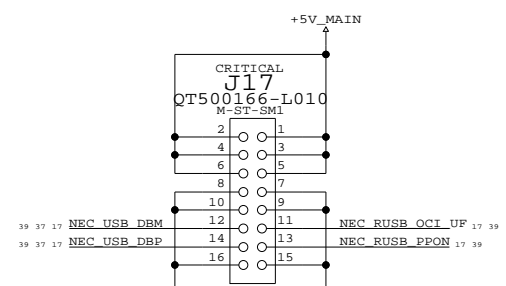
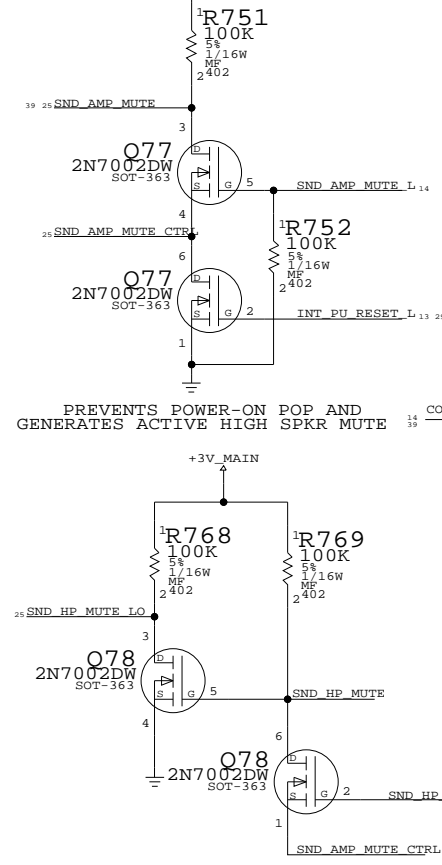
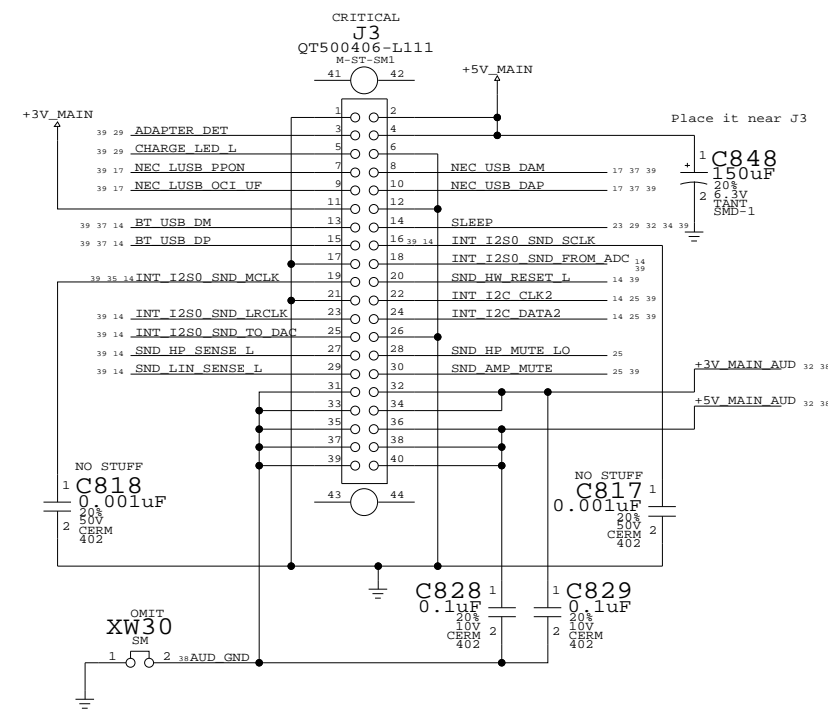
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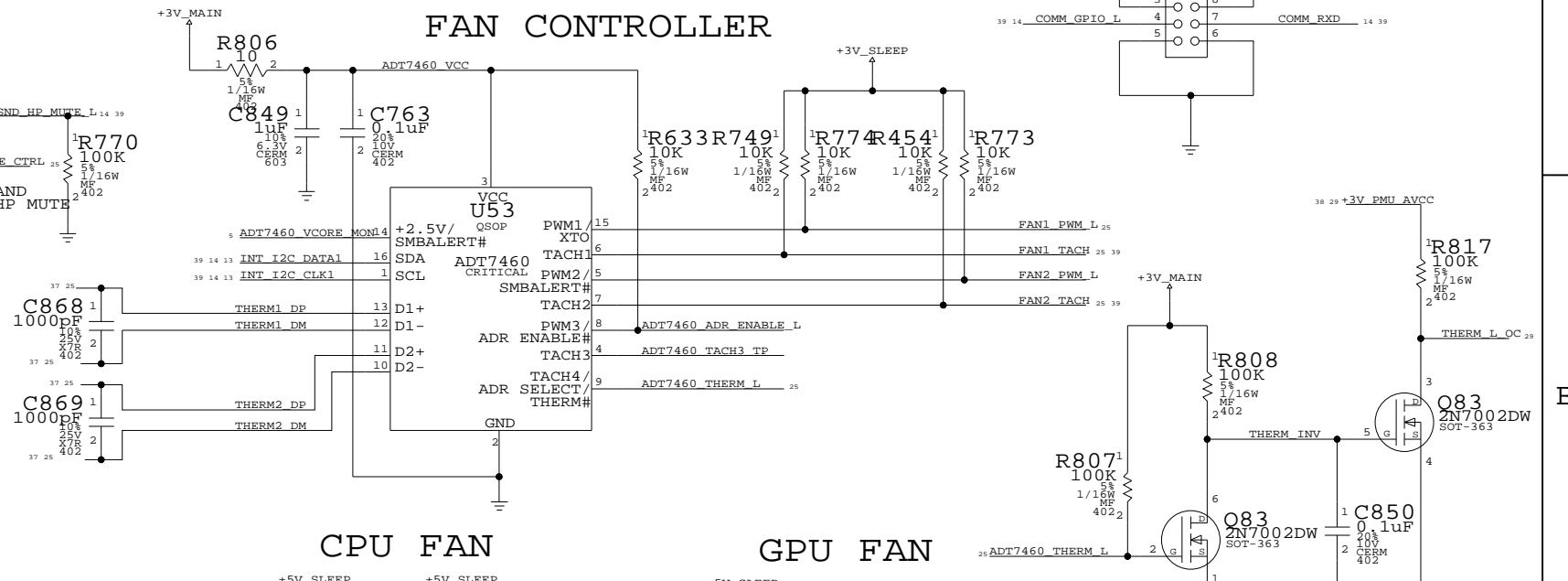
# LEFT I/O & AUDIO BOARD (LIO)

# USB MODEM/SOFT MODEM RIGHT USB BOARD



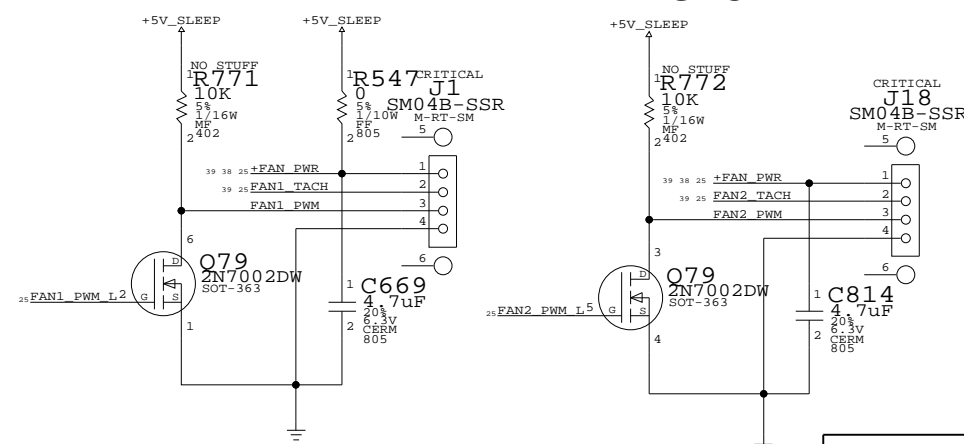
## FAN INTERFACE

### FAN CONTROLLER



### CPU FAN

### GPU FAN



### FAN/MODEM/SOUND/BACKUP BATT.

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D

C

B

A

D

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A

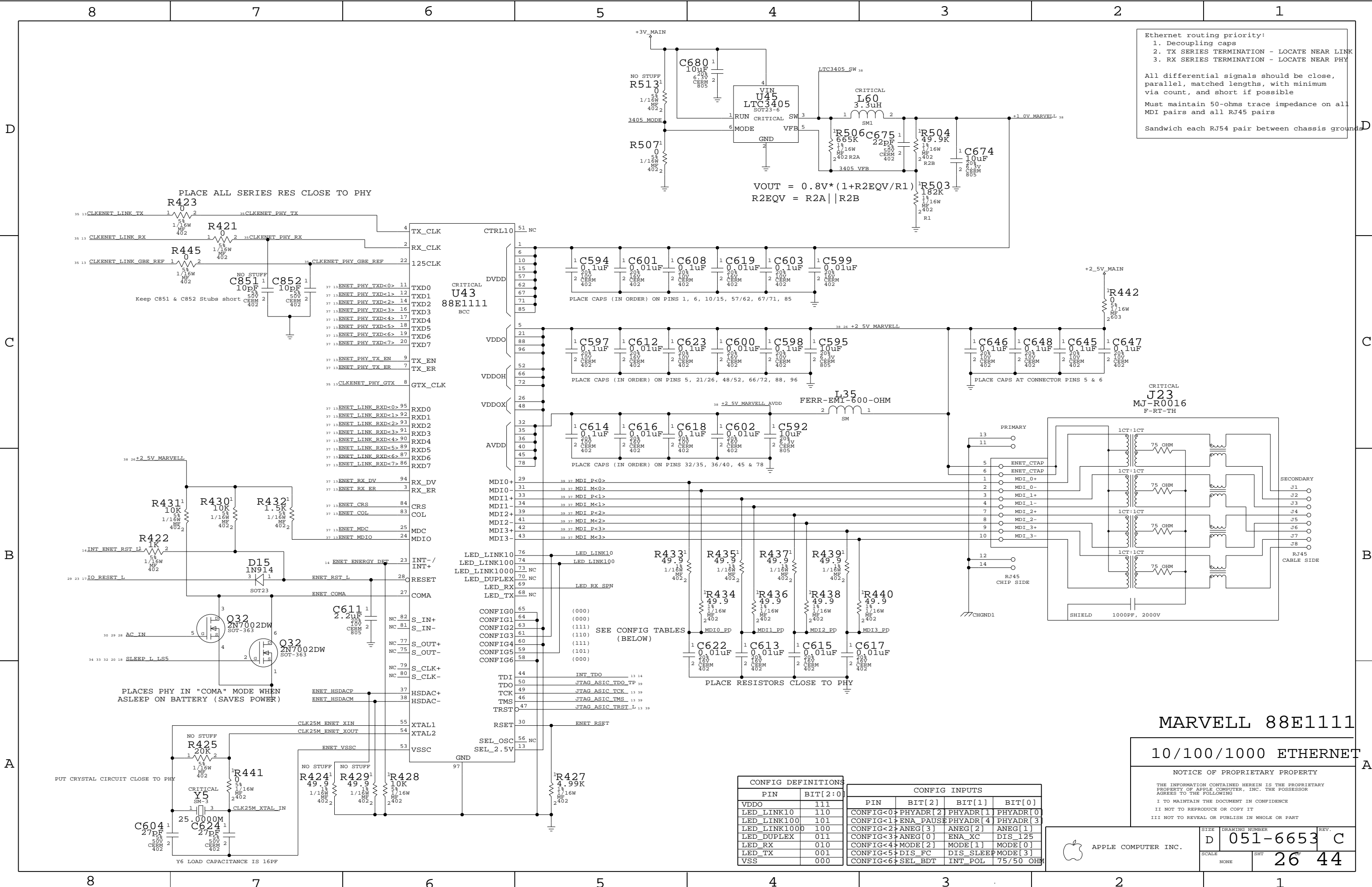
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Ethernet routing priority:  
 1. Decoupling caps  
 2. TX SERIES TERMINATION - LOCATE NEAR LINK  
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



$$V_{OUT} = 0.8V * (1 + R2EQV/R1)$$

$$R2EQV = R2A || R2B$$

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

PLACE ALL SERIES RES CLOSE TO PHY

Keep C851 & C852 Stubs short

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

CRITICAL U43 88E1111 BCC

### MARVELL 88E1111

### 10/100/1000 ETHERNET

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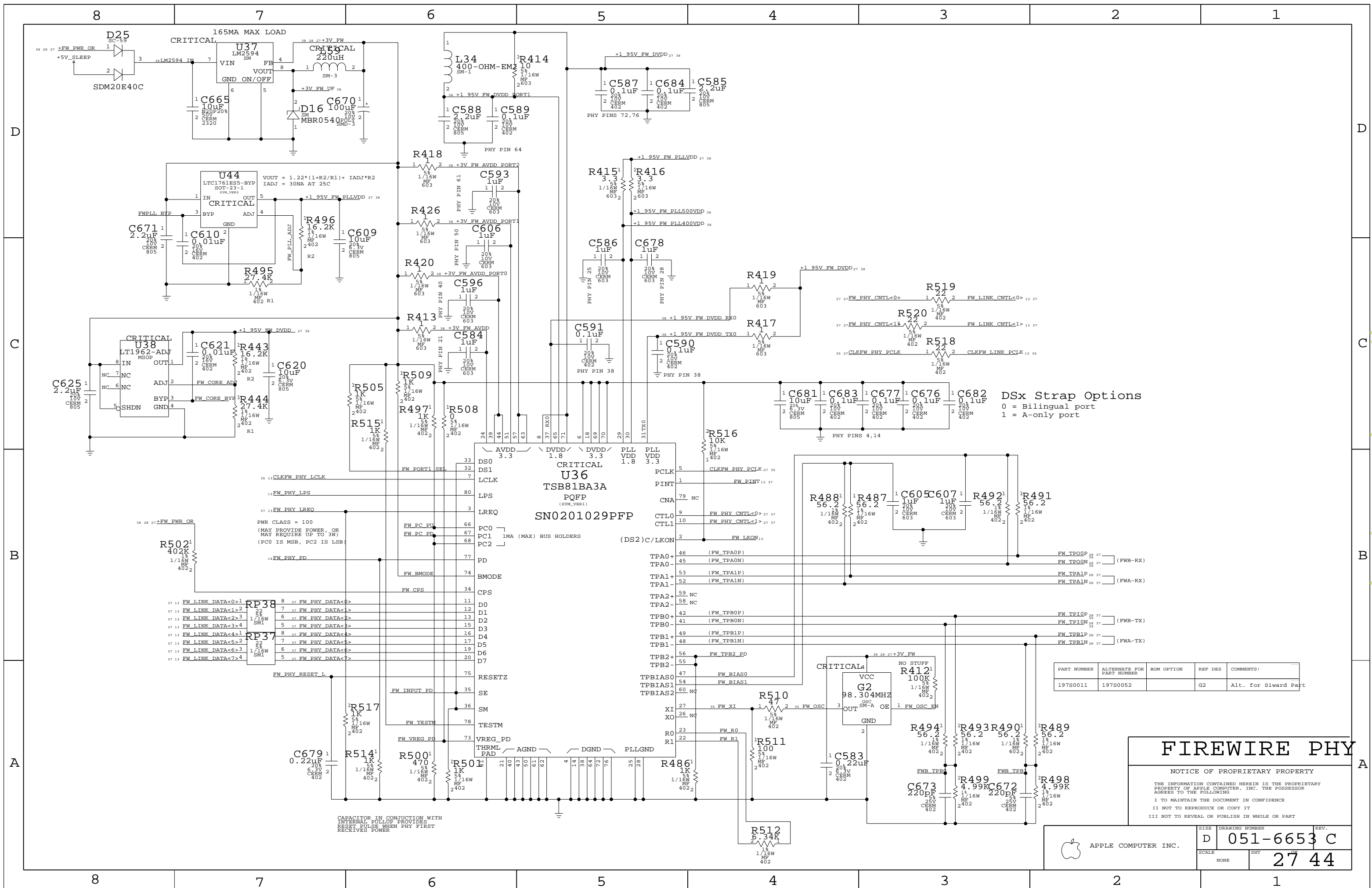
| CONFIG DEFINITIONS |          | CONFIG INPUTS |           |           |           |
|--------------------|----------|---------------|-----------|-----------|-----------|
| PIN                | BIT[2:0] | PIN           | BIT[2]    | BIT[1]    | BIT[0]    |
| VDDO               | 111      | CONFIG<0>     | PHYADR[2] | PHYADR[1] | PHYADR[0] |
| LED_LINK10         | 110      | CONFIG<1>     | ENA_PAUSE | PHYADR[4] | PHYADR[3] |
| LED_LINK100        | 101      | CONFIG<2>     | ANEG[3]   | ANEG[2]   | ANEG[1]   |
| LED_LINK1000       | 100      | CONFIG<3>     | ANEG[0]   | ENA_XC    | DIS_125   |
| LED_DUPLEX         | 011      | CONFIG<4>     | MODE[2]   | MODE[1]   | MODE[0]   |
| LED_RX             | 010      | CONFIG<5>     | DIS_FC    | DIS_SLEEP | MODE[3]   |
| LED_TX             | 001      | CONFIG<6>     | SEL_BDT   | INT_POL   | 75/50 OHM |
| VSS                | 000      |               |           |           |           |

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DSx Strap Options  
 0 = Bilingual port  
 1 = A-only port

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS            |
|-------------|---------------------------|------------|---------|---------------------|
| 197S0011    | 197S0052                  |            | G2      | Alt. for Sward Part |

**FIREWIRE PHY**

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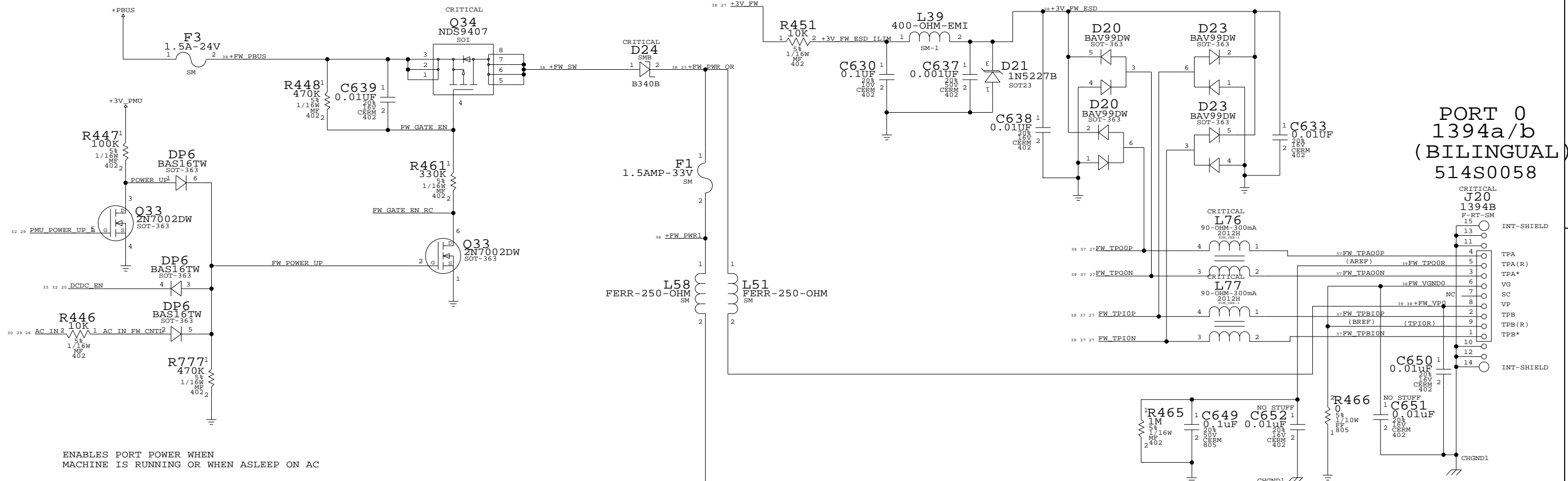
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|                     |       | 27             | 44   |

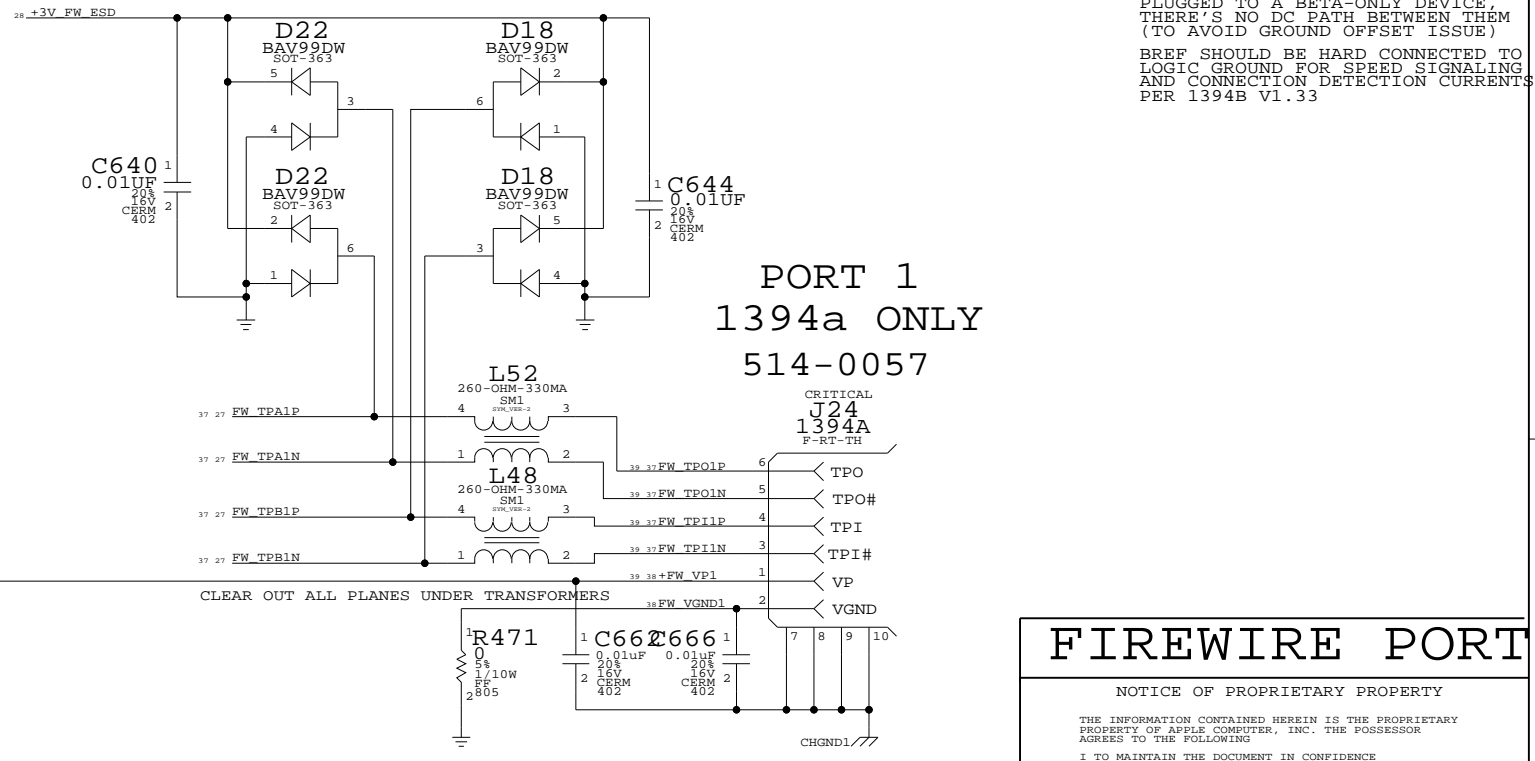
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# PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)  
BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33



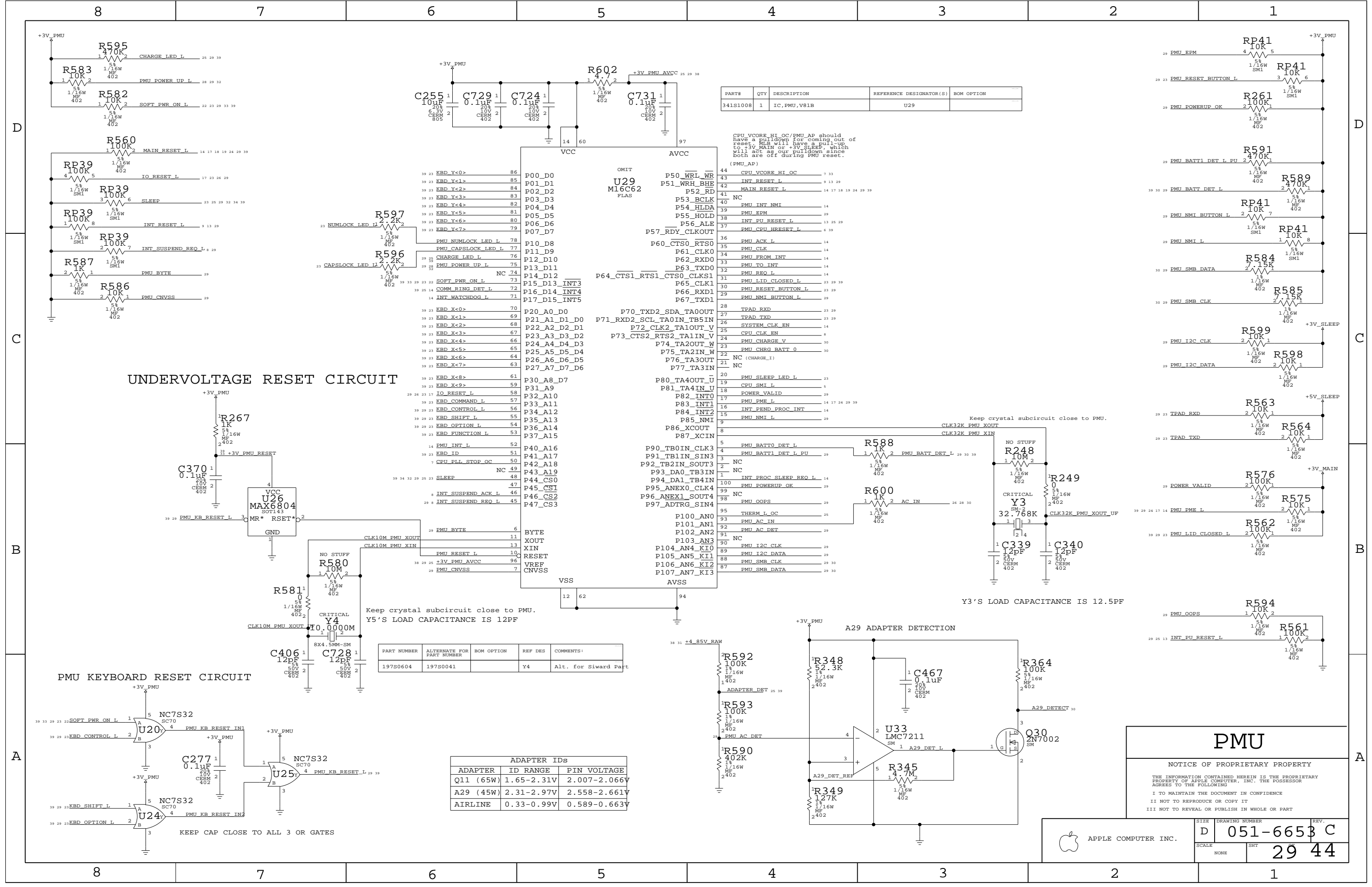
CLEAR OUT ALL PLANES UNDER TRANSFORMERS

## FIREWIRE PORTS

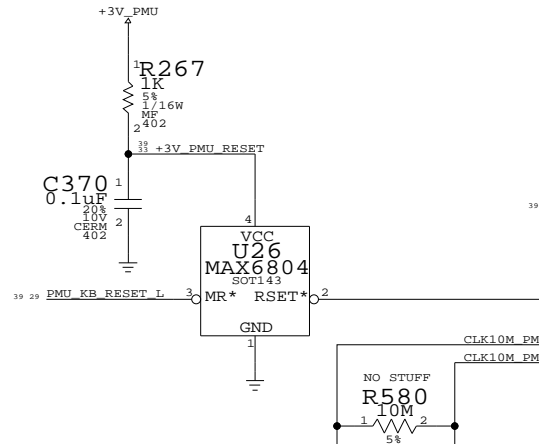
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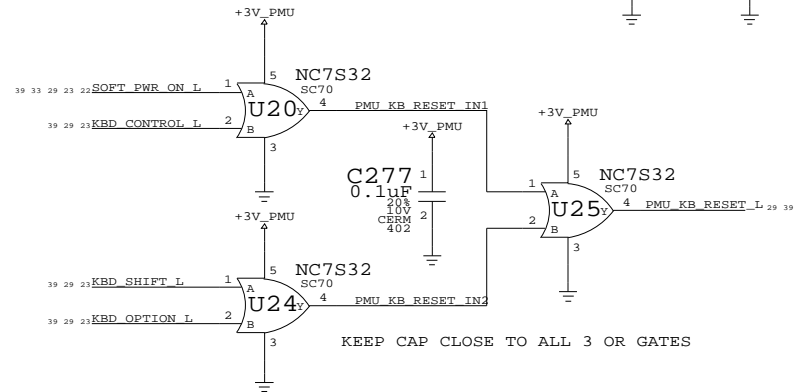
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UNDERVOLTAGE RESET CIRCUIT



PMU KEYBOARD RESET CIRCUIT



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS             |
|-------------|---------------------------|------------|---------|----------------------|
| 197S0604    | 197S0041                  |            | Y4      | Alt. for Siward Part |

| ADAPTER IDS |            |              |  |
|-------------|------------|--------------|--|
| ADAPTER     | ID RANGE   | PIN VOLTAGE  |  |
| Q11 (65W)   | 1.65-2.31V | 2.007-2.066V |  |
| A29 (45W)   | 2.31-2.97V | 2.558-2.661V |  |
| AIRLINE     | 0.33-0.99V | 0.589-0.663V |  |

| PART#    | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|-------------|-------------------------|------------|
| 341S1008 | 1   | IC,PMU,V81B | U29                     |            |

CPU VCORE\_HI\_OC/PMU\_AP should have a pulldown for coming out of reset. MBS will have a pull-up to +3V MAIN or +3V SLEEP, which will act as our pulldown since both are off during PMU reset.

(PMU\_AP)

| Pin | Signal       | Pin | Signal               |
|-----|--------------|-----|----------------------|
| 86  | P00_D0       | 44  | CPU VCORE_HI_OC      |
| 85  | P01_D1       | 43  | INT RESET L          |
| 84  | P02_D2       | 42  | MAIN RESET L         |
| 83  | P03_D3       | 41  | NC                   |
| 82  | P04_D4       | 40  | PMU INT NMI          |
| 81  | P05_D5       | 39  | PMU EPM              |
| 80  | P06_D6       | 38  | INT PU RESET L       |
| 79  | P07_D7       | 37  | PMU CPU HRESET L     |
| 78  | P10_D8       | 36  | PMU ACK L            |
| 77  | P11_D9       | 35  | PMU CLK              |
| 76  | P12_D10      | 34  | PMU FROM INT         |
| 75  | P13_D11      | 33  | PMU TO INT           |
| 74  | P14_D12      | 32  | PMU REQ L            |
| 73  | P15_D13_INT3 | 31  | PMU LID CLOSED L     |
| 72  | P16_D14_INT4 | 30  | PMU RESET BUTTON L   |
| 71  | P17_D15_INT5 | 29  | PMU NMI BUTTON L     |
| 70  | P20_A0_D0    | 28  | TPAD_RXD             |
| 69  | P21_A1_D1_D0 | 27  | TPAD_TXD             |
| 68  | P22_A2_D2_D1 | 26  | SYSTEM_CLK_EN        |
| 67  | P23_A3_D3_D2 | 25  | CPU_CLK_EN           |
| 66  | P24_A4_D4_D3 | 24  | PMU CHARGE V         |
| 65  | P25_A5_D5_D4 | 23  | PMU CHRG BATT 0      |
| 64  | P26_A6_D6_D5 | 22  | NC (CHARGE_1)        |
| 63  | P27_A7_D7_D6 | 21  | NC                   |
| 62  | P30_A8_D7    | 20  | PMU SLEEP_LED L      |
| 61  | P31_A9       | 19  | CPU_SMI L            |
| 60  | P32_A10      | 18  | POWER_VALID          |
| 59  | P33_A11      | 17  | PMU_PME L            |
| 58  | P34_A12      | 16  | INT_PEND_PROC_INT    |
| 57  | P35_A13      | 15  | PMU_NMI L            |
| 56  | P36_A14      | 14  | NC                   |
| 55  | P37_A15      | 13  | PMU_BATT0_DET L      |
| 54  | P40_A16      | 12  | PMU_BATT1_DET L_PU   |
| 53  | P41_A17      | 11  | NC                   |
| 52  | P42_A18      | 10  | NC                   |
| 51  | P43_A19      | 9   | INT_PROC_SLEEP_REQ L |
| 50  | P44_CS0      | 8   | PMU_POWERUP_OK       |
| 49  | P45_CSI      | 7   | NC                   |
| 48  | P46_CS2      | 6   | PMU_OOPS             |
| 47  | P47_CS3      | 5   | THERM_L_OC           |
| 46  | BYTE         | 4   | PMU_AC_IN            |
| 45  | XOUT         | 3   | PMU_AC_DET           |
| 44  | XIN          | 2   | NC                   |
| 43  | RESET        | 1   | PMU_I2C_CLK          |
| 42  | VREF         | 0   | PMU_I2C_DATA         |
| 41  | CNVSS        | 0   | PMU_SMB_CLK          |
| 40  |              | 0   | PMU_SMB_DATA         |
| 39  |              | 0   |                      |
| 38  |              | 0   |                      |
| 37  |              | 0   |                      |
| 36  |              | 0   |                      |
| 35  |              | 0   |                      |
| 34  |              | 0   |                      |
| 33  |              | 0   |                      |
| 32  |              | 0   |                      |
| 31  |              | 0   |                      |
| 30  |              | 0   |                      |
| 29  |              | 0   |                      |
| 28  |              | 0   |                      |
| 27  |              | 0   |                      |
| 26  |              | 0   |                      |
| 25  |              | 0   |                      |
| 24  |              | 0   |                      |
| 23  |              | 0   |                      |
| 22  |              | 0   |                      |
| 21  |              | 0   |                      |
| 20  |              | 0   |                      |
| 19  |              | 0   |                      |
| 18  |              | 0   |                      |
| 17  |              | 0   |                      |
| 16  |              | 0   |                      |
| 15  |              | 0   |                      |
| 14  |              | 0   |                      |
| 13  |              | 0   |                      |
| 12  |              | 0   |                      |
| 11  |              | 0   |                      |
| 10  |              | 0   |                      |
| 9   |              | 0   |                      |
| 8   |              | 0   |                      |
| 7   |              | 0   |                      |
| 6   |              | 0   |                      |
| 5   |              | 0   |                      |
| 4   |              | 0   |                      |
| 3   |              | 0   |                      |
| 2   |              | 0   |                      |
| 1   |              | 0   |                      |

Y3'S LOAD CAPACITANCE IS 12.5PF

PMU

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# DC POWER INPUT

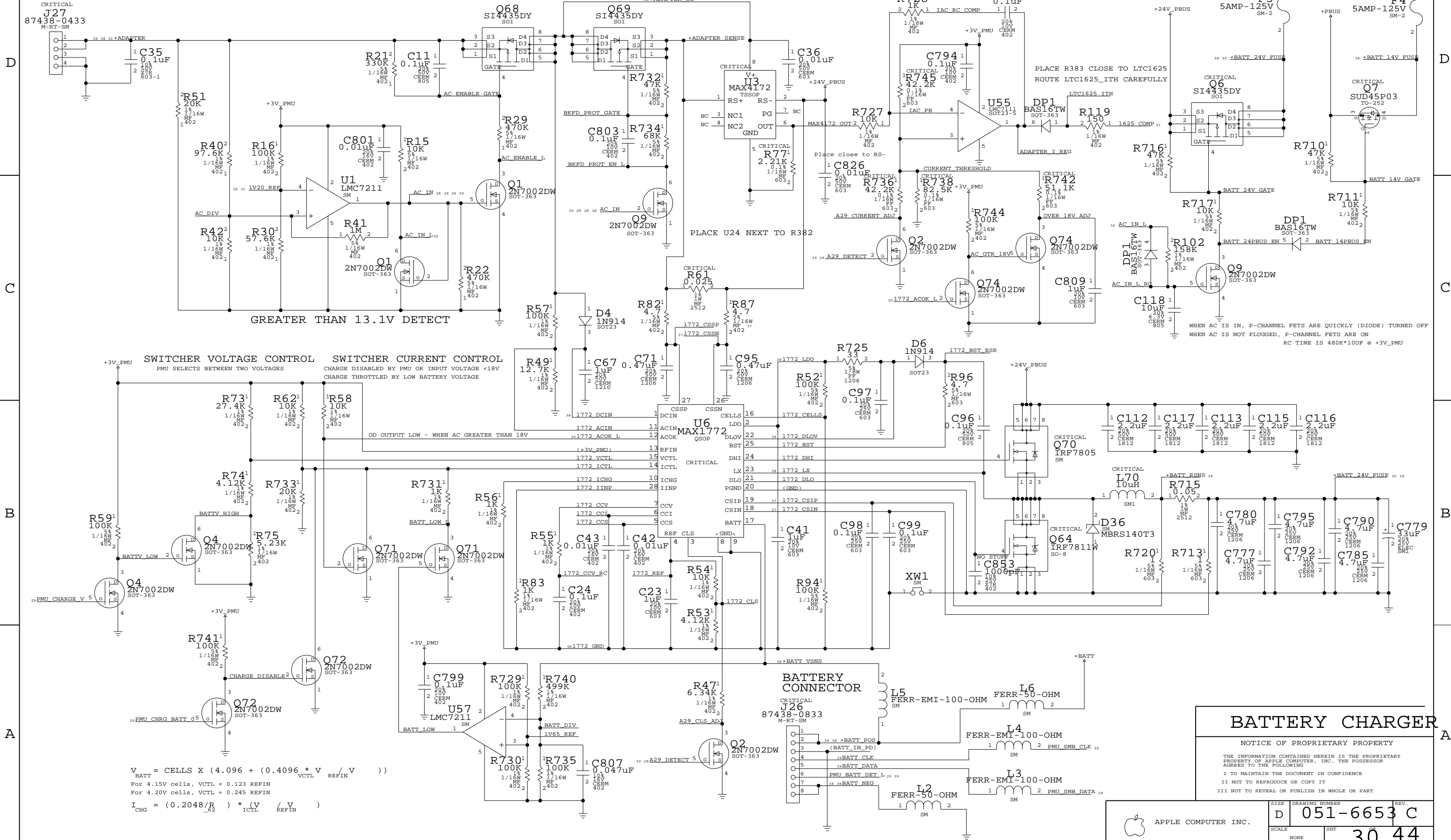
(POWER JACK, ETC. ON SEPARATE BOARD)

# DC INRUSH LIMITER

# BACKFEED PROTECTION

# +PBUS CURRENT LIMIT

# BATTERY SWITCH-OVER CIRCUIT



GREATER THAN 13.1V DETECT

PLACE U24 NEXT TO R382

PLACE R383 CLOSE TO LTC1625  
ROUTE LTC1625\_ITH CAREFULLY

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF  
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON  
RC TIME IS 480K\*10UF @ +3V\_PMU

$$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN  
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{G2}) * (V_{ICTL} / V_{REFIN})$$

## BATTERY CHARGER

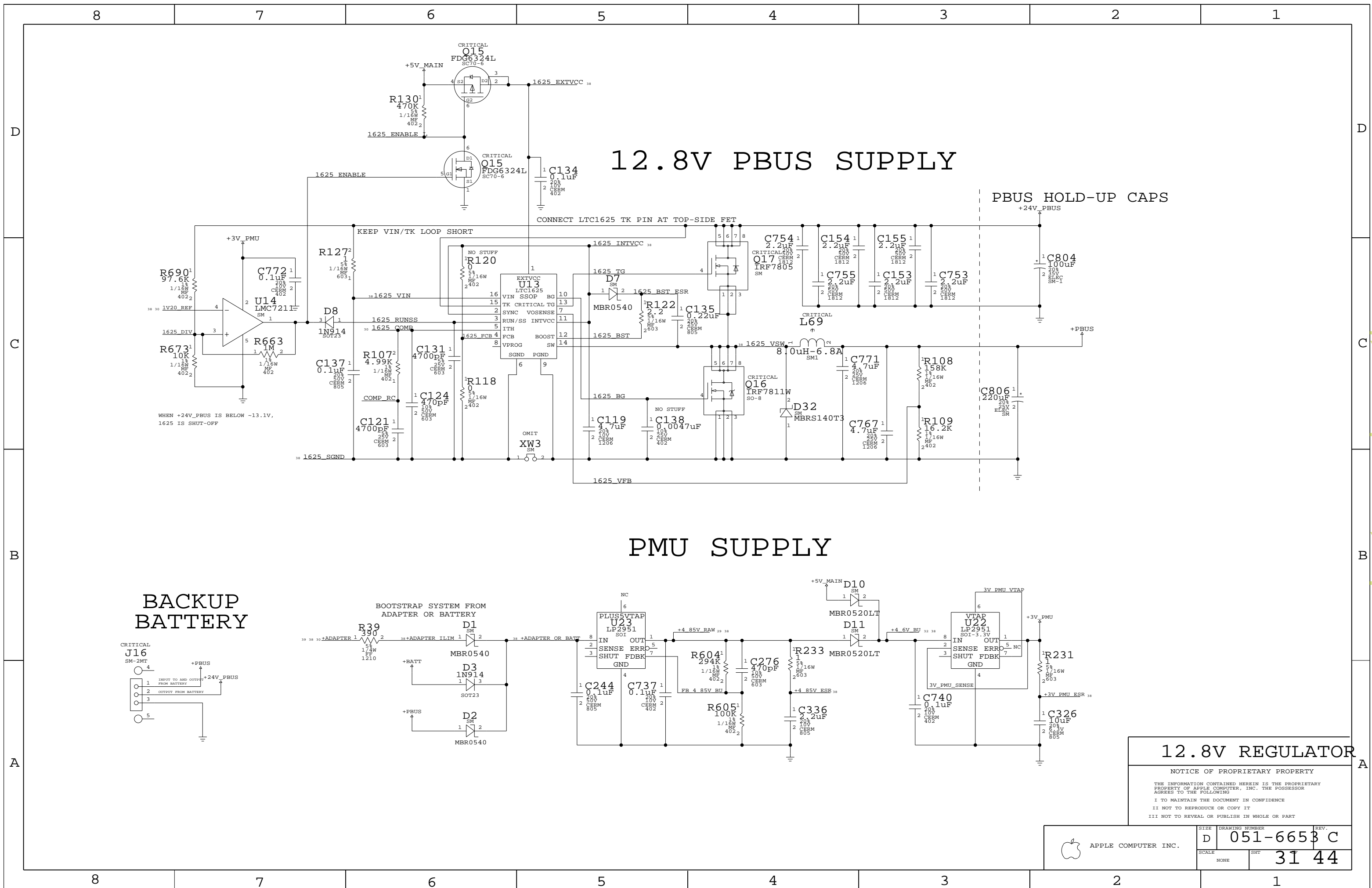
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# 12.8V PBus SUPPLY

# PMU SUPPLY

## BACKUP BATTERY

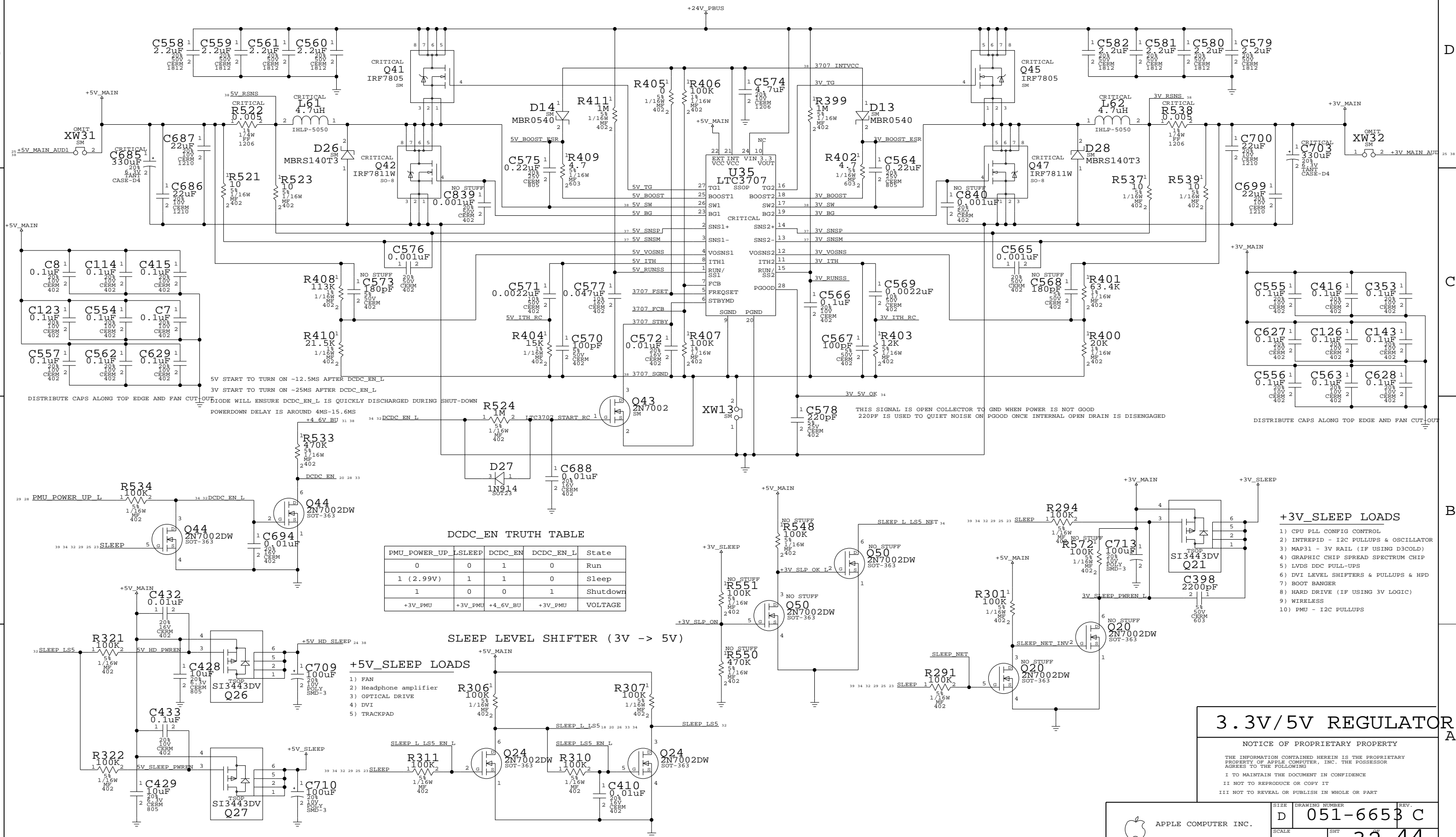
## 12.8V REGULATOR

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| SCALE               |      | SHT            |      |
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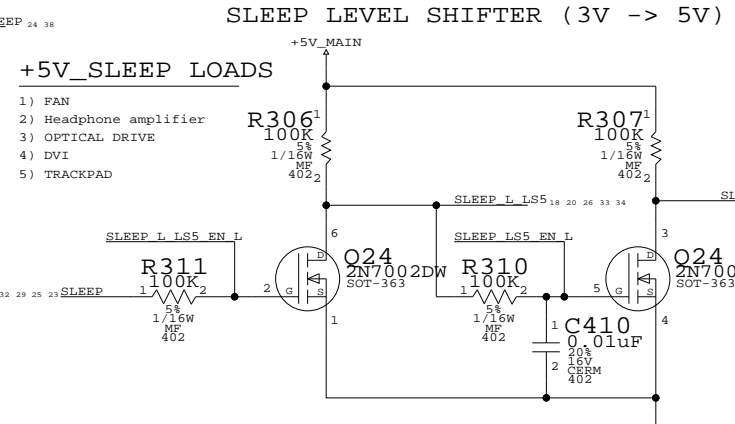
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# 3.3V/5V MAIN SUPPLY



**DCDC\_EN TRUTH TABLE**

| PMU_POWER_UP | LSLEEP  | DCDC_EN  | DCDC_EN_L | State    |
|--------------|---------|----------|-----------|----------|
| 0            | 0       | 1        | 0         | Run      |
| 1 (2.99V)    | 1       | 1        | 0         | Sleep    |
| 1            | 0       | 0        | 1         | Shutdown |
| +3V_PMU      | +3V_PMI | +4_6V_BU | +3V_PMU   | VOLTAGE  |



## 3.3V/5V REGULATOR

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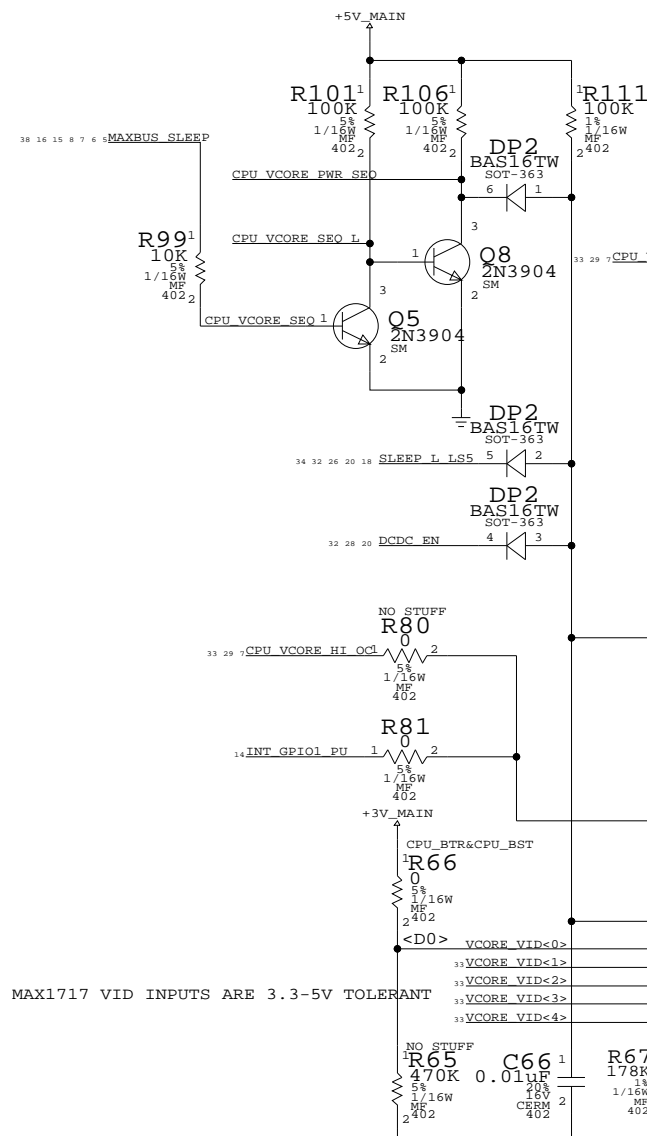
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|---------------------|------|----------------|------|
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| SCALE               | SHT  | 32 44          |      |
| NONE                |      |                |      |

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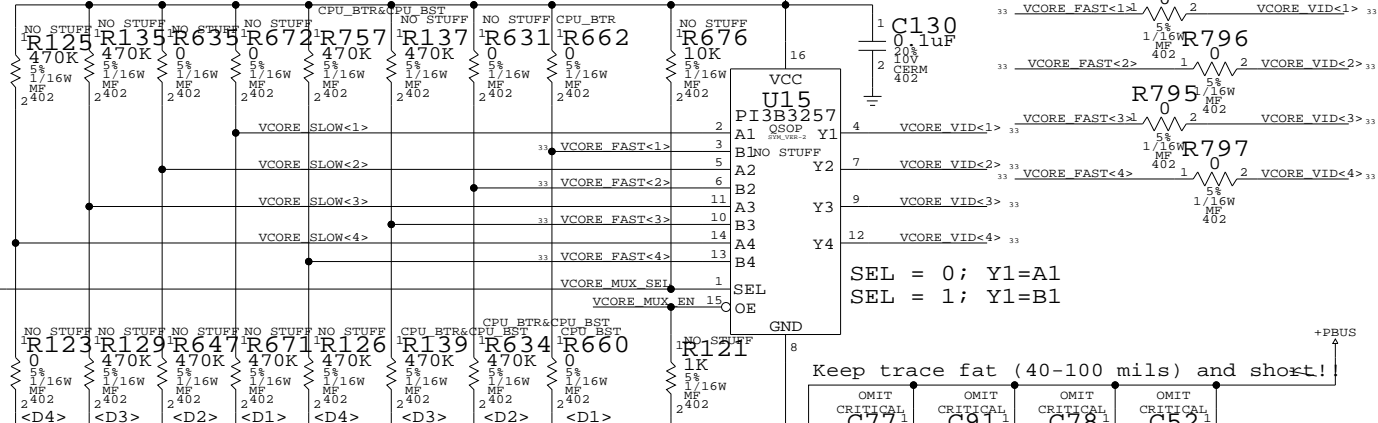
**VCORE POWER SEQUENCING**

CPU core follows CPU I/O voltage (approx. 7ms delay)



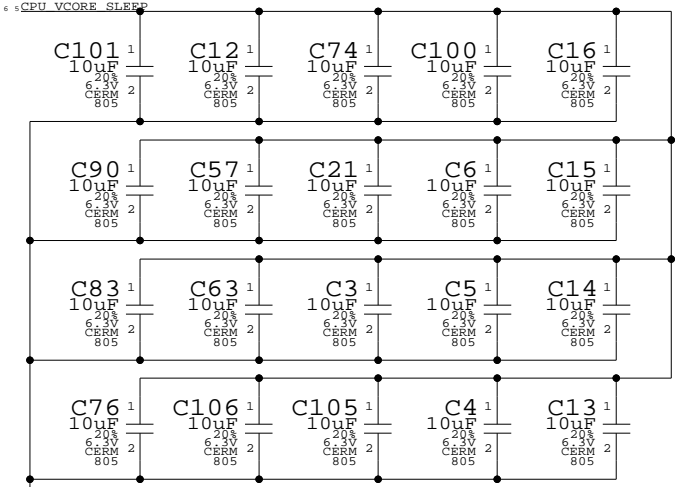
1.250V->0.975V 1.50Ghz  
1.200V->0.975V 1.33Ghz  
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support, R794,R795,R796&R797 have to be stuffed



Keep trace fat (40-100 mils) and short!!

| PART#    | QTY | DESCRIPTION  | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--|-------------------------|----------|------------|
| 126S0036 | 7   | CAP,AL,POLY,8.2uF,20%,16V,C51,C52,C77,C78,C91,C92,C111 |                         | CRITICAL |            |



**OUTPUT VOLTAGE**

| V <sub>DAC</sub> | D4=0   | D4=1 | D3 | D2 | D1 | D0 |
|------------------|--------|------|----|----|----|----|
| 2.00             | 1.275  | 0    | 0  | 0  | 0  | 0  |
| 1.95             | 1.250  | 0    | 0  | 0  | 0  | 1  |
| 1.90             | 1.225  | 0    | 0  | 0  | 1  | 0  |
| 1.85             | 1.200  | 0    | 0  | 0  | 1  | 1  |
| 1.80             | 1.175  | 0    | 1  | 0  | 0  | 0  |
| 1.75             | 1.150  | 0    | 1  | 0  | 1  | 0  |
| 1.70             | 1.125  | 0    | 1  | 1  | 0  | 0  |
| 1.65             | 1.100  | 0    | 1  | 1  | 1  | 0  |
| 1.60             | 1.075  | 1    | 0  | 0  | 0  | 0  |
| 1.55             | 1.050  | 1    | 0  | 0  | 1  | 0  |
| 1.50             | 1.025  | 1    | 0  | 1  | 0  | 0  |
| 1.45             | 1.000  | 1    | 0  | 1  | 1  | 0  |
| 1.40             | 0.975  | 1    | 1  | 0  | 0  | 0  |
| 1.35             | 0.950  | 1    | 1  | 1  | 0  | 0  |
| 1.30             | 0.925  | 1    | 1  | 1  | 1  | 0  |
| NO CPU           | NO CPU | 1    | 1  | 1  | 1  | 1  |

**FOR V-STEP:**

| D<4..0>    | A/B_ =  |         |
|------------|---------|---------|
|            | Hi/Fast | Lo/Slow |
| <= 1K PU   | 1       | 0       |
| >= 100K PU | 1       | 1       |
| >= 100K PD | 0       | 1       |
| <= 1K PD   | 0       | 0       |

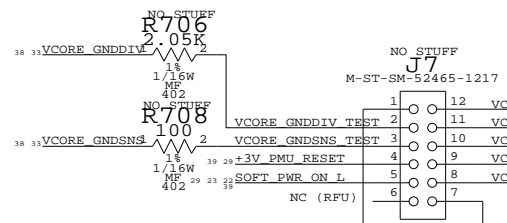
When A/B\_ is high (fast): D4-D0 read as-is  
When A/B\_ is low (slow): <=1K-ohm -> 0  
>=100K-ohm -> 1  
If all pull-ups are >=100K and all pull-downs are <=1K, A/V = V

**GROUND SENSE VOLTAGE DIVIDER**  
This allows for an offset to the ground sense to adjust the output voltage.  
VREF = 2.0V, HENCE VOFFSET = 2.0V \* 0.85 \* (Rb / Ra) AND VCORE = VDAC + VOFFSET.  
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)  
1.50Ghz 1.280V->0.990V  
1.33Ghz 1.220V->0.990V

| PART#    | QTY | DESCRIPTION                       | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-----------------------------------|-------------------------|----------|------------|
| 114S2003 | 1   | RES,MF,1/16W,2K OHM,1%,0402,SMD   | R97                     | ?        | CPU_BTR    |
| 114S5903 | 1   | RES,MF,1/16W,5.9K OHM,1%,0402,SMD | R93                     | ?        | CPU_BTR    |

**ROUTE AS DIFFERENTIAL PAIR Fmax Test Connections**



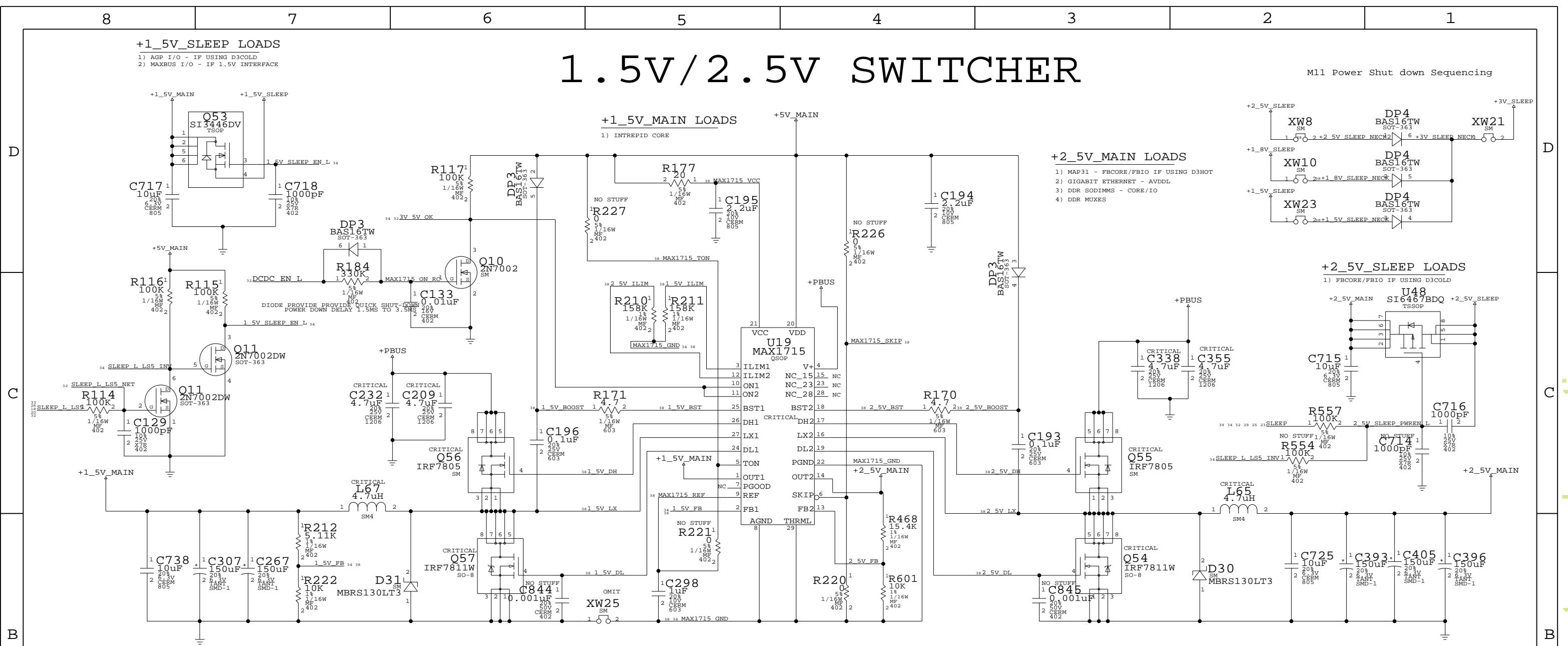
**VCORE SUPPLY**

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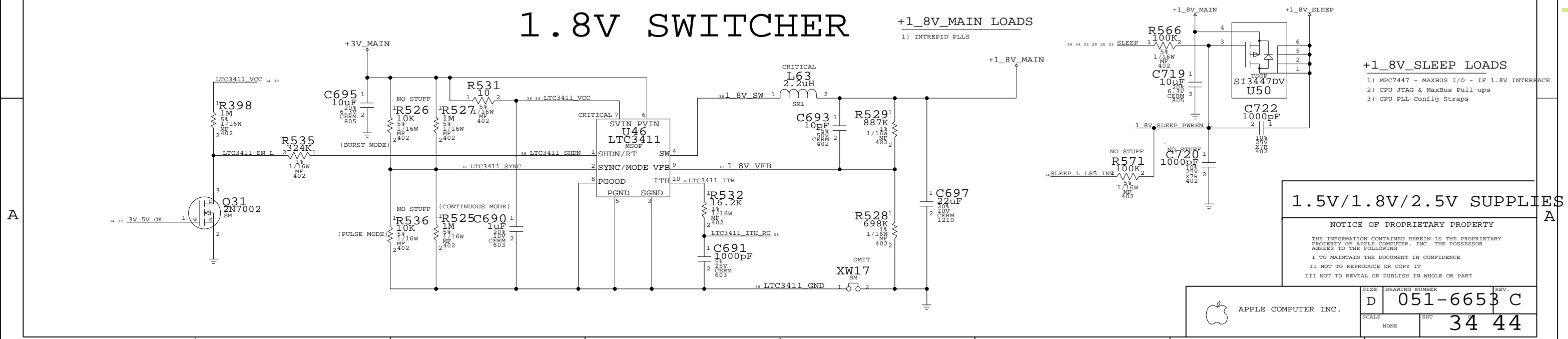
|                     |      |                |      |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-6653C      |      |
| SCALE               | SIT  | 33 44          |      |
| NONE                |      |                |      |

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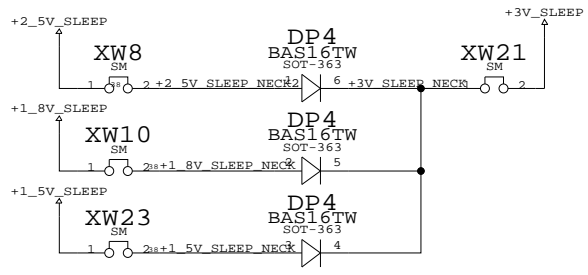
# 1.5V/2.5V SWITCHER



# 1.8V SWITCHER



M11 Power Shut down Sequencing



## +2.5V MAIN LOADS

- 1) MAP31 - FBCORE/FBIO IF USING D3HOT
- 2) GIGABIT ETHERNET - AVDDL
- 3) DDR SODIMMS - CORE/IO
- 4) DDR MUXES

## +2.5V SLEEP LOADS

- 1) FBCORE/FBIO IF USING D3COLD

## +1.8V MAIN LOADS

- 1) INTREPID PLLS

## +1.8V SLEEP LOADS

- 1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
- 2) CPU JTAG & MaxBus Pull-ups
- 3) CPU PLL Config Straps

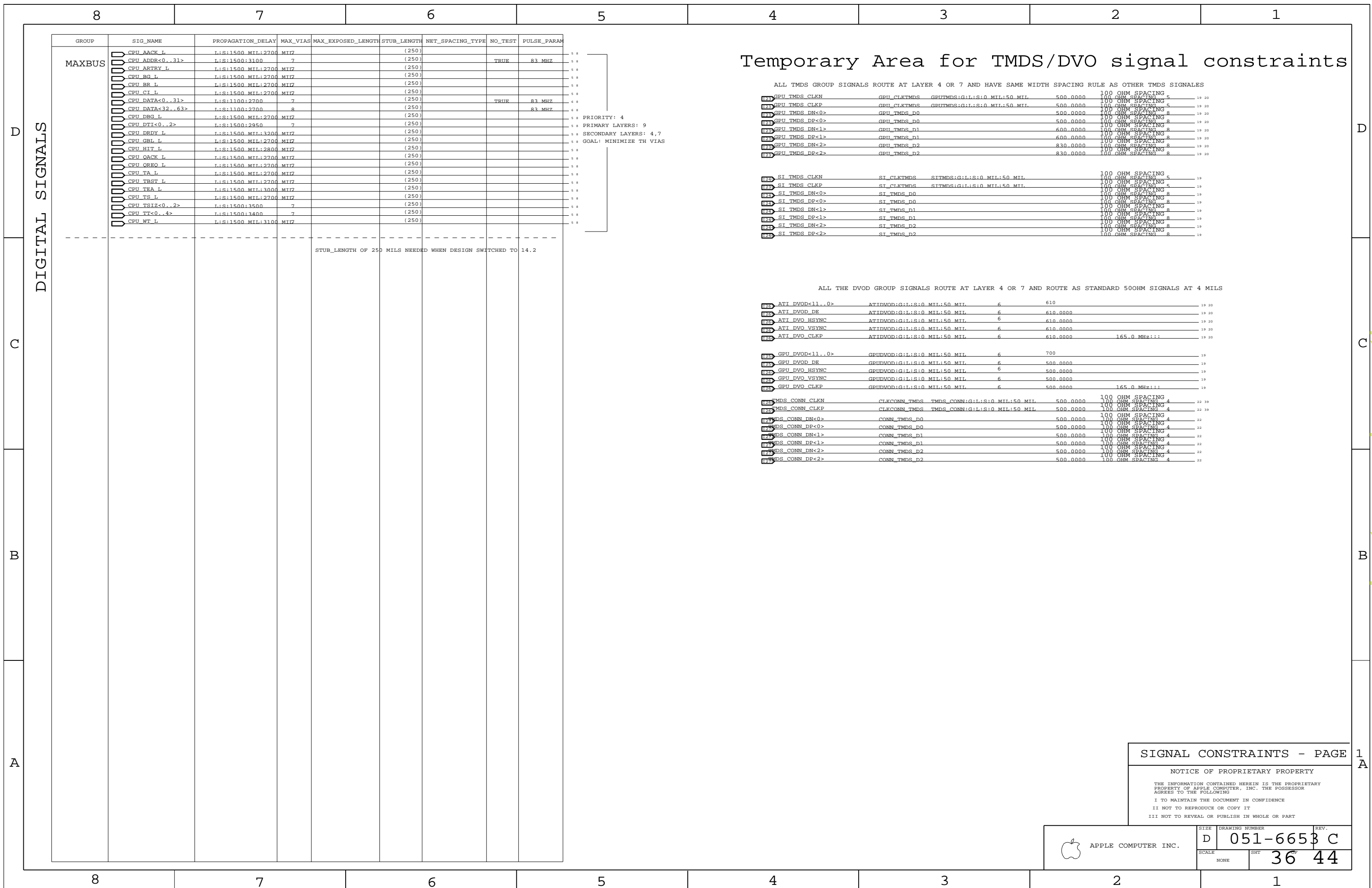
## 1.5V/1.8V/2.5V SUPPLIES

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|                     |      |                |       |
|---------------------|------|----------------|-------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.  |
|                     | D    | 051-6653       | C     |
| SCALE               | NONE | SHT            | 34 44 |

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DIGITAL SIGNALS

| GROUP  | SIG_NAME         | PROPAGATION_DELAY | MAX_VIAS | MAX_EXPOSED_LENGTH | STUB_LENGTH | NET_SPACING_TYPE | NO_TEST | PULSE_PARAM |
|--------|------------------|-------------------|----------|--------------------|-------------|------------------|---------|-------------|
| MAXBUS | CPU_AACK_L       | L:S:1500:MIL:2700 | MI17     | (250)              | (250)       |                  |         |             |
|        | CPU_ADDR<0..31>  | L:S:1500:3100     | 7        |                    | (250)       |                  | TRUE    | 83 MHZ      |
|        | CPU_ARTRY_L      | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_BG_L         | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_BR_L         | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_CI_L         | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_DATA<0..31>  | L:S:1100:2700     | 7        |                    | (250)       |                  | TRUE    | 83 MHZ      |
|        | CPU_DATA<32..63> | L:S:1100:2700     | 8        |                    | (250)       |                  |         |             |
|        | CPU_DBG_L        | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_DTI<0..2>    | L:S:1500:2950     | 7        |                    | (250)       |                  |         |             |
|        | CPU_DRDY_L       | L:S:1500:MIL:3200 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_GBL_L        | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_HIT_L        | L:S:1500:MIL:2800 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_OACK_L       | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_OREQ_L       | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_TA_L         | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_TBST_L       | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_TEA_L        | L:S:1500:MIL:3000 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_TS_L         | L:S:1500:MIL:2700 | MI17     |                    | (250)       |                  |         |             |
|        | CPU_TSIZ<0..2>   | L:S:1500:3500     | 7        |                    | (250)       |                  |         |             |
|        | CPU_TT<0..4>     | L:S:1500:3400     | 7        |                    | (250)       |                  |         |             |
|        | CPU_WT_L         | L:S:1500:MIL:3100 | MI17     |                    | (250)       |                  |         |             |

PRIORITY: 4  
PRIMARY LAYERS: 9  
SECONDARY LAYERS: 4,7  
GOAL: MINIMIZE TH VIAS

STUB\_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

## Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALS

| SIG_NAME       | PROPAGATION_DELAY | MAX_VIAS                    | MAX_EXPOSED_LENGTH | STUB_LENGTH     | NET_SPACING_TYPE | NO_TEST | PULSE_PARAM |
|----------------|-------------------|-----------------------------|--------------------|-----------------|------------------|---------|-------------|
| GPU_TMDS_CLKN  | GPU_CLKTMDS       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_CLKP  | GPU_CLKTMDS       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DN<0> | GPU_TMDS_D0       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DP<0> | GPU_TMDS_D0       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DN<1> | GPU_TMDS_D1       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 600.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DP<1> | GPU_TMDS_D1       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 600.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DN<2> | GPU_TMDS_D2       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 830.0000           | 100 OHM SPACING |                  |         |             |
| GPU_TMDS_DP<2> | GPU_TMDS_D2       | GPU_TMDS:G:L:S:0 MIL:50 MIL | 830.0000           | 100 OHM SPACING |                  |         |             |
| SI_TMDS_CLKN   | SI_CLKTMDS        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_CLKP   | SI_CLKTMDS        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DN<0>  | SI_TMDS_D0        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DP<0>  | SI_TMDS_D0        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DN<1>  | SI_TMDS_D1        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DP<1>  | SI_TMDS_D1        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DN<2>  | SI_TMDS_D2        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |
| SI_TMDS_DP<2>  | SI_TMDS_D2        | SI_TMDS:G:L:S:0 MIL:50 MIL  |                    | 100 OHM SPACING |                  |         |             |

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

| SIG_NAME        | PROPAGATION_DELAY           | MAX_VIAS                     | MAX_EXPOSED_LENGTH | STUB_LENGTH     | NET_SPACING_TYPE | NO_TEST | PULSE_PARAM  |
|-----------------|-----------------------------|------------------------------|--------------------|-----------------|------------------|---------|--------------|
| ATI_DVOD<1..0>  | ATI_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 610                |                 |                  |         |              |
| ATI_DVOD_DE     | ATI_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 610.0000           |                 |                  |         |              |
| ATI_DVO_HSYNC   | ATI_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 610.0000           |                 |                  |         |              |
| ATI_DVO_VSYNC   | ATI_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 610.0000           |                 |                  |         | 165.0 MHz::: |
| ATI_DVO_CLKP    | ATI_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 610.0000           |                 |                  |         |              |
| GPU_DVOD<1..0>  | GPU_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 700                |                 |                  |         |              |
| GPU_DVOD_DE     | GPU_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 500.0000           |                 |                  |         |              |
| GPU_DVO_HSYNC   | GPU_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 500.0000           |                 |                  |         |              |
| GPU_DVO_VSYNC   | GPU_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 500.0000           |                 |                  |         | 165.0 MHz::: |
| GPU_DVO_CLKP    | GPU_DVOD:G:L:S:0 MIL:50 MIL | 6                            | 500.0000           |                 |                  |         |              |
| TMDS_CONN_CLKN  | CLKCONN_TMDS                | TMDS_CONN:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_CLKP  | CLKCONN_TMDS                | TMDS_CONN:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DN<0> | CONN_TMDS_D0                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DP<0> | CONN_TMDS_D0                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DN<1> | CONN_TMDS_D1                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DP<1> | CONN_TMDS_D1                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DN<2> | CONN_TMDS_D2                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |
| TMDS_CONN_DP<2> | CONN_TMDS_D2                | CONN_TMDS:G:L:S:0 MIL:50 MIL | 500.0000           | 100 OHM SPACING |                  |         |              |

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|---------------------|-------|----------------|------|
| APPLE COMPUTER INC. | SCALE | DRAWING NUMBER | REV. |
|                     | NONE  | D 051-6653 C   |      |
|                     | SHT   | 36             | 44   |

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Digital Signals (cont'd)

Differential Signals

Table with columns: GROUP, SIG\_NAME, PROPAGATION\_DELAY, MAX\_VIA, MAX\_EXPOSED\_LENGTH, SUB\_LENGTH, NET\_SPACING\_TYPE, NO\_TEST, PULSE\_PARAMS. Includes sections for AGP, PCI, ULTRA ATA-100, EIDE INTREPID, OPTICAL, ETHERNET MI, and FIREWIRE MI.

Table with columns: GROUP, SIG\_NAME, DIFFERENTIAL\_PAIR, RELATIVE\_PROPAGATION\_DELAY, MAX\_EXPOSED\_LENGTH, NET\_SPACING\_TYPE, MAX\_VIAS. Includes sections for FIREWIRE, ETHERNET, LVDS, TMDS, USB 1, USB 2, POWER SUPPLIES, and THERMOSTAT.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS
Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

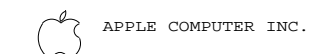
Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, TOTAL SHEETS. Values: D, 051-6653, C, NONE, 37, 44.



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# FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.  
 FUNC\_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC\_QTY IS FOR REFERENCE AND  
 LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.  
 FUNC\_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

| GROUP           | SIG_NAME              | FUNC_TEST | FUNC_QTY | FUNC_DIST  |
|-----------------|-----------------------|-----------|----------|------------|
| SCAN/TEST       | JTAG ASIC TMS         | TRUE      |          | 13 26      |
|                 | JTAG ASIC TDI         | TRUE      |          | 13         |
|                 | JTAG ASIC TDO TP      | TRUE      |          | 13 26      |
|                 | JTAG ASIC TCK         | TRUE      |          | 13 26      |
|                 | JTAG ASIC TRST L      | TRUE      |          | 13 26      |
|                 | CPU_CHKSTP_OUT L      | TRUE      |          | 5          |
|                 | CPU_SRESET L          | TRUE      |          | 5          |
|                 | CPU_HRESET L          | TRUE      |          | 5 6 7      |
|                 | JTAG_CPU_TMS          | TRUE      |          | 5 6        |
|                 | JTAG_CPU_TDI          | TRUE      |          | 5 6        |
|                 | JTAG_CPU_TDO TP       | TRUE      |          | 5          |
|                 | JTAG_CPU_TCK          | TRUE      |          | 5 6        |
|                 | JTAG_CPU_TRST L       | TRUE      |          | 5 6        |
|                 | INT_JTAG_TPI          | TRUE      |          | 13         |
|                 | INT_TST_MONIN_PD      | TRUE      |          | 13         |
|                 | INT_TST_MONOUT_TP     | TRUE      |          | 13         |
|                 | INT_TST_PLEN_PD       | TRUE      |          | 13         |
|                 | INT_I2C_CLK0          | TRUE      |          | 6 11 13 23 |
|                 | INT_I2C_DATA0         | TRUE      |          | 6 11 13 23 |
|                 | INT_I2C_CLK1          | TRUE      |          | 13 14 25   |
| INT_I2C_DATA1   | TRUE                  |           | 13 14 25 |            |
| PWR/GND         | +PBUS                 | TRUE      |          | 38         |
|                 | +24V_PBUS             | TRUE      |          | 38         |
|                 | GPU_VCORE             | TRUE      |          | 19 20 38   |
|                 | 1778_VFB              | TRUE      |          | 20 38      |
|                 | CPU_VCORE_SLEEP       | TRUE      |          | 5 6 13 38  |
|                 | VCORE_FB              | TRUE      |          | 33 38      |
|                 | +1_8V_MAIN            | TRUE      |          | 38         |
|                 | +2_5V_MAIN            | TRUE      |          | 38         |
|                 | +5V_MAIN              | TRUE      | 2        | 38 39      |
|                 | +5V_SLEEP             | TRUE      | 2        | 38 39      |
| +3V_MAIN        | TRUE                  | 4         | 23 38    |            |
| CARDBUS         | +3V_PMU               | TRUE      |          | 38         |
|                 | CBUS_DET_1_L          | TRUE      |          | 2000       |
|                 | CBUS_DET_2_L          | TRUE      |          | 2000       |
|                 | TMDS_DM<0..2>         | TRUE      |          | 1000       |
|                 | TMDS_DP<0..2>         | TRUE      |          | 1000       |
|                 | TMDS_CONN_CLKN        | TRUE      |          | 1000       |
|                 | TMDS_CONN_CLKP        | TRUE      |          | 1000       |
|                 | VGA_R                 | TRUE      |          | 1000       |
|                 | VGA_G                 | TRUE      |          | 1000       |
|                 | VGA_B                 | TRUE      |          | 1000       |
| VGA_HSYNC       | TRUE                  |           | 1000     |            |
| VGA_VSYNC       | TRUE                  |           | 1000     |            |
| DVI_DDC_CLK_UF  | TRUE                  |           | 1000     |            |
| DVI_DDC_DATA_UF | TRUE                  |           | 1000     |            |
| DVI_HPD_UF      | TRUE                  |           | 1000     |            |
| +5V_DDC_SLEEP   | TRUE                  |           | 2000     |            |
| LVDS            | LVDS_L0N              | TRUE      |          | 1000       |
|                 | LVDS_L0P              | TRUE      |          | 1000       |
|                 | LVDS_L1N              | TRUE      |          | 1000       |
|                 | LVDS_L1P              | TRUE      |          | 1000       |
|                 | LVDS_L2N              | TRUE      |          | 1000       |
|                 | LVDS_L2P              | TRUE      |          | 1000       |
|                 | CLKLVDS_LN            | TRUE      |          | 1000       |
|                 | CLKLVDS_LP            | TRUE      |          | 1000       |
|                 | LVDS_DDC_CLK          | TRUE      |          | 1000       |
|                 | LVDS_DDC_DATA         | TRUE      |          | 1000       |
| INVERTER        | +3V_LCD               | TRUE      | 2        | 2000       |
|                 | +3V_SLEEP             | TRUE      | 2        | 2000       |
|                 | +14V_INV              | TRUE      |          | 2000       |
|                 | +5V_INV_SW            | TRUE      |          | 2000       |
|                 | BRIGHT_PWM            | TRUE      |          | 2000       |
|                 | INV_GND               | TRUE      |          | 2000       |
|                 | TV_C                  | TRUE      |          | 1000       |
|                 | TV_Y                  | TRUE      |          | 1000       |
|                 | TV_COMP               | TRUE      |          | 1000       |
|                 | TV_GND1               | TRUE      |          | 1000       |
| TV_GND2         | TRUE                  |           | 1000     |            |
| L10             | INT_I2S0_SND_TO_DAC   | TRUE      |          | 1000       |
|                 | INT_I2S0_SND_LRCLK    | TRUE      |          | 1000       |
|                 | INT_I2S0_SND_MCLK     | TRUE      |          | 1000       |
|                 | INT_I2S0_SND_SCLK     | TRUE      |          | 1000       |
|                 | INT_I2S0_SND_FROM_ADC | TRUE      |          | 1000       |
|                 | SND_HP_MUTE_L         | TRUE      |          | 1000       |
|                 | SND_HP_MUTE           | TRUE      |          | 1000       |
|                 | SND_HW_RESET_L        | TRUE      |          | 1000       |
|                 | SND_HP_SENSE_L        | TRUE      |          | 1000       |
|                 | SND_LIN_SENSE_L       | TRUE      |          | 1000       |
| INT_I2C_CLK2    | TRUE                  |           | 1000     |            |
| INT_I2C_DATA2   | TRUE                  |           | 1000     |            |
| ADAPTER_DET     | TRUE                  |           | 1000     |            |
| CHARGE_LED_L    | TRUE                  |           | 1000     |            |
| NEC_LUSB_OCI_UF | TRUE                  |           | 1000     |            |
| NEC_LUSB_PPON   | TRUE                  |           | 1000     |            |
| +5V_MAIN        | TRUE                  | 2         | 2000     |            |
| +5V_SLEEP       | TRUE                  | 2         | 2000     |            |
| +3V_SLEEP       | TRUE                  |           | 2000     |            |

| GROUP            | SIG_NAME                 | FUNC_TEST        | FUNC_QTY | FUNC_DIST |      |
|------------------|--------------------------|------------------|----------|-----------|------|
| USB              | NEC_USB_DAM              | TRUE             |          | 17 25 37  |      |
|                  | NEC_USB_DAP              | TRUE             |          | 17 25 37  |      |
|                  | NEC_USB_DBM              | TRUE             |          | 17 25 37  |      |
|                  | NEC_USB_DBP              | TRUE             |          | 17 25 37  |      |
|                  | BT_USB_DM                | TRUE             |          | 14 25 37  |      |
|                  | BT_USB_DP                | TRUE             |          | 14 25 37  |      |
|                  | MODEM_USB_DM             | TRUE             |          | 14 25 37  |      |
|                  | MODEM_USB_DP             | TRUE             |          | 14 25 37  |      |
|                  | NEC_RUSB_PPON            | TRUE             |          | 17 25     |      |
|                  | NEC_RUSB_OCI_UF          | TRUE             |          | 17 25     |      |
| RT. USB WIRELESS | PCI_AD<0..31>            | TRUE             |          | 1000      |      |
|                  | PCI_FRAME_L              | TRUE             |          | 1000      |      |
|                  | PCI_TRDY_L               | TRUE             |          | 1000      |      |
|                  | PCI_IRDY_L               | TRUE             |          | 1000      |      |
|                  | PCI_DEVSEL_L             | TRUE             |          | 1000      |      |
|                  | PCI_STOP_L               | TRUE             |          | 1000      |      |
|                  | PCI_PAR                  | TRUE             |          | 1000      |      |
|                  | AIRPORT_PCI_REO_L        | TRUE             |          | 1000      |      |
|                  | AIRPORT_PCI_GNT_L        | TRUE             |          | 1000      |      |
|                  | AIRPORT_PCI_INT_L        | TRUE             |          | 1000      |      |
| OPTICAL          | EIDE_OPTICAL_DATA<0..15> | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_DMA_RO      | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_READ_L      | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_DMAACK_L    | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_ADDR<0..2>  | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_CS0_L       | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_CS1_L       | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_RST_L       | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_WRL_L       | TRUE             |          | 2000      |      |
|                  | EIDE_OPTICAL_IOCHRDY     | TRUE             |          | 2000      |      |
| TRACKPAD         | EIDE_OPTICAL_INT         | TRUE             |          | 2000      |      |
|                  | +5V_TPAD_SLEEP           | TRUE             |          | 3000      |      |
|                  | TPAD_F_TXD               | TRUE             |          | 3000      |      |
|                  | TPAD_F_RXD               | TRUE             |          | 3000      |      |
|                  | LID_CLOSED_L             | TRUE             |          | 3000      |      |
|                  | +3V_HALL_EFFECT          | TRUE             |          | 3000      |      |
|                  | SOFT_PWR_ON_L            | TRUE             |          | 3000      |      |
|                  | COMM_RESET_L             | TRUE             |          | 4000      |      |
|                  | COMM_SHUTDOWN            | TRUE             |          | 4000      |      |
|                  | COMM_RING_DET_L          | TRUE             |          | 4000      |      |
| MODEM/SERIAL     | COMM_TXD_L               | TRUE             |          | 4000      |      |
|                  | COMM_TRXC                | TRUE             |          | 4000      |      |
|                  | COMM_GPIO_L              | TRUE             |          | 4000      |      |
|                  | COMM_DTR_L               | TRUE             |          | 4000      |      |
|                  | COMM_RTS_L               | TRUE             |          | 4000      |      |
|                  | COMM_RXD                 | TRUE             |          | 4000      |      |
|                  | KEYBOARD                 | KBD_ID           | TRUE     |           | 3000 |
|                  |                          | KBD_INTL         | TRUE     |           | 3000 |
|                  |                          | KBD_JIS          | TRUE     |           | 3000 |
|                  |                          | KBD_CAPSLOCK_LED | TRUE     |           | 3000 |
| KBD_NUMLOCK_LED  |                          | TRUE             |          | 3000      |      |
| KBD_FUNCTION_L   |                          | TRUE             |          | 3000      |      |
| KBD_COMMAND_L    |                          | TRUE             |          | 3000      |      |
| KBD_OPTION_L     |                          | TRUE             |          | 3000      |      |
| KBD_CONTROL_L    |                          | TRUE             |          | 3000      |      |
| KBD_SHIFT_L      |                          | TRUE             |          | 3000      |      |
| BATTERY          | KBD_X<0..9>              | TRUE             |          | 3000      |      |
|                  | KBD_Y<0..7>              | TRUE             |          | 3000      |      |
|                  | +BATT_POS                | TRUE             |          | 1000      |      |
|                  | BATT_NEG                 | TRUE             |          | 1000      |      |
|                  | BATT_CLK                 | TRUE             |          | 1000      |      |
|                  | BATT_DATA                | TRUE             |          | 1000      |      |
|                  | PMU_BATT_DET_L           | TRUE             |          | 1000      |      |
|                  | FANS                     | +FAN_PWR         | TRUE     |           | 3000 |
|                  |                          | FAN1_TACH        | TRUE     |           | 3000 |
|                  |                          | FAN2_TACH        | TRUE     |           | 3000 |
| FAN1_GND         |                          | TRUE             |          | 3000      |      |
| FAN2_GND         |                          | TRUE             |          | 3000      |      |
| ETHERNET         |                          | MDI_P<0..3>      | TRUE     |           | 1000 |
|                  |                          | MDI_M<0..3>      | TRUE     |           | 1000 |
| FIREWIRE         |                          | FW_TP00P         | TRUE     |           | 1000 |
|                  |                          | FW_TP00N         | TRUE     |           | 1000 |
|                  |                          | FW_TP00R         | TRUE     |           | 1000 |
|                  | FW_TP10P                 | TRUE             |          | 1000      |      |
|                  | FW_TP10N                 | TRUE             |          | 1000      |      |
|                  | FW_VGND                  | TRUE             |          | 1000      |      |

| GROUP            | SIG_NAME         | FUNC_TEST | FUNC_QTY                    | FUNC_DIST      |  |
|------------------|------------------|-----------|-----------------------------|----------------|--|
| FIREWIRE (CONT.) | FW_TP01P         | TRUE      |                             | 1000           |  |
|                  | FW_TP01N         | TRUE      |                             | 1000           |  |
|                  | FW_TP11P         | TRUE      |                             | 1000           |  |
|                  | FW_TP11N         | TRUE      |                             | 1000           |  |
|                  | +FW_VP1          | TRUE      |                             | 1000           |  |
|                  | FW_VGND          | TRUE      |                             | 1000           |  |
| DC PWR IN        | +ADAPTER         | TRUE      | 3 (100 MIL PROBE PREFERRED) | 1000           |  |
|                  |                  |           |                             |                |  |
| LMU/ALS          | ST7_SLEEP_LED_H  | TRUE      |                             | 23             |  |
|                  | PMU_SLEEP_LED    | TRUE      |                             | 23             |  |
|                  | PMU_LID_CLOSED_L | TRUE      |                             | 23 29          |  |
|                  | LMU_DETECT       | TRUE      |                             | 23             |  |
| MISC.            | SLEEP_LED        | TRUE      |                             | 23             |  |
|                  | PMU_KB_RESET_L   | TRUE      |                             | 29             |  |
|                  | SLEEP            | TRUE      |                             | 23 25 29 32 34 |  |
|                  | PMU_CPU_HRESET_L | TRUE      |                             | 6 29           |  |
|                  | BB_RESET_L       | TRUE      |                             | 6              |  |
|                  | +3V_PMU_RESET    | TRUE      |                             | 29 33          |  |
|                  |                  |           |                             |                |  |
|                  |                  |           |                             |                |  |
|                  |                  |           |                             |                |  |
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# REVISION HISTORY

## Proto/EVT Release

- 10/27/03 - 1. Schematic originated from Q16 MLB
- 11/10/03 - 1. Replace U56 symbol  
 2. Connect OVDDSENSE to MAXBUS\_SLEEP  
 3. Modify SWD, SRW1 and IAPRYO connection  
 4. Connect SWD Sense to CPU\_VCORE\_SLEEP (PAGE 5)  
 5. Connect SENSEVDD to CPU\_VCORE\_SLEEP  
 6. Connect SENSEGND to GND  
 7. Add 4 pos. 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271)  
 8. Connect TEMP\_ANODE and TEMP\_CATHODE to ADT7460  
 9. Modify CPU PLL config  
 10. Add 0 ohm resistor on CG\_FSEL Intrepid side(R450)  
 11. Replace U1 symbol  
 12. Change R743 from 2m ohm to 1m ohm  
 13. Change R744, C781, C788, C793, C797, C802 from 220uF to 330uF  
 14. Change R748 from 410 ohm to 10 ohm
- 12/01/03 - 1. Modify CPU\_VCORE setting.
- 12/02/03 - 1. Modify CPU\_BTR CPU\_VCORE VID setting
- 12/05/03 - 1. Add CPU\_VDDD LDO (Page 5)  
 2. Change Q45 and Q41 to IRF7805 (376S0035)  
 3. Change Q47 and Q42 to IRF7811W (376S0104)  
 4. Change R402 and R405 to 4.7ohm resistors  
 5. Connect INT\_TDO from Intrepid to Cypress Chip PD\* (U31)
- 12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust  
 2. Modify CPU\_VCORE setting to Motorola new spec  
 3. Modify LDO power sequence
- 12/16/03 - 1. Add 10K pull down for INT\_TDO on page 13
- 12/17/03 - 1. Change LDO Vin from +3V\_MAIN to +3V\_SLEEP  
 2. Connect INT\_TDO from Intrepid to Marvell 88E1111(U43)  
 3. Add R755,R756,R758,R759 for power rail

## DVT Release (Rev. 02)

- 01/30/04 - 1. Add Soft Modem(Pin#37) 10K pull-up at J15.7 (Pg 25)  
 2. Add Bom Table for R450 2.2k Ohm VCore Offset (Pg 33)
- 02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5)  
 2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

## DVT Release (Rev. 03)

- 02/12/04 - 1. CPU\_VCORE adjustment for V1.1 A7PM CPU (Pg 33)  
 2. CPU\_VDD adjustment for V1.1 A7PM CPU (Pg 3)  
 3. ATI INT\_TMDS Termination change to 0 ohm, Qty:8 (Pg 20)  
 4. AGP I/O VREF voltage divider change to both 1k ohm (Pg 12)

## DVT Release (Rev. 04)

- 02/13/04 - 1. INT. TMDS Termination change to 2\* 49.9ohm = 100ohm (Pg 20)

## PVT Release (Rev. A)

- 03/11/04 - 1. INT. TMDS Termination change to 2\* 75 ohm = 150ohm (except CLK pair) (Pg 20)  
 2. USB series termination near NEC PHY change to 47 ohm (Pg 17)

## PVT Release (Rev. A - 051-6570)

- 04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)

## Production Release (Rev. A - 051-6653)

- 04/09/04 - 1. Updated to Apollo 7PM rev 1.1.1 part numbers (Pg 5)  
 04/09/04 - 2. Updated to production BootROM part number (Pg 9)


## Production Release (Rev. B - 051-6653)

- 04/30/04 - 1. Updated to Fast Intrepid part for 6A ReadMacro Delay value (Pg 8-15)  
 04/30/04 - 2. Add ATI M11 A16 parts as alternative for A15 parts (Pg 19-21)  
 04/30/04 - 3. Use new VGA filter to remove ghost image on external VGA display (Pg 22)

## Production Release (Rev. C - 051-6653)

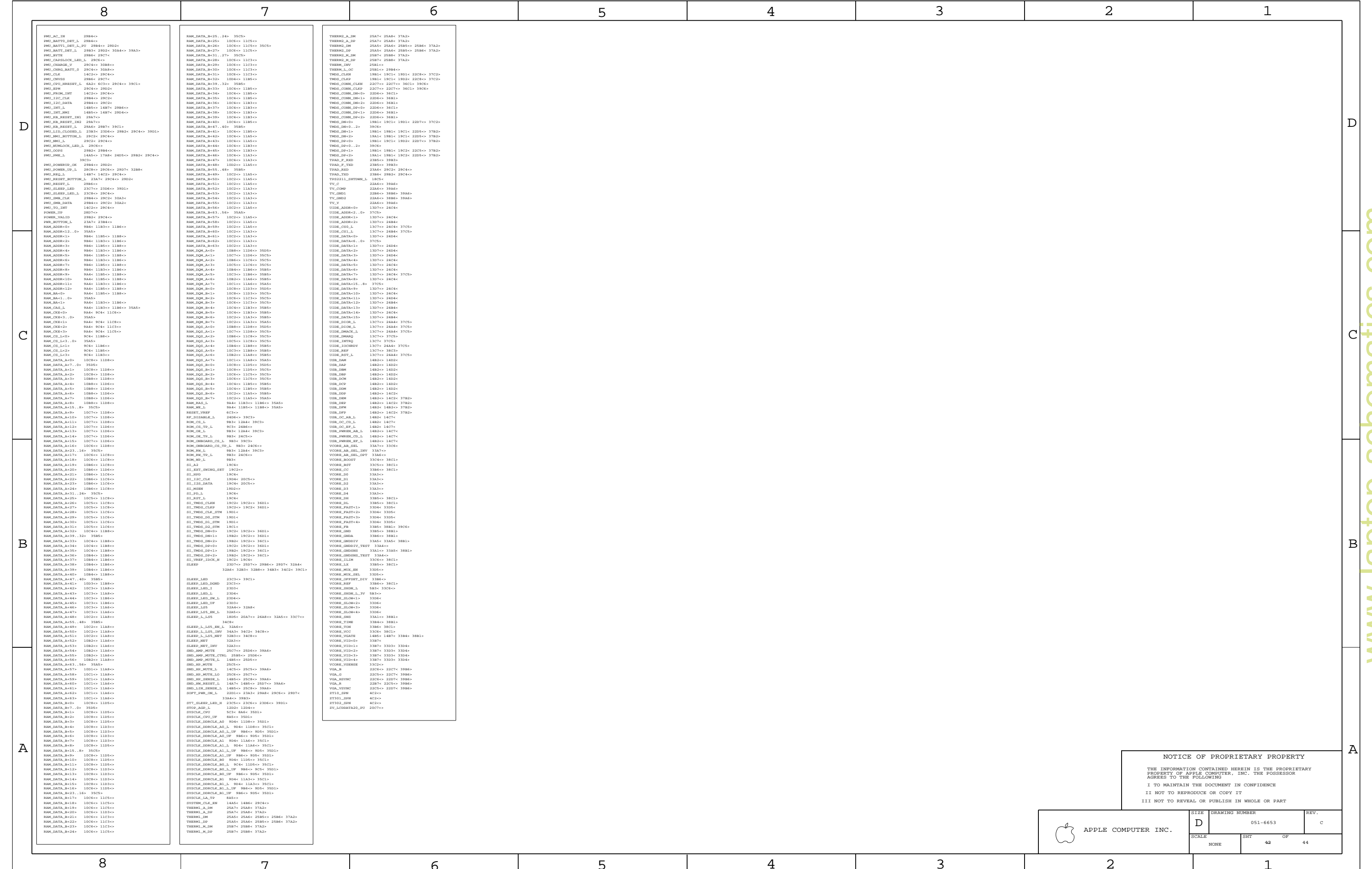
- 05/27/04 - 1. Updated BOM : 113S0006 -> 113S1000  
 05/27/04 - 2. Updated BOM : 132S0020 -> 132S0100

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