

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
B		35889	PRODUCTION RELEASED	01/07/05	

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SCHEM, AUDIO BRD, PB17"  
01/07/2005

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6752	1	SCHEM, AUDIO BRD, PB17	SCH1	
820-1733	1	PCBF, AUDIO BRD, PB17	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.																
XX :	_____																			
X.XX :	_____	<table border="1"> <tr> <td>DRAWER</td> <td>/</td> <td>DESIGN CK</td> <td>/</td> </tr> <tr> <td>ENG APPD</td> <td>/</td> <td>MFG APPD</td> <td>/</td> </tr> <tr> <td>QA APPD</td> <td>/</td> <td>DESIGNER</td> <td>/</td> </tr> <tr> <td>RELEASE</td> <td>/</td> <td>SCALE</td> <td>NONE</td> </tr> </table>	DRAWER	/	DESIGN CK	/	ENG APPD	/	MFG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	NONE	<b>NOTICE OF PROPRIETARY PROPERTY</b> THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
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QA APPD	/	DESIGNER	/																	
RELEASE	/	SCALE	NONE																	
X.XXX :	_____																			
ANGLES :	_____	MATERIAL/FINISH NOTED AS APPLICABLE		TITLE <b>SCHEM, AUDIO BRD, PB17</b>																
DO NOT SCALE DRAWING		THIRD ANGLE PROJECTION 		DRAWING NUMBER <b>051-6752</b> REV. <b>B</b>																
		SIZE D		SHEET 1 OF 14																

# PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
 1/2 OZ CU THICKNESS: 0.7 MILS  
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
 DIELECTRIC: FR-4  
 LAYER COUNT: 12  
 SIGNAL TRACE WIDTH: 4 MILS  
 SIGNAL TRACE SPACING: 4 MILS  
 PREPREG THICKNESS: 2-3 MILS

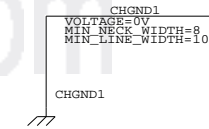
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

## BOARD STACK-UP AND CONSTRUCTION

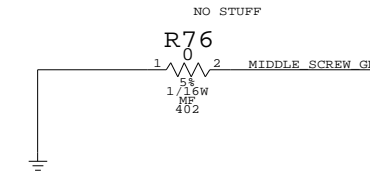
1	SIGNAL
2 PREPREG	GROUND
3 LAMINATE	SIGNAL
4 PREPREG	SIGNAL
5 LAMINATE	GROUND
6 PREPREG	CUT POWER PLANE
7 LAMINATE	CUT POWER PLANE
8 PREPREG	GROUND
9 LAMINATE	SIGNAL
10 PREPREG	SIGNAL
11 LAMINATE	GROUND
12 PREPREG	SIGNAL

## BOARD HOLES

PAD ON SLOT IN BETWEEN J4 AND J5 (LAYER 1 AND LAYER 12)



PAD ON MIDDLE HOLE (LAYER 1 AND LAYER 12)



## PCB BOARD STANDOFFS

### BOARD INFORMATION

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BLOCK DIAGRAM


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	SCALE NONE	SHET 3	OF 14

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REVISION NOTES

9/18/03  
 1) REMOVED R34 (PULLDOWN ON I2S1ERROR) ON SPDIF RECEIVER)  
 2) ADDED R37 AND R38 (100K 402) TO PUEDO-DIFF INPUT  
 3) CHANGED AUD\_SPDIF TO AUD\_SPDIF\_OUT ON U4 (CODEC)  
 4) CHANGED C23, C25, C28 TO 10UF SMB  
 5) ADDED C33||R41 AND C32||R40 AS RC FILTER BETWEEN LEFT AND INPUT AND OUTPUT OF U6, RESPECTIVELY  
 6) CHANGED R43 TO PULLDOWN ON MUTE INPUT TO U6 (SPEAKER AMP)  
 7) ADDED R39 AND R40 IN SERIES ON INPUTS TO U6  
 8) CHANGED AUD\_OUT\_AMP\_GND TO AUD\_AMP\_GND ON PGND OF U6  
 9) ADDED R56 (100K 402) AS PULLDOWN ON SHDN\_L ON U5  
 10) ADDED C35 (1UF 805) BETWEEN C1P AND C1N (CHARGE PUMP) OF U5  
 9/19/03  
 11) RE-PINNED J1  
 12) ADDED C36 AS BYPASS ON AUD\_5V\_PWRON1 AT U6 (SPEAKER AMP)  
 13) ADDED 0 OHM 402 BETWEEN I2S0\_MCLK AND AUD\_CODEC\_MCLK TO BYPASS U1 (NO STUFF)  
 14) ADDED L4-L23,C38-C39, AND C61-C68 FOR LINE IN HP OUT FILTER  
 15) ADDED D21 AND D22 ESD DIODES FOR LINE IN AND HP OUT  
 16) ADDED Q1, R58, R59,R61,R62,R68,R64,C71 AND C69 FOR HP ANALOG AND OPTICAL DETECT BUFFER  
 17) ADDED Q2, R63, R60,R67,R66,R65,R69,C72 AND C70 FOR LINE IN ANALOG AND OPTICAL DETECT BUFFER  
 18) ADDED C74,C73,C76,C75 10UF 10V CAPS IN PSEUDO-DIFF FILTER  
 9/19/03  
 19) FIXED MISSING CONNECTIONS IN HP AND LINE IN EMI FILTERS  
 20) ADDED ZT1 PLATED MOUNTING HOLE  
 21) MOVED CIRCUITS AROUND TO CONFORM TO HIERARCHY  
 9/22/03  
 22) CHANGED C20 AND C22 TO 10UF  
 23) ADDED C44 AS BYPASS ON OUTPUT OF 4.5V REGULATOR  
 24) ADDED R34 AS PULLDOWN ON SHDN\_L PIN OF U6 (SPEAKER AMP)  
 25) CHANGED J1 TO CORRECT CONNECTOR (514S0159)  
 9/24/03  
 26) REMOVED L9,L19, AND C68 ON OPTICAL IN PLUG DETECT  
 27) REMOVED U2,U1, AND U3 (SPDIF RECEIVER) AND ALL SURROUNDING COMPONENTS (PG 8)  
 28) MIRRORRED J1 (MLB CONNECTOR) TO CORRECT PINOUT  
 29) CORRECTED UNNAMED NETS IN LINE IN AND HP FILTERS  
 30) ADDED HEADPHONE CONNECTOR WITH OPTICAL TRANSMITTER (J4) 514-0137  
 31) ADDED LINE IN CONNECTOR (J5) 514-0061  
 9/25/03  
 32) REVERSED ALL CHANGES LISTED ABOVE ON 9/24/03  
 33) ADDED L27 AND L28 FOR POWER SUPPLY FILTERING ON U5 (HP AMP)  
 34) CHANGED L7,L8,L17,L18 TO 0402 1000OHM EMI FERRITES  
 35) ADDED L24, L25, AND L26 FOR INPUT FILTERING ON SPEAKER AMP INPUTS  
 36) CHANGED L9-L13 AND L19-L23 TO 1000OHM 0402 EMI FERRITES  
 37) UPDATED MLB CONNECTOR PINOUT  
 38) FIXED UNAMED NETS IN LINE IN (PG7) AND HP (PG6) EMI FILTERS  
 39) CHANGED MLB CONNECTOR (J1) FROM 516S0159 TO 516S0160 (CORRECTED FOR GENDER CONSISTENCY)  
 40) CHANGED R35,R36,R45,R46 TO 603 14 OHM FROM 805  
 9/26/03  
 41) FIXED MLB CONNECTOR PINT (MIRRORRED SYMBOL)  
 42) CHANGED ZT1 TO 195R106 PLATED THRU-HOLE  
 43) REMOVED C51-C54 FROM FILTERS ON SPEAKER AMP OUTPUTS  
 44) CHANGED MUTE INPUT OF U6 (SPEAKER AMP) FROM AUD\_5V\_PWRON1 TO AUD\_SPA\_MUTE  
 45) CHANGED L1 TO 0402 1000OHM EMI FERRITE  
 46) UPDATED SCHEMATIC CONSTRAINTS  
 9/27/03  
 47) MIRRORRED J1 (MLB CONNECTOR) TO FIX FLEX ROUTING  
 9/29/03  
 48) CHANGED C73-C76 TO 10UF ELECTROLYTIC 128S1010  
 49) CHANGED L2 AND L7-L26 TO 155S0137 TO CORRECT BOM PROBLEM  
 9/30/03  
 50) MOVED GND IN J1 TO IN BEWTEEN AUD\_LO\_DET\_L AND AUD\_LO\_METAL\_PLUG\_L  
 51) CHANGED C73-C76 TO 10UF SMB CAPS  
 52) ADDED PAGE 9 FOR FUNCTIONAL TEST POINTS  
 53) CORRECTED PINOUT OF J4 AND J5 FOR NEW CONNECTORS  
 54) CORRECTED OPTICAL/METAL DETECT PINOUT FOR J4 AND J5  
 10/1/03  
 55) ADDED MISSING LINE WIDTH CONSTRAINTS ON HP OUTPUT NETS  
 56) REPACKAGED TO PULL IN UPDATED FOOTPRINT FOR U5 (ADDED THERMAL VIAS)  
 57) CHANGED R52-R55 FROM 14K 1% TO 10K 1%  
 58) REMOVED XW1  
 59) CHANGED AUG\_GND ON DAC FILTER TO AUD\_AMP\_STARGND  
 60) CHANGED AUD\_GND ON C49 TO AUD\_AMP\_STARGND  
 61) CHANGED GND ON HP AMP (U5) TO AUD\_AMP\_STARGND  
 62) REMOVED Q2 AND R62 FROM AUD\_LO\_METAL\_PLUG\_L CIRCUIT  
 63) REMOVED Q2 AND R65 FROM AUD\_LI\_METAL\_PLUG\_L CIRCUIT  
 64) CHANGED AUD\_AMP\_GND ON XW4 TO AUD\_AMP\_STARGND  
 65) CHANGED AUD\_AMP\_GND TO AUD\_AMP\_STARGND ON J3  
 66) REPACKAGE TO PULL IN UPDATED I/O CONNECTOR SYMBOLS  
 67) CHANGED AUD\_GND TO AUD\_CODEC\_GND ON XW6  
 68) CHANGED MIN\_NECK\_WIDTH PROPERTIES TO BE DIFFERENT THAN MIN\_LINE\_WIDTH  
 69) CHANGED MIN\_LINE\_WIDTH TO 10 AND MIN\_NECK\_WIDTH TO 8 ON AUD\_5V\_PWRON1\_HPAMP\_PVDD  
 10/3/03  
 70) REMOVED Q1 AND R58 TO CORRECT SENSE OF AUDIO\_LO\_DET\_L  
 71) MOVED R67 TO AUD\_IN\_METAL SIDE OF R63 TO AVOID DIVIDER ON OUTPUT  
 72) MOVED R69 TO AUD\_IN\_FIBER SIDE OF R66 TO AVOID DIVIDER ON OUTPUT  
 73) MOVED R61 TO AUD\_OUT\_METAL SIDE OF R59 TO AVOID DIVIDER ON OUTPUT  
 74) MOVED R64 TO AUD\_OUT\_FIBER SIDE OF R64 TO AVOID DIVIDER ON OUTPUT  
 75) ADDED Q1 AND R58 TO CORRECT SENSE OF AUDIO\_LO\_DET\_L  
 76) ADDED Q1 AND R60 TO CORRECT SENSE OF AUDIO\_LI\_DET\_L  
 77) MOVED R67 TO AUDIO\_LI\_DET\_L SIDE OF R63 TO AVOID DIVIDER ON OUTPUT  
 78) MOVED R69 TO AUDIO\_LI\_METAL\_PLUG\_L SIDE OF R66 TO AVOID DIVIDER ON OUTPUT  
 79) MOVED R61 TO AUDIO\_LO\_DET\_L SIDE OF R59 TO AVOID DIVIDER ON OUTPUT  
 80) MOVED R64 TO AUDIO\_LO\_METAL\_PLUG\_L SIDE OF R64 TO AVOID DIVIDER ON OUTPUT  
 \*\*\* RELEASED FOR PROTO 1 \*\*\*

10/16/03  
 81) CHANGED U5 TO REFLECT UPDATED SYMBOL FOR MAX9722 (3X3)  
 10/27/03  
 82) ADDED R72-R75 TO SELECT POWER INPUT TO SPDIF TRANSMITTER AND RECEIVER  
 83) CHANGED VCC (PIN 2A) ON J4 (SPDIF TRANSMITTER) TO AUD\_SPDIF\_TRANS\_RUN  
 84) CHANGED VCC (PIN 1A) ON J5 (SPDIF RECEIVER) TO AUD\_SPDIF\_REC\_V\_RUN  
 85) CHANGED R44 TO 113S1470 FOR BOM CONSOLIDATION WITH LINK  
 86) CHANGED C37,C69,C71,C70,C72 TO 132S0045 FOR BOM CONSOLIDATION WITH LINK  
 10/31/03  
 87) REPACKAGED TO PULL IN UPDATED CONNECTOR FOOTPRINTS  
 11/4/03  
 88) ADDED MISSING CONSTRAINTS ON GND NETS  
 89) FIXED UNNAMED NETS  
 11/6/03  
 90) CHANGED C15 AND C16 TO 131S2723 TO REMOVE OEM PART FROM BOM  
 91) REMOVED ZT1 FROM SCHEMATIC TO IMPROVE GND HOLE TOLERANCE  
 92) ADDED R76 (NO STUFF) FOR OPTION OF GROUNDING MIDDLE SCREW HOLE TO FRAME  
 11/12/03  
 93) CHANGED J4 TO FINAL FOXCONN CONNECTOR (514-0140)  
 94) CHANGED J5 TO FINAL FOXCONN CONNECTOR (514-0144)  
 11/13/03  
 95) CHANGED C39,C39,C62,C64,C66,C68,C63,C65,C67,C61 FROM 603 100PF CERAMICS TO 402 100PF CERAMICS  
 96) ADDED Q2, R77, AND R78 TO ADJUST FOR PLUG DETECT SCHEME DIFFERENCE WITH NEW CONNECTORS  
 97) REMOVED L8, L7, L19, AND L23 IN T FILTERS BECAUSE SERIES R OF HIGHER VALUE MADE THEM REDUNDANT  
 98) ADDED C54 (1UF 603) TO VDD OF U6 AND MOVED C36 TO BETWEEN AUD\_5V\_PWRON1 AND AUD\_GND  
 99) CHANGED SGND (PIN 6) OF U5 TO AUD\_CODEC\_STARGND  
 100) CHANGED AUD\_AMP\_STARGND IN DAC FILTER TO AUD\_HP\_STARGND AND ADDED XW5 TO SHORT TO AUD\_GND  
 101) MOVED R63 TO INPUT SIDE OF R60 AND CHANGED TO 10K  
 102) MOVED R66 TO INPUT SIDE OF R78 AND CHANGED TO 10K  
 103) MOVED R59 TO INPUT SIDE OF R58 AND CHANGED TO 10K  
 104) MOVED R64 TO INPUT SIDE OF R77 AND CHANGED TO 10K  
 2/3/04  
 105) ADDED R81 AS 100K PULLUP TO AUD\_3V\_RUN ON U2 PIN 17 (AUDIO\_GPIO\_11)  
 2/4/04  
 106) CHANGED R80 TO NO STUFF TO REMOVE DIVIDER ON OUTPUT OF OPTICAL RECEIVER  
 107) CHANGED R74 TO NO STUFF AND R74 TO STUFFED TO CHANGE TO 3V3\_RUN FOR SPDIF RECEIVER  
 2/19/04  
 108) CHANGED R7 TO NO STUFF  
 3/14/04  
 109) REMOVED R72-R75 AS SPDIF OPTICS ARE 3V ONLY  
 110) CHANGED PIN 15 OF J1 TO AUD\_3V\_RUN  
 111) REMOVED R79 AND R80 TO REMOVED 5V SPDIF COMPATIBILITY  
 112) ADDED 22UF C55 AND C56 TO CLEAN UP AUD\_3V\_RUN FOR SPDIF  
 113) SWAPPED INPUTS TO SPEAKER AMP AFTER THE L'S TO CORRECT CHANNEL SWAP ERROR  
 114) FIXED NAMING CONFLICT ON PSEUDO-DIFF INPUT  
 6/8/04  
 115) CHANGED C73-C76 TO 10UF 10V 1206 TO SAVE SPACE IN PSEUDO-DIFF CIRCUIT  
 116) CHANGED C2 TO 0.02UF X5R 402, C7 TO 0.001UF 402, AND R1 TO 3K 5% 402 TO FIX SPDIF PLL FILTER  
 117) CHANGED AD1 INPUT ON SPDIF RCVR (U2) TO AUD\_3V\_RUN\_F TO CHANGE I2C ADDR TO 010  
 6/16/04  
 118) REARRANGED SCHEMATIC PAGES TO BE MORE DESIGN REUSE COMPLIANT  
 119) RENAMED POWER NETS TO BE DESIGN REUSE COMPLIANT  
 6/28/04  
 120) REASSIGNED CS4816 (U2) TO I2C ADDRESS 0X22 (AD=001) ON I2S-B BUS FOR Q41B/Q51 COMPATIBILITY  
 7/02/04  
 \*\*\*\* RELEASED FOR Q41B EVT  
 \*\*\*\*\*  
 \*\*\*\* SCHEMATIC UNDER Q41B PROJECT, NAME CHANGED TO SCHEM,CRYSTAL,Q41B  
 9/22/04  
 121> CHANGED PCM3052 TO PCM3052A WITH NEW FOOTPRINT  
 10/12/04  
 122> ADD 2 1KOHM FROM L AND R CHANNEL OUTPUT OF MAX9722 TO AUD\_GND  
 123> ADD 100KOHM ON PIN 15 OF CS8416 TO PULL-UP, NO STUFF THE PULL-DOWN  
 124> REPLACE R48, R49, R50, R51 WITH 20.5KOHM  
 125> CHANGE 2 FEEDBACK RESISTORS R41, R42 ON LM4866LQ TO 20.5OHM  
 126> CHANGE C42, C43 TO 0.1UF  
 127> CHANGE SPEAKER AMP TO NATIONAL SEMI. LM4866LQ  
 128> ADD MAX8510 AS LDO FOR CS8416  
 10/15/04  
 129> CHANGE SIGNAL: AUDIO\_GPIO\_11 TO SPDIF\_GPO0  
 130> CHANGE SIGNAL: AUDIO\_LO\_METAL\_PLUG\_L TO AUDIO\_LO\_OPTICAL\_PLUG\_L  
 131> CHANGE SIGNAL: AUDIO\_LI\_METAL\_PLUG\_L TO AUDIO\_LI\_OPTICAL\_PLUG\_L  
 \*\*\*\*\*  
 12/16/04  
 132> SCHEMATIC RELEASE FOR PRODUCTION  
 01/07/05  
 133> CHANGE ALL 138S0518 TO 138S0550  
 134> SCHEMATIC RELEASE FOR PRODUCTION (BOM REV B)

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	D	051-6752	B
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SIGNAL & POWER ALIASES

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# FUNCTIONAL TEST POINTS

	SIG_NAME	FUNC_TEST	FUNC_QTY	
101	AUDIO LO DET L	TRUE		7 10
102	AUDIO LO OPTICAL PLUG L	TRUE		7 10
103	AUDIO LI DET L	TRUE		7 11
104	AUDIO LI OPTICAL PLUG L	TRUE		7 11
105	I2S0 RESET L	TRUE		7 8
106	I2S1 RESET L	TRUE		7 12
107	PP3V3_RUN_AUDIO	TRUE		7 8 10 11 12
108	I2C_SDA	TRUE		7 8 12
109	I2C_SCL	TRUE		7 8 12
110	SLEEP_LED	TRUE		7
111	SLEEP_LED_GND	TRUE		7
112	I2S1_DEV_TO_SB_DTI	TRUE		7 12
113	I2S1_SYNC	TRUE		7 12
114	I2S1_BITCLK	TRUE		7 12
115	I2S0_DEV_TO_SB_DTI	TRUE		7 8
116	I2S0_SB_TO_DEV_DTO	TRUE		7 8
117	I2S0_BITCLK	TRUE		7 8 12
118	I2S0_MCLK	TRUE		7 12
119	AUDIO_SPKR_MUTE	TRUE		7 9
120	AUDIO_LO_MUTE_L	TRUE		7 10
121	AUDIO_EXT_MCLK_SEL	TRUE		7 12
122	SPDIF_GPO0	TRUE		7 12
123	AUD_GND	TRUE	4	7 8 9
124	PP5V_PWRON_AUDIO1	TRUE	3	7 9 10
125	PP5V_PWRON_AUDIO0	TRUE	3	7 8 12
		TRUE	3	7 8 12

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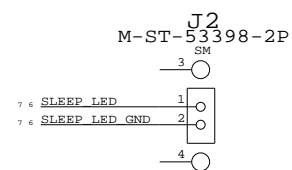
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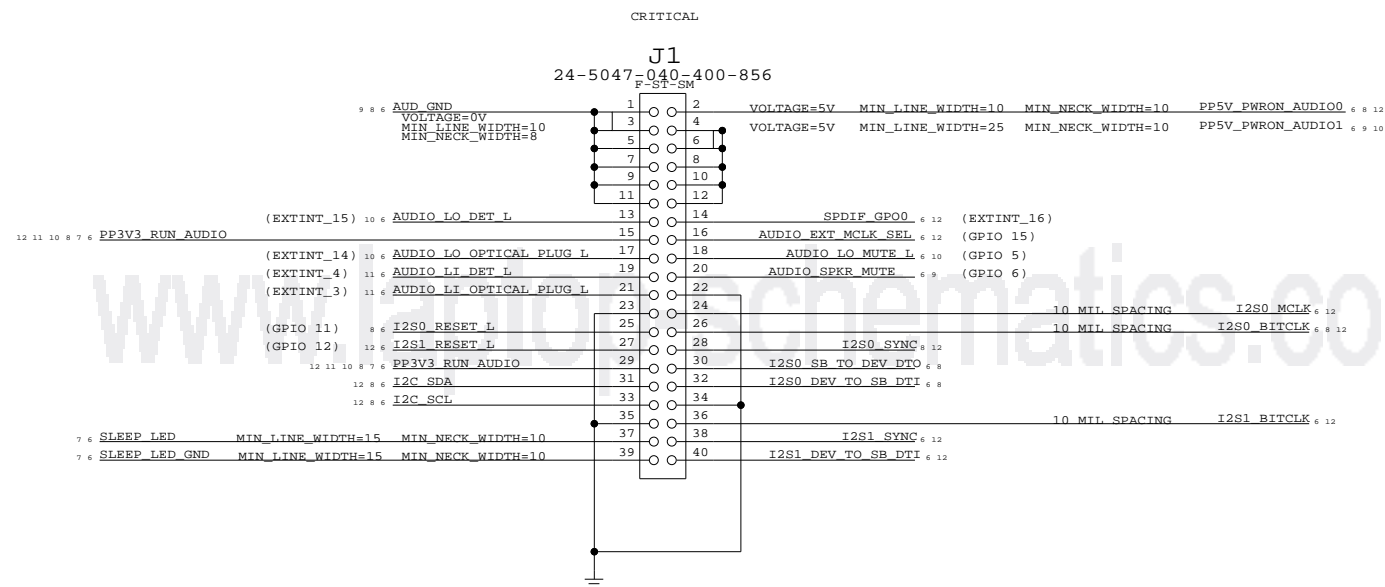
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### SLEEP LED CONNECTOR



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### AUDIO CONNECTOR (TO MLB)



### AUDIO CONNECTORS

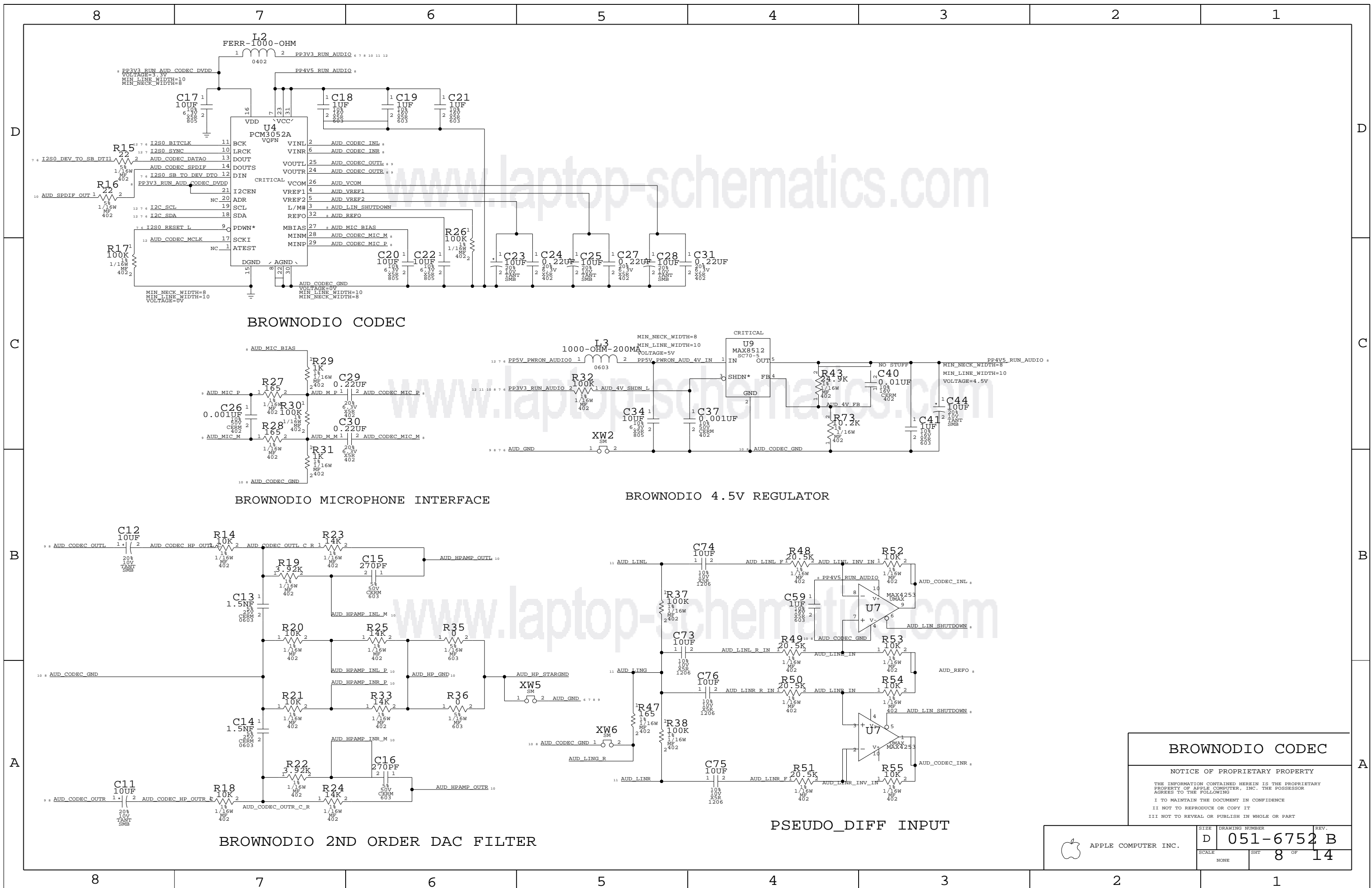
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BROWNODIO CODEC

BROWNODIO MICROPHONE INTERFACE

BROWNODIO 4.5V REGULATOR

BROWNODIO 2ND ORDER DAC FILTER

PSEUDO\_DIFF INPUT

**BROWNODIO CODEC**

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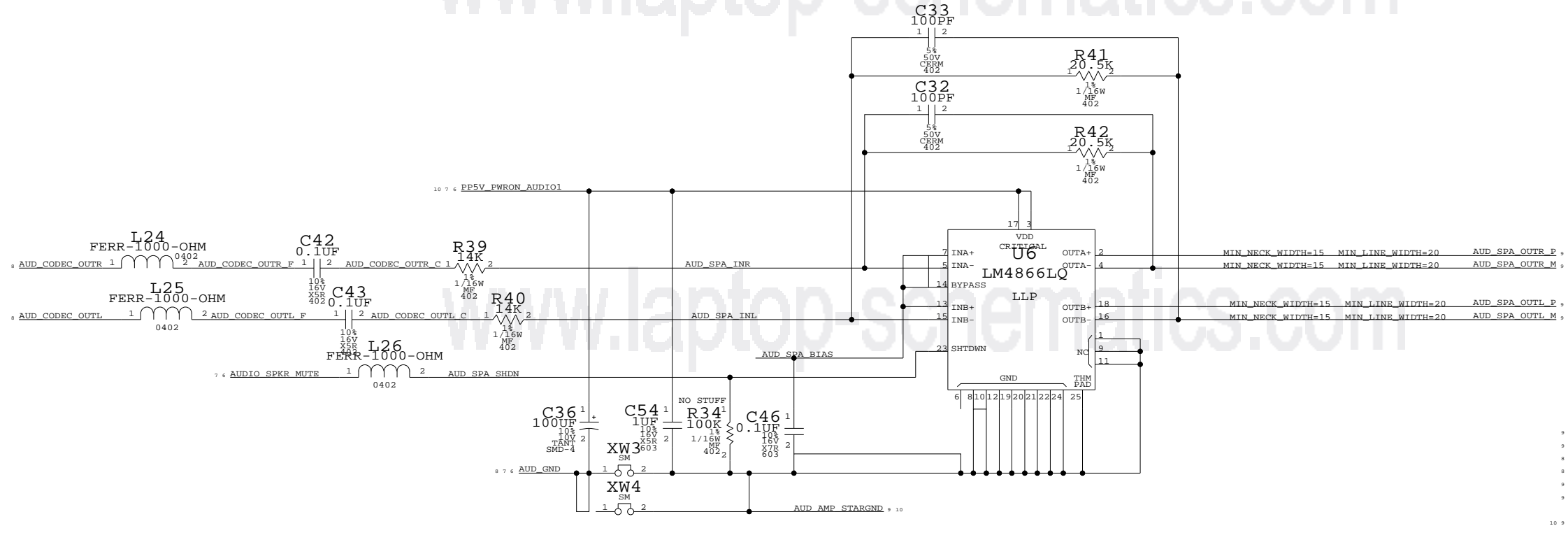


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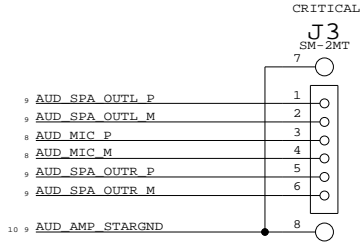
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### SPEAKER AMPLIFIER



### SPEAKER CONNECTOR

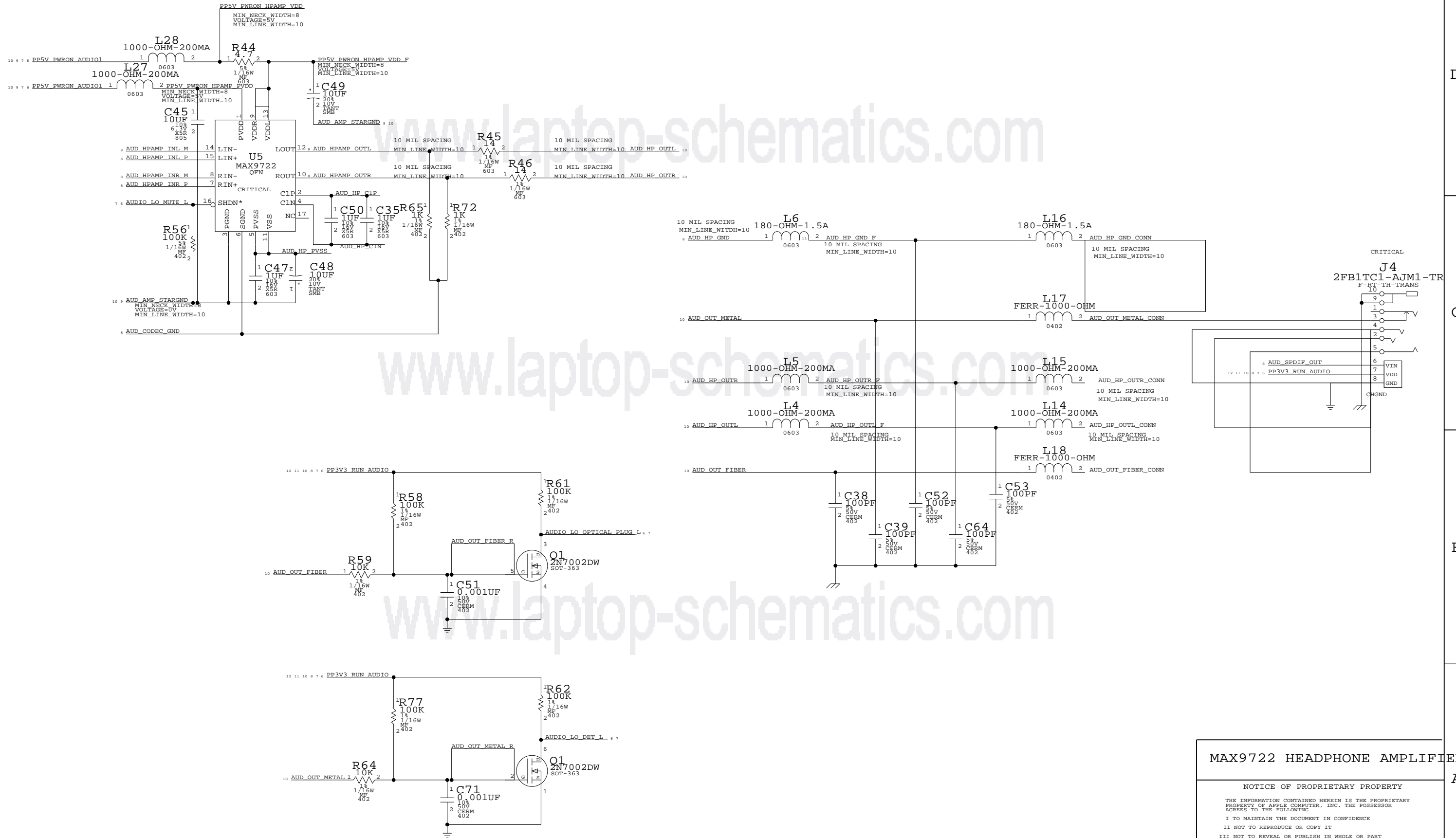


### MAX9710 SPEAKER AMPLIFIER

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NONE			

# HEADPHONE AMPLIFIER




## MAX9722 HEADPHONE AMPLIFIER

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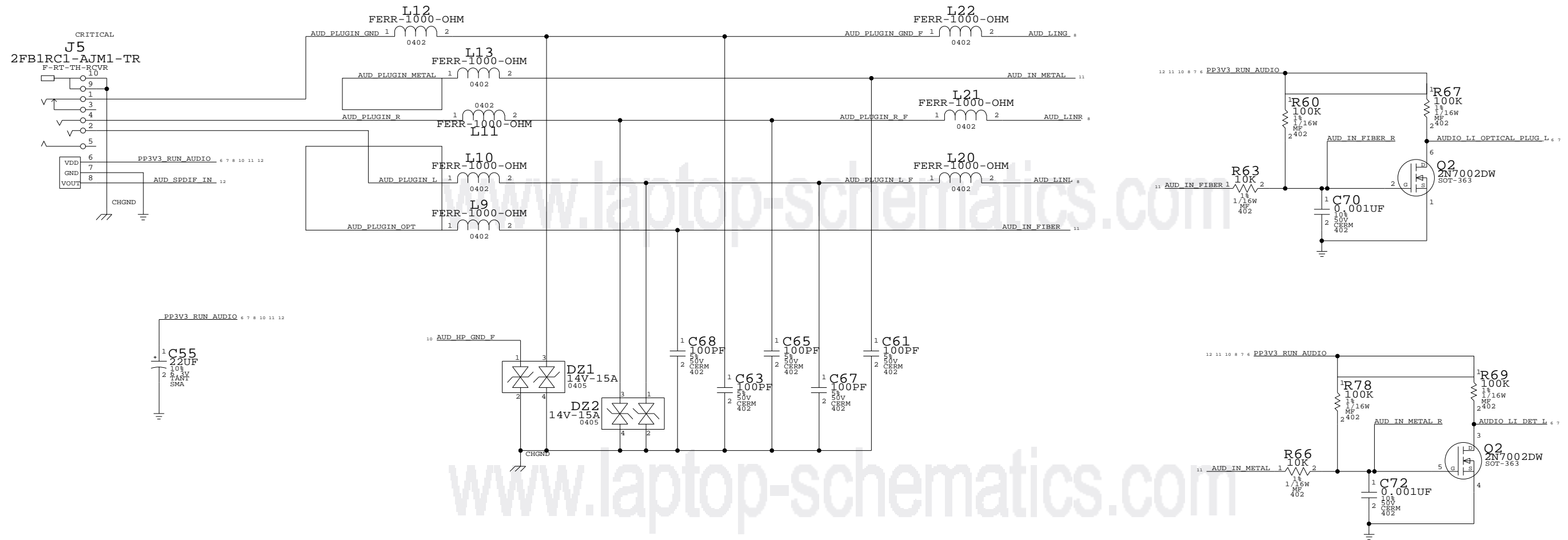
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	D	051-6752	B
SCALE	SHT	10 OF 14	
NONE			

LINE IN FILTER (PSEUDO-DIFF INPUT) ON CODEC PAGE  
 MIC PREAMP INCLUDED IN PCM3052A CODEC

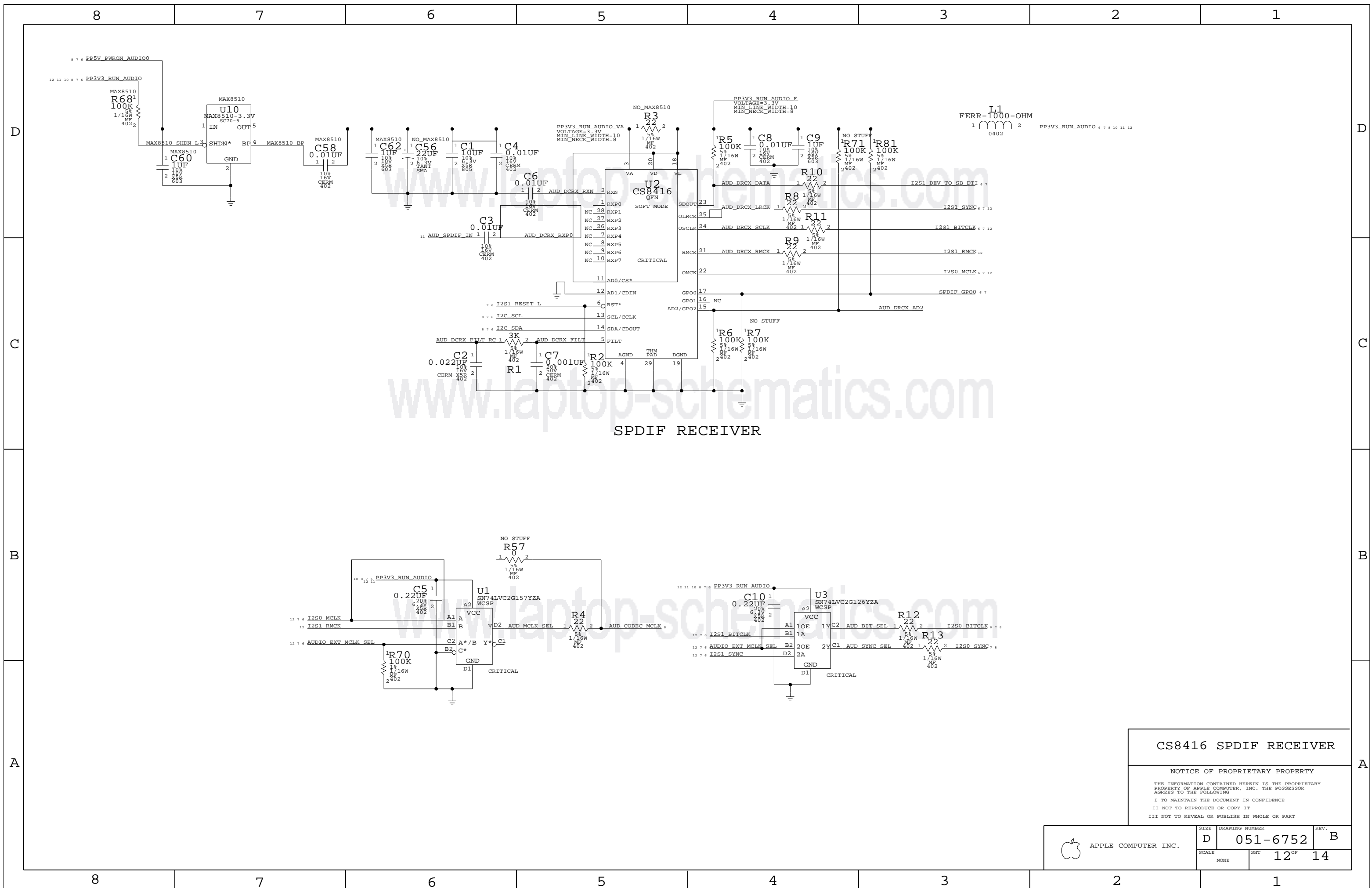
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NONE			



SPDIF RECEIVER

CS8416 SPDIF RECEIVER

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SCALE		SHT	12 OF 14
NONE			

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*** Signal Cross-Reference for the entire design ***
AUDIO_EXT_MCLK_SEL 6C5> 784<> 12A4<> 12A7<>
AUDIO_LL_DET_L 6D5> 785<> 1181<>
AUDIO_LL_OPTICAL_PLUG_L 6D5> 785<> 11C1<>
AUDIO_LO_DET_L 6D5> 785<> 10A5<>
AUDIO_LO_MUTE_L 6C5> 784<> 10C8<>
AUDIO_LO_OPTICAL_PLUG_L 6D5> 785<> 10B5<>
AUDIO_SPEK_MUTE 6C5> 784<> 9B7<>
AUD_AV_FB 8C4<>
AUD_AV_SHDN_L 8C5<>
AUD_AMP_STARGND 9B2<> 9B5<> 10C8<> 10D6<>
AUD_BIT_SEL 12B4<>
AUD_CODEC_DATA0 8D8<>
AUD_CODEC_GND 8A4< 8A5<> 8A8< 8B4<> 8B7< 8C7<
10C8<>
AUD_CODEC_HP_OUTL_C 8B8<>
AUD_CODEC_HP_OUTR_C 8A8<>
AUD_CODEC_INL 8A3<> 8D6<>
AUD_CODEC_INR 8A3<> 8D6<>
AUD_CODEC_MCLK 8C8< 12B5<>
AUD_CODEC_MIC_M 8B6< 8C6<>
AUD_CODEC_MIC_P 8C6< 8C6<>
AUD_CODEC_OUTL 8B8< 8D6<> 9C8<>
AUD_CODEC_OUTL_C 9C7<>
AUD_CODEC_OUTL_C_R 8B7<>
AUD_CODEC_OUTL_P 9C7<>
AUD_CODEC_OUTR 8A4< 8D6<> 9C8<>
AUD_CODEC_OUTR_C 9C7<>
AUD_CODEC_OUTR_C_R 8A7<>
AUD_CODEC_OUTR_P 9C7<>
AUD_CODEC_SFP1P 8D8<>
AUD_DCKL_FLT 12C3<>
AUD_DCKL_FLT_RC 12C6<>
AUD_DCKL_RSN 12D5<>
AUD_DCKL_S2V 12C5<>
AUD_DCKL_AD2 12C3<>
AUD_DCKL_DATA 12D4<>
AUD_DCKL_LACK 12D4<>
AUD_DCKL_RMCK 12C4<>
AUD_DCKL_SCLK 12C4<>
AUD_GND 6C5> 785<> 8A5<> 8B6<> 9B6<>
AUD_HPAMP_INL_M 8B6< 10D8<>
AUD_HPAMP_INL_P 8A6< 10D8<>
AUD_HPAMP_INM_M 8A6< 10C8<>
AUD_HPAMP_INM_P 8A6< 10C8<>
AUD_HPAMP_OUTL 8B6< 10D7<>
AUD_HPAMP_OUTR 8A6< 10C7<>
AUD_HP_C1N 10C6<>
AUD_HP_C1P 10C6<>
AUD_HP_GND 8A6< 10C5<>
AUD_HP_GND_CONN 10C2<>
AUD_HP_GND_F 10C4< 11B6<>
AUD_HP_OUTL 10B5< 10D5<>
AUD_HP_OUTL_CONN 10B2<>
AUD_HP_OUTL_F 10B4<>
AUD_HP_OUTR 10C5< 10C5<>
AUD_HP_OUTR_CONN 10C2<>
AUD_HP_OUTR_F 10C4<>
AUD_HP_PVSS 10C8<>
AUD_HP_STARGND 8A5<>
AUD_IN_FIBER 11C3< 11C3<>
AUD_IN_FIBER_R 11C2<>
AUD_IN_METAL 11B3< 11C3<>
AUD_INL 11B4<>
AUD_LING 8A5< 11C3<>
AUD_LING_R 8A5<>
AUD_LING_L 8B5< 11C3<>
AUD_LINL_P 8B4<>
AUD_LINL_IN 8A4<>
AUD_LINL_INV_IN 8B4<>
AUD_LINL_R_IN 8A4<>
AUD_LINR 8A5< 11C3<>
AUD_LINR_P 8A4<>
AUD_LINR_IN 8A4<>
AUD_LINR_INV_IN 8A4<>
AUD_LINR_IN_IN 8A4<>
AUD_LIN_SHUTDOWN 8A3<> 8B3<> 8D7<>
AUD_MCLK_SEL 12B6<>
AUD_MIC_BIAS 8C7< 8C7<>
AUD_MIC_M 8B7< 9B2<>
AUD_MIC_P 8C7< 9B2<>
AUD_M_P 8B7<>
AUD_M_P 8C7<>
AUD_OUT_FIBER 10B5< 10B7<>
AUD_OUT_FIBER_CONN 10B5<>
AUD_OUT_FIBER_R 10B5<>
AUD_OUT_METAL 10A7< 10C5<>
AUD_OUT_METAL_CONN 10C2<>
AUD_OUT_METAL_R 10A5<>
AUD_PLUGIN_GND 11C7<>
AUD_PLUGIN_GND_P 11C4<>
AUD_PLUGIN_L 11C7<>
AUD_PLUGIN_L_F 11C4<>
AUD_PLUGIN_METAL 11C7<>
AUD_PLUGIN_OPT 11C7<>
AUD_PLUGIN_R 11C7<>
AUD_PLUGIN_R_F 11C4<>
AUD_SFPO 8A3< 8D7<>
AUD_SPA_BIAS 9C5<>
AUD_SPA_INL 9C5<>
AUD_SPA_INR 9C5<>
AUD_SPA_OUTL_P 9B2<> 9C2<>
AUD_SPA_OUTL_P 9B2<> 9C2<>
AUD_SPA_OUTR_M 9B2<> 9C2<>
AUD_SPA_OUTR_P 9B2<> 9C2<>
AUD_SPA_SHEN 9B6<>
AUD_SFP1P_IN 11C7< 12C6<>
AUD_SFP1P_OUT 8D8< 10C2<>
AUD_SYNC_SEL 12A4<>
AUD_VCOM 8D7<>
AUD_VREF1 8D7<>
AUD_VREF2 8D7<>
CGND01 2D2<>
I2C_SCL 6D5> 7A5<> 8D6< 12C6<>
I2C_SDA 6D5> 7A5<> 8D8<> 12C6<>
I2S0_B1TCLK 6C5> 7A3<> 8D8<> 12B3<>
I2S0_DVY_TO_SB_PFI 6C5> 7A6<> 8D8<>
I2S0_MCLK 6C5> 7B3<> 12B7<> 12C3<>
I2S0_RESET_L 6D5> 785<> 8C8<>
I2S0_SB_TO_DVY_VDD 6C5> 7A6<> 8D8<>
I2S0_SYNC 7B4<> 8D8< 12A1<>
I2S0_B1TCLK 6C5> 7A3<> 12B4<> 12C3<>
I2S1_DVY_TO_SB_PFI 6C5> 7A6<> 12D3<>
I2S1_RESET_L 6D5> 785<> 12C6<>
I2S1_SCLK 12B7<> 12C3<>
I2S1_SYNC 6C5> 7A6<> 12A4<> 12D3<>
MAX910_BP 12D7<>
MAX910_SHDN_L 12D8<>
MIDDLE_COREM_GND 2C2<>
PP3V3_RUN_AUDIO 6D5> 7A5<> 7B6<> 8C6< 8D6< 10A7<
10B7< 10C5< 11B3< 11B7< 11C3< 11C7<
12B4< 12B6< 12D2< 12D8<
PP3V3_RUN_AUDIO_F 12D4<>
PP3V3_RUN_AUDIO_I0A 12D8<>
PP3V3_RUN_AUDIO_CODER_VDD0 8D8< 8D8<>
PP4V5_RUN_AUDIO 8B4< 8C2<> 8D6<>
PP5V_PWRON_AUDIO0 6C5> 7B3<> 8C6< 12D8<>
PP5V_PWRON_AUDIO1 6C5> 7B3<> 9C6< 10D8< 10D8<>
PP5V_PWRON_AUDIO_AV_IN 8C5<>
PP5V_PWRON_HPAMP_VDD 10D7<>
PP5V_PWRON_HPAMP_VDD 10D7<>
PP5V_PWRON_HPAMP_VDD_F 10D6<>
SLEEP_LED 6C5> 7A6<> 7C6<>
SLEEP_LED_GND 6C5> 7A6<> 12C3<>
SFP1P_GND 6C5> 7B4<> 12C3<>

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D

D

C

C

B

B

A

A

	8	7	6	5	4	3	2	1
D	<pre> *** Part Cross-Reference for the entire design *** C1 CAP 12 C2 CAP 12 C3 CAP 12 C4 CAP 12 C5 CAP 12 C6 CAP 12 C7 CAP 12 C8 CAP 12 C9 CAP 12 C10 CAP 12 C11 CAP_P 8 C12 CAP_P 8 C13 CAP 8 C14 CAP 8 C15 CAP 8 C16 CAP 8 C17 CAP 8 C18 CAP 8 C19 CAP 8 C20 CAP 8 C21 CAP 8 C22 CAP 8 C23 CAP_P 8 C24 CAP 8 C25 CAP_P 8 C26 CAP 8 C27 CAP 8 C28 CAP_P 8 C29 CAP 8 C30 CAP 8 C31 CAP 8 C32 CAP 9 C33 CAP 9 C34 CAP 8 C35 CAP 10 C36 CAP_P 9 C37 CAP 8 C38 CAP 10 C39 CAP 10 C40 CAP 8 C41 CAP 8 C42 CAP 9 C43 CAP 8 C44 CAP_P 8 C45 CAP 10 C46 CAP 9 C47 CAP 10 C48 CAP_P 10 C49 CAP_P 10 C50 CAP 10 C51 CAP 10 C52 CAP 10 C53 CAP 10 C54 CAP 9 C55 CAP_P 11 C56 CAP_P 12 C58 CAP 12 C59 CAP 8 C60 CAP 12 C61 CAP 11 C62 CAP 12 C63 CAP 11 C64 CAP 10 C65 CAP 11 C67 CAP 11 C68 CAP 11 C70 CAP 11 C71 CAP 10 C72 CAP 11 C73 CAP 8 C74 CAP 8 C75 CAP 8 C76 CAP 8 D01 SUPP_TRANSIENT_4P1 11 D02 SUPP_TRANSIENT_4P1 11 J1 COM_F45ST_D_SM 7 J2 COM_M2ST_S2MT_SM 7 J3 COM_M2ST_M2IN 9 J4 COM_P8RT_S2D1PTRAN_TH1 10 J5 COM_P8RT_S2D1PVCVR_TH1 11 L1 IND 12 L2 IND 8 L3 IND 8 L4 IND 10 L5 IND 10 L6 IND 10 L9 IND 11 L10 IND 11 L11 IND 11 L12 IND 11 L13 IND 11 L14 IND 10 L15 IND 10 L16 IND 10 L17 IND 10 L18 IND 10 L20 IND 11 L21 IND 11 L22 IND 11 L24 IND 9 L25 IND 9 L26 IND 9 L27 IND 10 L28 IND 10 Q1 TRA_2N7002DW 10 Q2 TRA_2N7002DW 11 R1 RES 12 R2 RES 12 R3 RES 12 R4 RES 12 R5 RES 12 R6 RES 12 R7 RES 12 R8 RES 12 R9 RES 12 R10 RES 12 R11 RES 12 R12 RES 12 R13 RES 12 R14 RES 8 R15 RES 8 R16 RES 8 R17 RES 8 R18 RES 8 R19 RES 8 R20 RES 8 R21 RES 8 R22 RES 8 R23 RES 8 R24 RES 8 R25 RES 8 R26 RES 8 R27 RES 8 R28 RES 8 R29 RES 8 R30 RES 8 R31 RES 8 R32 RES 8 R33 RES 8 R34 RES 9 R35 RES 8 R36 RES 8 R37 RES 8 R38 RES 8 R39 RES 9 R40 RES 9 R41 RES 9 R42 RES 9 R43 RES 8 R44 RES 10 R45 RES 10 R46 RES 10 R47 RES 8 R48 RES 8 R49 RES 8 R50 RES 8 R51 RES 8 R52 RES 8 R53 RES 8 R54 RES 8 R55 RES 8 R56 RES 10 R57 RES 12 R58 RES 10 R59 RES 10 R60 RES 11 </pre>		<pre> R61 RES 10 R62 RES 10 R63 RES 11 R64 RES 10 R65 RES 10 R66 RES 11 R67 RES 11 R68 RES 12 R69 RES 11 R70 RES 12 R71 RES 12 R72 RES 10 R73 RES 8 R76 RES 2 R77 RES 10 R78 RES 11 R81 RES 12 U1 INT74LVC2G157PZA 12 U2 C28416_S0P5 12 U3 INT74LVC2G126PZA 12 U4 AUDIO_PCM3052A 8 U5 MAX922 10 U6 AUDIO_IM4866LQ 9 U7 OPAMP_MAX4253 8 U9 MAX8512 8 U10 MAX8510 12 X02 SHORT 8 X03 SHORT 9 X04 SHORT 9 X05 SHORT 8 X06 SHORT 8 </pre>		D			
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