1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SEEDY
REV E

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
E		385505	PRODUCTION RELEASED	06/13/05	?

06/13/05

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK | ENG APPD | MFG APPD | QA APPD | DESIGNER | RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

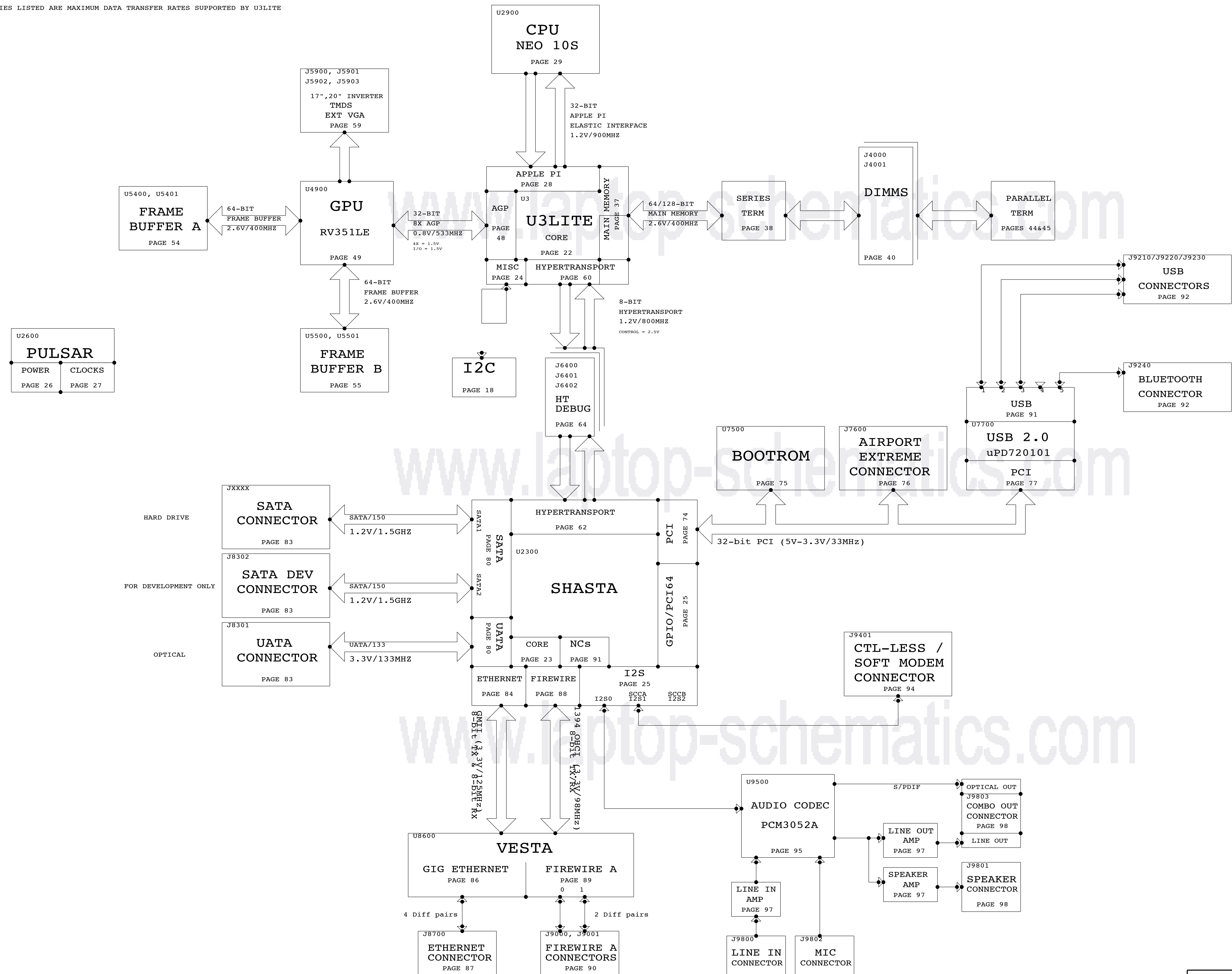
Apple Computer Inc.

TITLE SCH,MLB,SEEDY

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SHT 1 OF 102

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE



SYSTEM BLOCK DIAGRAM

SYNC_MASTER=N/A SYNC_DATE=N/A

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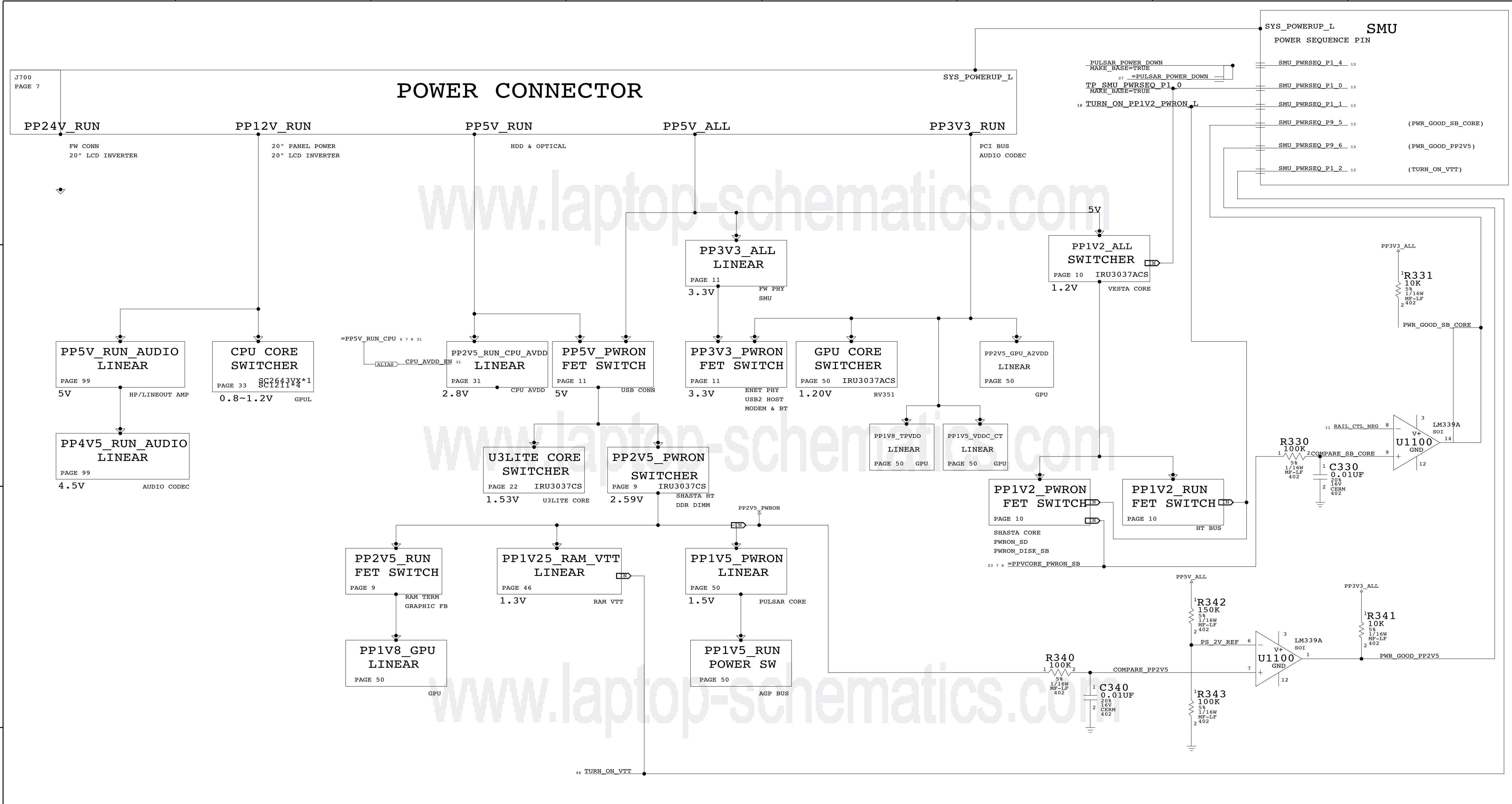
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 2 OF 102	

8 7 6 5 4 3 2 1 / D C B A



POWER BLOCK DIAGRAM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 3 OF 102	

DATE DESCRIPTION

DATE	DESCRIPTION
10/20/04	CLONED DESIGN FROM GILA (Q45 A/B) REV G CHECKIN 00002
10/21/04	ADDED VESTA ADDED 1.2V REGULATOR FOR VESTA CORE ADDED 2.5V LDO FOR VESTA ADDED FW LATE VG PROTECTION REMOVED BCM5231 ETHERNET PHY REMOVED FW802A FW PHY REMOVED FW PORT POWER CIRCUITRY REMOVED MICRODASH CONNECTOR CHECKIN 00003
10/22/04	REMOVED NV18/34 GPU REMOVED AGP VREG (VR5001) REMOVED GPU VTT VREG ADDED 2.5V VREG FOR A2VDD REMOVED EXTERNAL TMDS TRANSMITTER ADDED RV351LE GPU CHECKIN 00004
10/26/04	GPU CORE POWER UPDATES ADDED VESTA ETHERNET LOWPWR CIRCUIT ADDED DEVELOPMENT LEDS FOR VESTA ENET CHECKIN 00005
10/28/04	CONNECTED FRAME BUFFER ADDED 1.8V GPU VREG CONNECTED GPU TMDS AND VGA CONNECTED GPU POWER AND POWER FILTERS CHECKIN 00006
11/01/04	ADDED VOLTAGE, LINE WIDTH, AND NECK WIDTH PROPERTIES FOR GRAPHICS TIED PPVCORE_NB DIRECTLY TO PP1V5_PWRON (REMOVED R707) REPLACED EMC FERRITES WITH 0 OHM RESISTORS FOR GRAPHICS AND FANS REMOVED VESTA CORE REGULATOR REPURPOSED 1.2V REGULATOR FOR VESTA AND SHASTA CHANGED FW LATE VG CIRCUITRY TO MATCH Q78 & Q86 CHECKIN 00007
11/03/04	<RADAR 3848831> MOVED SMU RESET BUTTON TO DEVELOPMENT BOM <RADAR 3849762> MOVED SMU DOWNLOAD CONNECTOR TO DEVELOPMENT BOM <RADAR 3849798> REDUCED CAPACITANCE OF C1100 & C1102 MASTER PAGE SYNC: FRAME BUFFER SWAPS FOR CLEANER ROUTING REMOVED VESTA ROM AUDIO COST REDUCTIONS <RADAR 3849747 & 3849751> AUDIO 3052A CODEC ADDED 1.55V VREG FOR GPU VDDC_CT MOVED VTT VREG TO 2.5V PWRON TO REDUCE CURRENT THROUGH Q903 CHANGED FETS IN GPU CORE FOR COST REDUCTION ADDED SPACING & PHYSICAL CONSTRAINTS TO FRAME BUFFER CHECKIN 00008
11/04/04	REMOVED 1.6GHZ PROCESSORS CHANGED VOLTAGE SETTING OF 2.5V VREG TO 2.588V FROM 2.62V 1.2V VREG COST REDUCTIONS - Q1002 TO NTD60N02R; C1002/3 TO 10UF CERM U2850 - REMOVED MAXIM AS AN ALTERNATE MOVED GPU ZENER DIODES TO VREG PAGE SINCE THEY SHOULD BE PLACED NEAR THE VREGS ADDED 8MX32 GRAPHICS MEMORY ADDED GIGABIT ETHERNET CONNECTOR CHECKIN 00009
11/06/04	ADDED GPU STRAPS CONNECTED GPU GPIOS REMOVED ON BOARD POWER SUPPLY TEMP SENSOR ADDED AMBIENT LIGHT SENSOR CONNECTOR CONNECTED GPU TEMP SENSOR REMOVED CPU VREG 4TH PHASE ADDED DEVELOPMENT LEDS TO REGULATORS CHECKIN 00010
11/07/04	ADDED MORE GPU CONSTRAINTS <RADAR 3616348, 3621390> CHANGED FL5900-2 TO 220 OHM <RADAR 3848846> 2.5V RUN FET COST REDUCTION <RADAR 3848859> 1.2V, 1.5V RUN FET COST REDUCTIONS <RADAR 3848887> 5V & 3.3V PWRON FET COST REDUCTIONS <RADAR 3849622> STUFFED AROUND TMDS FILTERS <RADAR 3849656> STUFFED AROUND RGB FILTERS <RADAR 3849806> CHEAPER SMU CRYSTAL <RADAR 3849857> CHEAPER USB2 CRYSTAL BOM RELEASE REV 01
11/08/04	FRAME BUFFER PIN SWAPS <RADAR 3848846> UPDATE OF 2.5V RUN FET COST REDUCTION <RADAR 3849743> ADDED RESISTORS TO STUFF AROUND USB FILTERS CHECKIN 01001
11/09/04	<RADAR 3848850> REGULATOR COST REDUCTIONS <RADAR 3849767> 2.5V VREG COST REDUCTIONS <RADAR 3849772> REMOVED OUTPUT CAP ON 1.2V_ALL VREG <RADAR 3849820> SHASTA FILTER COST REDUCTION <RADAR 3849854> GPU CORE VREG COST REDUCTION <RADAR 3865344> SET GPU VDDC_CT VREG TO 1.55V CHECKIN 01002
11/10/04	CHANGED SOURCE OF Q1003 TO PP1V2_ALL RGB TERMINATION NOW CONNECTED TO DIGITAL GROUND WHITE LED - CHANGED INDUCTORS TO 0 OHM RESISTORS UPDATED POWER BLOCK DIAGRAM CHECKIN 01003 <RADAR 3848850> 2.5V VREG COST REDUCTION CHECKIN 01004
11/15/04	ADDED REGULATOR FOR GPU TPVDD ADDED POWER SEQUENCING FOR GRAPHICS REGULATORS ADDED TEST POINTS TO GRAPHICS FOR EXOR TESTING REMOVED EXTERNAL S/PDIF TRANSMITTER CHECKIN 01005
11/16/04	REMOVED P50 AIRPORT AND Q23 BLUETOOTH CONNECTORS, HOLES, & STANDOFFS ADDED Q85 AIRPORT & BLUETOOTH CONNECTOR CHECKIN 01006 (PP 16,17) REPLACED FAN CONTROL WITH NEW CIRCUIT (P 76) FINISHED CONNECTING Q85 CONNECTOR (P 7) ADDED PLATED HOLE ZH710 FOR TMDS GROUNDING (P 7) TIED BOTH EI RAILS TO 1.5V (P 5) NEW BOOTROM P/N (P 9) ADDED EXTRA 10UF INPUT CAP (P 12) VESTA_ENET_LOWPWR UPDATE (P 18) <RADAR 3878118> MOVED SMU I2C E BUS (P 22) CHANGED Q2250 TO 376S0143 (P 46) SLEEP SIGNAL TURNS OFF VTT VREG (P 58) REPLACED THERMAL SENSOR WITH LM63 (P 59) TIED UNUSED BUFFER ENABLE PINS HIGH (P 90) FIXED FW PORT NAMING (P 90) CHANGED R9090 TO 665 OHM (P 91) CHANGED USB2 CHIP GROUNDING (P 8) ALIASED VESTA JTAG TO TEST POINT NETS (P 9) <RADAR 3848846> ADDED PAD FOR 1NF CAP TO GATE OF Q903 CHECKIN 01007 / BOM RELEASE REV 02
11/18/04	ADDED PHYSICAL CONSTRAINTS AUDIO STUFFING CHANGES CHECKIN 02001
11/20/04	(P 36) CONNECTED NEW CPU DIODE REFERENCE (P 77) USB2 IDESEL - NOW FROM USB2 SIDE (P 56) ADDED BOMOPTIONS FOR MEMORY STRAPS (PP 56, 58) CONNECTED PWM FROM RV351LEP & PUT IN PROTO WORKAROUND (P 25) <RADAR 3849835> NEW SHASTA XTAL (P 62) <RADAR 3849855> SHASTA HT_PLL FILTER COST REDUCTION (P 91) <RADAR 3849858> USB CAP COST REDUCTION (P 76) ADDED STANDOFFS FOR Q85 CARD (PP 16,17) NEW FAN CIRCUIT CAPS (C1603, C1653, C1703) (P 50) <RADAR 3865344> VDDC_CT SET TO 1.50V (P 50) <RADAR 3877855> TP_VDD SET TO 1.80V (P 12) VESTA_ENET_LOWPWR UPDATE (PP 10, 22, 34, 50) USED COMPARATOR FOR LOW VOLTAGE RAIL LEDS CHECKIN 02002
11/22/04	(P 49) CONNECTED AGPTEST RESISTOR TO VDDP (P 56) ADDED PADS FOR STRAPPING RESISTORS TO GPU_GPIO<14> (P 58) ADDED CONSTRAINT SETS (P 59) STUFFED AROUND Q5900 PANEL PWR SEQUENCING (P 59) LED 3 NOW DRIVEN FROM FPD_PWR_ON (P 3) CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING (P 76) FIXED PCI_CBE_L<1> CONNECTION MORE PHYSICAL & SPACING UPDATES (P 83) <RADAR 3890225> OPTICAL DRIVE CONNECTOR CHANGED TO 516S0235 CHECKIN 02003 (P 56) ADDED OPTION OF USING PWM FROM SHASTA <RADAR 3849718, 3849767, 3849854> MADE ON & VISHAY FETS ALTERNATES (P5) ADDED U3L W/ NEW LAMINATE AS ALTERNATE (P 16) C1653 - REPLACED WITH LOWER HEIGHT CAP CHECKIN 02004
11/23/04	(P 76) TABLED IN NEW STANDOFFS FOR Q85 CARD PROTO RELEASE (REV 3)
12/02/04	(P 90) FIXED ALIAS PROBLEM WITH FW_TPB2_PD (P 90) FIXED FW_CPS SHORT (P 35) REMOVED DS3500 & DS3501 (P 83) REMOVED SECOND SATA CONNECTOR CHECKIN 03001 CONVERTED DISCRETES TO LEAD FREE CHECKIN 03002
12/07/04	CHANGED U7700 BACK TO LEADED PART (P 5) REMOVED ORIGINAL U3LITE (NEW LAMINATE ONLY FOR C/D) (P 49) CHANGED GPU TO RV351LEP (338S0231) (P 76) NOW HAVE CORRECT SYMBOL FOR STANDOFFS (P 76) J7650 - NEW TO ALLOW 5MM CONNECTED HEIGHT BOM RELEASE REV 04
12/09/04	CHANGED ALIASES TO SYNONYMS CHANGED LINE AND NECK WIDTHS TO METRTIC CHECKIN 04001
12/13/04	ADDED 2.0 GHZ AND ADDITIONAL 1.8 GHZ ALTERNATE PROCESSORS VESTA XTAL: R5815=249, R8609=332, R8921=332 VESTA ENET: R1262=10K, C1260=10U, R1251=NO STUFF, C1250=2.2U FANS: NO STUFF DZ1601, DZ1651, DZ1701 STUFFED R1604, R1654, R1704 CHECKIN 04002
12/14/04	2.5 V REGULATOR - NEW NARROWER OUTPUT CAPS (C908, C909) (P 46) REMOVED SEMTECH REGULATOR, ADDED RICHTEK AS ALTERNATE VTT (P 16) CHANGED FAN1 OUTPUT CAP BACK TO THROUGH-HOLE (P 59) SWAPPED INVERTER CONNECTOR GENDER CHECKIN 04003 (P 46) RICHTEK VTT UPDATES BOM RELEASE REV 5
12/15/04	(P 6) ADDED NO_TESET PROPERTIES (P 12) VESTA ENET LOW POWER FIX CHECKIN 05001
12/16/04	FIXED I2C_TMDS_SDA/SCL ON P 6 (P 46) NOSTUFF RICHTEK VTT VREG (P 59) STUFFED TMDS CHOKES (P 56) USING PWM FROM ATI GPU (P 38) FIXED MIN_NECK_WIDTH ON TD1 AND TD2 (P 92) ADDED NET_PHYSICAL_TYPE = USB2 TO TABLE (P 7) ADDED BATTERY SAFETY BYPASS OPTION (NOSTUFF) CHECKIN 05002 (P 50) ADDED Q5000 TO INPUT OF GPU VCORE VREG (P 6) REMOVED SOME FUNC_TEST PROPERTIES (P 50) GPU_VDCC_CT POWER SEQUENCING CHECKIN 05003
12/17/04	(P 6) ADDED/REMOVED MORE FUNC_TEST PROPERTIES CHECKIN 05004 (P 50) GPU POWER SEQUENCING CHECKIN 05005
12/20/04	MINOR TEXT/COMMENT CHANGES EVT RELEASE (REV 6)
01/11/05	(P 5) REMOVED BRA FROM PROCESSOR TABLE, REPLACED BPA WITH BNA (P 5) NEW SMU PART NUMBER
01/18/05	CHANGED SDF7601 TO PART 860-0567 BOM RELEASE REV 7
01/25/05	(P 5) CORRECTED 1.8GHZ CPU APPLE P/N FROM 337S2969 TO 337S2998 (P 12) NOSTUFF Q1250 TO DISCONNECT ENETFW_RESET FROM SHASTA GPIO (P 5) CORRECTED SMU PART NUMBER TO 341T1703 (P 16, 17) HAROLD'S FAN CIRCUIT CHANGES CHECKIN 07002
01/27/05	(P 25) REPLACED R2566 WITH 0 OHM TO ELIMINATE FW_LOWPWR GLITCH ADDED 0 OHM (R2570, NOSTUFF) TO BREAK FW_LOWPWR FROM SHASTA (P 56) STUFF R5610 TO PULL DOWN ATI_PWM SIGNAL TO ELIMINATE GLITCH (P 27-29) CONNECTED CPU_APSYNC FROM U3LITE AND DISCONNECTED FROM PULSAR NO STUFF: R2768,R2772,R2805,R2910 STUFF: R2806,R2911 (P 11) CHANGED C1102 TO 16V FOR SUPPLY AND COST ISSUES (P 5) ADDED KQA (337S3093) TO ALTERNATE PROCESSOR TABLE CHECKIN 07003 (P 5) MODIFIED PROCESSOR TABLE TO MATCH IBM'S TABLE, AGAIN. BOM RELEASE REV 8
02/01/05	(P 75) BOOTROM REFLASHING ISSUE FIX: CHANGED R7502 TO 470 OHM (P 12) ADDED A CLAMP CIRCUIT FOR ENET_LOWPWR GLITCH (P 10,22) SHASTA & U3LITE VCORE IMPROVEMENT: STUFF C1005 & C2205 WITH 2200PF (P 13) CHANGED U1301 TO LEADED PART (353S0653) DUE TO SUPPLY (P 5) ADDED 34S0284 AND 34S0282 AS U3LITE ALTERNATES (OLD LAM) BOM RELEASE REV 9
02/03/05	(P 28) CHANGED APSYNC SERIES TERMINATION R2806 TO 10 OHM (P 5) ADDED LEAD FREE PARTS AS ALTERNATE FOR U1301 & VRA201 DUE TO SUPPLY (P 8) REMOVED SMU DOWNLOAD CONNECTOR FROM DEVELOPMENT BOM (P 92) STUFFED USB COMMON MODE CHOKES FOR EMC CHECKIN 09002
02/04/05	(P 50) <RADAR 3919121> NOSTUFF U5090 AND RELATED COMPONENTS STUFFED R5092 FOR 1.5V GPU VDCC_CT
02/08/05	(P 7) REMOVED ZH701 (P 12) STUFF R1251, CHANGE C1250 TO 10UF, R1262=100K TO LENGTHEN VESTA RESET AND LOWPWR DELAY (P 59) <RADAR 3849662> STUFFED PANEL POWER SEQUENCING FOR BOTH 17 AND 20 INCH CHECKIN 09003 (P 92) <RADAR 3742725> CHANGED USB COMMON MODE CHOKES TO 120-OHM 155S0232 (P 59) NOSTUFF R5950, STUFF R5923 FOR 17 INCH PANEL POWER FROM PP3V3_RUN
02/09/05	CHECKIN 09004
02/10/05	(P 59) <RADAR 3919083> CHANGED R5971 AND R5972 TO 33 OHMS (P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: U5600, U5601 NOSTUFF: R5609, R5621 DVT RELEASE (REV 10) (P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: C5600, C5601
02/15/05	(P 12) CHANGED C1250 TO 6.3V PART, TO MATCH A PART ALREADY ON THE BOM (P 5) ADDED 353S0687 (LEADED) AS ALTERNATE FOR 353S0959 (LEAD FREE) U9800
02/16/05	ADDED PAGE TITLE PROPERTIES FOR SCHEMATIC REUSE WITH M23/M33
02/17/05	(P 12) YET ANOTHER VESTA RESET/LOWPWR STUFFING CHANGE (P 16,17,36) ADDED SIGNAL ALIASES FOR SCHEMATIC REUSE WITH M23 (P 50) RE-STUFFED GPU 1.5V VDCC_CT BECAUSE OF LEAKAGE WORRIES BOM RELEASE REV 11
03/07/05	(P 12) MADE CONNECTION FOR VESTA RESET FINAL FOR PVT (P 49) STUFFED 470 OHMS FOR R4912 TO AVOID PCI_RESET GLITCH FROM GPU (P 50) ADDED FET TO SPLIT 3.3V POWER TO GPU I/O (P 59) HACK FOR PANEL POWER SEQ.OPTION FROM SYS_SLEEP (P 6, 58) ADDED TEST POINTS FOR NEC AND ATI CHECKIN 11002 (03/11)
03/17/05	(P 50, 59) FINALIZED STUFFING OPTIONS FOR ATI POWER SEQUENCE HACK BOM RELEASE REV 12, CHECKIN 12001
03/21/05	(P 8,12,89) CHANGED VESTA STRAP PULL UP/DOWN RES TO 1K PER BROADCOM (P 13) RELOADED Y1300 DUE TO LIBRARY CHANGE BOM RELEASE REV 13
03/22/05	(P 16) REMOVED OPTICAL TEMP SENSOR (U1602) FOR BETTER I2C BUS ROUTING CHECKIN 13001
03/24/05	(P 5) ADDED LEADED ALTERNATE FOR VRA200, LM1117 (P 10,80) ADDED CAPS ON 1.2V RAIL TO REDUCE SATA POWER NOISE CHECKIN 13002
03/25/05	(P 80) CHANGED CAPS TO 1UF, REMOVED 10UF THAT WOULD NOT FIT (P 10) CHANGED R1003 TO 5.62K TO RAISE 1.2V REGULATOR TO 1.25 (P 6) ADDED NO_TEST PROPERTIES ON UNUSED SATA2 NETS (P 50) CHANGED R5091 TO 61.9K TO INCREASE VDCC_CT TO ABOUT 1.54V BOM RELEASE REV14, CHECKIN 14001
03/28/05	PVT RELEASE (REV A)
04/06/05	(P 25,62) RESTUFFED C2500,C2520,C2530,C6200,C6210 FOR SHASTA POWER DECOUPLING PVT RELEASE 2 (REV B)
04/22/05	(P 5) ADDED BPL, BRL, AND BNA PROCESSORS TO TABLE (P 50) CHANGED R5091 TO 56.2K TO INCREASE VDCC_CT TO ABOUT 1.65V REV C RELEASE
04/25/05	(P 50) STUFFED R5020 0-OHM TO HELP ICT
06/07/05	(P 54,55) CHANGED HYNIX FRAME BUFFER TO 333S0341 (NEW HYNIX SCREEN, SAME PART)
06/13/05	(P 6) ADDED 338S0263 AS ALTERNATE FOR U4900 (RV351 GPU WITH EUTECTIC BUMPING) REV E RELEASE

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PROCESSORS

QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3055	1	PROCESSOR	FBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,KPA	2.0GHZ	1.20V	42W	?	U2900	CPU_2_0GHZ
337S3060	1	PROCESSOR	FBGA-576-1MM	IC,GPUL,DD3.1,1.8G,85C,JPA	1.8GHZ	1.20V	42W	?	U2900	CPU_1_8GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3061	337S3060	CPU_1_8GHZ	U2900	IC,DD3.1,1.8G,JRA	1.25V
337S2969	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BPA	1.20V
337S2970	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BRA	1.25V
337S2981	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BPL	1.20V
337S2982	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BRL	1.25V
337S2998	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BNA	1.20V
337S3093	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KQA	1.15V
337S3056	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KRA	1.25V
337S3058	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CPA	1.20V
337S3059	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CRA	1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0320	1	IC,U3LITE,NEW LAM,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0321	343S0320		U3	U3L,NEW LAM,200MM
343S0284	343S0320		U3	U3L,OLD LAM,300MM
343S0282	343S0320		U3	U3L,OLD LAM,200MM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0324	1	IC,ASIC,VESTA,V1.3	U8600	

MISC PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
	062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
	820-1747	1	PCB,FAB,MLB	MLB1	
	825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
	051-6772	1	PCB,SCHEM,MLB	SCH1	
	341T1667	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
	341T1703	1	IC,SMU,Q45C/D	U1300	
CRITICAL	603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL	603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702,LED5900	KINGBRIGHT LED
376S0204	376S0130		Q3310,Q3320,Q3410	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q3311,Q3321,Q3411	MOSFET,N-CH,VISHAY
353S0960	353S0733		VRA201	MAX8510,L-F PART
353S0958	353S0653		U1301	DS1338, L-F PART
353S0687	353S0959		U9800	MAX9722 LEAD
353S0539	353S0898		VRA200	LM1117 LEAD
338S0263	338S0231		U4900	RV351 GPU EUTECTIC

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TABLE ITEMS

SYNC_MASTER=N/A SYNC_DATE=N/A

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8	7	6	5	4	3	2	1

I307	NO_TEST=YES	TP_FBBCS1_L	52
I824	NO_TEST=YES	AGP_CLK66M_GPU_R	27
I825	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
I826	NO_TEST=YES	AUD_4V5_FB	102
I828	NO_TEST=YES	CPU_HTBEN_R	27
I829	NO_TEST=YES	EI_CPU_SYNC_R	27
I831	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
I832	NO_TEST=YES	EI_NB_SYNC_R	27
I834	NO_TEST=YES	ERROR_LED	8
I833	NO_TEST=YES	HT_CLK66M_NB_R	27
I835	NO_TEST=YES	HT_CLK66M_SB_R	27
I838	NO_TEST=YES	HT_VREF_DEBUG	64
I837	NO_TEST=YES	ITS_RUNNING	7
I836	NO_TEST=YES	LED801_1	8
I839	NO_TEST=YES	LED802_1	8
I841	NO_TEST=YES	PCI_CLK66M_SB_INT_R	27
I840	NO_TEST=YES	PCI_CLK_P3_R	27
I842	NO_TEST=YES	PCI_CLK_P4_R	27
I845	NO_TEST=YES	PN1	33
I844	NO_TEST=YES	PN2	33
I843	NO_TEST=YES	PN3	34
I846	NO_TEST=YES	Q800_D	8
I847	NO_TEST=YES	Q800_G	8
I848	NO_TEST=YES	Q801_B	8
I849	NO_TEST=YES	Q802_B	8
I850	NO_TEST=YES	Q802_E	8
I851	NO_TEST=YES	Q803_B	8
I852	NO_TEST=YES	Q901_GATE	9
I853	NO_TEST=YES	Q902_DRAIN	9
I854	NO_TEST=YES	Q1002_DRAIN	10
I337	NO_TEST=YES	TP_AGP_MB_AGP8X_DET_L	48
I338	NO_TEST=YES	TP_ATTENTION	29
I344	NO_TEST=YES	TP_AFN	29
I345	NO_TEST=YES	TP_PSRO1	29
I346	NO_TEST=YES	TP_PSRO2	29
I347	NO_TEST=YES	TP_PSYNCOUT	29
I348	NO_TEST=YES	TP_USB2_PWREN<2>	92
I350	NO_TEST=YES	TP_USB2_PWREN<3>	92
I349	NO_TEST=YES	TP_USB2_PWREN<4>	92

I356	NO_TEST=YES	TP_NEC_NTEST1	77
I357	NO_TEST=YES	TP_NEC_SMC	77
I358	NO_TEST=YES	TP_NEC_SMI_L	77
I360	NO_TEST=YES	TP_NEC_SRCLK	77

I362	NO_TEST=YES	TP_NEC_SRMOD	77
I363	NO_TEST=YES	TP_NEC_TEB	77
I361	NO_TEST=YES	TP_NEC_TEST	77
I364	NO_TEST=YES	TP_PLS_CLK_66M_0	27
I365	NO_TEST=YES	TP_PLS_CLK_66M_1	27
I372	NO_TEST=YES	TP_PLS_REF_CML	27
I373	NO_TEST=YES	TP_PLS_TEST1	27
I371	NO_TEST=YES	TP_PLS_TEST2	27
I374	NO_TEST=YES	TP_PLS_TEST3	27
I375	NO_TEST=YES	TP_SB_FSTEST	25
I376	NO_TEST=YES	TP_SB_PLLTEST	25
I377	NO_TEST=YES	TP_VREF_CG	48
I378	NO_TEST=YES	TP_SB_NC_P7	91
I380	NO_TEST=YES	TP_SB_NC_P8	91
I379	NO_TEST=YES	TP_SB_NC_R3	91
I382	NO_TEST=YES	TP_SB_NC_R4	91
I383	NO_TEST=YES	TP_SB_NC_R5	91
I381	NO_TEST=YES	TP_SB_NC_R6	91
I384	NO_TEST=YES	TP_SB_NC_R7	91
I385	NO_TEST=YES	TP_SB_NC_R8	91
I386	NO_TEST=YES	TP_SB_NC_T1	91
I388	NO_TEST=YES	TP_SB_NC_T2	91
I387	NO_TEST=YES	TP_SB_NC_T3	91
I390	NO_TEST=YES	TP_SB_NC_T4	91
I389	NO_TEST=YES	TP_SB_NC_T5	91
I391	NO_TEST=YES	TP_SB_NC_T6	91
I393	NO_TEST=YES	TP_SB_NC_T7	91
I392	NO_TEST=YES	TP_SB_NC_T8	91
I395	NO_TEST=YES	TP_SB_NC_U1	91
I394	NO_TEST=YES	TP_SB_NC_U2	91
I396	NO_TEST=YES	TP_SB_NC_U3	91
I398	NO_TEST=YES	TP_SB_NC_U4	91
I397	NO_TEST=YES	TP_SB_NC_U5	91
I399	NO_TEST=YES	TP_SB_NC_U6	91
I401	NO_TEST=YES	TP_SB_NC_V1	91
I400	NO_TEST=YES	TP_SB_NC_V2	91
I403	NO_TEST=YES	TP_SB_NC_V3	91
I402	NO_TEST=YES	TP_SB_NC_V4	91
I404	NO_TEST=YES	TP_SB_NC_W1	91
I405	NO_TEST=YES	TP_SB_NC_W3	91
I406	NO_TEST=YES	TP_SB_NC_Y1	91
I408	NO_TEST=YES	TP_SB_NC_Y3	91
I407	NO_TEST=YES	TP_SATA_CLK25M	27
I429	NO_TEST=YES	TP_USB2_PWREN<0>	92
I428	NO_TEST=YES	TP_USB2_PWREN<1>	92
I431	NO_TEST=YES	TP_DUMMY_A	24
I430	NO_TEST=YES	TP_DUMMY_B	24
I432	NO_TEST=YES	TP_RAM_CKE_R<2>	8
I855	NO_TEST=YES	Q2201_GATE	22
I856	NO_TEST=YES	Q2202_DRAIN	22
I858	NO_TEST=YES	R904_P2	9
I857	NO_TEST=YES	R2204_P2	22
I860	NO_TEST=YES	RAM_CLK66M_NB_R	27

I434	NO_TEST=YES	TP_RAM_CKE_R<3>	8
I433	NO_TEST=YES	TP_RAM_CKE_R<6>	8
I436	NO_TEST=YES	TP_RAM_CKE_R<7>	8
I435	NO_TEST=YES	TP_RAM_CS_L_R<10>	8
I437	NO_TEST=YES	TP_RAM_CS_L_R<11>	8
I439	NO_TEST=YES	TP_RAM_CS_L_R<2>	8
I438	NO_TEST=YES	TP_RAM_CS_L_R<3>	8
I440	NO_TEST=YES	TP_RAM_MUXEN0	8
I441	NO_TEST=YES	TP_RAM_MUXEN4	8
I442	NO_TEST=YES	TP_NB_PM_SLEEP0	24
I444	NO_TEST=YES	TP_J4000_SJRESET_L	40
I443	NO_TEST=YES	TP_J4001_SJRESET_L	40
I781	NO_TEST=YES	U2100_UNUSED	21
I809	NO_TEST=YES	PLS_CLK_66M_0_R	27
I810	NO_TEST=YES	PLS_CLK_66M_1_R	27
I861	NO_TEST=YES	SATA_CLK25M_R	27

I866	NO_TEST=YES	SB_CLK25M_ATA_R	27
I867	NO_TEST=YES	TEK_HT_A7	64
I868	NO_TEST=YES	TEK_HT_A9	64
I869	NO_TEST=YES	TEK_HT_A10	64
I870	NO_TEST=YES	TEK_HT_A12	64
I872	NO_TEST=YES	TEK_HT_B10	64
I871	NO_TEST=YES	TEK_HT_B12	64
I878	NO_TEST=YES	TP_PCI_CLK_P4	8
I876	NO_TEST=YES	U900_COMP	9
I875	NO_TEST=YES	U900_GATE_H	9
I874	NO_TEST=YES	U900_GATE_L	9
I873	NO_TEST=YES	U900_SS	9
I879	NO_TEST=YES	U900_VC	9
I880	NO_TEST=YES	U900_VC_D	9
I881	NO_TEST=YES	U900_VC_R	9
I882	NO_TEST=YES	U1000_FEEDBACK	10
I883	NO_TEST=YES	UATA_DASP_L_DS	83

I884	NO_TEST=YES	RFBD<1>	53 54
I885	NO_TEST=YES	RFBD<2>	53 54
I886	NO_TEST=YES	RFBD<3>	53 54
I887	NO_TEST=YES	RFBD<4>	53 54
I888	NO_TEST=YES	RFBD<6>	53 54
I890	NO_TEST=YES	RFBD<7>	53 54
I889	NO_TEST=YES	RFBD<8>	53 54
I892	NO_TEST=YES	RFBD<9>	53 54
I891	NO_TEST=YES	RFBD<11>	53 54
I893	NO_TEST=YES	RFBD<12>	53 54
I895	NO_TEST=YES	RFBD<13>	53 54
I894	NO_TEST=YES	RFBD<14>	53 54
I897	NO_TEST=YES	RFBD<16>	53 54
I896	NO_TEST=YES	RFBD<18>	53 54
I898	NO_TEST=YES	RFBD<19>	53 54
I900	NO_TEST=YES	RFBD<21>	53 54
I899	NO_TEST=YES	RFBD<22>	53 54
I902	NO_TEST=YES	RFBD<23>	53 54
I901	NO_TEST=YES	RFBD<24>	53 54
I903	NO_TEST=YES	RFBD<25>	53 54
I904	NO_TEST=YES	RFBD<26>	53 54
I905	NO_TEST=YES	RFBD<28>	53 54
I906	NO_TEST=YES	RFBD<29>	53 54
I907	NO_TEST=YES	RFBD<30>	53 54
I908	NO_TEST=YES	RFBD<32>	53 54
I909	NO_TEST=YES	RFBD<33>	53 54
I910	NO_TEST=YES	RFBD<35>	53 54
I911	NO_TEST=YES	RFBD<36>	53 54
I912	NO_TEST=YES	RFBD<37>	53 54
I913	NO_TEST=YES	RFBD<38>	53 54
I915	NO_TEST=YES	RFBD<40>	53 54
I914	NO_TEST=YES	RFBD<42>	53 54
I916	NO_TEST=YES	RFBD<43>	53 54
I917	NO_TEST=YES	RFBD<45>	53 54
I919	NO_TEST=YES	RFBD<46>	53 54
I918	NO_TEST=YES	RFBD<47>	53 54
I920	NO_TEST=YES	RFBD<48>	53 54
I921	NO_TEST=YES	RFBD<49>	53 54

I922	NO_TEST=YES	U2200_COMP	22
I923	NO_TEST=YES	U2200_GATE_H	22
I925	NO_TEST=YES	U2200_GATE_L	22
I924	NO_TEST=YES	U2200_SS	22
I926	NO_TEST=YES	U2200_VC	22
I927	NO_TEST=YES	U2200_VC_D	22
I928	NO_TEST=YES	U2200_VC_R	22
I930	NO_TEST=YES	Q5001_GATE	50
I929	NO_TEST=YES	Q5002_DRAIN	50
I931	NO_TEST=YES	U3310_DRN	33
I932	NO_TEST=YES	U3320_DRN	33
I933	NO_TEST=YES	U3410_DRN	34
I934	NO_TEST=YES	U5000_COMP	50
I935	NO_TEST=YES	U5000_FEEDBACK	50
I936	NO_TEST=YES	U5000_GATE_H	50
I937	NO_TEST=YES	U5000_GATE_L	50
I938	NO_TEST=YES	U5000_SS	50
I939	NO_TEST=YES	U5000_VC	50

I947	NO_TEST=YES	TP_SATA_RXD_N2_C	83
I948	NO_TEST=YES	TP_SATA_RXD_P2_C	83
I949	NO_TEST=YES	TP_SATA_TXD_N2	83
I950	NO_TEST=YES	TP_SATA_TXD_P2	83

GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS:

I782	NO_TEST=TRUE	EI_CPU_TO_NB_AD<0..43>	14 28 29
I784	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	14 28 29
I785	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	14 28 29
I786	NO_TEST=TRUE	EI_CPU_TO_NB_SR_N<0..1>	14 28 29
I787	NO_TEST=TRUE	EI_CPU_TO_NB_SR_P<0..1>	14 28 29
I789	NO_TEST=TRUE	EI_NB_TO_CPU_AD<0..43>	14 28 29
I788	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	14 28 29
I790	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	14 28 29
I792	NO_TEST=TRUE	EI_NB_TO_CPU_SR_N<0..1>	14 28 29
I791	NO_TEST=TRUE	EI_NB_TO_CPU_SR_P<0..1>	14 28 29
I793	NO_TEST=YES	CHKSTOP_L	8 14 29
I794	NO_TEST=YES	CPU_HRESET_L	14 29 30
I795	NO_TEST=YES	CPU_INT_L	14 25 29 30
I796	NO_TEST=YES	CPU1_HTBEN	14
I797	NO_TEST=YES	EI_CPU1_CLK_N	14 27
I798	NO_TEST=YES	EI_CPU1_CLK_P	14 27
I799	NO_TEST=YES	EI_QACK_L	14 28 29
I800	NO_TEST=YES	EI_QREQ_L	14 28 29 30
I801	NO_TEST=YES	EI_SE	14 28 29 30
I802	NO_TEST=YES	I2C_SMU_A_SCL_OUT_L	13 14 18
I803	NO_TEST=YES	I2C_SMU_A_SDA_OUT_L	13 14 18
I804	NO_TEST=YES	MCP_L	14 29
I805	NO_TEST=YES	RI_L	14 29 30
I806	NO_TEST=YES	SYNCENABLE	14 29 30
I807	NO_TEST=YES	TP_PROC_TRIGGER_OUT	14 29
I808	NO_TEST=YES	EI_CPU1_SYNC	14 27
I827	NO_TEST=YES	CPU1_HTBEN_R	14 27
I830	NO_TEST=YES	EI_CPU1_SYNC_R	14 27

101	IN	AUD_MIC_IN_N_CONN		FUNC_TEST=TRUE
101	IN	AUD_MIC_IN_P_CONN		FUNC_TEST=TRUE
90	IN	FW_VP		FUNC_TEST=TRUE
101	IN	GND_AUDIO_MIC_CONN		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SCL		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SDA		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SCL		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SDA		FUNC_TEST=TRUE
36 33 31	IN	KPGND2		FUNC_TEST=TRUE
36 33 31	IN	KPVDD2		FUNC_TEST=TRUE
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
77 76 75 74 73	IN	PCI_AD<31..0>		FUNC_TEST=TRUE
77 76 74 73	IN	PCI_CBE_L<3..0>		FUNC_TEST=TRUE
8	IN	PCI_CLK33M_AIRPORT		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_REQ_L		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_GNT_L		FUNC_TEST=YES
76 25	IN	PCI_SLOTA_INT_L		FUNC_TEST=YES
74 56 8	IN	PCI_RESET_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_FRAME_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_TRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_IRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_STOP_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_DEVSEL_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_PAR		FUNC_TEST=YES
76	IN	PCI_SLOTA_IDSEL		FUNC_TEST=YES
76 75 74	IN	ROM_CS_L		FUNC_TEST=YES
76 75 74	IN	ROM_OE_L		FUNC_TEST=YES
76 75 74	IN	ROM_WE_L		FUNC_TEST=YES
76 75	IN	ROM_ONBOARD_CS_L		FUNC_TEST=YES
76	IN	AIRPORT_CLKRUN_L_PD		FUNC_TEST=YES
76	IN	USB_BT_N		FUNC_TEST=YES
76	IN	USB_BT_P		FUNC_TEST=YES
92	IN	USB2_PORT1_N_F		FUNC_TEST=YES
92	IN	USB2_PORT1_P_F		FUNC_TEST=YES
92	IN	USB2_PORT2_N_F		FUNC_TEST=YES
92	IN	USB2_PORT2_P_F		FUNC_TEST=YES
92	IN	USB2_PORT3_N_F		FUNC_TEST=YES
92	IN	USB2_PORT3_P_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT1_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT2_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT3_F		FUNC_TEST=YES
94 25	IN	I2S1_DEV_TO_SB_DTI	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SYNC	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_BITCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_MCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SB_TO_DEV_DTO	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_RESET_L	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	MODEM_RING2SYS_L	2 TEST POINTS	FUNC_TEST=YES
59 58	IN	TMDS_CKM		FUNC_TEST=YES
59 58	IN	TMDS_D1M		FUNC_TEST=YES
59	IN	PPVCC_TMDS		FUNC_TEST=YES
59	IN	PP3V3_DDC		FUNC_TEST=YES
59	IN	TD0M		FUNC_TEST=YES
59	IN	TD0P		FUNC_TEST=YES
59	IN	TD1P		FUNC_TEST=YES
59	IN	TD2M		FUNC_TEST=YES
59	IN	TD2P		FUNC_TEST=YES
59	IN	TCKP		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 7	IN	GND_CHASSIS_TMDS		FUNC_TEST=YES
59	IN	FILT_ANALOG_RED		FUNC_TEST=YES
59	IN	FILT_ANALOG_GRN		FUNC_TEST=YES
59	IN	FILT_ANALOG_BLU		FUNC_TEST=YES
59	IN	VGA_HSYNC_R		FUNC_TEST=YES
59	IN	VGA_VSYNC_R		FUNC_TEST=YES
59 58	IN	MON_DETECT		FUNC_TEST=YES
59	IN	PP24V_INV		FUNC_TEST=YES
59	IN	GND_20_INV		FUNC_TEST=YES
59	IN	INV_20_LCD_PWM_		FUNC_TEST=YES
59	IN	INV_20_CUR_HI_F		FUNC_TEST=YES
59	IN	GND_17_INV		FUNC_TEST=YES
59	IN	PP5V_AGP_RL		FUNC_TEST=YES
59	IN	INV_17_LCD_PWM_F		FUNC_TEST=YES
59	IN	INV_17_CUR_HI_F		FUNC_TEST=YES
33 8	IN	CPU_VID_R<5..0>		FUNC_TEST=TRUE
36	IN	KPVDD2_FMAX		FUNC_TEST=YES
36	IN	KPGND2_FMAX		FUNC_TEST=YES
36	IN	TDIODE_POS_FMAX		FUNC_TEST=YES
36	IN	TDIODE_NEG_FMAX		FUNC_TEST=YES
36 33	IN	CORE_ISNS_M		FUNC_TEST=YES
36 33	IN	CORE_ISNS_P		FUNC_TEST=YES

PP12V_RUN PP5V_RUN PP24V_RUN
PP5V_ALL PP3V3_RUN

	IN	PP12V_RUN	10 TEST POINTS	FUNC_TEST=YES
12 11 7	IN	PP5V_ALL	5 TEST POINTS	FUNC_TEST=YES
18 11 10 7	IN	PP5V_RUN	5 TEST POINTS	FUNC_TEST=YES
50 34 22 18 11 10 7	IN	PP3V3_RUN	5 TEST POINTS	FUNC_TEST=YES
	IN	PP24V_RUN	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP5V_DISK	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP12V_DISK	5 TEST POINTS	FUNC_TEST=YES
	IN	GND	12 TEST POINTS	FUNC_TEST=YES

PP2V5_RUN PP5V_PWRON PP1V2_PWRON
PP1V5_RUN PP3V3_PWRON

	IN	PP2V5_RUN		FUNC_TEST=YES
	IN	PP1V5_RUN		FUNC_TEST=YES
18 11	IN	PP5V_PWRON		FUNC_TEST=YES
58 27 18 11	IN	PP3V3_PWRON		FUNC_TEST=YES
	IN	PP1V2_PWRON		FUNC_TEST=YES
23 7 3	IN	=PPVCORE_PWRON_SB		FUNC_TEST=YES
13 8 7	IN	=PP3V3_ALL_SMU		FUNC_TEST=TRUE
31 8 7 3	IN	=PP5V_RUN_CPU		FUNC_TEST=YES
22	IN	PPVCORE_NB		FUNC_TEST=YES
35 34 33 7	IN	PPVCORE_CPU		FUNC_TEST=YES
34 33	IN	PP12V_CPU		FUNC_TEST=YES
33	IN	VCORE_SENSE_GND		FUNC_TEST=YES
33	IN	VCORE_SENSE_VOUT		FUNC_TEST=YES
8 7	IN	SMU_MANUAL_RESET_L	2 TEST POINTS	FUNC_TEST=YES
13 7	IN	SYS_POWER_BUTTON_L	2 TEST POINTS	FUNC_TEST=YES
7	IN	POWER_BUTTON_L		FUNC_TEST=YES
7	IN	RESET_BUTTON_L		FUNC_TEST=YES
13 8	IN	SMU_RESET_L		FUNC_TEST=YES
33 13 11 10 7	IN	SYS_POWERUP_L		FUNC_TEST=YES
50 46 22 11 10 9 8 59	IN	SYS_SLEEP		FUNC_TEST=YES
13 8	IN	SYS_POWERFAIL_L		FUNC_TEST=YES
9	IN	U900_FEEDBACK		FUNC_TEST=YES
22	IN	U2200_FEEDBACK		FUNC_TEST=YES
59 58	IN	ANALOG_RED		FUNC_TEST=YES
59 58	IN	ANALOG_GRN		FUNC_TEST=YES
59 58	IN	ANALOG_BLU		FUNC_TEST=YES
101 25	IN	AUDIO_LO_DET_L		FUNC_TEST=YES
75	IN	ROM_WP_L		FUNC_TEST=YES
83 80	IN	UATA_DD<15..0>		FUNC_TEST=TRUE
83 80	IN	UATA_DA<2..0>		FUNC_TEST=TRUE
83 80	IN	UATA_CS0_L		FUNC_TEST=YES
83 80	IN	UATA_CS1_L		FUNC_TEST=YES
83 80	IN	UATA_RESET_L		FUNC_TEST=YES
83	IN	UATA_DSTROBE_R		FUNC_TEST=YES
83 80	IN	UATA_HSTROBE		FUNC_TEST=YES
83 8066 83 80	IN	UATA_STOP		FUNC_TEST=YES
83	IN	UATA_DMARQ_R		FUNC_TEST=YES
83 80	IN	UATA_DMACK_L		FUNC_TEST=YES
83	IN	UATA_INTRQ_R		FUNC_TEST=YES
83	IN	UATA_IOCS16_PU		FUNC_TEST=YES
83	IN	UATA_CSEL_PD		FUNC_TEST=YES
83	IN	UATA_DASP_L		FUNC_TEST=TRUE
36 31	IN	TDIODE_NEG		FUNC_TEST=YES

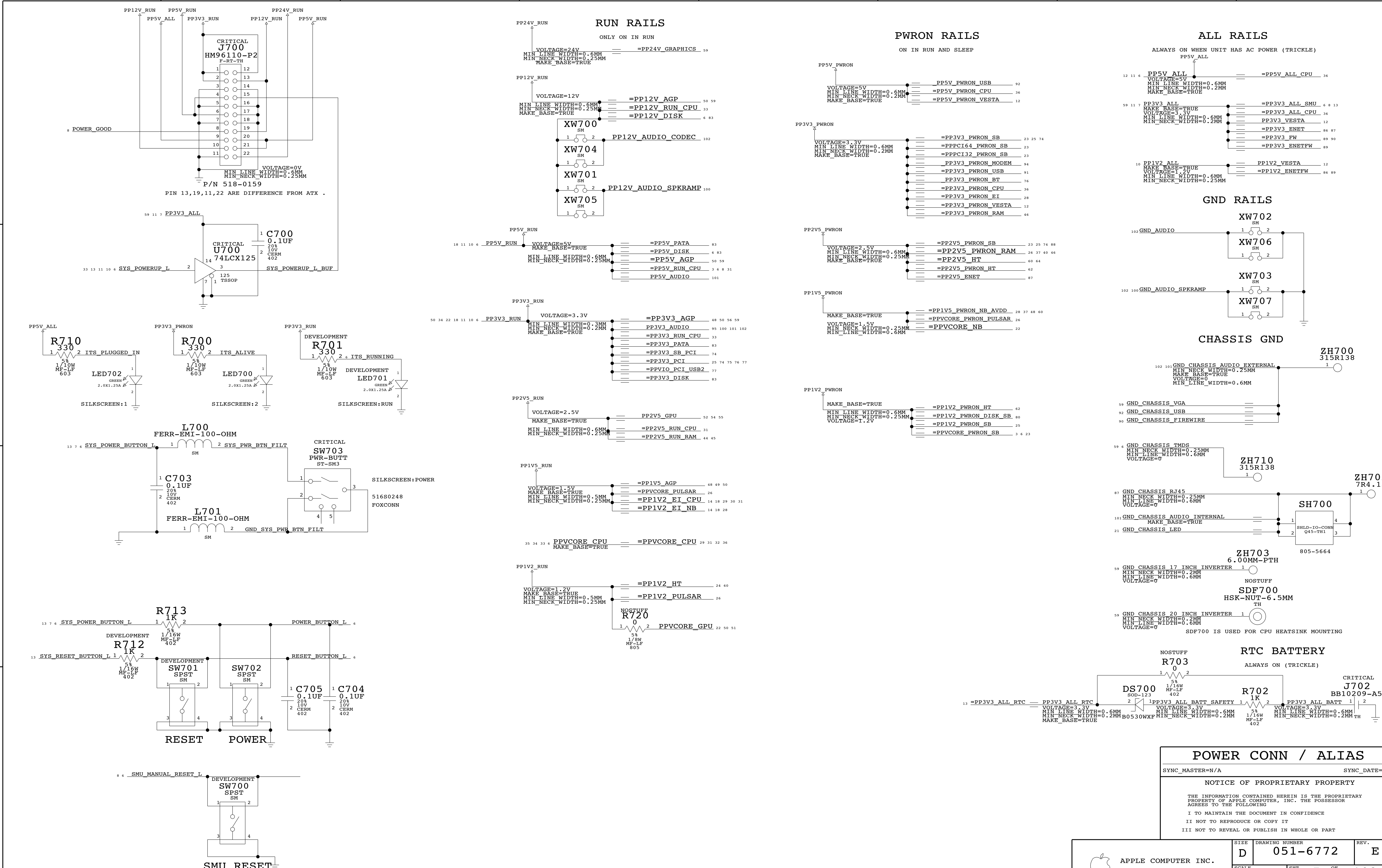
FUNC TEST

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6772 REV. E

SCALE NONE SHT 6 OF 102



POWER CONN / ALIAS

SYNC_MASTER=N/A SYNC_DATE=N/A

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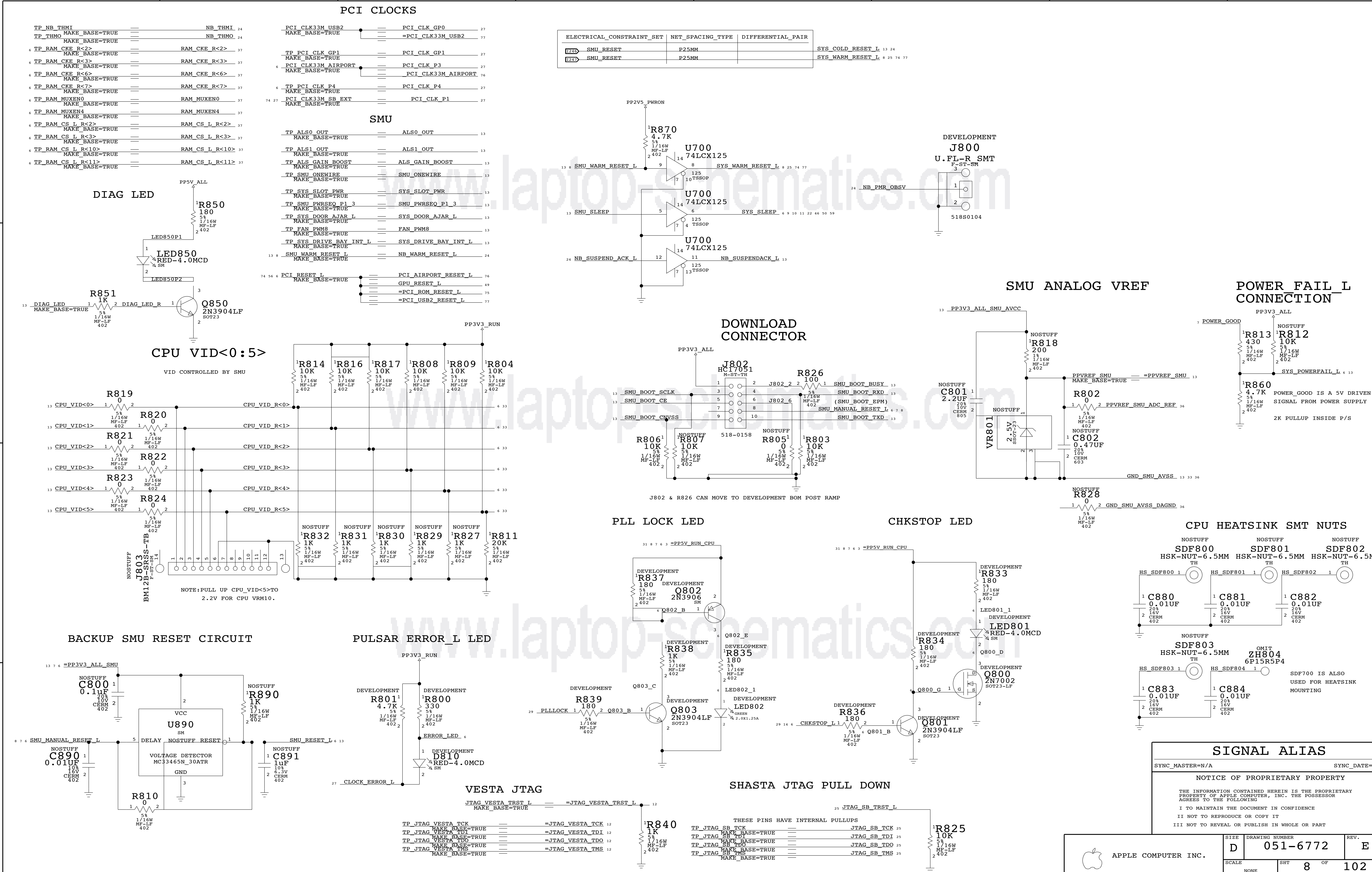

SIGNAL ALIAS

SYNC_MASTER=N/A SYNC_DATE=N/A

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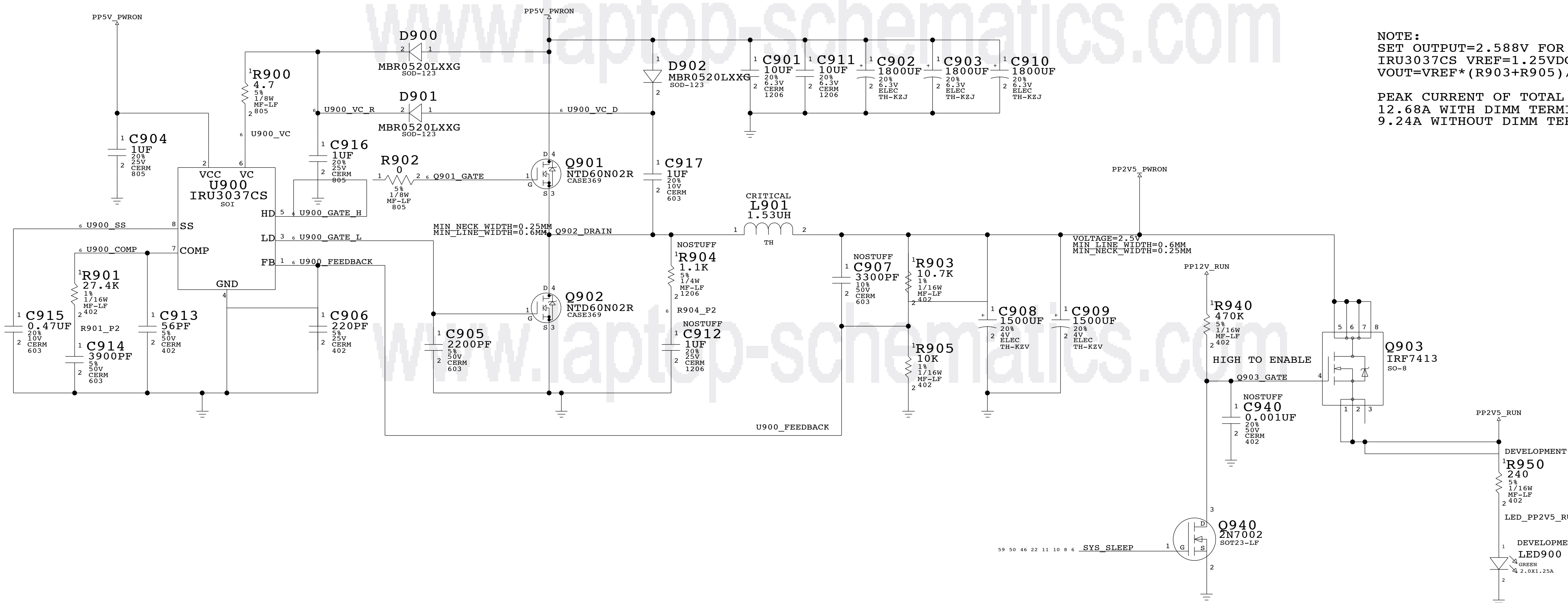
2.5V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=2.588V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.588VDC

PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

2.5V VREG	
SYNC_MASTER=N/A	SYNC_DATE=N/A

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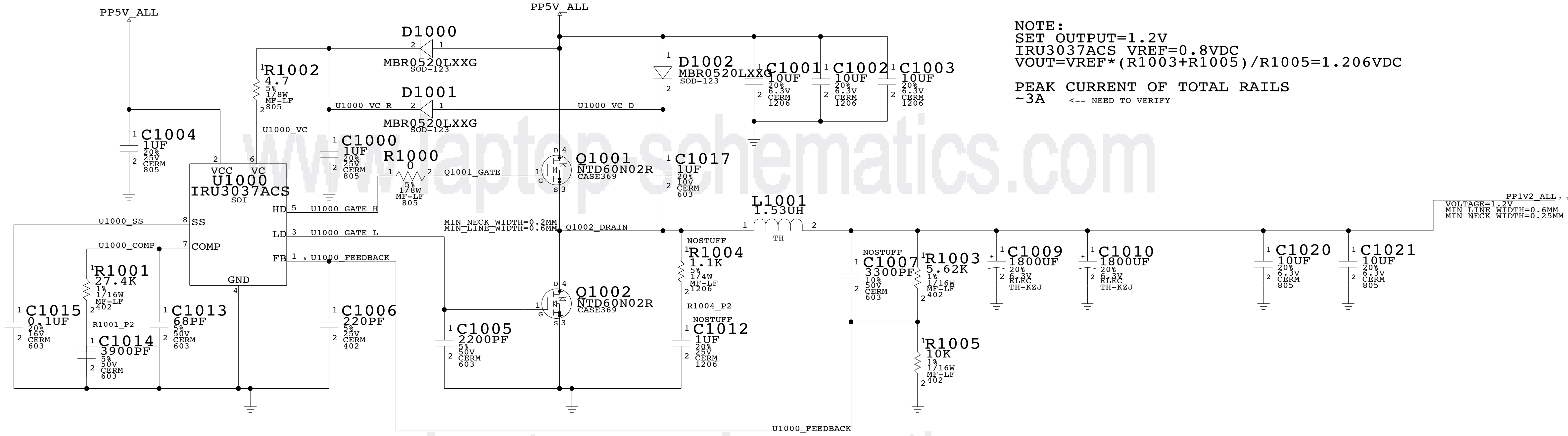
	SCALE NONE	SHT 9 OF 102	

PP1V2_ALL VOLTAGE REGULATOR

NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
~3A <-- NEED TO VERIFY

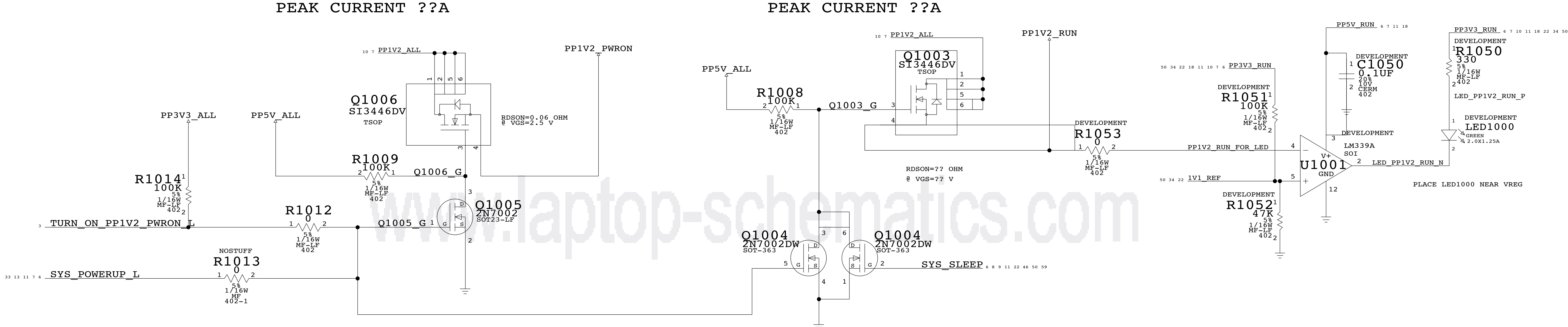


PP1V2_PWRON FET SWITCH

PEAK CURRENT ??A

PP1V2_RUN FET SWITCH

PEAK CURRENT ??A



1.2V VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

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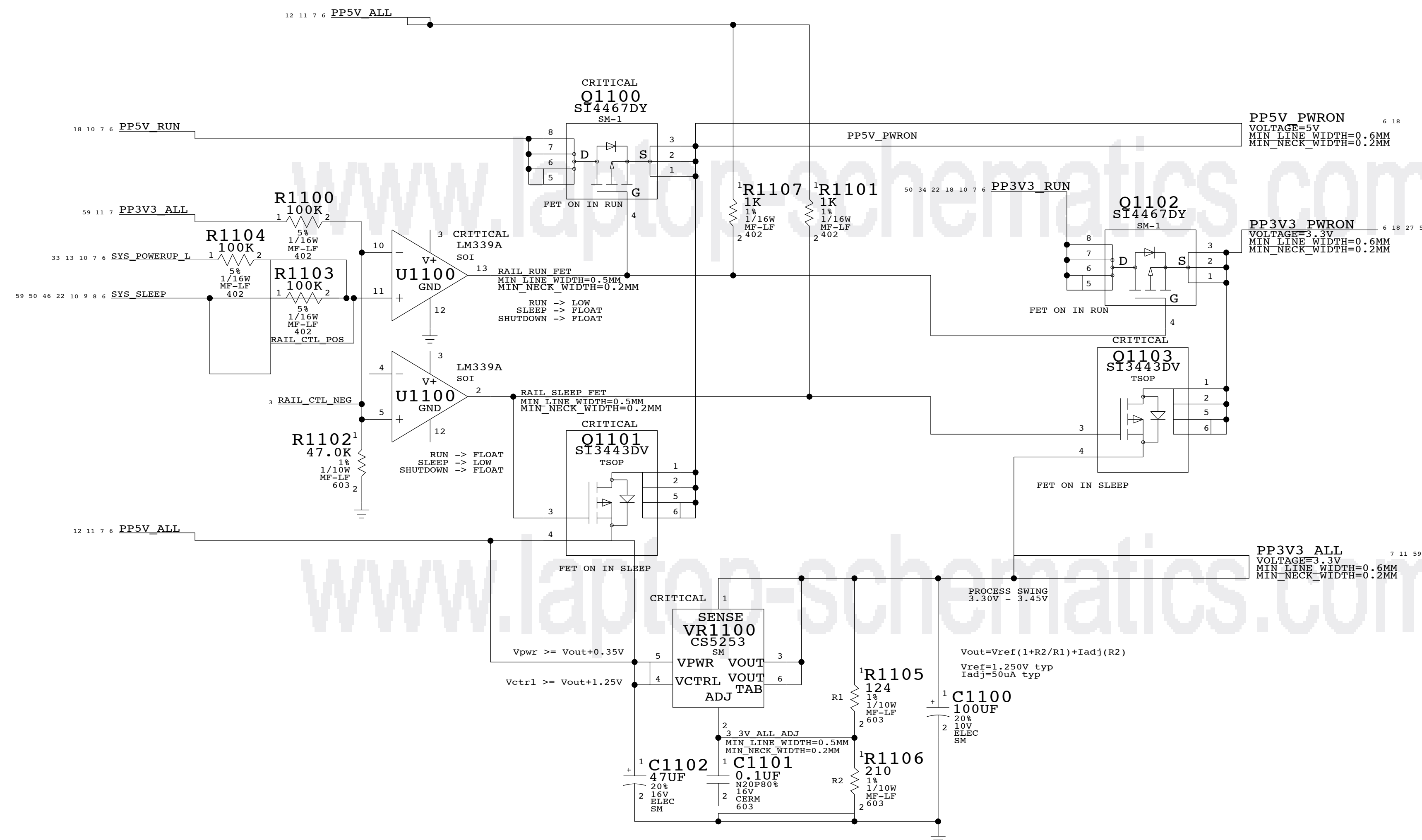

5V & 3.3V VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

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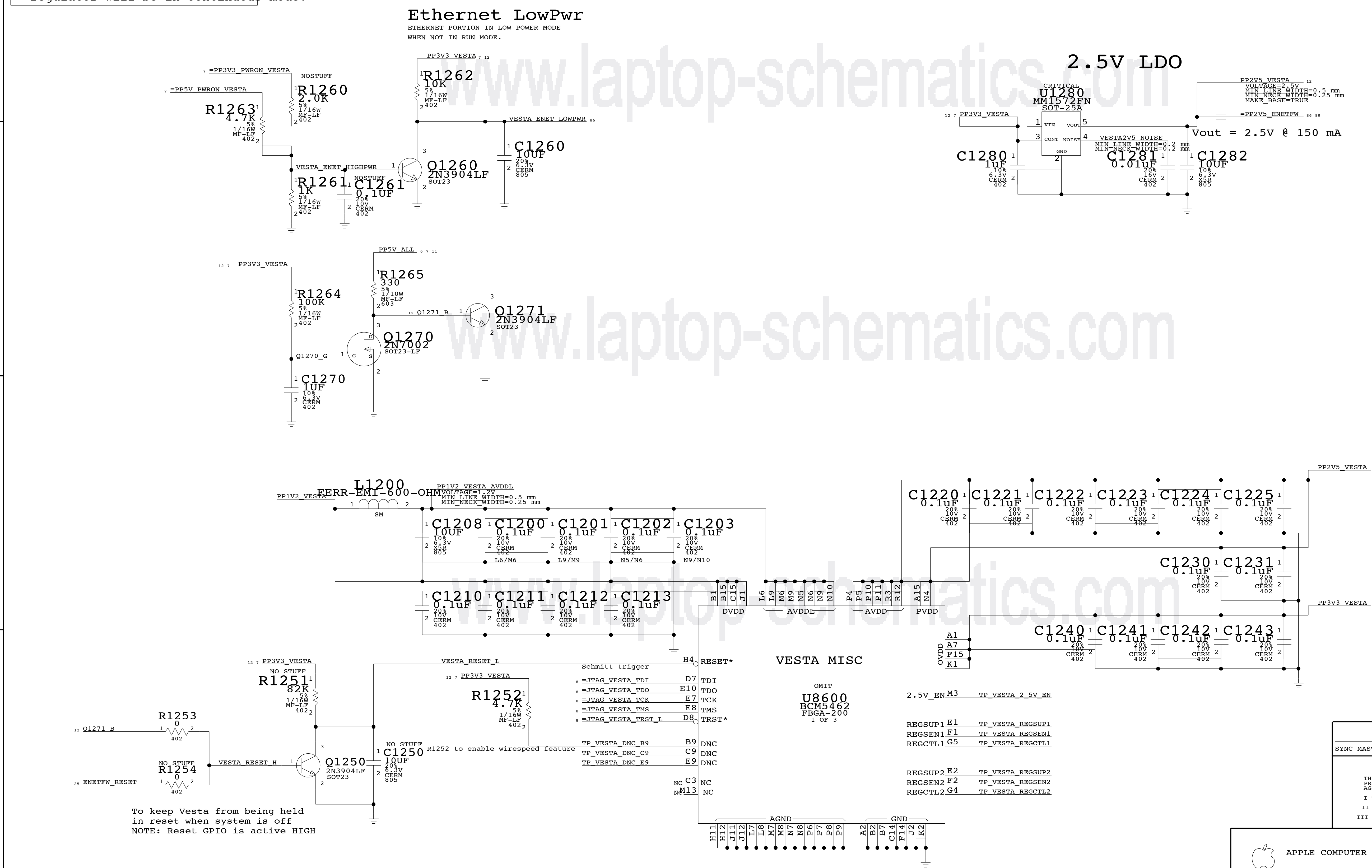
Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V
  regulator. If both options are off the
  regulator will be in continuous mode.



Vesta Core / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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D	051-6772	E
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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	P25MM		SMU_CLK10M_XIN
	P25MM		SMU_CLK10M_XOUT
	P25MM		SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	P25MM		RTC_CLK32K_X1
	P25MM		RTC_CLK32K_X2

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

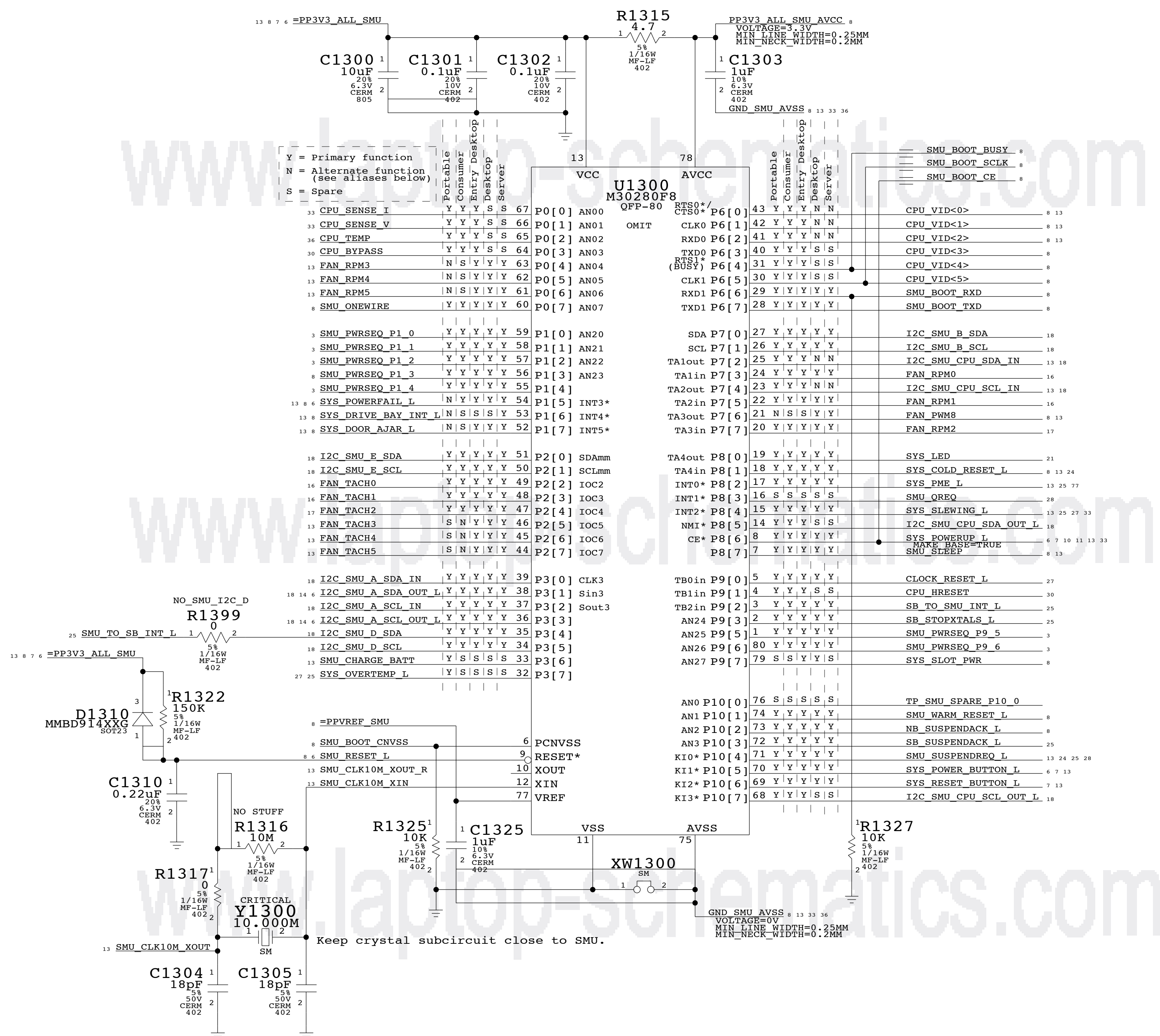
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

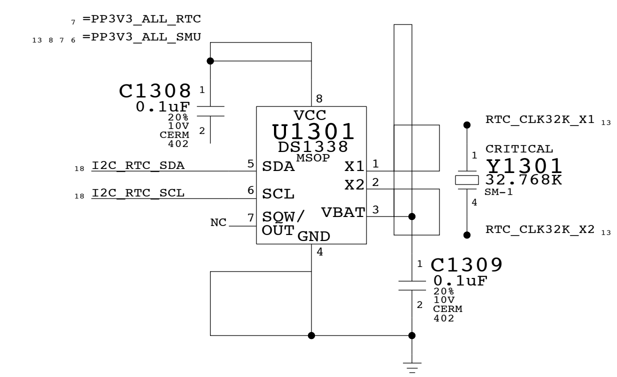
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

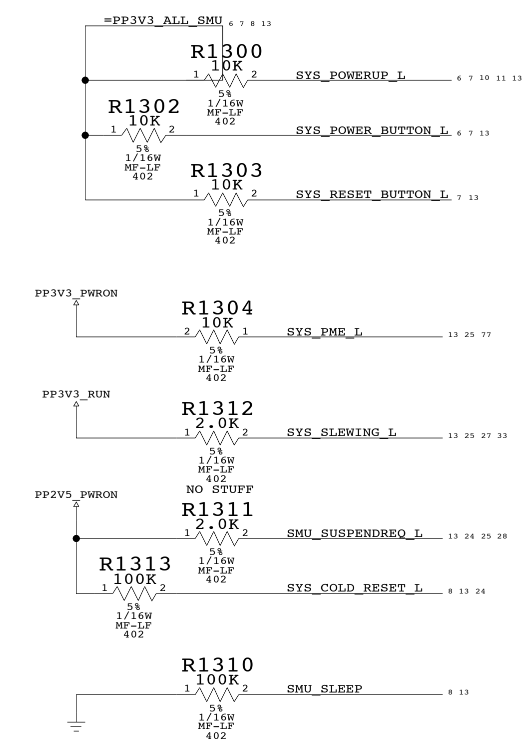
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4	—	ALS0_OUT
FAN_RPM4	0.5	—	ALS1_OUT
FAN_RPM5	0.6	—	ALS_GAIN_BOOST
SYS_POWERFAIL_L	1.5	—	SMU_ACIN
SYS_DRIVE_BAY_INT_L	1.6	—	SMU_BATT_DET_L
SYS_DOOR_AJAR_L	1.7	—	SYS_LID_OPEN
FAN_PWM8	7.6	—	SYS_KBDLED

Consumer

	Port		
FAN_TACH3	2.5	—	SYS_LED_RED
FAN_TACH4	2.6	—	SYS_LED_GREEN
FAN_TACH5	2.7	—	SYS_LED_BLUE
SMU_CHARGE_BATT	3.6	—	DIAG_LED

Tower & Server

	Port		
CPU_VID<0>	6.0	—	FAN_TACH6
CPU_VID<1>	6.1	—	FAN_TACH7
CPU_VID<2>	6.2	—	FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2	—	FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4	—	FAN_PWM7

System Management Unit

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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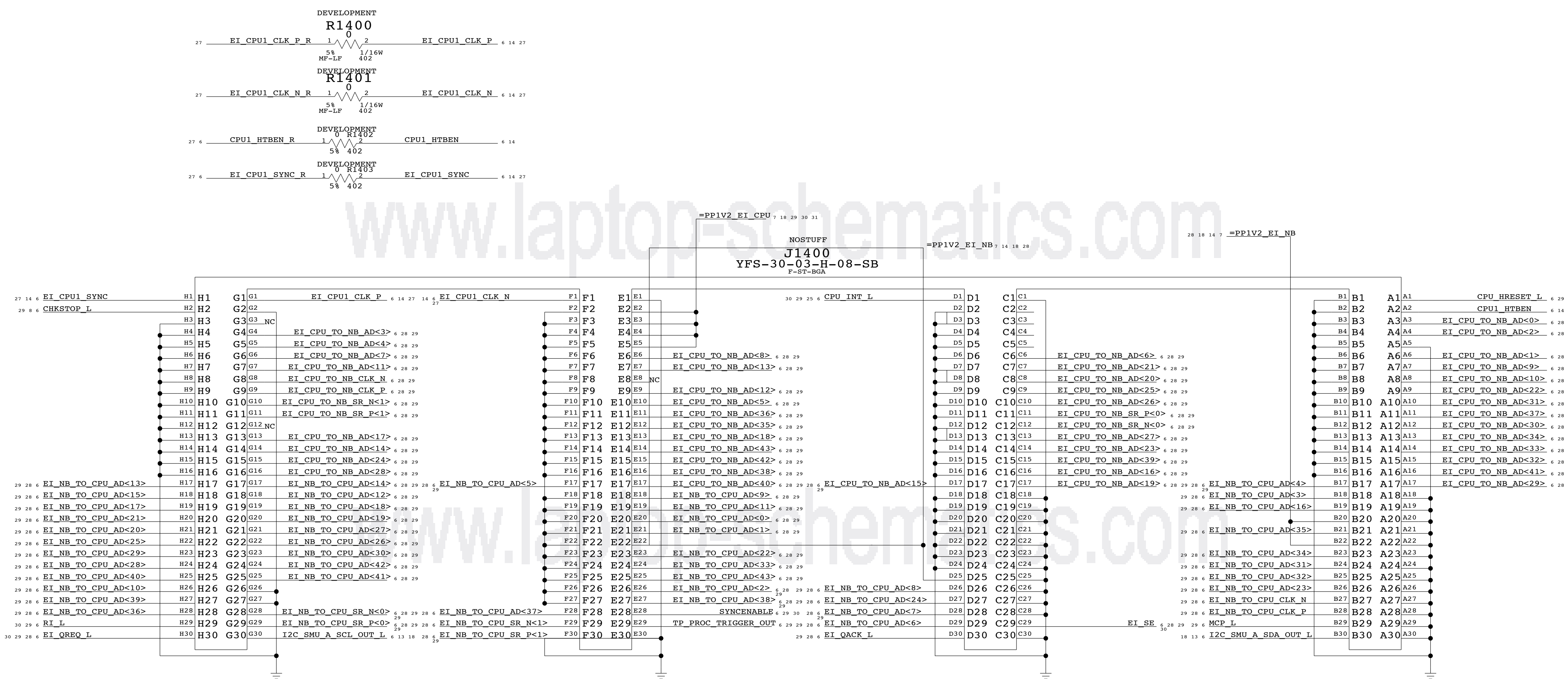

CPU LOGIC ANALYZER

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6772	E
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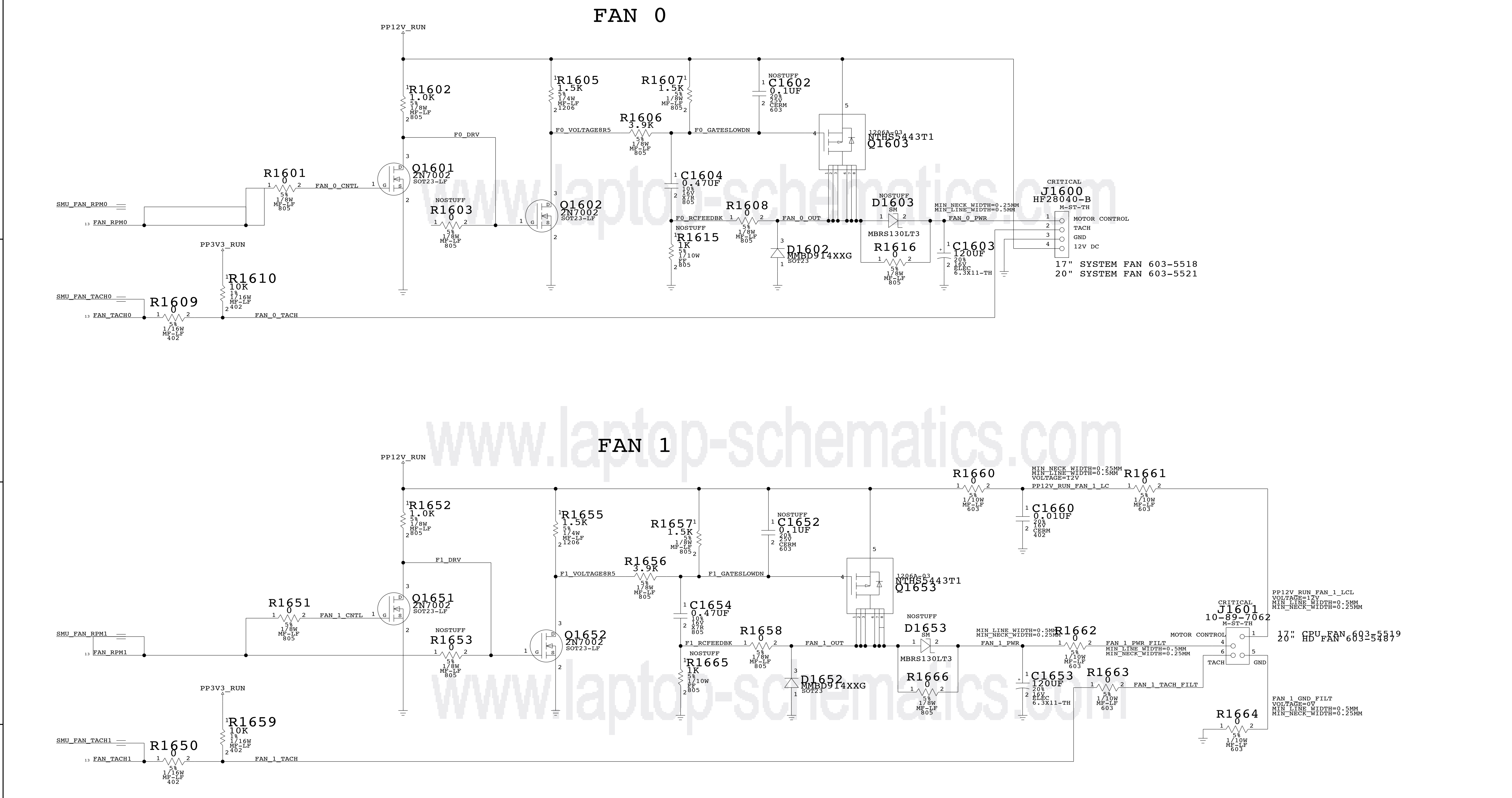

FAN 0, 1 & SYSTEM TEMP

SYNC_MASTER=N/A SYNC_DATE=N/A

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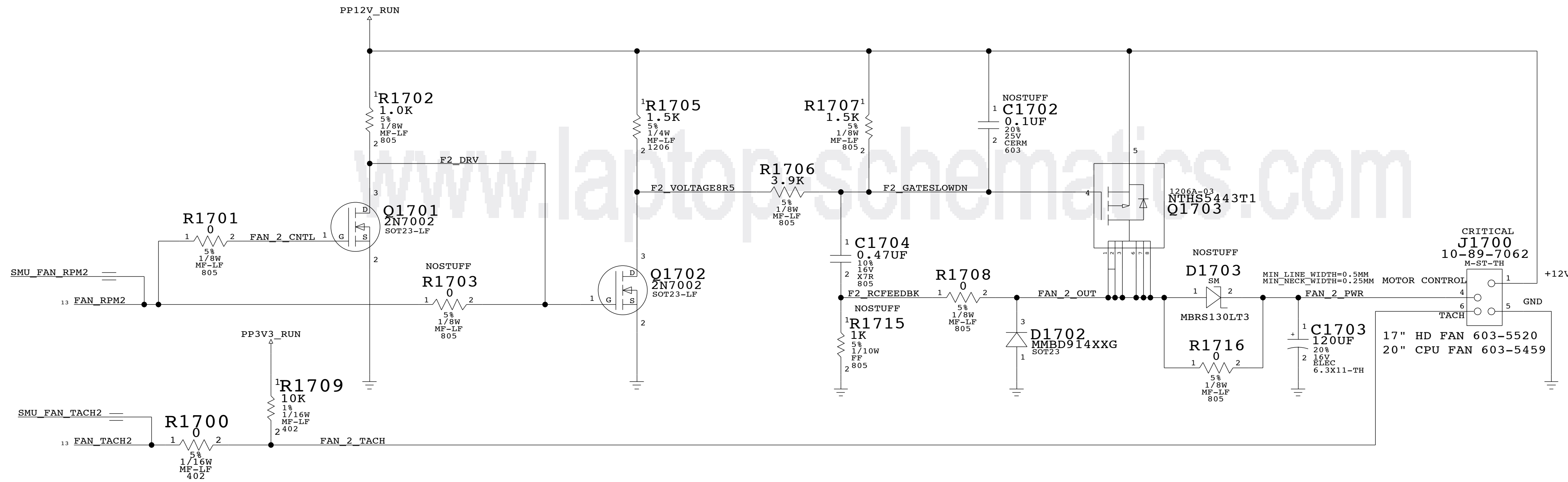
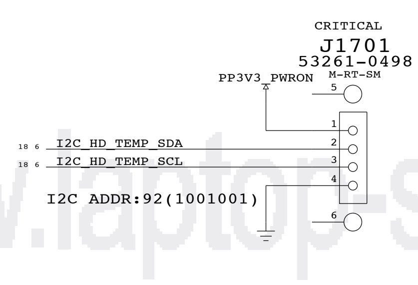
FAN 2



REMOTE HARD DRIVE TEMP SENSOR



FAN 2 & HD TEMP

SYNC_MASTER=N/A SYNC_DATE=N/A

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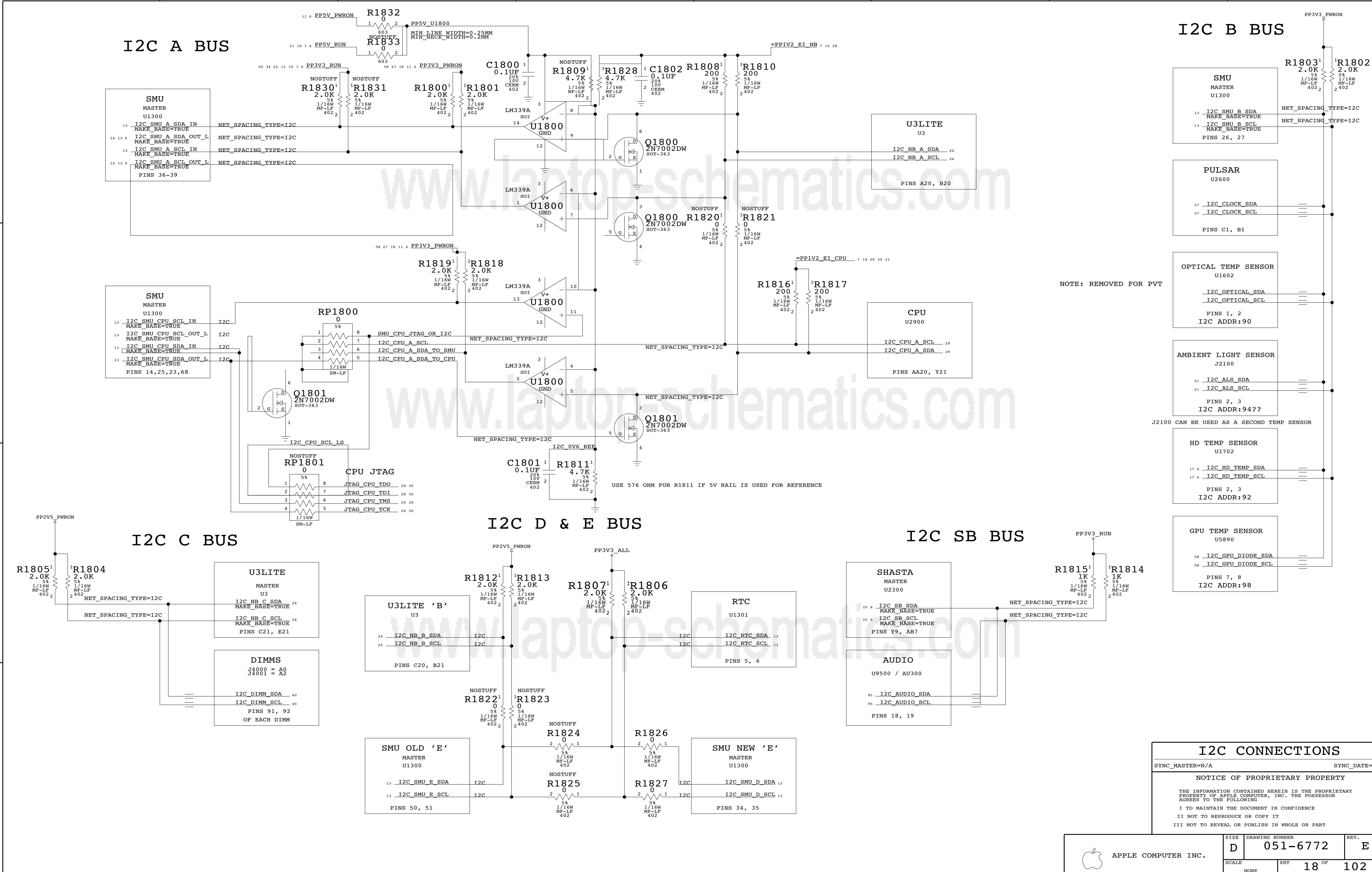
D	051-6772	E
SCALE NONE	SHT 17 OF 102	



I2C CONNECTIONS

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D	051-6772	E
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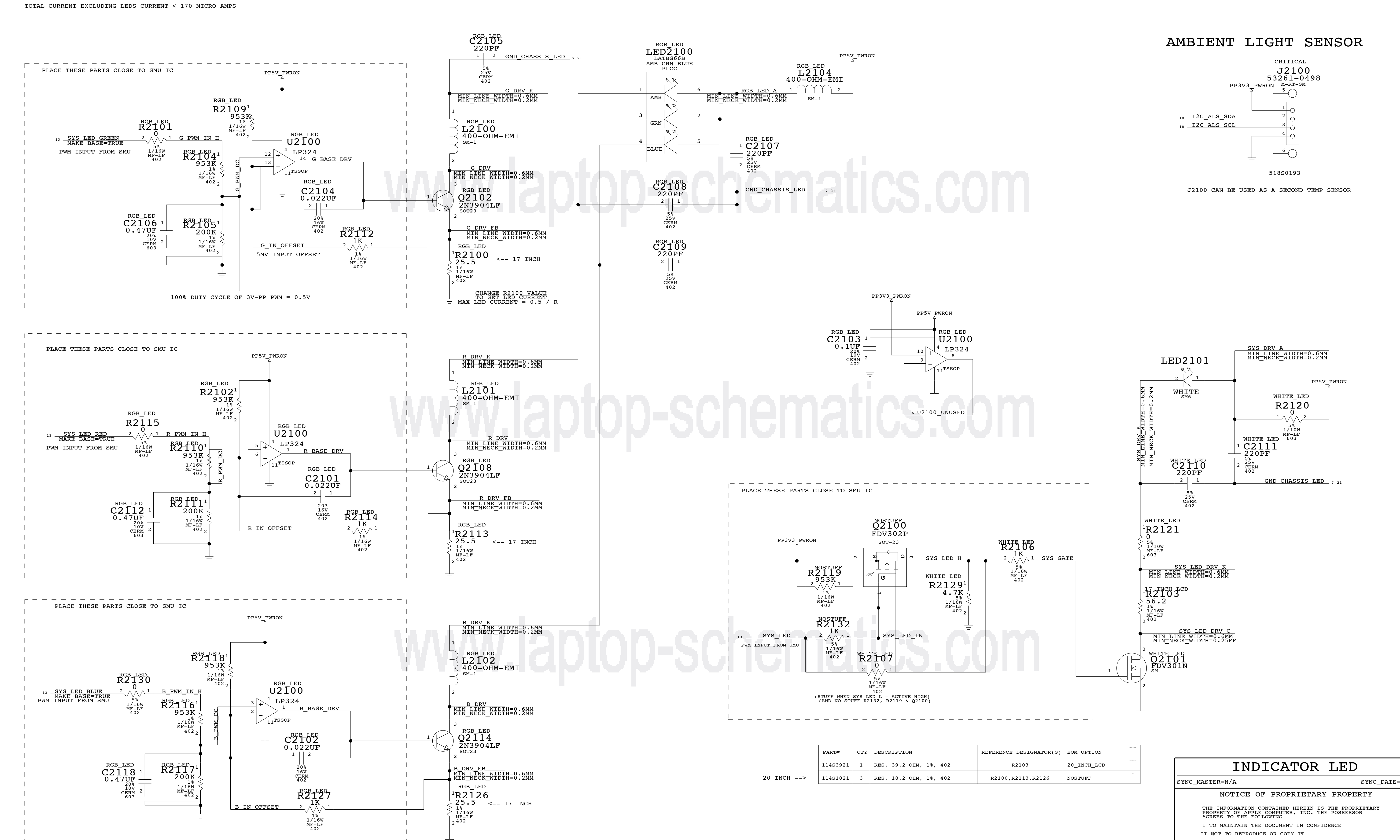

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
114S1821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

20 INCH -->

INDICATOR LED

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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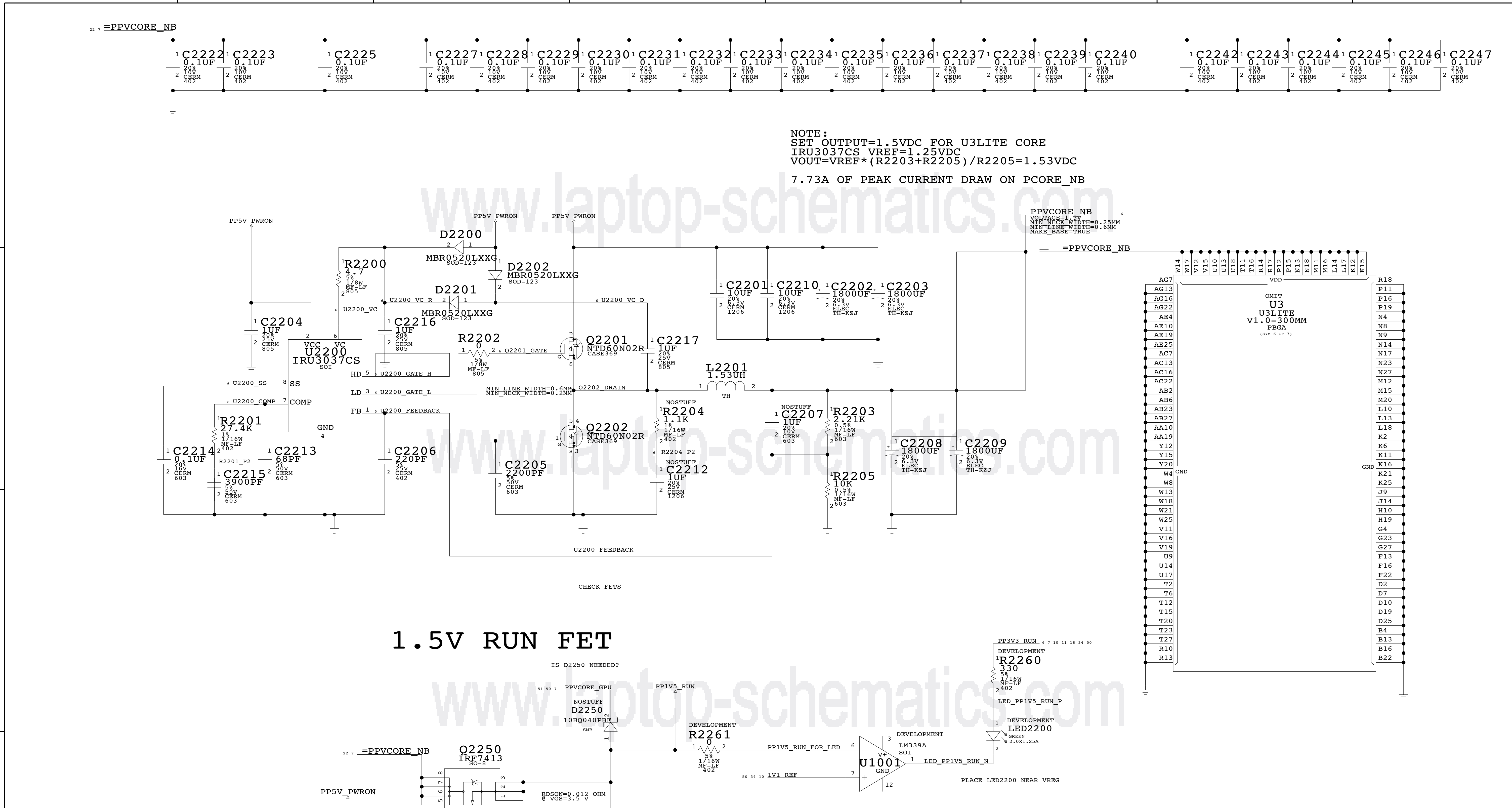

U3LITE CORE POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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Page Notes

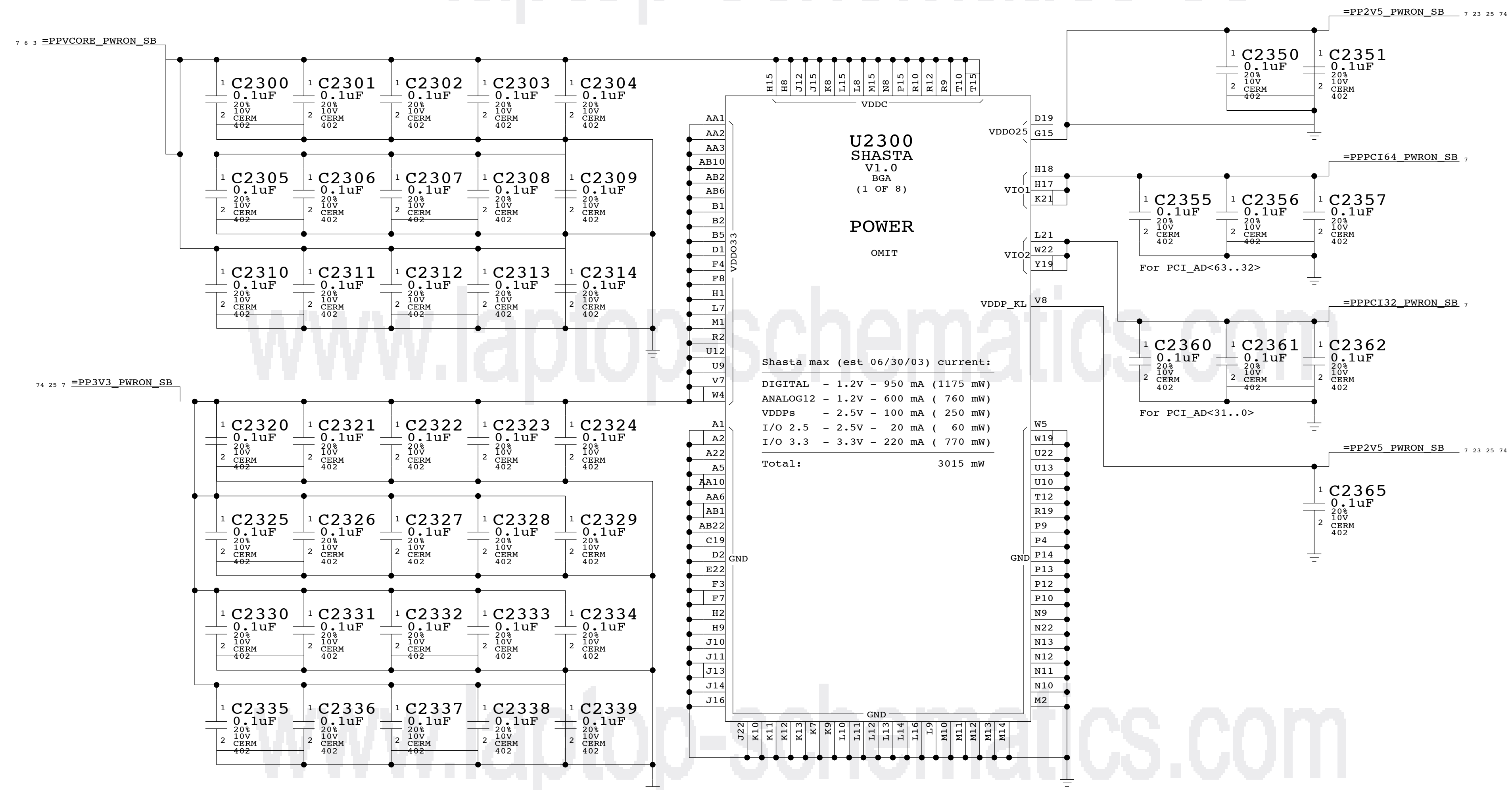
Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power

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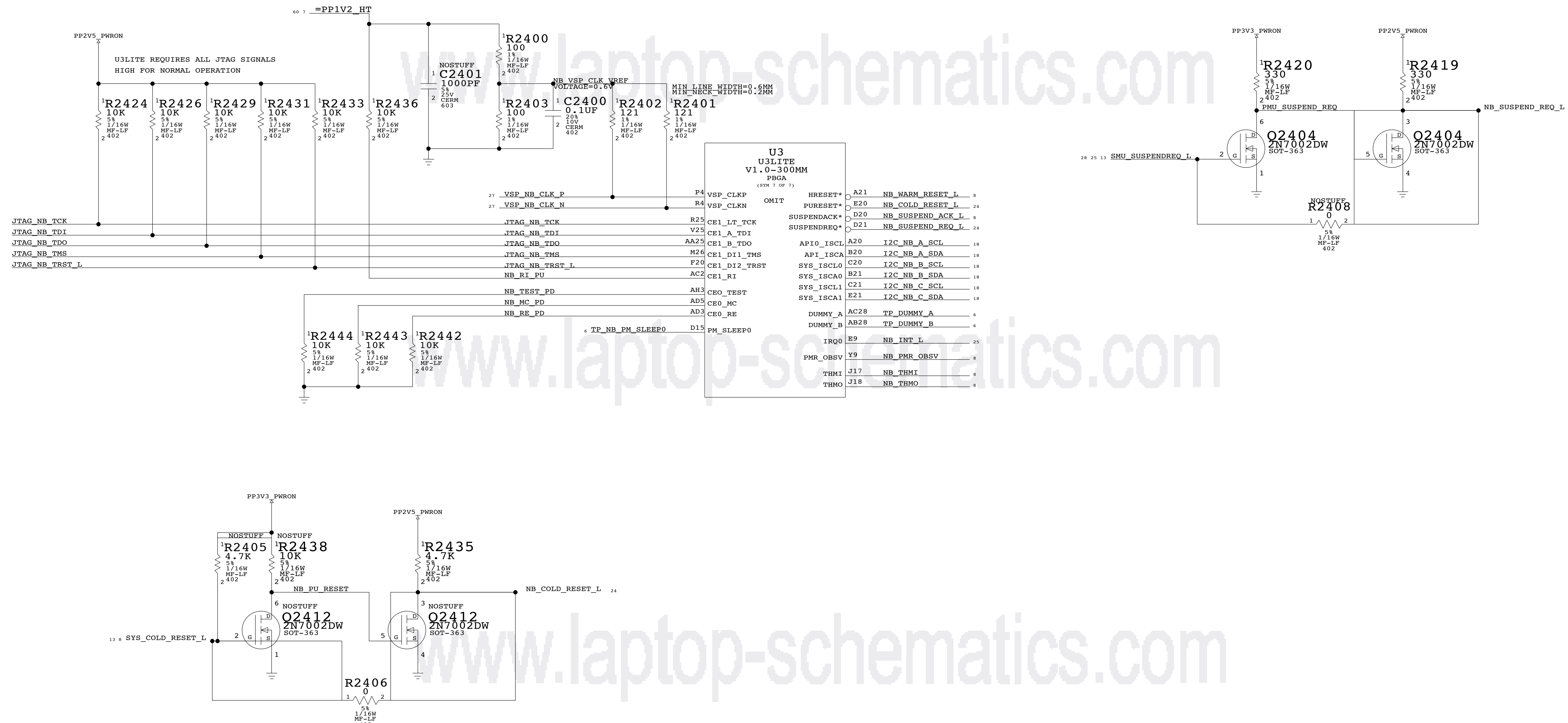
D	051-6772	E
SCALE NONE	SHT 23 OF 102	



U3LITE MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO
I2S0_TO_DEV	AUDIO		I2S0_MCLK
I2S0_BIDIR			I2S0_BITCLK
I2S0_BIDIR			I2S0_SYNC
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO
I2S1_TO_DEV	P25MM		I2S1_MCLK
I2S1_BIDIR			I2S1_BITCLK
I2S1_BIDIR			I2S1_SYNC
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO
I2S2_TO_DEV	P25MM		I2S2_MCLK
I2S2_BIDIR			I2S2_BITCLK
I2S2_BIDIR			I2S2_SYNC
SB_CLK18M_XTAL	CLOCKS		SB_CLK18M_XTALI
	CLOCKS		SB_CLK18M_XTALO
	CLOCKS		SB_CLK18M_XTALO_R
SB_CLK25M_ATA	CLOCKS		SB_CLK25M_ATA

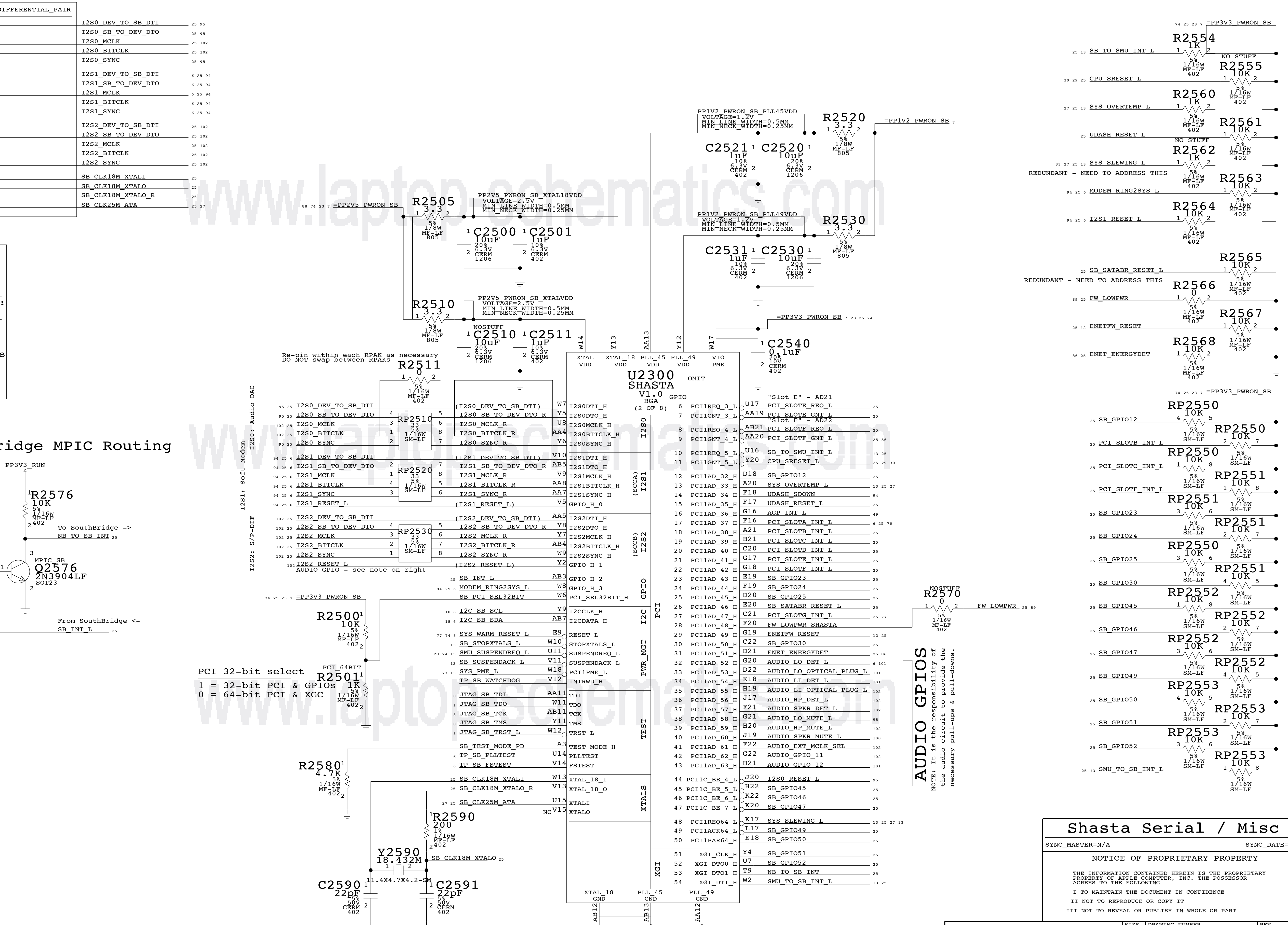
Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing



Shasta Serial / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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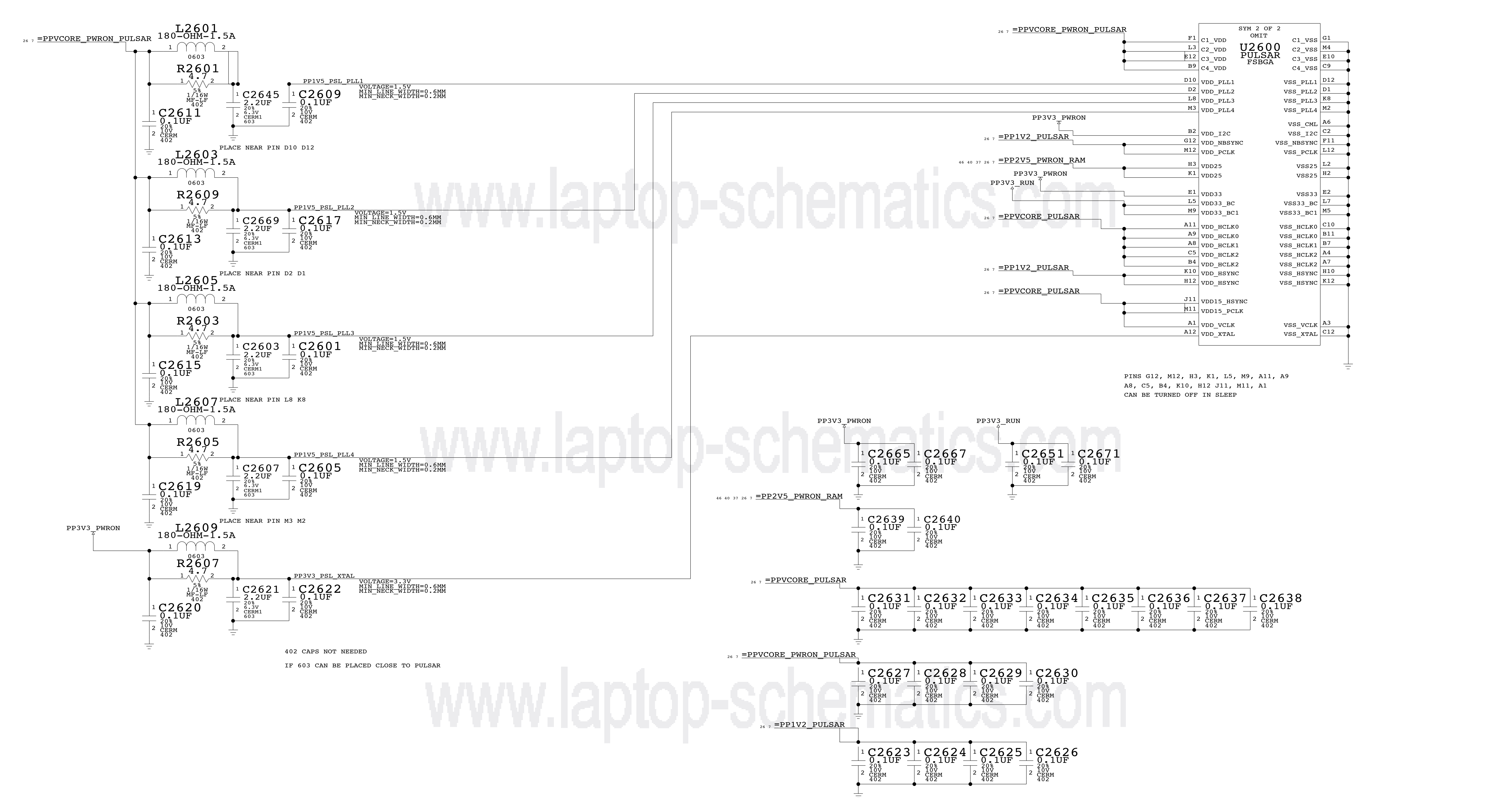
SIZE D DRAWING NUMBER 051-6772 REV. E
SCALE NONE SHT 25 OF 102



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

PULSAR POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE

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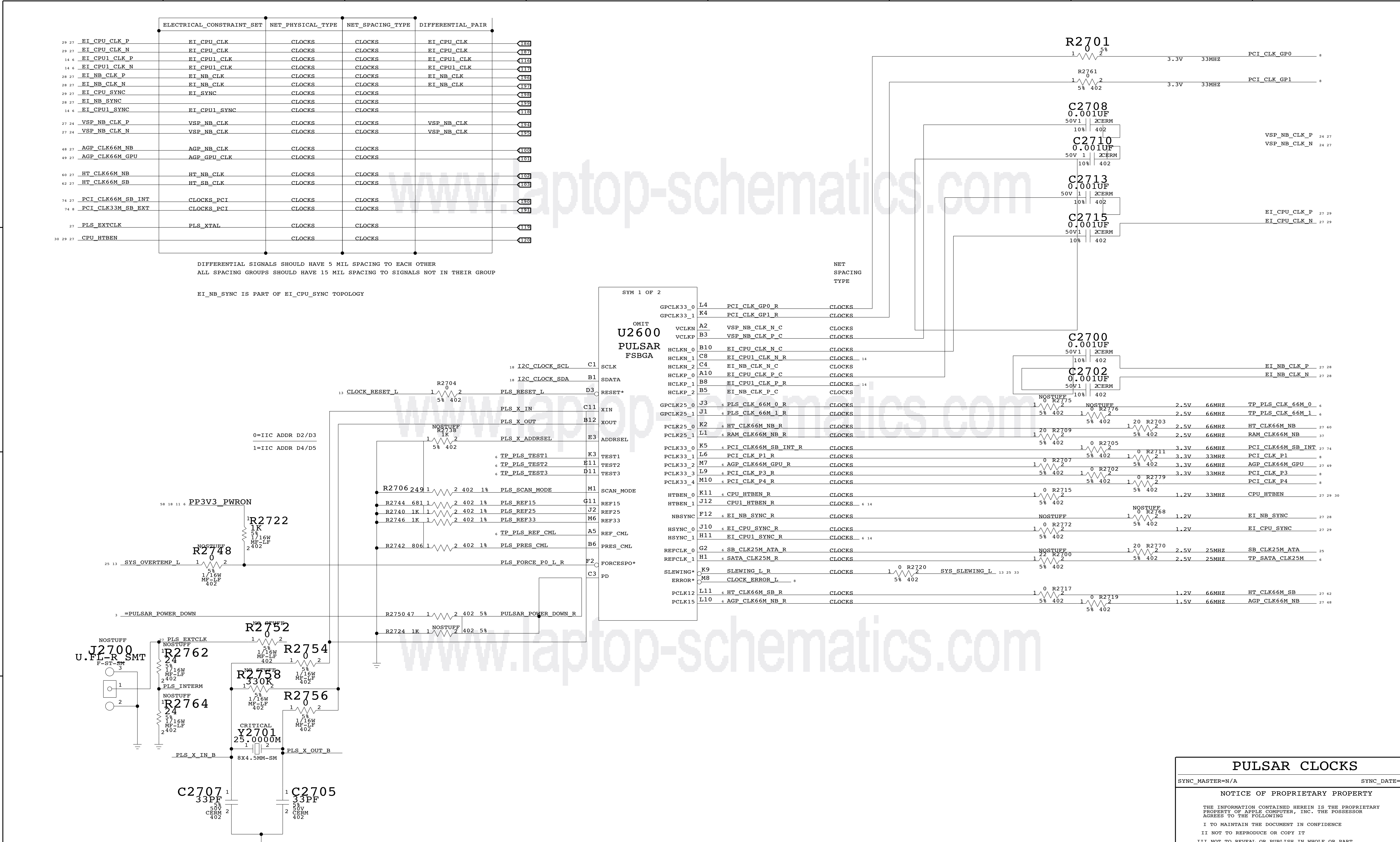

PULSAR CLOCKS

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SIZE	DRAWING NUMBER	REV.
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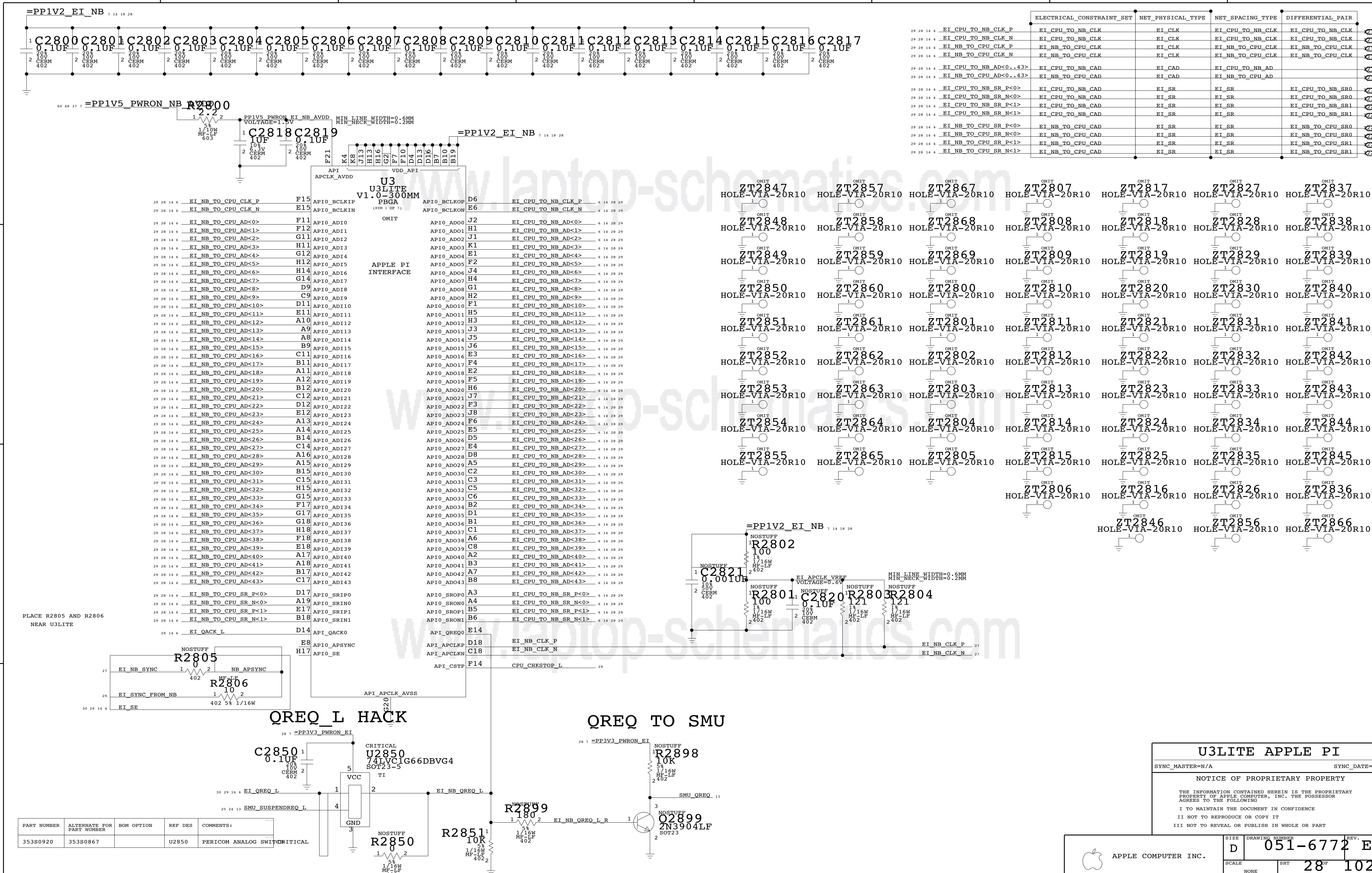
SCALE NONE	SHT 27 OF 102	



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CAD	EI_CPU_TO_NB_AD	
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_CAD	EI_NB_TO_CPU_AD	
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR1
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR1
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U2850	PERICOM ANALOG SWITCH CRITICAL

U3LITE APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

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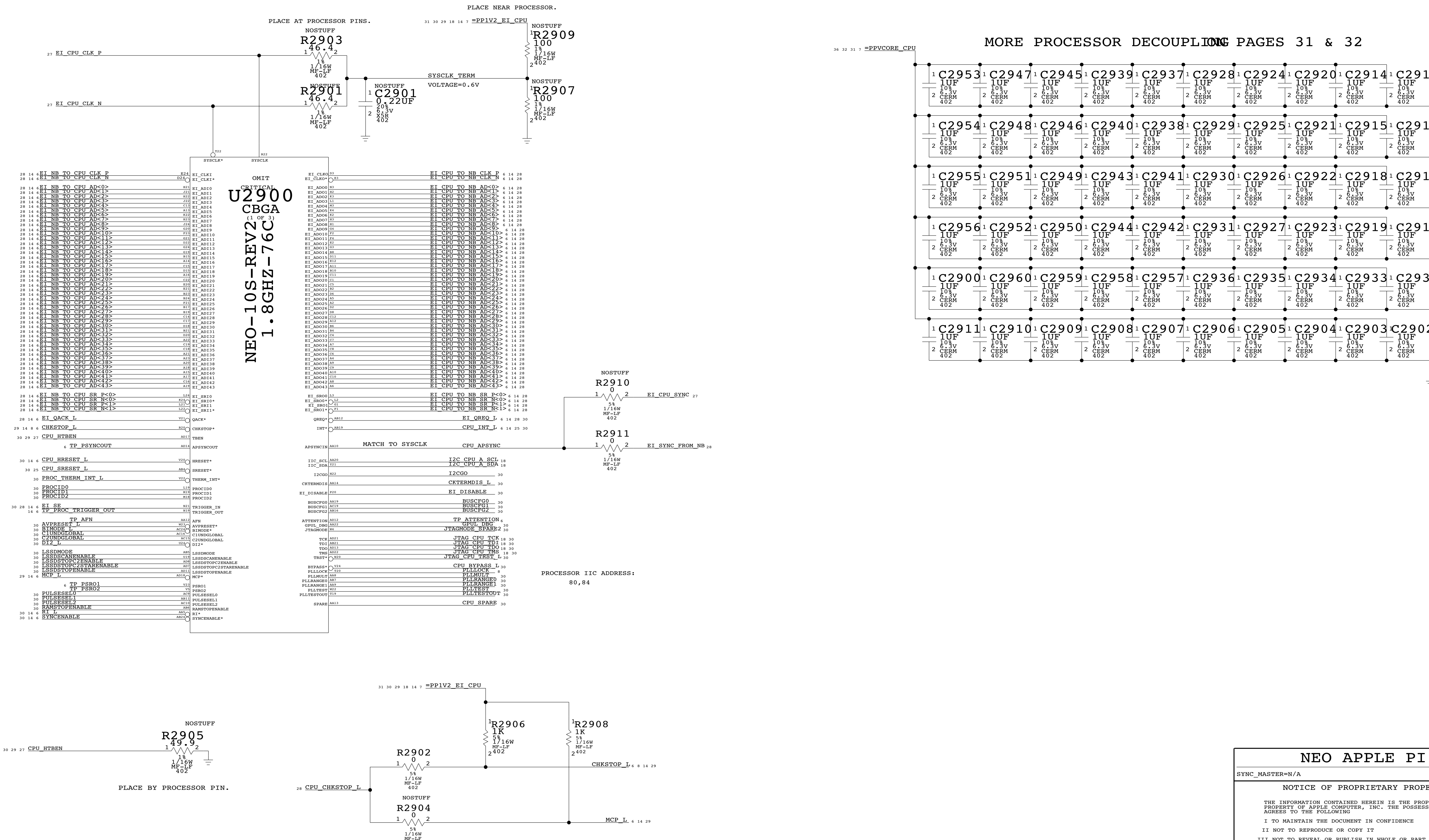

PROCESSOR LOGIC I/O

NEO APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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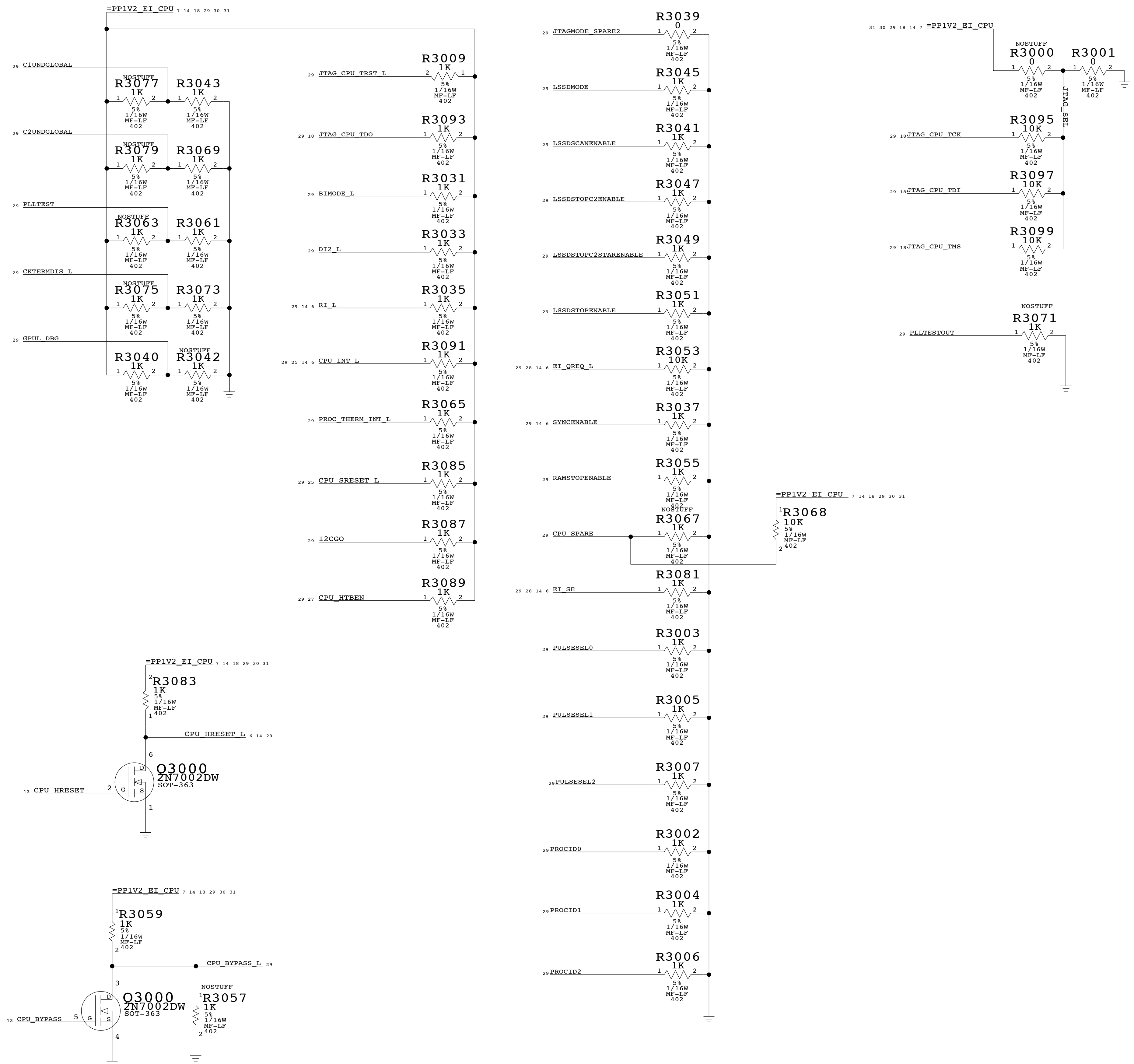


SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

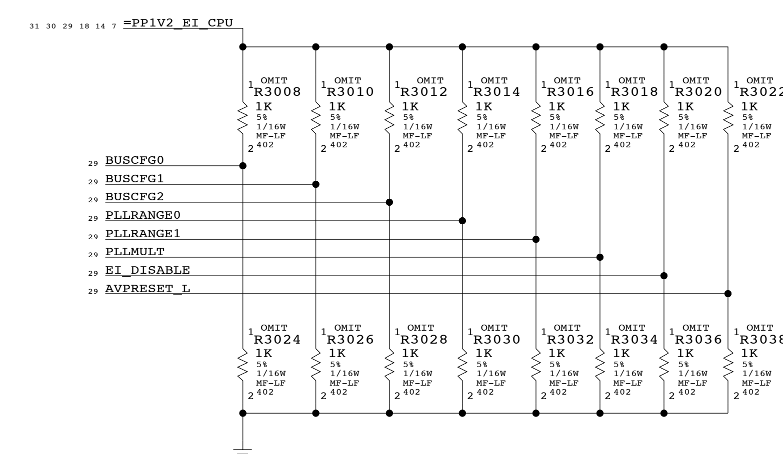
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	
>= 1.8 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	
<= 1.6 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



CPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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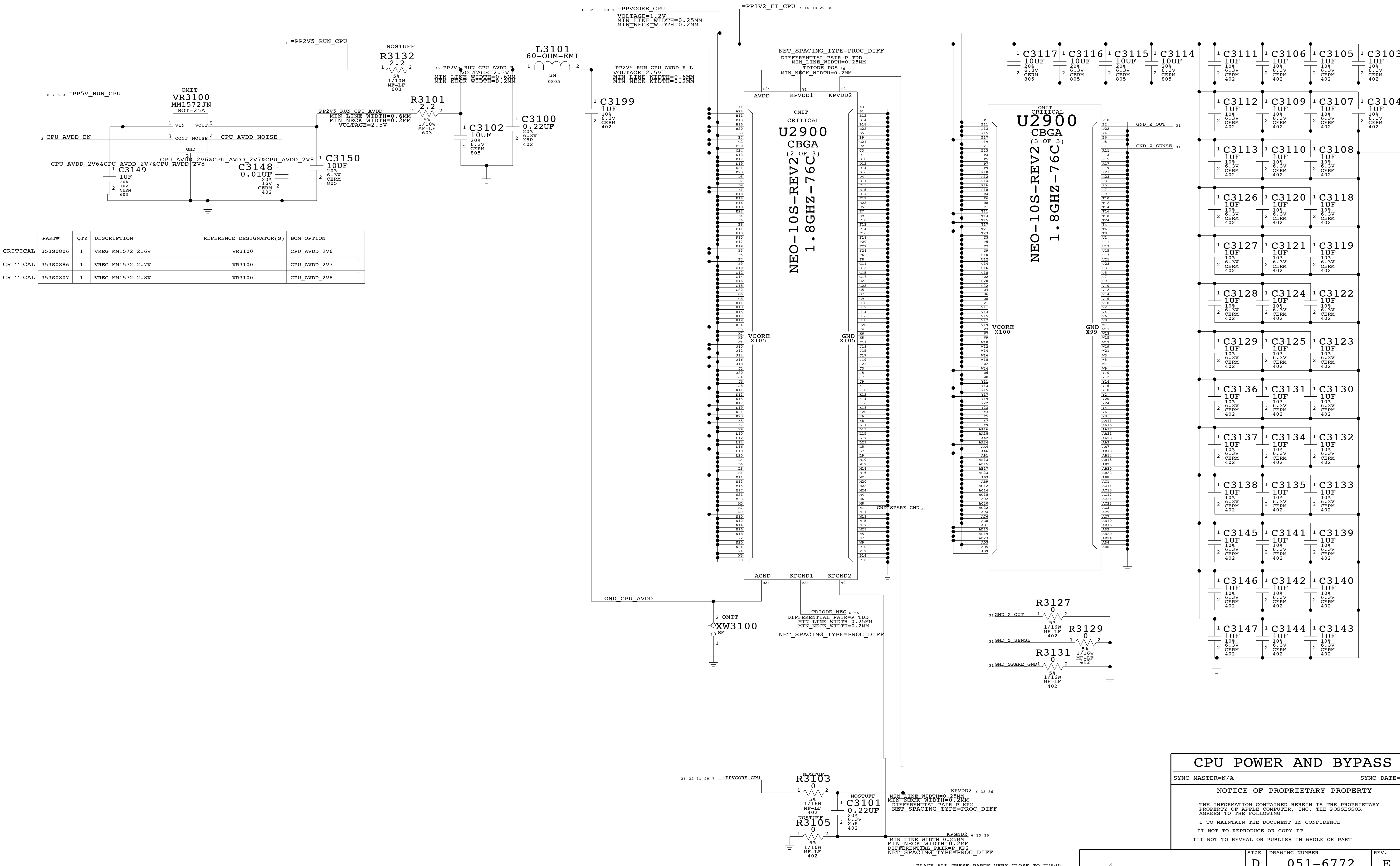
SCALE NONE SHT 30 OF 102



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL	353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

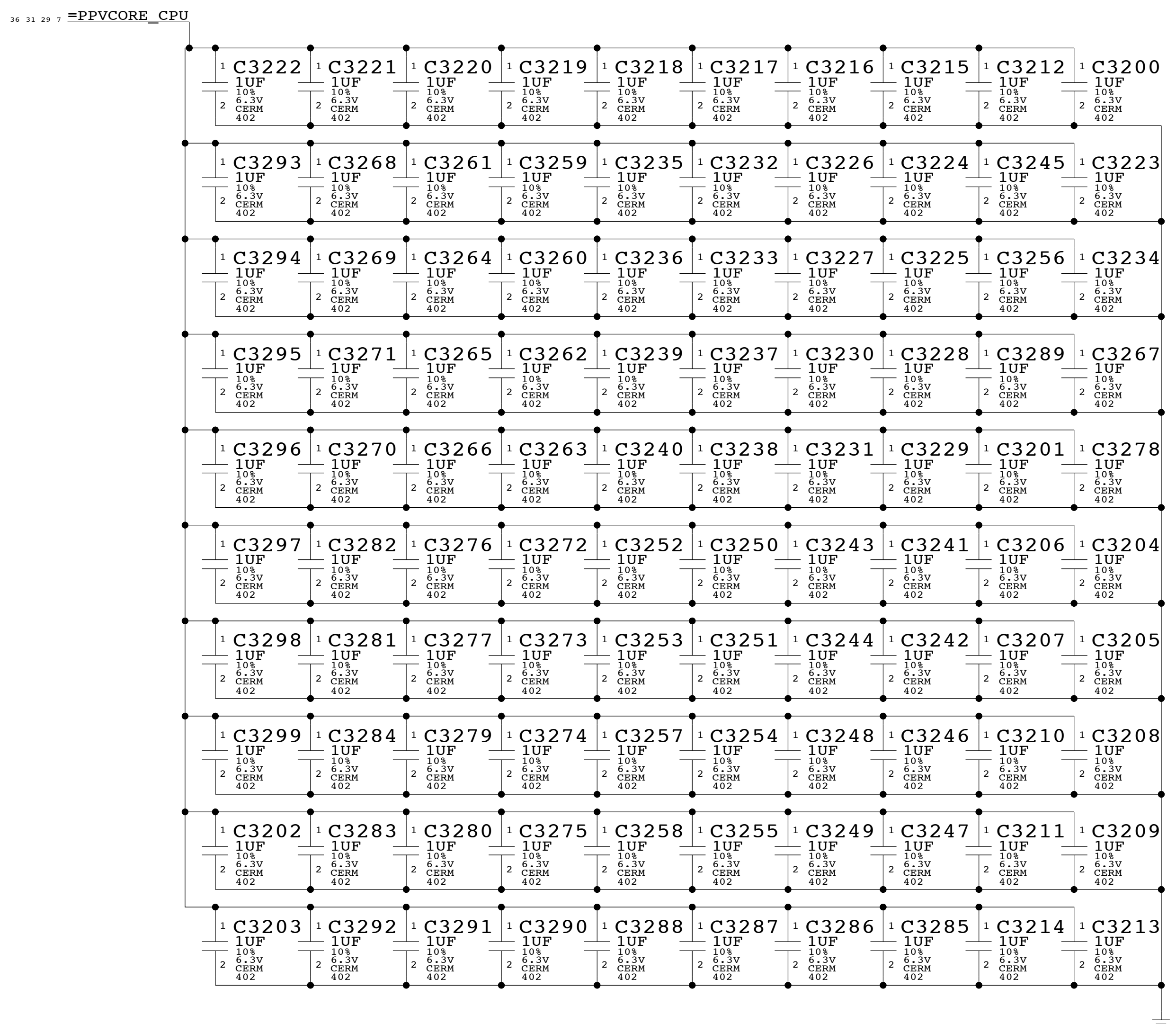
CPU POWER AND BYPASS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	31	102



PROC DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

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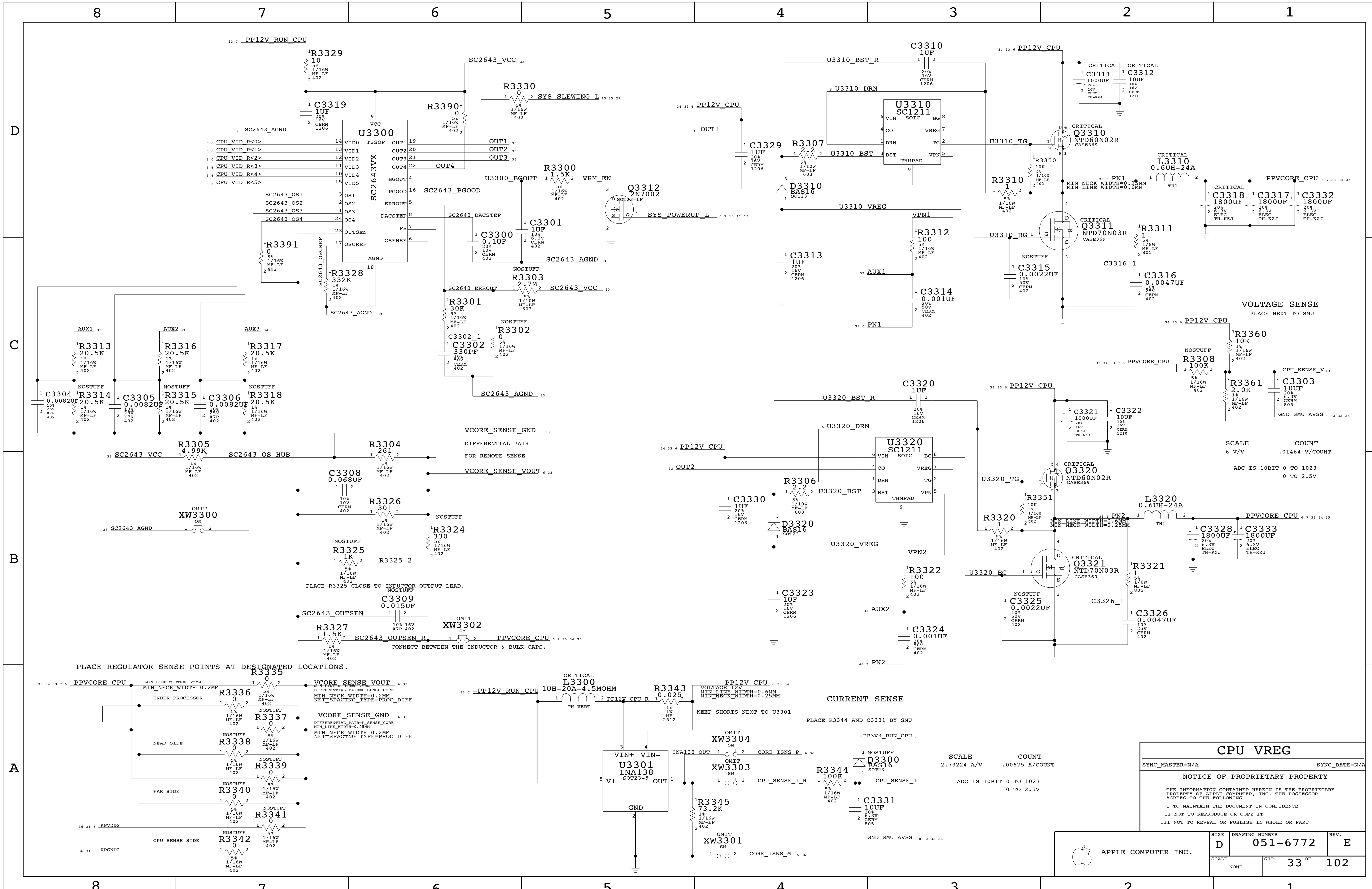
SCALE NONE	SHT 32 OF 102	


CPU VREG
SYNC_MASTER=N/A
SYNC_DATE=N/A
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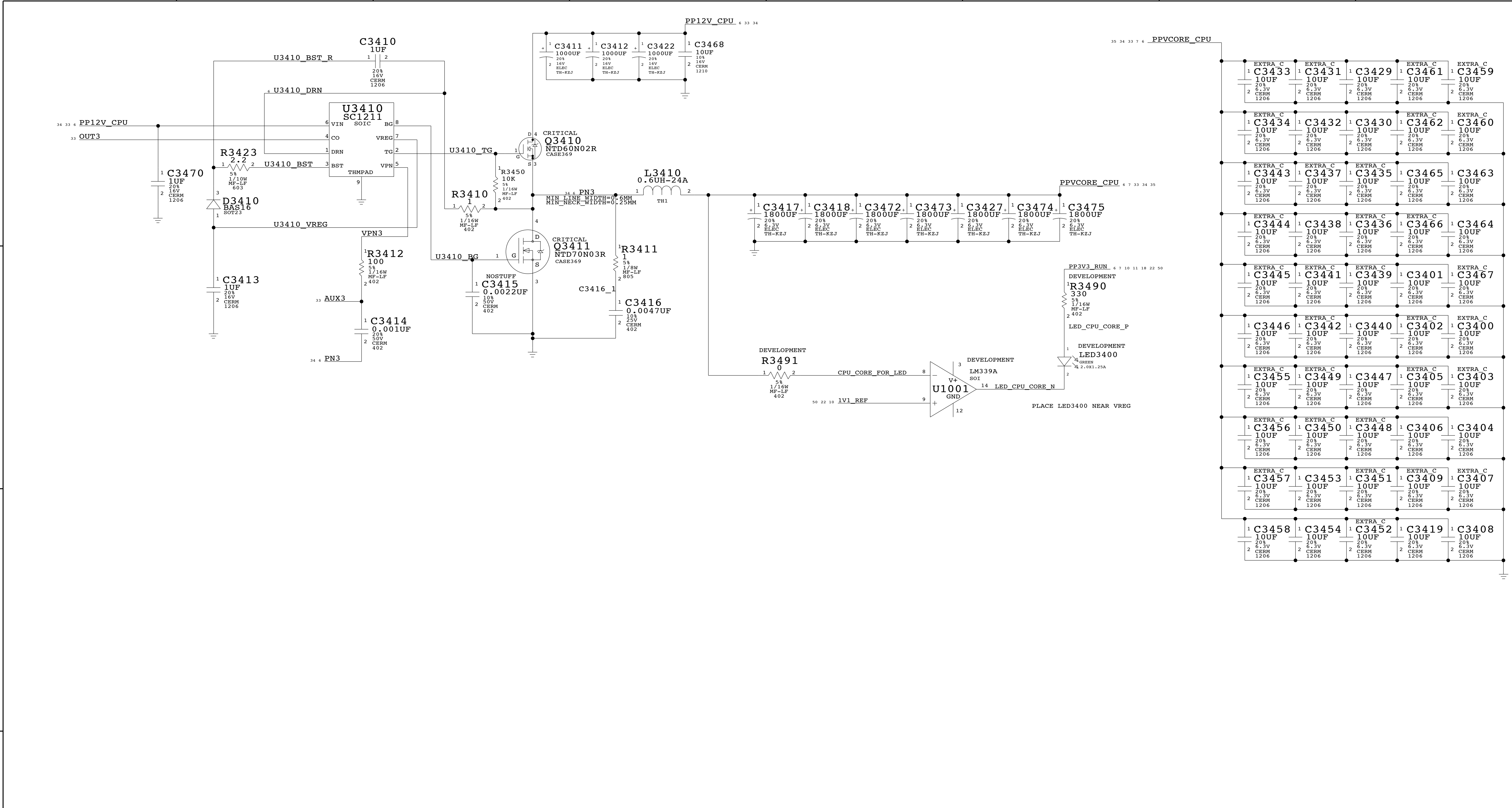
SIZE D
DRAWING NUMBER 051-6772
REV. E
SCALE NONE
SHT 33 OF 102
VOLTAGE SENSE
PLACE NEXT TO SMU
SCALE 6 V/V
COUNT .01464 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
CURRENT SENSE
PLACE R3344 AND C3331 BY SMU
KEEP SHORTS NEXT TO U3301
SCALE 2.73224 A/V
COUNT .00675 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
DIFFERENTIAL PAIR
FOR REMOTE SENSE
PLACE R3325 CLOSE TO INDUCTOR OUTPUT LEAD.
CONNECT BETWEEN THE INDUCTOR & BULK CAPS.
PLACE REGULATOR SENSE POINTS AT DESIGNATED LOCATIONS.
UNDER PROCESSOR
NEAR SIDE
FAR SIDE
CPU SENSE SIDE
U3300 SC2643VX
U3310 SC1211
U3320 SC1211
U3301 INA138



CPU VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

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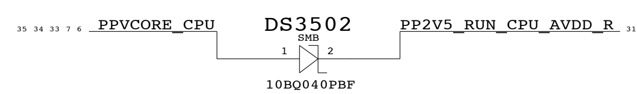
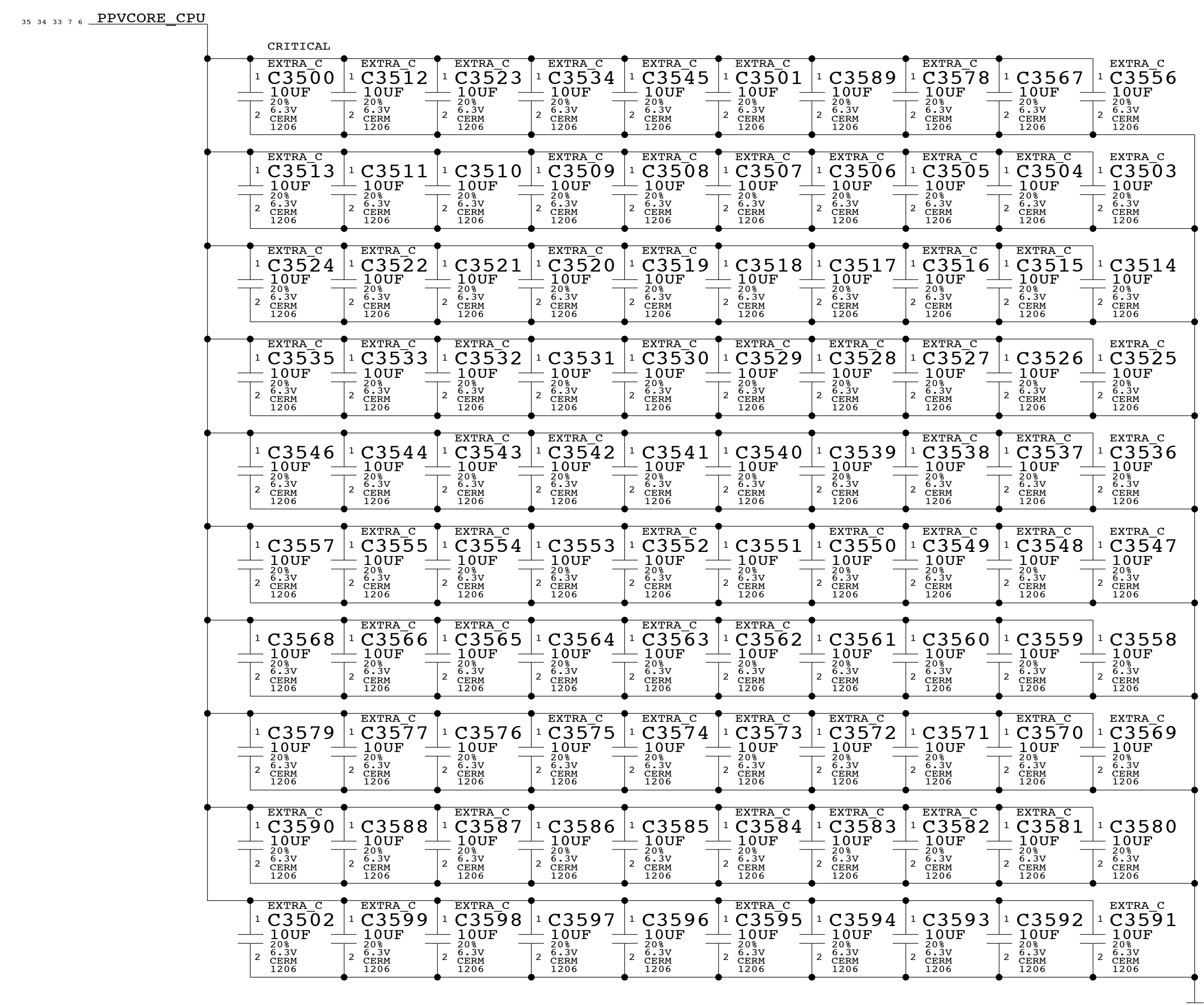
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 34 OF 102	



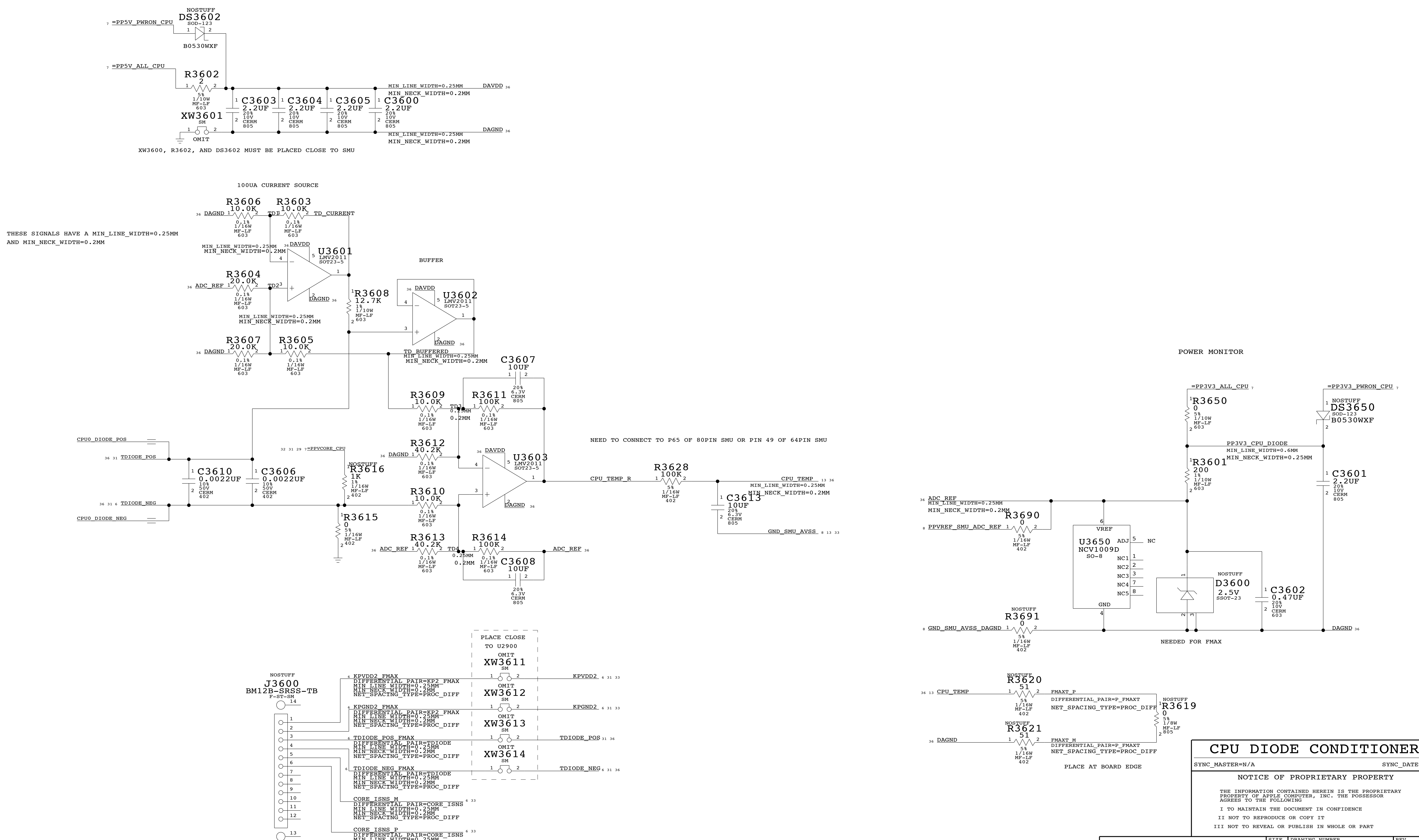


CPU VREG OUTPUT CAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 35 OF 102	



CPU DIODE CONDITIONER

SYNC_MASTER=N/A SYNC_DATE=N/A

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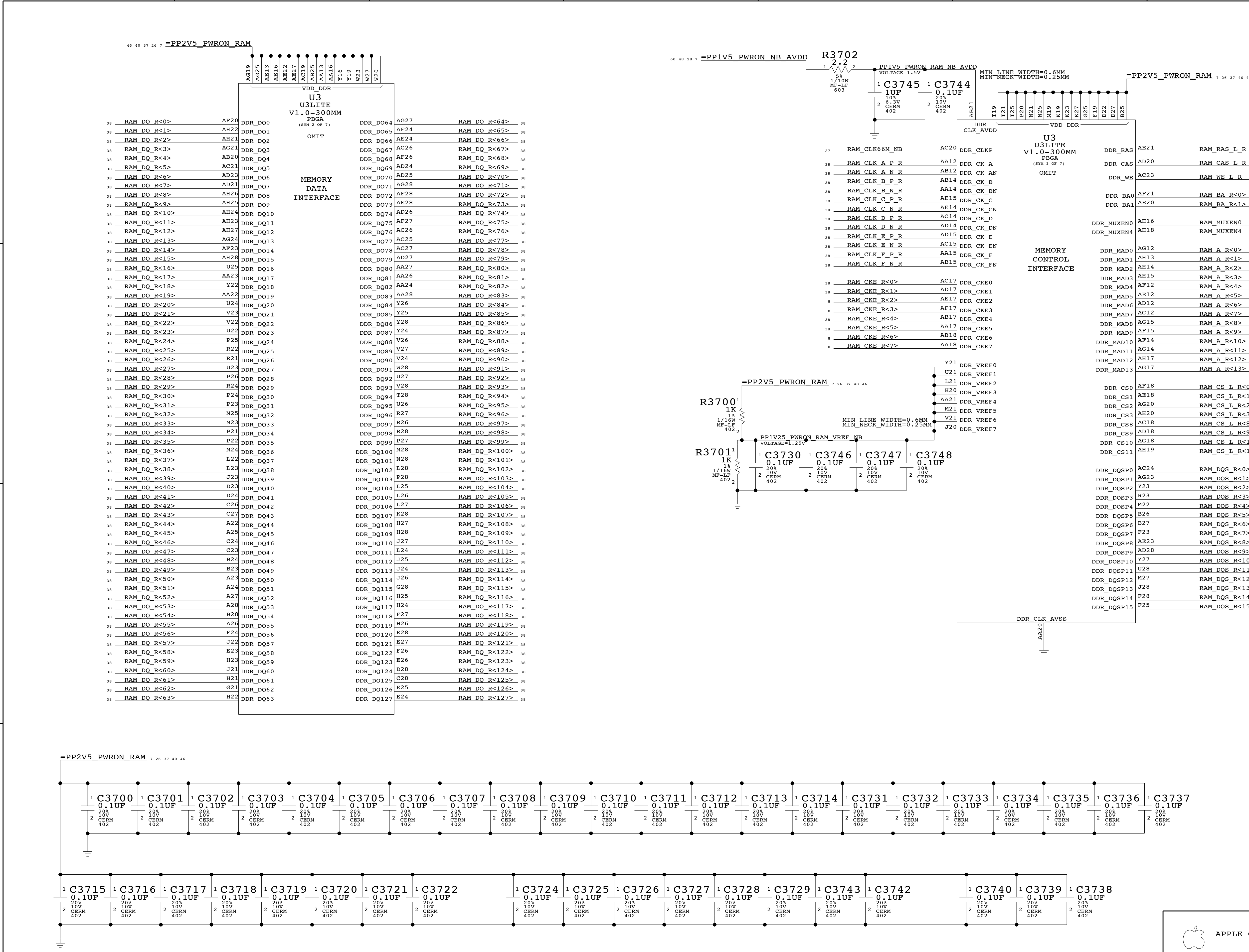
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 36	OF 102



U3LITE MEMORY

SYNC_MASTER=N/A

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 37 OF 102	

ALL R PACKS ARE 1/16W 5%

38 37	RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>	38 40 44
38 37	RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>	38 40 44
38 37	RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>	38 40 44
38 37	RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>	38 40 44
38 37	RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>	38 40 44
38 37	RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>	38 40 44
38 37	RAM_DQ_R<6>	RP3816	4	5	22	RAM_DQ<6>	38 40 44
38 37	RAM_DQ_R<5>	RP3816	3	6	22	RAM_DQ<5>	38 40 44
38 37	RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>	38 40 44
38 37	RAM_DQ_R<10>	RP3801	1	8	22	RAM_DQ<10>	38 40 44
38 37	RAM_DQ_R<11>	RP3801	3	6	22	RAM_DQ<11>	38 40 44
38 37	RAM_DQ_R<14>	RP3801	4	5	22	RAM_DQ<14>	38 40 44
38 37	RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>	38 40 44
38 37	RAM_DQ_R<13>	RP3801	2	7	22	RAM_DQ<13>	38 40 44
38 37	RAM_DQ_R<15>	RP3835	1	8	22	RAM_DQ<15>	38 40 44
38 37	RAM_DQ_R<8>	RP3835	3	6	22	RAM_DQ<8>	38 40 44
38 37	RAM_DQ_R<17>	RP3822	1	8	22	RAM_DQ<17>	38 40 44
38 37	RAM_DQ_R<22>	RP3822	4	5	22	RAM_DQ<22>	38 40 44
38 37	RAM_DQ_R<19>	RP3822	2	7	22	RAM_DQ<19>	38 40 44
38 37	RAM_DQ_R<18>	RP3822	3	6	22	RAM_DQ<18>	38 40 44
38 37	RAM_DQ_R<20>	RP3823	3	6	22	RAM_DQ<20>	38 40 44
38 37	RAM_DQ_R<16>	RP3823	4	5	22	RAM_DQ<16>	38 40 44
38 37	RAM_DQ_R<21>	RP3823	2	7	22	RAM_DQ<21>	38 40 44
38 37	RAM_DQ_R<23>	RP3823	1	8	22	RAM_DQ<23>	38 40 44
38 37	RAM_DQ_R<30>	RP3808	3	6	22	RAM_DQ<30>	38 40 44
38 37	RAM_DQ_R<26>	RP3824	2	7	22	RAM_DQ<26>	38 40 44
38 37	RAM_DQ_R<24>	RP3808	1	8	22	RAM_DQ<24>	38 40 44
38 37	RAM_DQ_R<27>	RP3824	1	8	22	RAM_DQ<27>	38 40 44
38 37	RAM_DQ_R<28>	RP3808	4	5	22	RAM_DQ<28>	38 40 44
38 37	RAM_DQ_R<31>	RP3808	2	7	22	RAM_DQ<31>	38 40 44
38 37	RAM_DQ_R<29>	RP3824	4	5	22	RAM_DQ<29>	38 40 44
38 37	RAM_DQ_R<25>	RP3824	3	6	22	RAM_DQ<25>	38 40 44
38 37	RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>	38 40 44
38 37	RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>	38 40 44
38 37	RAM_DQ_R<38>	RP3826	2	7	22	RAM_DQ<38>	38 40 44
38 37	RAM_DQ_R<37>	RP3807	4	5	22	RAM_DQ<37>	38 40 44
38 37	RAM_DQ_R<39>	RP3826	3	6	22	RAM_DQ<39>	38 40 44
38 37	RAM_DQ_R<33>	RP3807	3	6	22	RAM_DQ<33>	38 40 44
38 37	RAM_DQ_R<34>	RP3807	1	8	22	RAM_DQ<34>	38 40 44
38 37	RAM_DQ_R<36>	RP3826	1	8	22	RAM_DQ<36>	38 40 44
38 37	RAM_DQ_R<47>	RP3811	2	7	22	RAM_DQ<47>	38 40 44
38 37	RAM_DQ_R<46>	RP3811	1	8	22	RAM_DQ<46>	38 40 44
38 37	RAM_DQ_R<43>	RP3814	2	7	22	RAM_DQ<43>	38 40 44
38 37	RAM_DQ_R<41>	RP3814	1	8	22	RAM_DQ<41>	38 40 44
38 37	RAM_DQ_R<45>	RP3811	4	5	22	RAM_DQ<45>	38 40 44
38 37	RAM_DQ_R<42>	RP3814	3	6	22	RAM_DQ<42>	38 40 44
38 37	RAM_DQ_R<40>	RP3814	4	5	22	RAM_DQ<40>	38 40 44
38 37	RAM_DQ_R<44>	RP3811	3	6	22	RAM_DQ<44>	38 40 44
38 37	RAM_DQ_R<51>	RP3830	4	5	22	RAM_DQ<51>	38 40 44
38 37	RAM_DQ_R<50>	RP3830	2	7	22	RAM_DQ<50>	38 40 44
38 37	RAM_DQ_R<49>	RP3830	1	8	22	RAM_DQ<49>	38 40 44
38 37	RAM_DQ_R<48>	RP3830	3	6	22	RAM_DQ<48>	38 40 44
38 37	RAM_DQ_R<52>	RP3812	2	7	22	RAM_DQ<52>	38 40 44
38 37	RAM_DQ_R<53>	RP3812	3	6	22	RAM_DQ<53>	38 40 44
38 37	RAM_DQ_R<54>	RP3812	4	5	22	RAM_DQ<54>	38 40 44
38 37	RAM_DQ_R<55>	RP3812	1	8	22	RAM_DQ<55>	38 40 44
38 37	RAM_DQ_R<56>	RP3813	1	8	22	RAM_DQ<56>	38 40 44
38 37	RAM_DQ_R<63>	RP3831	4	5	22	RAM_DQ<63>	38 40 44
38 37	RAM_DQ_R<59>	RP3813	2	7	22	RAM_DQ<59>	38 40 44
38 37	RAM_DQ_R<61>	RP3831	2	7	22	RAM_DQ<61>	38 40 44
38 37	RAM_DQ_R<57>	RP3831	3	6	22	RAM_DQ<57>	38 40 44
38 37	RAM_DQ_R<60>	RP3831	1	8	22	RAM_DQ<60>	38 40 44
38 37	RAM_DQ_R<58>	RP3813	3	6	22	RAM_DQ<58>	38 40 44
38 37	RAM_DQ_R<62>	RP3813	4	5	22	RAM_DQ<62>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40 45
38 37	RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>	38 40 45
38 37	RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40 44
38 37	RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40 44
38 37	RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40 45
38 37	RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40 45
38 37	RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40 44
38 37	RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40 44
38 37	RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40 44
38 37	RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>	38 40 44
38 37	RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40 45
38 37	RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>	38 40 44
38 37	RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>	38 40 44
38 37	RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40 44
		RP3834	1	8	15		
38 37	RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40 44
38 37	RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>	38 40 44
38 37	RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>	38 40 44
38 37	RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>	38 40 44
38 37	RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>	38 40 44
38 37	RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>	38 40 44
38 37	RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L	38 40 45
38 37	RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>	38 40 45
38 37	RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>	38 40 45
38 37	RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L	38 40 45
38 37	RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>	38 40 45
38 37	RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>	38 40 44

38 37	RAM_DQ_R<68>	RP3818	2	7	22	RAM_DQ<68>	38 40 45
38 37	RAM_DQ_R<65>	RP3805	2	7	22	RAM_DQ<65>	38 40 45
38 37	RAM_DQ_R<70>	RP3818	4	5	22	RAM_DQ<70>	38 40 45
38 37	RAM_DQ_R<66>	RP3805	1	8	22	RAM_DQ<66>	38 40 45
38 37	RAM_DQ_R<71>	RP3818	3	6	22	RAM_DQ<71>	38 40 45
38 37	RAM_DQ_R<64>	RP3805	4	5	22	RAM_DQ<64>	38 40 45
38 37	RAM_DQ_R<67>	RP3805	3	6	22	RAM_DQ<67>	38 40 45
38 37	RAM_DQ_R<69>	RP3818	1	8	22	RAM_DQ<69>	38 40 45
38 37	RAM_DQ_R<74>	RP3817	3	6	22	RAM_DQ<74>	38 40 45
38 37	RAM_DQ_R<73>	RP3802	4	5	22	RAM_DQ<73>	38 40 45
38 37	RAM_DQ_R<72>	RP3817	2	7	22	RAM_DQ<72>	38 40 45
38 37	RAM_DQ_R<75>	RP3817	4	5	22	RAM_DQ<75>	38 40 45
38 37	RAM_DQ_R<78>	RP3802	2	7	22	RAM_DQ<78>	38 40 45
38 37	RAM_DQ_R<79>	RP3817	1	8	22	RAM_DQ<79>	38 40 45
38 37	RAM_DQ_R<77>	RP3802	1	8	22	RAM_DQ<77>	38 40 45
38 37	RAM_DQ_R<76>	RP3802	3	6	22	RAM_DQ<76>	38 40 45
38 37	RAM_DQ_R<87>	RP3806	2	7	22	RAM_DQ<87>	38 40 45
38 37	RAM_DQ_R<86>	RP3821	1	8	22	RAM_DQ<86>	38 40 45
38 37	RAM_DQ_R<81>	RP3821	4	5	22	RAM_DQ<81>	38 40 45
38 37	RAM_DQ_R<80>	RP3821	2	7	22	RAM_DQ<80>	38 40 45
38 37	RAM_DQ_R<84>	RP3806	1	8	22	RAM_DQ<84>	38 40 45
38 37	RAM_DQ_R<85>	RP3806	3	6	22	RAM_DQ<85>	38 40 45
38 37	RAM_DQ_R<83>	RP3821	3	6	22	RAM_DQ<83>	38 40 45
38 37	RAM_DQ_R<82>	RP3806	4	5	22	RAM_DQ<82>	38 40 45
38 37	RAM_DQ_R<91>	RP3819	3	6	22	RAM_DQ<91>	38 40 45
38 37	RAM_DQ_R<93>	RP3819	1	8	22	RAM_DQ<93>	38 40 45
38 37	RAM_DQ_R<94>	RP3803	2	7	22	RAM_DQ<94>	38 40 45
38 37	RAM_DQ_R<90>	RP3819	4	5	22	RAM_DQ<90>	38 40 45
38 37	RAM_DQ_R<88>	RP3803	4	5	22	RAM_DQ<88>	38 40 45
38 37	RAM_DQ_R<89>	RP3819	2	7	22	RAM_DQ<89>	38 40 45
38 37	RAM_DQ_R<92>	RP3803	3	6	22	RAM_DQ<92>	38 40 45
38 37	RAM_DQ_R<95>	RP3803	1	8	22	RAM_DQ<95>	38 40 45
38 37	RAM_DQ_R<98>	RP3820	4	5	22	RAM_DQ<98>	38 40 45
38 37	RAM_DQ_R<96>	RP3820	3	6	22	RAM_DQ<96>	38 40 45
38 37	RAM_DQ_R<103>	RP3820	2	7	22	RAM_DQ<103>	38 40 45
38 37	RAM_DQ_R<97>	RP3820	1	8	22	RAM_DQ<97>	38 40 45
38 37	RAM_DQ_R<100>	RP3825	2	7	22	RAM_DQ<100>	38 40 45
38 37	RAM_DQ_R<99>	RP3825	3	6	22	RAM_DQ<99>	38 40 45
38 37	RAM_DQ_R<102>	RP3825	1	8	22	RAM_DQ<102>	38 40 45
38 37	RAM_DQ_R<101>	RP3825	4	5	22	RAM_DQ<101>	38 40 45
38 37	RAM_DQ_R<111>	RP3809	1	8	22	RAM_DQ<111>	38 40 45
38 37	RAM_DQ_R<106>	RP3809	3	6	22	RAM_DQ<106>	38 40 45
38 37	RAM_DQ_R<105>	RP3809	2	7	22	RAM_DQ<105>	38 40 45
38 37	RAM_DQ_R<108>	RP3829	2	7	22	RAM_DQ<108>	38 40 45
38 37	RAM_DQ_R<107>	RP3829	4	5	22	RAM_DQ<107>	38 40 45
38 37	RAM_DQ_R<110>	RP3829	3	6	22	RAM_DQ<110>	38 40 45
38 37	RAM_DQ_R<104>	RP3809	4	5	22	RAM_DQ<104>	38 40 45
38 37	RAM_DQ_R<109>	RP3829	1	8	22	RAM_DQ<109>	38 40 45
38 37	RAM_DQ_R<119>	RP3828	4	5	22	RAM_DQ<119>	38 40 45
38 37	RAM_DQ_R<112>	RP3815	2	7	22	RAM_DQ<112>	38 40 45
38 37	RAM_DQ_R<117>	RP3815	1	8	22	RAM_DQ<117>	38 40 45
38 37	RAM_DQ_R<118>	RP3828	1	8	22	RAM_DQ<118>	38 40 45
38 37	RAM_DQ_R<113>	RP3815	3	6	22	RAM_DQ<113>	38 40 45
38 37	RAM_DQ_R<115>	RP3828	3	6	22	RAM_DQ<115>	38 40 45
38 37	RAM_DQ_R<116>	RP3828	2	7	22	RAM_DQ<116>	38 40 45
38 37	RAM_DQ_R<114>	RP3815	4	5	22	RAM_DQ<114>	38 40 45
38 37	RAM_DQ_R<121>	RP3827	3	6	22	RAM_DQ<121>	38 40 45
38 37	RAM_DQ_R<124>	RP3827	2	7	22	RAM_DQ<124>	38 40 45
38 37	RAM_DQ_R<120>	RP3827	4	5	22	RAM_DQ<120>	38 40 45
38 37	RAM_DQ_R<123>	RP3810	2	7	22	RAM_DQ<123>	38 40 45
38 37	RAM_DQ_R<125>	RP3827	1	8	22	RAM_DQ<125>	38 40 45
38 37	RAM_DQ_R<122>	RP3810	4	5	22	RAM_DQ<122>	38 40 45
38 37	RAM_DQ_R<126>	RP3810	1	8	22	RAM_DQ<126>	38 40 45
38 37	RAM_DQ_R<127>	RP3810	3	6	22	RAM_DQ<127>	38 40 45

THE FOLLOWING ARE 0402 5% RESISTORS

38 37	RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40
38 37	RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N	38 40
38 37	RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40
38 37	RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40
38 37	RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40
38 37	RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40
38 37	RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40
38 37	RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40
38 37	RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40
38 37	RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40
38 37	RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P	38 40
38 37	RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40

38 37	RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>	38 40 44
38 37	RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>	38 40 44
38 37	RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40 44
38 37	RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40 44
38 37	RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>	38 40 44
38 37	RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>	38 40 44
38 37	RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>	38 40 44
38 37	RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>	38 40 44
38 37	RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>	38 40 45
38 37	RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>	38 40 45
38 37	RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>	38 40 45
38 37	RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>	38 40 45
38 37	RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>	38 40 45
38 37	RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>	38 40 45
38 37	RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>	38 40 45
38 37	RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>	38 40 45

		ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
38 37	RAM_CLK_A_P_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	I206
38 37	RAM_CLK_A_N_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	I207
38 37	RAM_CLK_B_P_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	I208
38 37	RAM_CLK_B_N_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	I209
38 37	RAM_CLK_C_P_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	I210
38 37	RAM_CLK_C_N_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	I211
38 37	RAM_CLK_D_P_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	I212
38 37	RAM_CLK_D_N_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	I213
38 37	RAM_CLK_E_P_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	I214
38 37	RAM_CLK_E_N_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	I215
38 37	RAM_CLK_F_P_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	I216
38 37	RAM_CLK_F_N_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	I217
40 38	RAM_CLK_A_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	I218
40 38	RAM_CLK_A_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	I219
40 38	RAM_CLK_B_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	I220
40 38	RAM_CLK_B_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	I221
40 38	RAM_CLK_C_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	I222
40 38	RAM_CLK_C_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	I223
40 38	RAM_CLK_D_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	I224
40 38	RAM_CLK_D_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	I225
40 38	RAM_CLK_E_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	I226
40 38	RAM_CLK_E_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	I227
40 38	RAM_CLK_F_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	I228
40 38	RAM_CLK_F_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	I229
38 37	RAM_CKE_R<1..0>		RAM_CAD	RAM_CAD		I230
38 37	RAM_CKE_R<5..4>		RAM_CAD	RAM_CAD		I232
44 40 38	RAM_CKE<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		I234
44 40 38	RAM_CKE<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		I236
45 40 38	RAM_CKE<4>	RAM_CKECS1	RAM_CAD	RAM_CAD		I235
45 40 38	RAM_CKE<5>	RAM_CKECS1	RAM_CAD	RAM_CAD		I237
38 37	RAM_CS_L_R<1..0>		RAM_CAD	RAM_CAD		I238
38 37	RAM_CS_L_R<9..8>		RAM_CAD	RAM_CAD		I241
44 40 38	RAM_CS_L<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		I243
44 40 38	RAM_CS_L<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		I242
45 40 38	RAM_CS_L<8>	RAM_CKECS1	RAM_CAD	RAM_CAD		I245
45 40 38	RAM_CS_L<9>	RAM_CKECS1	RAM_CAD	RAM_CAD		I244
38 37	RAM_DQS_R<15..0>		RAM_CAD	RAM_CAD		I305
38 37	RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		I294
45 44 40 38	RAM_DQ<127..0>		RAM_CAD	RAM_CAD		I293
44 40 38	RAM_DQS<0>	RAM_DQS0	RAM_CAD	RAM_CAD		I246
44 40 38	RAM_DQ<7..0>	RAM_DQS0	RAM_CAD	RAM_CAD		I248
44 40 38	RAM_DQS<1>	RAM_DQS1	RAM_CAD	RAM_CAD		I251
44 40 38	RAM_DQ<15..8>	RAM_DQS1	RAM_CAD	RAM_CAD		I252
44 40 38	RAM_DQS<2>	RAM_DQS2	RAM_CAD	RAM_CAD		I253
44 40 38	RAM_DQ<23..16>	RAM_DQS2	RAM_CAD	RAM_CAD		I254
44 40 38	RAM_DQS<3>	RAM_DQS3	RAM_CAD	RAM_CAD		I255
44 40 38	RAM_DQ<31..24>	RAM_DQS3	RAM_CAD	RAM_CAD		I256
44 40 38	RAM_DQS<4>	RAM_DQS4	RAM_CAD	RAM_CAD		I257
44 40 38	RAM_DQ<39..32>	RAM_DQS4	RAM_CAD	RAM_CAD		I258
44 40 38	RAM_DQS<5>	RAM_DQS5	RAM_CAD	RAM_CAD		I259
44 40 38	RAM_DQ<47..40>	RAM_DQS5	RAM_CAD	RAM_CAD		I260
44 40 38	RAM_DQS<6>	RAM_DQS6	RAM_CAD	RAM_CAD		I261
44 40 38	RAM_DQ<55..48>	RAM_DQS6	RAM_CAD	RAM_CAD		I262
44 40 38	RAM_DQS<7>	RAM_DQS7	RAM_CAD	RAM_CAD		I263
44 40 38	RAM_DQ<63..56>	RAM_DQS7	RAM_CAD	RAM_CAD		I264
45 40 38	RAM_DQS<8>	RAM_DQS8	RAM_CAD	RAM_CAD		I265
45 40 38	RAM_DQ<71..64>	RAM_DQS8	RAM_CAD	RAM_CAD		I267
45 40 38	RAM_DQS<9>	RAM_DQS9	RAM_CAD	RAM_CAD		I266
45 40 38	RAM_DQ<79..72>	RAM_DQS9	RAM_CAD	RAM_CAD		I268
45 40 38	RAM_DQS<10>	RAM_DQS10	RAM_CAD	RAM_CAD		I270
45 40 38	RAM_DQ<87..80>	RAM_DQS10	RAM_CAD	RAM_CAD		I269
45 40 38	RAM_DQS<11>	RAM_DQS11	RAM_CAD	RAM_CAD		I272
45 40 38	RAM_DQ<95..88>	RAM_DQS11	RAM_CAD	RAM_CAD		I271
45 40 38	RAM_DQS<12>	RAM_DQS12	RAM_CAD	RAM_CAD		I273
45 40 38	RAM_DQ<103..96>	RAM_DQS12	RAM_CAD	RAM_CAD		I275
45 40 38	RAM_DQS<13>	RAM_DQS13	RAM_CAD	RAM_CAD		I274
45 40 38	RAM_DQ<111..104>	RAM_DQS13	RAM_CAD	RAM_CAD		I277
45 40 38	RAM_DQS<14>	RAM_DQS14	RAM_CAD	RAM_CAD		I276
45 40 38	RAM_DQ<119..112>	RAM_DQS14	RAM_CAD	RAM_CAD		I278
45 40 38	RAM_DQS<15>	RAM_DQS15	RAM_CAD	RAM_CAD		I280
45 40 38	RAM_DQ<127..120>	RAM_DQS15	RAM_CAD	RAM_CAD		I279
38 37	RAM_A_R<13..0>		RAM_CAD	RAM_CAD		I295
38 37	RAM_BA_R<1..0>		RAM_CAD	RAM_CAD		I296
38 37	RAM_RAS_L_R		RAM_CAD	RAM_CAD		I297
38 37	RAM_CAS_L_R		RAM_CAD	RAM_CAD		I298
38 37	RAM_WE_L_R		RAM_CAD	RAM_CAD		I299
45 44 40 38	RAM_A<13..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		I300
45 40 38	RAM_BA<1..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		I304
45 40 38	RAM_RAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		I303
45 40 38	RAM_CAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		I302
45 40 38	RAM_WE_L	RAM_A_CTL	RAM_CAD	RAM_CAD		I301

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

SERIES TERM

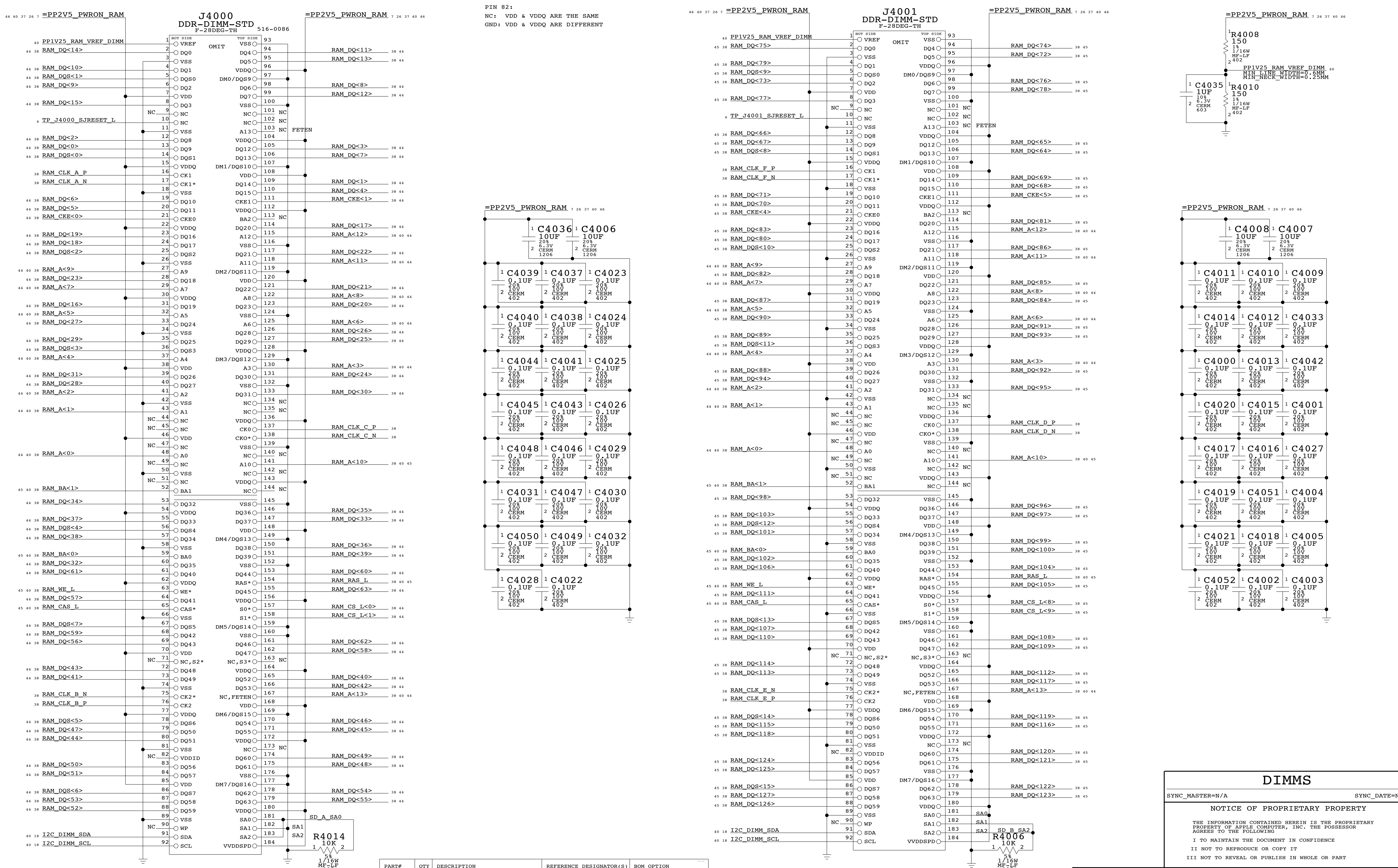
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 38 OF 102

PIN 82:
NC: VDD & VDDQ ARE THE SAME
GND: VDD & VDDQ ARE DIFFERENT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD	CRITICAL
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD	CRITICAL

R'S ADJACENT TO V'S OR G'S
V'S ADJACENT TO G'S FORBIDDEN

DIMMS

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

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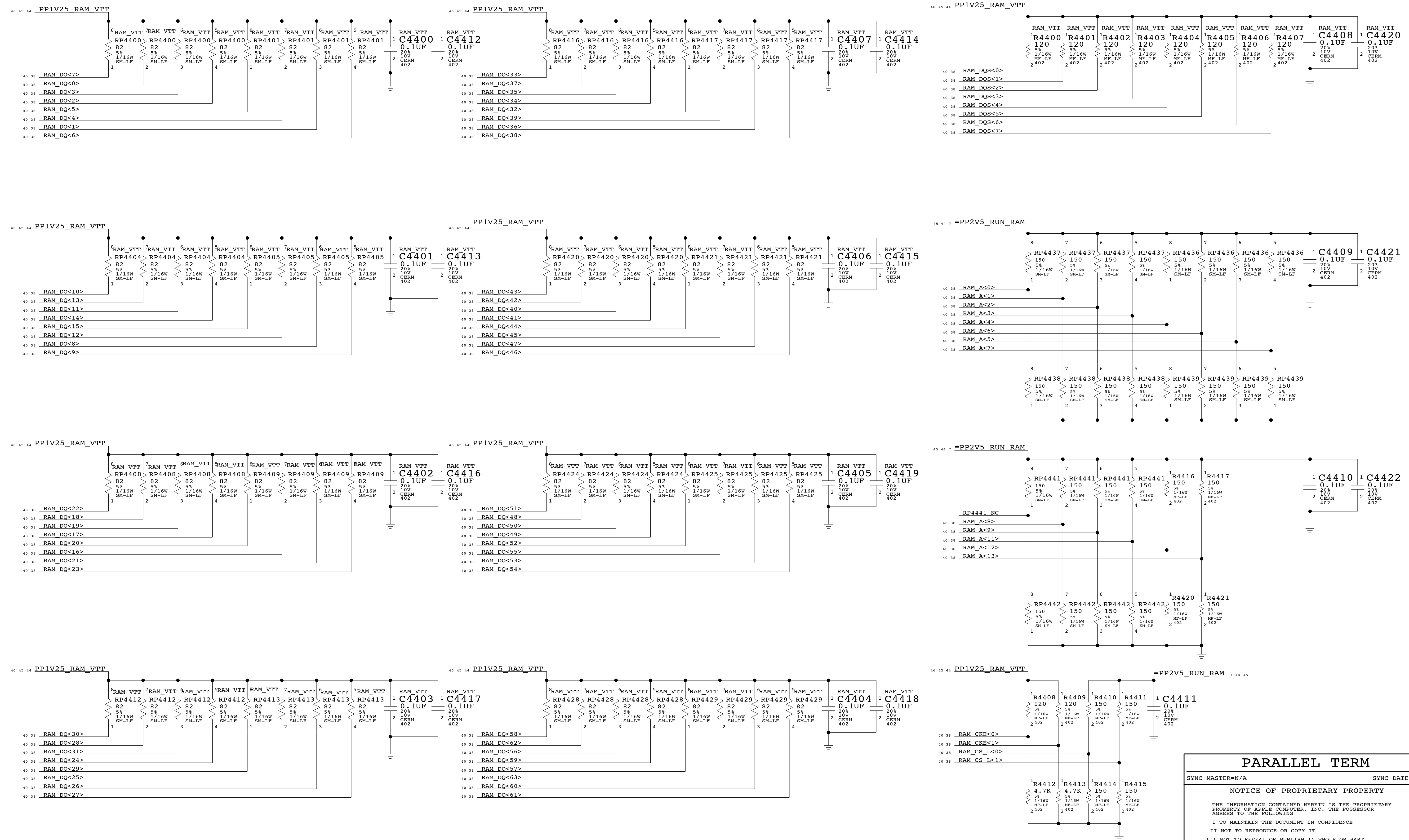

PARALLEL TERM

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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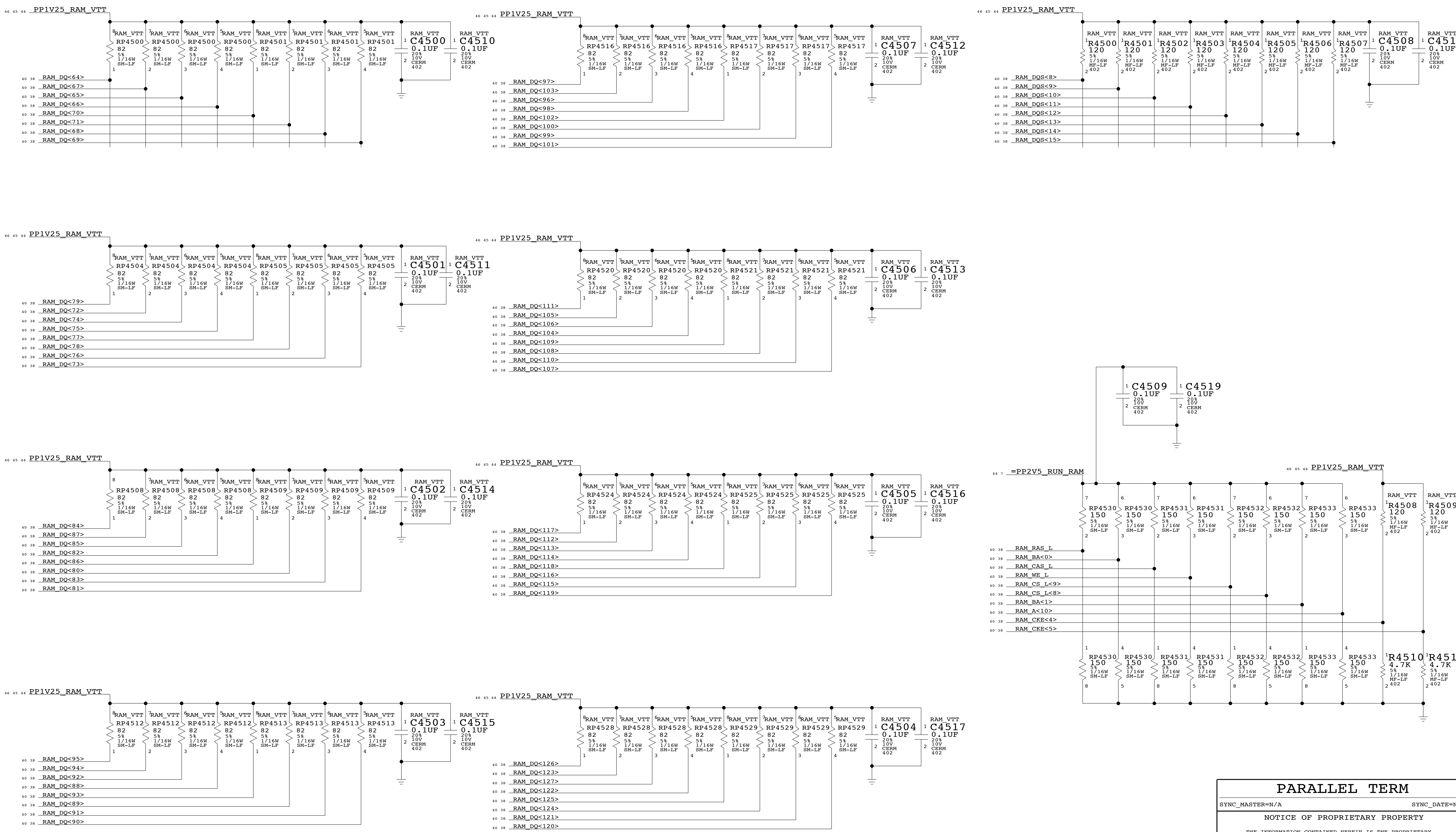

PARALLEL TERM

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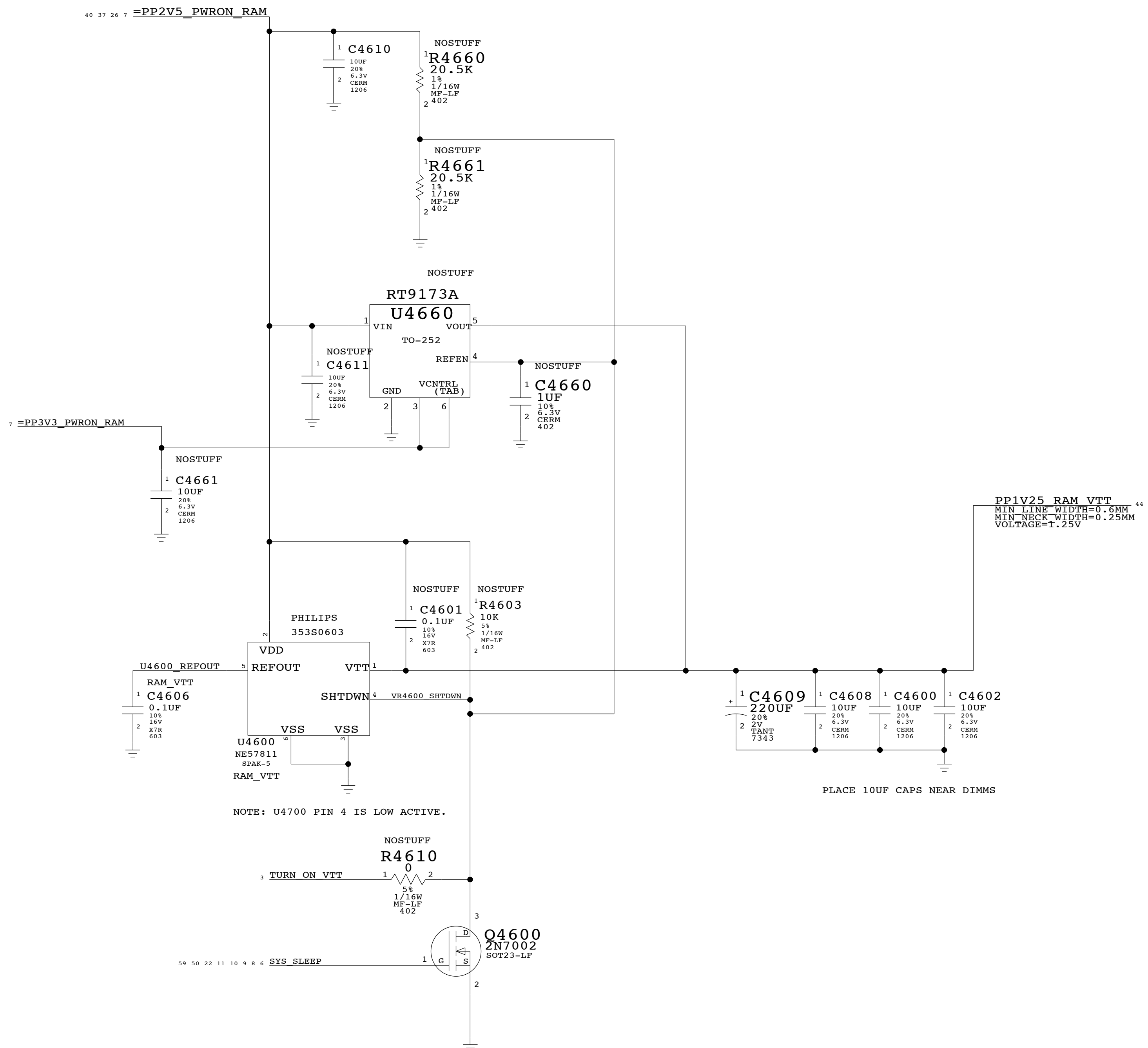
ONLY STUFF ONE VTT VREG



MEM TERM VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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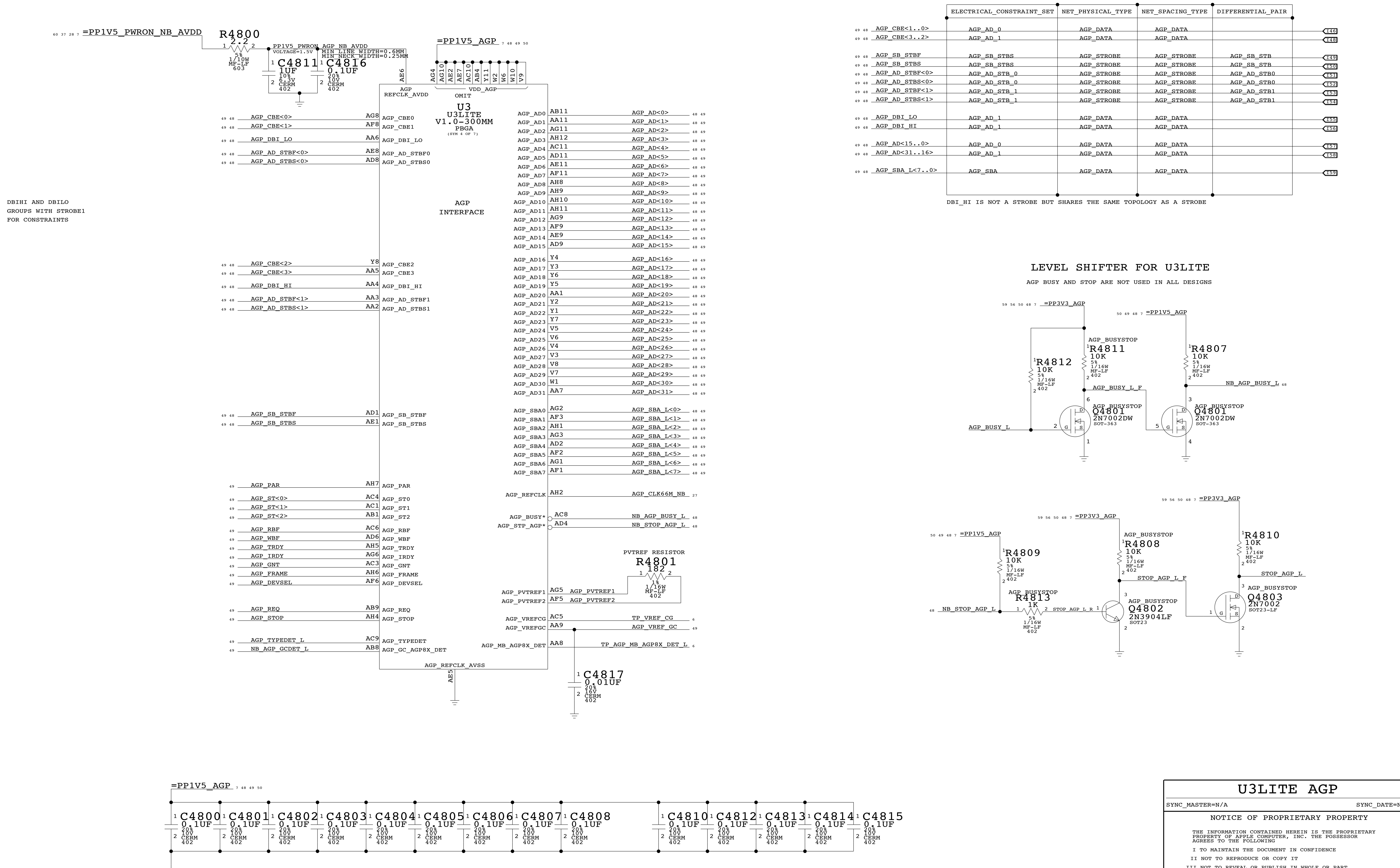
SCALE NONE	SHT 46 OF 102	



ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA	AGP_DATA	
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_STROBE	AGP_SB_STB
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_STROBE	AGP_SB_STB
AGP_AD_STBF<0>	AGP_AD_STB_0	AGP_STROBE	AGP_STROBE	AGP_AD_STB0
AGP_AD_STBS<0>	AGP_AD_STB_0	AGP_STROBE	AGP_STROBE	AGP_AD_STB0
AGP_AD_STBF<1>	AGP_AD_STB_1	AGP_STROBE	AGP_STROBE	AGP_AD_STB1
AGP_AD_STBS<1>	AGP_AD_STB_1	AGP_STROBE	AGP_STROBE	AGP_AD_STB1
AGP_DBI_LO	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_DBI_HI	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_AD<15..0>	AGP_AD_0	AGP_DATA	AGP_DATA	
AGP_AD<31..16>	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA	AGP_DATA	

DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

U3LITE AGP

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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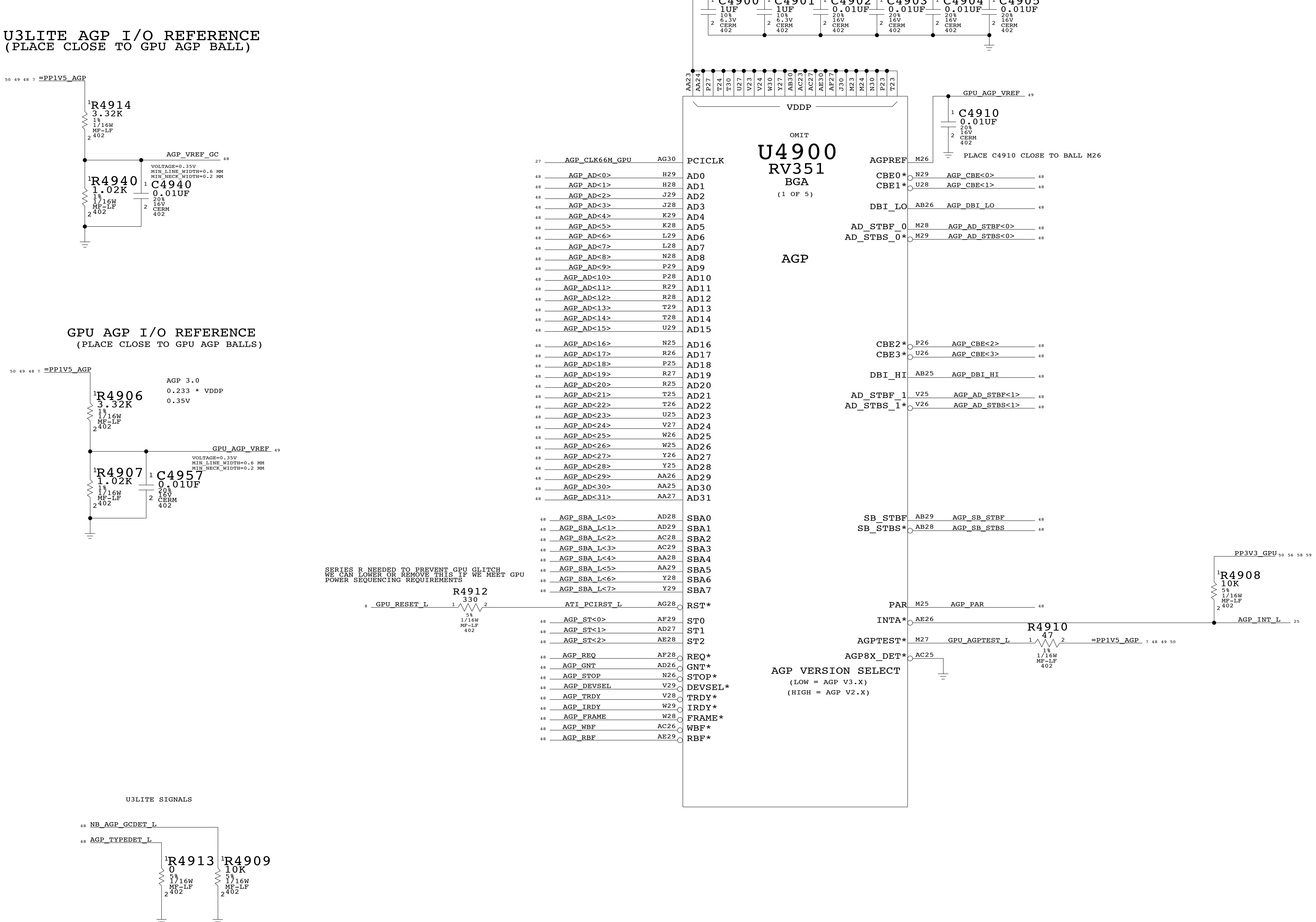
SCALE NONE	SHT 48 OF 102	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0231	1	IC,RV351LE, GRAPHICS CTLR	U4900	



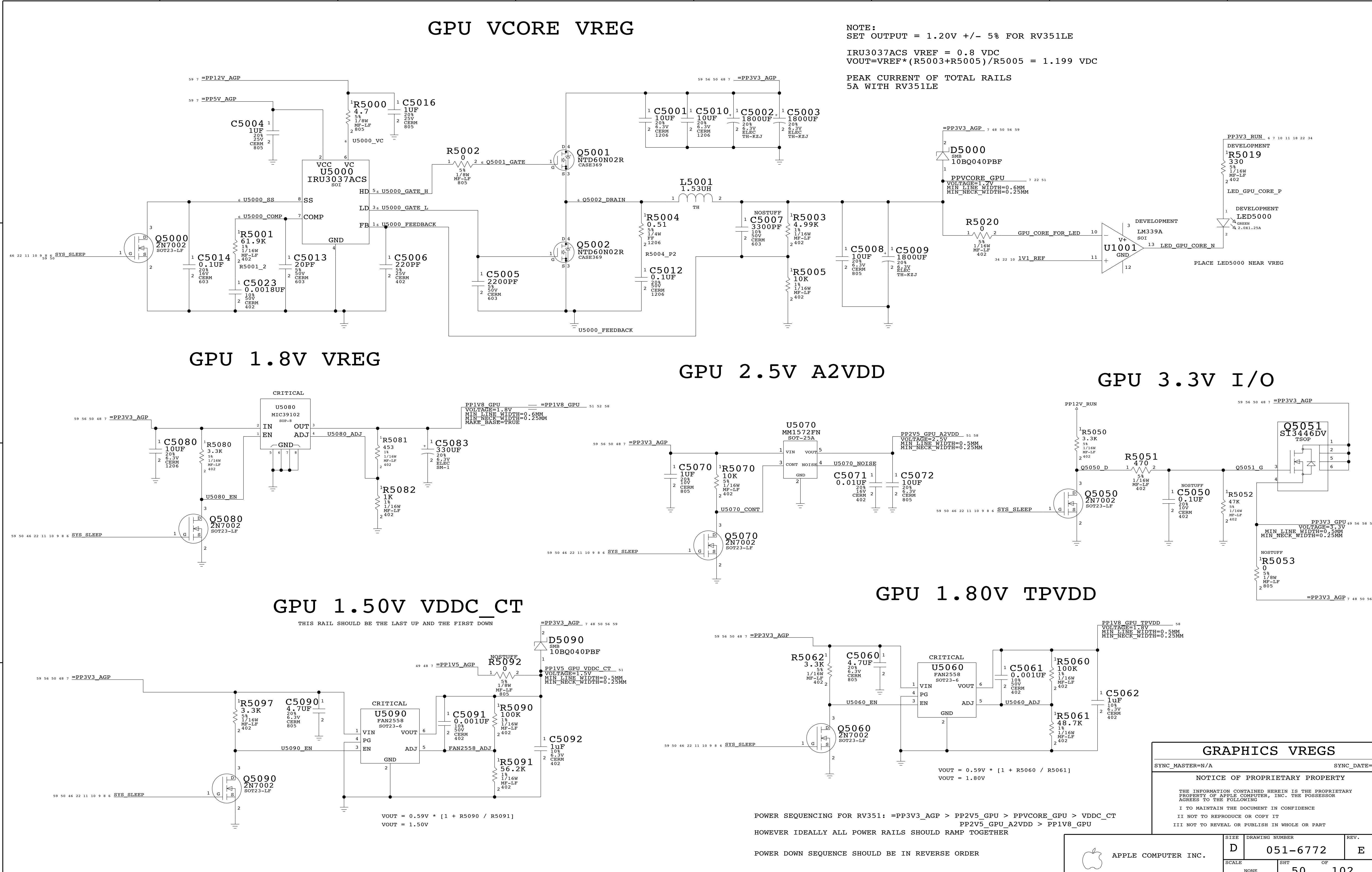
GPU AGP

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 49 OF 102	



NOTE:
SET OUTPUT = 1.20V +/- 5% FOR RV351LE

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R5003+R5005)/R5005 = 1.199 VDC

PEAK CURRENT OF TOTAL RAILS
5A WITH RV351LE

POWER SEQUENCING FOR RV351: =PP3V3_AGP > PP2V5_GPU > PPVCORE_GPU > VDDC_CT
PP2V5_GPU_A2VDD > PP1V8_GPU

HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER

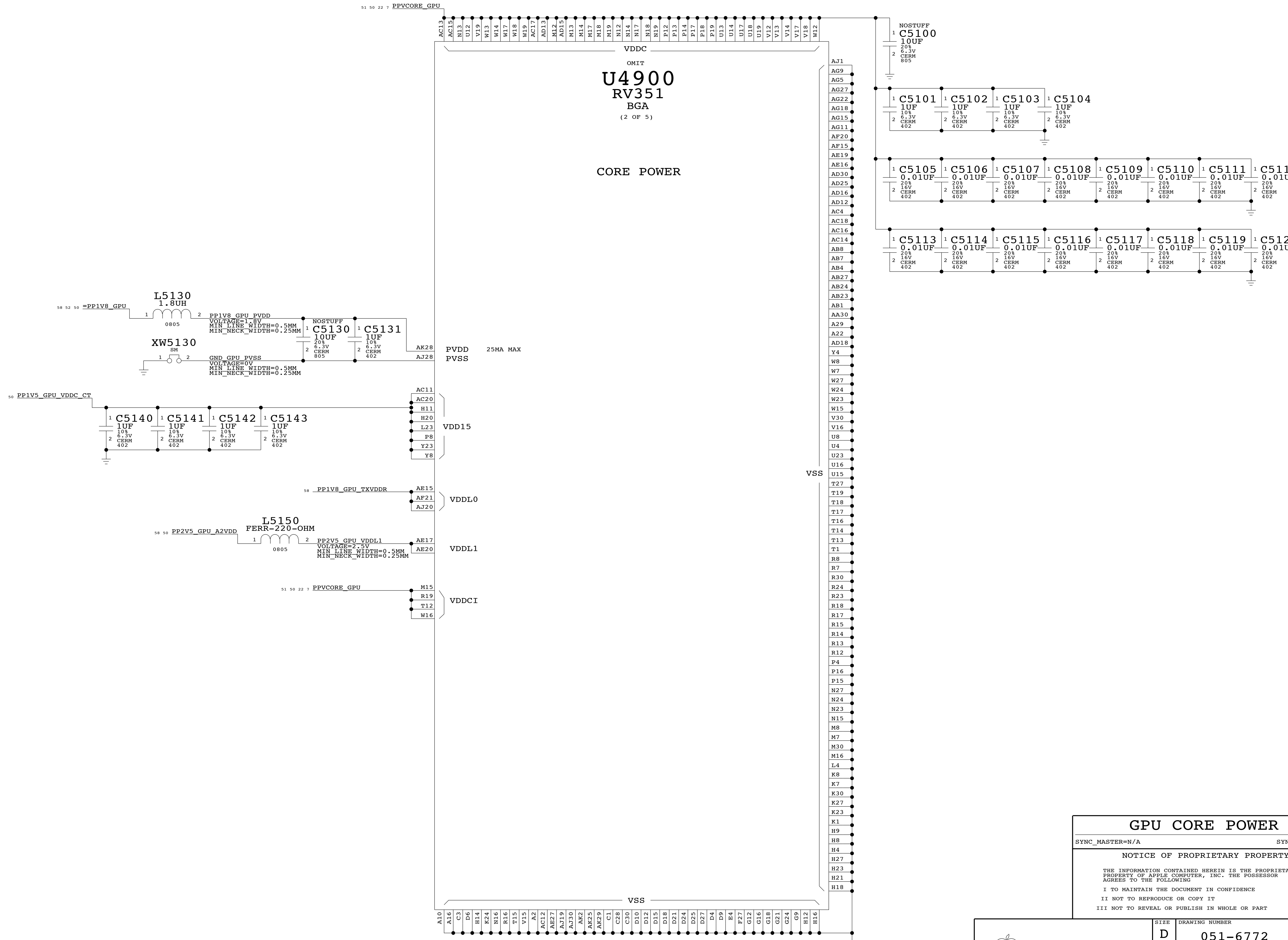
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

GRAPHICS VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 50	OF 102



GPU CORE POWER

SYNC_MASTER=N/A | SYNC_DATE=N/A

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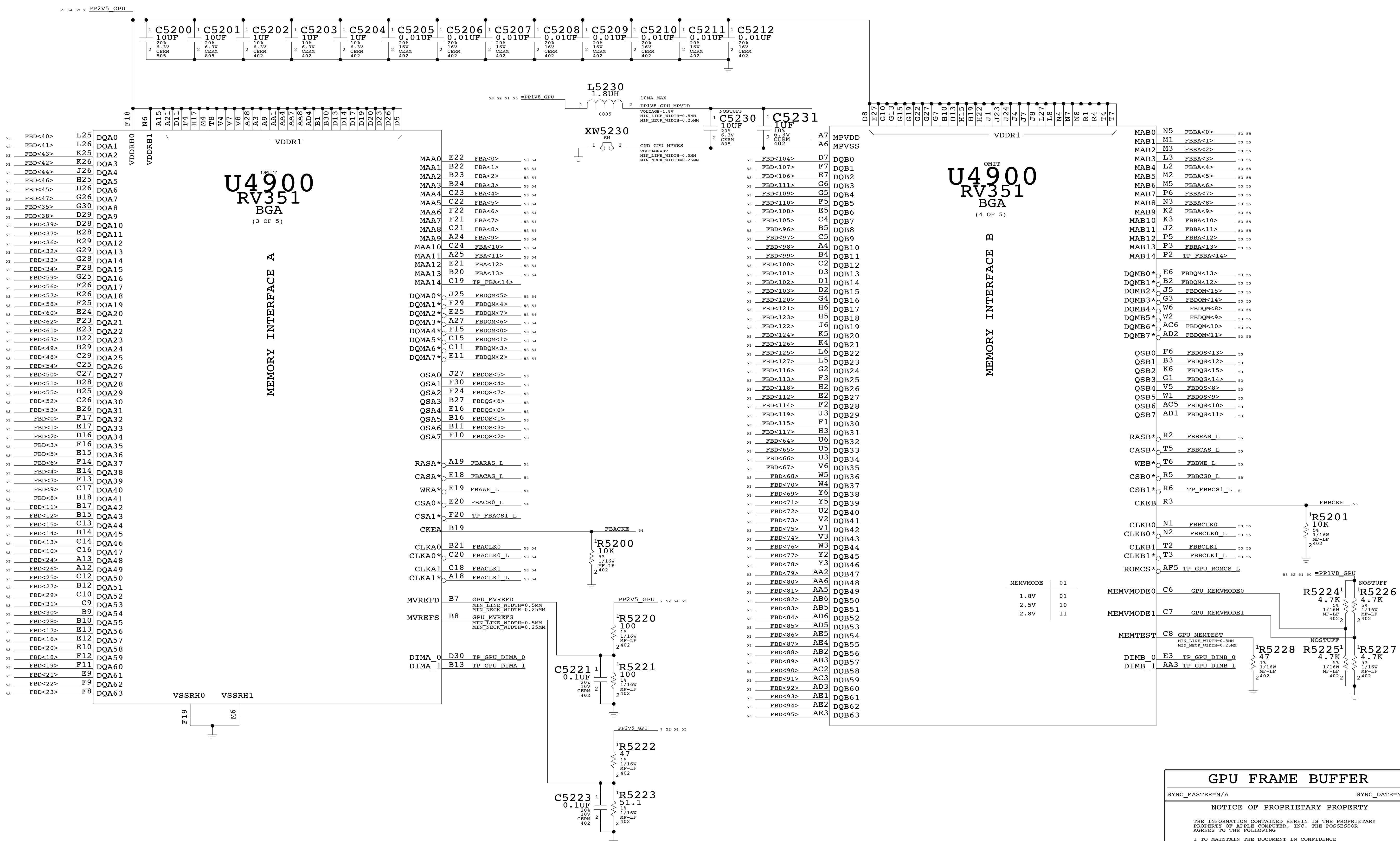
D	051-6772	E
SCALE NONE	SHT 51	OF 102



GPU FRAME BUFFER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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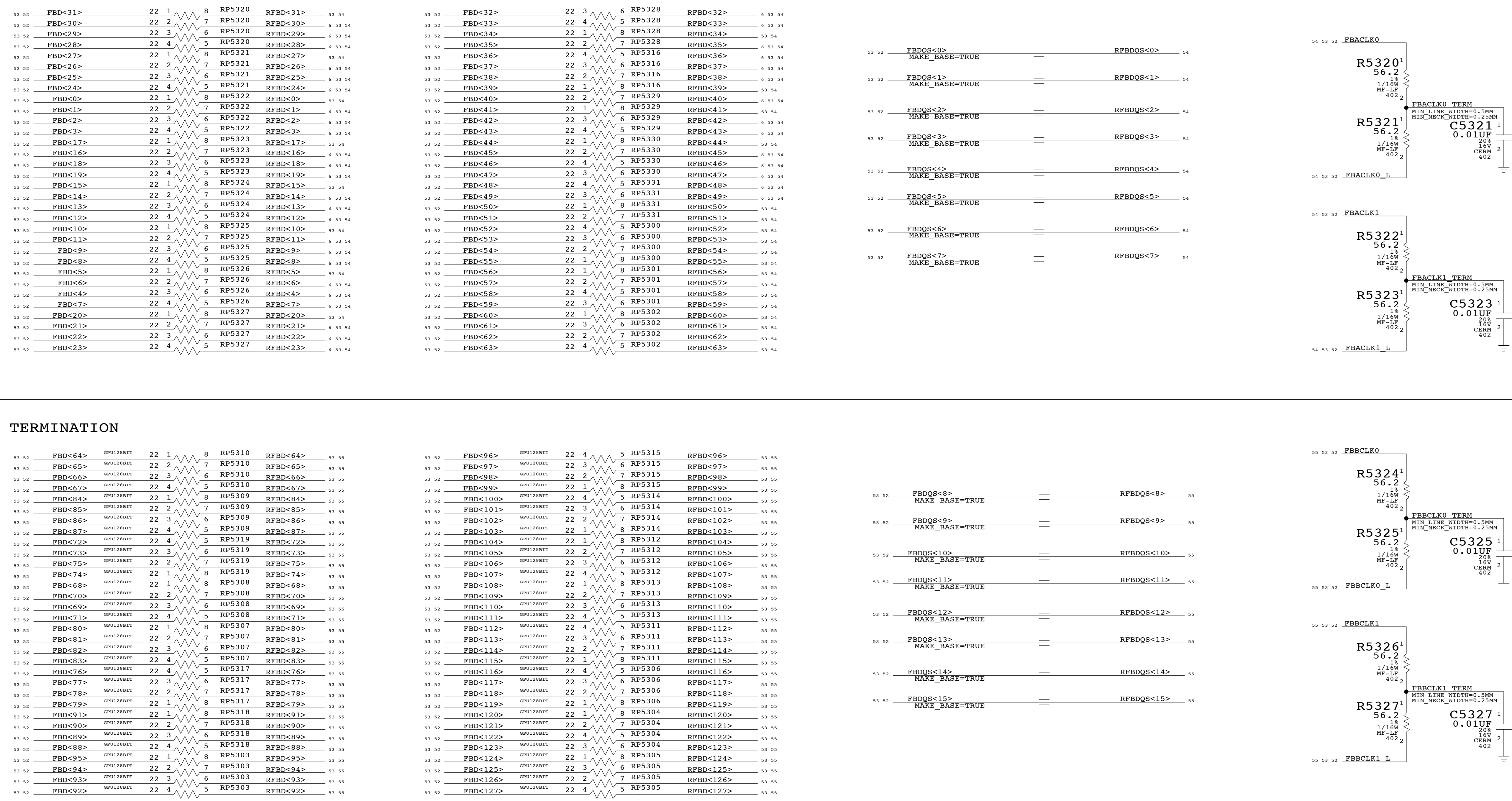
SCALE NONE	SHT 52	OF 102

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION



FRAME BUFFER B TERMINATION

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>		GPU_FB	GPU_FB	
RFBD<127..0>		GPU_FB	GPU_FB	
FBA<13..0>		GPU_FB	GPU_FB	
FBBA<13..0>		GPU_FB	GPU_FB	
FBDQM<15..0>		GPU_FB	GPU_FB	
FBDQS<15..0>		GPU_FB	GPU_FB	
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1

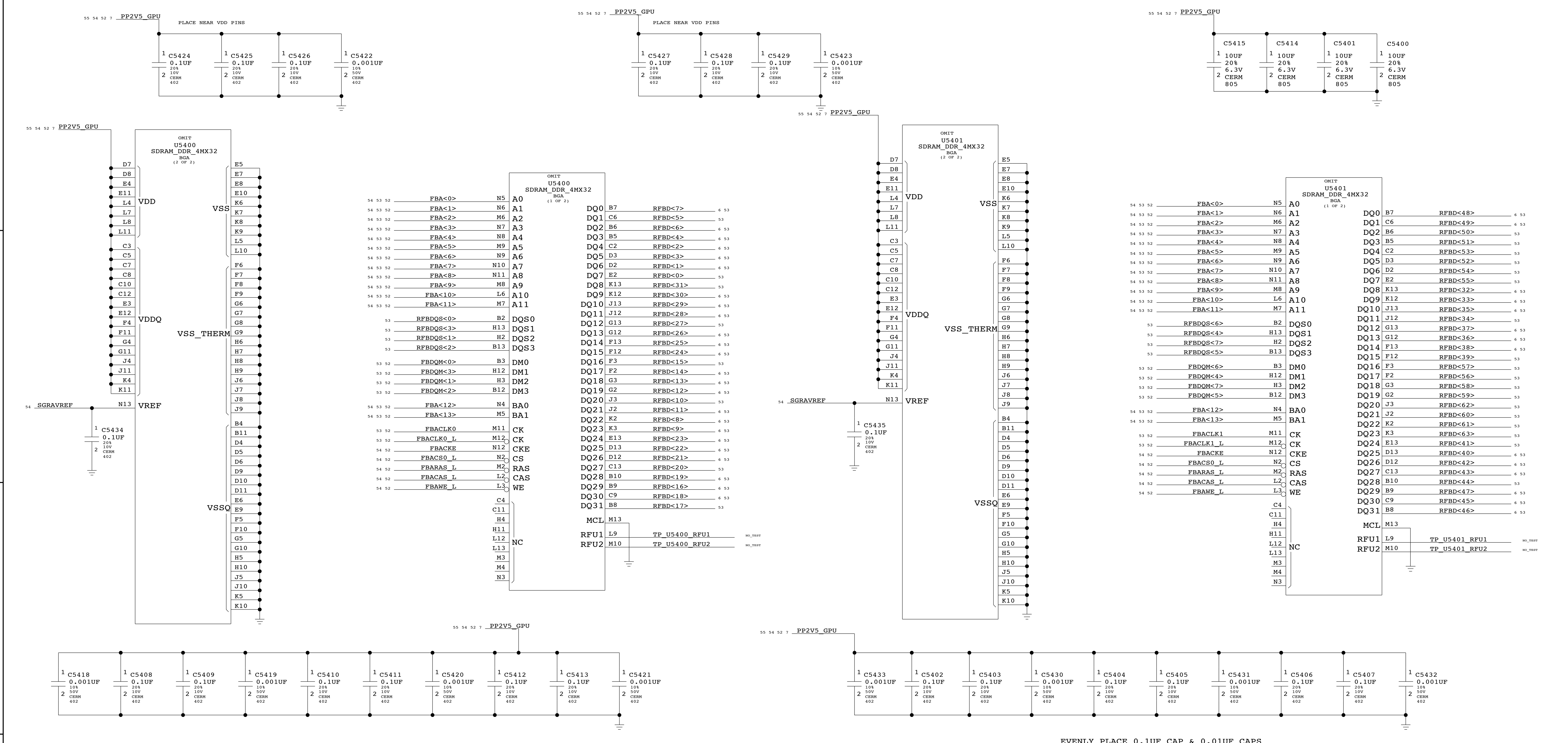
FB TERMINATION

SYNC_MASTER=N/A SYNC_DATE=N/A

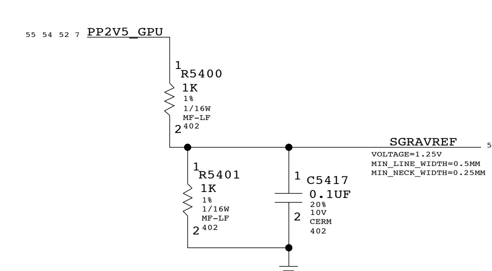
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 53 OF 102



DDR SDRAM A VREF



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX64
333S0341	2	SDRAM,8MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX128

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0290	333S0251	SAMSUNG64	U5400,U5401,U5500,U5501	HYN4M G-DIE
333S0292	333S0252	HYNIX64	U5400,U5401,U5500,U5501	SAM4M B-DIE

GPU DDR SDRAM A

SYNC_MASTER=N/A SYNC_DATE=N/A

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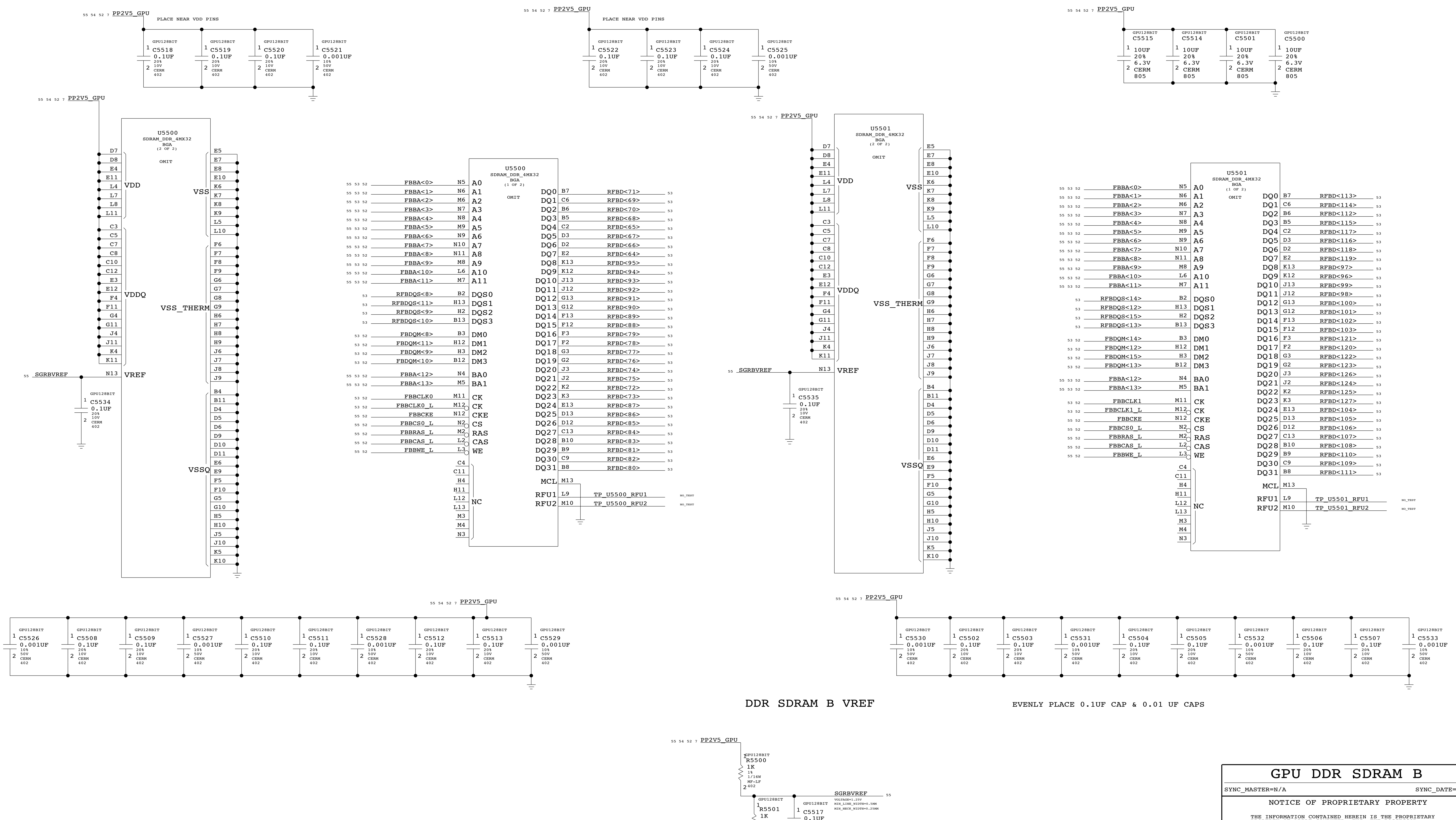
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE: NONE SHT 54 OF 102



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX64
333S0341	2	SDRAM,8MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX128

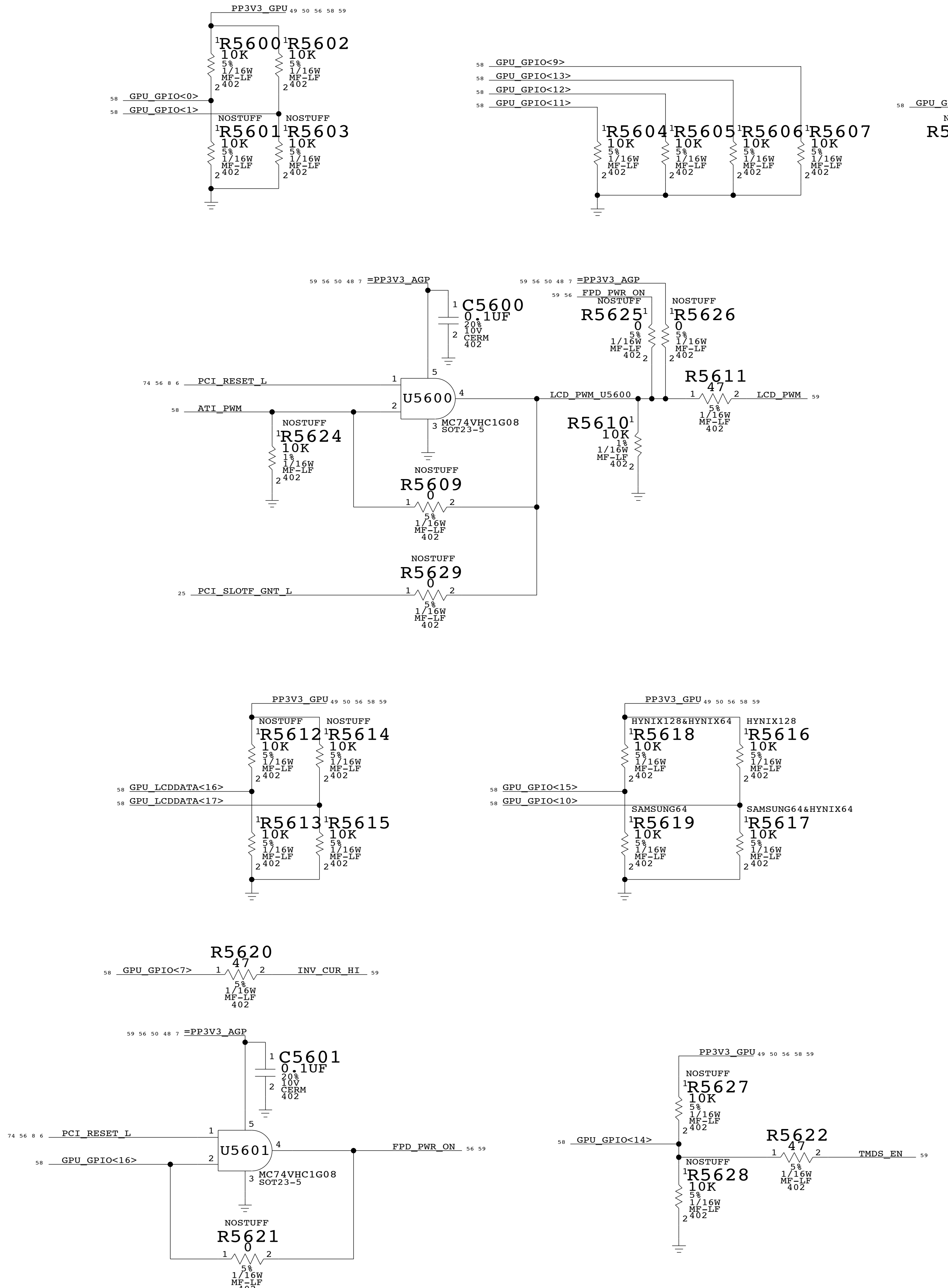
GPU DDR SDRAM B

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 55 OF 102



APPLE GPIO	ATI STRAP	PIN	DESCRIPTION	DEFAULT
	AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK) 00 - REFCLK SLIGHTLY EARLIER THEN FEEDBACK 01 - REFCLK 1 TAP EARLIER THEN FEEDBACK 10 - REFCLK 1 TAP LATER THEN FEEDBACK 11 - REFCLK 2 TAPS EARLIER THEN FEEDBACK CLOCK (ATI RECOMMENDED)	00 INTERNAL PULL-DOWN
	X1CLK_SKWE(1:0)	GPIO(3:2)	CLOCK PHASE ADJUSTMENT BETWEEN X1 CLK AND X2CLK 00 - 0 TAP DELAY	00 INTERNAL PULL-DOWN
	ROMIDCFG(3:0)	GPIO(9,13:11)	IF NO ROM ATTACHED, CONTROLS CHIP IDS. IF ROM- IDENTIFIES TYPE 0X0X - NO ROM, CHG_ID=0	
	ID_DISABLE	GPIO(8)	STRAP 0 - NORMAL OPERATION 1 - SHUTS THE CHIP DOWN BY NOT RESPONDING TO ANY CONFIG CYCLES	0 INTERNAL PULL-DOWN
	BUSCFG(2:0)	GPIO(6:4)	AGP8X_DETB BUSCFG[2:0] AGPMODE SIGNALING IDSEL 0 000 AGP8X 0.8V AD16	000 INTERNAL PULL-DOWN
	MULTIFUNC(1:0)	LCDDATA(17:16)	MULTI-FUNCTION DEVICE SELECT 00 - SINGLE FUNCTION DEVICE. 01 - TWO FUNCTION DEVICE. NO AGP IN EITHER FUNCTION 10 - TWO FUNCTION DEVICE. AGP ONLY IN FUNCTION 0 11 - TWO FUNCTION DEVICE. AGP IN BOTH FUNCTIONS IF BUSCFG PIN BASED STRAPS ARE SET TO PCI, THEN AGP WILL NOT BE ENABLED IN ANY FUNCTION.	00
	MEMSTRAP(1:0)	GPU_GPIO<15,10>	00 - SAMSUNG 4MX32 01 - UNDEFINED 10 - HYNIX 4MX32 11 - HYNIX 8MX32	
INV_CUR_HI		GPIO<7>	OUTPUT: GPU READS PANEL ID AND SETS THIS BIT ACCORDINGLY FOR REFERENCE ONLY, ACTIONS COME FROM BOOTROM SYSTEM / PANEL ID / INV_CUR_HI Q45 A / 0X9C27 / 1 0X9C38 / 0 Q45 B / 0X9C3A / 1 0X9C39 / 0 Q45 C / TBD / 1 TBD / 0 Q45 D / 0X9C3A / 1 Q45 A/B SUPPORT IS FOR DEVELOPMENT	
FPD_PWR_ON		GPIO<16>	OUTPUT: PANEL POWER SEQUENCING	
TMDS_EN		GPIO<14>	INPUT: PANEL POWER SEQUENCING	

GPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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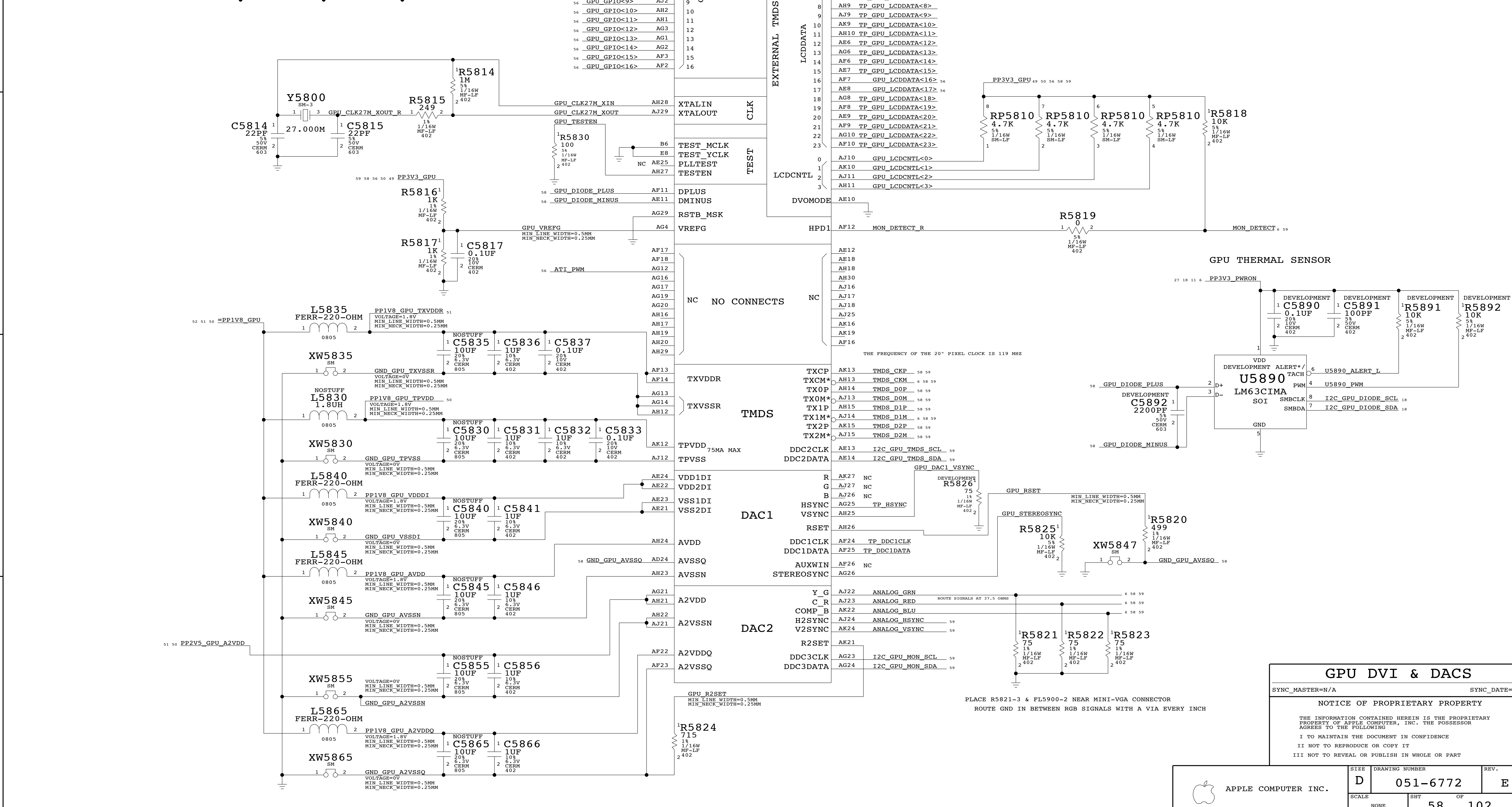
DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_CKP	TMDS	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS_CKM		GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS_D0P	TMDS	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS_D0M		GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS_D1P	TMDS	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS_D1M		GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS_D2P	TMDS	GPU_TMDS	GPU_TMDS	TMDS_D2
TMDS_D2M		GPU_TMDS	GPU_TMDS	TMDS_D2
ANALOG_GRN		GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_RED		GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_BLU		GPU_VGA_37P5	GPU_VGA_37P5	



GPU DVI & DACS

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE NONE SHT 58 OF 102

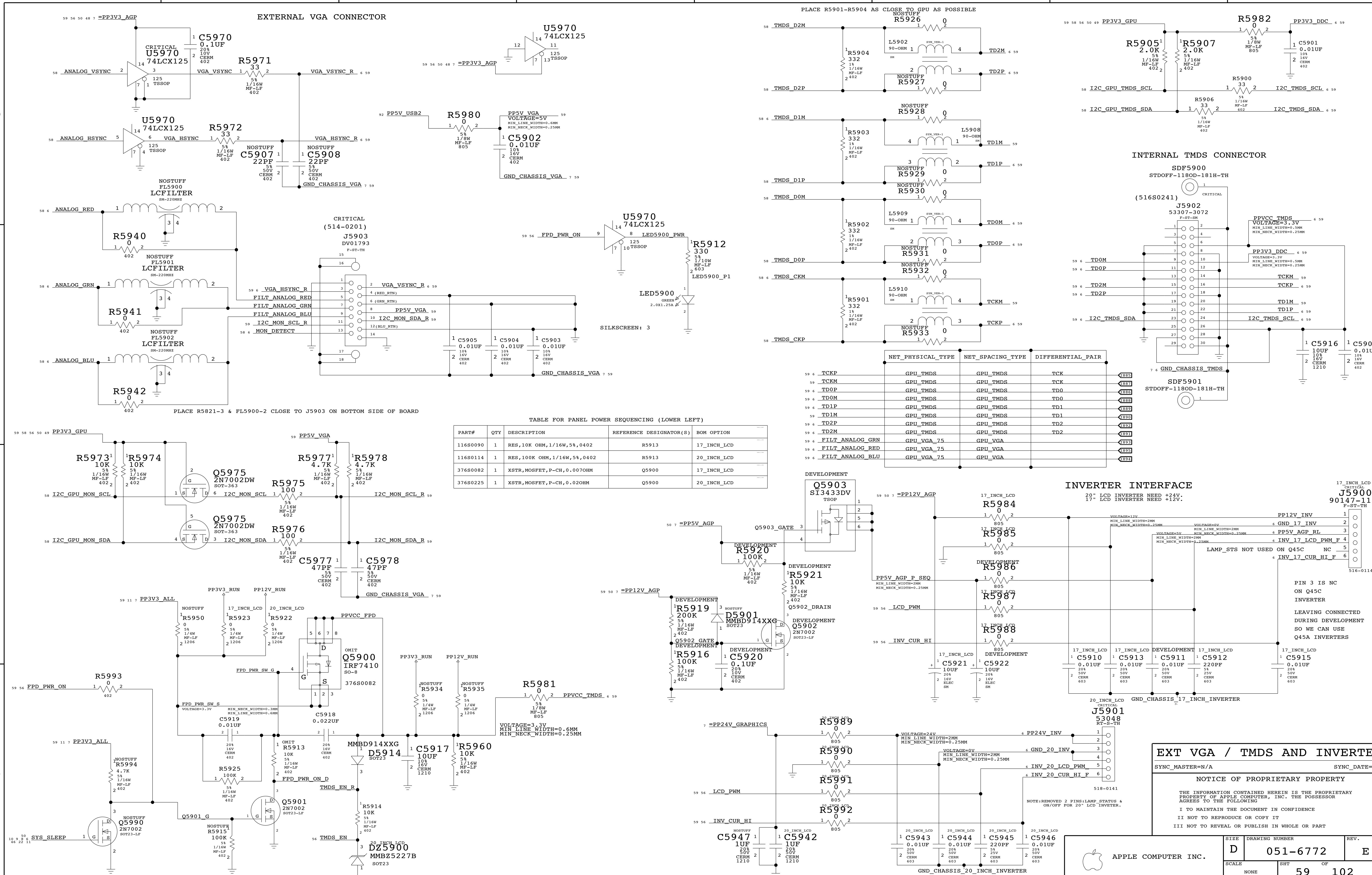


TABLE FOR PANEL POWER SEQUENCING (LOWER LEFT)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S0114	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
376S0082	1	XSTR,MOSFET,P-CH,0.007OHM	Q5900	17_INCH_LCD
376S0225	1	XSTR,MOSFET,P-CH,0.020HM	Q5900	20_INCH_LCD

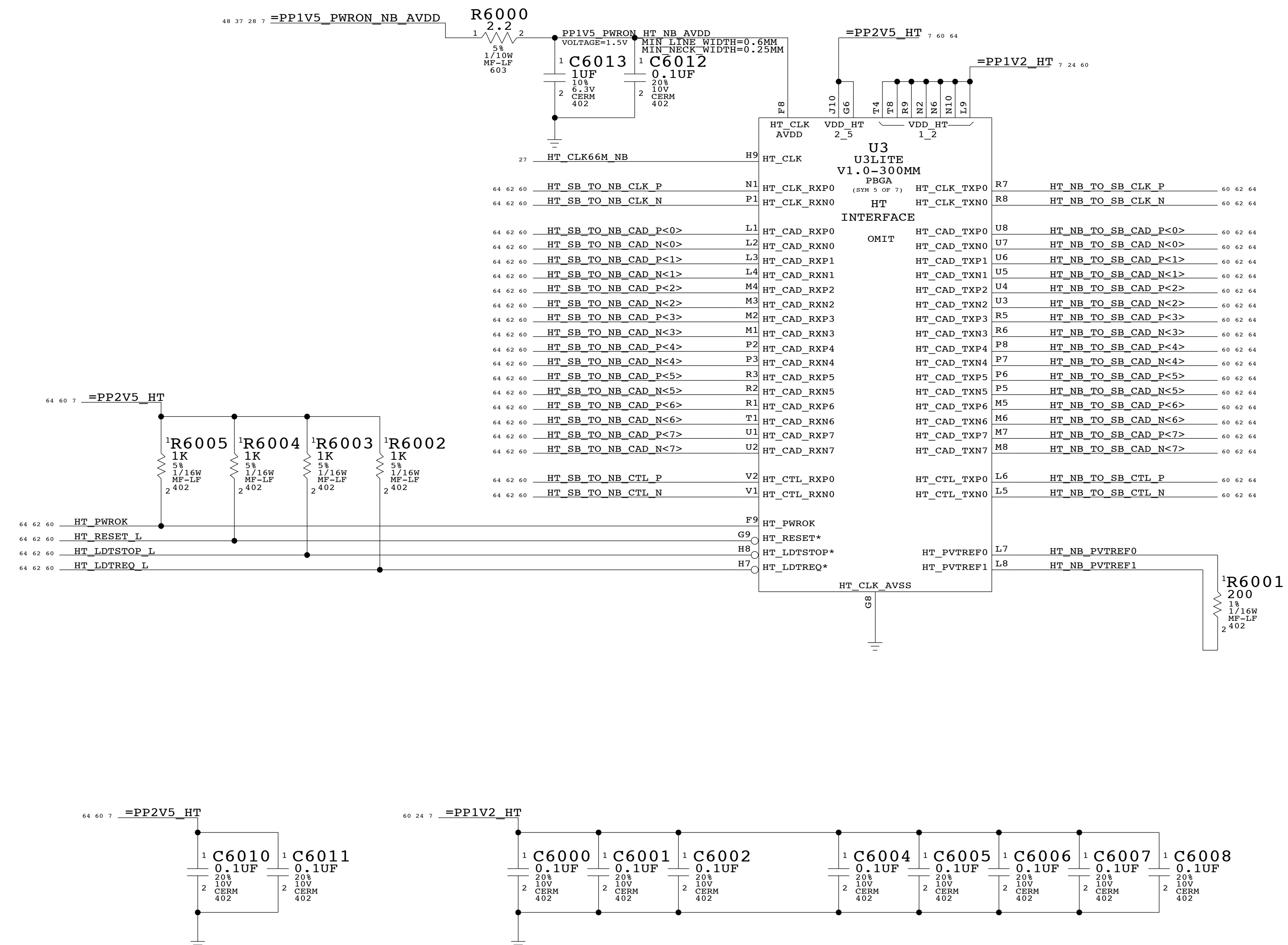
	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TCKP	GPU_TMDS	GPU_TMDS	TCK
TCKM	GPU_TMDS	GPU_TMDS	TCK
TD0P	GPU_TMDS	GPU_TMDS	TD0
TD0M	GPU_TMDS	GPU_TMDS	TD0
TD1P	GPU_TMDS	GPU_TMDS	TD1
TD1M	GPU_TMDS	GPU_TMDS	TD1
TD2P	GPU_TMDS	GPU_TMDS	TD2
TD2M	GPU_TMDS	GPU_TMDS	TD2
FILT_ANALOG_GRN	GPU_VGA_75	GPU_VGA	
FILT_ANALOG_RED	GPU_VGA_75	GPU_VGA	
FILT_ANALOG_BLU	GPU_VGA_75	GPU_VGA	

EXT VGA / TMDS AND INVERTER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 59	OF 102



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
HT_PWROK	HT_PWROK	HT_2V5	HT_2V5	
HT_RESET_L	HT_CTL	HT_2V5	HT_2V5	
HT_LDTSTOP_L	HT_CTL	HT_2V5	HT_2V5	
HT_LDTREQ_L	HT_CTL	HT_2V5	HT_2V5	

HT_NB_TO_SB HT_SB_TO_NB

5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5

4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE CAN BE LOOSE
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

U3LITE HT

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE NONE SHT 60 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	P25MM	

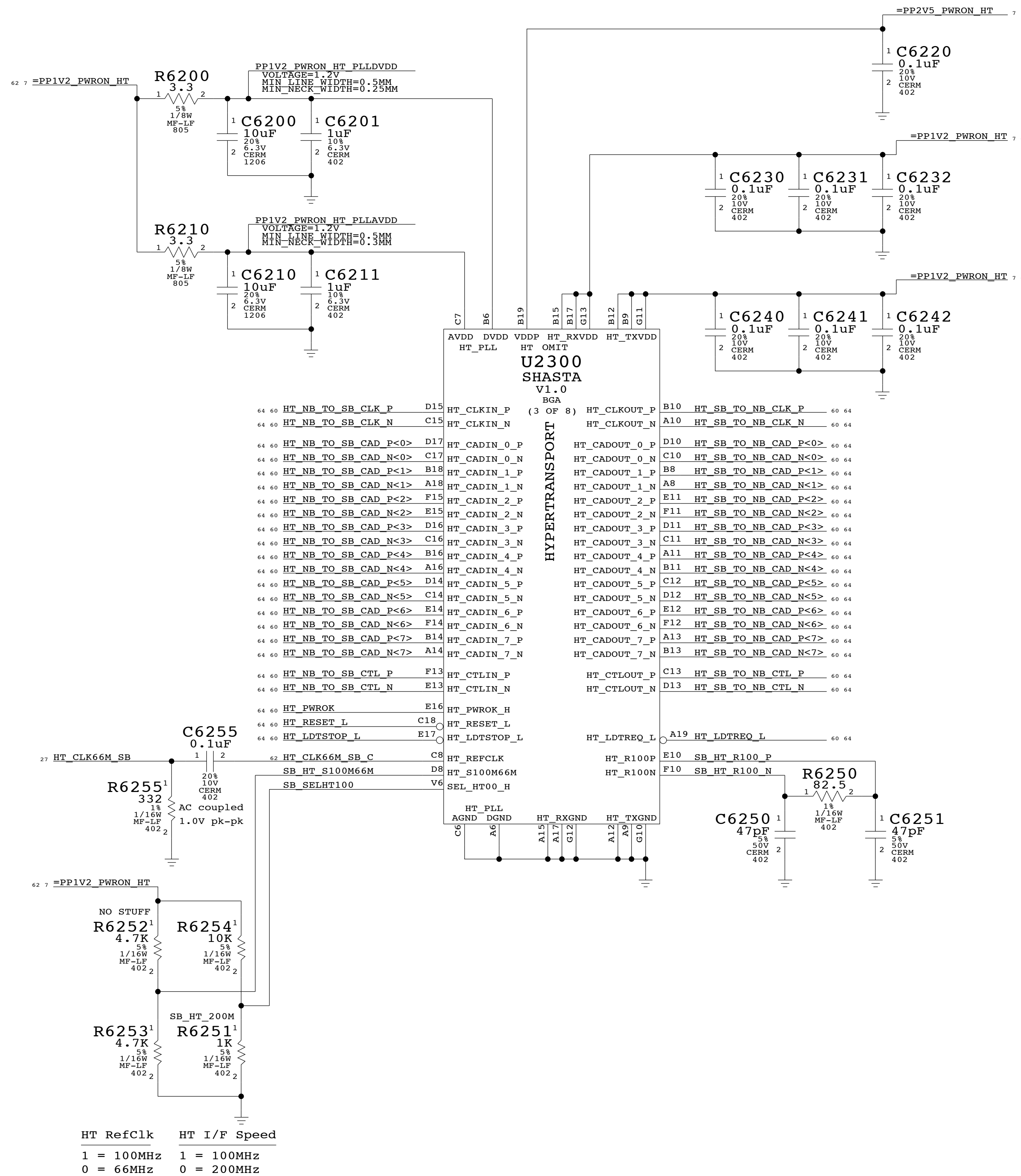
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



Shasta HyperTransport

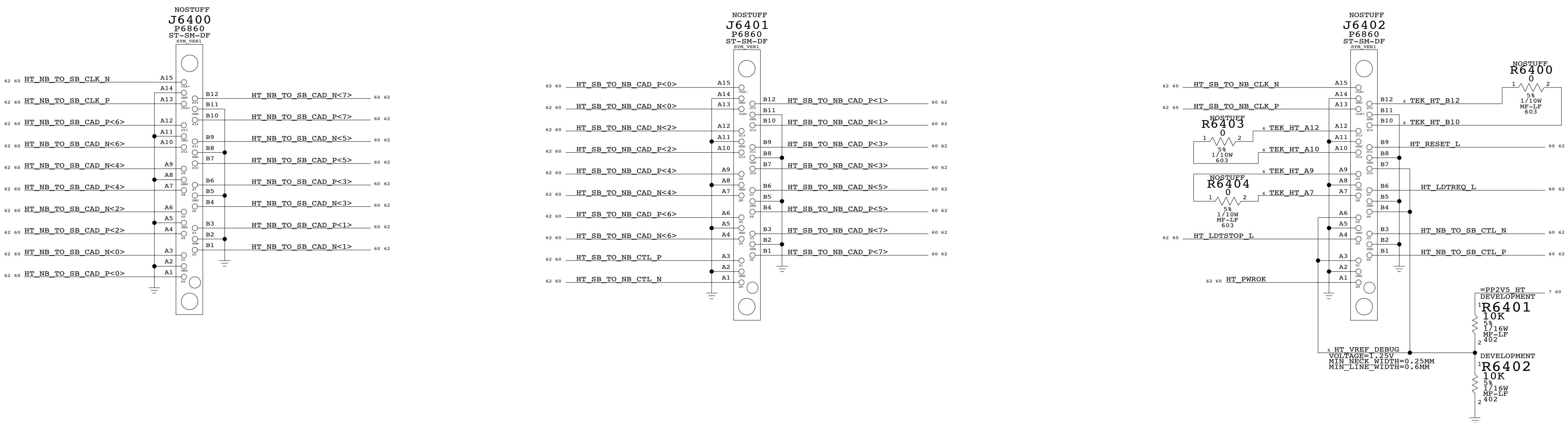
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 62	OF 102

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2



HT DEBUG CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 64 OF 102	

8	7	6	5	4	3	2	1

D

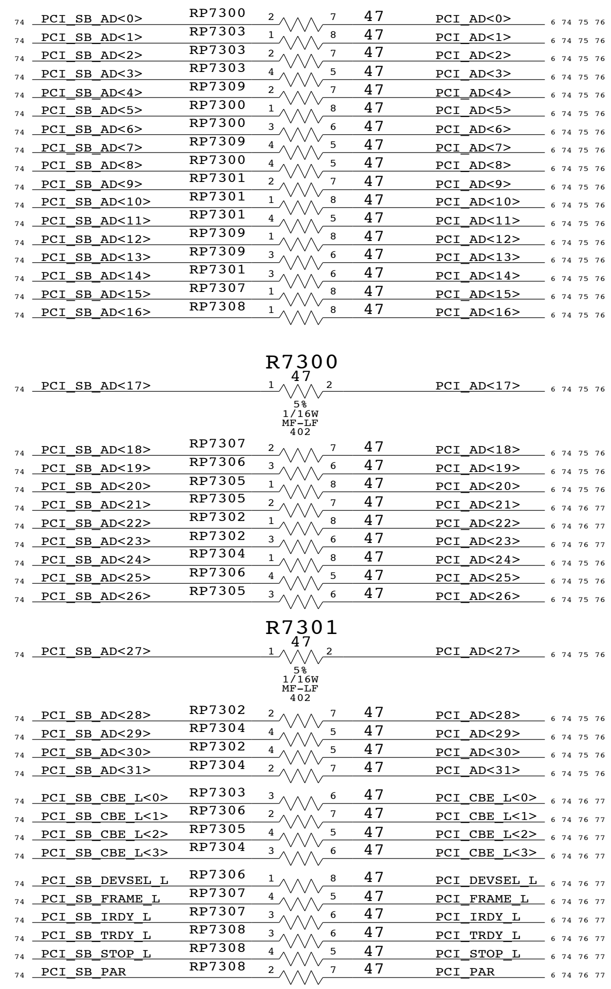
C

B

A

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)



PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 73 OF 102	

8	7	6	5	4	3	2	1

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCI_AD	PCI		PCI_AD<31..28> 6 73 75 76 77
PCI_AD27	PCI		PCI_AD<27> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<26..24> 6 73 75 76 77
PCI_AD23	PCI		PCI_AD<23> 6 73 76 77
PCI_AD22	PCI		PCI_AD<22> 6 73 76 77
PCI_AD21	PCI		PCI_AD<21> 6 73 76 77
PCI_AD20	PCI		PCI_AD<20> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<19..18> 6 73 75 76 77
PCI_AD17	PCI		PCI_AD<17> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<16..0> 6 73 75 76 77
PCI	PCI		PCI_CBE_L<3..0> 6 73 76 77
PCI	PCI		PCI_PAR 6 73 76 77
PCI_CTL	PCI		PCI_DEVSEL_L 6 73 74 76 77
PCI_CTL	PCI		PCI_FRAME_L 6 73 74 76 77
PCI_CTL	PCI		PCI_IRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_TRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_STOP_L 6 73 74 76 77

Page Notes

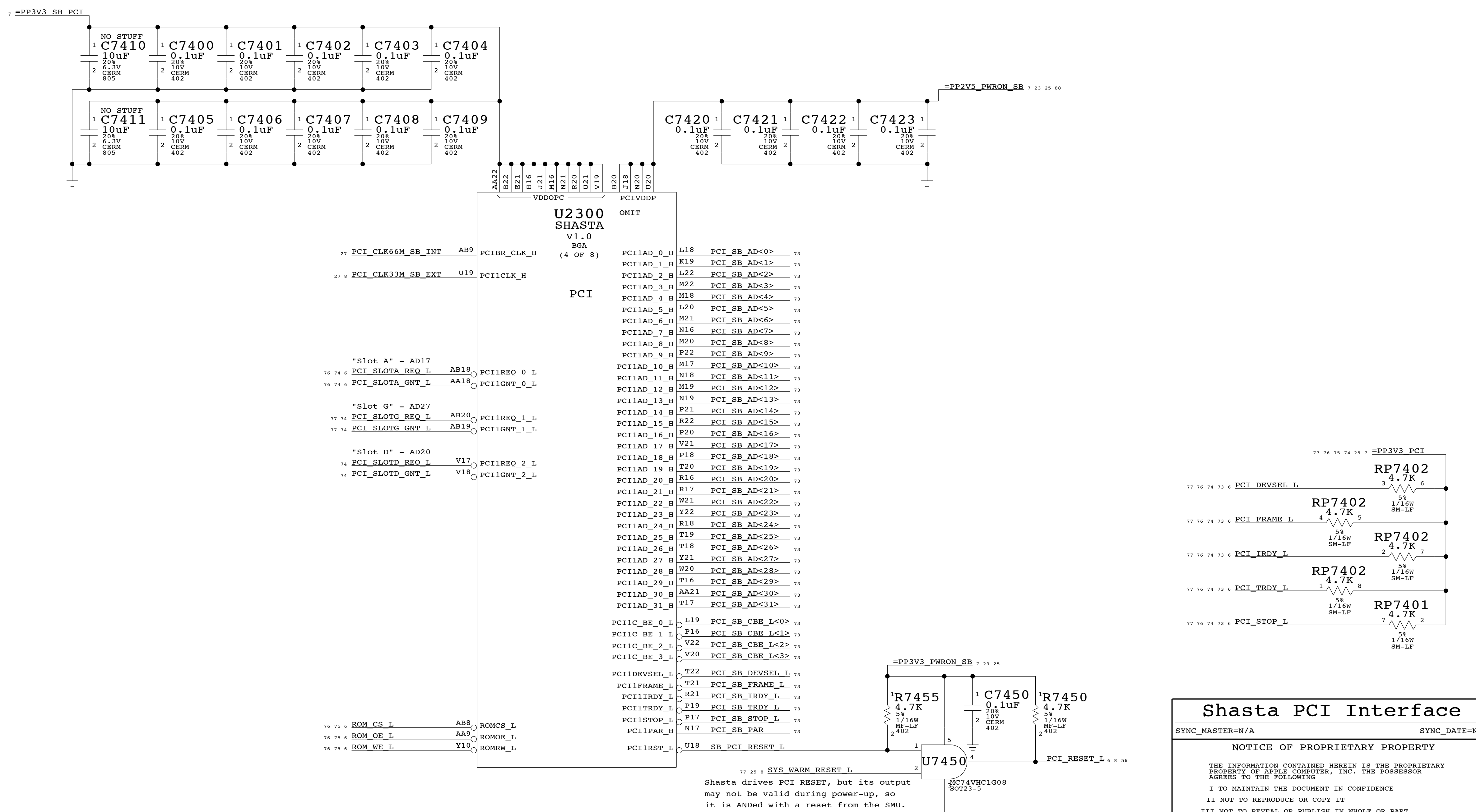
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

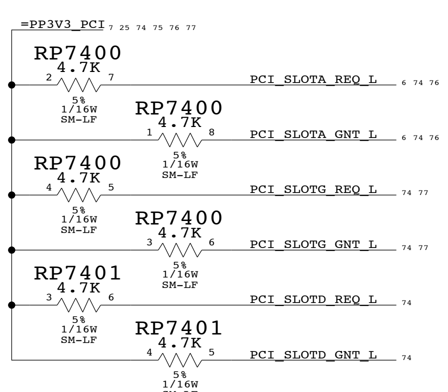
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)





Shasta PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 74 OF 102	

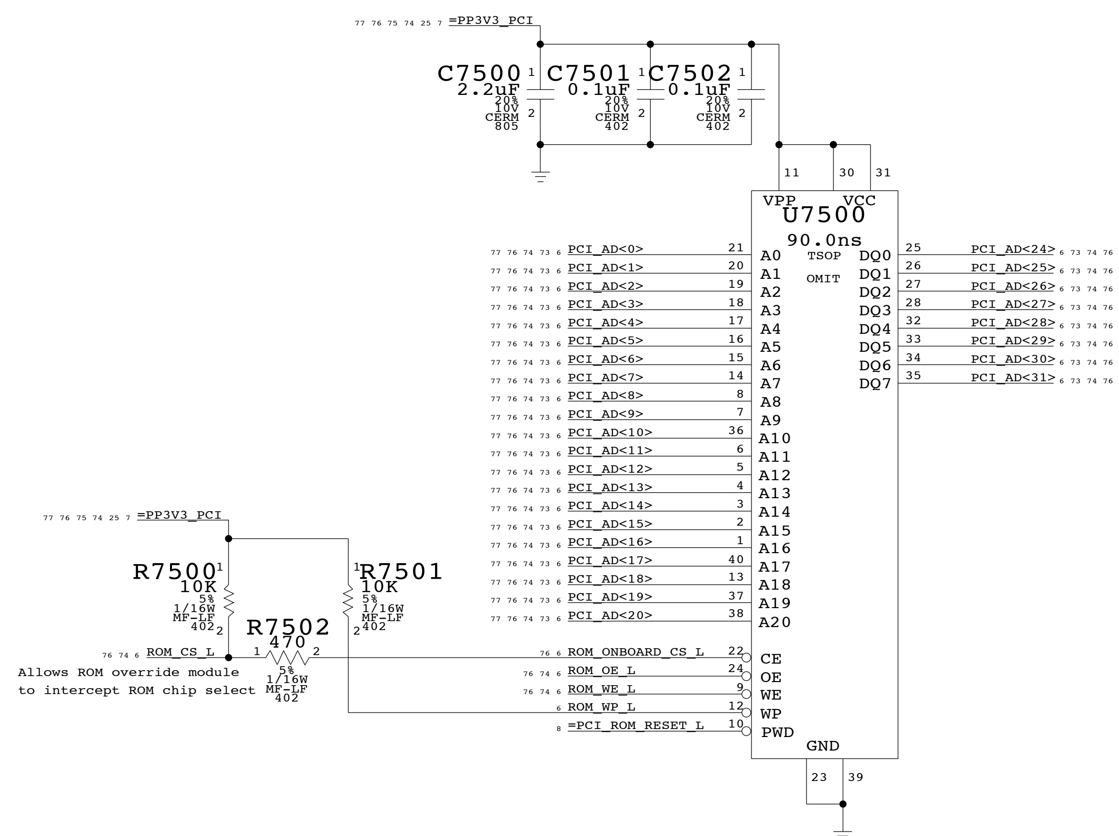
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 75	OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

_PCI_CLK33M_AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

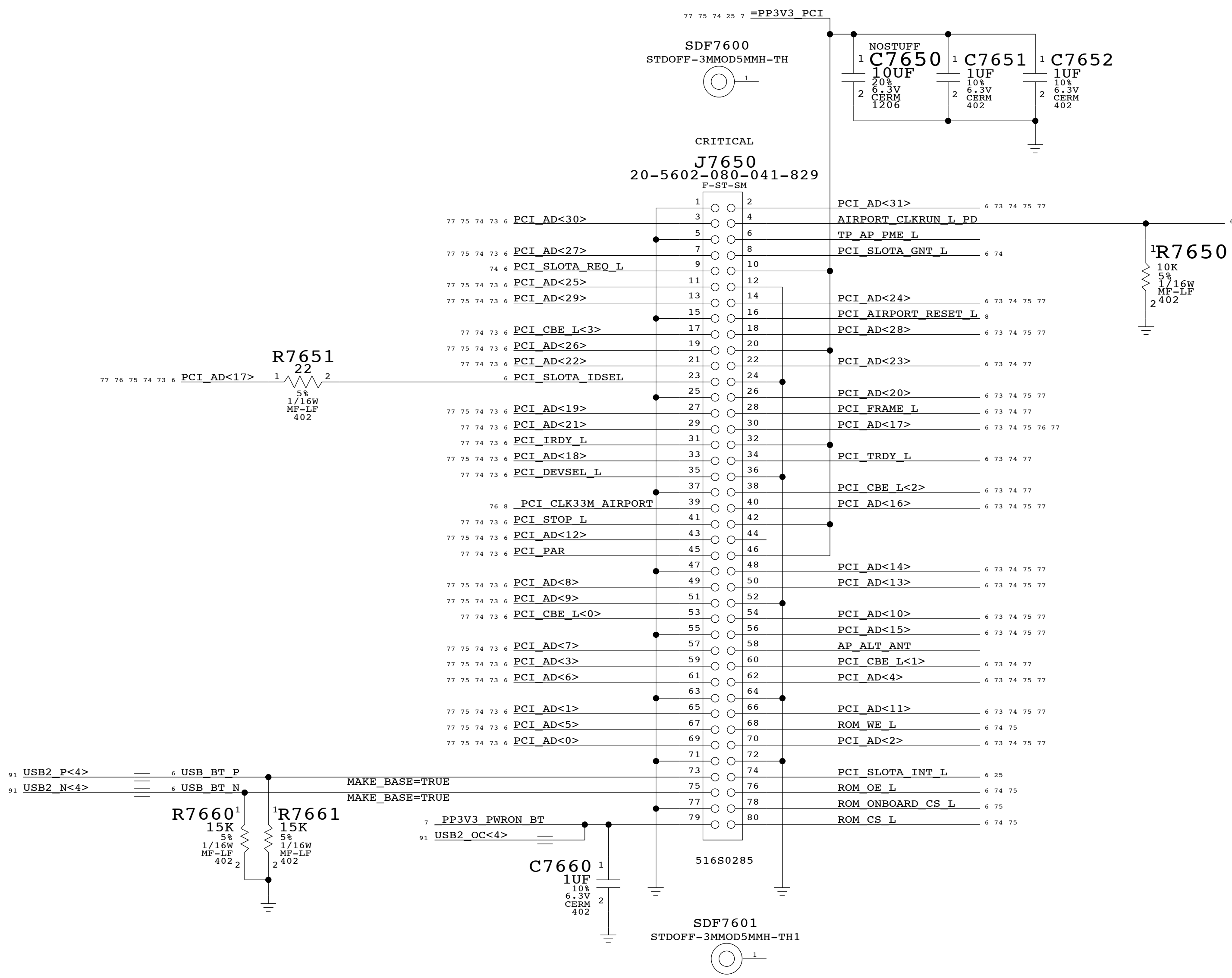
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does
not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 76	OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

=PCI_CLK33M_USB2 8 77

Page Notes

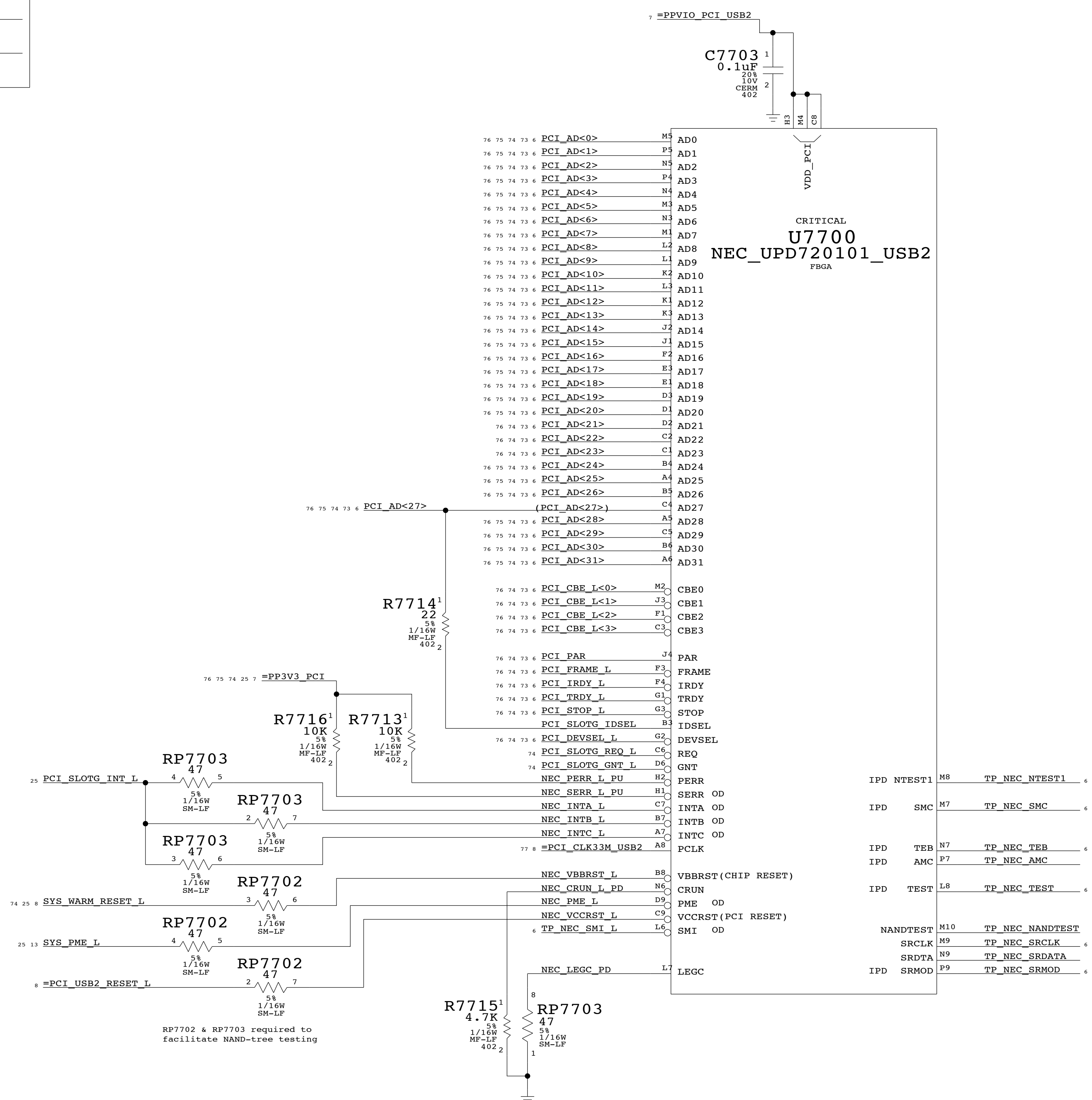
Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.



USB 2.0 PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 77	OF 102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD				UATA_DD<15..8>
UATA_DD7				UATA_DD<7>
UATA_DD				UATA_DD<6..0>
UATA_HOST				UATA_DA<2..0>
UATA_HOST				UATA_CS0_L
UATA_HOST				UATA_CS1_L
UATA_HOST				UATA_HSTROBE
UATA_HOST				UATA_STOP
UATA_HOST_R				UATA_DMACK_L
UATA_HOST_R				UATA_RESET_L
UATA_DEV_R_C				UATA_DSTROBE
UATA_DEV_R				UATA_DMARQ
UATA_DEV_R				UATA_INTRQ

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

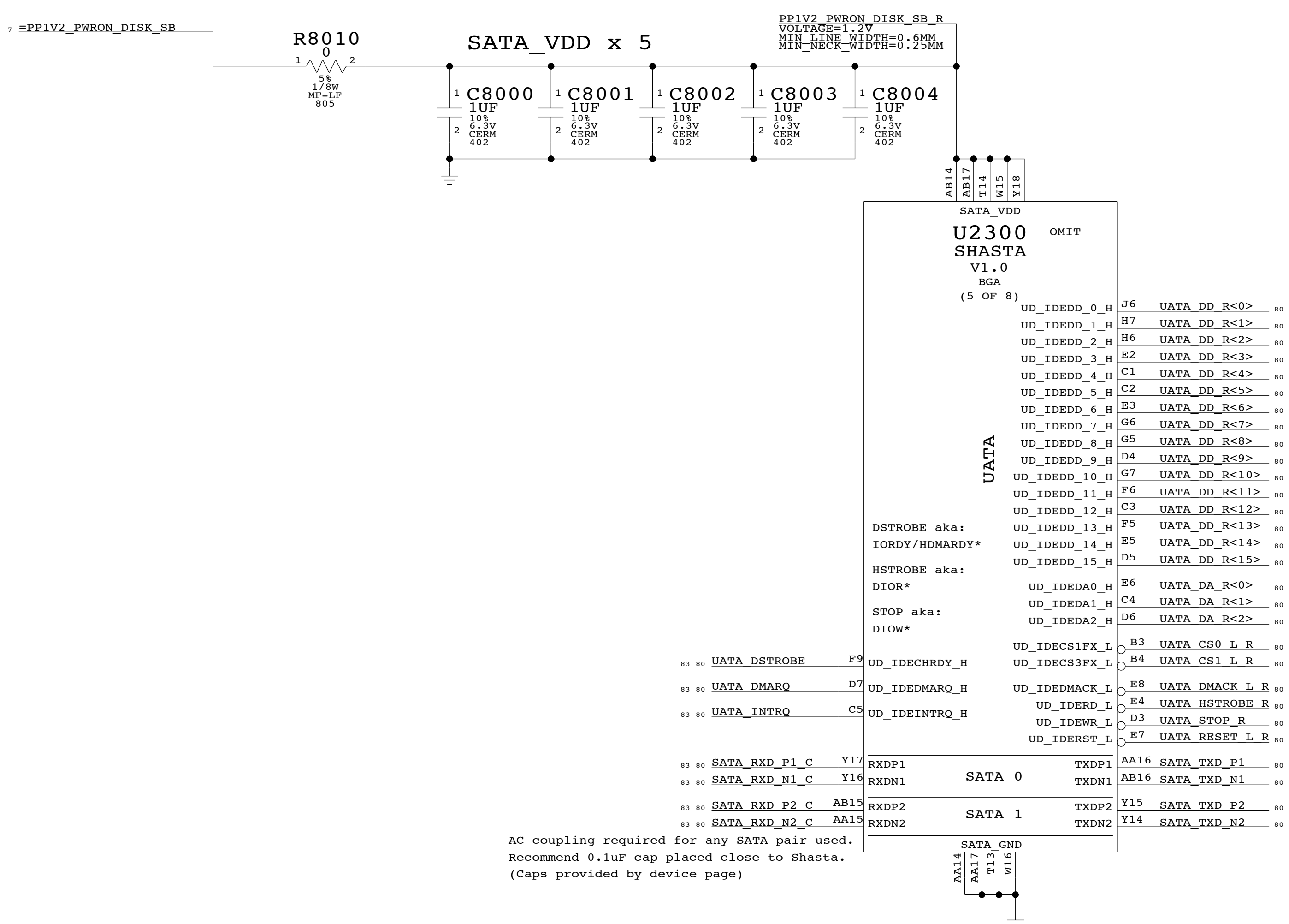
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

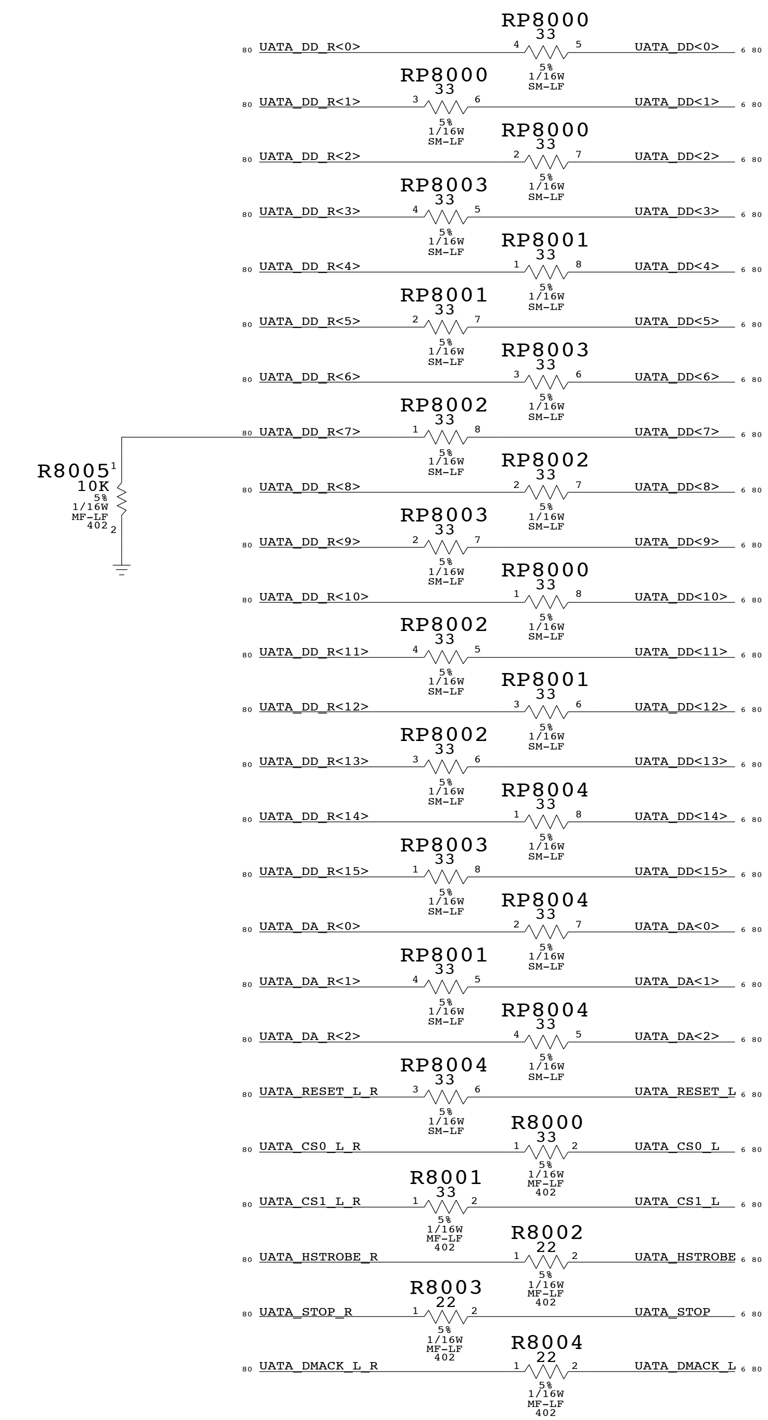
Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.



UATA Termination



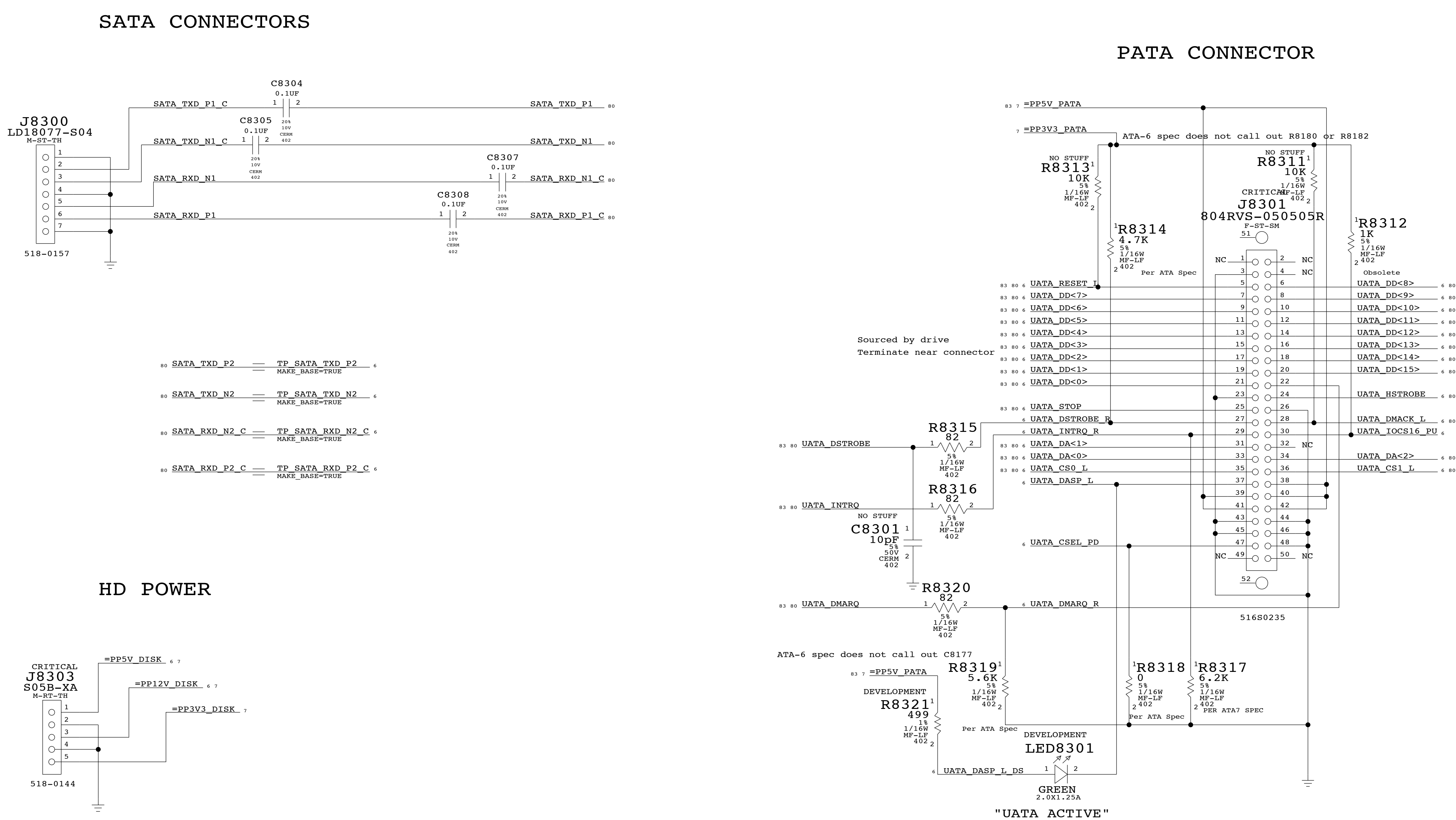
Shasta Disk

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 80 OF 102	

Net	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
UATA_DD<15..8>	UATA_DD			
UATA_DD<7>	UATA_DD7			
UATA_DD<6..0>	UATA_DD			
UATA_DA<2..0>	UATA_HOST			
UATA_CS0_L	UATA_HOST			
UATA_CS1_L	UATA_HOST			
UATA_HSTROBE	UATA_HOST			
UATA_STOP	UATA_HOST			
UATA_DMACK_L	UATA_HOST_R			
UATA_RESET_L	UATA_HOST_R			
UATA_DSTROBE	UATA_DEV_R_C			
UATA_DMARQ	UATA_DEV_R			
UATA_INTRQ	UATA_DEV_R			



DISK CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 83	OF 102

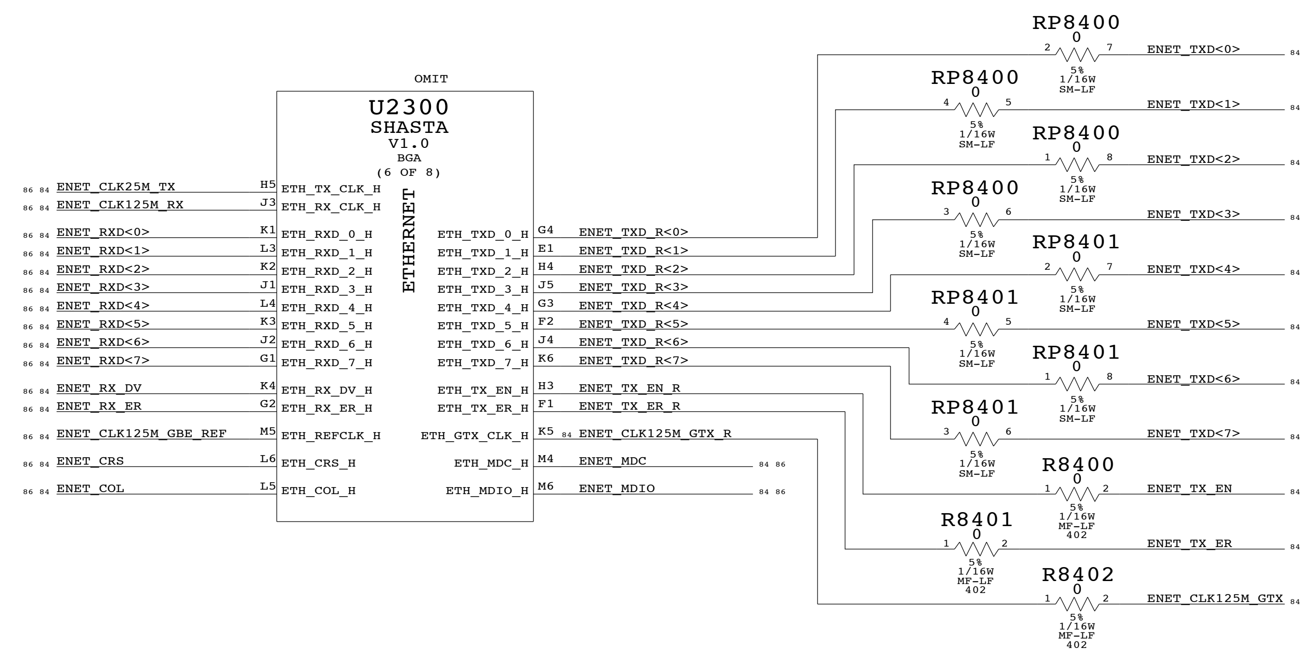
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_RX_CLK		P25MM		ENET_CLK25M_TX
ENET_RX_CLK		P25MM		ENET_CLK125M_RX
ENET_GBE_REF		P25MM		ENET_CLK125M_GBE_REF
ENET_TX_CLK		P25MM		ENET_CLK125M_GTX
				ENET_CLK125M_GTX_R
ENET_RX				ENET_RXD<7..0>
ENET_RX_CTL				ENET_RX_DV
ENET_RX_CTL				ENET_RX_ER
ENET_TX				ENET_TXD<7..0>
ENET_TX_CTL				ENET_TX_EN
ENET_TX_CTL				ENET_TX_ER
ENET_RX_CTL				ENET_CRS
ENET_RX_CTL				ENET_COL
ENET_MDC				ENET_MDC
ENET_MDIO				ENET_MDIO

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Shasta Ethernet

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 84	OF 102

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	P25MM			ENET_CLK125M_GBE_REF_R
	P25MM			ENET_CLK125M_RX_R
	P25MM			ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTAL	P25MM			VESTA_CLK25M_XTALI
	P25MM			VESTA_CLK25M_XTALO
	P25MM			VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

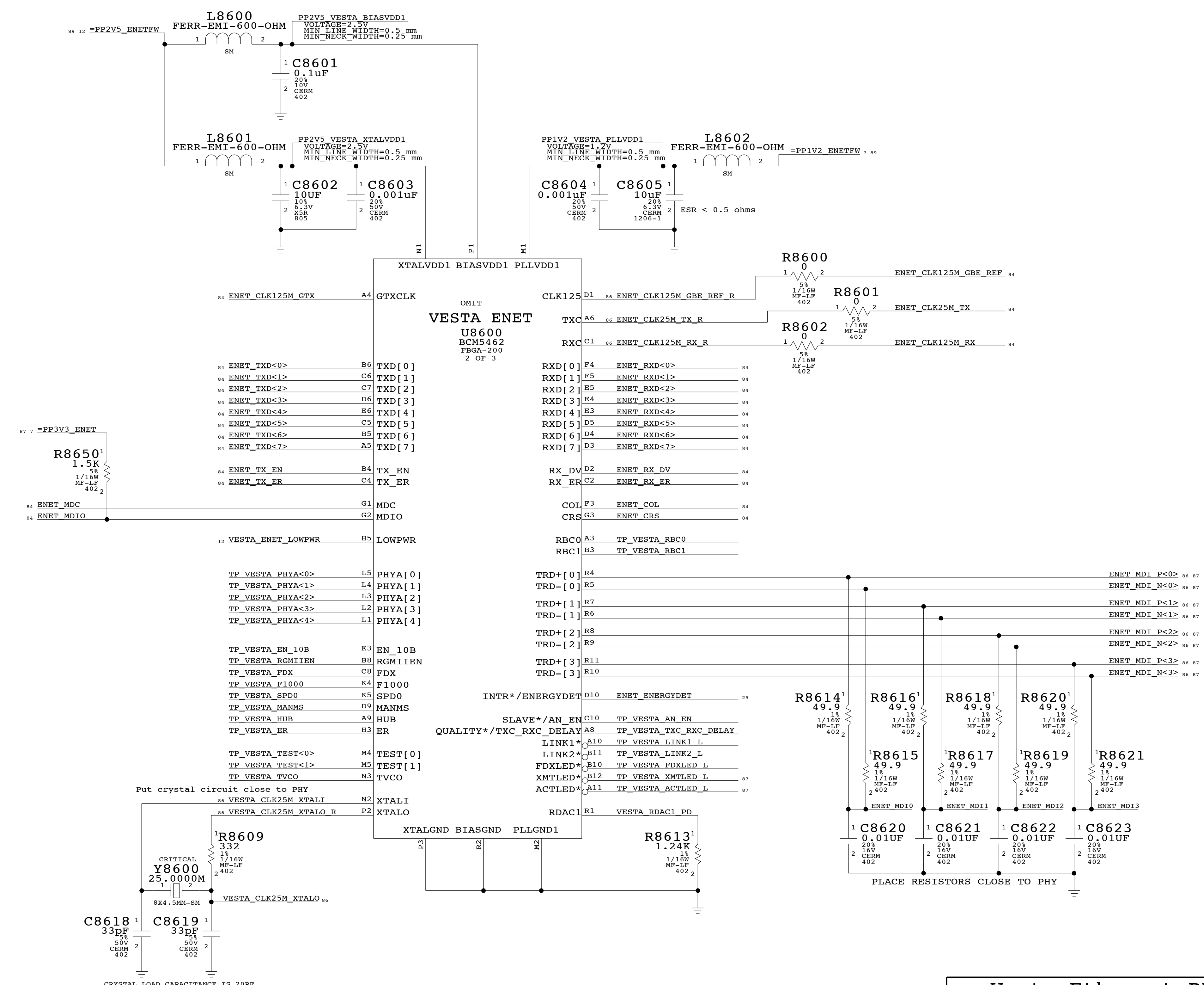
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line:	0.38 mms
Length Tolerance:	50 mils
Primary Max Sep:	5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.



Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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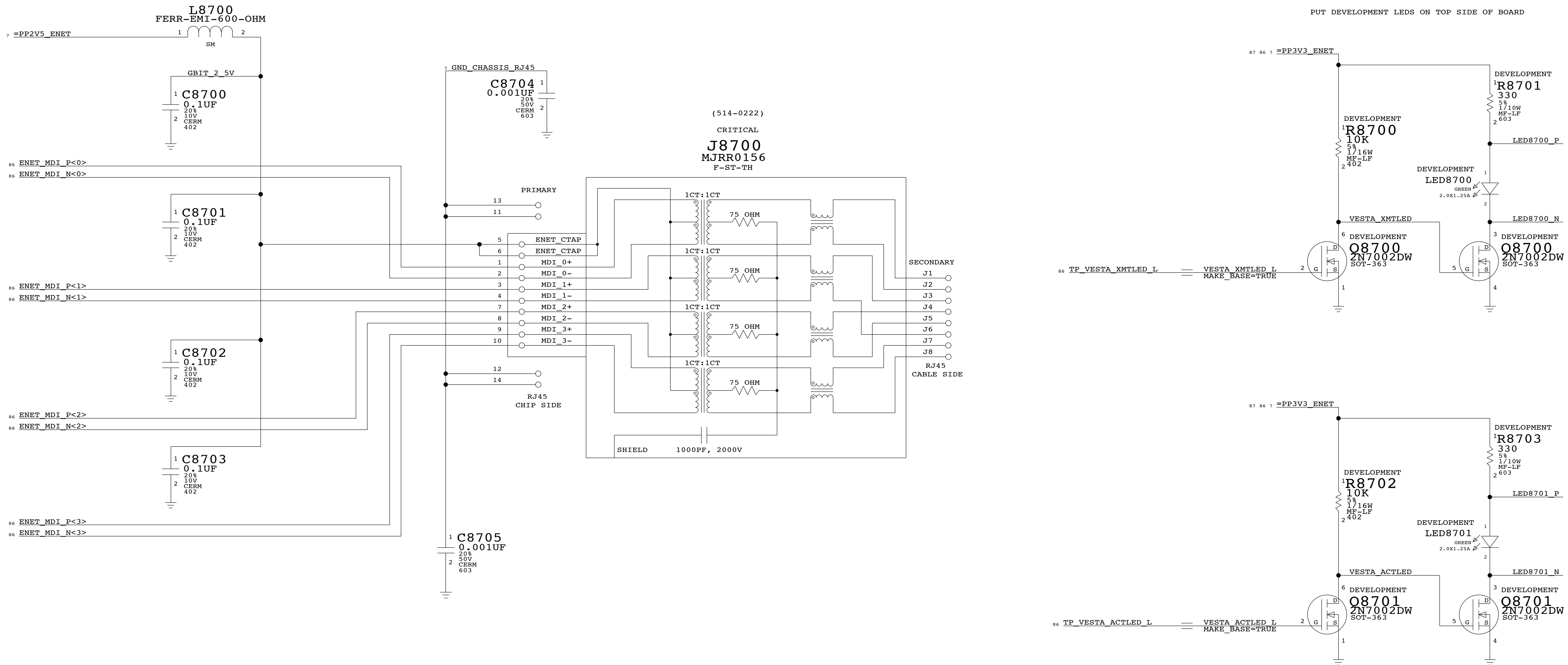

ETHERNET CONNECTOR

SYNC_MASTER=N/A SYNC_DATE=N/A

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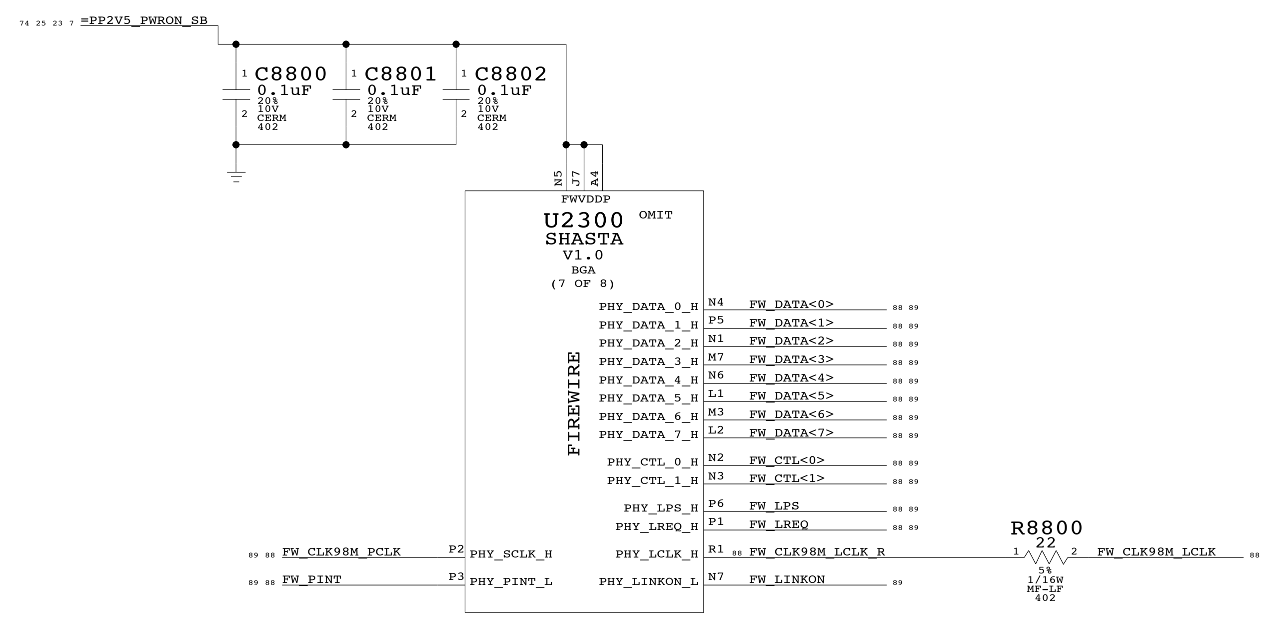
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FW				FW_DATA<7..0>
FW				FW_CTL<1..0>
FW_LPS				FW_LPS
FW_LREQ				FW_LREQ
FW_PINT				FW_PINT
FW_LCLK		P25MM		FW_CLK98M_LCLK
FW_PCLK		P25MM		FW_CLK98M_PCLK
		P25MM		FW_CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Shasta FireWire

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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SCALE NONE SHT 88 OF 102

	ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET	
		NET_TYPE				
I402	(PROVIDED BY LINK PAGE)	P38MM	CLOCKS		FW_CLK98M_PCLK_R	89
I403	FW_TPA1	FW	FW	FW_TPA0	FW_TPA_P<0>	89 90
I405	FW_TPA1	FW	FW	FW_TPA0	FW_TPA_N<0>	89 90
I404	FW_TPB1	FW	FW	FW_TPB0	FW_TPB_P<0>	89 90
I406	FW_TPB1	FW	FW	FW_TPB0	FW_TPB_N<0>	89 90
I407	FW_TPA2	FW	FW	FW_TPA1	FW_TPA_P<1>	89 90
I408	FW_TPA2	FW	FW	FW_TPA1	FW_TPA_N<1>	89 90
I410	FW_TPB2	FW	FW	FW_TPB1	FW_TPB_P<1>	89 90
I409	FW_TPB2	FW	FW	FW_TPB1	FW_TPB_N<1>	89 90
I412	FW_TPA3	FW	FW	FW_TPA2	FW_TPA_P<2>	89 90
I411	FW_TPA3	FW	FW	FW_TPA2	FW_TPA_N<2>	89 90
I414	FW_TPB3	FW	FW	FW_TPB2	FW_TPB_P<2>	89 90
I413	FW_TPB3	FW	FW	FW_TPB2	FW_TPB_N<2>	89 90
I416	VESTA_CLK24M_XTAL	P38MM			VESTA_CLK24M_XTALI	89
I415		P38MM			VESTA_CLK24M_XTALO	89
I417		P38MM			VESTA_CLK24M_XTALO_R	89

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

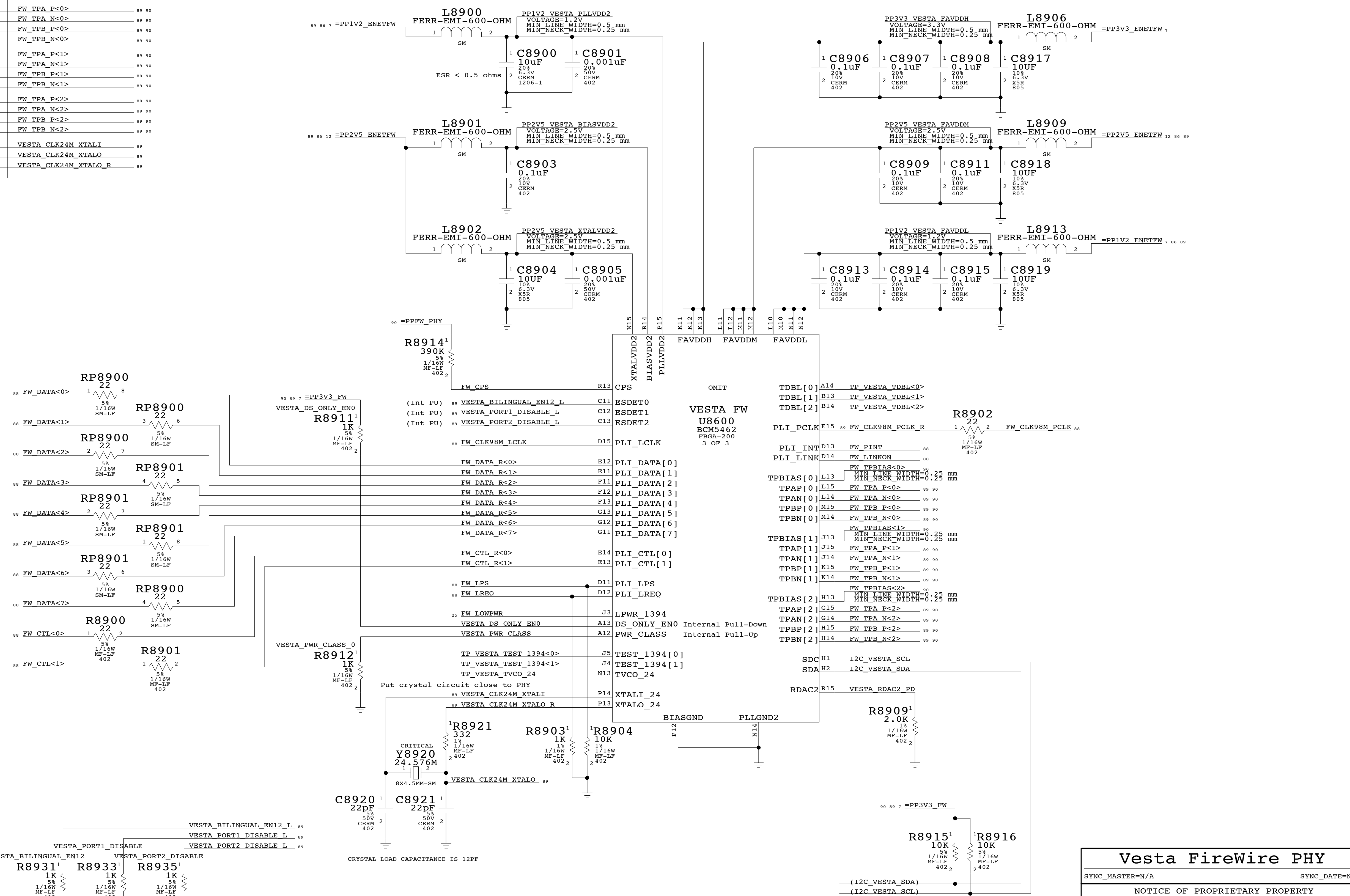
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.



Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

Vesta FireWire PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE D | DRAWING NUMBER 051-6772 | REV. E
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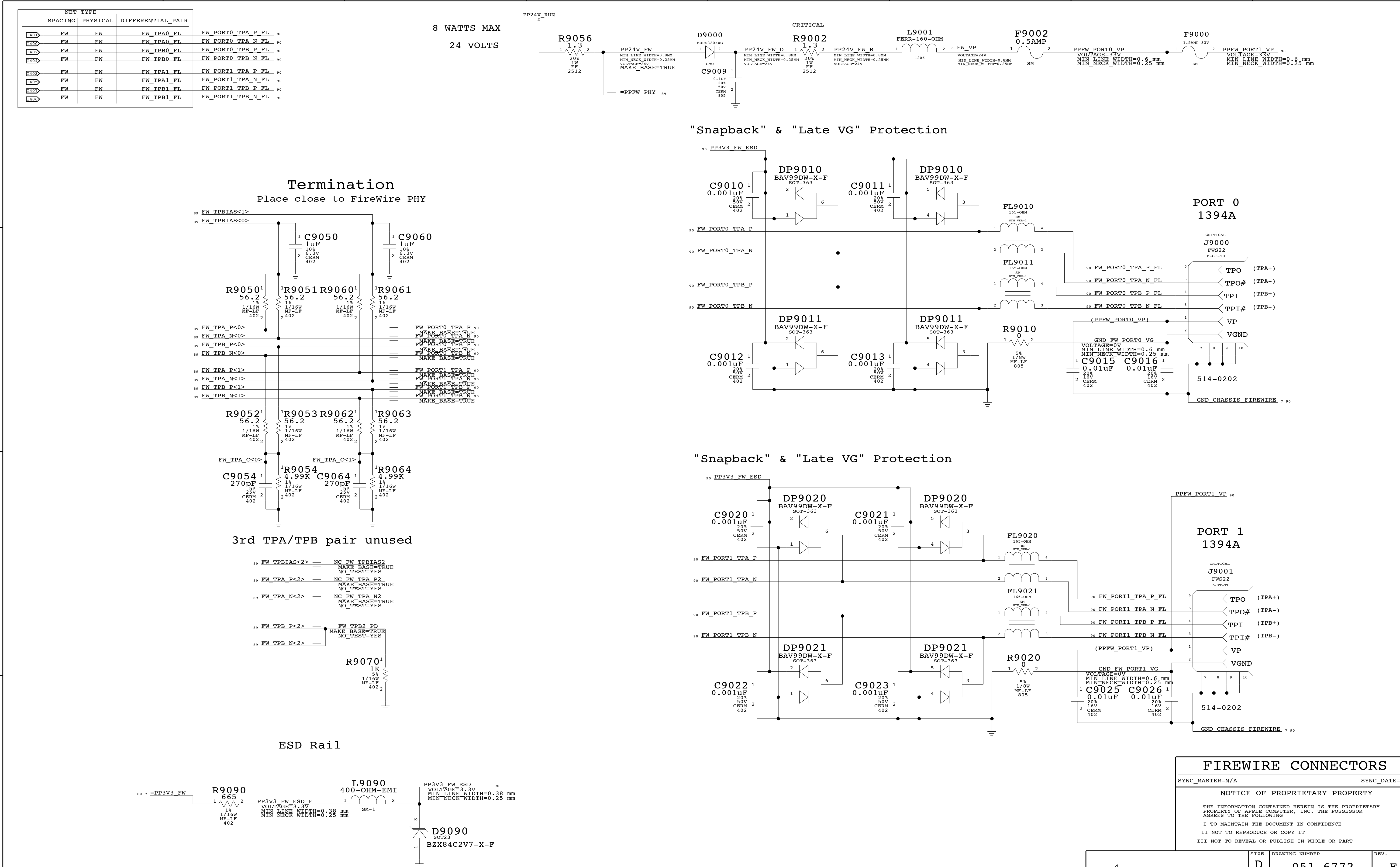

FIREWIRE CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

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ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 91 92
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 91 92
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 76 91
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 76 91
USB2_NEC_XTAL		P25MM		NEC_CLK30M_XT1 91
		P25MM		NEC_CLK30M_XT2 91
		P25MM		NEC_CLK30M_XT2_R 91

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

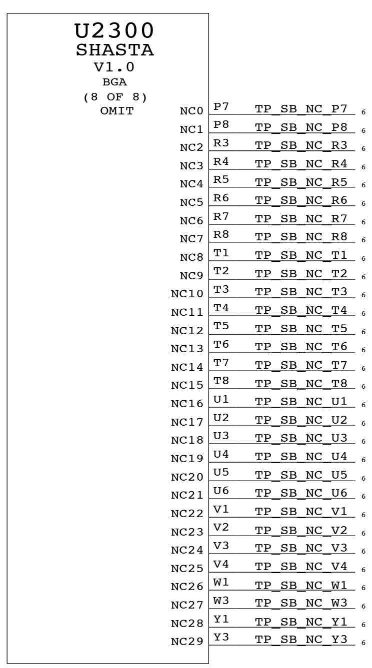
Signal aliases required by this page:
(NONE)

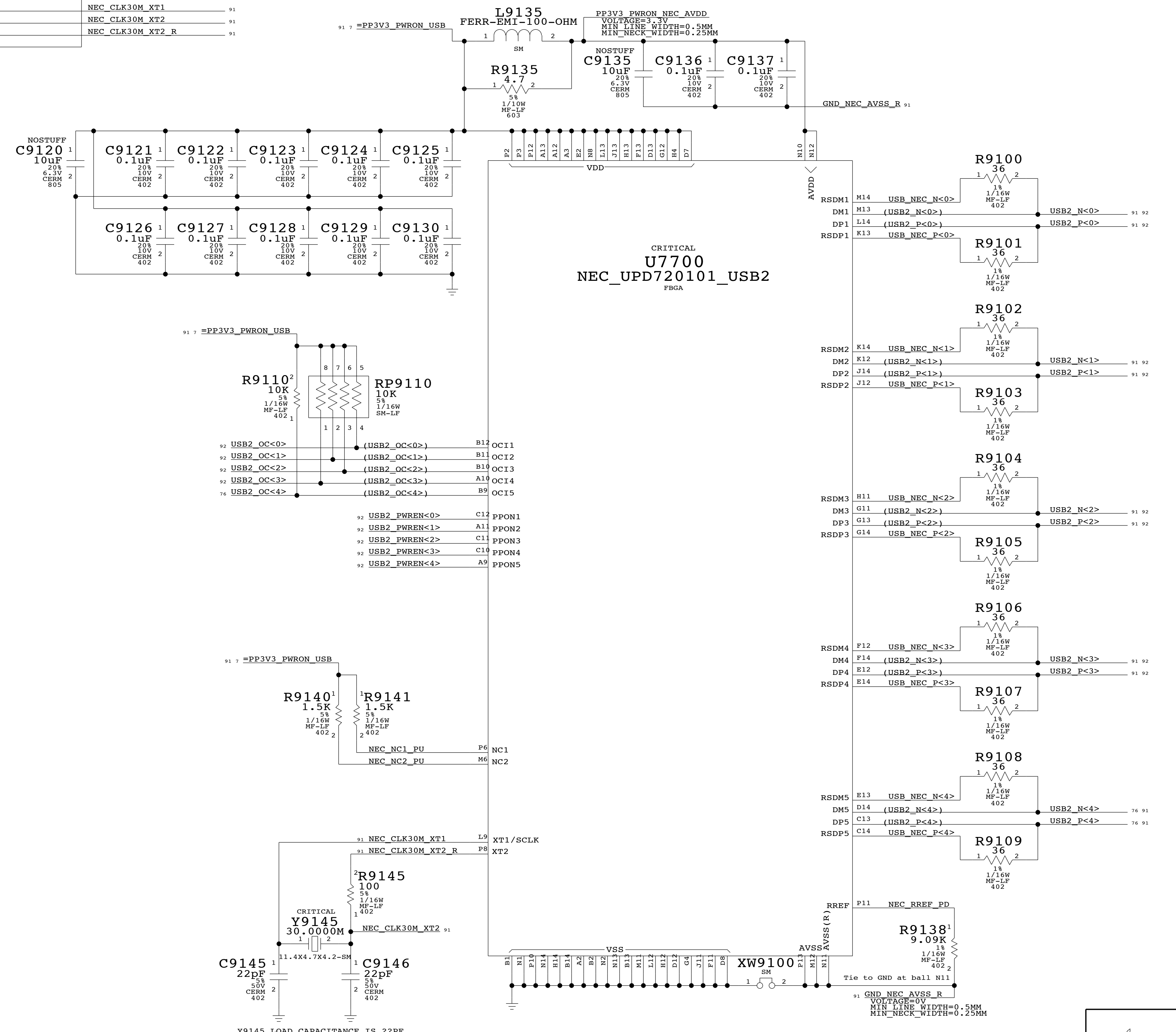
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





USB Host Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F
BY	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F
USB	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F
CONTROLLER	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F

External USB Ports

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

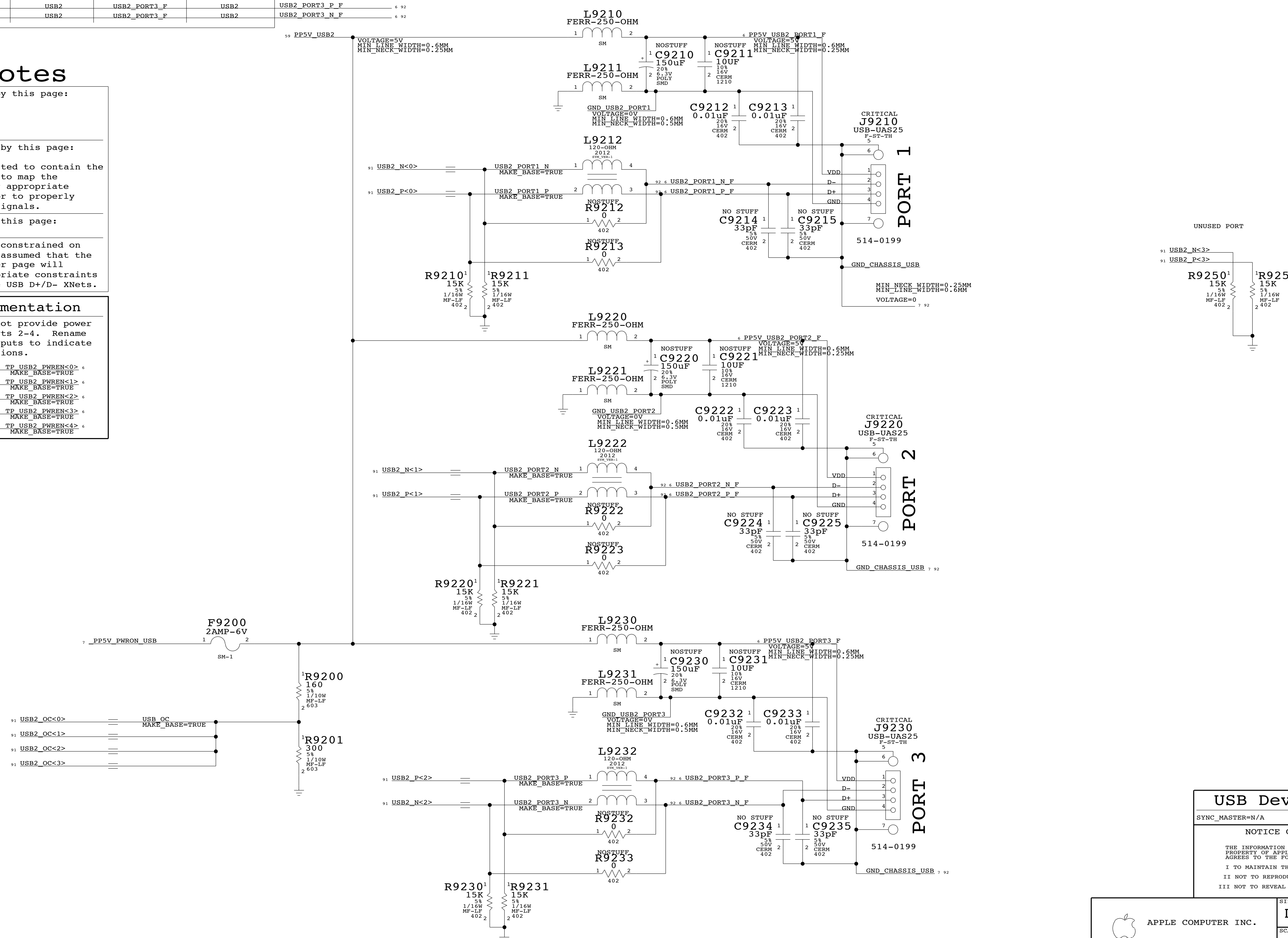
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

USB2_PWREN<0>	TP_USB2_PWREN<0>	MAKE_BASE=TRUE
USB2_PWREN<1>	TP_USB2_PWREN<1>	MAKE_BASE=TRUE
USB2_PWREN<2>	TP_USB2_PWREN<2>	MAKE_BASE=TRUE
USB2_PWREN<3>	TP_USB2_PWREN<3>	MAKE_BASE=TRUE
USB2_PWREN<4>	TP_USB2_PWREN<4>	MAKE_BASE=TRUE



USB Device Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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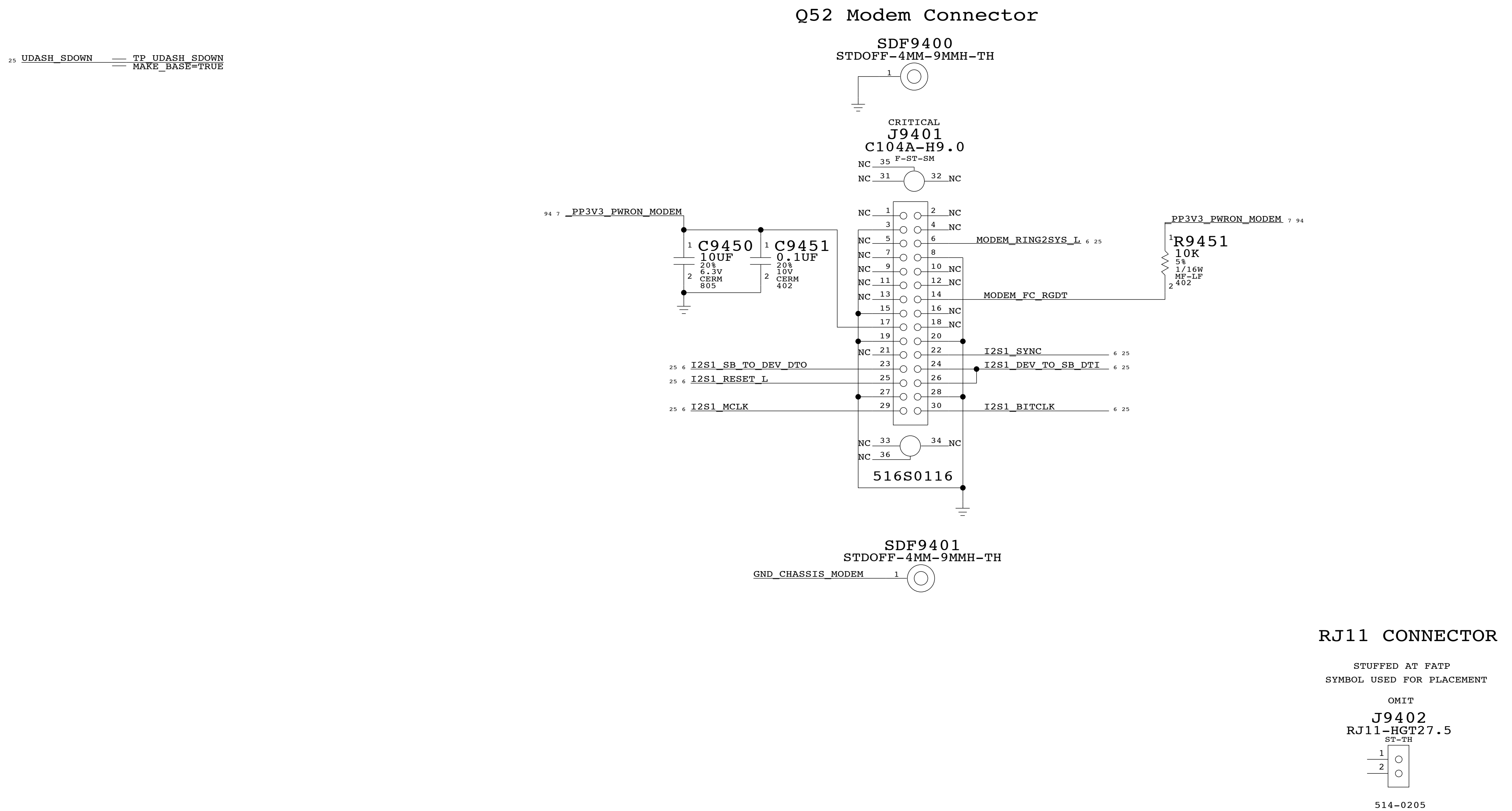
Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

Modem Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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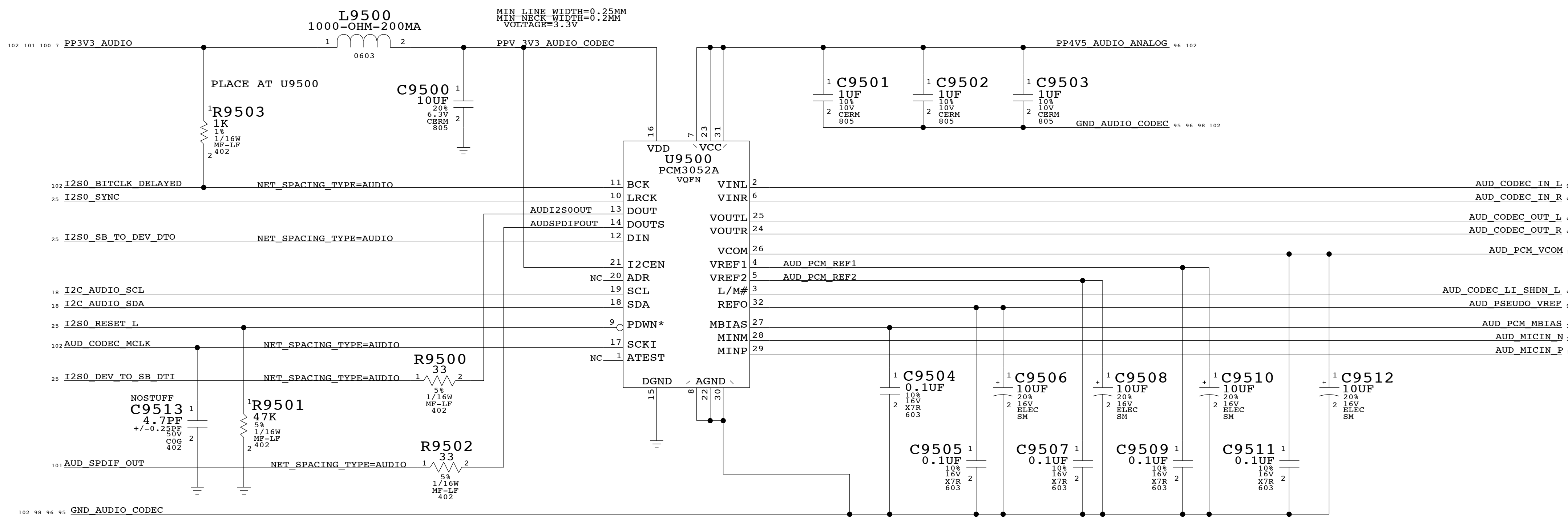
AUDIO CODEC

APPLE P/N 353S0933



AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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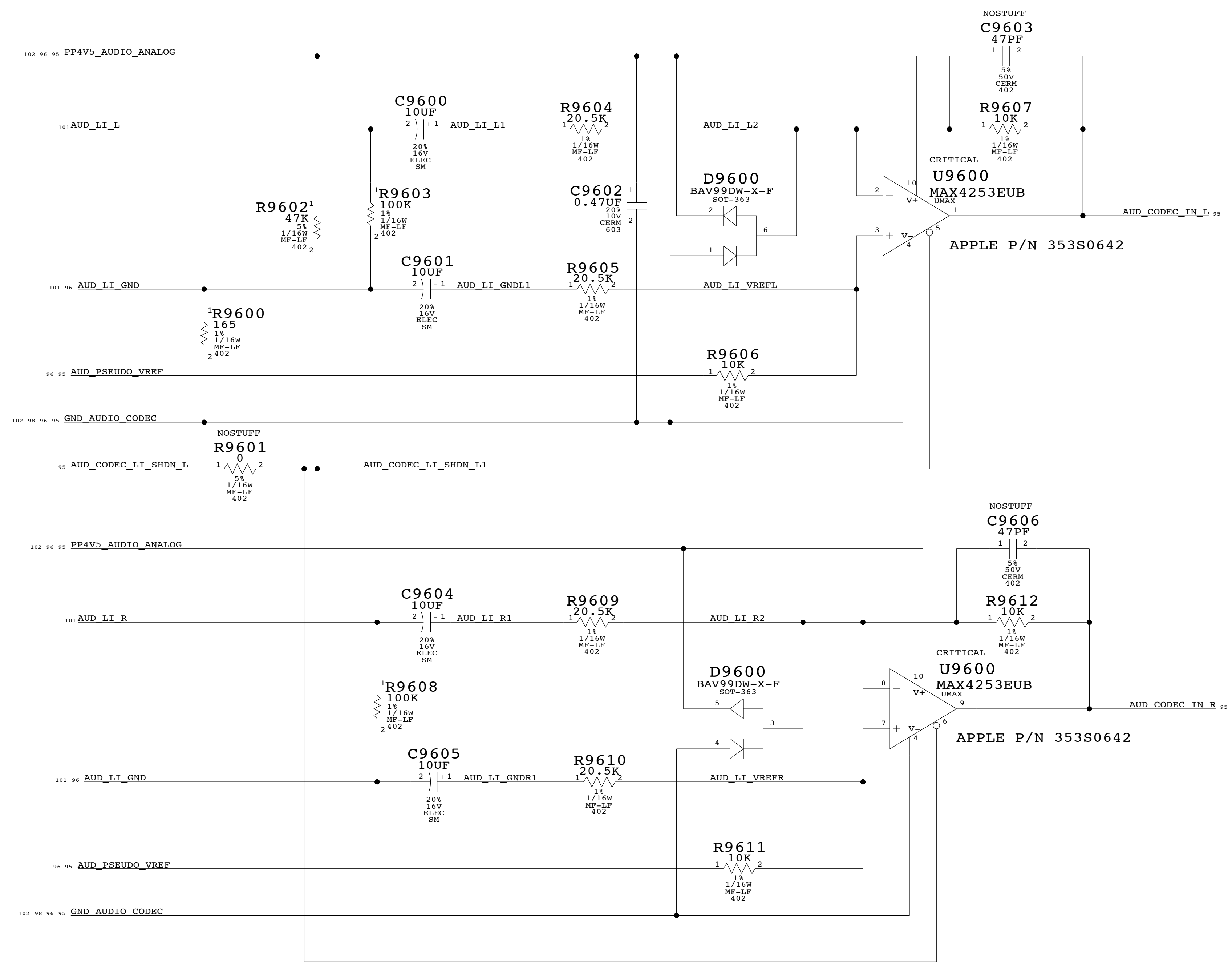
LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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D	051-6772	E
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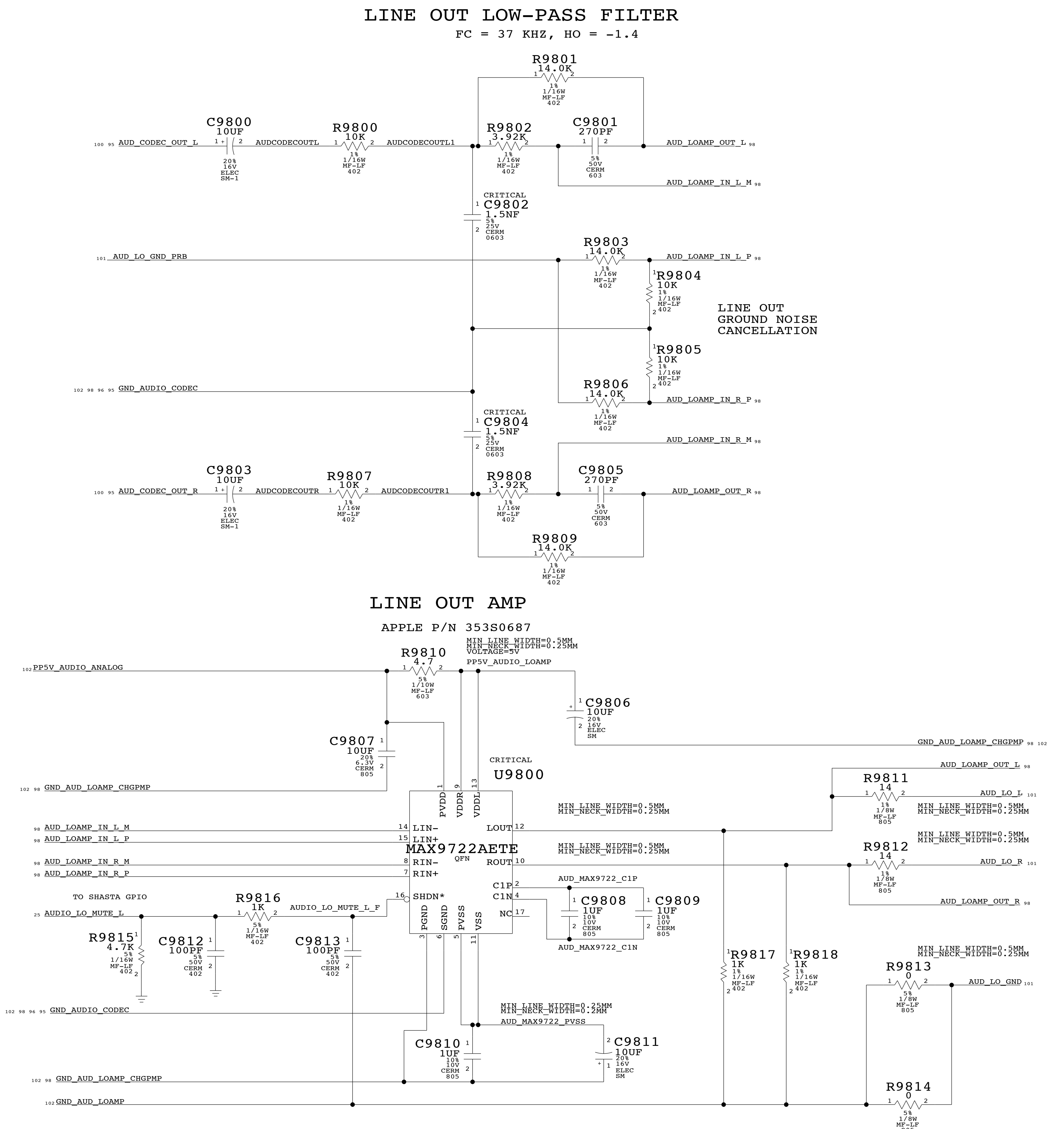

AUDIO: LINE OUT AMP

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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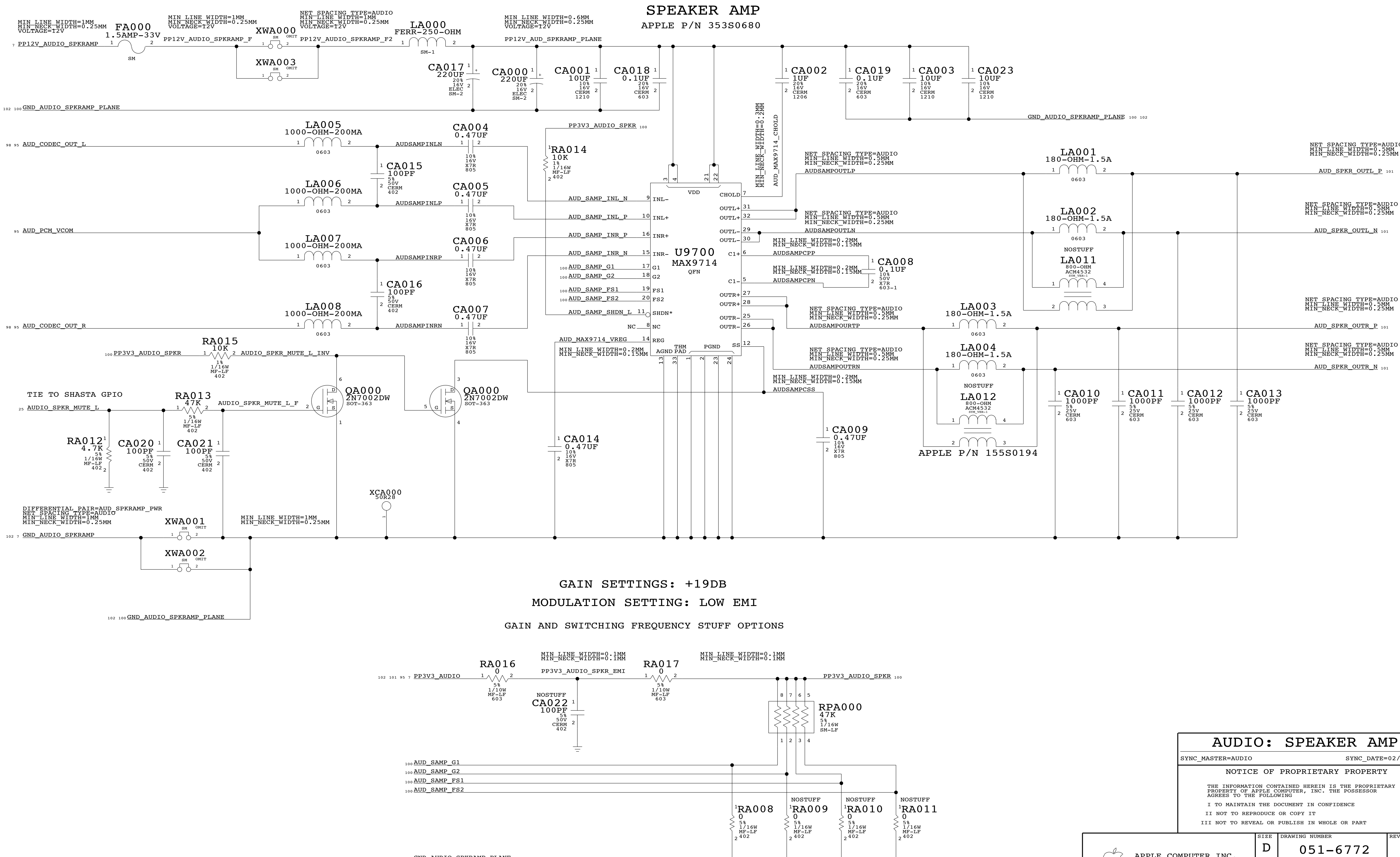

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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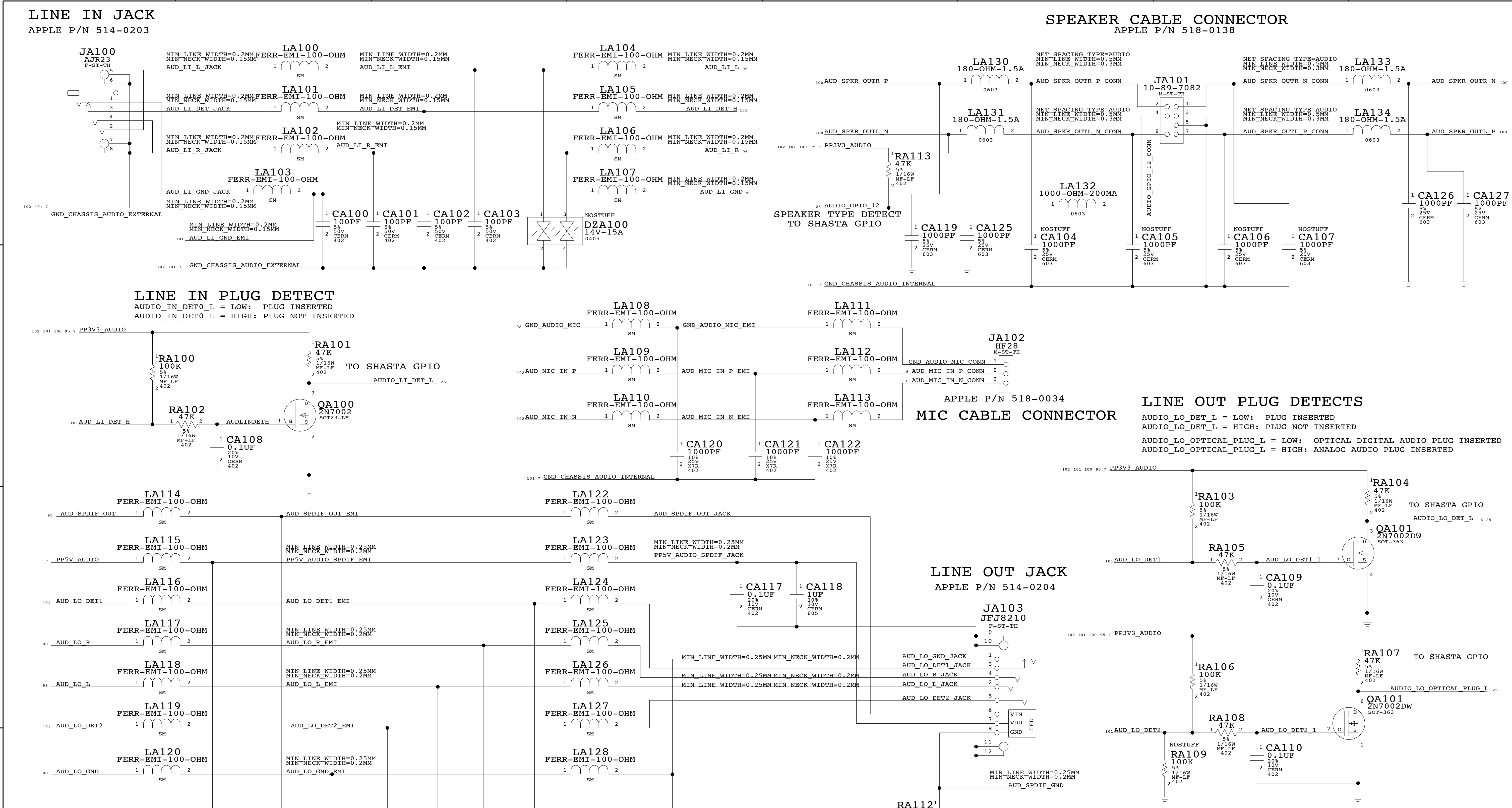

AUDIO: Q45 CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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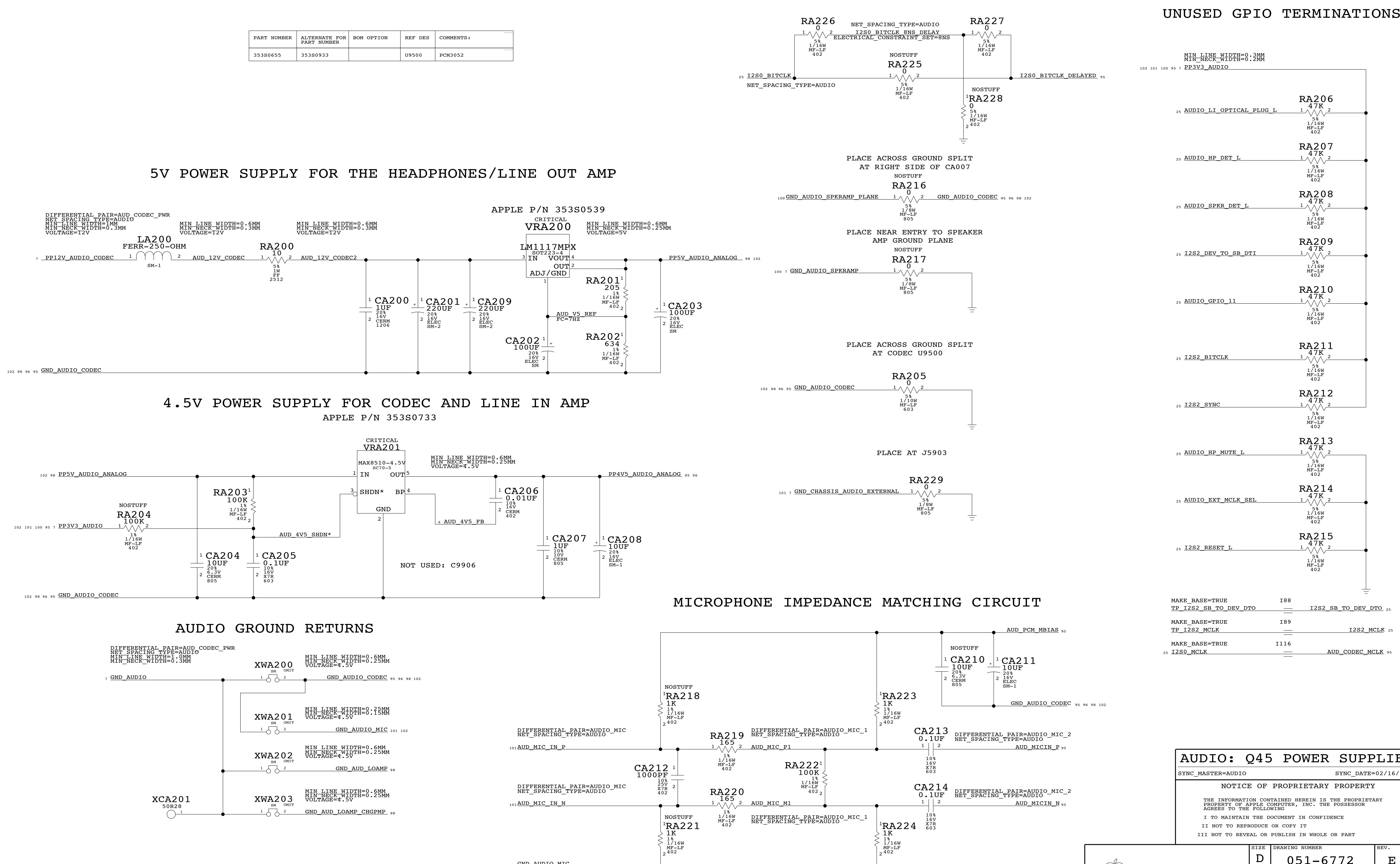
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052



AUDIO: Q45 POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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SCALE	SHT	OF
NONE	102	102