1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,Q45D,SEEDY_U

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		385505	PRODUCTION RELEASED	06/13/05	?

08/03/05

CSA	PDF	CIRCUIT	BLOCK
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3	3	POWER BLOCK DIAGRAM	
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48	40	U3LITE AGP	GRAPHICS
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CSA	PDF	CIRCUIT	BLOCK
51	43	GPU CORE POWER	GRAPHICS
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54	46	GRAPHICS DDR SDRAM A	
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56	48	GPU STRAPS	
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62	52	SHASTA HYPERTRANSPORT	
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86	62	VESTA ETHERNET PHY	
87	63	ETHERNET CONNECTOR	
88	64	SHASTA FIREWIRE	FIREWIRE
89	65	VESTA FIREWIRE PHY	
90	66	FIREWIRE CONNECTORS	
91	67	USB HOST INTERFACE	USB
92	68	USB DEVICE INTERFACE	
94	69	MODEM CONNECTOR	MODEM
95*	70	PCM3052A AUDIO CODEC	AUDIO
96*	71	LINE IN AMP	
98*	72	LINE OUT AMP	
100*	73	SPEAKER AMP	
101*	74	AUDIO CONNECTORS	
102*	75	AUDIO POWER SUPPLIES	

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE
SCHEMATIC,MLB,SEEDY_U

DRAWING NUMBER 051-6772 | REV. E

SHT 1 OF 102

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

U2900
CPU
NEO 10S
PAGE 29

32-BIT
APPLE PI
ELASTIC INTERFACE
1.2V/900MHZ

J5900, J5901
J5902, J5903
17",20" INVERTER
TMDS
EXT VGA
PAGE 59

U1300
SMU
PAGE 13

U1301
RTC
PAGE 13

U5400, U5401
FRAME
BUFFER A
PAGE 54

64-BIT
FRAME BUFFER
2.6V/400MHZ

U4900
GPU
RV351LE
PAGE 49

32-BIT
8X AGP
0.8V/533MHZ
4X = 1.5V
I/O = 1.5V

APPLE PI
PAGE 28

AGP
PAGE 48

U3
U3LITE
CORE
PAGE 22

MAIN MEMORY
PAGE 37

64/128-BIT
MAIN MEMORY
2.6V/400MHZ

SERIES
TERM
PAGE 38

J4000
J4001
DIMMS
PAGE 40

PARALLEL
TERM
PAGES 44&45

64-BIT
FRAME BUFFER
2.6V/400MHZ

U5500, U5501
FRAME
BUFFER B
PAGE 55

MISC
PAGE 24

HYPERTRANSPORT
PAGE 60

8-BIT
HYPERTRANSPORT
1.2V/800MHZ
CONTROL = 2.5V

J9210/J9220/J9230
USB
CONNECTORS
PAGE 92

U2600
PULSAR
POWER
PAGE 26
CLOCKS
PAGE 27

I2C
PAGE 18

J6400
J6401
J6402
HT
DEBUG
PAGE 64

J9240
BLUETOOTH
CONNECTOR
PAGE 92

USB
PAGE 91

U7700
USB 2.0
uPD720101
PCI
PAGE 77

U7500
BOOTROM
PAGE 75

J7600
AIRPORT
EXTREME
CONNECTOR
PAGE 76

HARD DRIVE

JXXXX
SATA
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA1
SATA
PAGE 80

HYPERTRANSPORT
PAGE 62

U2300

PCI
PAGE 74

32-bit PCI (5V-3.3V/33MHz)

J8302
SATA DEV
CONNECTOR
PAGE 83

FOR DEVELOPMENT ONLY

SATA/150
1.2V/1.5GHZ

SATA2

SHASTA

GPIO/PCI164
PAGE 25

J8301
UATA
CONNECTOR
PAGE 83

OPTICAL

UATA/133
3.3V/133MHZ

UATA
PAGE 80

CORE
PAGE 23

NCs
PAGE 91

J9401
CTL-LESS /
SOFT MODEM
CONNECTOR
PAGE 94

ETHERNET
PAGE 84

FIREWIRE
PAGE 88

I2S
PAGE 25
I2S0
SCCA I2S1
SCCB I2S2

GMII (3.3V/125MHz)
8-Bit Tx & 8-Bit Rx

1394 OHCI (3.3V/98MHz)

U9500
AUDIO CODEC
PCM3052A
PAGE 95

S/PDIF

OPTICAL OUT

J9803
COMBO OUT
CONNECTOR
PAGE 98

LINE OUT

LINE OUT
AMP
PAGE 97

SPEAKER
AMP
PAGE 97

J9801
SPEAKER
CONNECTOR
PAGE 98

LINE IN
AMP
PAGE 97

U8600
VESTA
GIG ETHERNET
PAGE 86
FIREWIRE A
PAGE 89
0 1

4 Diff pairs
2 Diff pairs

J8700
ETHERNET
CONNECTOR
PAGE 87

J9000, J9001
FIREWIRE A
CONNECTORS
PAGE 90

J9800
LINE IN
CONNECTOR
PAGE 98

J9802
MIC
CONNECTOR
PAGE 98

SYSTEM BLOCK DIAGRAM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE NONE SHT 2 OF 102

POWER CONNECTOR

J700
PAGE 7

PP24V_RUN — FW CONN, 20" LCD INVERTER
PP12V_RUN — 20" PANEL POWER, 20" LCD INVERTER
PP5V_RUN — HDD & OPTICAL
PP5V_ALL
PP3V3_RUN — PCI BUS, AUDIO CODEC
SYS_POWERUP_L

SMU
SYS_POWERUP_L
POWER SEQUENCE PIN

PULSAR_POWER_DOWN, MAKE_BASE=TRUE → 27 =PULSAR_POWER_DOWN
TP_SMU_PWRSEQ_P1_0, MAKE_BASE=TRUE
16 TURN_ON_PP1V2_PWRON_L

SMU_PWRSEQ_P1_4 13
SMU_PWRSEQ_P1_0 13
SMU_PWRSEQ_P1_1 13
SMU_PWRSEQ_P9_5 13 (PWR_GOOD_SB_CORE)
SMU_PWRSEQ_P9_6 13 (PWR_GOOD_PP2V5)
SMU_PWRSEQ_P1_2 13 (TURN_ON_VTT)

5V

PP5V_RUN_AUDIO LINEAR — PAGE 99 — 5V — HP/LINEOUT AMP
PP4V5_RUN_AUDIO LINEAR — PAGE 99 — 4.5V — AUDIO CODEC
CPU CORE SWITCHER — PAGE 33 — SC2643VX*1 SC1211*4 — 0.8~1.2V — GPUL

=PP5V_RUN_CPU 6 7 8 31 → ALIAS CPU_AVDD_EN 31
PP2V5_RUN_CPU_AVDD LINEAR — PAGE 31 — 2.8V — CPU AVDD
PP5V_PWRON FET SWITCH — PAGE 11 — 5V — USB CONN

PP3V3_ALL LINEAR — PAGE 11 — 3.3V — FW PHY, SMU
PP3V3_PWRON FET SWITCH — PAGE 11 — 3.3V — ENET PHY, USB2 HOST, MODEM & BT
GPU CORE SWITCHER — PAGE 50 — IRU3037ACS — 1.20V — RV351
PP2V5_GPU_A2VDD LINEAR — PAGE 50 — GPU

PP1V2_ALL SWITCHER — PAGE 10 — IRU3037ACS — 1.2V — VESTA CORE

PP1V8_TPVDD LINEAR — PAGE 50 — GPU
PP1V5_VDDC_CT LINEAR — PAGE 50 — GPU

U3LITE CORE SWITCHER — PAGE 22 — IRU3037CS — 1.53V — U3LITE CORE
PP2V5_PWRON SWITCHER — PAGE 9 — IRU3037CS — 2.59V — SHASTA HT, DDR DIMM

PP1V2_PWRON FET SWITCH — PAGE 10 — SHASTA CORE, PWRON_SD, PWRON_DISK_SB
PP1V2_RUN FET SWITCH — PAGE 10 — HT BUS
23 7 6 =PPVCORE_PWRON_SB

PP2V5_PWRON

PP2V5_RUN FET SWITCH — PAGE 9 — RAM TERM, GRAPHIC FB
PP1V8_GPU LINEAR — PAGE 50 — GPU
PP1V25_RAM_VTT LINEAR — PAGE 46 — 1.3V — RAM VTT
PP1V5_PWRON LINEAR — PAGE 50 — 1.5V — PULSAR CORE
PP1V5_RUN POWER SW — PAGE 50 — AGP BUS
46 TURN_ON_VTT

PP3V3_ALL
R331 10K 5% 1/16W MF-LF 402
PWR_GOOD_SB_CORE

11 RAIL_CTL_NEG
R330 100K 5% 1/16W MF-LF 402
COMPARE_SB_CORE
C330 0.01UF 20% 16V CERM 402
U1100 LM339A SOI (V+, GND)

PP5V_ALL
R342 150K 5% 1/16W MF-LF 402
PS_2V_REF
R340 100K 5% 1/16W MF-LF 402
COMPARE_PP2V5
C340 0.01UF 20% 16V CERM 402
R343 100K 5% 1/16W MF-LF 402

PP3V3_ALL
R341 10K 5% 1/16W MF-LF 402
PWR_GOOD_PP2V5

U1100 LM339A SOI (V+, GND)

POWER BLOCK DIAGRAM

SYNC_MASTER=N/A
SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 3 OF 102	

DATE DESCRIPTION

10/20/04 CLONED DESIGN FROM GILA (Q45 A/B) REV G
CHECKIN 00002

10/21/04 ADDED VESTA
ADDED 1.2V REGULATOR FOR VESTA CORE
ADDED 2.5V LDO FOR VESTA
ADDED FW LATE VG PROTECTION
REMOVED BCM5231 ETHERNET PHY
REMOVED FW802A FW PHY
REMOVED FW PORT POWER CIRCUITRY
REMOVED MICRODASH CONNECTOR
CHECKIN 00003

10/22/04 REMOVED NV18/34 GPU
REMOVED AGP VREG (VR5001)
REMOVED GPU VTT VREG
ADDED 2.5V VREG FOR A2VDD
REMOVED EXTERNAL TMDS TRANSMITTER
ADDED RV351LE GPU
CHECKIN 00004

10/26/04 GPU CORE POWER UPDATES
ADDED VESTA ETHERNET LOWPWR CIRCUIT
ADDED DEVELOPMENT LEDS FOR VESTA ENET
CHECKIN 00005

10/28/04 CONNECTED FRAME BUFFER
ADDED 1.8V GPU VREG
CONNECTED GPU TMDS AND VGA
CONNECTED GPU POWER AND POWER FILTERS
CHECKIN 00006

11/01/04 ADDED VOLTAGE, LINE WIDTH, AND NECK WIDTH PROPERTIES FOR GRAPHICS
TIED PPVCORE_NB DIRECTLY TO PP1V5_PWRON (REMOVED R707)
REPLACED EMC FERRITES WITH 0 OHM RESISTORS FOR GRAPHICS AND FANS
REMOVED VESTA CORE REGULATOR
REPURPOSED 1.2V REGULATOR FOR VESTA AND SHASTA
CHANGED FW LATE VG CIRCUITRY TO MATCH Q78 & Q86
CHECKIN 00007

11/03/04 <RADAR 3848831> MOVED SMU RESET BUTTON TO DEVELOPMENT BOM
<RADAR 3849762> MOVED SMU DOWNLOAD CONNECTOR TO DEVELOPMENT BOM
<RADAR 3849798> REDUCED CAPACITANCE OF C1100 & C1102
MASTER PAGE SYNC:
FRAME BUFFER SWAPS FOR CLEANER ROUTING
REMOVED VESTA ROM
AUDIO COST REDUCTIONS <RADAR 3849747 & 3849751>
AUDIO 3052A CODEC
ADDED 1.55V VREG FOR GPU VDDC_CT
MOVED VTT VREG TO 2.5V PWRON TO REDUCE CURRENT THROUGH Q903
CHANGED FETS IN GPU CORE FOR COST REDUCTION
ADDED SPACING & PHYSICAL CONSTRAINTS TO FRAME BUFFER
CHECKIN 00008

11/04/04 REMOVED 1.6GHZ PROCESSORS
CHANGED VOLTAGE SETTING OF 2.5V VREG TO 2.588V FROM 2.62V
1.2V VREG COST REDUCTIONS - Q1002 TO NTD60N02R; C1002/3 TO 10UF CERM
U2850 - REMOVED MAXIM AS AN ALTERNATE
MOVED GPU ZENER DIODES TO VREG PAGE SINCE THEY SHOULD BE PLACED NEAR THE VREGS
ADDED 8MX32 GRAPHICS MEMORY
ADDED GIGABIT ETHERNET CONNECTOR
CHECKIN 00009

11/06/04 ADDED GPU STRAPS
CONNECTED GPU GPIOS
REMOVED ON BOARD POWER SUPPLY TEMP SENSOR
ADDED AMBIENT LIGHT SENSOR CONNECTOR
CONNECTED GPU TEMP SENSOR
REMOVED CPU VREG 4TH PHASE
ADDED DEVELOPMENT LEDS TO REGULATORS
CHECKIN 00010

11/07/04 ADDED MORE GPU CONSTRAINTS
<RADAR 3616348, 3621390> CHANGED FL5900-2 TO 220 OHM
<RADAR 3848846> 2.5V RUN FET COST REDUCTION
<RADAR 3848859> 1.2V, 1.5V RUN FET COST REDUCTIONS
<RADAR 3848887> 5V & 3.3V PWRON FET COST REDUCTIONS
<RADAR 3849622> STUFFED AROUND TMDS FILTERS
<RADAR 3849656> STUFFED AROUND RGB FILTERS
<RADAR 3849806> CHEAPER SMU CRYSTAL
<RADAR 3849857> CHEAPER USB2 CRYSTAL
BOM RELEASE REV 01

11/08/04 FRAME BUFFER PIN SWAPS
<RADAR 3848846> UPDATE OF 2.5V RUN FET COST REDUCTION
<RADAR 3849743> ADDED RESISTORS TO STUFF AROUND USB FILTERS
CHECKIN 01001

11/09/04 <RADAR 3848850> REGULATOR COST REDUCTIONS
<RADAR 3849767> 2.5V VREG COST REDUCTIONS
<RADAR 3849772> REMOVED OUTPUT CAP ON 1.2V_ALL VREG
<RADAR 3849820> SHASTA FILTER COST REDUCTION
<RADAR 3849854> GPU CORE VREG COST REDUCTION
<RADAR 3865344> SET GPU VDDC_CT VREG TO 1.55V
CHECKIN 01002

11/10/04 CHANGED SOURCE OF Q1003 TO PP1V2_ALL
RGB TERMINATION NOW CONNECTED TO DIGITAL GROUND
WHITE LED - CHANGED INDUCTORS TO 0 OHM RESISTORS
UPDATED POWER BLOCK DIAGRAM
CHECKIN 01003
<RADAR 3848850> 2.5V VREG COST REDUCTION
CHECKIN 01004

11/15/04 ADDED REGULATOR FOR GPU TPVDD
ADDED POWER SEQUENCING FOR GRAPHICS REGULATORS
ADDED TEST POINTS TO GRAPHICS FOR EXOR TESTING
REMOVED EXTERNAL S/PDIF TRANSMITTER
CHECKIN 01005

11/16/04 REMOVED P50 AIRPORT AND Q23 BLUETOOTH CONNECTORS, HOLES, & STANDOFFS
ADDED Q85 AIRPORT & BLUETOOTH CONNECTOR
CHECKIN 01006
(PP 16,17) REPLACED FAN CONTROL WITH NEW CIRCUIT
(P 76) FINISHED CONNECTING Q85 CONNECTOR
(P 7) ADDED PLATED HOLE ZH710 FOR TMDS GROUNDING
(P 7) TIED BOTH EI RAILS TO 1.5V
(P 5) NEW BOOTROM P/N
(P 9) ADDED EXTRA 10UF INPUT CAP
(P 12) VESTA_ENET_LOWPWR UPDATE
(P 18) <RADAR 3878118> MOVED SMU I2C E BUS
(P 22) CHANGED Q2250 TO 376S0143
(P 46) SLEEP SIGNAL TURNS OFF VTT VREG
(P 58) REPLACED THERMAL SENSOR WITH LM63
(P 59) TIED UNUSED BUFFER ENABLE PINS HIGH
(P 90) FIXED FW PORT NAMING
(P 90) CHANGED R9090 TO 665 OHM
(P 91) CHANGED USB2 CHIP GROUNDING
(P 8) ALIASED VESTA JTAG TO TEST POINT NETS
(P 9) <RADAR 3848846> ADDED PAD FOR 1NF CAP TO GATE OF Q903
CHECKIN 01007 / BOM RELEASE REV 02

11/18/04 ADDED PHYSICAL CONSTRAINTS
AUDIO STUFFING CHANGES
CHECKIN 02001

11/20/04 (P 36) CONNECTED NEW CPU DIODE REFERENCE
(P 77) USB2 IDESEL - NOW FROM USB2 SIDE
(P 56) ADDED BOMOPTIONS FOR MEMORY STRAPS
(PP 56, 58) CONNECTED PWM FROM RV351LEP & PUT IN PROTO WORKAROUND
(P 25) <RADAR 3849835> NEW SHASTA XTAL
(P 62) <RADAR 3849855> SHASTA HT_PLL FILTER COST REDUCTION
(P 91) <RADAR 3849858> USB CAP COST REDUCTION
(P 76) ADDED STANDOFFS FOR Q85 CARD
(PP 16,17) NEW FAN CIRCUIT CAPS (C1603, C1653, C1703)
(P 50) <RADAR 3865344> VDDC_CT SET TO 1.50V
(P 50) <RADAR 3877855> TP_VDD SET TO 1.80V
(P 12) VESTA_ENET_LOWPWR UPDATE
(PP 10, 22, 34, 50) USED COMPARATOR FOR LOW VOLTAGE RAIL LEDS
CHECKIN 02002

11/22/04 (P 49) CONNECTED AGPTEST RESISTOR TO VDDP
(P 56) ADDED PADS FOR STRAPPING RESISTORS TO GPU_GPIO<14>
(P 58) ADDED CONSTRAINT SETS
(P 59) STUFFED AROUND Q5900 PANEL PWR SEQUENCING
(P 59) LED 3 NOW DRIVEN FROM FPD_PWR_ON
(P 3) CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING
(P 76) FIXED PCI_CBE_L<1> CONNECTION
MORE PHYSICAL & SPACING UPDATES
(P 83) <RADAR 3890225> OPTICAL DRIVE CONNECTOR CHANGED TO 516S0235
CHECKIN 02003
(P 56) ADDED OPTION OF USING PWM FROM SHASTA
<RADAR 3849718, 3849767, 3849854> MADE ON & VISHAY FETS ALTERNATES
(P5) ADDED U3L W/ NEW LAMINATE AS ALTERNATE
(P 16) C1653 - REPLACED WITH LOWER HEIGHT CAP
CHECKIN 02004

11/23/04 (P 76) TABLED IN NEW STANDOFFS FOR Q85 CARD
PROTO RELEASE (REV 3)

12/02/04 (P 90) FIXED ALIAS PROBLEM WITH FW_TPB2_PD
(P 90) FIXED FW_CPS SHORT
(P 35) REMOVED DS3500 & DS3501
(P 83) REMOVED SECOND SATA CONNECTOR
CHECKIN 03001
CONVERTED DISCRETES TO LEAD FREE
CHECKIN 03002

12/07/04 CHANGED U7700 BACK TO LEADED PART
(P 5) REMOVED ORIGINAL U3LITE (NEW LAMINATE ONLY FOR C/D)
(P 49) CHANGED GPU TO RV351LEP (338S0231)
(P 76) NOW HAVE CORRECT SYMBOL FOR STANDOFFS
(P 76) J7650 - NEW TO ALLOW 5MM CONNECTED HEIGHT
BOM RELEASE REV 04

12/09/04 CHANGED ALIASES TO SYNONYMS
CHANGED LINE AND NECK WIDTHS TO METRTIC
CHECKIN 04001

12/13/04 ADDED 2.0 GHZ AND ADDITIONAL 1.8 GHZ ALTERNATE PROCESSORS
VESTA XTAL: R5815=249, R8609=332, R8921=332
VESTA ENET: R1262=10K, C1260=10U, R1251=NO STUFF, C1250=2.2U
FANS: NO STUFF DZ1601, DZ1651, DZ1701
STUFFED R1604, R1654, R1704
CHECKIN 04002

12/14/04 2.5 V REGULATOR - NEW NARROWER OUTPUT CAPS (C908, C909)
(P 46) REMOVED SEMTECH REGULATOR, ADDED RICHTEK AS ALTERNATE VTT
(P 16) CHANGED FAN1 OUTPUT CAP BACK TO THROUGH-HOLE
(P 59) SWAPPED INVERTER CONNECTOR GENDER
CHECKIN 04003
(P 46) RICHTEK VTT UPDATES
BOM RELEASE REV 5

12/15/04 (P 6) ADDED NO_TESET PROPERTIES
(P 12) VESTA ENET LOW POWER FIX
CHECKIN 05001

12/16/04 FIXED I2C_TMDS_SDA/SCL ON P 6
(P 46) NOSTUFF RICHTEK VTT VREG
(P 59) STUFFED TMDS CHOKES
(P 56) USING PWM FROM ATI GPU
(P 38) FIXED MIN_NECK_WIDTH ON TD1 AND TD2
(P 92) ADDED NET_PHYSICAL_TYPE = USB2 TO TABLE
(P 7) ADDED BATTERY SAFETY BYPASS OPTION (NOSTUFF)
CHECKIN 05002
(P 50) ADDED Q5000 TO INPUT OF GPU VCORE VREG
(P 6) REMOVED SOME FUNC_TEST PROPERTIES
(P 50) GPU_VDCC_CT POWER SEQUENCING
CHECKIN 05003

12/17/04 (P 6) ADDED/REMOVED MORE FUNC_TEST PROPERTIES
CHECKIN 05004
(P 50) GPU POWER SEQUENCING
CHECKIN 05005

12/20/04 MINOR TEXT/COMMENT CHANGES
EVT RELEASE (REV 6)

01/11/05 (P 5) REMOVED BRA FROM PROCESSOR TABLE, REPLACED BPA WITH BNA
(P 5) NEW SMU PART NUMBER

01/18/05 CHANGED SDF7601 TO PART 860-0567
BOM RELEASE REV 7

01/25/05 (P 5) CORRECTED 1.8GHZ CPU APPLE P/N FROM 337S2969 TO 337S2998
(P 12) NOSTUFF Q1250 TO DISCONNECT ENETFW_RESET FROM SHASTA GPIO
(P 5) CORRECTED SMU PART NUMBER TO 341T1703
(P 16, 17) HAROLD'S FAN CIRCUIT CHANGES
CHECKIN 07002

01/27/05 (P 25) REPLACED R2566 WITH 0 OHM TO ELIMINATE FW_LOWPWR GLITCH
ADDED 0 OHM (R2570, NOSTUFF) TO BREAK FW_LOWPWR FROM SHASTA
(P 56) STUFF R5610 TO PULL DOWN ATI_PWM SIGNAL TO ELIMINATE GLITCH
(P 27-29) CONNECTED CPU_APSYNC FROM U3LITE AND DISCONNECTED FROM PULSAR
NO STUFF: R2768,R2772,R2805,R2910
STUFF: R2806,R2911
(P 11) CHANGED C1102 TO 16V FOR SUPPLY AND COST ISSUES
(P 5) ADDED KQA (337S3093) TO ALTERNATE PROCESSOR TABLE
CHECKIN 07003
(P 5) MODIFIED PROCESSOR TABLE TO MATCH IBM'S TABLE, AGAIN.
BOM RELEASE REV 8

02/01/05 (P 75) BOOTROM REFLASHING ISSUE FIX: CHANGED R7502 TO 470 OHM
(P 12) ADDED A CLAMP CIRCUIT FOR ENET_LOWPWR GLITCH
(P 10,22) SHASTA & U3LITE VCORE IMPROVEMENT: STUFF C1005 & C2205 WITH 2200PF
(P 13) CHANGED U1301 TO LEADED PART (353S0653) DUE TO SUPPLY
(P 5) ADDED 34S0284 AND 34S0282 AS U3LITE ALTERNATES (OLD LAM)
BOM RELEASE REV 9

02/03/05 (P 28) CHANGED APSYNC SERIES TERMINATION R2806 TO 10 OHM
(P 5) ADDED LEAD FREE PARTS AS ALTERNATE FOR U1301 & VRA201 DUE TO SUPPLY
(P 8) REMOVED SMU DOWNLOAD CONNECTOR FROM DEVELOPMENT BOM
(P 92) STUFFED USB COMMON MODE CHOKES FOR EMC
CHECKIN 09002

02/04/05 (P 50) <RADAR 3919121> NOSTUFF U5090 AND RELATED COMPONENTS
STUFFED R5092 FOR 1.5V GPU VDCC_CT

02/08/05 (P 7) REMOVED ZH701
(P 12) STUFF R1251, CHANGE C1250 TO 10UF, R1262=100K TO LENGTHEN
VESTA RESET AND LOWPWR DELAY
(P 59) <RADAR 3849662> STUFFED PANEL POWER SEQUENCING FOR BOTH 17 AND 20 INCH
CHECKIN 09003
(P 92) <RADAR 3742725> CHANGED USB COMMON MODE CHOKES TO 120-OHM 155S0232
(P 59) NOSTUFF R5950, STUFF R5923 FOR 17 INCH PANEL POWER FROM PP3V3_RUN

02/09/05 CHECKIN 09004

02/10/05 (P 59) <RADAR 3919083> CHANGED R5971 AND R5972 TO 33 OHMS
(P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: U5600, U5601
NOSTUFF: R5609, R5621
DVT RELEASE (REV 10)
(P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: C5600, C5601

02/15/05 (P 12) CHANGED C1250 TO 6.3V PART, TO MATCH A PART ALREADY ON THE BOM
(P 5) ADDED 353S0687 (LEADED) AS ALTERNATE FOR 353S0959 (LEAD FREE) U9800

02/16/05 ADDED PAGE TITLE PROPERTIES FOR SCHEMATIC REUSE WITH M23/M33

02/17/05 (P 12) YET ANOTHER VESTA RESET/LOWPWR STUFFING CHANGE
(P 16,17,36) ADDED SIGNAL ALIASES FOR SCHEMATIC REUSE WITH M23
(P 50) RE-STUFFED GPU 1.5V VDCC_CT BECAUSE OF LEAKAGE WORRIES
BOM RELEASE REV 11

03/07/05 (P 12) MADE CONNECTION FOR VESTA RESET FINAL FOR PVT
(P 49) STUFFED 470 OHMS FOR R4912 TO AVOID PCI_RESET GLITCH FROM GPU
(P 50) ADDED FET TO SPLIT 3.3V POWER TO GPU I/O
(P 59) HACK FOR PANEL POWER SEQ.OPTION FROM SYS_SLEEP
(P 6, 58) ADDED TEST POINTS FOR NEC AND ATI
CHECKIN 11002 (03/11)

03/17/05 (P 50, 59) FINALIZED STUFFING OPTIONS FOR ATI POWER SEQUENCE HACK
BOM RELEASE REV 12, CHECKIN 12001

03/21/05 (P 8,12,89) CHANGED VESTA STRAP PULL UP/DOWN RES TO 1K PER BROADCOM
(P 13) RELOADED Y1300 DUE TO LIBRARY CHANGE
BOM RELEASE REV 13

03/22/05 (P 16) REMOVED OPTICAL TEMP SENSOR (U1602) FOR BETTER I2C BUS ROUTING
CHECKIN 13001

03/24/05 (P 5) ADDED LEADED ALTERNATE FOR VRA200, LM1117
(P 10,80) ADDED CAPS ON 1.2V RAIL TO REDUCE SATA POWER NOISE
CHECKIN 13002

03/25/05 (P 80) CHANGED CAPS TO 1UF, REMOVED 10UF THAT WOULD NOT FIT
(P 10) CHANGED R1003 TO 5.62K TO RAISE 1.2V REGULATOR TO 1.25
(P 6) ADDED NO_TEST PROPERTIES ON UNUSED SATA2 NETS
(P 50) CHANGED R5091 TO 61.9K TO INCREASE VDCC_CT TO ABOUT 1.54V
BOM RELEASE REV14, CHECKIN 14001

03/28/05 PVT RELEASE (REV A)

04/06/05 (P 25,62) RESTUFFED C2500,C2520,C2530,C6200,C6210 FOR SHASTA POWER DECOUPLING
PVT RELEASE 2 (REV B)

04/22/05 (P 5) ADDED BPL, BRL, AND BNA PROCESSORS TO TABLE
(P 50) CHANGED R5091 TO 56.2K TO INCREASE VDCC_CT TO ABOUT 1.65V
REV C RELEASE

04/25/05 (P 50) STUFFED R5020 0-OHM TO HELP ICT

06/07/05 (P 54,55) CHANGED HYNIX FRAME BUFFER TO 333S0341 (NEW HYNIX SCREEN, SAME PART)

06/13/05 (P 6) ADDED 338S0263 AS ALTERNATE FOR U4900 (RV351 GPU WITH EUTECTIC BUMPING)
REV E RELEASE

E

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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PROCESSORS

QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3055	1	PROCESSOR	FBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,KPA	2.0GHZ	1.20V	42W	?	U2900	CPU_2_0GHZ
337S3060	1	PROCESSOR	FBGA-576-1MM	IC,GPUL,DD3.1,1.8G,85C,JPA	1.8GHZ	1.20V	42W	?	U2900	CPU_1_8GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3061	337S3060	CPU_1_8GHZ	U2900	IC,DD3.1,1.8G,JRA	1.25V
337S2969	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BPA	1.20V
337S2970	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BRA	1.25V
337S2981	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BPL	1.20V
337S2982	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BRL	1.25V
337S2998	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BNA	1.20V
337S3093	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KQA	1.15V
337S3056	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KRA	1.25V
337S3058	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CPA	1.20V
337S3059	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CRA	1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0320	1	IC,U3LITE,NEW LAM,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0321	343S0320		U3	U3L,NEW LAM,200MM
343S0284	343S0320		U3	U3L,OLD LAM,300MM
343S0282	343S0320		U3	U3L,OLD LAM,200MM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0324	1	IC,ASIC,VESTA,V1.3	U8600	

MISC PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
	062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
	820-1747	1	PCB,FAB,MLB	MLB1	
	825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
	051-6772	1	PCB,SCHEM,MLB	SCH1	
	341T1667	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
	341T1703	1	IC,SMU,Q45C/D	U1300	
CRITICAL	603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL	603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702,LED5900	KINGBRIGHT LED
376S0204	376S0130		Q3310,Q3320,Q3410	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q3311,Q3321,Q3411	MOSFET,N-CH,VISHAY
353S0960	353S0733		VRA201	MAX8510,L-F PART
353S0958	353S0653		U1301	DS1338, L-F PART
353S0687	353S0959		U9800	MAX9722 LEAD
353S0539	353S0898		VRA200	LM1117 LEAD
338S0263	338S0231		U4900	RV351 GPU EUTECTIC

TABLE ITEMS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV E

SCALE NONE | SHT 5 OF 102

E30	NO_TEST=YES	TP_FBBCS1_L	52
E29	NO_TEST=YES	AGP_CLK66M_GPU_R	27
E28	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
E26	NO_TEST=YES	AUD_4V5_FB	102
E25	NO_TEST=YES	CPU_HTBEN_R	27
E24	NO_TEST=YES	EI_CPU_SYNC_R	27
E23	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
E22	NO_TEST=YES	EI_NB_SYNC_R	27
E21	NO_TEST=YES	ERROR_LED	8
E20	NO_TEST=YES	HT_CLK66M_NB_R	27
E19	NO_TEST=YES	HT_CLK66M_SB_R	27
E18	NO_TEST=YES	HT_VREF_DEBUG	64
E17	NO_TEST=YES	ITS_RUNNING	7
E16	NO_TEST=YES	LED801_1	8
E15	NO_TEST=YES	LED802_1	8
E14	NO_TEST=YES	PCI_CLK66M_SB_INT_R	27
E13	NO_TEST=YES	PCI_CLK_P3_R	27
E12	NO_TEST=YES	PCI_CLK_P4_R	27
E11	NO_TEST=YES	PN1	33
E10	NO_TEST=YES	PN2	33
E9	NO_TEST=YES	PN3	34
E8	NO_TEST=YES	Q800_D	8
E7	NO_TEST=YES	Q800_G	8
E6	NO_TEST=YES	Q801_B	8
E5	NO_TEST=YES	Q802_B	8
E4	NO_TEST=YES	Q802_E	8
E3	NO_TEST=YES	Q803_B	8
E2	NO_TEST=YES	Q901_GATE	9
E1	NO_TEST=YES	Q902_DRAIN	9
D5	NO_TEST=YES	Q1002_DRAIN	10
D3	NO_TEST=YES	TP_AGP_MB_AGP8X_DET_L	48
D4	NO_TEST=YES	TP_ATTENTION	29
D2	NO_TEST=YES	TP_AFN	29
C4	NO_TEST=YES	TP_PSRO1	29
C3	NO_TEST=YES	TP_PSRO2	29
C2	NO_TEST=YES	TP_PSYNCOUT	29
C1	NO_TEST=YES	TP_USB2_PWREN<2>	92
B5	NO_TEST=YES	TP_USB2_PWREN<3>	92
B4	NO_TEST=YES	TP_USB2_PWREN<4>	92
B35	NO_TEST=YES	TP_NEC_NTEST1	77
B34	NO_TEST=YES	TP_NEC_SMC	77
B33	NO_TEST=YES	TP_NEC_SMI_L	77
B32	NO_TEST=YES	TP_NEC_SRCLK	77
B31	NO_TEST=YES	TP_NEC_SRMOD	77
B30	NO_TEST=YES	TP_NEC_TEB	77
B29	NO_TEST=YES	TP_NEC_TEST	77
B28	NO_TEST=YES	TP_PLS_CLK_66M_0	27
B27	NO_TEST=YES	TP_PLS_CLK_66M_1	27
B26	NO_TEST=YES	TP_PLS_REF_CML	27
B25	NO_TEST=YES	TP_PLS_TEST1	27
B24	NO_TEST=YES	TP_PLS_TEST2	27
B23	NO_TEST=YES	TP_PLS_TEST3	27
B22	NO_TEST=YES	TP_SB_FSTEST	25
B21	NO_TEST=YES	TP_SB_PLLTEST	25
B20	NO_TEST=YES	TP_VREF_CG	48
B19	NO_TEST=YES	TP_SB_NC_P7	91
B18	NO_TEST=YES	TP_SB_NC_P8	91
B17	NO_TEST=YES	TP_SB_NC_R3	91
B16	NO_TEST=YES	TP_SB_NC_R4	91
B15	NO_TEST=YES	TP_SB_NC_R5	91
B14	NO_TEST=YES	TP_SB_NC_R6	91
B13	NO_TEST=YES	TP_SB_NC_R7	91
B12	NO_TEST=YES	TP_SB_NC_R8	91
B11	NO_TEST=YES	TP_SB_NC_T1	91
B10	NO_TEST=YES	TP_SB_NC_T2	91
B9	NO_TEST=YES	TP_SB_NC_T3	91
B8	NO_TEST=YES	TP_SB_NC_T4	91
B7	NO_TEST=YES	TP_SB_NC_T5	91
B6	NO_TEST=YES	TP_SB_NC_T6	91
B5	NO_TEST=YES	TP_SB_NC_T7	91
B4	NO_TEST=YES	TP_SB_NC_T8	91
B3	NO_TEST=YES	TP_SB_NC_U1	91
B2	NO_TEST=YES	TP_SB_NC_U2	91
B1	NO_TEST=YES	TP_SB_NC_U3	91
A35	NO_TEST=YES	TP_SB_NC_U4	91
A34	NO_TEST=YES	TP_SB_NC_U5	91
A33	NO_TEST=YES	TP_SB_NC_U6	91
A32	NO_TEST=YES	TP_SB_NC_V1	91
A31	NO_TEST=YES	TP_SB_NC_V2	91
A30	NO_TEST=YES	TP_SB_NC_V3	91
A29	NO_TEST=YES	TP_SB_NC_V4	91
A28	NO_TEST=YES	TP_SB_NC_W1	91
A27	NO_TEST=YES	TP_SB_NC_W3	91
A26	NO_TEST=YES	TP_SB_NC_Y1	91
A25	NO_TEST=YES	TP_SB_NC_Y3	91
A24	NO_TEST=YES	TP_SATA_CLK25M	27
A23	NO_TEST=YES	TP_USB2_PWREN<0>	92
A22	NO_TEST=YES	TP_USB2_PWREN<1>	92
A21	NO_TEST=YES	TP_DUMMY_A	24
A20	NO_TEST=YES	TP_DUMMY_B	24
A19	NO_TEST=YES	TP_RAM_CKE_R<2>	8
A18	NO_TEST=YES	Q2201_GATE	22
A17	NO_TEST=YES	Q2202_DRAIN	22
A16	NO_TEST=YES	R904_P2	9
A15	NO_TEST=YES	R2204_P2	22
A14	NO_TEST=YES	RAM_CLK66M_NB_R	27

E43	NO_TEST=YES	TP_RAM_CKE_R<3>	8
E42	NO_TEST=YES	TP_RAM_CKE_R<6>	8
E41	NO_TEST=YES	TP_RAM_CKE_R<7>	8
E40	NO_TEST=YES	TP_RAM_CS_L_R<10>	8
E39	NO_TEST=YES	TP_RAM_CS_L_R<11>	8
E38	NO_TEST=YES	TP_RAM_CS_L_R<2>	8
E37	NO_TEST=YES	TP_RAM_CS_L_R<3>	8
E36	NO_TEST=YES	TP_RAM_MUXEN0	8
E35	NO_TEST=YES	TP_RAM_MUXEN4	8
E34	NO_TEST=YES	TP_NB_PM_SLEEP0	24
E33	NO_TEST=YES	TP_J4000_SJRESET_L	40
E32	NO_TEST=YES	TP_J4001_SJRESET_L	40
E31	NO_TEST=YES	U2100_UNUSED	21
D61	NO_TEST=YES	PLS_CLK_66M_0_R	27
B60	NO_TEST=YES	PLS_CLK_66M_1_R	27
B59	NO_TEST=YES	SATA_CLK25M_R	27
B66	NO_TEST=YES	SB_CLK25M_ATA_R	27
B67	NO_TEST=YES	TEK_HT_A7	64
B68	NO_TEST=YES	TEK_HT_A9	64
B69	NO_TEST=YES	TEK_HT_A10	64
B70	NO_TEST=YES	TEK_HT_A12	64
B71	NO_TEST=YES	TEK_HT_B10	64
B72	NO_TEST=YES	TEK_HT_B12	64
B73	NO_TEST=YES	TP_PCI_CLK_P4	8
B74	NO_TEST=YES	U900_COMP	9
B75	NO_TEST=YES	U900_GATE_H	9
B76	NO_TEST=YES	U900_GATE_L	9
B77	NO_TEST=YES	U900_SS	9
B78	NO_TEST=YES	U900_VC	9
B80	NO_TEST=YES	U900_VC_D	9
B81	NO_TEST=YES	U900_VC_R	9
B82	NO_TEST=YES	U1000_FEEDBACK	10
B83	NO_TEST=YES	UATA_DASP_L_DS	83
B85	NO_TEST=YES	RFBD<1>	53 54
B86	NO_TEST=YES	RFBD<2>	53 54
B87	NO_TEST=YES	RFBD<3>	53 54
B88	NO_TEST=YES	RFBD<4>	53 54
B89	NO_TEST=YES	RFBD<6>	53 54
B90	NO_TEST=YES	RFBD<7>	53 54
B91	NO_TEST=YES	RFBD<8>	53 54
B92	NO_TEST=YES	RFBD<9>	53 54
B94	NO_TEST=YES	RFBD<11>	53 54
B95	NO_TEST=YES	RFBD<12>	53 54
B96	NO_TEST=YES	RFBD<13>	53 54
B97	NO_TEST=YES	RFBD<14>	53 54
B98	NO_TEST=YES	RFBD<16>	53 54
B99	NO_TEST=YES	RFBD<18>	53 54
B100	NO_TEST=YES	RFBD<19>	53 54
B101	NO_TEST=YES	RFBD<21>	53 54
B102	NO_TEST=YES	RFBD<22>	53 54
B103	NO_TEST=YES	RFBD<23>	53 54
B104	NO_TEST=YES	RFBD<24>	53 54
B105	NO_TEST=YES	RFBD<25>	53 54
B106	NO_TEST=YES	RFBD<26>	53 54
B107	NO_TEST=YES	RFBD<28>	53 54
B108	NO_TEST=YES	RFBD<29>	53 54
B109	NO_TEST=YES	RFBD<30>	53 54
B110	NO_TEST=YES	RFBD<32>	53 54
B111	NO_TEST=YES	RFBD<33>	53 54
B112	NO_TEST=YES	RFBD<35>	53 54
B113	NO_TEST=YES	RFBD<36>	53 54
B114	NO_TEST=YES	RFBD<37>	53 54
B115	NO_TEST=YES	RFBD<38>	53 54
B116	NO_TEST=YES	RFBD<40>	53 54
B117	NO_TEST=YES	RFBD<42>	53 54
B118	NO_TEST=YES	RFBD<43>	53 54
B119	NO_TEST=YES	RFBD<45>	53 54
B120	NO_TEST=YES	RFBD<46>	53 54
B121	NO_TEST=YES	RFBD<47>	53 54
B122	NO_TEST=YES	RFBD<48>	53 54
B123	NO_TEST=YES	RFBD<49>	53 54
B125	NO_TEST=YES	U2200_COMP	22
B126	NO_TEST=YES	U2200_GATE_H	22
B127	NO_TEST=YES	U2200_GATE_L	22
B128	NO_TEST=YES	U2200_SS	22
B129	NO_TEST=YES	U2200_VC	22
B130	NO_TEST=YES	U2200_VC_D	22
B131	NO_TEST=YES	U2200_VC_R	22
B132	NO_TEST=YES	Q5001_GATE	50
B133	NO_TEST=YES	Q5002_DRAIN	50
B134	NO_TEST=YES	U3310_DRN	33
B135	NO_TEST=YES	U3320_DRN	33
B136	NO_TEST=YES	U3410_DRN	34
B137	NO_TEST=YES	U5000_COMP	50
B138	NO_TEST=YES	U5000_FEEDBACK	50
B139	NO_TEST=YES	U5000_GATE_H	50
B140	NO_TEST=YES	U5000_GATE_L	50
B141	NO_TEST=YES	U5000_SS	50
B142	NO_TEST=YES	U5000_VC	50
B144	NO_TEST=YES	TP_SATA_RXD_N2_C	83
B145	NO_TEST=YES	TP_SATA_RXD_P2_C	83
B146	NO_TEST=YES	TP_SATA_TXD_N2	83
B150	NO_TEST=YES	TP_SATA_TXD_P2	83

GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS:

I74	NO_TEST=TRUE	EI_CPU_TO_NB_AD<0..43>	14 28 29
I76	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	14 28 29
I77	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	14 28 29
I78	NO_TEST=TRUE	EI_CPU_TO_NB_SR_N<0..1>	14 28 29
I79	NO_TEST=TRUE	EI_CPU_TO_NB_SR_P<0..1>	14 28 29
I81	NO_TEST=TRUE	EI_NB_TO_CPU_AD<0..43>	14 28 29
I83	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	14 28 29
I84	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	14 28 29
I85	NO_TEST=TRUE	EI_NB_TO_CPU_SR_N<0..1>	14 28 29
I87	NO_TEST=TRUE	EI_NB_TO_CPU_SR_P<0..1>	14 28 29
I91	NO_TEST=YES	CHKSTOP_L	8 14 29
I92	NO_TEST=YES	CPU_HRESET_L	14 29 30
I93	NO_TEST=YES	CPU_INT_L	14 25 29 30
I95	NO_TEST=YES	CPU1_HTBEN	14
I97	NO_TEST=YES	EI_CPU1_CLK_N	14 27
I98	NO_TEST=YES	EI_CPU1_CLK_P	14 27
I99	NO_TEST=YES	EI_QACK_L	14 28 29
I100	NO_TEST=YES	EI_QREQ_L	14 28 29 30
I101	NO_TEST=YES	EI_SE	14 28 29 30
I102	NO_TEST=YES	I2C_SMU_A_SCL_OUT_L	13 14 18
I103	NO_TEST=YES	I2C_SMU_A_SDA_OUT_L	13 14 18
I104	NO_TEST=YES	MCP_L	14 29
I105	NO_TEST=YES	RI_L	14 29 30
I106	NO_TEST=YES	SYNCENABLE	14 29 30
I107	NO_TEST=YES	TP_PROC_TRIGGER_OUT	14 29
I108	NO_TEST=YES	EI_CPU1_SYNC	14 27
I122	NO_TEST=YES	CPU1_HTBEN_R	14 27
I131	NO_TEST=YES	EI_CPU1_SYNC_R	14 27

101	IN	AUD_MIC_IN_N_CONN		FUNC_TEST=TRUE
101	IN	AUD_MIC_IN_P_CONN		FUNC_TEST=TRUE
90	IN	FW_VP		FUNC_TEST=TRUE
101	IN	GND_AUDIO_MIC_CONN		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SCL		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SDA		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SCL		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SDA		FUNC_TEST=TRUE
36 33 31	IN	KPGND2		FUNC_TEST=TRUE
36 33 31	IN	KPVDD2		FUNC_TEST=TRUE
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
77 76 75 74 73	IN	PCI_AD<31..0>		FUNC_TEST=TRUE
77 76 74 73	IN	PCI_CBE_L<3..0>		FUNC_TEST=TRUE
8	IN	PCI_CLK33M_AIRPORT		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_REQ_L		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_GNT_L		FUNC_TEST=YES
76 25	IN	PCI_SLOTA_INT_L		FUNC_TEST=YES
74 56 8	IN	PCI_RESET_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_FRAME_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_TRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_IRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_STOP_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_DEVSEL_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_PAR		FUNC_TEST=YES
76	IN	PCI_SLOTA_IDSEL		FUNC_TEST=YES
76 75 74	IN	ROM_CS_L		FUNC_TEST=YES
76 75 74	IN	ROM_OE_L		FUNC_TEST=YES
76 75 74	IN	ROM_WE_L		FUNC_TEST=YES
76 75	IN	ROM_ONBOARD_CS_L		FUNC_TEST=YES
76	IN	AIRPORT_CLKRUN_L_PD		FUNC_TEST=YES
76	IN	USB_BT_N		FUNC_TEST=YES
76	IN	USB_BT_P		FUNC_TEST=YES
92	IN	USB2_PORT1_N_F		FUNC_TEST=YES
92	IN	USB2_PORT1_P_F		FUNC_TEST=YES
92	IN	USB2_PORT2_N_F		FUNC_TEST=YES
92	IN	USB2_PORT2_P_F		FUNC_TEST=YES
92	IN	USB2_PORT3_N_F		FUNC_TEST=YES
92	IN	USB2_PORT3_P_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT1_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT2_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT3_F		FUNC_TEST=YES
94 25	IN	I2S1_DEV_TO_SB_DTI	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SYNC	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_BITCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_MCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SB_TO_DEV_DTO	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_RESET_L	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	MODEM_RING2SYS_L	2 TEST POINTS	FUNC_TEST=YES
59 58	IN	TMDS_CKM		FUNC_TEST=YES
59 58	IN	TMDS_D1M		FUNC_TEST=YES
59	IN	PPVCC_TMDS		FUNC_TEST=YES
59	IN	PP3V3_DDC		FUNC_TEST=YES
59	IN	TD0M		FUNC_TEST=YES
59	IN	TD0P		FUNC_TEST=YES
59	IN	TD1P		FUNC_TEST=YES
59	IN	TD2M		FUNC_TEST=YES
59	IN	TD2P		FUNC_TEST=YES
59	IN	TCKP		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 7	IN	GND_CHASSIS_TMDS		FUNC_TEST=YES
59	IN	FILT_ANALOG_RED		FUNC_TEST=YES
59	IN	FILT_ANALOG_GRN		FUNC_TEST=YES
59	IN	FILT_ANALOG_BLU		FUNC_TEST=YES
59	IN	VGA_HSYNC_R		FUNC_TEST=YES
59	IN	VGA_VSYNC_R		FUNC_TEST=YES
59 58	IN	MON_DETECT		FUNC_TEST=YES
59	IN	PP24V_INV		FUNC_TEST=YES
59	IN	GND_20_INV		FUNC_TEST=YES
59	IN	INV_20_LCD_PWM_		FUNC_TEST=YES
59	IN	INV_20_CUR_HI_F		FUNC_TEST=YES
59	IN	GND_17_INV		FUNC_TEST=YES
59	IN	PP5V_AGP_RL		FUNC_TEST=YES
59	IN	INV_17_LCD_PWM_F		FUNC_TEST=YES
59	IN	INV_17_CUR_HI_F		FUNC_TEST=YES
33 8	IN	CPU_VID_R<5..0>		FUNC_TEST=TRUE
36	IN	KPVDD2_FMAX		FUNC_TEST=YES
36	IN	KPGND2_FMAX		FUNC_TEST=YES
36	IN	TDIODE_POS_FMAX		FUNC_TEST=YES
36	IN	TDIODE_NEG_FMAX		FUNC_TEST=YES
36 33	IN	CORE_ISNS_M		FUNC_TEST=YES
36 33	IN	CORE_ISNS_P		FUNC_TEST=YES

PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN

	IN	PP12V_RUN	10 TEST POINTS	FUNC_TEST=YES
12 11 7	IN	PP5V_ALL	5 TEST POINTS	FUNC_TEST=YES
18 11 10 7	IN	PP5V_RUN	5 TEST POINTS	FUNC_TEST=YES
50 34 22 18 11 10 7	IN	PP3V3_RUN	5 TEST POINTS	FUNC_TEST=YES
	IN	PP24V_RUN	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP5V_DISK	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP12V_DISK	5 TEST POINTS	FUNC_TEST=YES
	IN	GND	12 TEST POINTS	FUNC_TEST=YES

PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON

	IN	PP2V5_RUN		FUNC_TEST=YES
	IN	PP1V5_RUN		FUNC_TEST=YES
18 13	IN	PP5V_PWRON		FUNC_TEST=YES
58 27 18 13	IN	PP3V3_PWRON		FUNC_TEST=YES
7	IN	PP1V2_PWRON		FUNC_TEST=YES
23 7 7	IN	=PPVCORE_PWRON_SB		FUNC_TEST=YES
13 8 7	IN	=PP3V3_ALL_SMU		FUNC_TEST=TRUE
31 8 7 7	IN	=PP5V_RUN_CPU		FUNC_TEST=YES
22	IN	PPVCORE_NB		FUNC_TEST=YES
35 34 33 7	IN	PPVCORE_CPU		FUNC_TEST=YES
34 33	IN	PP12V_CPU		FUNC_TEST=YES
33	IN	VCORE_SENSE_GND		FUNC_TEST=YES
33	IN	VCORE_SENSE_VOUT		FUNC_TEST=YES
8 7	IN	SMU_MANUAL_RESET_L	2 TEST POINTS	FUNC_TEST=YES
13 7	IN	SYS_POWER_BUTTON_L	2 TEST POINTS	FUNC_TEST=YES
7	IN	POWER_BUTTON_L		FUNC_TEST=YES
7	IN	RESET_BUTTON_L		FUNC_TEST=YES
13 8	IN	SMU_RESET_L		FUNC_TEST=YES
33 13 11 10 7	IN	SYS_POWERUP_L		FUNC_TEST=YES
50 46 22 11 10 9 8 59	IN	SYS_SLEEP		FUNC_TEST=YES
13 8	IN	SYS_POWERFAIL_L		FUNC_TEST=YES
9	IN	U900_FEEDBACK		FUNC_TEST=YES
22	IN	U2200_FEEDBACK		FUNC_TEST=YES
59 58	IN	ANALOG_RED		FUNC_TEST=YES
59 58	IN	ANALOG_GRN		FUNC_TEST=YES
59 58	IN	ANALOG_BLU		FUNC_TEST=YES
101 25	IN	AUDIO_LO_DET_L		FUNC_TEST=YES
75	IN	ROM_WP_L		FUNC_TEST=YES
83 80	IN	UATA_DD<15..0>		FUNC_TEST=TRUE
83 80	IN	UATA_DA<2..0>		FUNC_TEST=TRUE
83 80	IN	UATA_CS0_L		FUNC_TEST=YES
83 80	IN	UATA_CS1_L		FUNC_TEST=YES
83 80	IN	UATA_RESET_L		FUNC_TEST=YES
83	IN	UATA_DSTROBE_R		FUNC_TEST=YES
83 80	IN	UATA_HSTROBE		FUNC_TEST=YES
83 8066 83 80	IN	UATA_STOP		FUNC_TEST=YES
83	IN	UATA_DMARQ_R		FUNC_TEST=YES
83 80	IN	UATA_DMACK_L		FUNC_TEST=YES
83	IN	UATA_INTRQ_R		FUNC_TEST=YES
83	IN	UATA_IOCS16_PU		FUNC_TEST=YES
83	IN	UATA_CSEL_PD		FUNC_TEST=YES
83	IN	UATA_DASP_L		FUNC_TEST=TRUE
36 31	IN	TDIODE_NEG		FUNC_TEST=YES

FUNC TEST

SYNC_MASTER=N/A SYNC_DATE=N/A

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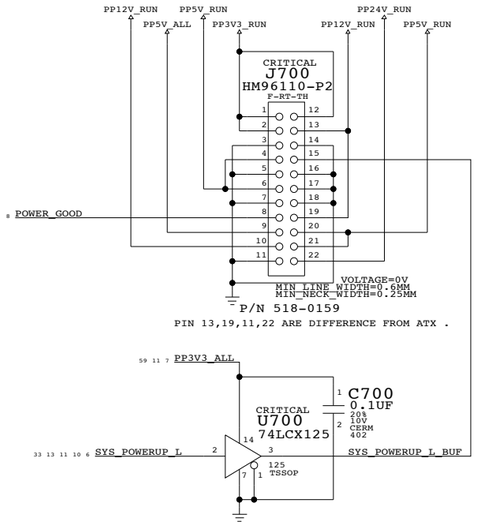
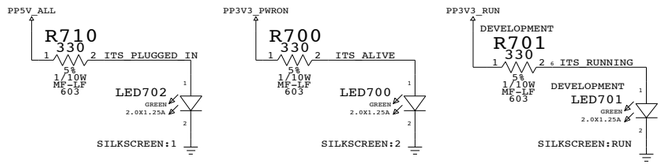
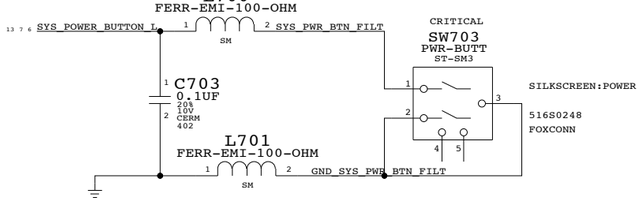
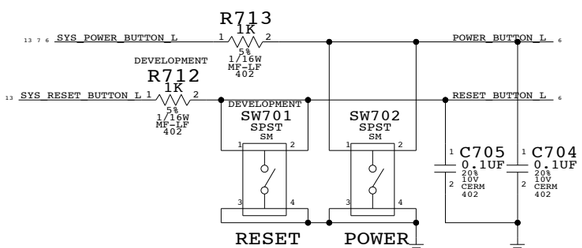
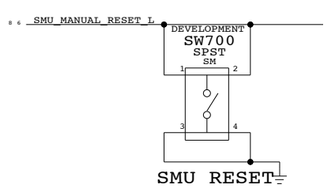
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 6 OF 102	











RUN RAILS

ONLY ON IN RUN

PP24V_RUN
VOLTAGE=24V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP24V_GRAPHICS 59

PP12V_RUN
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP12V_AGP 50 59
=PP12V_RUN_CPU 33
=PP12V_DISK 6 83

XW700 SM
XW704 SM
XW701 SM
XW705 SM
PP12V_AUDIO_CODEC 102
PP12V_AUDIO_SPKRAMP 100

PP5V_RUN
PP5V_RUN
VOLTAGE=5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
=PP5V_PATA 83
=PP5V_DISK 6 83
=PP5V_AGP 50 59
=PP5V_RUN_CPU 3 6 8 31
PP5V_AUDIO 101

PP3V3_RUN
PP3V3_RUN
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP3V3_AGP 48 50 56 59
PP3V3_AUDIO 95 100 101 102
=PP3V3_RUN_CPU 33
=PP3V3_PATA 83
=PP3V3_SB_PCI 74
=PP3V3_PCI 25 74 75 76 77
=PPVIO_PCI_USB2 77
=PP3V3_DISK 83

PP2V5_RUN
VOLTAGE=2.5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
PP2V5_GPU 52 54 55
=PP2V5_RUN_CPU 31
=PP2V5_RUN_RAM 44 45

PP1V5_RUN
PP1V5_RUN
VOLTAGE=1.5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PP1V5_AGP 48 49 50
=PPVCORE_PULSAR 26
=PP1V2_EI_CPU 14 18 29 30 31
=PP1V2_EI_NB 14 18 28

PPVCORE_CPU
MAKE_BASE=TRUE
=PPVCORE_CPU 29 31 32 36

PP1V2_RUN
VOLTAGE=1.2V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PP1V2_HT 24 60
=PP1V2_PULSAR 26
NOSTUFF
R720
0
PPVCORE_GPU 22 50 51

PWRON RAILS

ON IN RUN AND SLEEP

PP5V_PWRON
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
PP5V_PWRON_USB 92
=PP5V_PWRON_CPU 36
=PP5V_PWRON_VESTA 12

PP3V3_PWRON
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP3V3_PWRON_SB 23 25 74
=PPPCI64_PWRON_SB 23
=PPPCI32_PWRON_SB 23
PP3V3_PWRON_MODEM 94
=PP3V3_PWRON_USB 91
PP3V3_PWRON_BT 76
=PP3V3_PWRON_CPU 36
=PP3V3_PWRON_EI 28
=PP3V3_PWRON_VESTA 12
=PP3V3_PWRON_RAM 46

PP2V5_PWRON
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP2V5_PWRON_SB 23 25 74 88
=PP2V5_PWRON_RAM 26 37 40 46
=PP2V5_HT 60 64
=PP2V5_PWRON_HT 62
=PP2V5_ENET 87

PP1V5_PWRON
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
=PP1V5_PWRON_NB_AVDD 28 37 48 60
=PPVCORE_PWRON_PULSAR 26
=PPVCORE_NB 22

PP1V2_PWRON
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.2V
=PP1V2_PWRON_HT 62
=PP1V2_PWRON_DISK_SB 80
=PP1V2_PWRON_SB 25
=PPVCORE_PWRON_SB 3 6 23

ALL RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP5V_ALL
PP5V_ALL
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP5V_ALL_CPU 36

PP3V3_ALL
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
=PP3V3_ALL_SMU 6 8 13
=PP3V3_ALL_CPU 36
=PP3V3_VESTA 12
=PP3V3_ENET 86 87
=PP3V3_FW 89 90
=PP3V3_ENETFW 89

PP1V2_ALL
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
PP1V2_VESTA 12
=PP1V2_ENETFW 86 89

GND RAILS

XW702 SM
GND_AUDIO 102
XW706 SM
XW703 SM
GND_AUDIO_SPKRAMP 102 100
XW707 SM

CHASSIS GND

GND_CHASSIS_AUDIO_EXTERNAL 102 101
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
VOLTAGE=0
MIN_LINE_WIDTH=0.6MM
ZH700
315R138
GND_CHASSIS_VGA 59
GND_CHASSIS_USB 92
GND_CHASSIS_FIREWIRE 90

GND_CHASSIS_TMDS 59 6
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
ZH710
315R138
ZH702
7R4.15
GND_CHASSIS_RJ45 87
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
SH700
SHLD-IO-CONN
Q45-TH1
805-5664
GND_CHASSIS_AUDIO_INTERNAL 101
MAKE_BASE=TRUE
GND_CHASSIS_LED 21
ZH703
6.00MM-PTH
GND_CHASSIS_17_INCH_INVERTER 59
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
NOSTUFF
SDF700
HSK-NUT-6.5MM
TH
GND_CHASSIS_20_INCH_INVERTER 59
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
SDF700 IS USED FOR CPU HEATSINK MOUNTING

RTC BATTERY

ALWAYS ON (TRICKLE)

NOSTUFF
R703
0
DS700
SOD-123
=PP3V3_ALL_RTC 13
PP3V3_ALL_RTC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
B0530WXF
PP3V3_ALL_BATT_SAFETY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
R702
1K
PP3V3_ALL_BATT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CRITICAL
J702
BB10209-A5
TH

POWER CONN / ALIAS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	7	102

PCI CLOCKS

TP_NB_THMI — NB_THMI (24)
TP_THMO (MAKE_BASE=TRUE) — NB_THMO (24)
TP_RAM_CKE_R<2> (MAKE_BASE=TRUE) — RAM_CKE_R<2> (37)
TP_RAM_CKE_R<3> (MAKE_BASE=TRUE) — RAM_CKE_R<3> (37)
TP_RAM_CKE_R<6> (MAKE_BASE=TRUE) — RAM_CKE_R<6> (37)
TP_RAM_CKE_R<7> (MAKE_BASE=TRUE) — RAM_CKE_R<7> (37)
TP_RAM_MUXEN0 (MAKE_BASE=TRUE) — RAM_MUXEN0 (37)
TP_RAM_MUXEN4 (MAKE_BASE=TRUE) — RAM_MUXEN4 (37)
TP_RAM_CS_L_R<2> (MAKE_BASE=TRUE) — RAM_CS_L_R<2> (37)
TP_RAM_CS_L_R<3> (MAKE_BASE=TRUE) — RAM_CS_L_R<3> (37)
TP_RAM_CS_L_R<10> (MAKE_BASE=TRUE) — RAM_CS_L_R<10> (37)
TP_RAM_CS_L_R<11> (MAKE_BASE=TRUE) — RAM_CS_L_R<11> (37)

PCI_CLK33M_USB2 (MAKE_BASE=TRUE) — PCI_CLK_GP0 (27); =PCI_CLK33M_USB2 (77)
TP_PCI_CLK_GP1 (MAKE_BASE=TRUE) — PCI_CLK_GP1 (27)
PCI_CLK33M_AIRPORT (MAKE_BASE=TRUE) — PCI_CLK_P3 (27); PCI_CLK33M_AIRPORT (76)
TP_PCI_CLK_P4 (MAKE_BASE=TRUE) — PCI_CLK_P4 (27)
PCI_CLK33M_SB_EXT (MAKE_BASE=TRUE) — PCI_CLK_P1 (27)

SMU

TP_ALS0_OUT (MAKE_BASE=TRUE) — ALS0_OUT (13)
TP_ALS1_OUT (MAKE_BASE=TRUE) — ALS1_OUT (13)
TP_ALS_GAIN_BOOST (MAKE_BASE=TRUE) — ALS_GAIN_BOOST (13)
TP_SMU_ONEWIRE (MAKE_BASE=TRUE) — SMU_ONEWIRE (13)
TP_SYS_SLOT_PWR (MAKE_BASE=TRUE) — SYS_SLOT_PWR (13)
TP_SMU_PWRSEQ_P1_3 (MAKE_BASE=TRUE) — SMU_PWRSEQ_P1_3 (13)
TP_SYS_DOOR_AJAR_L (MAKE_BASE=TRUE) — SYS_DOOR_AJAR_L (13)
TP_FAN_PWM8 (MAKE_BASE=TRUE) — FAN_PWM8 (13)
TP_SYS_DRIVE_BAY_INT_L (MAKE_BASE=TRUE) — SYS_DRIVE_BAY_INT_L (13)
SMU_WARM_RESET_L (MAKE_BASE=TRUE) — NB_WARM_RESET_L (24)

PCI_RESET_L (MAKE_BASE=TRUE) — PCI_AIRPORT_RESET_L (76); GPU_RESET_L (49); =PCI_ROM_RESET_L (75); =PCI_USB2_RESET_L (77)

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PD45 SMU_RESET	P25MM		SYS_COLD_RESET_L 13 24
PD45 SMU_RESET	P25MM		SYS_WARM_RESET_L 8 25 74 77

DIAG LED

PP5V_ALL
R850 180 5% 1/16W MF-LF 402
LED850P1
LED850 RED-4.0MCD SM
LED850P2
DIAG_LED (13) — R851 1K 5% 1/16W MF-LF 402 — DIAG_LED_R
Q850 2N3904LF SOT23

CPU VID<0:5>

VID CONTROLLED BY SMU

PP3V3_RUN
R814 10K, R816 10K, R817 10K, R808 10K, R809 10K, R804 10K (5% 1/16W MF-LF 402)

CPU_VID<0> (13) — R819 0 — CPU_VID_R<0> (6 33)
CPU_VID<1> (13) — R820 0 — CPU_VID_R<1> (6 33)
CPU_VID<2> (13) — R821 0 — CPU_VID_R<2> (6 33)
CPU_VID<3> (13) — R822 0 — CPU_VID_R<3> (6 33)
CPU_VID<4> (13) — R823 0 — CPU_VID_R<4> (6 33)
CPU_VID<5> (13) — R824 0 — CPU_VID_R<5> (6 33)
(5% 1/16W MF-LF 402)

J803 BM12B-SRSS-TB (LF)(SN) F-ST-SM (NOSTUFF)

NOSTUFF: R832 1K, R831 1K, R830 1K, R829 1K, R827 1K, R811 20K (5% 1/16W MF-LF 402)

NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

BACKUP SMU RESET CIRCUIT

13 7 6 =PP3V3_ALL_SMU
NOSTUFF C800 0.1UF 20% 10V CERM 402
U890 SM: VCC, DELAY, NOSTUFF RESET, GND; VOLTAGE DETECTOR MC33465N_30ATR
NOSTUFF R890 1K 5% 1/16W MF-LF 402
8 7 6 SMU_MANUAL_RESET_L
NOSTUFF C890 0.01UF 20% 16V CERM 402
SMU_RESET_L (6 13)
NOSTUFF C891 1UF 10% 6.3V CERM 402
R810 0 5% 1/16W MF-LF 402

PULSAR ERROR_L LED

PP3V3_RUN
DEVELOPMENT R801 4.7K 5% 1/16W MF-LF 402
DEVELOPMENT R800 330 5% 1/16W MF-LF 402
ERROR_LED (6)
DEVELOPMENT D810 RED-4.0MCD SM
27 CLOCK_ERROR_L

VESTA JTAG

JTAG_VESTA_TRST_L (MAKE_BASE=TRUE) — =JTAG_VESTA_TRST_L (12)
TP_JTAG_VESTA_TCK (MAKE_BASE=TRUE) — =JTAG_VESTA_TCK (12)
TP_JTAG_VESTA_TDI (MAKE_BASE=TRUE) — =JTAG_VESTA_TDI (12)
TP_JTAG_VESTA_TDO (MAKE_BASE=TRUE) — =JTAG_VESTA_TDO (12)
TP_JTAG_VESTA_TMS (MAKE_BASE=TRUE) — =JTAG_VESTA_TMS (12)
R840 1K 5% 1/16W MF-LF 402

DOWNLOAD CONNECTOR

PP3V3_ALL
J802 HCT17U51 M-ST-TH
SMU_BOOT_SCLK (13) — J802_2 — R826 100 5% 1/16W MF-LF 402 — SMU_BOOT_BUSY (13)
SMU_BOOT_CE (13) — J802_6 — SMU_BOOT_RXD (13)
(SMU_BOOT_EPM)
SMU_BOOT_CNVSS (13) — SMU_MANUAL_RESET_L (6 7 8) — SMU_BOOT_TXD (13)
518-0158
NOSTUFF R806 10K, R807 10K (5% 1/16W MF-LF 402)
R805 0 (5% 1/16W MF-LF 402)
R803 10K (5% 1/16W MF-LF 402)

J802 & R826 CAN MOVE TO DEVELOPMENT BOM POST RAMP

PLL LOCK LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R837 180 5% 1/16W MF-LF 402
DEVELOPMENT Q802 2N3906 SM
Q802_B, Q802_E
DEVELOPMENT R838 1K 5% 1/16W MF-LF 402
DEVELOPMENT R835 180 5% 1/16W MF-LF 402
LED802_1
DEVELOPMENT LED802 GREEN 2.0X1.25A
Q803_C
DEVELOPMENT R839 180 5% 1/16W MF-LF 402
29 PLLLOCK (1) — Q803_B (2)
DEVELOPMENT Q803 2N3904LF SOT23

CHKSTOP LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R833 180 5% 1/16W MF-LF 402
LED801_1
DEVELOPMENT LED801 RED-4.0MCD SM
Q800_D
DEVELOPMENT R834 180 5% 1/16W MF-LF 402
Q800_G
DEVELOPMENT Q800 2N7002 SOT23-LF
DEVELOPMENT R836 180 5% 1/16W MF-LF 402
29 14 6 CHKSTOP_L (1) — Q801_B (2)
DEVELOPMENT Q801 2N3904LF SOT23

DEVELOPMENT J800

U.FL-R-SMT F-ST-SM
24 NB_PMR_OBSV
518S0104

SMU ANALOG VREF

13 PP3V3_ALL_SMU_AVCC
NOSTUFF R818 200 1% 1/16W MF-LF 402
NOSTUFF C801 2.2UF 20% 10V CERM 805
NOSTUFF VR801 2.5V SOT23
PPVREF_SMU (MAKE_BASE=TRUE) — =PPVREF_SMU (13)
R802 0 5% 1/16W MF-LF 402 — PPVREF_SMU_ADC_REF (36)
NOSTUFF C802 0.47UF 20% 10V CERM 603
GND_SMU_AVSS (13 33 36)
NOSTUFF R828 0 5% 1/16W MF-LF 402 — GND_SMU_AVSS_DAGND (36)

POWER_FAIL_L CONNECTION

7 POWER_GOOD
PP3V3_ALL
R813 430 5% 1/16W MF-LF 402
NOSTUFF R812 10K 5% 1/16W MF-LF 402
SYS_POWERFAIL_L (6 13)
R860 4.7K 5% 1/16W MF-LF 402
POWER_GOOD IS A 5V DRIVEN SIGNAL FROM POWER SUPPLY
2K PULLUP INSIDE P/S

CPU HEATSINK SMT NUTS

NOSTUFF SDF800 HSK-NUT-6.5MM TH — HS_SDF800 — C880 0.01UF 20% 16V CERM 402
NOSTUFF SDF801 HSK-NUT-6.5MM TH — HS_SDF801 — C881 0.01UF 20% 16V CERM 402
NOSTUFF SDF802 HSK-NUT-6.5MM TH — HS_SDF802 — C882 0.01UF 20% 16V CERM 402
NOSTUFF SDF803 HSK-NUT-6.5MM TH — HS_SDF803 — C883 0.01UF 20% 16V CERM 402
OMIT ZH804 6P15R5P4 — HS_SDF804 — C884 0.01UF 20% 16V CERM 402
SDF700 IS ALSO USED FOR HEATSINK MOUNTING

SHASTA JTAG PULL DOWN

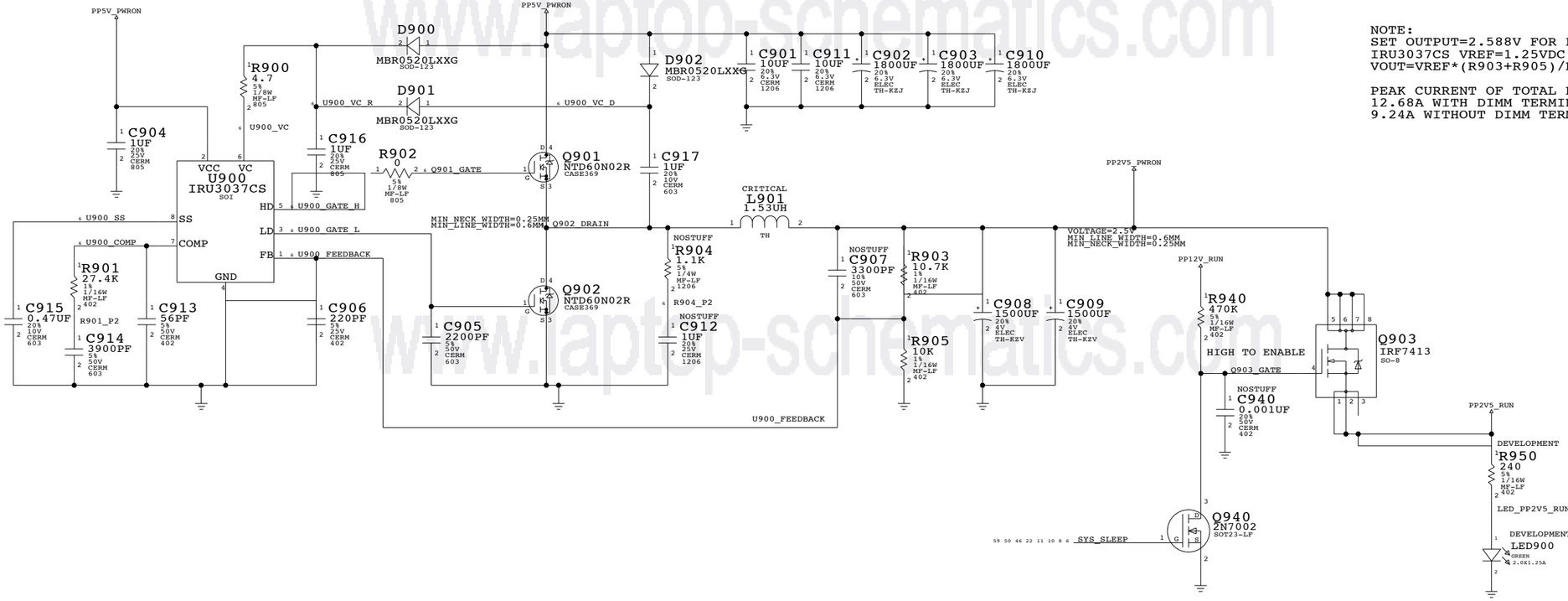
25 JTAG_SB_TRST_L
R825 10K 5% 1/16W MF-LF 402
THESE PINS HAVE INTERNAL PULLUPS
TP_JTAG_SB_TCK (MAKE_BASE=TRUE) — JTAG_SB_TCK (25)
TP_JTAG_SB_TDI (MAKE_BASE=TRUE) — JTAG_SB_TDI (25)
TP_JTAG_SB_TDO (MAKE_BASE=TRUE) — JTAG_SB_TDO (25)
TP_JTAG_SB_TMS (MAKE_BASE=TRUE) — JTAG_SB_TMS (25)

SIGNAL ALIAS

SYNC_MASTER=N/A — SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6772 | REV. E
SCALE NONE | SHT 8 OF 102

2.5V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=2.588V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.588VDC

PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

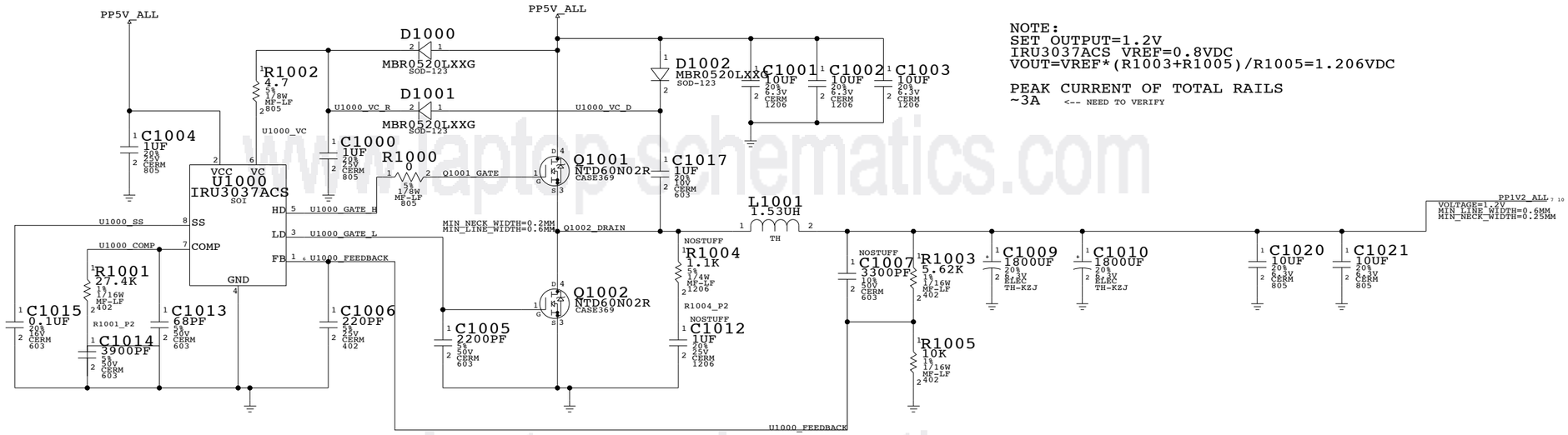
2.5V VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 9 OF 102	

PP1V2_ALL VOLTAGE REGULATOR

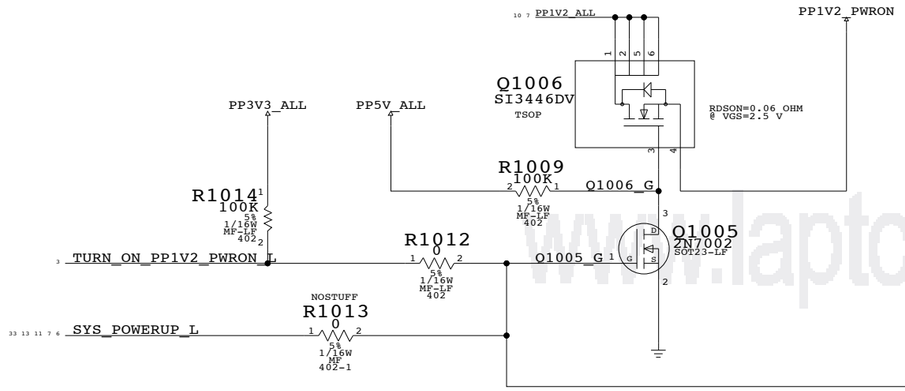


NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
~3A <-- NEED TO VERIFY

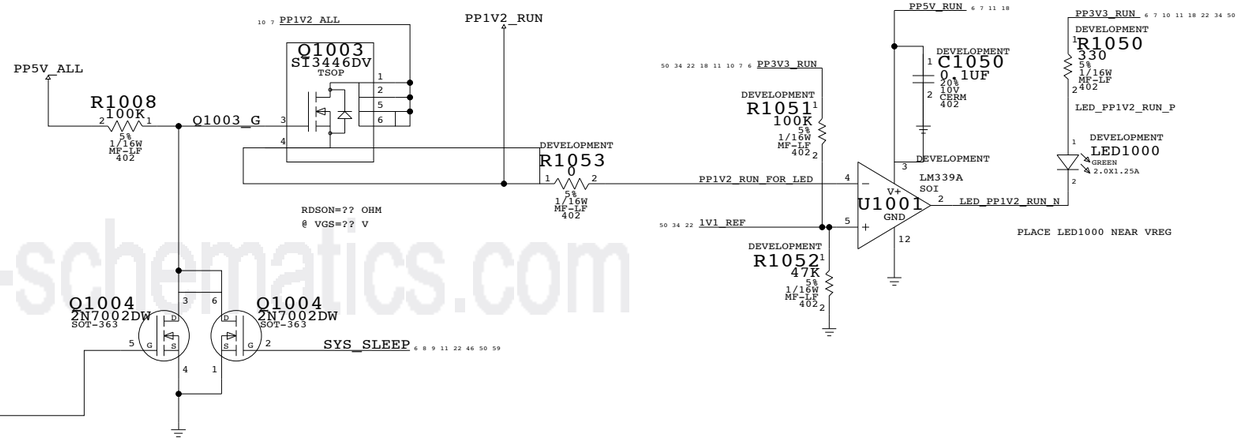
PP1V2_PWRON FET SWITCH

PEAK CURRENT ??A



PP1V2_RUN FET SWITCH

PEAK CURRENT ??A

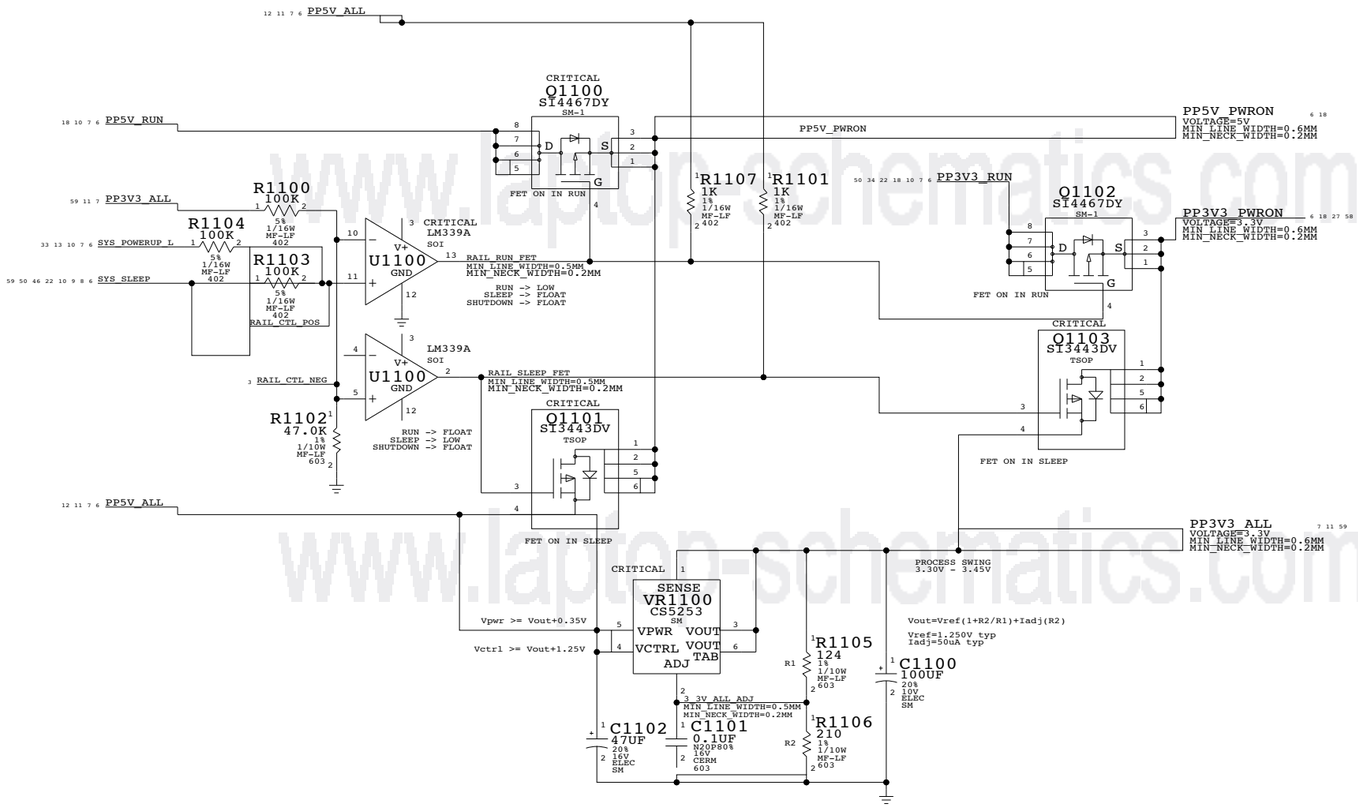


1.2V VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 10 OF 102	



5V & 3.3V VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	11	102

Page Notes

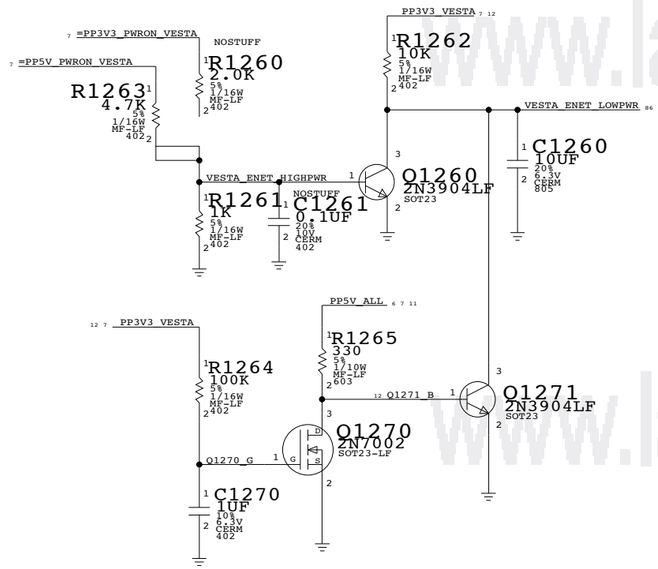
Power aliases required by this page:

Signal aliases required by this page:
(NONE)

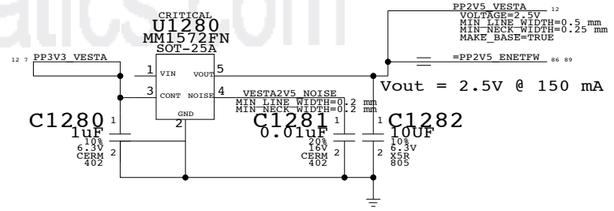
BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

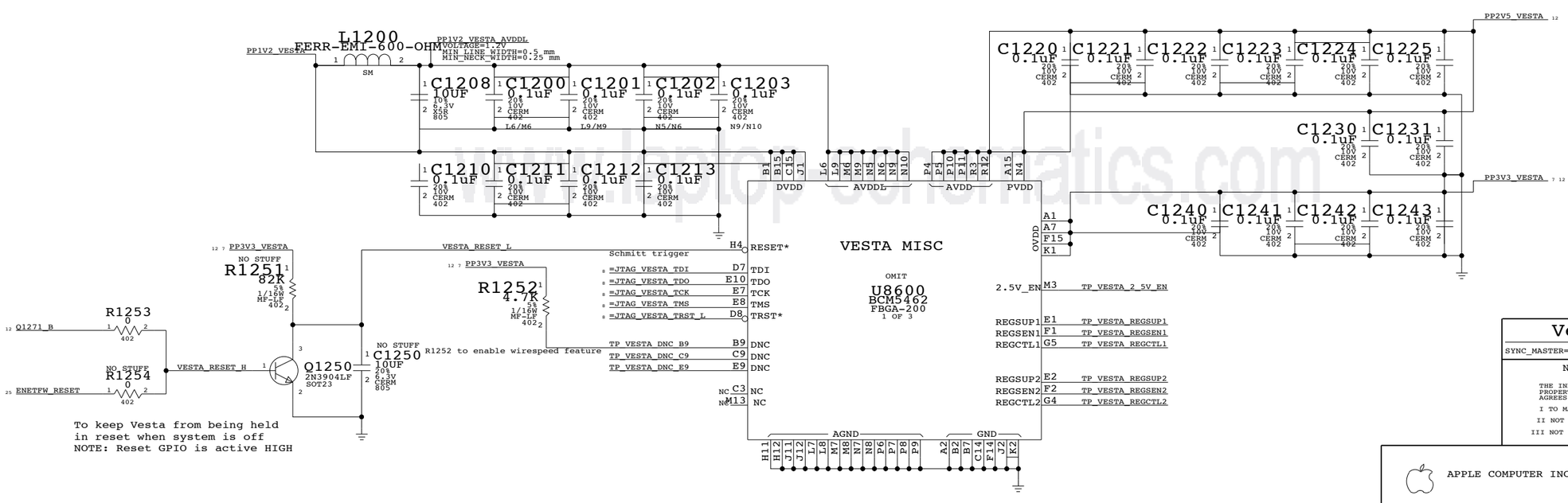
Ethernet LowPwr

ETHERNET PORTION IN LOW POWER MODE
WHEN NOT IN RUN MODE.



2.5V LDO





Vesta Core / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 6 OF 12	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	P25MM		SMU_CLK10M_XIN 13
	P25MM		SMU_CLK10M_XOUT 13
	P25MM		SMU_CLK10M_XOUT_R 13
RTC_CLK32K_XTAL	P25MM		RTC_CLK32K_X1 13
	P25MM		RTC_CLK32K_X2 13

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

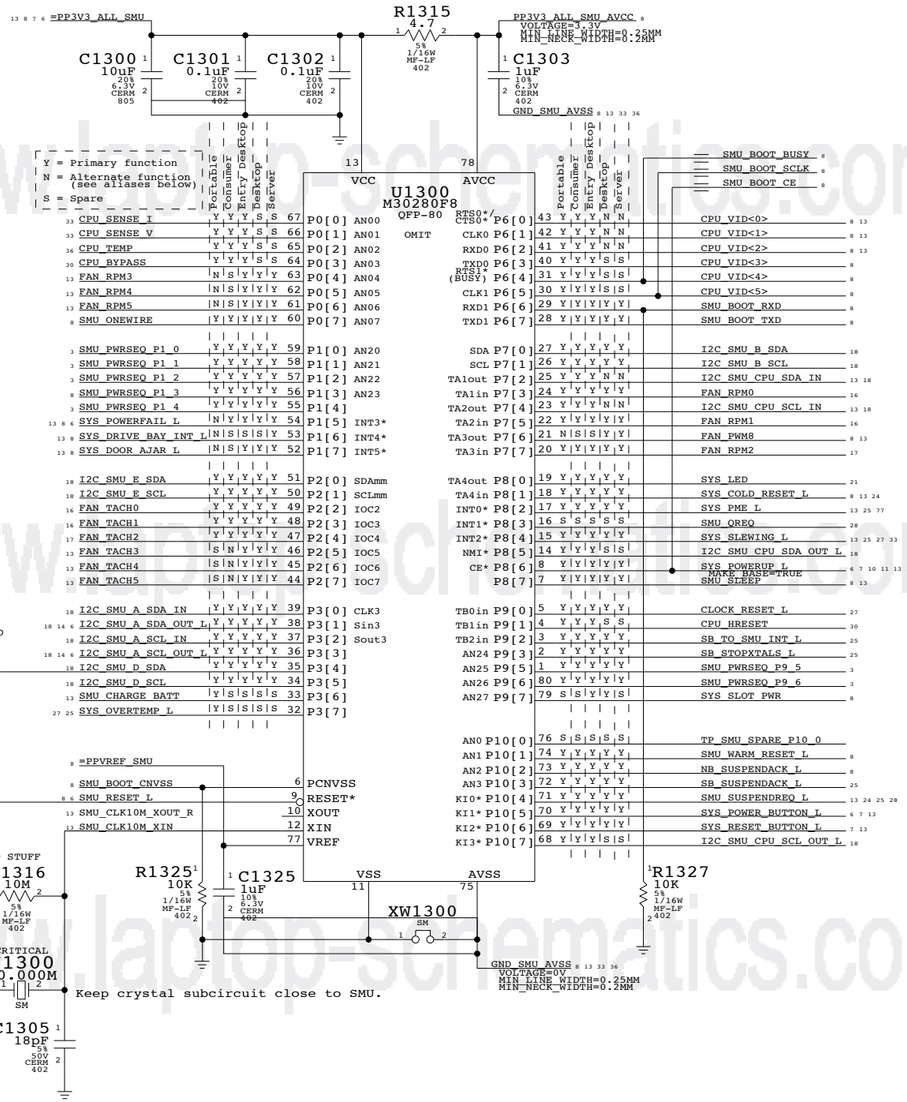
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

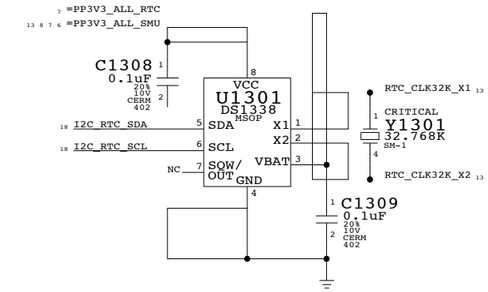
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

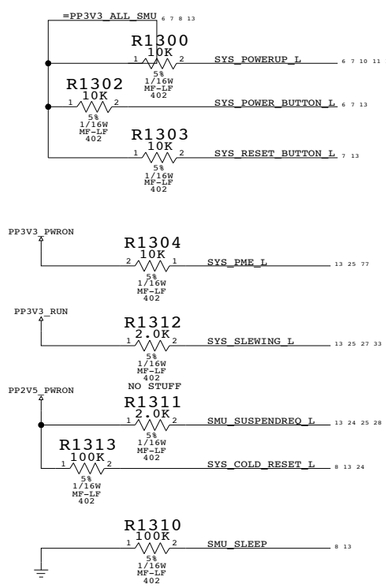
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4		ALS0_OUT
FAN_RPM4	0.5		ALS1_OUT
FAN_RPM5	0.6		ALS_GAIN_BOOST
SYS_POWERFAIL_L	1.5		SMU_ACIN
SYS_DRIVE_BAY_INT_L	1.6		SMU_BATT_DET_L
SYS_DOOR_AJAR_L	1.7		SYS_LID_OPEN
FAN_PWM8	7.6		SYS_KBDLED

Consumer

	Port		
FAN_TACH3	2.5		SYS_LED_RED
FAN_TACH4	2.6		SYS_LED_GREEN
FAN_TACH5	2.7		SYS_LED_BLUE
SMU_CHARGE_BATT	3.6		DIAG_LED

Tower & Server

	Port		
CPU_VID<0>	6.0		FAN_TACH6
CPU_VID<1>	6.1		FAN_TACH7
CPU_VID<2>	6.2		FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2		FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4		FAN_PWM7

System Management Unit

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 13 OF 102	

DEVELOPMENT
R1400
0
27 EI_CPU1_CLK_P_R 1 2 EI_CPU1_CLK_P 6 14 27
5% 1/16W
MF-LF 402

DEVELOPMENT
R1401
0
27 EI_CPU1_CLK_N_R 1 2 EI_CPU1_CLK_N 6 14 27
5% 1/16W
MF-LF 402

DEVELOPMENT
0 R1402
27 6 CPU1_HTBEN_R 1 2 CPU1_HTBEN 6 14
5% 402

DEVELOPMENT
0 R1403
27 6 EI_CPU1_SYNC_R 1 2 EI_CPU1_SYNC 6 14 27
5% 402

=PP1V2_EI_CPU 7 18 29 30 31

NOSTUFF
=PP1V2_EI_NB 7 14 18 28

J1400
YFS-30-03-H-08-SB
F-ST-BGA

28 18 14 7 =PP1V2_EI_NB

27 14 6 EI_CPU1_SYNC
29 8 6 CHKSTOP_L
EI_CPU1_CLK_P 6 14 27 14 6
EI_CPU1_CLK_N 6 14 27
EI_CPU_TO_NB_AD<3> 6 28 29
EI_CPU_TO_NB_AD<4> 6 28 29
EI_CPU_TO_NB_AD<7> 6 28 29
EI_CPU_TO_NB_AD<11> 6 28 29
EI_CPU_TO_NB_CLK_N 6 28 29
EI_CPU_TO_NB_CLK_P 6 28 29
EI_CPU_TO_NB_SR_N<1> 6 28 29
EI_CPU_TO_NB_SR_P<1> 6 28 29
EI_CPU_TO_NB_AD<17> 6 28 29
EI_CPU_TO_NB_AD<14> 6 28 29
EI_CPU_TO_NB_AD<24> 6 28 29
EI_CPU_TO_NB_AD<28> 6 28 29
29 28 6 EI_NB_TO_CPU_AD<13>
29 28 6 EI_NB_TO_CPU_AD<15>
29 28 6 EI_NB_TO_CPU_AD<17>
29 28 6 EI_NB_TO_CPU_AD<21>
29 28 6 EI_NB_TO_CPU_AD<20>
29 28 6 EI_NB_TO_CPU_AD<25>
29 28 6 EI_NB_TO_CPU_AD<29>
29 28 6 EI_NB_TO_CPU_AD<28>
29 28 6 EI_NB_TO_CPU_AD<40>
29 28 6 EI_NB_TO_CPU_AD<10>
29 28 6 EI_NB_TO_CPU_AD<39>
29 28 6 EI_NB_TO_CPU_AD<36>
30 29 6 RI_L
30 29 28 6 EI_OREQ_L
EI_NB_TO_CPU_AD<14> 6 28 29 28 6 EI_NB_TO_CPU_AD<5>
EI_NB_TO_CPU_AD<12> 6 28 29
EI_NB_TO_CPU_AD<18> 6 28 29
EI_NB_TO_CPU_AD<19> 6 28 29
EI_NB_TO_CPU_AD<27> 6 28 29
EI_NB_TO_CPU_AD<26> 6 28 29
EI_NB_TO_CPU_AD<30> 6 28 29
EI_NB_TO_CPU_AD<42> 6 28 29
EI_NB_TO_CPU_AD<41> 6 28 29
EI_NB_TO_CPU_SR_N<0> 6 28 29 28 6 EI_NB_TO_CPU_AD<37>
EI_NB_TO_CPU_SR_P<0> 6 28 29 28 6 EI_NB_TO_CPU_SR_N<1>
I2C_SMU_A_SCL_OUT_L 6 13 18 28 6 EI_NB_TO_CPU_SR_P<1>
30 29 6 CPU_INT_L
EI_CPU_TO_NB_AD<8> 6 28 29
EI_CPU_TO_NB_AD<13> 6 28 29
EI_CPU_TO_NB_AD<12> 6 28 29
EI_CPU_TO_NB_AD<5> 6 28 29
EI_CPU_TO_NB_AD<36> 6 28 29
EI_CPU_TO_NB_AD<35> 6 28 29
EI_CPU_TO_NB_AD<18> 6 28 29
EI_CPU_TO_NB_AD<43> 6 28 29
EI_CPU_TO_NB_AD<42> 6 28 29
EI_CPU_TO_NB_AD<38> 6 28 29
EI_CPU_TO_NB_AD<40> 6 28 29 28 6 EI_CPU_TO_NB_AD<15>
EI_NB_TO_CPU_AD<9> 6 28 29
EI_NB_TO_CPU_AD<11> 6 28 29
EI_NB_TO_CPU_AD<0> 6 28 29
EI_NB_TO_CPU_AD<1> 6 28 29
EI_NB_TO_CPU_AD<22> 6 28 29
EI_NB_TO_CPU_AD<33> 6 28 29
EI_NB_TO_CPU_AD<43> 6 28 29
EI_NB_TO_CPU_AD<2> 6 28 29 28 6 EI_NB_TO_CPU_AD<8>
EI_NB_TO_CPU_AD<38> 6 28 29 28 6 EI_NB_TO_CPU_AD<24>
SYNCENABLE 6 29 30 28 6 EI_NB_TO_CPU_AD<7>
TP_PROC_TRIGGER_OUT 6 29 29 28 6 EI_NB_TO_CPU_AD<6>
29 28 6 EI_QACK_L
EI_CPU_TO_NB_AD<6> 6 28 29
EI_CPU_TO_NB_AD<21> 6 28 29
EI_CPU_TO_NB_AD<20> 6 28 29
EI_CPU_TO_NB_AD<25> 6 28 29
EI_CPU_TO_NB_AD<26> 6 28 29
EI_CPU_TO_NB_SR_P<0> 6 28 29
EI_CPU_TO_NB_SR_N<0> 6 28 29
EI_CPU_TO_NB_AD<27> 6 28 29
EI_CPU_TO_NB_AD<23> 6 28 29
EI_CPU_TO_NB_AD<39> 6 28 29
EI_CPU_TO_NB_AD<16> 6 28 29
EI_CPU_TO_NB_AD<19> 6 28 29 28 6
EI_SE 6 28 29 29 6
EI_NB_TO_CPU_AD<4>
EI_NB_TO_CPU_AD<3>
EI_NB_TO_CPU_AD<16>
EI_NB_TO_CPU_AD<35>
EI_NB_TO_CPU_AD<34>
EI_NB_TO_CPU_AD<31>
EI_NB_TO_CPU_AD<32>
EI_NB_TO_CPU_AD<23>
EI_NB_TO_CPU_CLK_N
EI_NB_TO_CPU_CLK_P
MCP_L
18 13 6 I2C_SMU_A_SDA_OUT_L
CPU_HRESET_L 6 29 30
CPU1_HTBEN 6 14
EI_CPU_TO_NB_AD<0> 6 28 29
EI_CPU_TO_NB_AD<2> 6 28 29
EI_CPU_TO_NB_AD<1> 6 28 29
EI_CPU_TO_NB_AD<9> 6 28 29
EI_CPU_TO_NB_AD<10> 6 28 29
EI_CPU_TO_NB_AD<22> 6 28 29
EI_CPU_TO_NB_AD<31> 6 28 29
EI_CPU_TO_NB_AD<37> 6 28 29
EI_CPU_TO_NB_AD<30> 6 28 29
EI_CPU_TO_NB_AD<34> 6 28 29
EI_CPU_TO_NB_AD<33> 6 28 29
EI_CPU_TO_NB_AD<32> 6 28 29
EI_CPU_TO_NB_AD<41> 6 28 29
EI_CPU_TO_NB_AD<29> 6 28 29

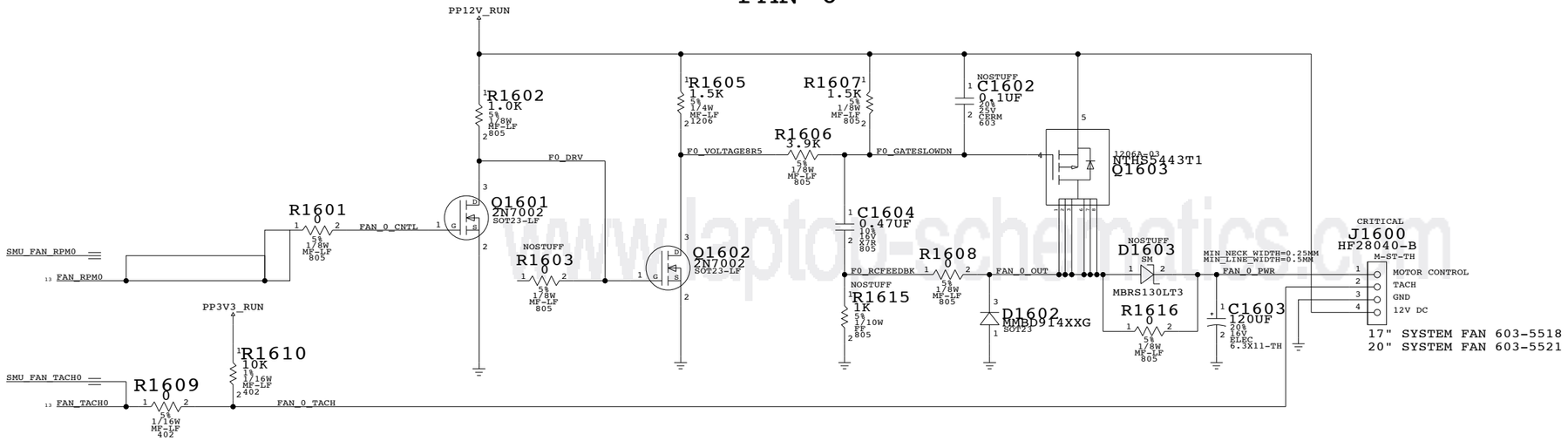
CPU LOGIC ANALYZER

SYNC_MASTER=N/A SYNC_DATE=N/A

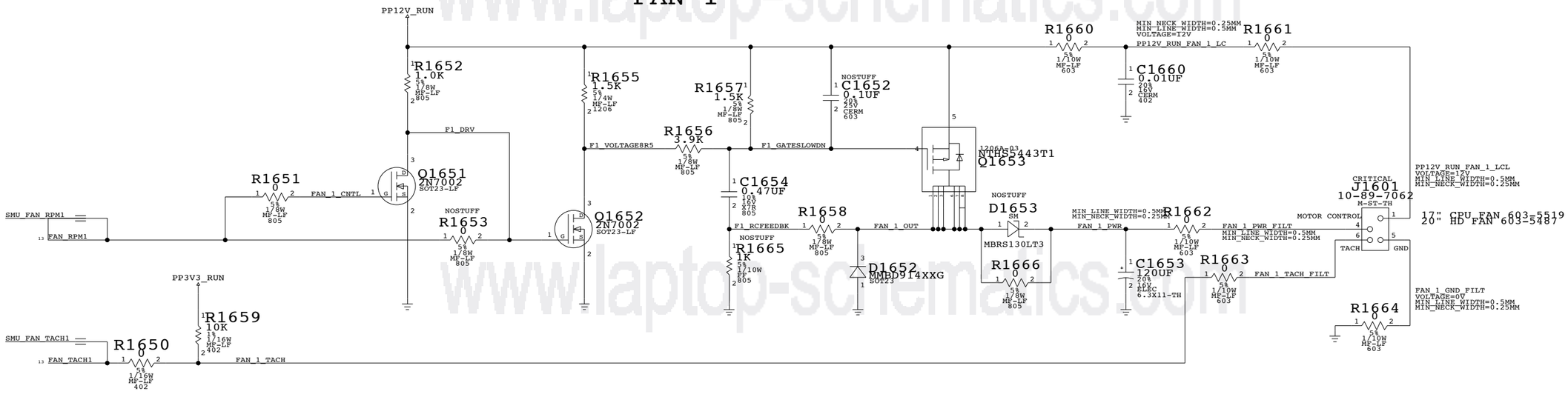
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 14 OF 102	

FAN 0



FAN 1



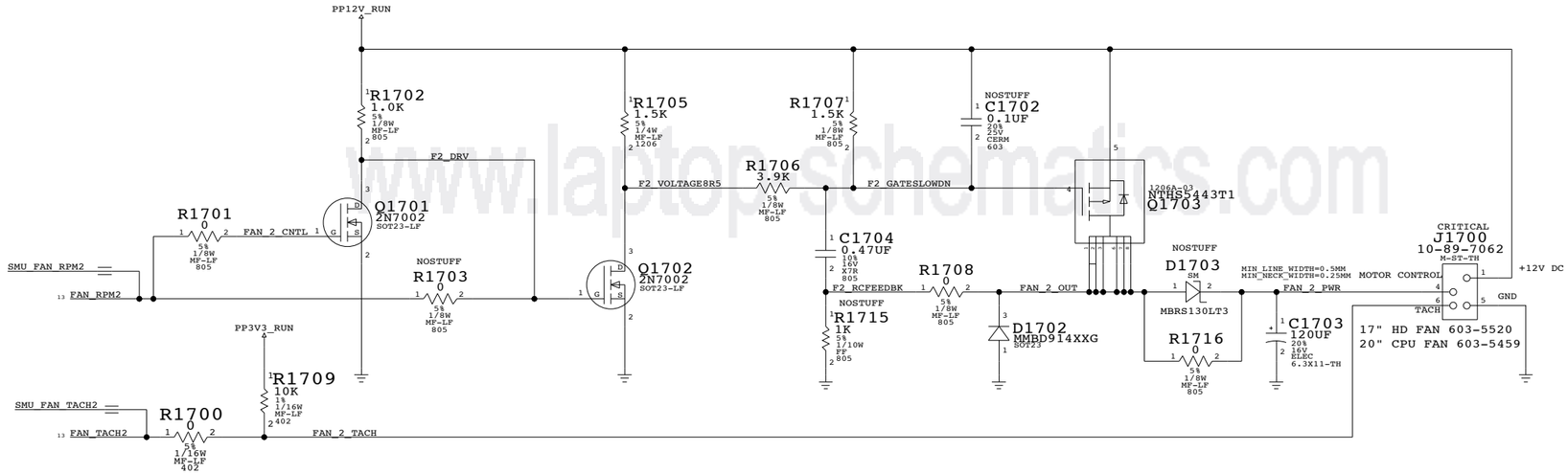
FAN 0, 1 & SYSTEM TEMP

SYNC_MASTER=N/A SYNC_DATE=N/A

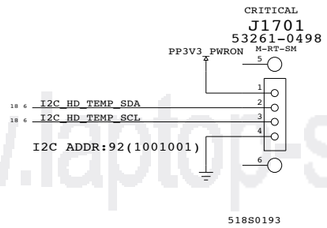
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 16 OF 102	

FAN 2



REMOTE HARD DRIVE TEMP SENSOR



FAN 2 & HD TEMP		
SYNC_MASTER=N/A		SYNC_DATE=N/A

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6772	E
	SCALE NONE	SHT 17 OF 102	

I2C A BUS

R1832 0 603 NOSTUFF — PP5V_PWRON → PP5V_U1800
R1833 0 603 — PP5V_RUN → PP5V_U1800
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM

C1800 0.1UF 20% 10V CERM 402 — PP3V3_RUN / PP3V3_PWRON

SMU MASTER U1300
- I2C_SMU_A_SDA_IN — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
- I2C_SMU_A_SDA_OUT_L — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
- I2C_SMU_A_SCL_IN — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
- I2C_SMU_A_SCL_OUT_L — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C

PINS 36-39

R1830 2.0K NOSTUFF, R1831 2.0K NOSTUFF, R1800 2.0K, R1801 2.0K — 5% 1/16W MF-LF 402

U1800 LM339A SOI (V+, GND)

R1809 4.7K NOSTUFF, R1828 4.7K, C1802 0.1UF 20% 10V CERM 402, R1808 200, R1810 200 — 5% 1/16W MF-LF 402 — =PP1V2_EI_NB

Q1800 2N7002DW SOT-363

U3LITE U3
- I2C_NB_A_SDA — 24
- I2C_NB_A_SCL — 24

PINS A20, B20

R1820 0 NOSTUFF, R1821 0 NOSTUFF — 5% 1/16W MF-LF 402

R1819 2.0K, R1818 2.0K — PP3V3_PWRON

R1816 200, R1817 200 — 5% 1/16W MF-LF 402 — =PP1V2_EI_CPU

SMU MASTER U1300
- I2C_SMU_CPU_SCL_IN — MAKE_BASE=TRUE — I2C
- I2C_SMU_CPU_SCL_OUT_L — MAKE_BASE=TRUE — I2C
- I2C_SMU_CPU_SDA_IN — MAKE_BASE=TRUE — I2C
- I2C_SMU_CPU_SDA_OUT_L — MAKE_BASE=TRUE — I2C

PINS 14,25,23,68

RP1800 0 5% 1/16W SM-LF
- SMU_CPU_JTAG_OR_I2C — NET_SPACING_TYPE=I2C
- I2C_CPU_A_SCL
- I2C_CPU_A_SDA_TO_SMU
- I2C_CPU_A_SDA_TO_CPU

CPU U2900
- I2C_CPU_A_SCL — 29
- I2C_CPU_A_SDA — 29

PINS AA20, Y21

Q1801 2N7002DW SOT-363 — I2C_CPU_SCL_LS

NOSTUFF RP1801 0 5% 1/16W SM-LF — CPU JTAG
- JTAG_CPU_TDO — 29 30
- JTAG_CPU_TDI — 29 30
- JTAG_CPU_TMS — 29 30
- JTAG_CPU_TCK — 29 30

C1801 0.1UF 20% 10V CERM 402 — I2C_0V6_REF

R1811 4.7K 5% 1/16W MF-LF 402

USE 576 OHM FOR R1811 IF 5V RAIL IS USED FOR REFERENCE

I2C B BUS

R1803 2.0K, R1802 2.0K — 5% 1/16W MF-LF 402 — PP3V3_PWRON

SMU MASTER U1300
- I2C_SMU_B_SDA — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
- I2C_SMU_B_SCL — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C

PINS 26, 27

PULSAR U2600
- I2C_CLOCK_SDA — 27
- I2C_CLOCK_SCL — 27

PINS C1, B1

NOTE: REMOVED FOR PVT

OPTICAL TEMP SENSOR U1602
- I2C_OPTICAL_SDA
- I2C_OPTICAL_SCL

PINS 1, 2
I2C ADDR:90

AMBIENT LIGHT SENSOR J2100
- I2C_ALS_SDA — 21
- I2C_ALS_SCL — 21

PINS 2, 3
I2C ADDR:94??

J2100 CAN BE USED AS A SECOND TEMP SENSOR

HD TEMP SENSOR U1702
- I2C_HD_TEMP_SDA — 17 6
- I2C_HD_TEMP_SCL — 17 6

PINS 2, 3
I2C ADDR:92

GPU TEMP SENSOR U5890
- I2C_GPU_DIODE_SDA — 58
- I2C_GPU_DIODE_SCL — 58

PINS 7, 8
I2C ADDR:98

I2C C BUS

PP2V5_PWRON

R1805 2.0K, R1804 2.0K — 5% 1/16W MF-LF 402 — NET_SPACING_TYPE=I2C

U3LITE MASTER U3
- I2C_NB_C_SDA — MAKE_BASE=TRUE — 24
- I2C_NB_C_SCL — MAKE_BASE=TRUE — 24

PINS C21, E21

DIMMS
J4000 = A0
J4001 = A2
- I2C_DIMM_SDA — 40
- I2C_DIMM_SCL — 40

PINS 91, 92 OF EACH DIMM

I2C D & E BUS

PP2V5_PWRON — PP3V3_ALL

R1812 2.0K, R1813 2.0K, R1807 2.0K, R1806 2.0K — 5% 1/16W MF-LF 402

U3LITE 'B' U3
- I2C_NB_B_SDA — 24 — I2C
- I2C_NB_B_SCL — 24 — I2C

PINS C20, B21

RTC U1301
- I2C_RTC_SDA — 13 — I2C
- I2C_RTC_SCL — 13 — I2C

PINS 5, 6

R1822 0 NOSTUFF, R1823 0 NOSTUFF — 5% 1/16W MF-LF 402

R1824 0 NOSTUFF, R1826 0, R1825 0 NOSTUFF, R1827 0 — 5% 1/16W MF-LF 402

SMU OLD 'E' MASTER U1300
- I2C_SMU_E_SDA — I2C
- I2C_SMU_E_SCL — I2C

PINS 50, 51

SMU NEW 'E' MASTER U1300
- I2C_SMU_D_SDA — I2C — 13
- I2C_SMU_D_SCL — I2C — 13

PINS 34, 35

I2C SB BUS

PP3V3_RUN

R1815 1K, R1814 1K — 5% 1/16W MF-LF 402

SHASTA MASTER U2300
- I2C_SB_SDA — MAKE_BASE=TRUE — 25 6
- I2C_SB_SCL — MAKE_BASE=TRUE — 25 6

PINS Y9, AB7

AUDIO U9500 / AU300
- I2C_AUDIO_SDA — 95
- I2C_AUDIO_SCL — 95

PINS 18, 19

I2C CONNECTIONS

SYNC_MASTER=N/A — SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 18 OF 102

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2101 0 1/16W MF-LF 402 5%
SYS_LED_GREEN MAKE_BASE=TRUE
PWM INPUT FROM SMU
G_PWM_IN_H

RGB_LED R2109 953K 1% 1/16W MF-LF 402
RGB_LED R2104 953K 1% 1/16W MF-LF 402
RGB_LED U2100 LP324 TSSOP
G_PWM_DC
RGB_LED C2104 0.022UF 20% 16V CERM 402
G_BASE_DRV

RGB_LED C2106 0.47UF 20% 10V CERM 603
RGB_LED R2105 200K 1% 1/16W MF-LF 402
G_IN_OFFSET
5MV INPUT OFFSET
RGB_LED R2112 1K 1% 1/16W MF-LF 402

100% DUTY CYCLE OF 3V-PP PWM = 0.5V

RGB_LED C2105 220PF 5% 25V CERM 402
GND_CHASSIS_LED 7 21

G_DRV_K MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED L2100 400-OHM-EMI SM-1
G_DRV MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED Q2102 2N3904LF SOT23
G_DRV_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED R2100 25.5 1% 1/16W MF-LF 402 <-- 17 INCH
CHANGE R2100 VALUE TO SET LED CURRENT
MAX LED CURRENT = 0.5 / R

RGB_LED LED2100 LATBG66B AMB-GRN-BLUE PLCC
AMB
GRN
BLUE
RGB_LED_A MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED L2104 400-OHM-EMI SM-1
PP5V_PWRON

RGB_LED C2107 220PF 5% 25V CERM 402
RGB_LED C2108 220PF 5% 25V CERM 402
GND_CHASSIS_LED 7 21
RGB_LED C2109 220PF 5% 25V CERM 402

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2102 953K 1% 1/16W MF-LF 402
RGB_LED R2115 0 5% 1/16W MF-LF 402
SYS_LED_RED MAKE_BASE=TRUE
PWM INPUT FROM SMU
R_PWM_IN_H

RGB_LED R2110 953K 1% 1/16W MF-LF 402
RGB_LED U2100 LP324 TSSOP
R_PWM_DC
RGB_LED C2101 0.022UF 20% 16V CERM 402
R_BASE_DRV

RGB_LED C2112 0.47UF 20% 10V CERM 603
RGB_LED R2111 200K 1% 1/16W MF-LF 402
R_IN_OFFSET
RGB_LED R2114 1K 1% 1/16W MF-LF 402

R_DRV_K MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED L2101 400-OHM-EMI SM-1
R_DRV MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED Q2108 2N3904LF SOT23
R_DRV_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED R2113 25.5 1% 1/16W MF-LF 402 <-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2118 953K 1% 1/16W MF-LF 402
RGB_LED R2130 0 5% 1/16W MF-LF 402
SYS_LED_BLUE MAKE_BASE=TRUE
PWM INPUT FROM SMU
B_PWM_IN_H

RGB_LED R2116 953K 1% 1/16W MF-LF 402
RGB_LED U2100 LP324 TSSOP
B_PWM_DC
RGB_LED C2102 0.022UF 20% 16V CERM 402
B_BASE_DRV

RGB_LED C2118 0.47UF 20% 10V CERM 603
RGB_LED R2117 200K 1% 1/16W MF-LF 402
B_IN_OFFSET
RGB_LED R2127 1K 1% 1/16W MF-LF 402

B_DRV_K MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED L2102 400-OHM-EMI SM-1
B_DRV MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED Q2114 2N3904LF SOT23
B_DRV_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RGB_LED R2126 25.5 1% 1/16W MF-LF 402 <-- 17 INCH

PP3V3_PWRON
PP5V_PWRON
RGB_LED C2103 0.1UF 20% 10V CERM 402
RGB_LED U2100 LP324 TSSOP
6 U2100 UNUSED

PLACE THESE PARTS CLOSE TO SMU IC

NOSTUFF Q2100 FDV302P SOT-23
PP3V3_PWRON
NOSTUFF R2119 953K 1% 1/16W MF-LF 402
SYS_LED_H
WHITE_LED R2106 1K 5% 1/16W MF-LF 402
SYS_GATE
WHITE_LED R2129 4.7K 5% 1/16W MF-LF 402
NOSTUFF R2132 1K 5% 1/16W MF-LF 402
SYS_LED
PWM INPUT FROM SMU
SYS_LED_IN
WHITE_LED R2107 0 5% 1/16W MF-LF 402
(STUFF WHEN SYS_LED_L = ACTIVE HIGH)
(AND NO STUFF R2132, R2119 & Q2100)

AMBIENT LIGHT SENSOR

CRITICAL
J2100 53261-0498 M-RT-SM
PP3V3_PWRON
I2C_ALS_SDA 18
I2C_ALS_SCL 18
518S0193

J2100 CAN BE USED AS A SECOND TEMP SENSOR

LED2101
WHITE SM6
SYS_DRV_A MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_PWRON
WHITE_LED R2120 0 5% 1/10W MF-LF 603
WHITE_LED C2111 220PF 5% 25V CERM 402
WHITE_LED C2110 220PF 5% 25V CERM 402
GND_CHASSIS_LED 7 21
WHITE_LED R2121 0 5% 1/10W MF-LF 603
SYS_LED_DRV_K MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
17_INCH_LCD
R2103 56.2 1% 1/16W MF-LF 402
SYS_LED_DRV_C MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
WHITE_LED Q2101 FDV301N SM

20 INCH -->

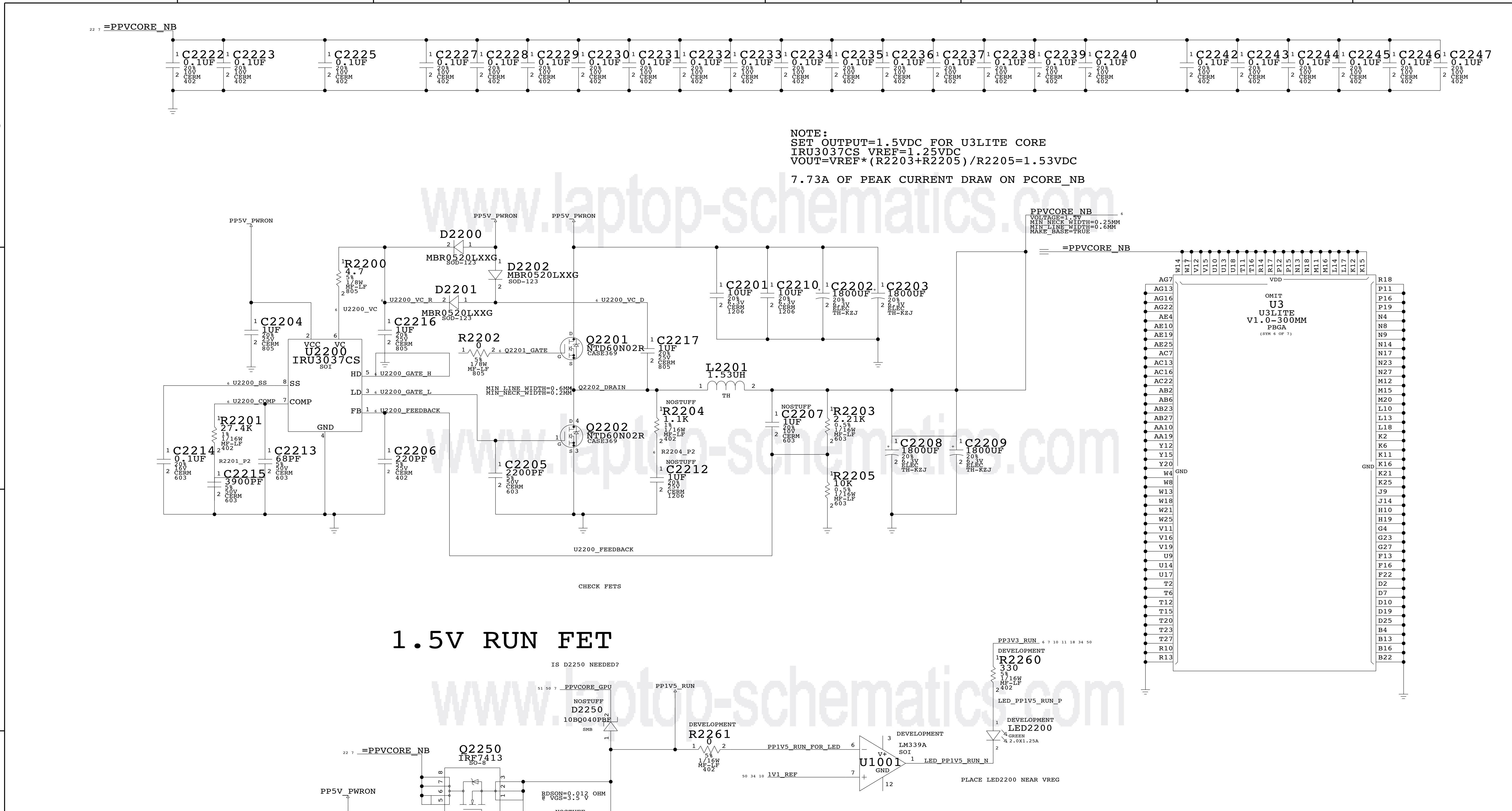
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
114S1821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

INDICATOR LED

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 21 OF 102	



=PPVCORE_NB
C2222 0.1UF 20% 10V CERM 402
C2223 0.1UF
C2225 0.1UF
C2227 0.1UF
C2228 0.1UF
C2229 0.1UF
C2230 0.1UF
C2231 0.1UF
C2232 0.1UF
C2233 0.1UF
C2234 0.1UF
C2235 0.1UF
C2236 0.1UF
C2237 0.1UF
C2238 0.1UF
C2239 0.1UF
C2240 0.1UF
C2242 0.1UF
C2243 0.1UF
C2244 0.1UF
C2245 0.1UF
C2246 0.1UF
C2247 0.1UF
NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R2203+R2205)/R2205=1.53VDC
7.73A OF PEAK CURRENT DRAW ON PCORE_NB
PP5V_PWRON
D2200 MBR0520LXXG SOD-123
D2202 MBR0520LXXG SOD-123
D2201 MBR0520LXXG
R2200 4.7 5% 1/8W MF-LF 805
C2204 1UF 20% 25V CERM 805
U2200 IRU3037CS SO1
VCC VC HD LD FB SS COMP GND
U2200_VC_R
U2200_VC_D
U2200_VC
C2216 1UF 20% 25V CERM 805
R2202 0 5% 1/8W MF-LF 805
Q2201_GATE
Q2201 NTD60N02R CASE369
C2217 1UF 20% 25V CERM 805
U2200_GATE_H
U2200_GATE_L
U2200_FEEDBACK
U2200_SS
U2200_COMP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
Q2202_DRAIN
L2201 1.53UH TH
Q2202 NTD60N02R CASE369
R2201 27.4K 1% 1/16W MF-LF 402
R2201_P2
C2214 0.1UF 20% 16V CERM 603
C2215 3900PF 5% 50V CERM 603
C2213 68PF 5% 50V CERM 603
C2206 220PF 5% 25V CERM 402
C2205 2200PF 5% 50V CERM 603
NOSTUFF
R2204 1.1K 1% 1/16W MF-LF 402
R2204_P2
C2212 1UF 20% 25V CERM 1206
C2201 10UF 20% 6.3V CERM 1206
C2210 10UF 20% 6.3V CERM 1206
C2202 1800UF 20% 6.3V ELEC TH-KZJ
C2203 1800UF 20% 6.3V ELEC TH-KZJ
C2207 1UF 20% 10V CERM 603
R2203 2.21K 0.5% 1/16W MF-LF 603
R2205 10K 0.5% 1/16W MF-LF 603
C2208 1800UF 20% 6.3V ELEC TH-KZJ
C2209 1800UF 20% 6.3V ELEC TH-KZJ
PPVCORE_NB
VOLTAGE=1.5V
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
MAKE_BASE=TRUE
=PPVCORE_NB
OMIT
U3
U3LITE
V1.0-300MM
PBGA
(SYM 6 OF 7)
VDD GND
CHECK FETS
1.5V RUN FET
IS D2250 NEEDED?
PPVCORE_GPU
NOSTUFF
D2250 10BQ040PBF SMB
PP1V5_RUN
DEVELOPMENT
R2261 0 5% 1/16W MF-LF 402
PP1V5_RUN_FOR_LED
1V1_REF
U1001 LM339A SOI
LED_PP1V5_RUN_N
PP3V3_RUN
R2260 330 5% 1/16W MF-LF 402
LED_PP1V5_RUN_P
LED2200 GREEN 2.0X1.25A
PLACE LED2200 NEAR VREG
=PPVCORE_NB
Q2250 IRF7413 SO-8
PP5V_PWRON
RDSON=0.012 OHM @ VGS=3.5 V
C2250 0.1UF 20% 10V CERM 402
R2250 100K 5% 1/16W MF-LF 402
Q5006G
Q2251 2N7002 SOT23-LF
SYS_SLEEP

U3LITE CORE POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 22 OF 102	

Page Notes

Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

=PPVCORE_PWRON_SB

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.0
BGA
(1 OF 8)

POWER

OMIT

VDDC: H15 H8 J12 J15 K8 L15 L8 M15 N8 P15 R10 R12 R9 T10 T14

VDDO33: AA1 AA2 AA3 AB10 AB2 AB6 B1 B2 B5 D1 F4 F8 H1 L7 M1 R2 U12 U9 V7 W4

GND: A1 A2 A22 A5 AA10 AA6 AB1 AB22 C19 D2 E22 F3 F7 H2 H9 J10 J11 J13 J14 J16

GND: J22 K10 K11 K12 K13 K7 K9 L10 L11 L12 L13 L14 L16 L9 M10 M11 M12 M13 M14

GND: W5 W19 U22 U13 U10 T12 R19 P9 P4 P14 P13 P12 P10 N9 N22 N13 N12 N11 N10 M2

Shasta max (est 06/30/03) current:

DIGITAL	- 1.2V -	950 mA	(1175 mW)
ANALOG12	- 1.2V -	600 mA	(760 mW)
VDDPs	- 2.5V -	100 mA	(250 mW)
I/O 2.5	- 2.5V -	20 mA	(60 mW)
I/O 3.3	- 3.3V -	220 mA	(770 mW)
Total:			3015 mW

=PP2V5_PWRON_SB

VDDO25: D19 G15

C2350 C2351
0.1uF 20% 10V CERM 402

=PPPCI64_PWRON_SB

VIO1: H18 H17 K21

C2355 C2356 C2357
0.1uF 20% 10V CERM 402

For PCI_AD<63..32>

VIO2: L21 W22 V19

VDDP_KL: V8

=PPPCI32_PWRON_SB

C2360 C2361 C2362
0.1uF 20% 10V CERM 402

For PCI_AD<31..0>

=PP2V5_PWRON_SB

C2365
0.1uF 20% 10V CERM 402

Shasta Core Power

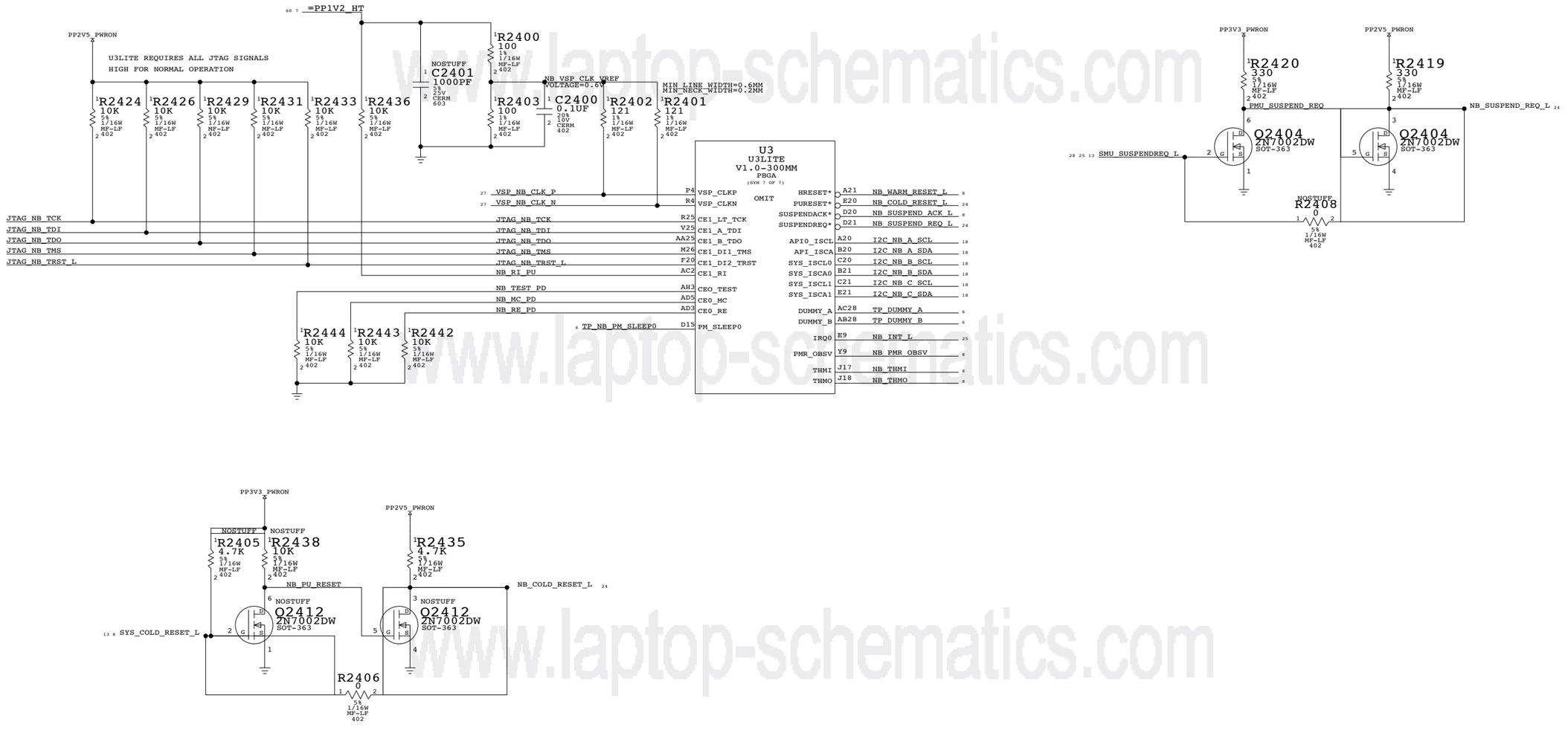
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE: NONE

SHT 23 OF 102



U3LITE MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 24 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI	25 95
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO	25 95
I2S0_TO_DEV	AUDIO		I2S0_MCLK	25 102
I2S0_BIDIR			I2S0_BITCLK	25 102
I2S0_BIDIR			I2S0_SYNC	25 95
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI	6 25 94
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO	6 25 94
I2S1_TO_DEV	P25MM		I2S1_MCLK	6 25 94
I2S1_BIDIR			I2S1_BITCLK	6 25 94
I2S1_BIDIR			I2S1_SYNC	6 25 94
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI	25 102
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO	25 102
I2S2_TO_DEV	P25MM		I2S2_MCLK	25 102
I2S2_BIDIR			I2S2_BITCLK	25 102
I2S2_BIDIR			I2S2_SYNC	25 102
SB_CLK18M_XTAL	CLOCKS		SB_CLK18M_XTALI	25
	CLOCKS		SB_CLK18M_XTALO	25
	CLOCKS		SB_CLK18M_XTALO_R	25
SB_CLK25M_ATA	CLOCKS		SB_CLK25M_ATA	25 27

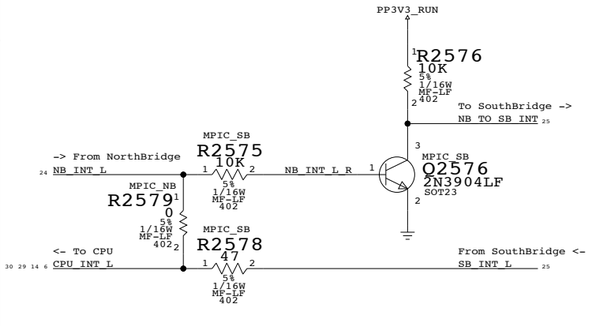
Page Notes

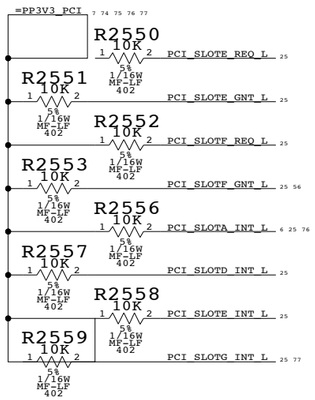
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

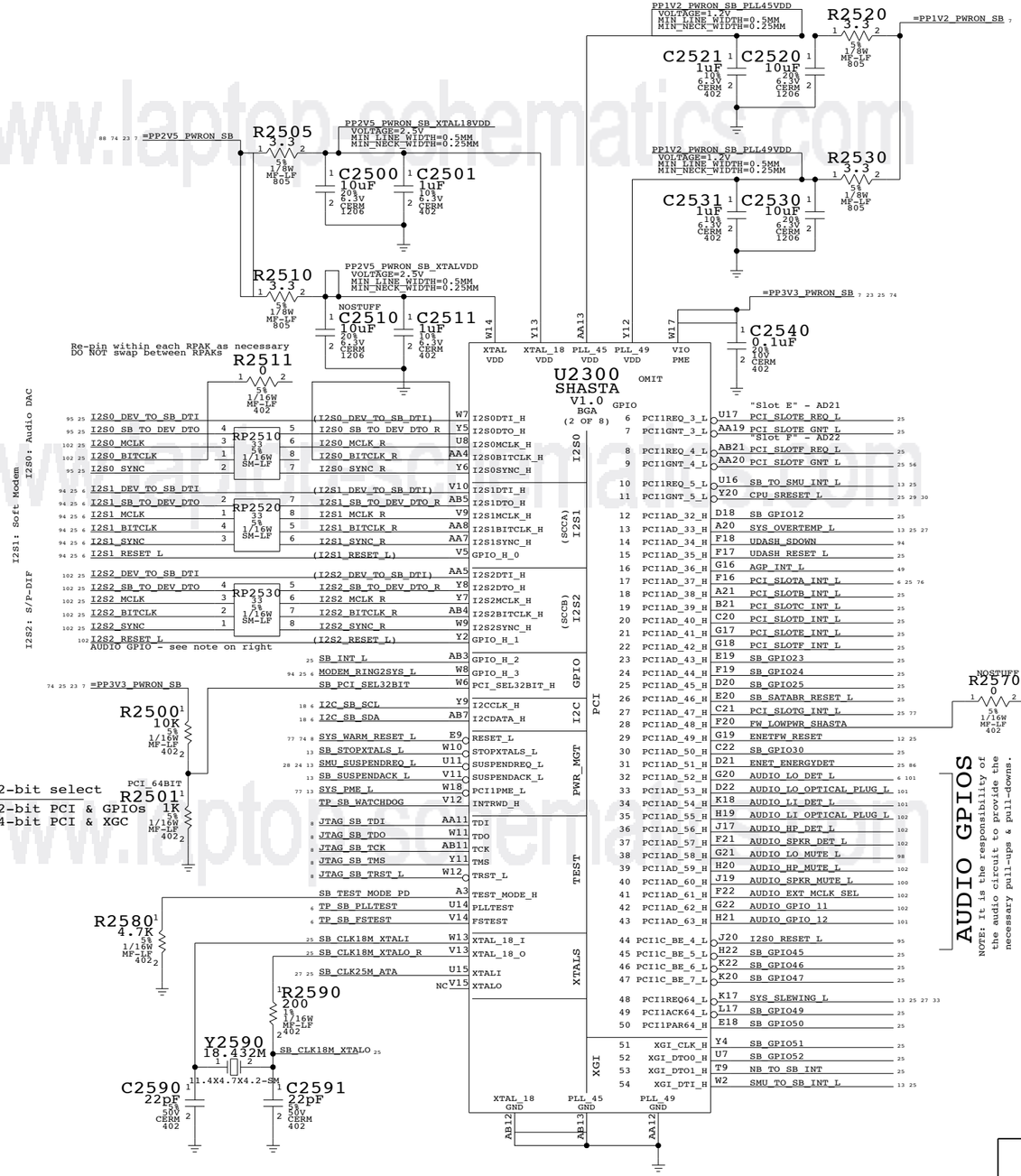
NorthBridge / SouthBridge MPIC Routing





Page Notes

PCI 32-bit select
1 = 32-bit PCI & GPIOs
0 = 64-bit PCI & XGC

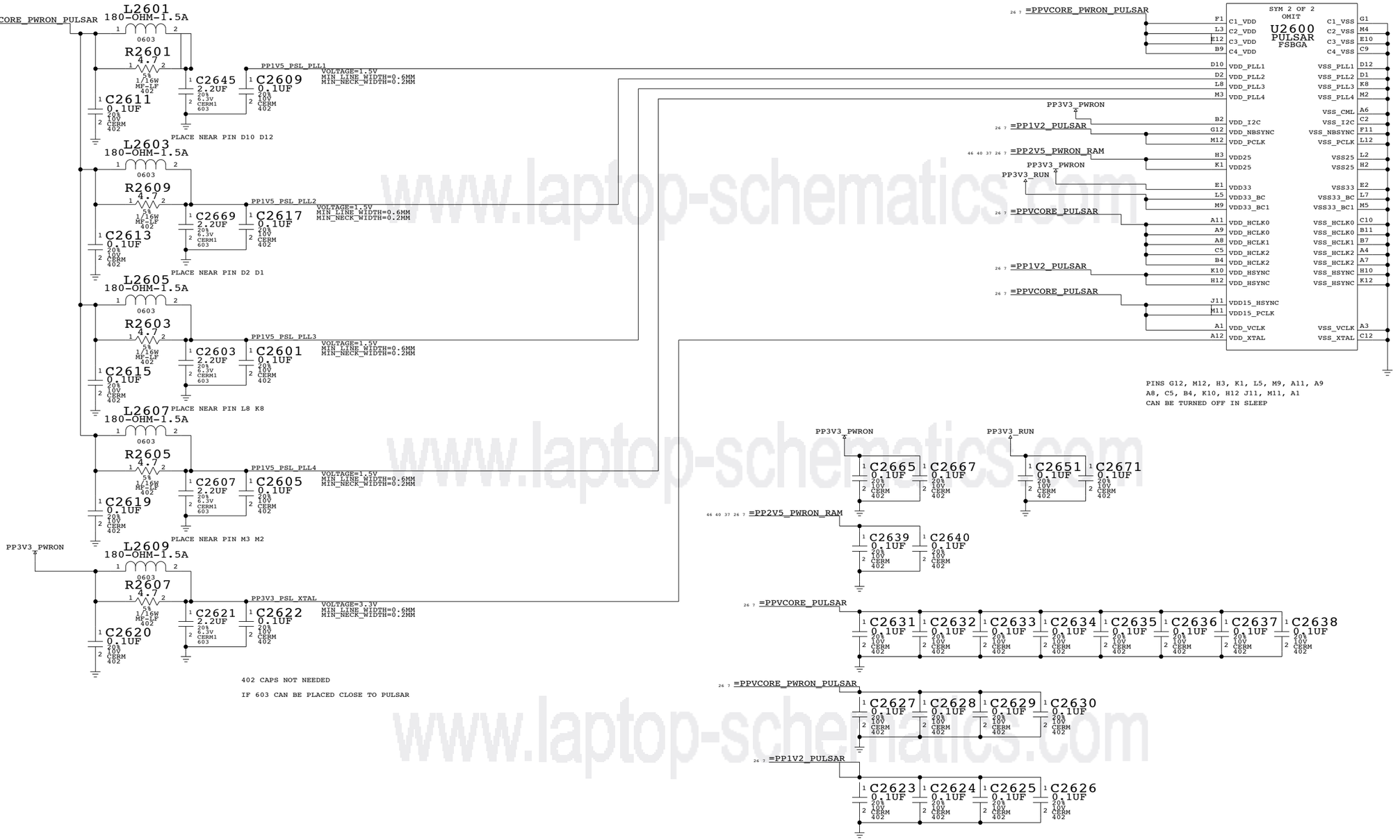


Shasta Serial / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 25 OF 102	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

PULSAR POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 26 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	CLOCKS	EI_CPU_CLK
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	CLOCKS	EI_CPU_CLK
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	CLOCKS	EI_CPU1_CLK
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	CLOCKS	EI_CPU1_CLK
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	CLOCKS	EI_NB_CLK
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	CLOCKS	EI_NB_CLK
EI_CPU_SYNC	EI_SYNC	CLOCKS	CLOCKS	
EI_NB_SYNC		CLOCKS	CLOCKS	
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	CLOCKS	
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	CLOCKS	VSP_NB_CLK
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	CLOCKS	VSP_NB_CLK
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	CLOCKS	
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	CLOCKS	
HT_CLK66M_NB	HT_NB_CLK	CLOCKS	CLOCKS	
HT_CLK66M_SB	HT_SB_CLK	CLOCKS	CLOCKS	
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	CLOCKS	
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	CLOCKS	
PLS_EXTCLK	PLS_XTAL	CLOCKS	CLOCKS	
CPU_HTBEN		CLOCKS	CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

			NET SPACING TYPE
GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING*	K9	SLEWING_L_R	CLOCKS
ERROR*	M8	CLOCK_ERROR_L	
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

SCLK	C1	I2C_CLOCK_SCL
SDATA	B1	I2C_CLOCK_SDA
RESET*	D3	PLS_RESET_L
XIN	C11	PLS_X_IN
XOUT	B12	PLS_X_OUT
ADDRSEL	E3	PLS_X_ADDRSEL
TEST1	K3	TP_PLS_TEST1
TEST2	E11	TP_PLS_TEST2
TEST3	D11	TP_PLS_TEST3
SCAN_MODE	M1	PLS_SCAN_MODE
REF15	G11	PLS_REF15
REF25	J2	PLS_REF25
REF33	M6	PLS_REF33
REF_CML	A5	TP_PLS_REF_CML
PRES_CML	B6	PLS_PRES_CML
FORCESPO*	F2	PLS_FORCE_P0_L_R
PD	C3	

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

PP3V3_PWRON
SYS_OVERTEMP_L
=PULSAR_POWER_DOWN
PULSAR_POWER_DOWN_R
PLS_EXTCLK
PLS_INTERM
PLS_X_IN_B
PLS_X_OUT_B
CLOCK_RESET_L

R2722 1K 5% 1/16W MF-LF 402
R2748 0 NOSTUFF 5% 1/16W MF-LF 402
R2704 0 5% 402
R2738 1K NOSTUFF 5% 402
R2706 249 1% 402
R2744 681 1% 402
R2740 1K 1% 402
R2746 1K 1% 402
R2742 806 1% 402
R2750 47 5% 402
R2724 1K NOSTUFF 5% 402
R2752 0 NO STUFF 5% 1/16W MF-LF 402
R2754 0 5% 1/16W MF-LF 402
R2758 330K 5% 1/16W MF-LF 402
R2756 0 5% 1/16W MF-LF 402
R2762 24 5% 1/16W MF-LF 402 NOSTUFF
R2764 24 5% 1/16W MF-LF 402 NOSTUFF
J2700 U.FL-R-SMT F-ST-SM NOSTUFF
Y2701 25.0000M CRITICAL 8X4.5MM-SM
C2707 33PF 5% 50V CERM 402
C2705 33PF 5% 50V CERM 402

R2701 0 5% 3.3V 33MHZ PCI_CLK_GP0
R2761 0 5% 402 3.3V 33MHZ PCI_CLK_GP1
C2708 0.001UF 50V 10% 2CERM 402
C2710 0.001UF 50V 10% 2CERM 402
C2713 0.001UF 50V 10% 2CERM 402
C2715 0.001UF 50V 10% 2CERM 402
C2700 0.001UF 50V 10% 2CERM 402
C2702 0.001UF 50V 10% 2CERM 402

VSP_NB_CLK_P
VSP_NB_CLK_N
EI_CPU_CLK_P
EI_CPU_CLK_N
EI_NB_CLK_P
EI_NB_CLK_N

R2775	0	NOSTUFF	2.5V 66MHZ	TP_PLS_CLK_66M_0
R2776	0		2.5V 66MHZ	TP_PLS_CLK_66M_1
R2703	20		2.5V 66MHZ	HT_CLK66M_NB
R2709	20		2.5V 66MHZ	RAM_CLK66M_NB
R2705	0		3.3V 66MHZ	PCI_CLK66M_SB_INT
R2711	0		3.3V 33MHZ	PCI_CLK_P1
R2707	0		3.3V 66MHZ	AGP_CLK66M_GPU
R2702	0		3.3V 33MHZ	PCI_CLK_P3
R2779	0			PCI_CLK_P4
R2715	0		1.2V 33MHZ	CPU_HTBEN
R2768	0	NOSTUFF	1.2V	EI_NB_SYNC
R2772	0		1.2V	EI_CPU_SYNC
R2770	20	NOSTUFF	2.5V 25MHZ	SB_CLK25M_ATA
R2700	22		2.5V 25MHZ	TP_SATA_CLK25M
R2720	0		SYS_SLEWING_L	
R2717	0		1.2V 66MHZ	HT_CLK66M_SB
R2719	0		1.5V 66MHZ	AGP_CLK66M_NB

PULSAR CLOCKS

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 27 OF 102	

=PP1V2_EI_NB

C2800 C2801 C2802 C2803 C2804 C2805 C2806 C2807 C2808 C2809 C2810 C2811 C2812 C2813 C2814 C2815 C2816 C2817
0.1UF 20% 100V CERM 402

=PP1V5_PWRON_NB_AVDD

R2800
2.2
5% 1/10W MF-LF 603

PP1V5_PWRON_EI_NB_AVDD
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

C2818 1UF 10% 6.3V CERM 402
C2819 0.1UF 20% 10V CERM 402

=PP1V2_EI_NB

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CAD	EI_CPU_TO_NB_AD	
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_CAD	EI_NB_TO_CPU_AD	
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_CPU_TO_NB_SR0	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_CPU_TO_NB_SR1	EI_CPU_TO_NB_SR1
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR1
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1

U3 U3LITE V1.0-300MM PBGA (SYM 1 OF 7) OMIT

APPLE PI INTERFACE

EI_NB_TO_CPU_CLK_P	F15	APIO_BCLKIP	APIO_BCLKOP D6 EI_CPU_TO_NB_CLK_P
EI_NB_TO_CPU_CLK_N	E15	APIO_BCLKIN	APIO_BCLKON E6 EI_CPU_TO_NB_CLK_N
EI_NB_TO_CPU_AD<0>	F11	APIO_ADI0	APIO_ADO0 J2 EI_CPU_TO_NB_AD<0>
EI_NB_TO_CPU_AD<1>	F12	APIO_ADI1	APIO_ADO1 H1 EI_CPU_TO_NB_AD<1>
EI_NB_TO_CPU_AD<2>	G11	APIO_ADI2	APIO_ADO2 J1 EI_CPU_TO_NB_AD<2>
EI_NB_TO_CPU_AD<3>	H11	APIO_ADI3	APIO_ADO3 K1 EI_CPU_TO_NB_AD<3>
EI_NB_TO_CPU_AD<4>	G12	APIO_ADI4	APIO_ADO4 E1 EI_CPU_TO_NB_AD<4>
EI_NB_TO_CPU_AD<5>	H12	APIO_ADI5	APIO_ADO5 F2 EI_CPU_TO_NB_AD<5>
EI_NB_TO_CPU_AD<6>	H14	APIO_ADI6	APIO_ADO6 J4 EI_CPU_TO_NB_AD<6>
EI_NB_TO_CPU_AD<7>	G14	APIO_ADI7	APIO_ADO7 H4 EI_CPU_TO_NB_AD<7>
EI_NB_TO_CPU_AD<8>	D9	APIO_ADI8	APIO_ADO8 G1 EI_CPU_TO_NB_AD<8>
EI_NB_TO_CPU_AD<9>	C9	APIO_ADI9	APIO_ADO9 H2 EI_CPU_TO_NB_AD<9>
EI_NB_TO_CPU_AD<10>	D11	APIO_ADI10	APIO_ADO10 F1 EI_CPU_TO_NB_AD<10>
EI_NB_TO_CPU_AD<11>	E11	APIO_ADI11	APIO_ADO11 H5 EI_CPU_TO_NB_AD<11>
EI_NB_TO_CPU_AD<12>	A10	APIO_ADI12	APIO_ADO12 H3 EI_CPU_TO_NB_AD<12>
EI_NB_TO_CPU_AD<13>	A9	APIO_ADI13	APIO_ADO13 J3 EI_CPU_TO_NB_AD<13>
EI_NB_TO_CPU_AD<14>	A8	APIO_ADI14	APIO_ADO14 J5 EI_CPU_TO_NB_AD<14>
EI_NB_TO_CPU_AD<15>	B9	APIO_ADI15	APIO_ADO15 J6 EI_CPU_TO_NB_AD<15>
EI_NB_TO_CPU_AD<16>	C11	APIO_ADI16	APIO_ADO16 E3 EI_CPU_TO_NB_AD<16>
EI_NB_TO_CPU_AD<17>	B11	APIO_ADI17	APIO_ADO17 F4 EI_CPU_TO_NB_AD<17>
EI_NB_TO_CPU_AD<18>	A11	APIO_ADI18	APIO_ADO18 E2 EI_CPU_TO_NB_AD<18>
EI_NB_TO_CPU_AD<19>	A12	APIO_ADI19	APIO_ADO19 F5 EI_CPU_TO_NB_AD<19>
EI_NB_TO_CPU_AD<20>	B12	APIO_ADI20	APIO_ADO20 H6 EI_CPU_TO_NB_AD<20>
EI_NB_TO_CPU_AD<21>	C12	APIO_ADI21	APIO_ADO21 J7 EI_CPU_TO_NB_AD<21>
EI_NB_TO_CPU_AD<22>	D12	APIO_ADI22	APIO_ADO22 F3 EI_CPU_TO_NB_AD<22>
EI_NB_TO_CPU_AD<23>	E12	APIO_ADI23	APIO_ADO23 J8 EI_CPU_TO_NB_AD<23>
EI_NB_TO_CPU_AD<24>	A13	APIO_ADI24	APIO_ADO24 F6 EI_CPU_TO_NB_AD<24>
EI_NB_TO_CPU_AD<25>	A14	APIO_ADI25	APIO_ADO25 E5 EI_CPU_TO_NB_AD<25>
EI_NB_TO_CPU_AD<26>	B14	APIO_ADI26	APIO_ADO26 D5 EI_CPU_TO_NB_AD<26>
EI_NB_TO_CPU_AD<27>	C14	APIO_ADI27	APIO_ADO27 E4 EI_CPU_TO_NB_AD<27>
EI_NB_TO_CPU_AD<28>	A16	APIO_ADI28	APIO_ADO28 D8 EI_CPU_TO_NB_AD<28>
EI_NB_TO_CPU_AD<29>	A15	APIO_ADI29	APIO_ADO29 A5 EI_CPU_TO_NB_AD<29>
EI_NB_TO_CPU_AD<30>	B15	APIO_ADI30	APIO_ADO30 C2 EI_CPU_TO_NB_AD<30>
EI_NB_TO_CPU_AD<31>	C15	APIO_ADI31	APIO_ADO31 C3 EI_CPU_TO_NB_AD<31>
EI_NB_TO_CPU_AD<32>	H15	APIO_ADI32	APIO_ADO32 C5 EI_CPU_TO_NB_AD<32>
EI_NB_TO_CPU_AD<33>	G15	APIO_ADI33	APIO_ADO33 C6 EI_CPU_TO_NB_AD<33>
EI_NB_TO_CPU_AD<34>	F17	APIO_ADI34	APIO_ADO34 B2 EI_CPU_TO_NB_AD<34>
EI_NB_TO_CPU_AD<35>	G17	APIO_ADI35	APIO_ADO35 D1 EI_CPU_TO_NB_AD<35>
EI_NB_TO_CPU_AD<36>	G18	APIO_ADI36	APIO_ADO36 B1 EI_CPU_TO_NB_AD<36>
EI_NB_TO_CPU_AD<37>	H18	APIO_ADI37	APIO_ADO37 C1 EI_CPU_TO_NB_AD<37>
EI_NB_TO_CPU_AD<38>	F18	APIO_ADI38	APIO_ADO38 A6 EI_CPU_TO_NB_AD<38>
EI_NB_TO_CPU_AD<39>	E18	APIO_ADI39	APIO_ADO39 C8 EI_CPU_TO_NB_AD<39>
EI_NB_TO_CPU_AD<40>	A17	APIO_ADI40	APIO_ADO40 A2 EI_CPU_TO_NB_AD<40>
EI_NB_TO_CPU_AD<41>	A18	APIO_ADI41	APIO_ADO41 B3 EI_CPU_TO_NB_AD<41>
EI_NB_TO_CPU_AD<42>	B17	APIO_ADI42	APIO_ADO42 A7 EI_CPU_TO_NB_AD<42>
EI_NB_TO_CPU_AD<43>	C17	APIO_ADI43	APIO_ADO43 B8 EI_CPU_TO_NB_AD<43>
EI_NB_TO_CPU_SR_P<0>	D17	APIO_SRIP0	APIO_SROP0 A3 EI_CPU_TO_NB_SR_P<0>
EI_NB_TO_CPU_SR_N<0>	A19	APIO_SRIN0	APIO_SRON0 A4 EI_CPU_TO_NB_SR_N<0>
EI_NB_TO_CPU_SR_P<1>	E17	APIO_SRIP1	APIO_SROP1 B5 EI_CPU_TO_NB_SR_P<1>
EI_NB_TO_CPU_SR_N<1>	B18	APIO_SRIN1	APIO_SRON1 B6 EI_CPU_TO_NB_SR_N<1>
EI_QACK_L	D14	API_QACK0	API_QREQ0 E14
	E8	APIO_APSYNC	
	H17	APIO_SE	API_APCLKP D18 EI_NB_CLK_P
			API_APCLKN C18 EI_NB_CLK_N
			API_CSTP F14 CPU_CHKSTOP_L

PLACE R2805 AND R2806 NEAR U3LITE

R2805 0 5% 1/16W MF-LF 402
R2806 10 5% 1/16W MF-LF 402

EI_NB_SYNC → NB_APSYNC
EI_SYNC_FROM_NB
EI_SE

API_APCLK_AVSS

QREQ_L HACK

=PP3V3_PWRON_EI

C2850 0.1UF 10% 10V CERM 402

CRITICAL
U2850 74LVC1G66DBVG4 SOT23-5 TI

EI_QREQ_L → VCC
SMU_SUSPENDREQ_L → GND
EI_NB_QREQ_L

R2850 NOSTUFF 0 5% 1/16W MF-LF 402

R2851 10K 5% 1/16W MF-LF 402

PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U2850	PERICOM ANALOG SWITCH CRITICAL

QREQ TO SMU

=PP3V3_PWRON_EI

R2898 10K 5% 1/16W MF-LF 402

R2899 180 5% 1/16W MF-LF 402

EI_NB_QREQ_L_R

SMU_QREQ

Q2899 2N3904LF SOT23

=PP1V2_EI_NB

R2802 100 1% 1/16W MF-LF 402

C2821 0.001UF 10% 50V CERM 402

EI_APCLK_VREF VOLTAGE=0.6V

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

R2801 100 1% 1/16W MF-LF 402
C2820 0.1UF 20% 10V CERM 402
R2803 121 1% 1/16W MF-LF 402
R2804 121 1% 1/16W MF-LF 402

EI_NB_CLK_P
EI_NB_CLK_N

ZT2847 ZT2857 ZT2867 ZT2807 ZT2817 ZT2827 ZT2837
ZT2848 ZT2858 ZT2868 ZT2808 ZT2818 ZT2828 ZT2838
ZT2849 ZT2859 ZT2869 ZT2809 ZT2819 ZT2829 ZT2839
ZT2850 ZT2860 ZT2800 ZT2810 ZT2820 ZT2830 ZT2840
ZT2851 ZT2861 ZT2801 ZT2811 ZT2821 ZT2831 ZT2841
ZT2852 ZT2862 ZT2802 ZT2812 ZT2822 ZT2832 ZT2842
ZT2853 ZT2863 ZT2803 ZT2813 ZT2823 ZT2833 ZT2843
ZT2854 ZT2864 ZT2804 ZT2814 ZT2824 ZT2834 ZT2844
ZT2855 ZT2865 ZT2805 ZT2815 ZT2825 ZT2835 ZT2845
ZT2806 ZT2816 ZT2826 ZT2836
ZT2846 ZT2856 ZT2866

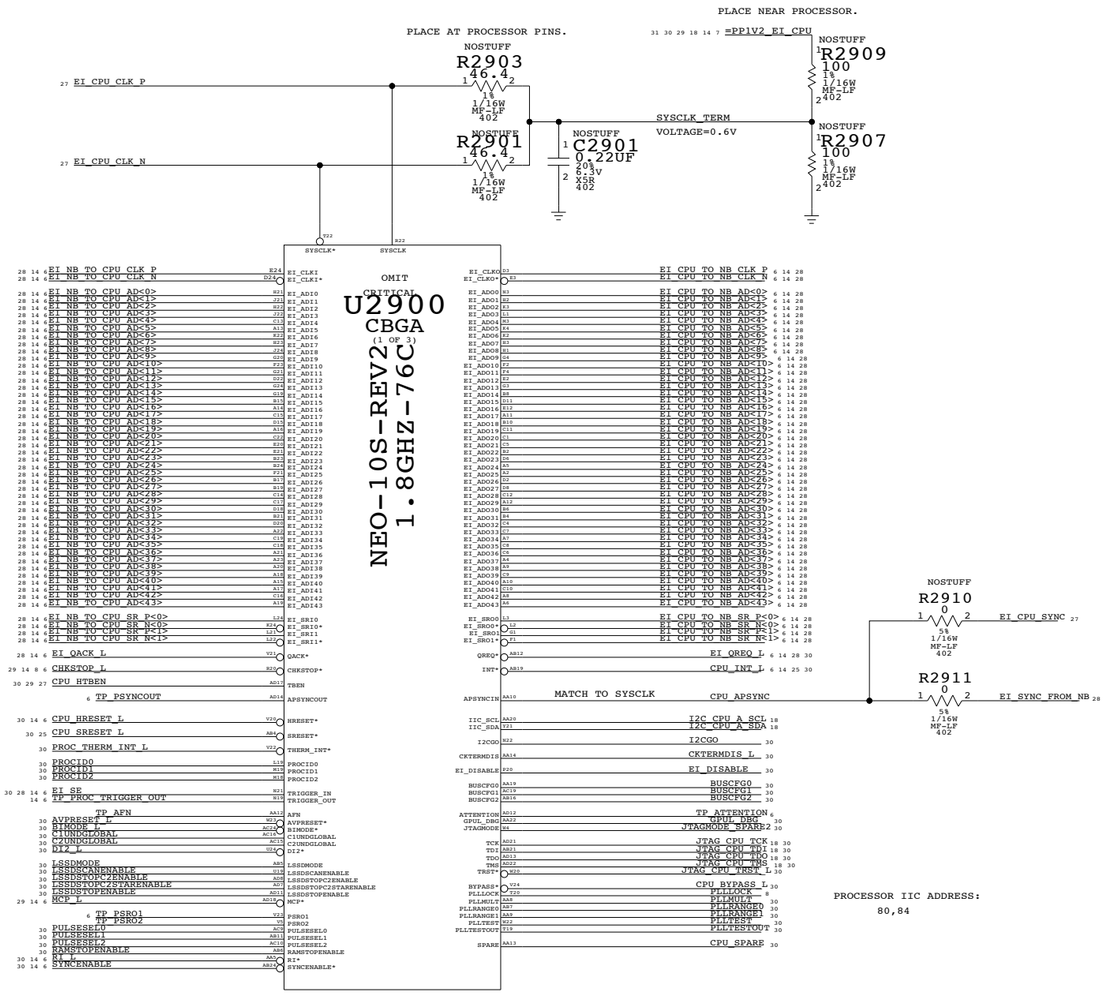
All: OMIT HOLE-VIA-20R10

U3LITE APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 28 OF 102	



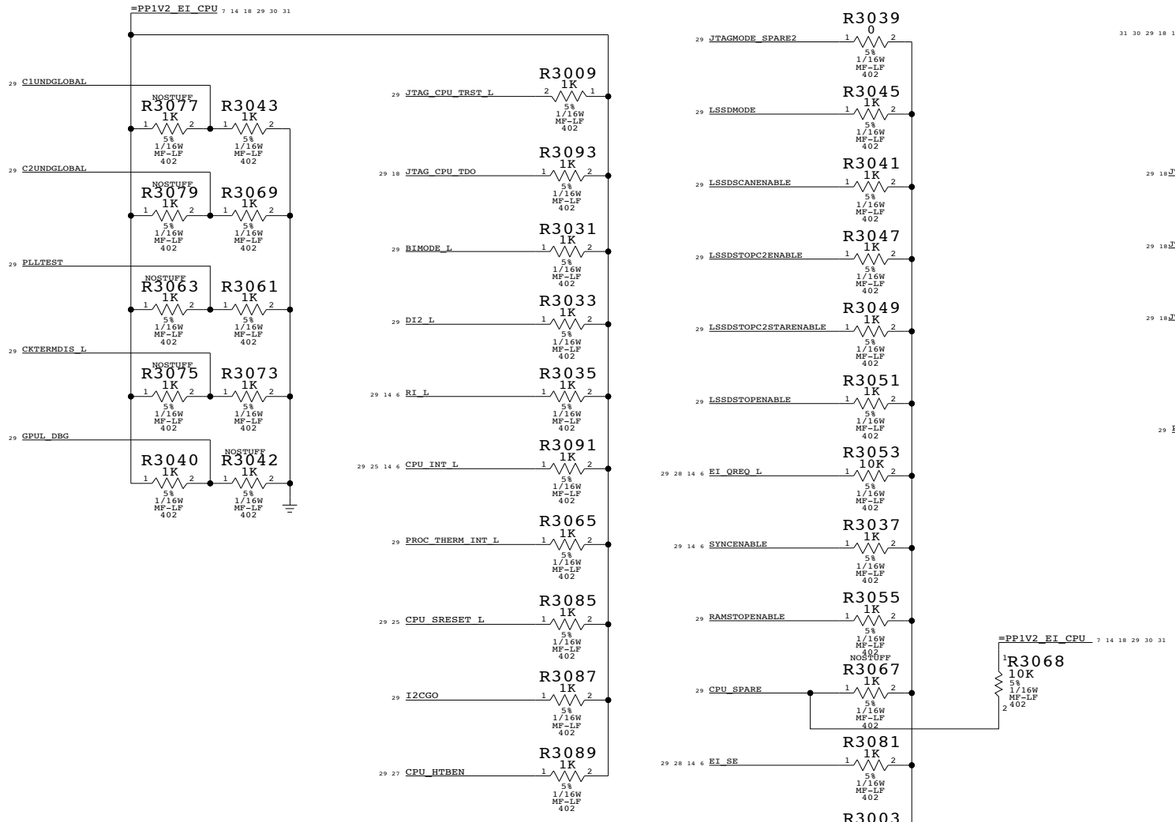
PROCESSOR LOGIC I/O

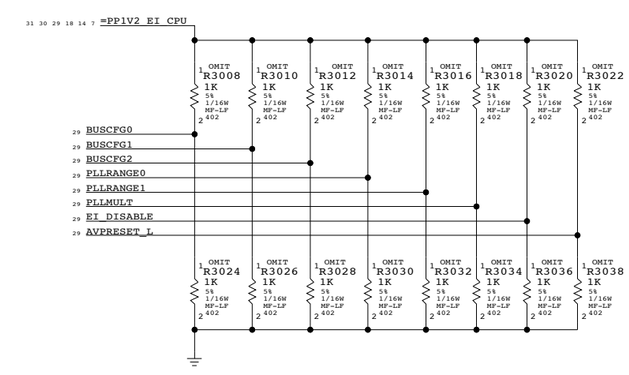
NEO APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 29 OF 102	





SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
>= 1.8 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	
<= 1.6 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

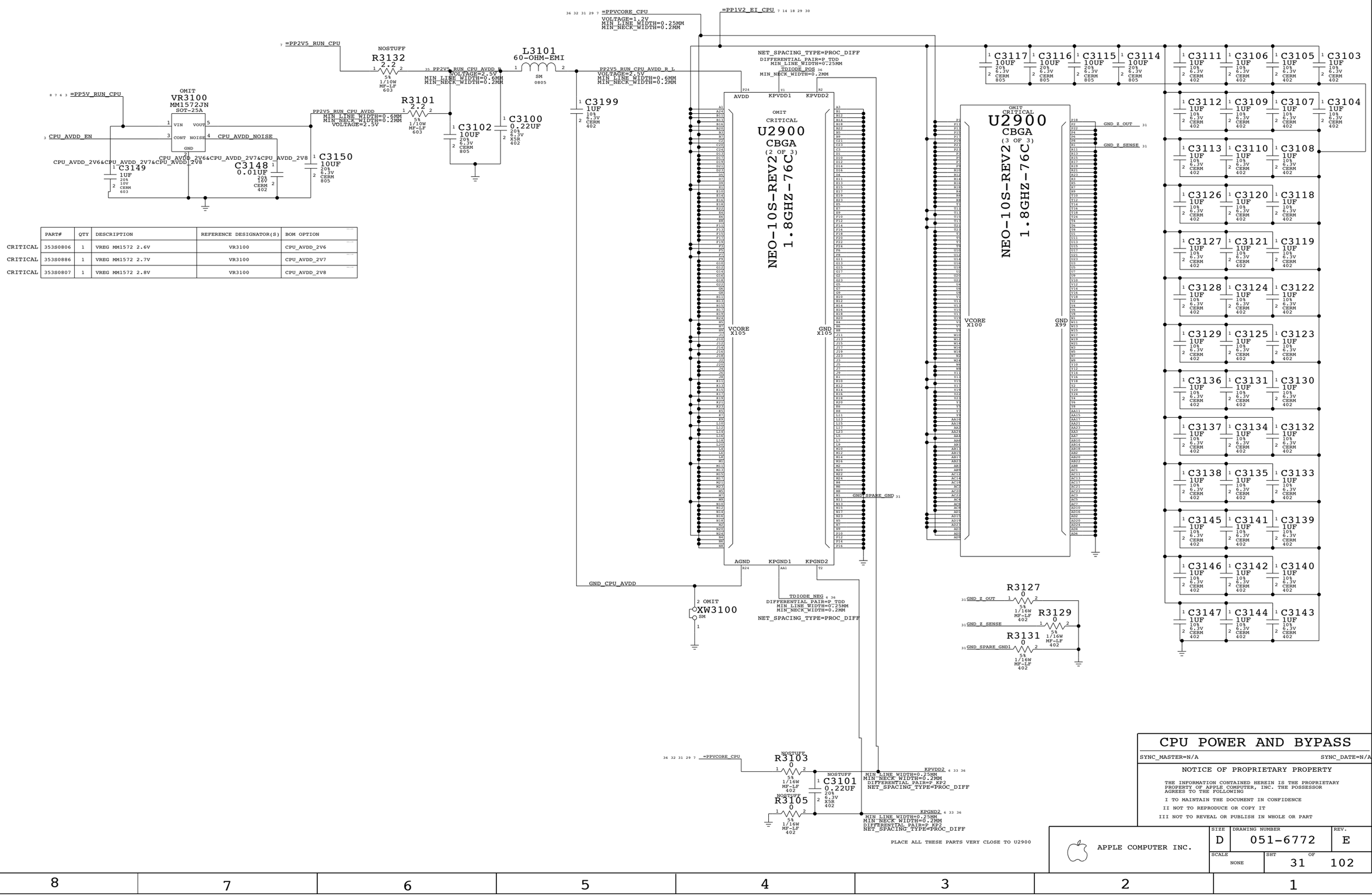
SYSTEM CONFIGURATION

CPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 30 OF 102	



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL	353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

CPU POWER AND BYPASS

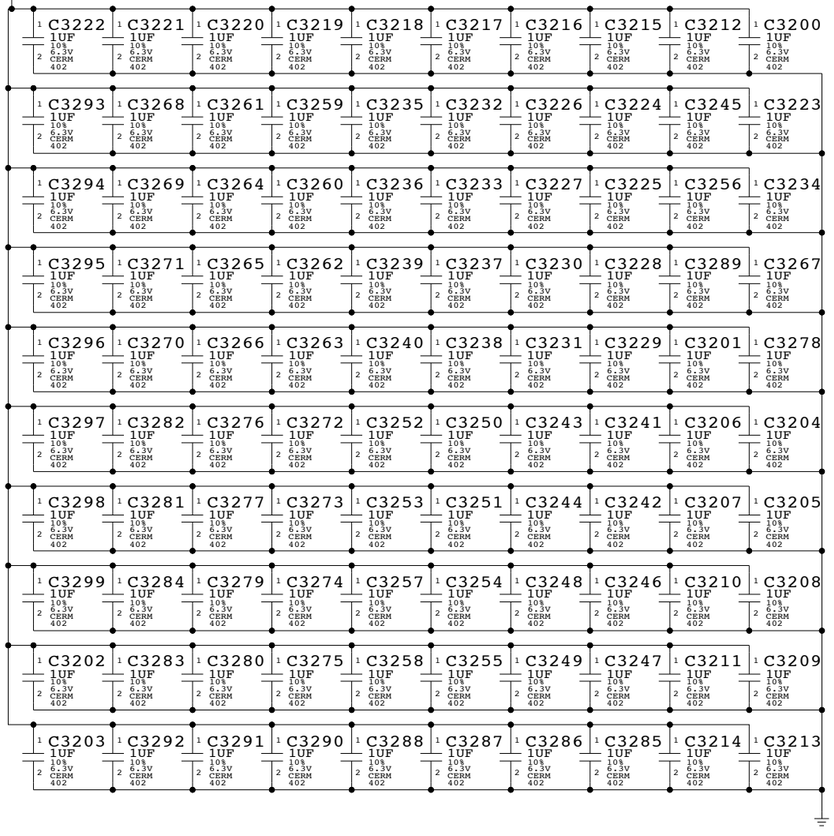
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	31	102

36 31 29 7 =PPVCORE_CPU

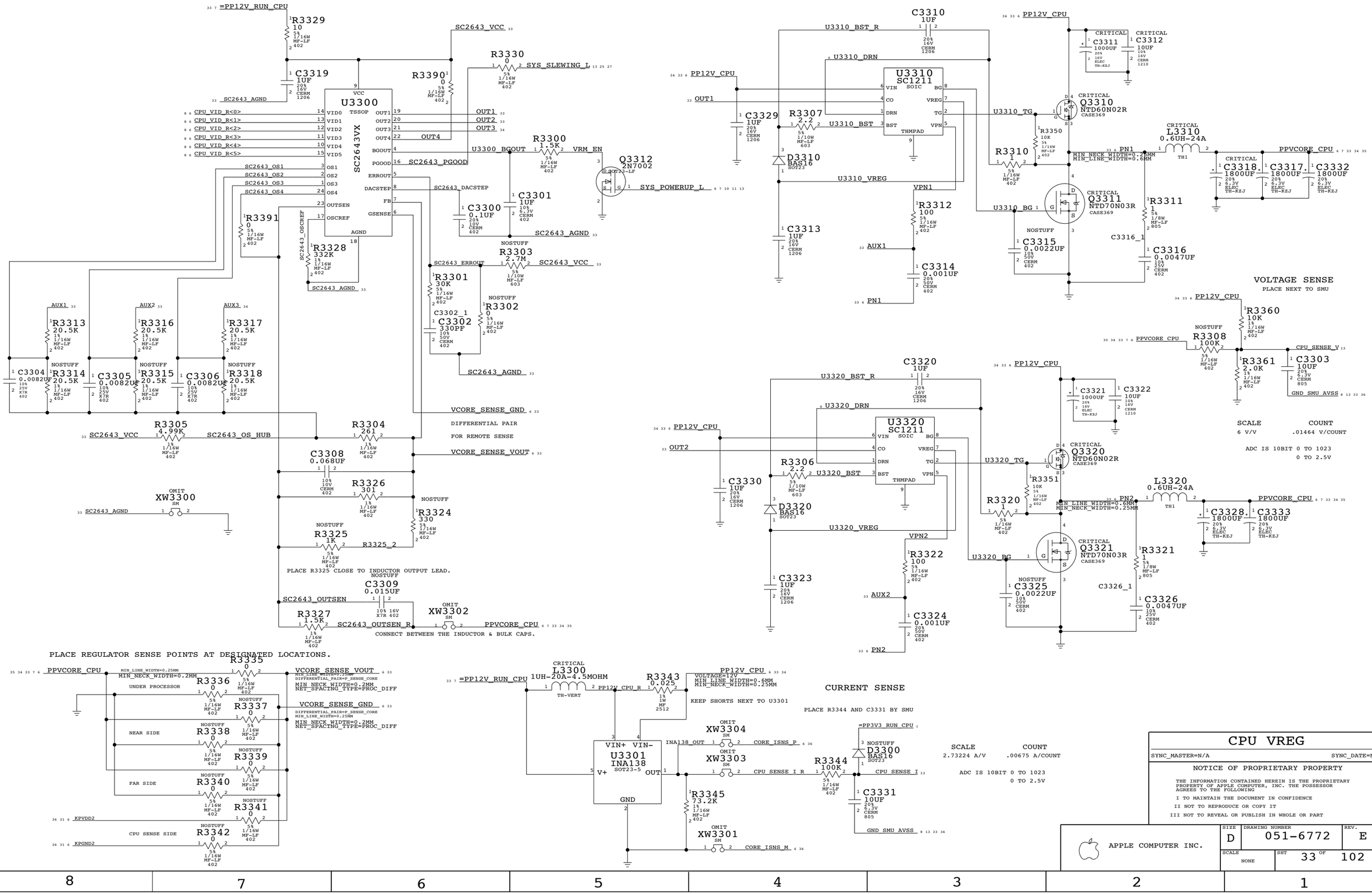


PROC DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 32 OF 102	


=PP12V_RUN_CPU
R3329 10 5% 1/16W MF-LF 402
C3319 1UF 20% 16V CERM 1206
SC2643_AGND
SC2643_VCC
R3330 0 5% 1/16W MF-LF 402
SYS_SLEWING_L
R3390 0 5% 1/16W MF-LF 402
U3300
SC2643VX
VCC
TSSOP
CPU_VID_R<0>
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VID0
VID1
VID2
VID3
VID4
VID5
OUT1
OUT2
OUT3
OUT4
BGOUT
PGOOD
EROUT
DACSTEP
FB
GSENSE
OUTSEN
OSCREF
AGND
SC2643_PGOOD
SC2643_DACSTEP
SC2643_ERROUT
SC2643_OS1
SC2643_OS2
SC2643_OS3
SC2643_OS4
SC2643_OSCREF
SC2643_OUTSEN
R3300 1.5K 5% 1/16W MF-LF 402
U3300_BGOUT
VRM_EN
Q3312 2N7002 SOT23-LF
SYS_POWERUP_L
C3300 0.1UF 20% 10V CERM 402
C3301 1UF 10% 6.3V CERM 402
R3303 2.7M 5% 1/10W MF-LF 603
R3301 30K 5% 1/16W MF-LF 402
R3302 0 5% 1/16W MF-LF 402
C3302_1
C3302 330PF 10% 50V CERM 402
R3328 332K 1% 1/16W MF-LF 402
R3391 0 5% 1/16W MF-LF 402
AUX1
AUX2
AUX3
R3313 20.5K 1% 1/16W MF-LF 402
R3314 20.5K 1% 1/16W MF-LF 402
R3316 20.5K 1% 1/16W MF-LF 402
R3315 20.5K 1% 1/16W MF-LF 402
R3317 20.5K 1% 1/16W MF-LF 402
R3318 20.5K 1% 1/16W MF-LF 402
NOSTUFF
C3304 0.0082UF 10% 25V X7R 402
C3305 0.0082UF 10% 25V X7R 402
C3306 0.0082UF 10% 25V X7R 402
R3305 4.99K 1% 1/16W MF-LF 402
R3304 261 1% 1/16W MF-LF 402
C3308 0.068UF 10% 10V CERM 402
R3326 301 1% 1/16W MF-LF 402
R3324 330 5% 1/16W MF-LF 402
R3325 1K 5% 1/16W MF-LF 402
R3325_2
PLACE R3325 CLOSE TO INDUCTOR OUTPUT LEAD.
C3309 0.015UF 10% 16V X7R 402
R3327 1.5K 1% 1/16W MF-LF 402
SC2643_OUTSEN_R
OMIT XW3302 SM
PPVCORE_CPU
CONNECT BETWEEN THE INDUCTOR & BULK CAPS.
OMIT XW3300 SM
VCORE_SENSE_GND
DIFFERENTIAL PAIR
FOR REMOTE SENSE
VCORE_SENSE_VOUT
C3310 1UF 20% 16V CERM 1206
U3310_BST_R
U3310_DRN
U3310 SC1211 SOIC THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
U3310_TG
U3310_BST
U3310_VREG
PP12V_CPU
OUT1
C3329 1UF 20% 16V CERM 1206
R3307 2.2 5% 1/10W MF-LF 603
D3310 BAS16 SOT23
C3313 1UF 20% 16V CERM 1206
VPN1
R3312 100 5% 1/16W MF-LF 402
AUX1
C3314 0.001UF 20% 50V CERM 402
PN1
CRITICAL Q3310 NTD60N02R CASE369
CRITICAL C3311 1000UF 20% 16V ELEC TH-KZJ
CRITICAL C3312 10UF 10% 16V CERM 1210
R3350 10K 5% 1/16W MF-LF 402
R3310 1 5% 1/16W MF-LF 402
CRITICAL L3310 0.6UH-24A TH1
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
CRITICAL C3318 1800UF 20% 6.3V ELEC TH-KZJ
CRITICAL C3317 1800UF 20% 6.3V ELEC TH-KZJ
C3332 1800UF 20% 6.3V ELEC TH-KZJ
PPVCORE_CPU
U3310_BG
CRITICAL Q3311 NTD70N03R CASE369
R3311 1 5% 1/8W MF-LF 805
C3315 0.0022UF 10% 50V CERM 402
C3316_1
C3316 0.0047UF 10% 25V CERM 402
VOLTAGE SENSE
PLACE NEXT TO SMU
R3360 10K 1% 1/16W MF-LF 402
R3308 100K 5% 1/16W MF-LF 402
R3361 2.0K 1% 1/16W MF-LF 402
CPU_SENSE_V
C3303 10UF 20% 6.3V CERM 805
GND_SMU_AVSS
SCALE 6 V/V
COUNT .01464 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
C3320 1UF 20% 16V CERM 1206
U3320_BST_R
U3320_DRN
U3320 SC1211 SOIC THMPAD
U3320_TG
U3320_BST
U3320_VREG
U3320_BG
OUT2
C3330 1UF 20% 16V CERM 1206
R3306 2.2 5% 1/10W MF-LF 603
D3320 BAS16 SOT23
C3323 1UF 20% 16V CERM 1206
VPN2
R3322 100 5% 1/16W MF-LF 402
AUX2
C3324 0.001UF 20% 50V CERM 402
PN2
CRITICAL Q3320 NTD60N02R CASE369
CRITICAL C3321 1000UF 20% 16V ELEC TH-KZJ
C3322 10UF 10% 16V CERM 1210
R3351 10K 5% 1/16W MF-LF 402
R3320 1 5% 1/16W MF-LF 402
L3320 0.6UH-24A TH1
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
C3328 1800UF 20% 6.3V ELEC TH-KZJ
C3333 1800UF 20% 6.3V ELEC TH-KZJ
CRITICAL Q3321 NTD70N03R CASE369
R3321 1 5% 1/8W MF-LF 805
C3325 0.0022UF 10% 50V CERM 402
C3326_1
C3326 0.0047UF 10% 25V CERM 402
PLACE REGULATOR SENSE POINTS AT DESIGNATED LOCATIONS.
PPVCORE_CPU
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
UNDER PROCESSOR
NEAR SIDE
FAR SIDE
CPU SENSE SIDE
R3335 0 5% 1/16W MF-LF 402
R3336 0 5% 1/16W MF-LF 402
R3337 0 5% 1/16W MF-LF 402
R3338 0 5% 1/16W MF-LF 402
R3339 0 5% 1/16W MF-LF 402
R3340 0 5% 1/16W MF-LF 402
R3341 0 5% 1/16W MF-LF 402
R3342 0 5% 1/16W MF-LF 402
KPVDD2
KPGND2
VCORE_SENSE_VOUT
VCORE_SENSE_GND
DIFFERENTIAL_PAIR=P_SENSE_CORE
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PROC_DIFF
CURRENT SENSE
PLACE R3344 AND C3331 BY SMU
CRITICAL L3300 1UH-20A-4.5MOHM TH-VERT
=PP12V_RUN_CPU
PP12V_CPU_R
R3343 0.025 1% 1W MF 2512
PP12V_CPU
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
KEEP SHORTS NEXT TO U3301
U3301 INA138 SOT23-5
VIN+ VIN- V+ OUT GND
INA138_OUT
OMIT XW3304 SM
OMIT XW3303 SM
CPU_SENSE_I_R
R3345 73.2K 1% 1/16W MF-LF 402
OMIT XW3301 SM
CORE_ISNS_M
CORE_ISNS_P
=PP3V3_RUN_CPU
D3300 BAS16 SOT23
R3344 100K 5% 1/16W MF-LF 402
CPU_SENSE_I
C3331 10UF 20% 6.3V CERM 805
GND_SMU_AVSS
SCALE 2.73224 A/V
COUNT .00675 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
CPU VREG
SYNC_MASTER=N/A
SYNC_DATE=N/A
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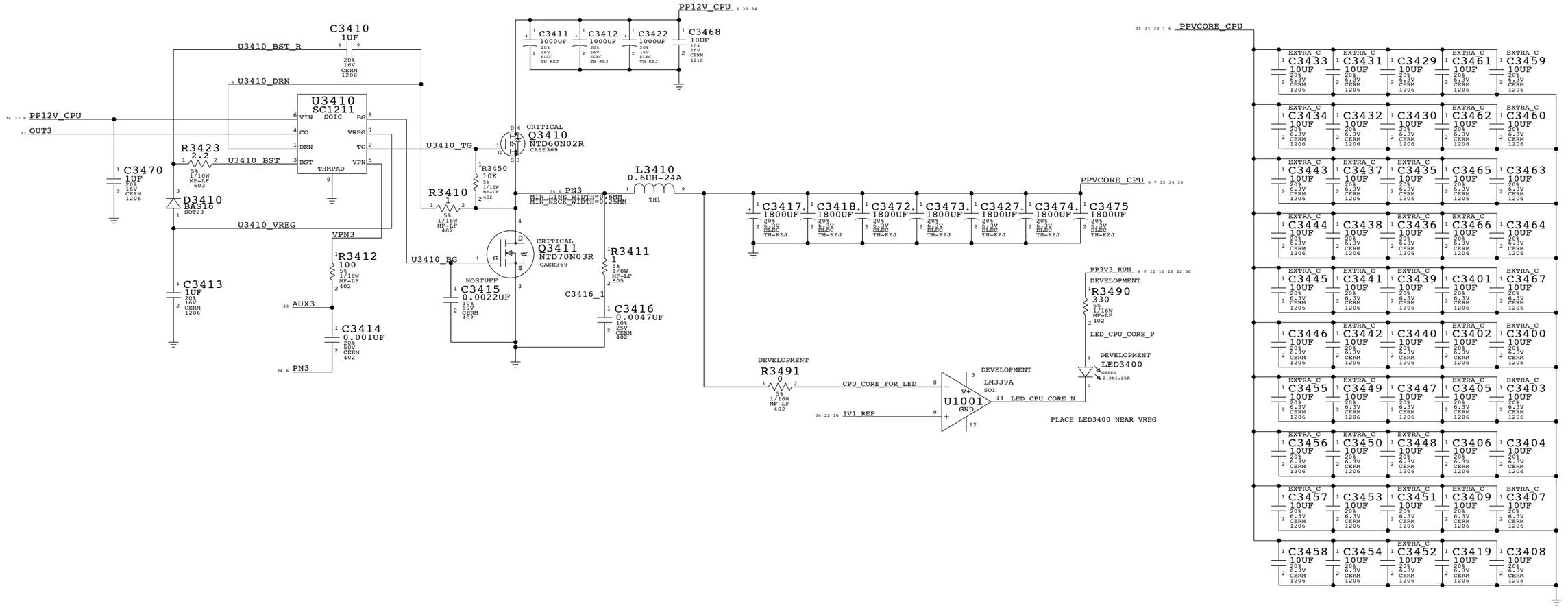
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6772
REV. E
SCALE NONE
SHT 33 OF 102



CPU VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE NONE SHT 34 OF 102

35 34 33 7 6 PPVCORE_CPU

DS3502
SMB
1 2
10BQ040PBF

35 PP2V5_RUN_CPU_AVDD_R

35 34 33 7 6 PPVCORE_CPU

CRITICAL

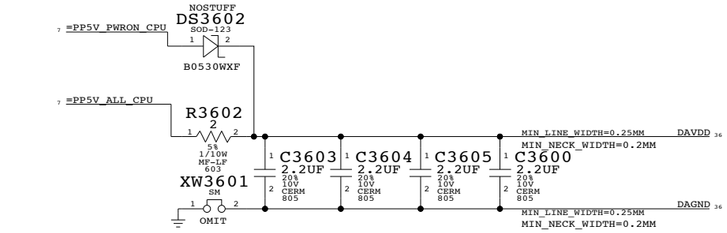
EXTRA_C C3500 10UF 20% 6.3V CERM 1206	EXTRA_C C3512 10UF 20% 6.3V CERM 1206	EXTRA_C C3523 10UF 20% 6.3V CERM 1206	EXTRA_C C3534 10UF 20% 6.3V CERM 1206	EXTRA_C C3545 10UF 20% 6.3V CERM 1206	EXTRA_C C3501 10UF 20% 6.3V CERM 1206	EXTRA_C C3589 10UF 20% 6.3V CERM 1206	EXTRA_C C3578 10UF 20% 6.3V CERM 1206	EXTRA_C C3567 10UF 20% 6.3V CERM 1206	EXTRA_C C3556 10UF 20% 6.3V CERM 1206
EXTRA_C C3513 10UF 20% 6.3V CERM 1206	EXTRA_C C3511 10UF 20% 6.3V CERM 1206	EXTRA_C C3510 10UF 20% 6.3V CERM 1206	EXTRA_C C3509 10UF 20% 6.3V CERM 1206	EXTRA_C C3508 10UF 20% 6.3V CERM 1206	EXTRA_C C3507 10UF 20% 6.3V CERM 1206	EXTRA_C C3506 10UF 20% 6.3V CERM 1206	EXTRA_C C3505 10UF 20% 6.3V CERM 1206	EXTRA_C C3504 10UF 20% 6.3V CERM 1206	EXTRA_C C3503 10UF 20% 6.3V CERM 1206
EXTRA_C C3524 10UF 20% 6.3V CERM 1206	EXTRA_C C3522 10UF 20% 6.3V CERM 1206	EXTRA_C C3521 10UF 20% 6.3V CERM 1206	EXTRA_C C3520 10UF 20% 6.3V CERM 1206	EXTRA_C C3519 10UF 20% 6.3V CERM 1206	EXTRA_C C3518 10UF 20% 6.3V CERM 1206	EXTRA_C C3517 10UF 20% 6.3V CERM 1206	EXTRA_C C3516 10UF 20% 6.3V CERM 1206	EXTRA_C C3515 10UF 20% 6.3V CERM 1206	EXTRA_C C3514 10UF 20% 6.3V CERM 1206
EXTRA_C C3535 10UF 20% 6.3V CERM 1206	EXTRA_C C3533 10UF 20% 6.3V CERM 1206	EXTRA_C C3532 10UF 20% 6.3V CERM 1206	EXTRA_C C3531 10UF 20% 6.3V CERM 1206	EXTRA_C C3530 10UF 20% 6.3V CERM 1206	EXTRA_C C3529 10UF 20% 6.3V CERM 1206	EXTRA_C C3528 10UF 20% 6.3V CERM 1206	EXTRA_C C3527 10UF 20% 6.3V CERM 1206	EXTRA_C C3526 10UF 20% 6.3V CERM 1206	EXTRA_C C3525 10UF 20% 6.3V CERM 1206
EXTRA_C C3546 10UF 20% 6.3V CERM 1206	EXTRA_C C3544 10UF 20% 6.3V CERM 1206	EXTRA_C C3543 10UF 20% 6.3V CERM 1206	EXTRA_C C3542 10UF 20% 6.3V CERM 1206	EXTRA_C C3541 10UF 20% 6.3V CERM 1206	EXTRA_C C3540 10UF 20% 6.3V CERM 1206	EXTRA_C C3539 10UF 20% 6.3V CERM 1206	EXTRA_C C3538 10UF 20% 6.3V CERM 1206	EXTRA_C C3537 10UF 20% 6.3V CERM 1206	EXTRA_C C3536 10UF 20% 6.3V CERM 1206
EXTRA_C C3557 10UF 20% 6.3V CERM 1206	EXTRA_C C3555 10UF 20% 6.3V CERM 1206	EXTRA_C C3554 10UF 20% 6.3V CERM 1206	EXTRA_C C3553 10UF 20% 6.3V CERM 1206	EXTRA_C C3552 10UF 20% 6.3V CERM 1206	EXTRA_C C3551 10UF 20% 6.3V CERM 1206	EXTRA_C C3550 10UF 20% 6.3V CERM 1206	EXTRA_C C3549 10UF 20% 6.3V CERM 1206	EXTRA_C C3548 10UF 20% 6.3V CERM 1206	EXTRA_C C3547 10UF 20% 6.3V CERM 1206
EXTRA_C C3568 10UF 20% 6.3V CERM 1206	EXTRA_C C3566 10UF 20% 6.3V CERM 1206	EXTRA_C C3565 10UF 20% 6.3V CERM 1206	EXTRA_C C3564 10UF 20% 6.3V CERM 1206	EXTRA_C C3563 10UF 20% 6.3V CERM 1206	EXTRA_C C3562 10UF 20% 6.3V CERM 1206	EXTRA_C C3561 10UF 20% 6.3V CERM 1206	EXTRA_C C3560 10UF 20% 6.3V CERM 1206	EXTRA_C C3559 10UF 20% 6.3V CERM 1206	EXTRA_C C3558 10UF 20% 6.3V CERM 1206
EXTRA_C C3579 10UF 20% 6.3V CERM 1206	EXTRA_C C3577 10UF 20% 6.3V CERM 1206	EXTRA_C C3576 10UF 20% 6.3V CERM 1206	EXTRA_C C3575 10UF 20% 6.3V CERM 1206	EXTRA_C C3574 10UF 20% 6.3V CERM 1206	EXTRA_C C3573 10UF 20% 6.3V CERM 1206	EXTRA_C C3572 10UF 20% 6.3V CERM 1206	EXTRA_C C3571 10UF 20% 6.3V CERM 1206	EXTRA_C C3570 10UF 20% 6.3V CERM 1206	EXTRA_C C3569 10UF 20% 6.3V CERM 1206
EXTRA_C C3590 10UF 20% 6.3V CERM 1206	EXTRA_C C3588 10UF 20% 6.3V CERM 1206	EXTRA_C C3587 10UF 20% 6.3V CERM 1206	EXTRA_C C3586 10UF 20% 6.3V CERM 1206	EXTRA_C C3585 10UF 20% 6.3V CERM 1206	EXTRA_C C3584 10UF 20% 6.3V CERM 1206	EXTRA_C C3583 10UF 20% 6.3V CERM 1206	EXTRA_C C3582 10UF 20% 6.3V CERM 1206	EXTRA_C C3581 10UF 20% 6.3V CERM 1206	EXTRA_C C3580 10UF 20% 6.3V CERM 1206
EXTRA_C C3502 10UF 20% 6.3V CERM 1206	EXTRA_C C3599 10UF 20% 6.3V CERM 1206	EXTRA_C C3598 10UF 20% 6.3V CERM 1206	EXTRA_C C3597 10UF 20% 6.3V CERM 1206	EXTRA_C C3596 10UF 20% 6.3V CERM 1206	EXTRA_C C3595 10UF 20% 6.3V CERM 1206	EXTRA_C C3594 10UF 20% 6.3V CERM 1206	EXTRA_C C3593 10UF 20% 6.3V CERM 1206	EXTRA_C C3592 10UF 20% 6.3V CERM 1206	EXTRA_C C3591 10UF 20% 6.3V CERM 1206

CPU VREG OUTPUT CAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

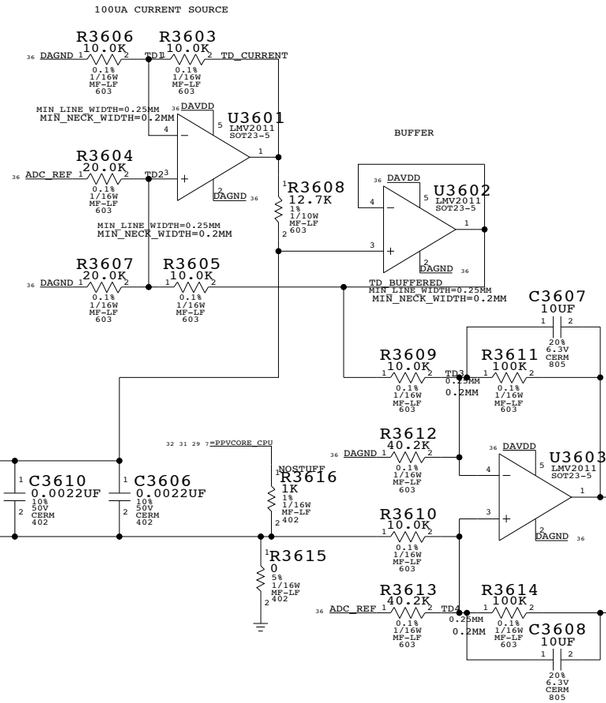
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 35 OF 102	

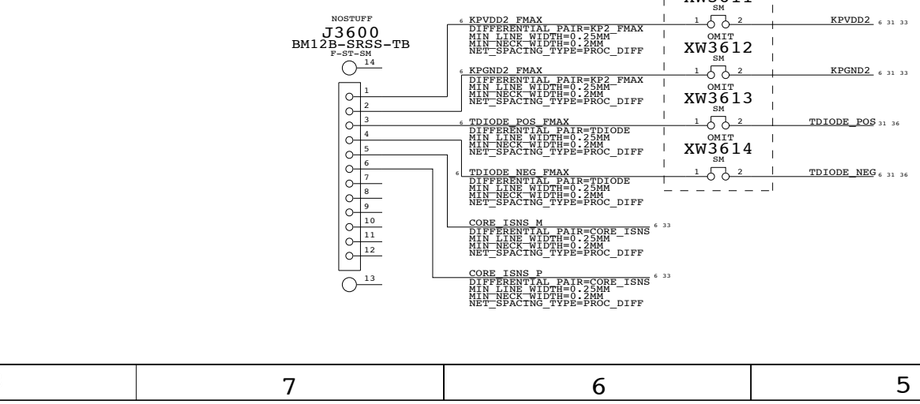


XW3600, R3602, AND DS3602 MUST BE PLACED CLOSE TO SMU

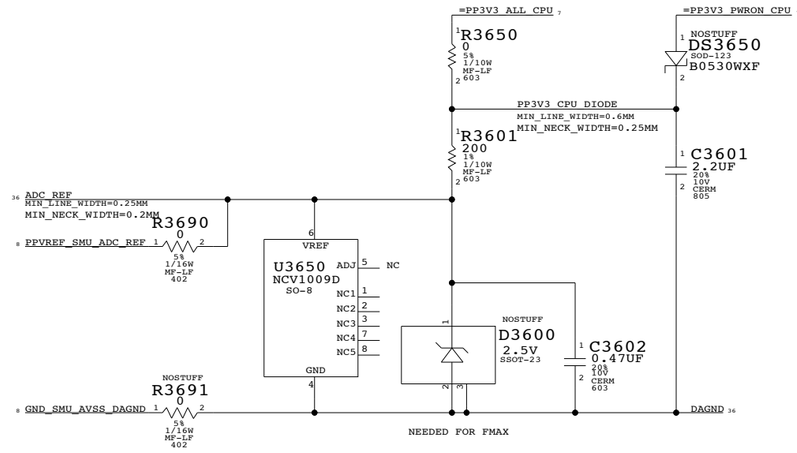
THESE SIGNALS HAVE A MIN_LINE_WIDTH=0.25MM
AND MIN_NECK_WIDTH=0.2MM



NEED TO CONNECT TO P65 OF 80PIN SMU OR PIN 49 OF 64PIN SMU



POWER MONITOR



CPU DIODE CONDITIONER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 36 OF 102	

U3TWINS DO NOT HAVE MASKS

=PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT

MEMORY DATA INTERFACE

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RAM_DQ_R<46>	C24	DDR_DQ46	DDR_DQ110 / J27 / RAM_DQ_R<110>
RAM_DQ_R<47>	C23	DDR_DQ47	DDR_DQ111 / L24 / RAM_DQ_R<111>
RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112 / J25 / RAM_DQ_R<112>
RAM_DQ_R<49>	B23	DDR_DQ49	DDR_DQ113 / J24 / RAM_DQ_R<113>
RAM_DQ_R<50>	A23	DDR_DQ50	DDR_DQ114 / J26 / RAM_DQ_R<114>
RAM_DQ_R<51>	A24	DDR_DQ51	DDR_DQ115 / G28 / RAM_DQ_R<115>
RAM_DQ_R<52>	A27	DDR_DQ52	DDR_DQ116 / H25 / RAM_DQ_R<116>
RAM_DQ_R<53>	A28	DDR_DQ53	DDR_DQ117 / H24 / RAM_DQ_R<117>
RAM_DQ_R<54>	B28	DDR_DQ54	DDR_DQ118 / F27 / RAM_DQ_R<118>
RAM_DQ_R<55>	A26	DDR_DQ55	DDR_DQ119 / H26 / RAM_DQ_R<119>
RAM_DQ_R<56>	F24	DDR_DQ56	DDR_DQ120 / E28 / RAM_DQ_R<120>
RAM_DQ_R<57>	J22	DDR_DQ57	DDR_DQ121 / E27 / RAM_DQ_R<121>
RAM_DQ_R<58>	E23	DDR_DQ58	DDR_DQ122 / F26 / RAM_DQ_R<122>
RAM_DQ_R<59>	H23	DDR_DQ59	DDR_DQ123 / E26 / RAM_DQ_R<123>
RAM_DQ_R<60>	J21	DDR_DQ60	DDR_DQ124 / D28 / RAM_DQ_R<124>
RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125 / C28 / RAM_DQ_R<125>
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126 / E25 / RAM_DQ_R<126>
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127 / E24 / RAM_DQ_R<127>

=PP1V5_PWRON_NB_AVDD

R3702 2.2 5% 1/10W MF-LF 603

PP1V5_PWRON_RAM_NB_AVDD VOLTAGE=1.5V

C3745 1UF 10% 6.3V CERM 402

C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

=PP2V5_PWRON_RAM

DDR CLK_AVDD (AB21)

VDD_DDR (T19, T21, T25, P20, N21, N25, M19, K19, K23, K27, G25, F19, D22, D27, B25)

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT

MEMORY CONTROL INTERFACE

RAM_CLK66M_NB	AC20	DDR_CLKP	
RAM_CLK_A_P_R	AA12	DDR_CK_A	
RAM_CLK_A_N_R	AB12	DDR_CK_AN	
RAM_CLK_B_P_R	AB14	DDR_CK_B	
RAM_CLK_B_N_R	AA14	DDR_CK_BN	
RAM_CLK_C_P_R	AE15	DDR_CK_C	
RAM_CLK_C_N_R	AE14	DDR_CK_CN	
RAM_CLK_D_P_R	AC14	DDR_CK_D	
RAM_CLK_D_N_R	AD14	DDR_CK_DN	
RAM_CLK_E_P_R	AD15	DDR_CK_E	
RAM_CLK_E_N_R	AC15	DDR_CK_EN	
RAM_CLK_F_P_R	AA15	DDR_CK_F	
RAM_CLK_F_N_R	AB15	DDR_CK_FN	
RAM_CKE_R<0>	AC17	DDR_CKE0	
RAM_CKE_R<1>	AD17	DDR_CKE1	
RAM_CKE_R<2>	AE17	DDR_CKE2	
RAM_CKE_R<3>	AF17	DDR_CKE3	
RAM_CKE_R<4>	AB17	DDR_CKE4	
RAM_CKE_R<5>	AA17	DDR_CKE5	
RAM_CKE_R<6>	AB18	DDR_CKE6	
RAM_CKE_R<7>	AA18	DDR_CKE7	
	Y21	DDR_VREF0	
	U21	DDR_VREF1	
	L21	DDR_VREF2	
	H20	DDR_VREF3	
	AA21	DDR_VREF4	
	M21	DDR_VREF5	
	V21	DDR_VREF6	
	J20	DDR_VREF7	
	AE21	DDR_RAS	RAM_RAS_L_R
	AD20	DDR_CAS	RAM_CAS_L_R
	AC23	DDR_WE	RAM_WE_L_R
	AF21	DDR_BA0	RAM_BA_R<0>
	AE20	DDR_BA1	RAM_BA_R<1>
	AH16	DDR_MUXEN0	RAM_MUXEN0
	AH18	DDR_MUXEN4	RAM_MUXEN4
	AG12	DDR_MAD0	RAM_A_R<0>
	AH13	DDR_MAD1	RAM_A_R<1>
	AH14	DDR_MAD2	RAM_A_R<2>
	AH15	DDR_MAD3	RAM_A_R<3>
	AF12	DDR_MAD4	RAM_A_R<4>
	AE12	DDR_MAD5	RAM_A_R<5>
	AD12	DDR_MAD6	RAM_A_R<6>
	AC12	DDR_MAD7	RAM_A_R<7>
	AG15	DDR_MAD8	RAM_A_R<8>
	AF15	DDR_MAD9	RAM_A_R<9>
	AF14	DDR_MAD10	RAM_A_R<10>
	AG14	DDR_MAD11	RAM_A_R<11>
	AH17	DDR_MAD12	RAM_A_R<12>
	AG17	DDR_MAD13	RAM_A_R<13>
	AF18	DDR_CS0	RAM_CS_L_R<0>
	AE18	DDR_CS1	RAM_CS_L_R<1>
	AG20	DDR_CS2	RAM_CS_L_R<2>
	AH20	DDR_CS3	RAM_CS_L_R<3>
	AC18	DDR_CS8	RAM_CS_L_R<8>
	AD18	DDR_CS9	RAM_CS_L_R<9>
	AG18	DDR_CS10	RAM_CS_L_R<10>
	AH19	DDR_CS11	RAM_CS_L_R<11>
	AC24	DDR_DQSP0	RAM_DQS_R<0>
	AG23	DDR_DQSP1	RAM_DQS_R<1>
	Y23	DDR_DQSP2	RAM_DQS_R<2>
	R23	DDR_DQSP3	RAM_DQS_R<3>
	M22	DDR_DQSP4	RAM_DQS_R<4>
	B26	DDR_DQSP5	RAM_DQS_R<5>
	B27	DDR_DQSP6	RAM_DQS_R<6>
	F23	DDR_DQSP7	RAM_DQS_R<7>
	AE23	DDR_DQSP8	RAM_DQS_R<8>
	AD28	DDR_DQSP9	RAM_DQS_R<9>
	Y27	DDR_DQSP10	RAM_DQS_R<10>
	U28	DDR_DQSP11	RAM_DQS_R<11>
	M27	DDR_DQSP12	RAM_DQS_R<12>
	J28	DDR_DQSP13	RAM_DQS_R<13>
	F28	DDR_DQSP14	RAM_DQS_R<14>
	F25	DDR_DQSP15	RAM_DQS_R<15>

DDR_CLK_AVSS (AA20)

=PP2V5_PWRON_RAM

R3700 1K 1% 1/16W MF-LF 402

R3701 1K 1% 1/16W MF-LF 402

PP1V25_PWRON_RAM_VREF_NB VOLTAGE=1.25V

C3730 0.1UF 20% 10V CERM 402

C3746 0.1UF 20% 10V CERM 402

C3747 0.1UF 20% 10V CERM 402

C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

=PP2V5_PWRON_RAM

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 — 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 — 0.1UF 20% 10V CERM 402

C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 — 0.1UF 20% 10V CERM 402

C3740 C3739 C3738 — 0.1UF 20% 10V CERM 402

U3LITE MEMORY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE: NONE

SHT 37 OF 102

ALL R PACKS ARE 1/16W 5%

38 37	RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>
38 37	RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>
38 37	RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>
38 37	RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>
38 37	RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>
38 37	RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>
38 37	RAM_DQ_R<6>	RP3816	4	5	22	RAM_DQ<6>
38 37	RAM_DQ_R<5>	RP3816	3	6	22	RAM_DQ<5>
38 37	RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>
38 37	RAM_DQ_R<10>	RP3801	1	8	22	RAM_DQ<10>
38 37	RAM_DQ_R<11>	RP3801	3	6	22	RAM_DQ<11>
38 37	RAM_DQ_R<14>	RP3801	4	5	22	RAM_DQ<14>
38 37	RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>
38 37	RAM_DQ_R<13>	RP3801	2	7	22	RAM_DQ<13>
38 37	RAM_DQ_R<15>	RP3835	1	8	22	RAM_DQ<15>
38 37	RAM_DQ_R<8>	RP3835	3	6	22	RAM_DQ<8>
38 37	RAM_DQ_R<17>	RP3822	1	8	22	RAM_DQ<17>
38 37	RAM_DQ_R<22>	RP3822	4	5	22	RAM_DQ<22>
38 37	RAM_DQ_R<19>	RP3822	2	7	22	RAM_DQ<19>
38 37	RAM_DQ_R<18>	RP3822	3	6	22	RAM_DQ<18>
38 37	RAM_DQ_R<20>	RP3823	3	6	22	RAM_DQ<20>
38 37	RAM_DQ_R<16>	RP3823	4	5	22	RAM_DQ<16>
38 37	RAM_DQ_R<21>	RP3823	2	7	22	RAM_DQ<21>
38 37	RAM_DQ_R<23>	RP3823	1	8	22	RAM_DQ<23>
38 37	RAM_DQ_R<30>	RP3808	3	6	22	RAM_DQ<30>
38 37	RAM_DQ_R<26>	RP3824	2	7	22	RAM_DQ<26>
38 37	RAM_DQ_R<24>	RP3808	1	8	22	RAM_DQ<24>
38 37	RAM_DQ_R<27>	RP3824	1	8	22	RAM_DQ<27>
38 37	RAM_DQ_R<28>	RP3808	4	5	22	RAM_DQ<28>
38 37	RAM_DQ_R<31>	RP3808	2	7	22	RAM_DQ<31>
38 37	RAM_DQ_R<29>	RP3824	4	5	22	RAM_DQ<29>
38 37	RAM_DQ_R<25>	RP3824	3	6	22	RAM_DQ<25>
38 37	RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>
38 37	RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>
38 37	RAM_DQ_R<38>	RP3826	2	7	22	RAM_DQ<38>
38 37	RAM_DQ_R<37>	RP3807	4	5	22	RAM_DQ<37>
38 37	RAM_DQ_R<39>	RP3826	3	6	22	RAM_DQ<39>
38 37	RAM_DQ_R<33>	RP3807	3	6	22	RAM_DQ<33>
38 37	RAM_DQ_R<34>	RP3807	1	8	22	RAM_DQ<34>
38 37	RAM_DQ_R<36>	RP3826	1	8	22	RAM_DQ<36>
38 37	RAM_DQ_R<47>	RP3811	2	7	22	RAM_DQ<47>
38 37	RAM_DQ_R<46>	RP3811	1	8	22	RAM_DQ<46>
38 37	RAM_DQ_R<43>	RP3814	2	7	22	RAM_DQ<43>
38 37	RAM_DQ_R<41>	RP3814	1	8	22	RAM_DQ<41>
38 37	RAM_DQ_R<45>	RP3811	4	5	22	RAM_DQ<45>
38 37	RAM_DQ_R<42>	RP3814	3	6	22	RAM_DQ<42>
38 37	RAM_DQ_R<40>	RP3814	4	5	22	RAM_DQ<40>
38 37	RAM_DQ_R<44>	RP3811	3	6	22	RAM_DQ<44>
38 37	RAM_DQ_R<51>	RP3830	4	5	22	RAM_DQ<51>
38 37	RAM_DQ_R<50>	RP3830	2	7	22	RAM_DQ<50>
38 37	RAM_DQ_R<49>	RP3830	1	8	22	RAM_DQ<49>
38 37	RAM_DQ_R<48>	RP3830	3	6	22	RAM_DQ<48>
38 37	RAM_DQ_R<52>	RP3812	2	7	22	RAM_DQ<52>
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38 37	RAM_DQ_R<54>	RP3812	4	5	22	RAM_DQ<54>
38 37	RAM_DQ_R<55>	RP3812	1	8	22	RAM_DQ<55>
38 37	RAM_DQ_R<56>	RP3813	1	8	22	RAM_DQ<56>
38 37	RAM_DQ_R<63>	RP3831	4	5	22	RAM_DQ<63>
38 37	RAM_DQ_R<59>	RP3813	2	7	22	RAM_DQ<59>
38 37	RAM_DQ_R<61>	RP3831	2	7	22	RAM_DQ<61>
38 37	RAM_DQ_R<57>	RP3831	3	6	22	RAM_DQ<57>
38 37	RAM_DQ_R<60>	RP3831	1	8	22	RAM_DQ<60>
38 37	RAM_DQ_R<58>	RP3813	3	6	22	RAM_DQ<58>
38 37	RAM_DQ_R<62>	RP3813	4	5	22	RAM_DQ<62>

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>
38 37	RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>
38 37	RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>
38 37	RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>
38 37	RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>
38 37	RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>
38 37	RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>
38 37	RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>
38 37	RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>
38 37	RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>
38 37	RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L
38 37	RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>
38 37	RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>
38 37	RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>
		RP3834	1	8	15	
38 37	RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>
38 37	RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>
38 37	RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>
38 37	RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>
38 37	RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>
38 37	RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>
38 37	RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L
38 37	RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>
38 37	RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>
38 37	RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L
38 37	RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>
38 37	RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>

38 37	RAM_DQ_R<68>	RP3818	2	7	22	RAM_DQ<68>
38 37	RAM_DQ_R<65>	RP3805	2	7	22	RAM_DQ<65>
38 37	RAM_DQ_R<70>	RP3818	4	5	22	RAM_DQ<70>
38 37	RAM_DQ_R<66>	RP3805	1	8	22	RAM_DQ<66>
38 37	RAM_DQ_R<71>	RP3818	3	6	22	RAM_DQ<71>
38 37	RAM_DQ_R<64>	RP3805	4	5	22	RAM_DQ<64>
38 37	RAM_DQ_R<67>	RP3805	3	6	22	RAM_DQ<67>
38 37	RAM_DQ_R<69>	RP3818	1	8	22	RAM_DQ<69>
38 37	RAM_DQ_R<74>	RP3817	3	6	22	RAM_DQ<74>
38 37	RAM_DQ_R<73>	RP3802	4	5	22	RAM_DQ<73>
38 37	RAM_DQ_R<72>	RP3817	2	7	22	RAM_DQ<72>
38 37	RAM_DQ_R<75>	RP3817	4	5	22	RAM_DQ<75>
38 37	RAM_DQ_R<78>	RP3802	2	7	22	RAM_DQ<78>
38 37	RAM_DQ_R<79>	RP3817	1	8	22	RAM_DQ<79>
38 37	RAM_DQ_R<77>	RP3802	1	8	22	RAM_DQ<77>
38 37	RAM_DQ_R<76>	RP3802	3	6	22	RAM_DQ<76>
38 37	RAM_DQ_R<87>	RP3806	2	7	22	RAM_DQ<87>
38 37	RAM_DQ_R<86>	RP3821	1	8	22	RAM_DQ<86>
38 37	RAM_DQ_R<81>	RP3821	4	5	22	RAM_DQ<81>
38 37	RAM_DQ_R<80>	RP3821	2	7	22	RAM_DQ<80>
38 37	RAM_DQ_R<84>	RP3806	1	8	22	RAM_DQ<84>
38 37	RAM_DQ_R<85>	RP3806	3	6	22	RAM_DQ<85>
38 37	RAM_DQ_R<83>	RP3821	3	6	22	RAM_DQ<83>
38 37	RAM_DQ_R<82>	RP3806	4	5	22	RAM_DQ<82>
38 37	RAM_DQ_R<91>	RP3819	3	6	22	RAM_DQ<91>
38 37	RAM_DQ_R<93>	RP3819	1	8	22	RAM_DQ<93>
38 37	RAM_DQ_R<94>	RP3803	2	7	22	RAM_DQ<94>
38 37	RAM_DQ_R<90>	RP3819	4	5	22	RAM_DQ<90>
38 37	RAM_DQ_R<88>	RP3803	4	5	22	RAM_DQ<88>
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38 37	RAM_DQ_R<92>	RP3803	3	6	22	RAM_DQ<92>
38 37	RAM_DQ_R<95>	RP3803	1	8	22	RAM_DQ<95>
38 37	RAM_DQ_R<98>	RP3820	4	5	22	RAM_DQ<98>
38 37	RAM_DQ_R<96>	RP3820	3	6	22	RAM_DQ<96>
38 37	RAM_DQ_R<103>	RP3820	2	7	22	RAM_DQ<103>
38 37	RAM_DQ_R<97>	RP3820	1	8	22	RAM_DQ<97>
38 37	RAM_DQ_R<100>	RP3825	2	7	22	RAM_DQ<100>
38 37	RAM_DQ_R<99>	RP3825	3	6	22	RAM_DQ<99>
38 37	RAM_DQ_R<102>	RP3825	1	8	22	RAM_DQ<102>
38 37	RAM_DQ_R<101>	RP3825	4	5	22	RAM_DQ<101>
38 37	RAM_DQ_R<111>	RP3809	1	8	22	RAM_DQ<111>
38 37	RAM_DQ_R<106>	RP3809	3	6	22	RAM_DQ<106>
38 37	RAM_DQ_R<105>	RP3809	2	7	22	RAM_DQ<105>
38 37	RAM_DQ_R<108>	RP3829	2	7	22	RAM_DQ<108>
38 37	RAM_DQ_R<107>	RP3829	4	5	22	RAM_DQ<107>
38 37	RAM_DQ_R<110>	RP3829	3	6	22	RAM_DQ<110>
38 37	RAM_DQ_R<104>	RP3809	4	5	22	RAM_DQ<104>
38 37	RAM_DQ_R<109>	RP3829	1	8	22	RAM_DQ<109>
38 37	RAM_DQ_R<119>	RP3828	4	5	22	RAM_DQ<119>
38 37	RAM_DQ_R<112>	RP3815	2	7	22	RAM_DQ<112>
38 37	RAM_DQ_R<117>	RP3815	1	8	22	RAM_DQ<117>
38 37	RAM_DQ_R<118>	RP3828	1	8	22	RAM_DQ<118>
38 37	RAM_DQ_R<113>	RP3815	3	6	22	RAM_DQ<113>
38 37	RAM_DQ_R<115>	RP3828	3	6	22	RAM_DQ<115>
38 37	RAM_DQ_R<116>	RP3828	2	7	22	RAM_DQ<116>
38 37	RAM_DQ_R<114>	RP3815	4	5	22	RAM_DQ<114>
38 37	RAM_DQ_R<121>	RP3827	3	6	22	RAM_DQ<121>
38 37	RAM_DQ_R<124>	RP3827	2	7	22	RAM_DQ<124>
38 37	RAM_DQ_R<120>	RP3827	4	5	22	RAM_DQ<120>
38 37	RAM_DQ_R<123>	RP3810	2	7	22	RAM_DQ<123>
38 37	RAM_DQ_R<125>	RP3827	1	8	22	RAM_DQ<125>
38 37	RAM_DQ_R<122>	RP3810	4	5	22	RAM_DQ<122>
38 37	RAM_DQ_R<126>	RP3810	1	8	22	RAM_DQ<126>
38 37	RAM_DQ_R<127>	RP3810	3	6	22	RAM_DQ<127>

THE FOLLOWING ARE 0402 5% RESISTORS

38 37	RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P
38 37	RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N
38 37	RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P
38 37	RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N
38 37	RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P
38 37	RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N
38 37	RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P
38 37	RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N
38 37	RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P
38 37	RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N
38 37	RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P
38 37	RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N

38 37	RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>
38 37	RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>
38 37	RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>
38 37	RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>
38 37	RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>
38 37	RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>
38 37	RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>
38 37	RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>
38 37	RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>
38 37	RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>
38 37	RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>
38 37	RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>
38 37	RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>
38 37	RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>
38 37	RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>
38 37	RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>

		ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
38 37	RAM_CLK_A_P_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	P206
38 37	RAM_CLK_A_N_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	P207
38 37	RAM_CLK_B_P_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	P208
38 37	RAM_CLK_B_N_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	P209
38 37	RAM_CLK_C_P_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	P210
38 37	RAM_CLK_C_N_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	P211
38 37	RAM_CLK_D_P_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	P212
38 37	RAM_CLK_D_N_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	P213
38 37	RAM_CLK_E_P_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	P214
38 37	RAM_CLK_E_N_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	P215
38 37	RAM_CLK_F_P_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	P216
38 37	RAM_CLK_F_N_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	P217
40 38	RAM_CLK_A_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	P218
40 38	RAM_CLK_A_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	P219
40 38	RAM_CLK_B_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	P220
40 38	RAM_CLK_B_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	P221
40 38	RAM_CLK_C_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	P222
40 38	RAM_CLK_C_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	P223
40 38	RAM_CLK_D_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	P224
40 38	RAM_CLK_D_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	P225
40 38	RAM_CLK_E_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	P226
40 38	RAM_CLK_E_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	P227
40 38	RAM_CLK_F_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	P228
40 38	RAM_CLK_F_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	P229
38 37	RAM_CKE_R<1..0>		RAM_CAD	RAM_CAD		P230
38 37	RAM_CKE_R<5..4>		RAM_CAD	RAM_CAD		P231
44 40 38	RAM_CKE<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		P232
44 40 38	RAM_CKE<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		P233
45 40 38	RAM_CKE<4>	RAM_CKECS1	RAM_CAD	RAM_CAD		P234
45 40 38	RAM_CKE<5>	RAM_CKECS1	RAM_CAD	RAM_CAD		P235
38 37	RAM_CS_L_R<1..0>		RAM_CAD	RAM_CAD		P236
38 37	RAM_CS_L_R<9..8>		RAM_CAD	RAM_CAD		P237
44 40 38	RAM_CS_L<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		P238
44 40 38	RAM_CS_L<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		P239
45 40 38	RAM_CS_L<8>	RAM_CKECS1	RAM_CAD	RAM_CAD		P240
45 40 38	RAM_CS_L<9>	RAM_CKECS1	RAM_CAD	RAM_CAD		P241
38 37	RAM_DQS_R<15..0>		RAM_CAD	RAM_CAD		P242
38 37	RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		P243
45 44 40 38	RAM_DQ<127..0>		RAM_CAD	RAM_CAD		P244
44 40 38	RAM_DQS<0>	RAM_DQS0	RAM_CAD	RAM_CAD		P245
44 40 38	RAM_DQ<7..0>	RAM_DQS0	RAM_CAD	RAM_CAD		P246
44 40 38	RAM_DQS<1>	RAM_DQS1	RAM_CAD	RAM_CAD		P247
44 40 38	RAM_DQ<15..8>	RAM_DQS1	RAM_CAD	RAM_CAD		P248
44 40 38	RAM_DQS<2>	RAM_DQS2	RAM_CAD	RAM_CAD		P249
44 40 38	RAM_DQ<23..16>	RAM_DQS2	RAM_CAD	RAM_CAD		P250
44 40 38	RAM_DQS<3>	RAM_DQS3	RAM_CAD	RAM_CAD		P251
44 40 38	RAM_DQ<31..24>	RAM_DQS3	RAM_CAD	RAM_CAD		P252
44 40 38	RAM_DQS<4>	RAM_DQS4	RAM_CAD	RAM_CAD		P253
44 40 38	RAM_DQ<39..32>	RAM_DQS4	RAM_CAD	RAM_CAD		P254
45 40 38	RAM_DQS<5>	RAM_DQS5	RAM_CAD	RAM_CAD		P255
45 40 38	RAM_DQ<47..40>	RAM_DQS5	RAM_CAD	RAM_CAD		P256
44 40 38	RAM_DQS<6>	RAM_DQS6	RAM_CAD	RAM_CAD		P257
44 40 38	RAM_DQ<55..48>	RAM_DQS6	RAM_CAD	RAM_CAD		P258
44 40 38	RAM_DQS<7>	RAM_DQS7	RAM_CAD	RAM_CAD		P259
44 40 38	RAM_DQ<63..56>	RAM_DQS7	RAM_CAD	RAM_CAD		P260
45 40 38	RAM_DQS<8>	RAM_DQS8	RAM_CAD	RAM_CAD		P261
45 40 38	RAM_DQ<71..64>	RAM_DQS8	RAM_CAD	RAM_CAD		P262
45 40 38	RAM_DQS<9>	RAM_DQS9	RAM_CAD	RAM_CAD		P263
45 40 38	RAM_DQ<79..72>	RAM_DQS9	RAM_CAD	RAM_CAD		P264
45 40 38	RAM_DQS<10>	RAM_DQS10	RAM_CAD	RAM_CAD		P265
45 40 38	RAM_DQ<87..80>	RAM_DQS10	RAM_CAD	RAM_CAD		P266
45 40 38	RAM_DQS<11>	RAM_DQS11	RAM_CAD	RAM_CAD		P267
45 40 38	RAM_DQ<95..88>	RAM_DQS11	RAM_CAD	RAM_CAD		P268
45 40 38	RAM_DQS<12>	RAM_DQS12	RAM_CAD	RAM_CAD		P269
45 40 38	RAM_DQ<103..96>	RAM_DQS12	RAM_CAD	RAM_CAD		P270
45 40 38	RAM_DQS<13>	RAM_DQS13	RAM_CAD	RAM_CAD		P271
45 40 38	RAM_DQ<111..104>	RAM_DQS13	RAM_CAD	RAM_CAD		P272
45 40 38	RAM_DQS<14>	RAM_DQS14	RAM_CAD	RAM_CAD		P273
45 40 38	RAM_DQ<119..112>	RAM_DQS14	RAM_CAD	RAM_CAD		P274
45 40 38	RAM_DQS<15>	RAM_DQS15	RAM_CAD	RAM_CAD		P275
45 40 38	RAM_DQ<127..120>	RAM_DQS15	RAM_CAD	RAM_CAD		P276
38 37	RAM_A_R<13..0>		RAM_CAD	RAM_CAD		P277
38 37	RAM_BA_R<1..0>		RAM_CAD	RAM_CAD		P278
38 37	RAM_RAS_L_R		RAM_CAD	RAM_CAD		P279
38 37	RAM_CAS_L_R		RAM_CAD	RAM_CAD		P280
38 37	RAM_WE_L_R		RAM_CAD	RAM_CAD		P281
45 44 40 38	RAM_A<13..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		P300
45 40 38	RAM_BA<1..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		P301
45 40 38	RAM_RAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		P302
45 40 38	RAM_CAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		P303
45 40 38	RAM_WE_L	RAM_A_CTL	RAM_CAD	RAM_CAD		P304

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

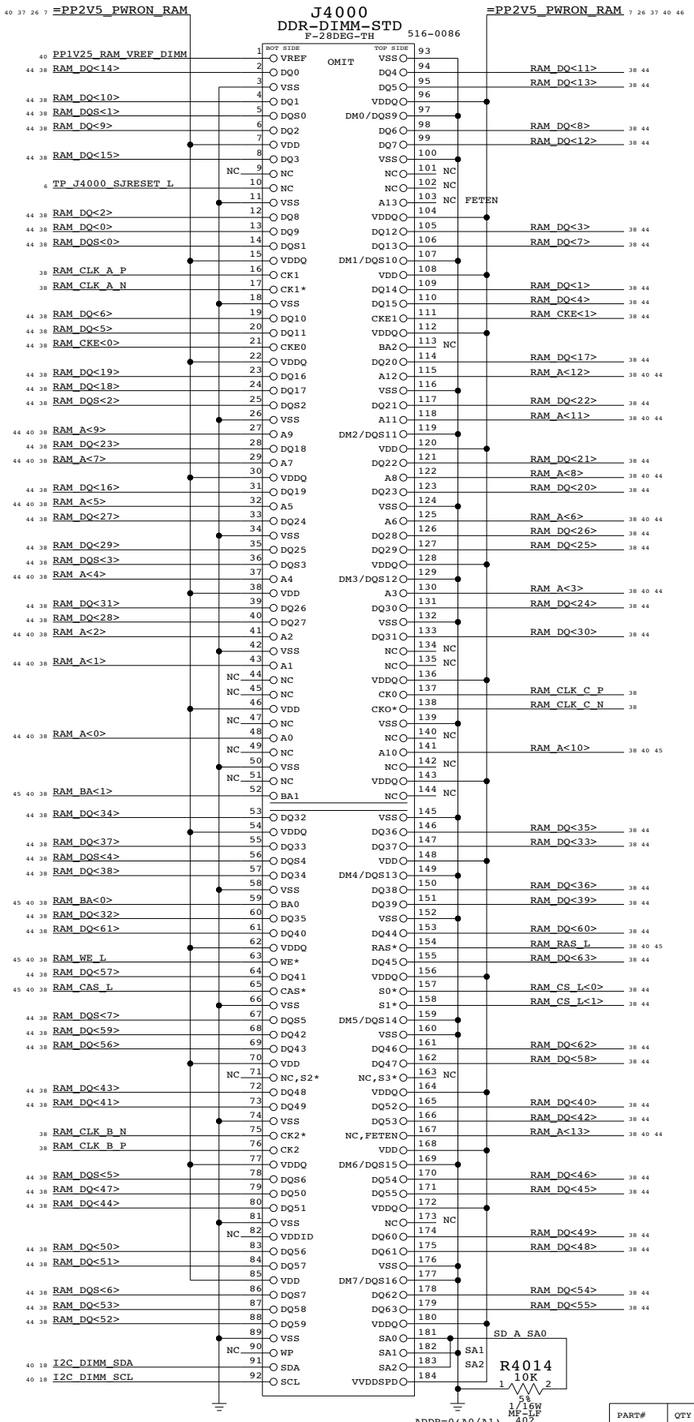
RAM_CAD SPACING IS 10MIL

SERIES TERM

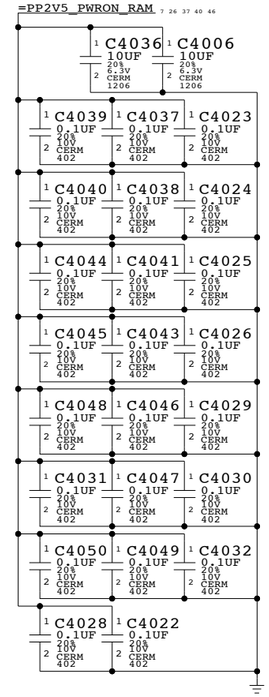
SYNC_MASTER=N/A SYNC_DATE=N/A

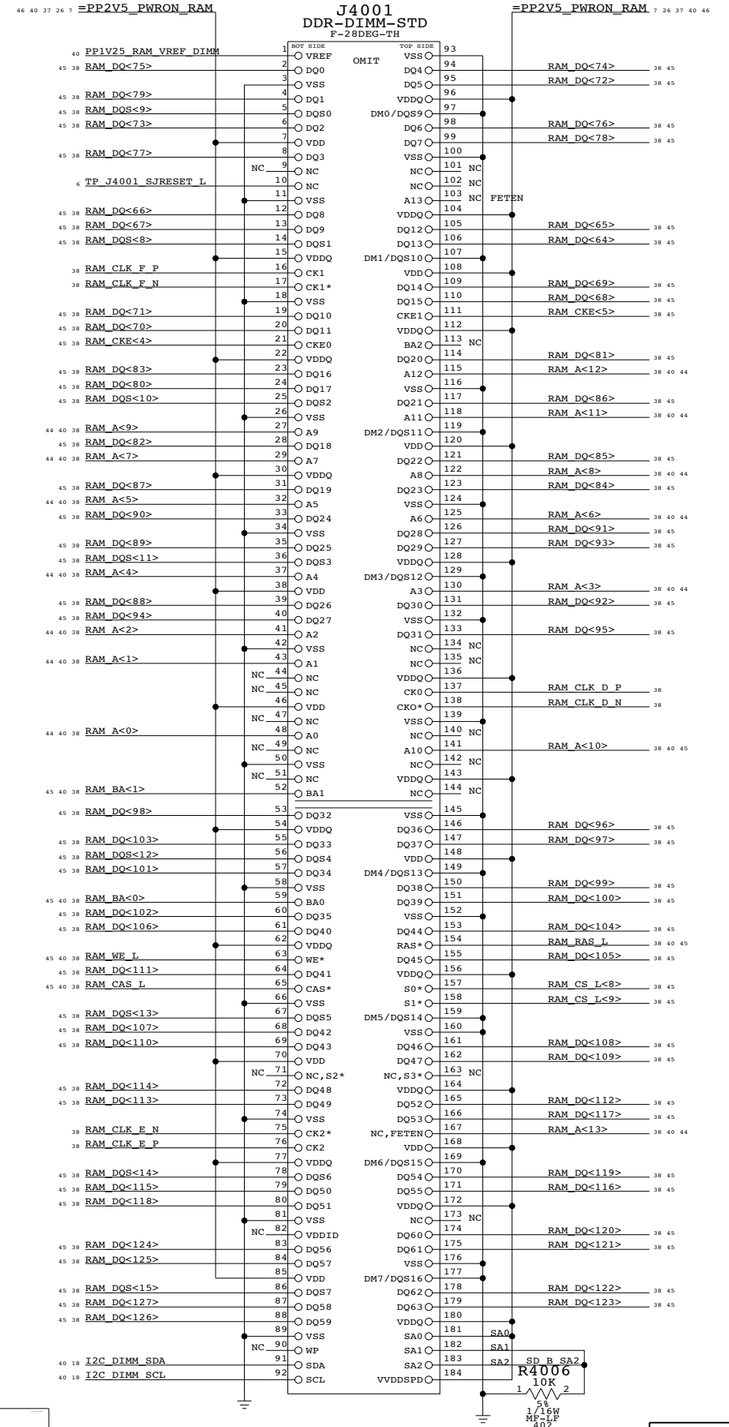
APPLE COMPUTER INC.

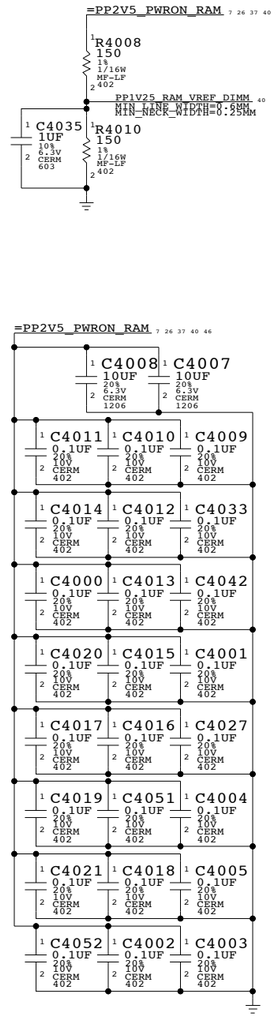
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 38 OF 102	



PIN 82:
NC: VDD & VDDQ ARE THE SAME
GND: VDD & VDDQ ARE DIFFERENT







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD	CRITICAL
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD	CRITICAL

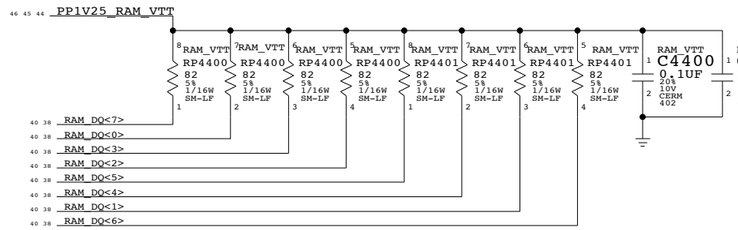
VVR R'S ADJACENT TO V'S OR G'S
VVR V'S ADJACENT TO G'S FORBIDDEN

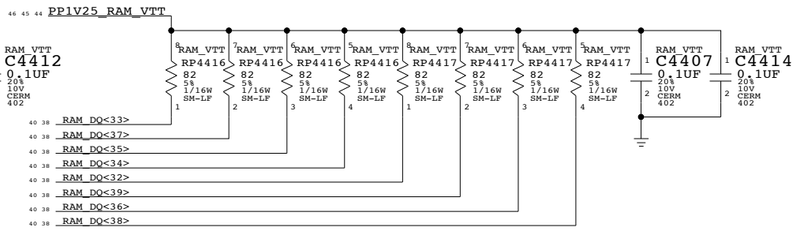
DIMMS

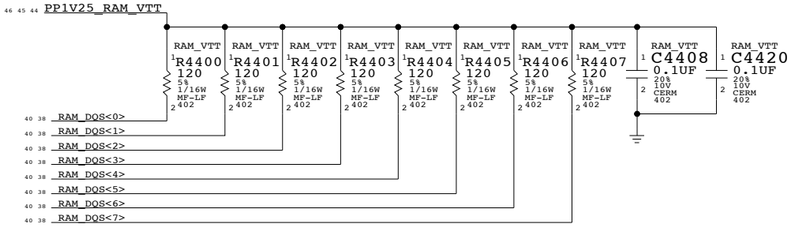
SYNC_MASTER=N/A SYNC_DATE=N/A

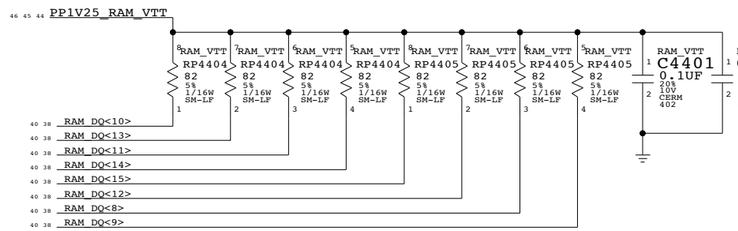
APPLE COMPUTER INC.

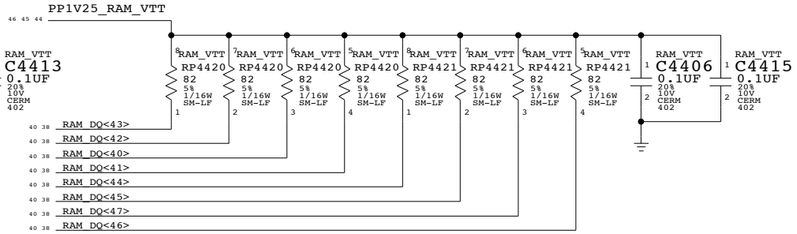
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 40 OF 102	

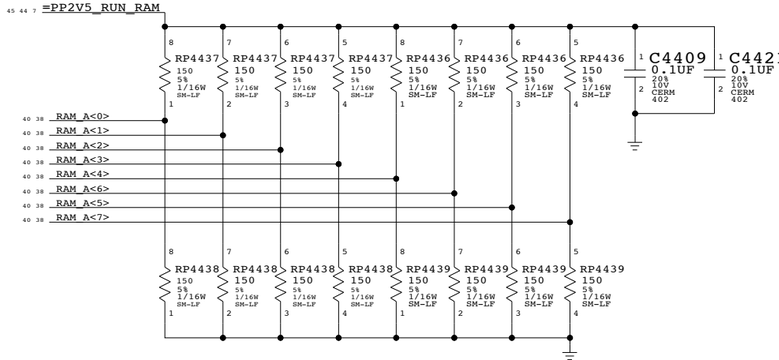


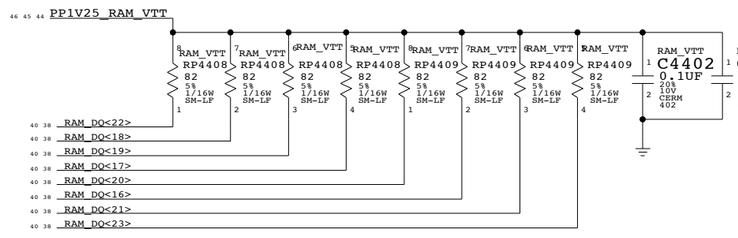


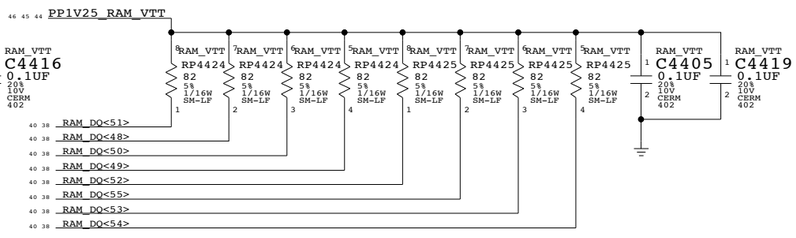


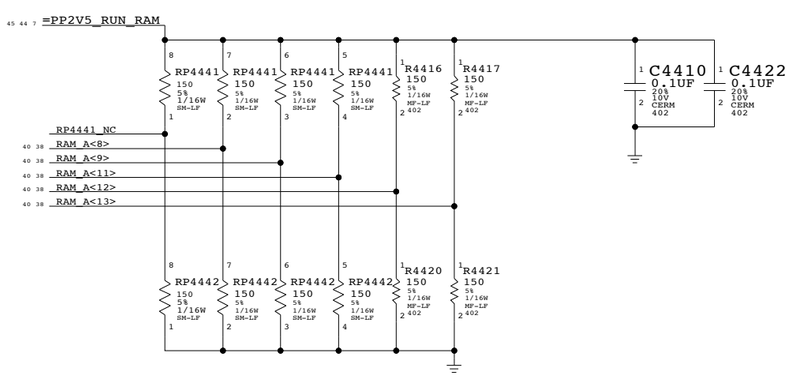


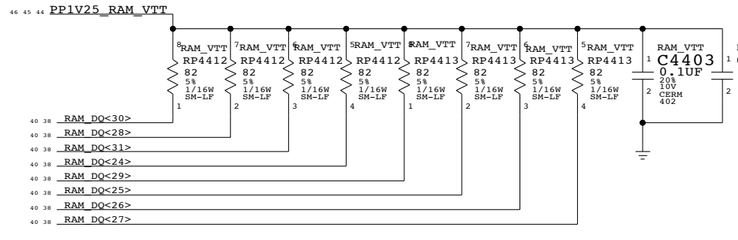


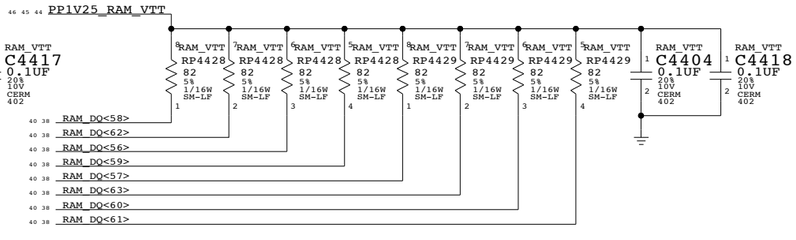


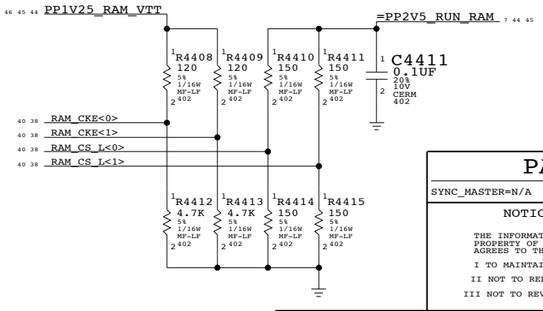












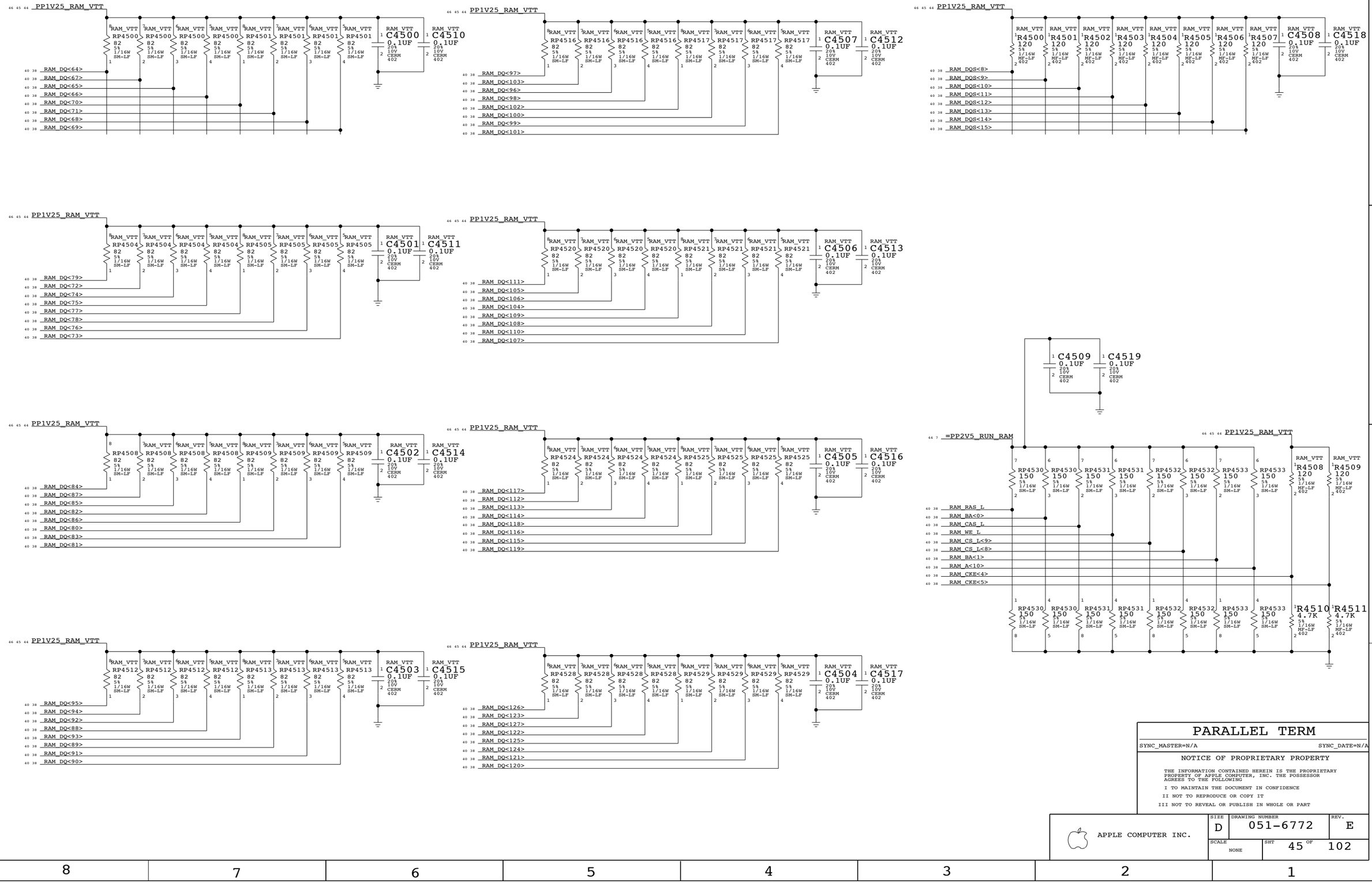
PARALLEL TERM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT OF
NONE	44 OF 102



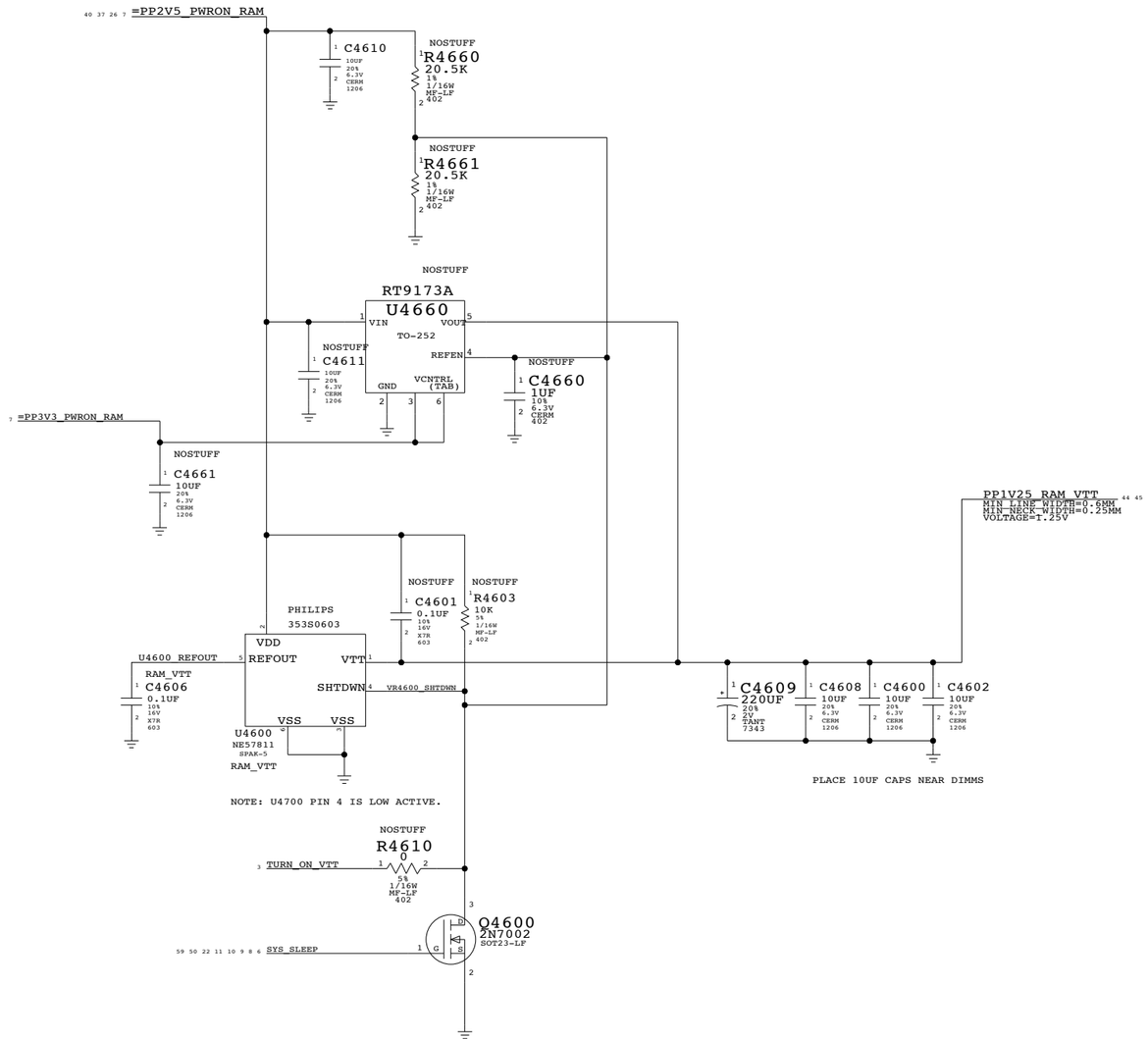
PARALLEL TERM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 45 OF 102	

ONLY STUFF ONE VTT VREG



MEM TERM VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE: NONE

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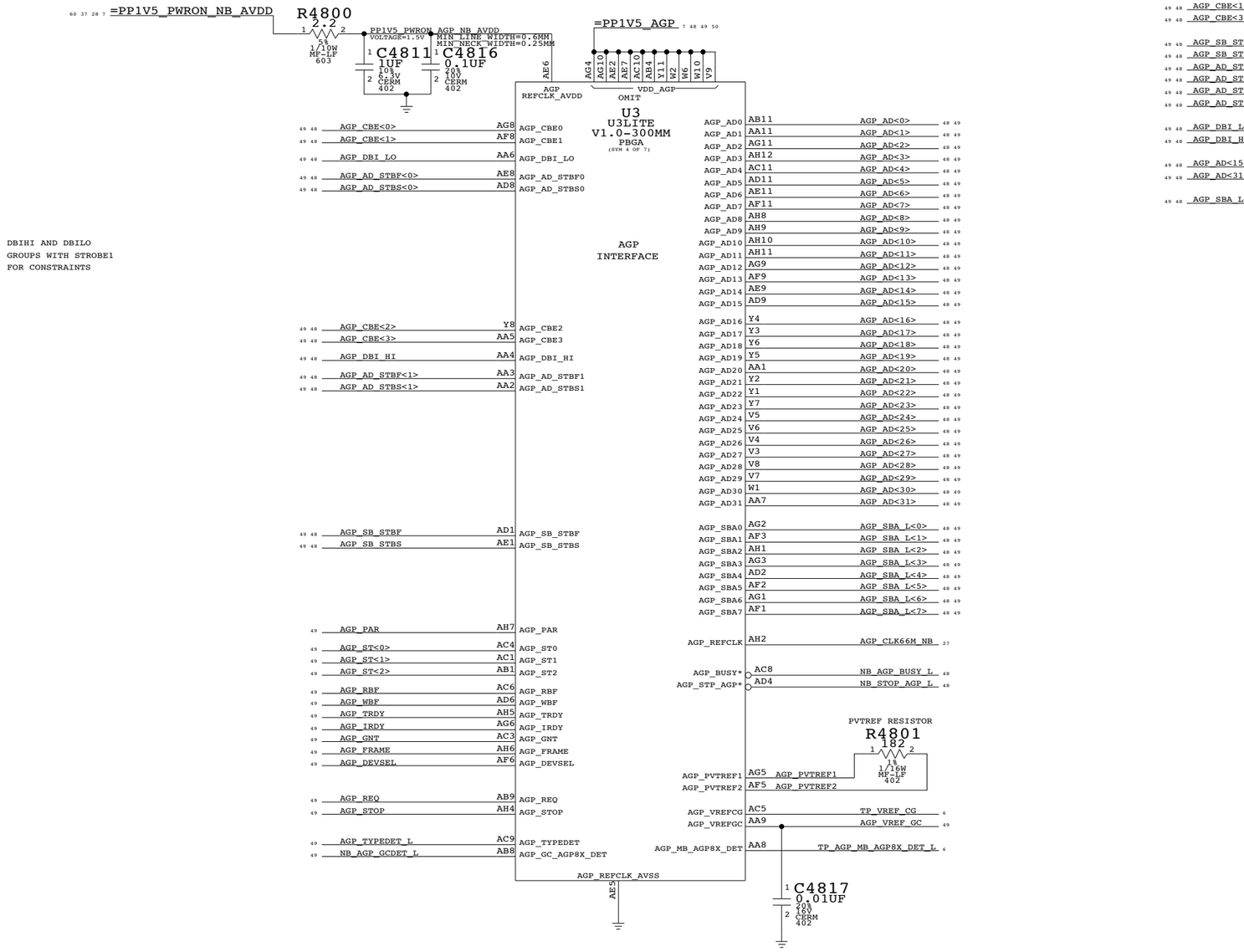
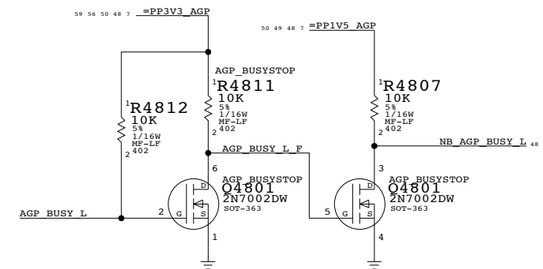


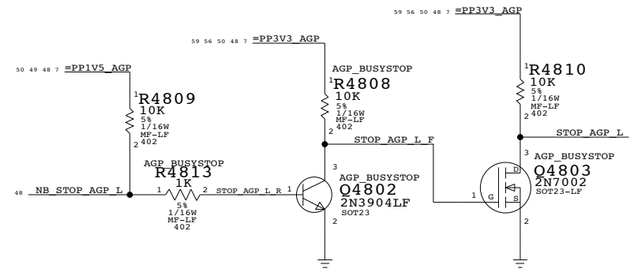
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
AGP_CBE<1..0>	AGP_DATA	AGP_DATA		146
AGP_CBE<3..2>	AGP_DATA	AGP_DATA		148
AGP_SB_STBF	AGP_STROBE	AGP_STROBE	AGP_SB_STB	149
AGP_SB_STBS	AGP_STROBE	AGP_STROBE	AGP_SB_STB	150
AGP_AD_STBF<0>	AGP_STROBE	AGP_STROBE	AGP_AD_STB0	151
AGP_AD_STBS<0>	AGP_STROBE	AGP_STROBE	AGP_AD_STB0	152
AGP_AD_STBF<1>	AGP_STROBE	AGP_STROBE	AGP_AD_STB1	153
AGP_AD_STBS<1>	AGP_STROBE	AGP_STROBE	AGP_AD_STB1	154
AGP_DBI_LO	AGP_DATA	AGP_DATA		155
AGP_DBI_HI	AGP_DATA	AGP_DATA		156
AGP_AD<15..0>	AGP_DATA	AGP_DATA		157
AGP_AD<31..16>	AGP_DATA	AGP_DATA		158
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA		159

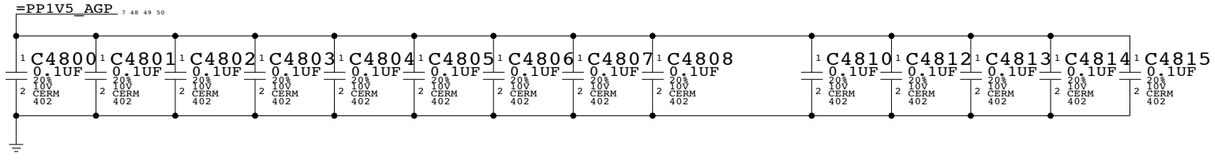
DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

LEVEL SHIFTER FOR U3LITE

AGP BUSY AND STOP ARE NOT USED IN ALL DESIGNS







SYNC_MASTER=N/A	SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 48 OF 102	

U3LITE AGP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0231	1	IC,RV351LE, GRAPHICS CTLR	U4900	

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)

50 49 48 7 =PP1V5_AGP

R4914 3.32K 1% 1/16W MF-LF 402

AGP_VREF_GC 48

R4940 1.02K 1% 1/16W MF-LF 402

C4940 0.01UF 20% 16V CERM 402

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)

50 49 48 7 =PP1V5_AGP

AGP 3.0
0.233 * VDDP
0.35V

R4906 3.32K 1% 1/16W MF-LF 402

GPU_AGP_VREF 49

R4907 1.02K 1% 1/16W MF-LF 402

C4957 0.01UF 20% 16V CERM 402

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

U3LITE SIGNALS

48 NB_AGP_GCDET_L

48 AGP_TYPEDET_L

R4913 0 5% 1/16W MF-LF 402

R4909 10K 5% 1/16W MF-LF 402

50 49 48 7 =PP1V5_AGP

C4900 1UF 10% 6.3V CERM 402

C4901 1UF 10% 6.3V CERM 402

C4902 0.01UF 20% 16V CERM 402

C4903 0.01UF 20% 16V CERM 402

C4904 0.01UF 20% 16V CERM 402

C4905 0.01UF 20% 16V CERM 402

AA23 AA24 P27 P24 P30 U27 V23 V24 W30 Y27 AB30 AC23 AC27 AE30 AF27 J30 M23 M24 N30 P23 T23

VDDP

GPU_AGP_VREF 49

C4910 0.01UF 20% 16V CERM 402

PLACE C4910 CLOSE TO BALL M26

OMIT

U4900
RV351
BGA
(1 OF 5)

AGP

27 AGP_CLK66M_GPU	AG30	PCICLK	AGPREF	M26	
48 AGP_AD<0>	H29	AD0	CBE0*	N29	AGP_CBE<0> 48
48 AGP_AD<1>	H28	AD1	CBE1*	U28	AGP_CBE<1> 48
48 AGP_AD<2>	J29	AD2			
48 AGP_AD<3>	J28	AD3	DBI_LO	AB26	AGP_DBI_LO 48
48 AGP_AD<4>	K29	AD4			
48 AGP_AD<5>	K28	AD5	AD_STBF_0	M28	AGP_AD_STBF<0> 48
48 AGP_AD<6>	L29	AD6	AD_STBS_0*	M29	AGP_AD_STBS<0> 48
48 AGP_AD<7>	L28	AD7			
48 AGP_AD<8>	N28	AD8			
48 AGP_AD<9>	P29	AD9			
48 AGP_AD<10>	P28	AD10			
48 AGP_AD<11>	R29	AD11			
48 AGP_AD<12>	R28	AD12			
48 AGP_AD<13>	T29	AD13			
48 AGP_AD<14>	T28	AD14			
48 AGP_AD<15>	U29	AD15			
48 AGP_AD<16>	N25	AD16	CBE2*	P26	AGP_CBE<2> 48
48 AGP_AD<17>	R26	AD17	CBE3*	U26	AGP_CBE<3> 48
48 AGP_AD<18>	P25	AD18			
48 AGP_AD<19>	R27	AD19	DBI_HI	AB25	AGP_DBI_HI 48
48 AGP_AD<20>	R25	AD20			
48 AGP_AD<21>	T25	AD21	AD_STBF_1	V25	AGP_AD_STBF<1> 48
48 AGP_AD<22>	T26	AD22	AD_STBS_1*	V26	AGP_AD_STBS<1> 48
48 AGP_AD<23>	U25	AD23			
48 AGP_AD<24>	V27	AD24			
48 AGP_AD<25>	W26	AD25			
48 AGP_AD<26>	W25	AD26			
48 AGP_AD<27>	Y26	AD27			
48 AGP_AD<28>	Y25	AD28			
48 AGP_AD<29>	AA26	AD29			
48 AGP_AD<30>	AA25	AD30			
48 AGP_AD<31>	AA27	AD31			
48 AGP_SBA_L<0>	AD28	SBA0	SB_STBF	AB29	AGP_SB_STBF 48
48 AGP_SBA_L<1>	AD29	SBA1	SB_STBS*	AB28	AGP_SB_STBS 48
48 AGP_SBA_L<2>	AC28	SBA2			
48 AGP_SBA_L<3>	AC29	SBA3			
48 AGP_SBA_L<4>	AA28	SBA4			
48 AGP_SBA_L<5>	AA29	SBA5			
48 AGP_SBA_L<6>	Y28	SBA6			
48 AGP_SBA_L<7>	Y29	SBA7			
8 GPU_RESET_L	AG28	RST*	PAR	M25	AGP_PAR 48
48 AGP_ST<0>	AF29	ST0	INTA*	AE26	AGP_INT_L 25
48 AGP_ST<1>	AD27	ST1	AGPTEST*	M27	GPU_AGPTEST_L
48 AGP_ST<2>	AE28	ST2			
48 AGP_REQ	AF28	REQ*			
48 AGP_GNT	AD26	GNT*	AGP8X_DET*	AC25	
48 AGP_STOP	N26	STOP*			
48 AGP_DEVSEL	V29	DEVSEL*			
48 AGP_TRDY	V28	TRDY*			
48 AGP_IRDY	W29	IRDY*			
48 AGP_FRAME	W28	FRAME*			
48 AGP_WBF	AC26	WBF*			
48 AGP_RBF	AE29	RBF*			

SERIES R NEEDED TO PREVENT GPU GLITCH
WE CAN LOWER OR REMOVE THIS IF WE MEET GPU
POWER SEQUENCING REQUIREMENTS

R4912 330 5% 1/16W MF-LF 402

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

PP3V3_GPU 50 56 58 59

R4908 10K 5% 1/16W MF-LF 402

R4910 47 1% 1/16W MF-LF 402 =PP1V5_AGP 7 48 49 50

GPU AGP

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

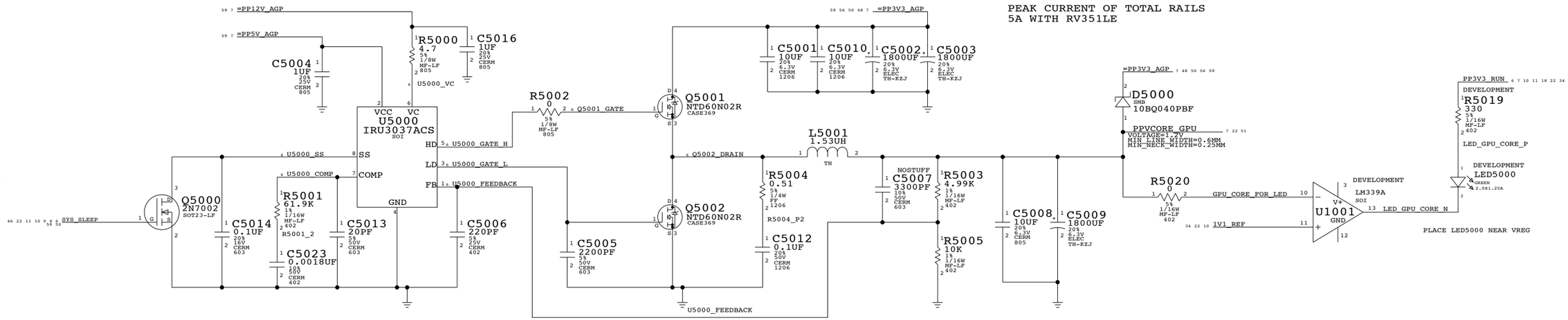
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 49 OF 102	

GPU VCORE VREG

NOTE:
SET OUTPUT = 1.20V +/- 5% FOR RV351LE

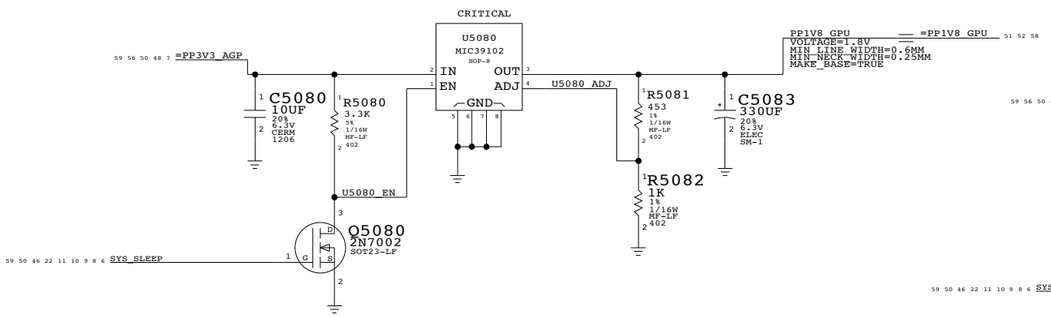
IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R5003+R5005)/R5005 = 1.199 VDC

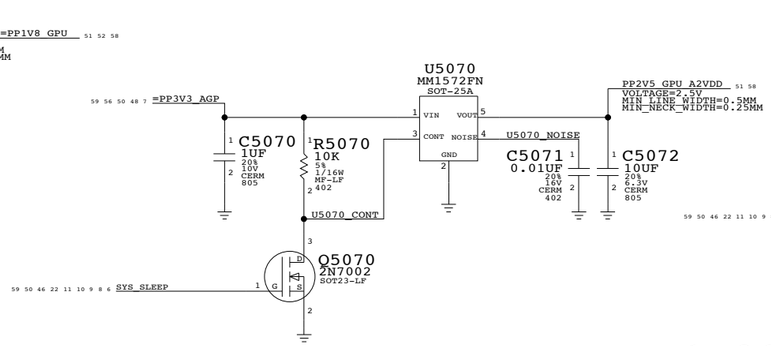
PEAK CURRENT OF TOTAL RAILS
5A WITH RV351LE



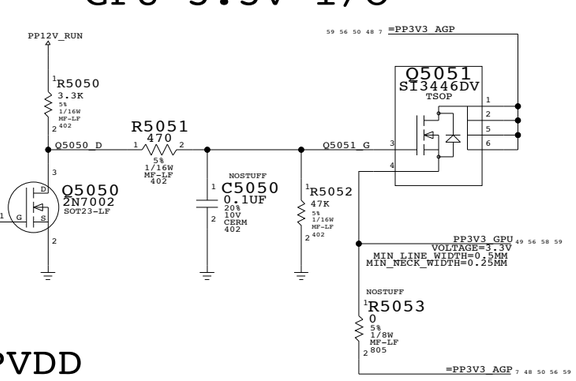
GPU 1.8V VREG

GPU 2.5V A2VDD



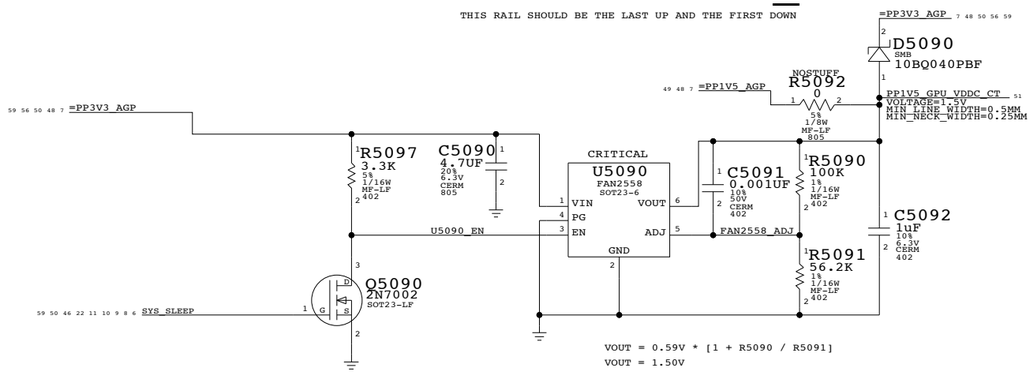


GPU 3.3V I/O



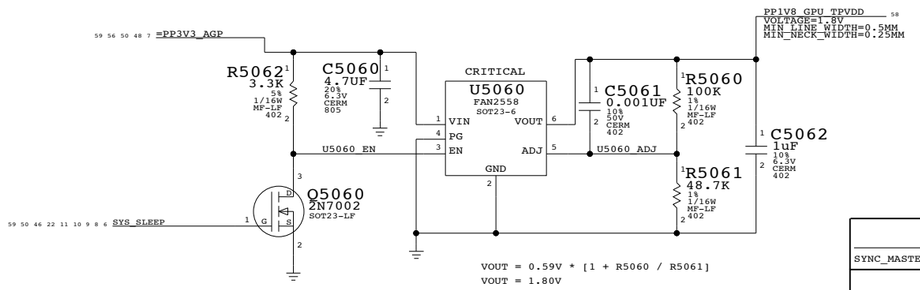
GPU 1.50V VDDC_CT

THIS RAIL SHOULD BE THE LAST UP AND THE FIRST DOWN



VOUT = 0.59V * [1 + R5090 / R5091]
VOUT = 1.50V

GPU 1.80V TPVDD



VOUT = 0.59V * [1 + R5060 / R5061]
VOUT = 1.80V

POWER SEQUENCING FOR RV351: =PP3V3_AGP > PP2V5_GPU > PPVCORE_GPU > VDDC_CT
PP2V5_GPU_A2VDD > PP1V8_GPU
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER

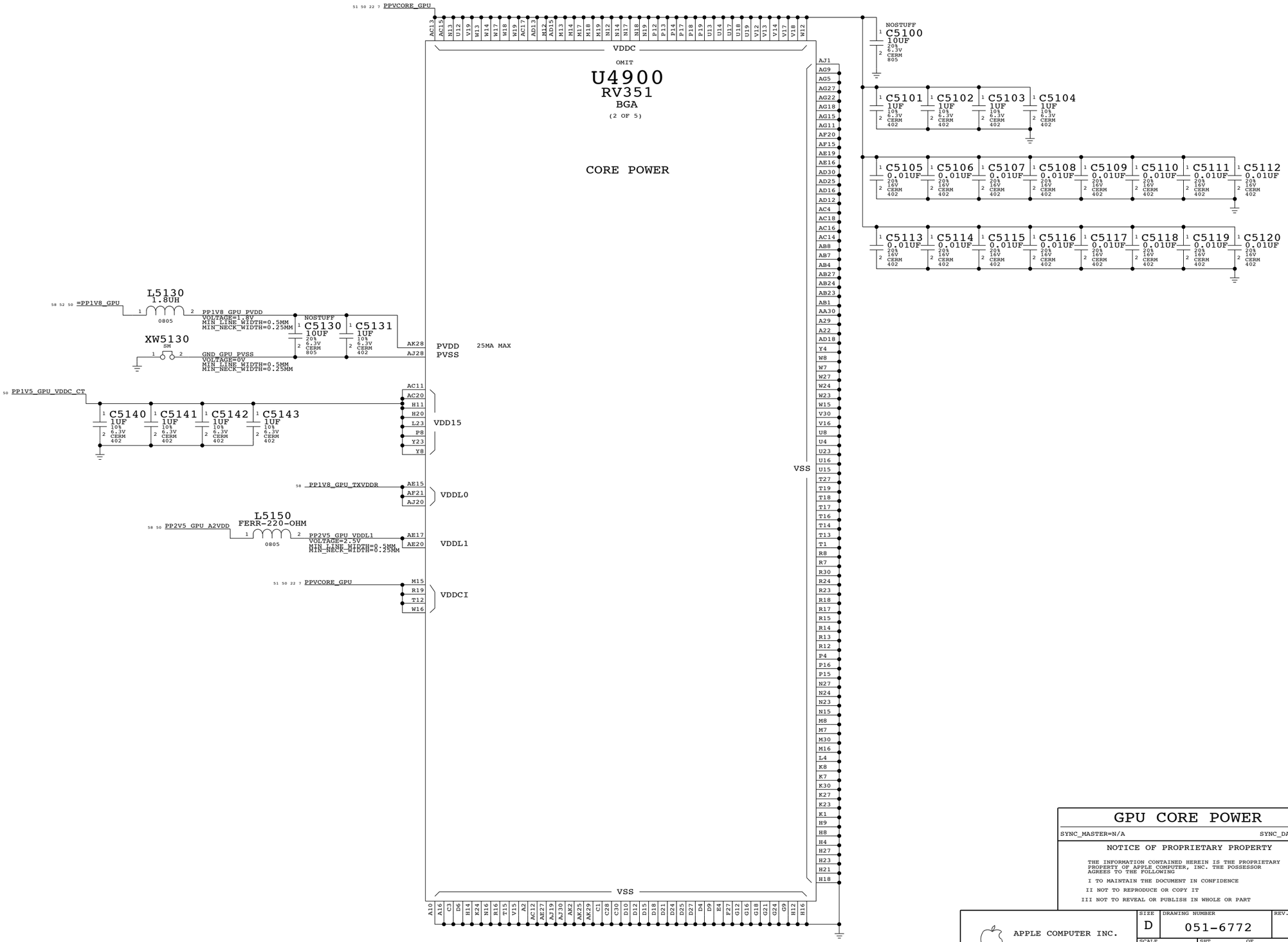
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

GRAPHICS VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 50 OF 102	



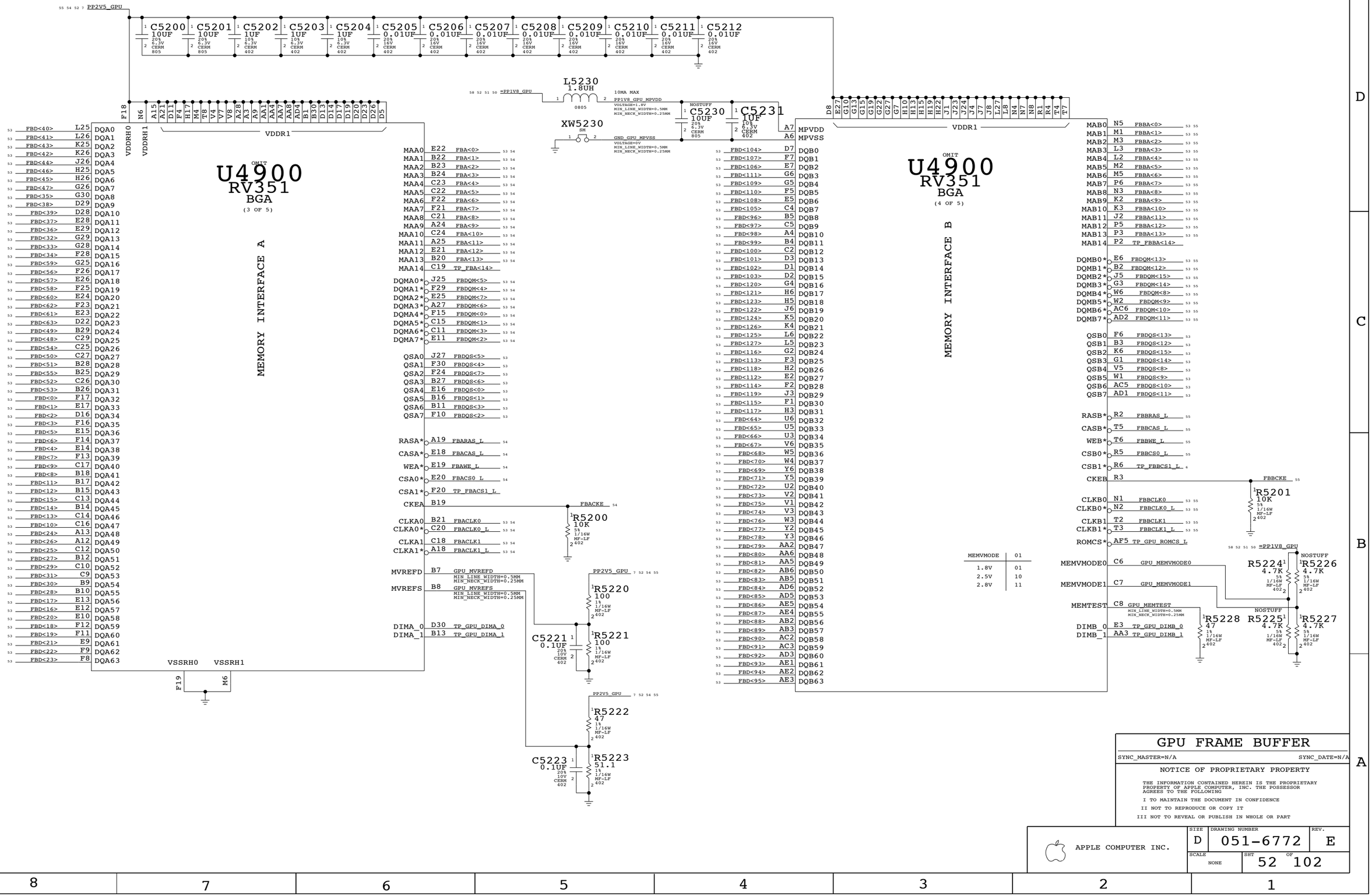
GPU CORE POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	51	102



GPU FRAME BUFFER

SYNC_MASTER=N/A SYNC_DATE=N/A

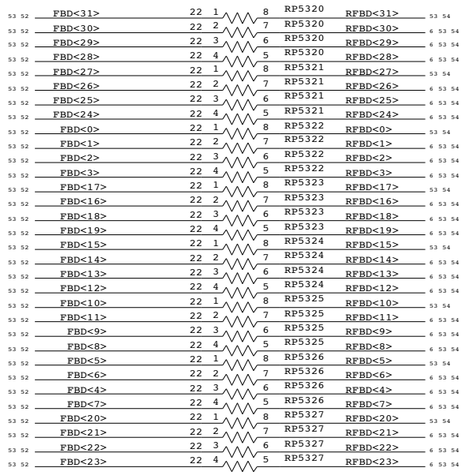
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

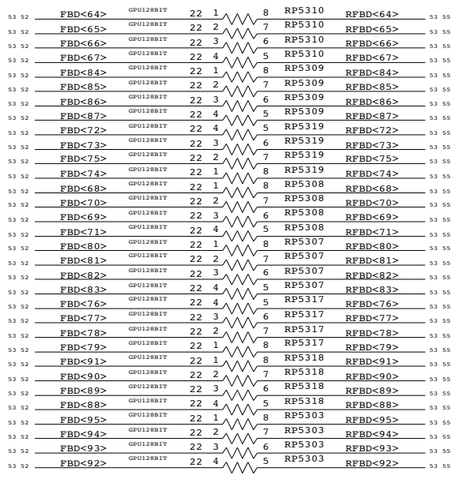
SCALE	SHT	OF
NONE	52	102

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY



FRAME BUFFER B TERMINATION



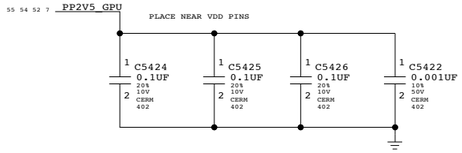
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>	GPU_FB	GPU_FB	
RFBD<127..0>	GPU_FB	GPU_FB	
FBA<13..0>	GPU_FB	GPU_FB	
FBBA<13..0>	GPU_FB	GPU_FB	
FBDQM<15..0>	GPU_FB	GPU_FB	
FBDQS<15..0>	GPU_FB	GPU_FB	
FBACLK0	GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L	GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1	GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L	GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0	GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L	GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1	GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L	GPU_FBCLK	GPU_FBCLK	FBBCLK1

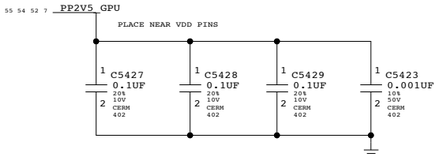
FB TERMINATION

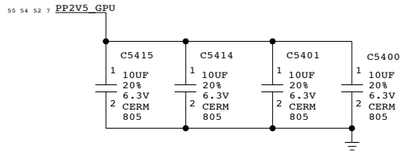
SYNC_MASTER=N/A SYNC_DATE=N/A

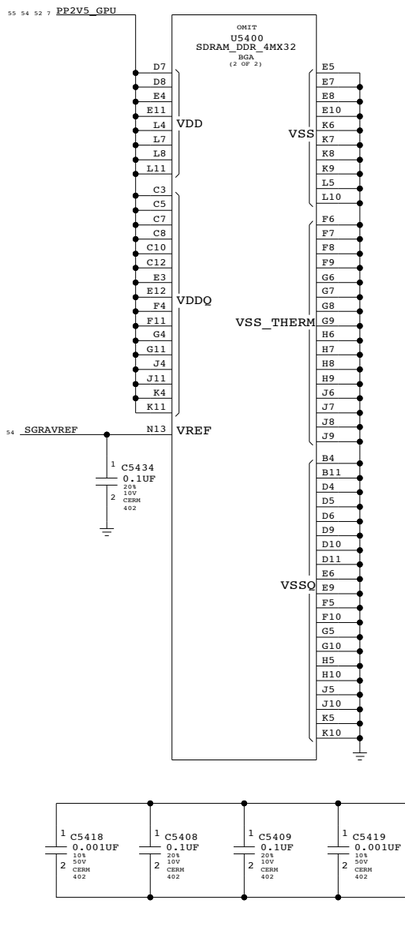
APPLE COMPUTER INC.

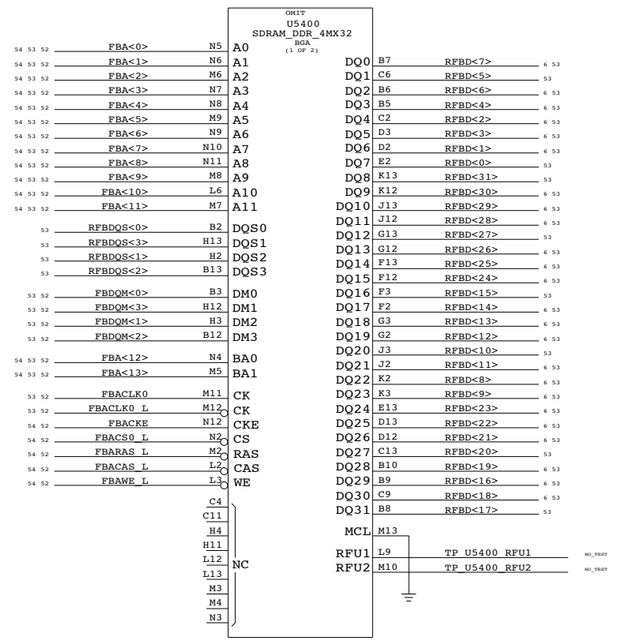
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 53 OF 102	

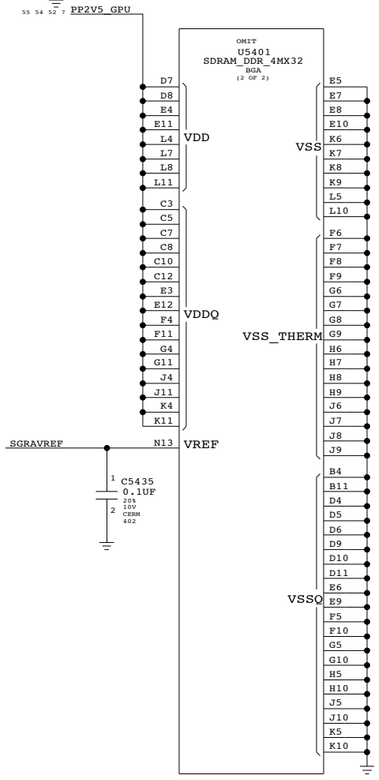


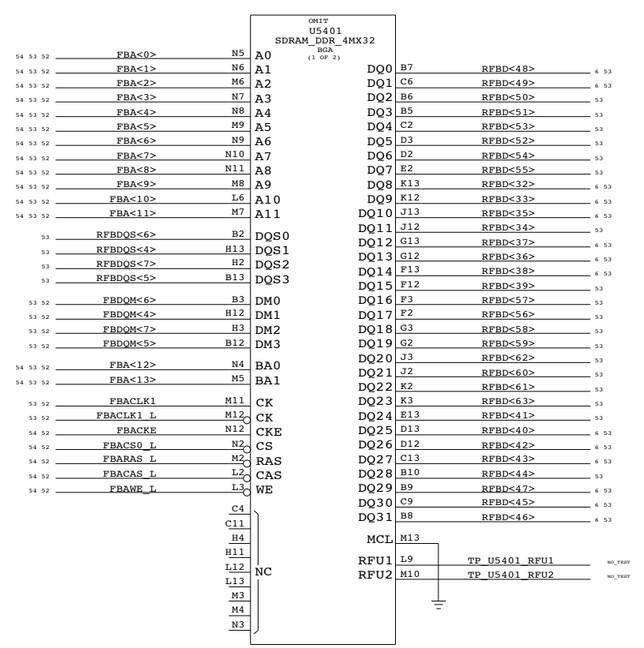


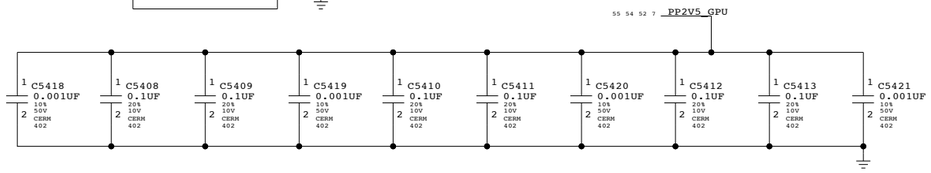


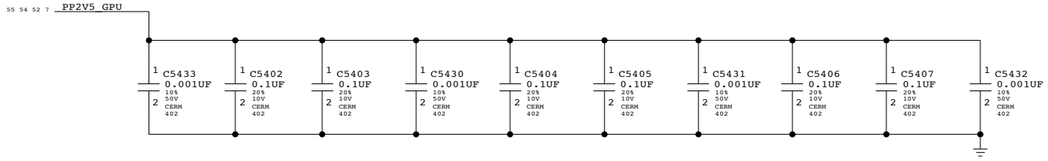












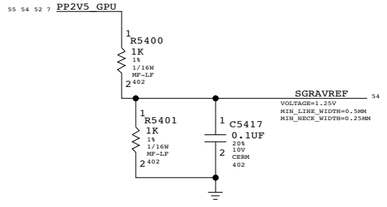
EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX64
333S0341	2	SDRAM,8MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX128

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0290	333S0251	SAMSUNG64	U5400,U5401,U5500,U5501	HYN4M G-DIE
333S0292	333S0252	HYNIX64	U5400,U5401,U5500,U5501	SAM4M B-DIE



GPU DDR SDRAM A

SYNC_MASTER=N/A SYNC_DATE=N/A

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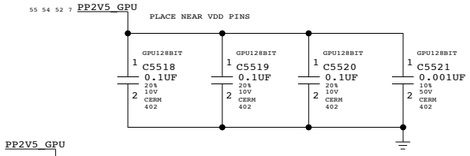
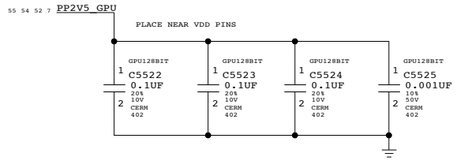
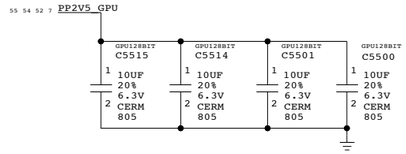
APPLE COMPUTER INC.

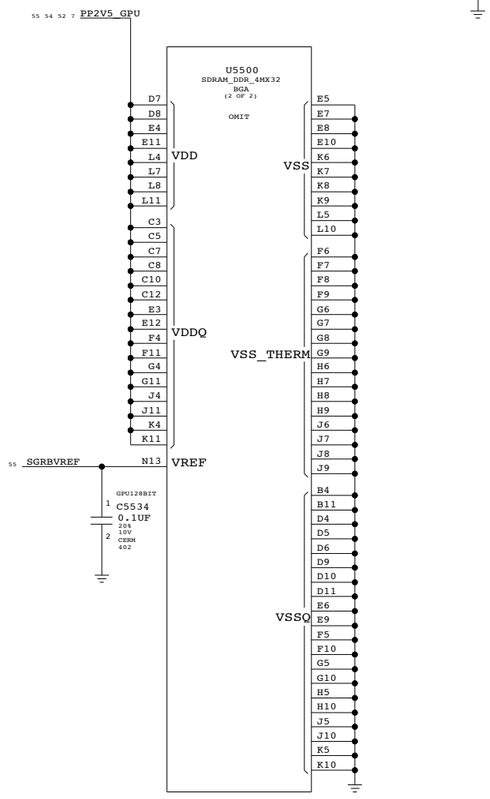
SIZE	DRAWING NUMBER	REV.
D	051-6772	E

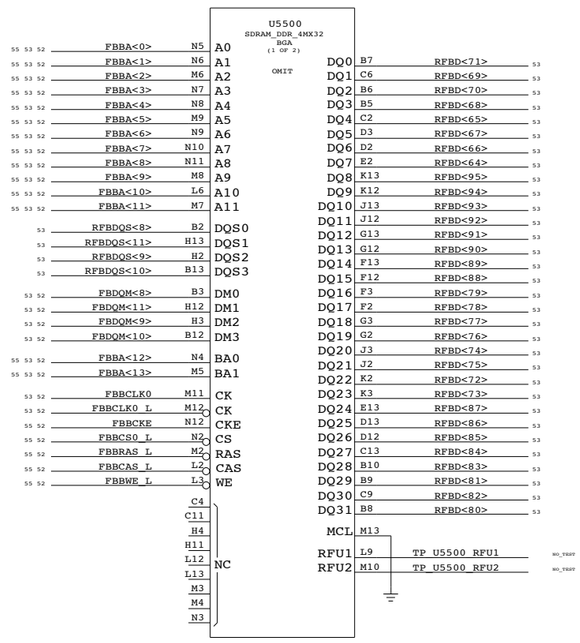
SCALE	SHT	OF
NONE	54	102

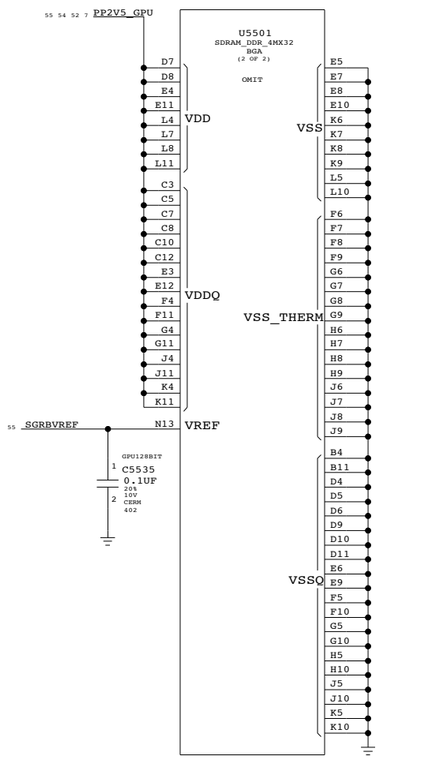


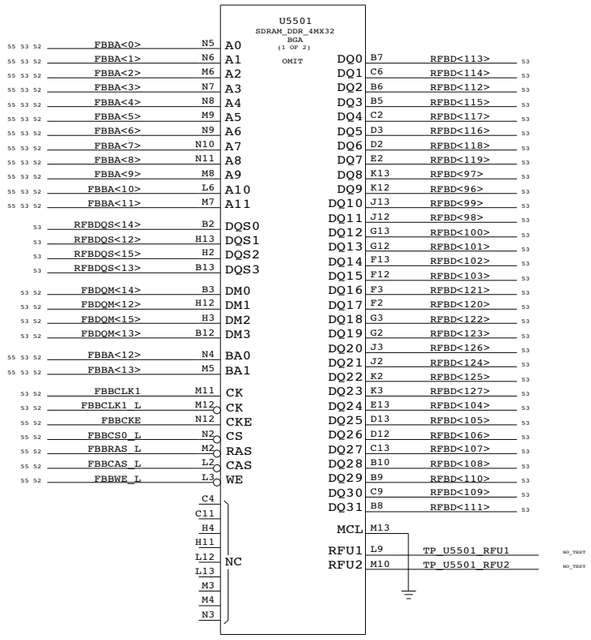


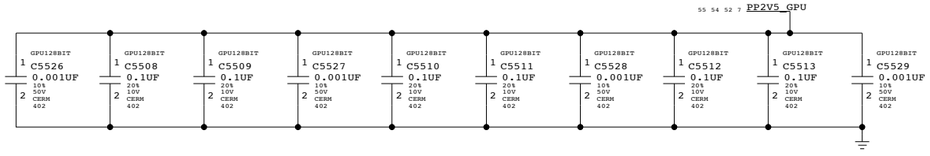




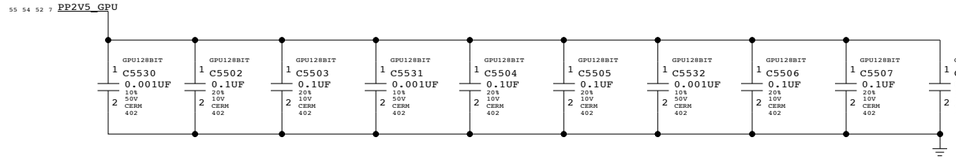




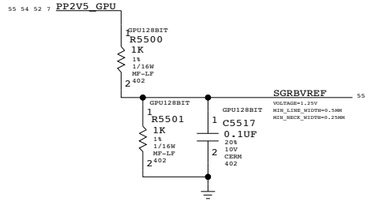




DDR SDRAM B VREF



EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX64
333S0341	2	SDRAM,8MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX128

GPU DDR SDRAM B

SYNC_MASTER=N/A SYNC_DATE=N/A

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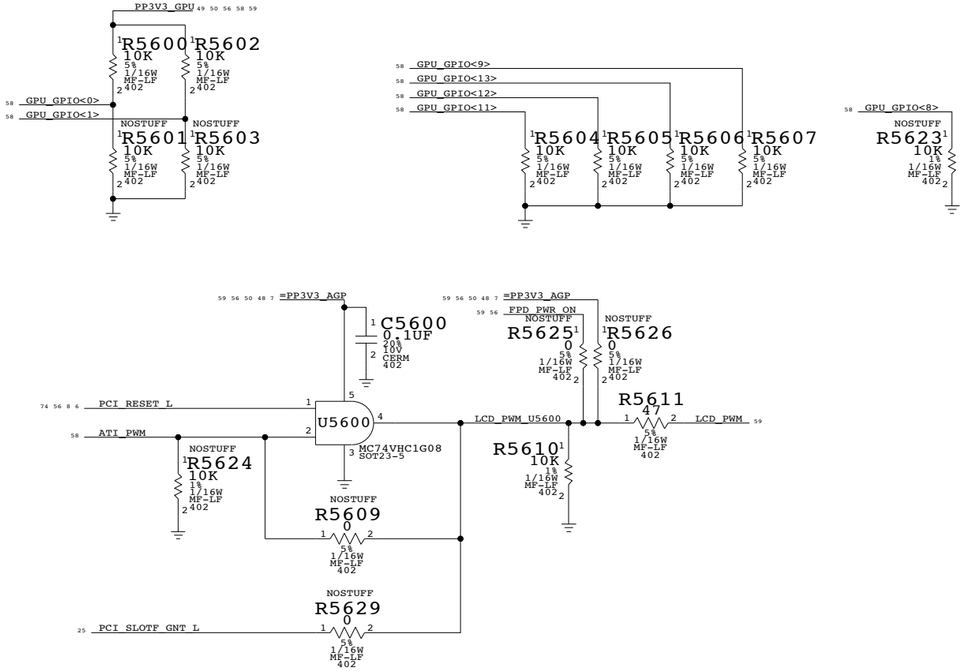
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 55 OF 102	



APPLE GPIO	ATI STRAP	PIN	DESCRIPTION	DEFAULT
	AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK) 00 - REFCLK SLIGHTLY EARLIER THEN FEEDBACK 01 - REFCLK 1 TAP EARLIER THEN FEEDBACK 10 - REFCLK 1 TAP LATER THEN FEEDBACK 11 - REFCLK 2 TAPS EARLIER THEN FEEDBACK CLOCK (ATI RECOMMENDED)	00 INTERNAL PULL-DOWN
	X1CLK_SKWE(1:0)	GPIO(3:2)	CLOCK PHASE ADJUSTMENT BETWEEN X1 CLK AND X2CLK 00 - 0 TAP DELAY	00 INTERNAL PULL-DOWN
	ROMIDCFG(3:0)	GPIO(9,13:11)	IF NO ROM ATTACHED, CONTROLS CHIP IDS. IF ROM- IDENTIFIES TYPE 0X0X - NO ROM, CHG_ID=0	
	ID_DISABLE	GPIO(8)	STRAP 0 - NORMAL OPERATION 1 - SHUTS THE CHIP DOWN BY NOT RESPONDING TO ANY CONFIG CYCLES	0 INTERNAL PULL-DOWN
	BUSCFG(2:0)	GPIO(6:4)	AGP8X_DETB BUSCFG[2:0] AGPMODE SIGNALING IDSEL 0 000 AGP8X 0.8V AD16	000 INTERNAL PULL-DOWN
	MULTIFUNC(1:0)	LCDDATA(17:16)	MULTI-FUNCTION DEVICE SELECT 00 - SINGLE FUNCTION DEVICE. 01 - TWO FUNCTION DEVICE. NO AGP IN EITHER FUNCTION 10 - TWO FUNCTION DEVICE. AGP ONLY IN FUNCTION 0 11 - TWO FUNCTION DEVICE. AGP IN BOTH FUNCTIONS IF BUSCFG PIN BASED STRAPS ARE SET TO PCI, THEN AGP WILL NOT BE ENABLED IN ANY FUNCTION.	00
	MEMSTRAP(1:0)	GPU_GPIO<15,10>	00 - SAMSUNG 4MX32 01 - UNDEFINED 10 - HYNIX 4MX32 11 - HYNIX 8MX32	
INV_CUR_HI		GPIO<7>	OUTPUT: GPU READS PANEL ID AND SETS THIS BIT ACCORDINGLY FOR REFERENCE ONLY, ACTIONS COME FROM BOOTROM SYSTEM / PANEL ID / INV_CUR_HI Q45 A / 0X9C27 / 1 0X9C38 / 0 Q45 B / 0X9C3A / 1 0X9C39 / 0 Q45 C / TBD / 1 TBD / 0 Q45 D / 0X9C3A / 1 Q45 A/B SUPPORT IS FOR DEVELOPMENT	
FPD_PWR_ON		GPIO<16>	OUTPUT: PANEL POWER SEQUENCING	
TMDS_EN		GPIO<14>	INPUT: PANEL POWER SEQUENCING	

GPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 56 OF 102

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_CKP	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS_CKM	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS_D0P	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS_D0M	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS_D1P	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS_D1M	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS_D2P	GPU_TMDS	GPU_TMDS	TMDS_D2
TMDS_D2M	GPU_TMDS	GPU_TMDS	TMDS_D2
ANALOG_GRN	GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_RED	GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_BLU	GPU_VGA_37P5	GPU_VGA_37P5	

PP3V3_GPU

C5800 10UF 20% 6.3V CERM 805 NOSTUFF
C5801 1UF 10% 6.3V CERM 402
C5802 1UF 10% 6.3V CERM 402
C5803 1UF 10% 6.3V CERM 402

U4900 RV351 BGA (5 OF 5)

VDDR3 OMIT
VDDR4

GPIO
- GPU_GPIO<0> AJ5
- GPU_GPIO<1> AH5
- TP_GPU_GPIO<2> AJ4
- TP_GPU_GPIO<3> AK4
- TP_GPU_GPIO<4> AH4
- TP_GPU_GPIO<5> AF4
- TP_GPU_GPIO<6> AJ3
- GPU_GPIO<7> AK3
- GPU_GPIO<8> AH3
- GPU_GPIO<9> AJ2
- GPU_GPIO<10> AH2
- GPU_GPIO<11> AH1
- GPU_GPIO<12> AG3
- GPU_GPIO<13> AG1
- GPU_GPIO<14> AG2
- GPU_GPIO<15> AF3
- GPU_GPIO<16> AF2

EXTERNAL TMDS LCDDATA
- TP_GPU_LCDDATA<0> AH6
- TP_GPU_LCDDATA<1> AJ6
- TP_GPU_LCDDATA<2> AK6
- TP_GPU_LCDDATA<3> AH7
- TP_GPU_LCDDATA<4> AK7
- TP_GPU_LCDDATA<5> AJ7
- TP_GPU_LCDDATA<6> AH8
- TP_GPU_LCDDATA<7> AJ8
- TP_GPU_LCDDATA<8> AH9
- TP_GPU_LCDDATA<9> AJ9
- TP_GPU_LCDDATA<10> AK9
- TP_GPU_LCDDATA<11> AH10
- TP_GPU_LCDDATA<12> AE6
- TP_GPU_LCDDATA<13> AG6
- TP_GPU_LCDDATA<14> AF6
- TP_GPU_LCDDATA<15> AE7
- GPU_LCDDATA<16> AF7
- GPU_LCDDATA<17> AE8
- TP_GPU_LCDDATA<18> AG8
- TP_GPU_LCDDATA<19> AF8
- TP_GPU_LCDDATA<20> AE9
- TP_GPU_LCDDATA<21> AF9
- TP_GPU_LCDDATA<22> AG10
- TP_GPU_LCDDATA<23> AF10

LCDCNTL
- GPU_LCDCNTL<0> AJ10
- GPU_LCDCNTL<1> AK10
- GPU_LCDCNTL<2> AJ11
- GPU_LCDCNTL<3> AH11

DVOMODE AE10

HPD1 AF12 MON_DETECT_R

PP3V3_GPU
RP5810 4.7K 5% 1/16W SM-LF
RP5818 10K 5% 1/16W MF-LF 402
R5819 0 5% 1/16W MF-LF 402
MON_DETECT

Y5800 SM-3 27.000M
C5814 22PF 5% 50V CERM 603
C5815 22PF 5% 50V CERM 603
R5814 1M 5% 1/16W MF-LF 402
R5815 249 1% 1/16W MF-LF 402
GPU_CLK27M_XIN AH28
GPU_CLK27M_XOUT AJ29
GPU_TESTEN
R5830 100 5% 1/16W MF-LF 402

XTALIN
XTALOUT
CLK

TEST_MCLK B6
TEST_YCLK E8
PLLTEST NC AE25
TESTEN AH27
TEST

R5816 1K 1% 1/16W MF-LF 402
R5817 1K 1% 1/16W MF-LF 402
C5817 0.1UF 20% 10V CERM 402
GPU_VREFG AG4
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

GPU_DIODE_PLUS AF11
GPU_DIODE_MINUS AE11
DPLUS
DMINUS
RSTB_MSK AG29
VREFG AF17

ATI_PWM AG12

NC NO NECTS

THE FREQUENCY OF THE 20" PIXEL CLOCK IS 119 MHZ

TMDS
- TXCP AK13 TMDS_CKP
- TXCM* AH13 TMDS_CKM
- TX0P AH14 TMDS_D0P
- TX0M* AJ13 TMDS_D0M
- TX1P AH15 TMDS_D1P
- TX1M* AJ14 TMDS_D1M
- TX2P AK15 TMDS_D2P
- TX2M* AJ15 TMDS_D2M

TXVDDR AF13
TXVSSR AF14
TPVDD AG13 75MA MAX
TPVSS AG14
AK12
AJ12

DDC2CLK AE13 I2C_GPU_TMDS_SCL
DDC2DATA AE14 I2C_GPU_TMDS_SDA

DAC1
- VDD1DI AE24
- VDD2DI AE22
- VSS1DI AE23
- VSS2DI AE21
- AVDD AH24
- AVSSQ AD24 GND_GPU_AVSSQ
- AVSSN AH23

R AK27 NC
G AJ27 NC
B AJ26 NC
HSYNC AG25 TP_HSYNC
VSYNC AH25
RSET AH26
DDC1CLK AF24 TP_DDC1CLK
DDC1DATA AF25 TP_DDC1DATA
AUXWIN AF26 NC
STEREOSYNC AG26

GPU_DAC1_VSYNC
DEVELOPMENT R5826 75 1% 1/16W MF-LF 402
GPU_RSET
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
GPU_STEREOSYNC
R5825 10K 5% 1/16W MF-LF 402
XW5847 SM GND_GPU_AVSSQ
R5820 499 1% 1/16W MF-LF 402

DAC2
- A2VDD AG21
- A2VSSN AH21
- A2VDDQ AH22
- A2VSSQ AJ21
- AF22
- AF23

Y_G AJ22 ANALOG_GRN
C_R AJ23 ANALOG_RED
COMP_B AK22 ANALOG_BLU
H2SYNC AJ24 ANALOG_HSYNC
V2SYNC AK24 ANALOG_VSYNC
R2SET AK21
DDC3CLK AG23 I2C_GPU_MON_SCL
DDC3DATA AG24 I2C_GPU_MON_SDA

ROUTE SIGNALS AT 37.5 OHMS
R5821 75 1% 1/16W MF-LF 402
R5822 75 1% 1/16W MF-LF 402
R5823 75 1% 1/16W MF-LF 402

PLACE R5821-3 & FL5900-2 NEAR MINI-VGA CONNECTOR
ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

GPU_R2SET
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R5824 715 1% 1/16W MF-LF 402

GPU THERMAL SENSOR

PP3V3_PWRON
DEVELOPMENT C5890 0.1UF 20% 10V CERM 402
DEVELOPMENT C5891 100PF 5% 50V CERM 402
DEVELOPMENT R5891 10K 5% 1/16W MF-LF 402
DEVELOPMENT R5892 10K 5% 1/16W MF-LF 402

U5890 LM63CIMA SOI
VDD
DEVELOPMENT ALERT*/TACH U5890_ALERT_L
PWM U5890_PWM
SMBCLK I2C_GPU_DIODE_SCL
SMBDA I2C_GPU_DIODE_SDA
GND
GPU_DIODE_PLUS
GPU_DIODE_MINUS
DEVELOPMENT C5892 2200PF 5% 50V CERM 603

L5835 FERR-220-OHM 0805 PP1V8_GPU_TXVDDR VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
=PP1V8_GPU
C5835 10UF 20% 6.3V CERM 805 NOSTUFF
C5836 1UF 10% 6.3V CERM 402
C5837 0.1UF 20% 10V CERM 402
XW5835 SM GND_GPU_TXVSSR VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5830 1.8UH 0805 NOSTUFF PP1V8_GPU_TPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C5830 10UF 20% 6.3V CERM 805 NOSTUFF
C5831 1UF 10% 6.3V CERM 402
C5832 1UF 10% 6.3V CERM 402
C5833 0.1UF 20% 10V CERM 402
XW5830 SM GND_GPU_TPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5840 FERR-220-OHM 0805 PP1V8_GPU_VDDDI VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C5840 10UF 20% 6.3V CERM 805 NOSTUFF
C5841 1UF 10% 6.3V CERM 402
XW5840 SM GND_GPU_VSSDI VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5845 FERR-220-OHM 0805 PP1V8_GPU_AVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C5845 10UF 20% 6.3V CERM 805 NOSTUFF
C5846 1UF 10% 6.3V CERM 402
XW5845 SM GND_GPU_AVSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

PP2V5_GPU_A2VDD
C5855 10UF 20% 6.3V CERM 805 NOSTUFF
C5856 1UF 10% 6.3V CERM 402
XW5855 SM GND_GPU_A2VSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5865 FERR-220-OHM 0805 PP1V8_GPU_A2VDDQ VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C5865 10UF 20% 6.3V CERM 805 NOSTUFF
C5866 1UF 10% 6.3V CERM 402
XW5865 SM GND_GPU_A2VSSQ VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

GPU DVI & DACS

SYNC_MASTER=N/A SYNC_DATE=N/A

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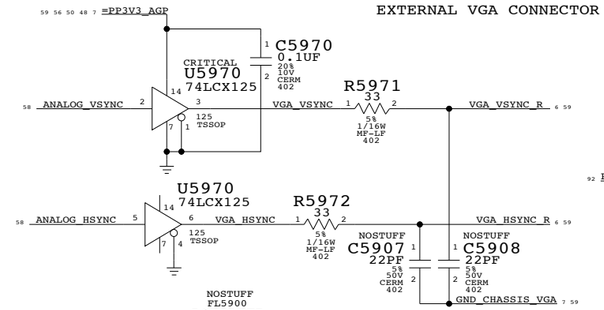
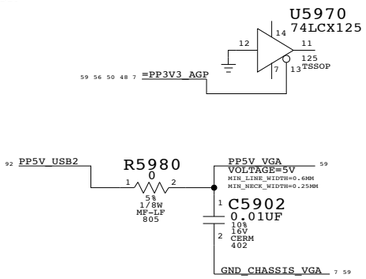
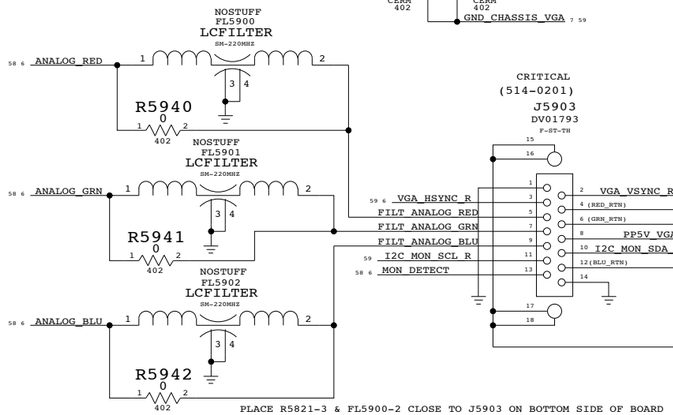
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 58 OF 102	

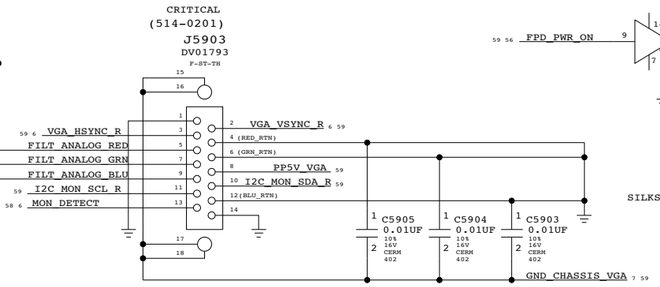
EXTERNAL VGA CONNECTOR

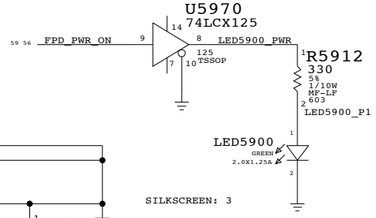






PLACE R5821-3 & FL5900-2 CLOSE TO J5903 ON BOTTOM SIDE OF BOARD



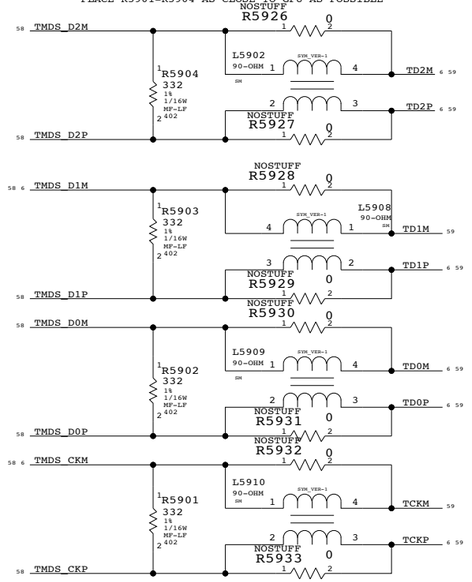


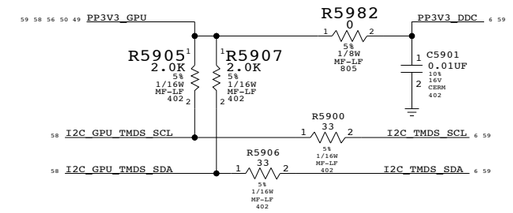
SILKSCREEN: 3

TABLE FOR PANEL POWER SEQUENCING (LOWER LEFT)

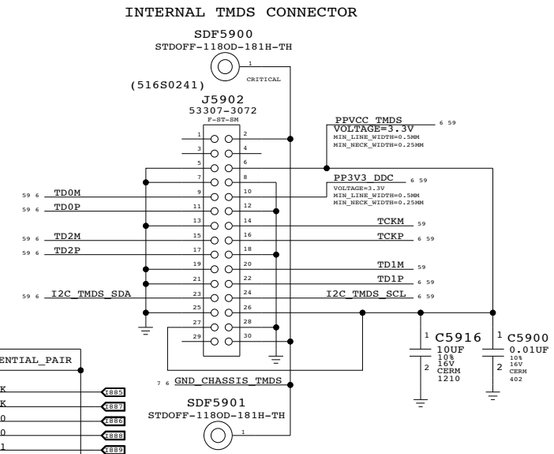
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S0114	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
376S0082	1	XSTR,MOSFET,P-CH,0.007OHM	Q5900	17_INCH_LCD
376S0225	1	XSTR,MOSFET,P-CH,0.02OHM	Q5900	20_INCH_LCD

PLACE R5901-R5904 AS CLOSE TO GPU AS POSSIBLE

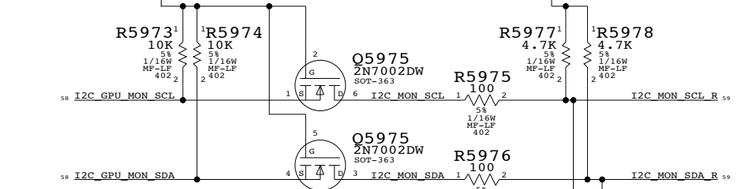


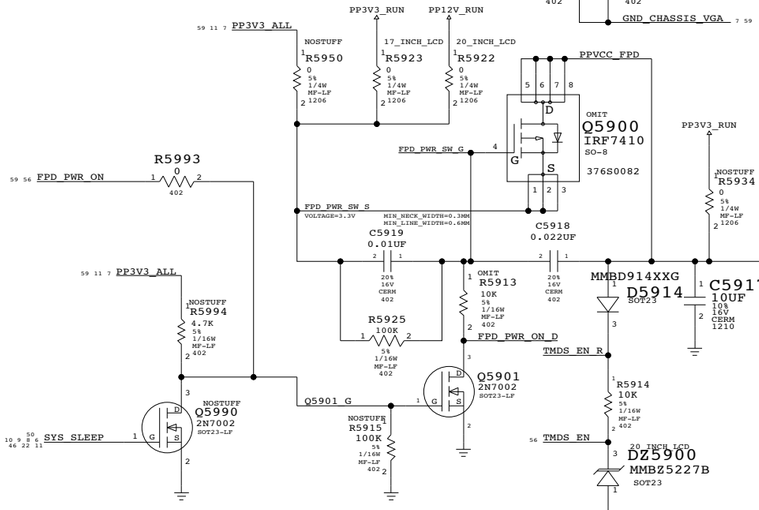


INTERNAL TMDS CONNECTOR



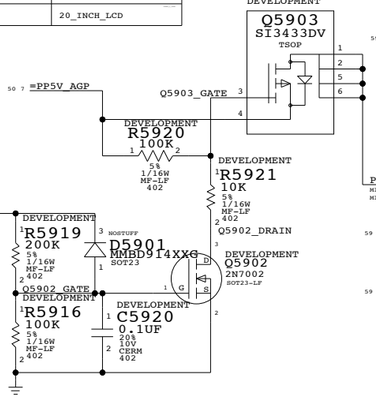
NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
59 6 TCKP	GPU_TMDS	GPU_TMDS	TCK	4885
59 TCKM	GPU_TMDS	GPU_TMDS	TCK	4887
59 6 TD0P	GPU_TMDS	GPU_TMDS	TD0	4886
59 6 TD0M	GPU_TMDS	GPU_TMDS	TD0	4888
59 6 TD1P	GPU_TMDS	GPU_TMDS	TD1	4889
59 TD1M	GPU_TMDS	GPU_TMDS	TD1	4890
59 6 TD2P	GPU_TMDS	GPU_TMDS	TD2	4892
59 6 TD2M	GPU_TMDS	GPU_TMDS	TD2	4891
59 6 FILT_ANALOG_GRN	GPU_VGA_75	GPU_VGA		4893
59 6 FILT_ANALOG_RED	GPU_VGA_75	GPU_VGA		4895
59 6 FILT_ANALOG_BLU	GPU_VGA_75	GPU_VGA		4894

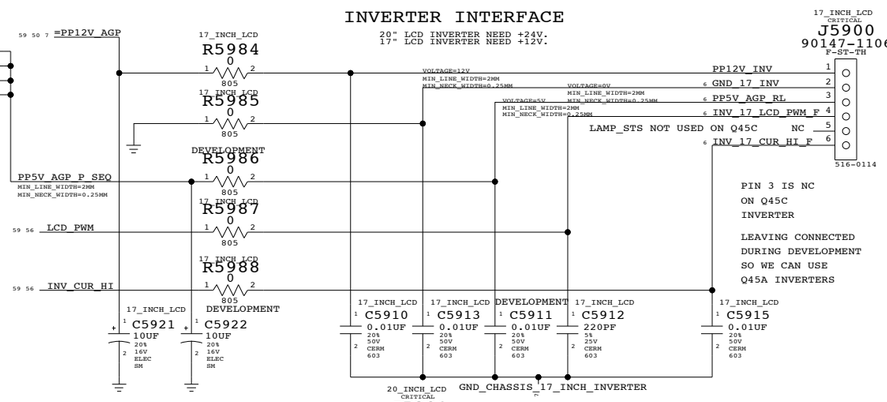


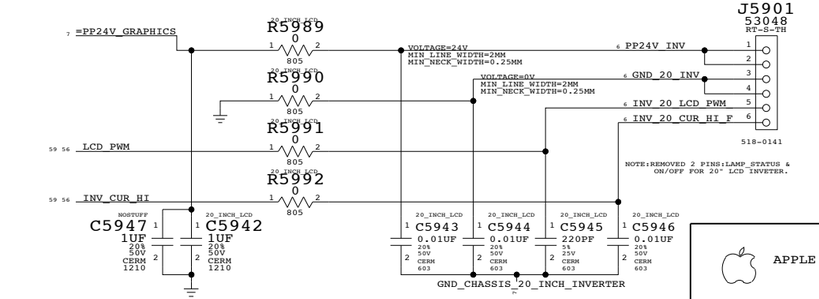


INVERTER INTERFACE

20" LCD INVERTER NEED +24V.
17" LCD INVERTER NEED +12V.







EXT VGA / TMDS AND INVERTER

SYNC_MASTER=N/A SYNC_DATE=N/A

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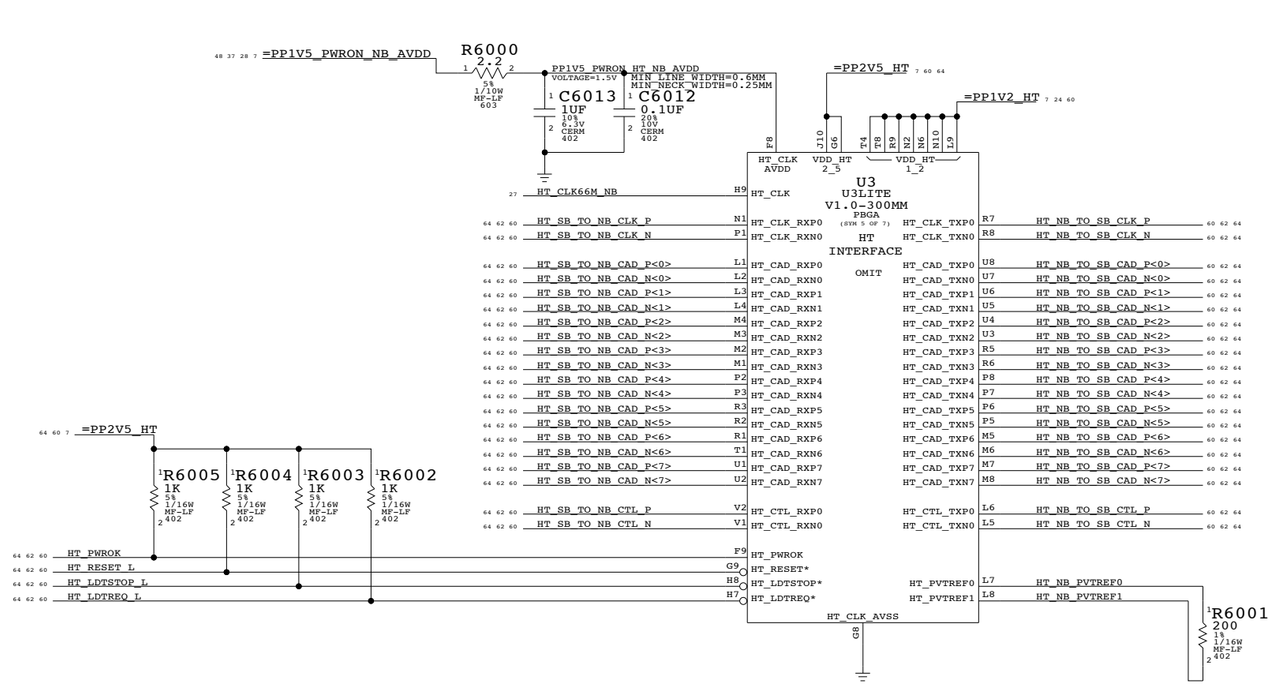
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 59 OF 102	

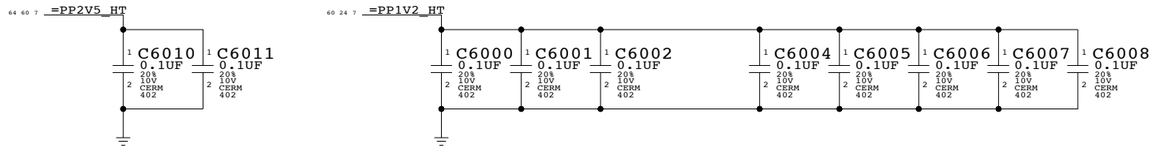


	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5	HT_2V5		189

HT_NB_TO_SB HT_SB_TO_NB
5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5
4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE CAN BE LOOSE
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH



U3LITE HT

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SCALE: NONE	SHT 60 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	P25MM	

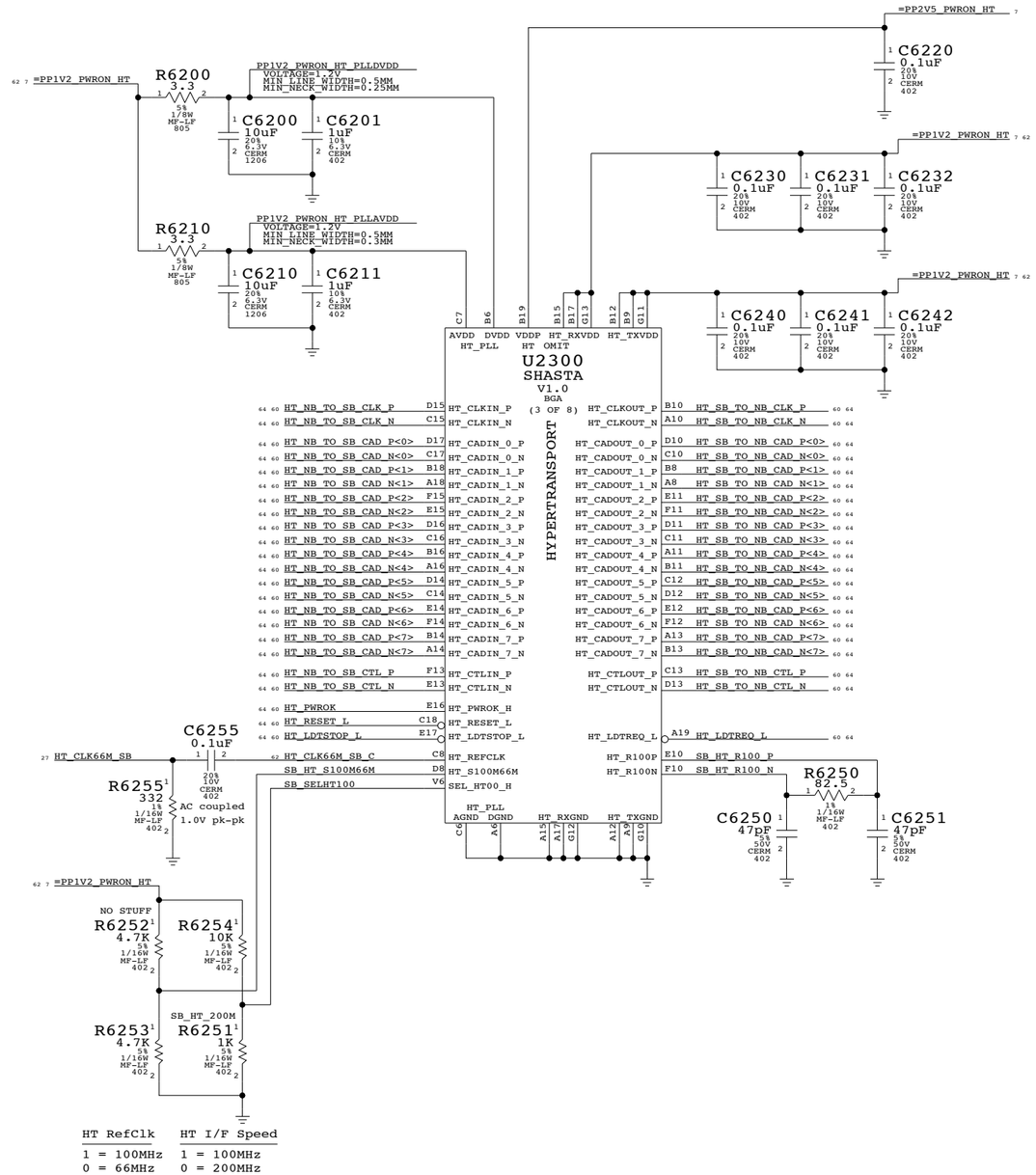
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



Shasta HyperTransport

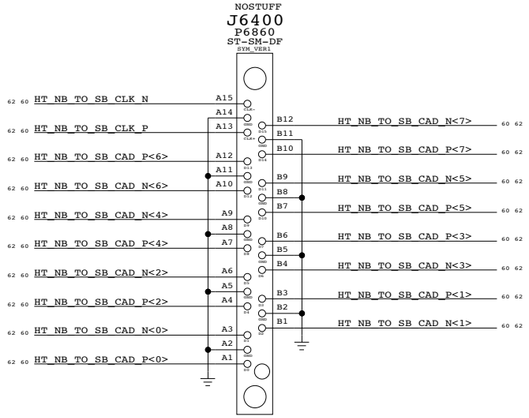
SYNC_MASTER=N/A SYNC_DATE=N/A

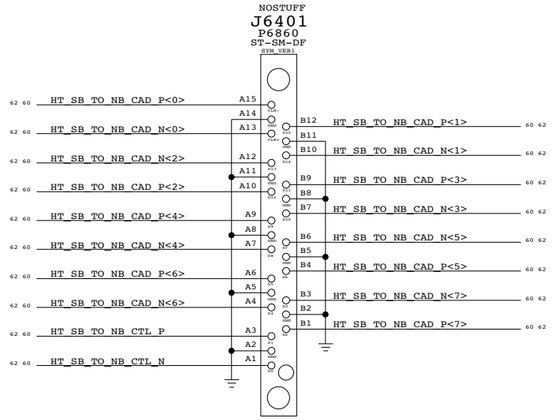
APPLE COMPUTER INC.

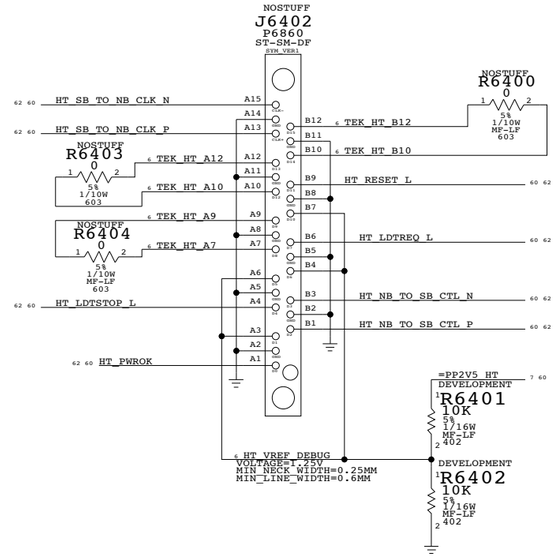
SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 62 OF 102	

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2







HT DEBUG CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 64 OF 102	

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

74	PCI_SB_AD<0>	RP7300	2	7	47	PCI_AD<0>	6 74 75 76 77
74	PCI_SB_AD<1>	RP7303	1	8	47	PCI_AD<1>	6 74 75 76 77
74	PCI_SB_AD<2>	RP7303	2	7	47	PCI_AD<2>	6 74 75 76 77
74	PCI_SB_AD<3>	RP7303	4	5	47	PCI_AD<3>	6 74 75 76 77
74	PCI_SB_AD<4>	RP7309	2	7	47	PCI_AD<4>	6 74 75 76 77
74	PCI_SB_AD<5>	RP7300	1	8	47	PCI_AD<5>	6 74 75 76 77
74	PCI_SB_AD<6>	RP7300	3	6	47	PCI_AD<6>	6 74 75 76 77
74	PCI_SB_AD<7>	RP7309	4	5	47	PCI_AD<7>	6 74 75 76 77
74	PCI_SB_AD<8>	RP7300	4	5	47	PCI_AD<8>	6 74 75 76 77
74	PCI_SB_AD<9>	RP7301	2	7	47	PCI_AD<9>	6 74 75 76 77
74	PCI_SB_AD<10>	RP7301	1	8	47	PCI_AD<10>	6 74 75 76 77
74	PCI_SB_AD<11>	RP7301	4	5	47	PCI_AD<11>	6 74 75 76 77
74	PCI_SB_AD<12>	RP7309	1	8	47	PCI_AD<12>	6 74 75 76 77
74	PCI_SB_AD<13>	RP7309	3	6	47	PCI_AD<13>	6 74 75 76 77
74	PCI_SB_AD<14>	RP7301	3	6	47	PCI_AD<14>	6 74 75 76 77
74	PCI_SB_AD<15>	RP7307	1	8	47	PCI_AD<15>	6 74 75 76 77
74	PCI_SB_AD<16>	RP7308	1	8	47	PCI_AD<16>	6 74 75 76 77

R7300
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<17>		1	2		PCI_AD<17>	6 74 75 76 77

74	PCI_SB_AD<18>	RP7307	2	7	47	PCI_AD<18>	6 74 75 76 77
74	PCI_SB_AD<19>	RP7306	3	6	47	PCI_AD<19>	6 74 75 76 77
74	PCI_SB_AD<20>	RP7305	1	8	47	PCI_AD<20>	6 74 75 76 77
74	PCI_SB_AD<21>	RP7305	2	7	47	PCI_AD<21>	6 74 76 77
74	PCI_SB_AD<22>	RP7302	1	8	47	PCI_AD<22>	6 74 76 77
74	PCI_SB_AD<23>	RP7302	3	6	47	PCI_AD<23>	6 74 76 77
74	PCI_SB_AD<24>	RP7304	1	8	47	PCI_AD<24>	6 74 75 76 77
74	PCI_SB_AD<25>	RP7306	4	5	47	PCI_AD<25>	6 74 75 76 77
74	PCI_SB_AD<26>	RP7305	3	6	47	PCI_AD<26>	6 74 75 76 77

R7301
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<27>		1	2		PCI_AD<27>	6 74 75 76 77

74	PCI_SB_AD<28>	RP7302	2	7	47	PCI_AD<28>	6 74 75 76 77
74	PCI_SB_AD<29>	RP7304	4	5	47	PCI_AD<29>	6 74 75 76 77
74	PCI_SB_AD<30>	RP7302	4	5	47	PCI_AD<30>	6 74 75 76 77
74	PCI_SB_AD<31>	RP7304	2	7	47	PCI_AD<31>	6 74 75 76 77
74	PCI_SB_CBE_L<0>	RP7303	3	6	47	PCI_CBE_L<0>	6 74 76 77
74	PCI_SB_CBE_L<1>	RP7306	2	7	47	PCI_CBE_L<1>	6 74 76 77
74	PCI_SB_CBE_L<2>	RP7305	4	5	47	PCI_CBE_L<2>	6 74 76 77
74	PCI_SB_CBE_L<3>	RP7304	3	6	47	PCI_CBE_L<3>	6 74 76 77
74	PCI_SB_DEVSEL_L	RP7306	1	8	47	PCI_DEVSEL_L	6 74 76 77
74	PCI_SB_FRAME_L	RP7307	4	5	47	PCI_FRAME_L	6 74 76 77
74	PCI_SB_IRDY_L	RP7307	3	6	47	PCI_IRDY_L	6 74 76 77
74	PCI_SB_TRDY_L	RP7308	3	6	47	PCI_TRDY_L	6 74 76 77
74	PCI_SB_STOP_L	RP7308	4	5	47	PCI_STOP_L	6 74 76 77
74	PCI_SB_PAR	RP7308	2	7	47	PCI_PAR	6 74 76 77

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. E

SCALE NONE | SHT 73 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCI_AD	PCI		PCI_AD<31..28> 6 73 75 76 77
PCI_AD27	PCI		PCI_AD<27> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<26..24> 6 73 75 76 77
PCI_AD23	PCI		PCI_AD<23> 6 73 76 77
PCI_AD22	PCI		PCI_AD<22> 6 73 76 77
PCI_AD21	PCI		PCI_AD<21> 6 73 76 77
PCI_AD20	PCI		PCI_AD<20> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<19..18> 6 73 75 76 77
PCI_AD17	PCI		PCI_AD<17> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<16..0> 6 73 75 76 77
PCI	PCI		PCI_CBE_L<3..0> 6 73 76 77
PCI	PCI		PCI_PAR 6 73 76 77
PCI_CTL	PCI		PCI_DEVSEL_L 6 73 74 76 77
PCI_CTL	PCI		PCI_FRAME_L 6 73 74 76 77
PCI_CTL	PCI		PCI_IRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_TRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_STOP_L 6 73 74 76 77

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

7 =PP3V3_SB_PCI

NO STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

=PP2V5_PWRON_SB 7 23 25 88

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

VDDOPC: AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19
PCIVDDP: B20 J18 N20 U20

U2300 SHASTA V1.0 BGA (4 OF 8) OMIT

PCI

27 PCI_CLK66M_SB_INT	AB9	PCIBR_CLK_H	
27 8 PCI_CLK33M_SB_EXT	U19	PCI1CLK_H	
"Slot A" - AD17			
76 74 6 PCI_SLOTA_REQ_L	AB18	PCI1REQ_0_L	
76 74 6 PCI_SLOTA_GNT_L	AA18	PCI1GNT_0_L	
"Slot G" - AD27			
77 74 PCI_SLOTG_REQ_L	AB20	PCI1REQ_1_L	
77 74 PCI_SLOTG_GNT_L	AB19	PCI1GNT_1_L	
"Slot D" - AD20			
74 PCI_SLOTD_REQ_L	V17	PCI1REQ_2_L	
74 PCI_SLOTD_GNT_L	V18	PCI1GNT_2_L	
76 75 6 ROM_CS_L	AB8	ROMCS_L	
76 75 6 ROM_OE_L	AA9	ROMOE_L	
76 75 6 ROM_WE_L	Y10	ROMRW_L	

PCI1AD_0_H	L18	PCI_SB_AD<0>	73
PCI1AD_1_H	K19	PCI_SB_AD<1>	73
PCI1AD_2_H	L22	PCI_SB_AD<2>	73
PCI1AD_3_H	M22	PCI_SB_AD<3>	73
PCI1AD_4_H	M18	PCI_SB_AD<4>	73
PCI1AD_5_H	L20	PCI_SB_AD<5>	73
PCI1AD_6_H	M21	PCI_SB_AD<6>	73
PCI1AD_7_H	N16	PCI_SB_AD<7>	73
PCI1AD_8_H	M20	PCI_SB_AD<8>	73
PCI1AD_9_H	P22	PCI_SB_AD<9>	73
PCI1AD_10_H	M17	PCI_SB_AD<10>	73
PCI1AD_11_H	N18	PCI_SB_AD<11>	73
PCI1AD_12_H	M19	PCI_SB_AD<12>	73
PCI1AD_13_H	N19	PCI_SB_AD<13>	73
PCI1AD_14_H	P21	PCI_SB_AD<14>	73
PCI1AD_15_H	R22	PCI_SB_AD<15>	73
PCI1AD_16_H	P20	PCI_SB_AD<16>	73
PCI1AD_17_H	V21	PCI_SB_AD<17>	73
PCI1AD_18_H	P18	PCI_SB_AD<18>	73
PCI1AD_19_H	T20	PCI_SB_AD<19>	73
PCI1AD_20_H	R16	PCI_SB_AD<20>	73
PCI1AD_21_H	R17	PCI_SB_AD<21>	73
PCI1AD_22_H	W21	PCI_SB_AD<22>	73
PCI1AD_23_H	Y22	PCI_SB_AD<23>	73
PCI1AD_24_H	R18	PCI_SB_AD<24>	73
PCI1AD_25_H	T19	PCI_SB_AD<25>	73
PCI1AD_26_H	T18	PCI_SB_AD<26>	73
PCI1AD_27_H	Y21	PCI_SB_AD<27>	73
PCI1AD_28_H	W20	PCI_SB_AD<28>	73
PCI1AD_29_H	T16	PCI_SB_AD<29>	73
PCI1AD_30_H	AA21	PCI_SB_AD<30>	73
PCI1AD_31_H	T17	PCI_SB_AD<31>	73
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	73
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	73
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	73
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	73
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	73
PCI1FRAME_L	T21	PCI_SB_FRAME_L	73
PCI1IRDY_L	R21	PCI_SB_IRDY_L	73
PCI1TRDY_L	P19	PCI_SB_TRDY_L	73
PCI1STOP_L	P17	PCI_SB_STOP_L	73
PCI1PAR_H	N17	PCI_SB_PAR	73
PCI1RST_L	U18	SB_PCI_RESET_L	

=PP3V3_PCI 7 25 74 75 76 77

RP7400 4.7K 5% 1/16W SM-LF
- 2 — 7: PCI_SLOTA_REQ_L 6 74 76
- 1 — 8: PCI_SLOTA_GNT_L 6 74 76
- 4 — 5: PCI_SLOTG_REQ_L 74 77
- 3 — 6: PCI_SLOTG_GNT_L 74 77

RP7401 4.7K 5% 1/16W SM-LF
- 3 — 6: PCI_SLOTD_REQ_L 74
- 4 — 5: PCI_SLOTD_GNT_L 74

=PP3V3_PWRON_SB 7 23 25

R7455 4.7K 5% 1/16W MF-LF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF-LF 402

U7450 MC74VHC1G08 SOT23-5

77 25 8 SYS_WARM_RESET_L

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

PCI_RESET_L 6 8 56

77 76 75 74 25 7 =PP3V3_PCI

RP7402 4.7K 5% 1/16W SM-LF
- 77 76 74 73 6 PCI_DEVSEL_L — 3 6
- 77 76 74 73 6 PCI_FRAME_L — 4 5
- 77 76 74 73 6 PCI_IRDY_L — 2 7
- 77 76 74 73 6 PCI_TRDY_L — 1 8

RP7401 4.7K 5% 1/16W SM-LF
- 77 76 74 73 6 PCI_STOP_L — 7 2

Shasta PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 74 OF 102	

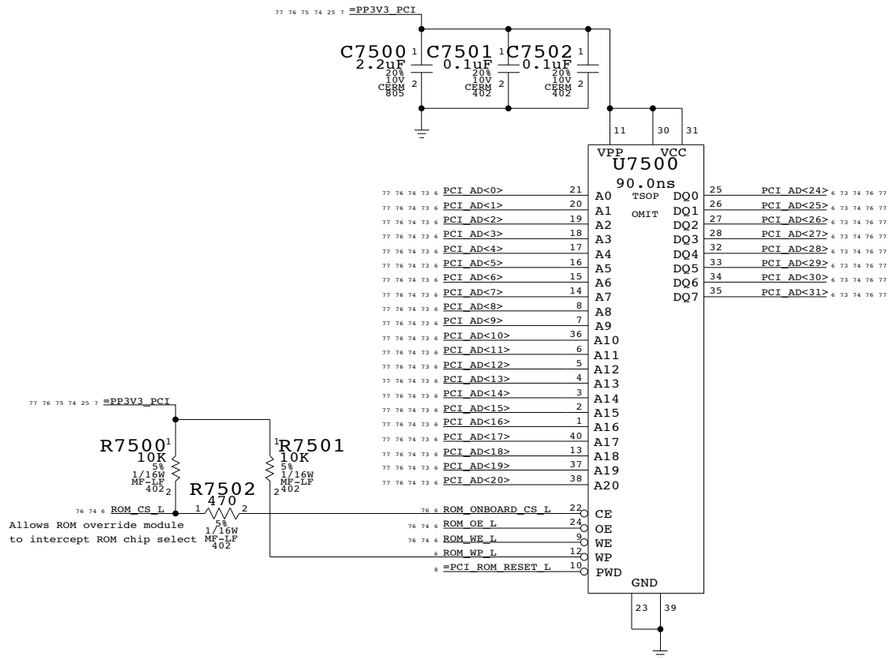
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	75	102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI CLK33M AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR

77 75 74 25 7 =PP3V3_PCI

SDF7600
STDOFF-3MMOD5MMH-TH

NOSTUFF
C7650 1 2 10UF 20% 6.3V CERM 1206

C7651 1 2 1UF 10% 6.3V CERM 402

C7652 1 2 1UF 10% 6.3V CERM 402

CRITICAL
J7650
20-5602-080-041-829
F-ST-SM

	1	2	PCI_AD<31>	6 73 74 75 77
77 75 74 73 6 PCI_AD<30>	3	4	AIRPORT_CLKRUN_L_PD	6
	5	6	TP_AP_PME_L	
77 75 74 73 6 PCI_AD<27>	7	8	PCI_SLOTA_GNT_L	6 74
74 6 PCI_SLOTA_REQ_L	9	10		
77 75 74 73 6 PCI_AD<25>	11	12		
77 75 74 73 6 PCI_AD<29>	13	14	PCI_AD<24>	6 73 74 75 77
	15	16	PCI_AIRPORT_RESET_L	8
77 74 73 6 PCI_CBE_L<3>	17	18	PCI_AD<28>	6 73 74 75 77
77 75 74 73 6 PCI_AD<26>	19	20		
77 74 73 6 PCI_AD<22>	21	22	PCI_AD<23>	6 73 74 77
6 PCI_SLOTA_IDSEL	23	24		
77 75 74 73 6 PCI_AD<19>	25	26	PCI_AD<20>	6 73 74 75 77
77 74 73 6 PCI_AD<21>	27	28	PCI_FRAME_L	6 73 74 77
77 74 73 6 PCI_IRDY_L	29	30	PCI_AD<17>	6 73 74 75 76 77
77 75 74 73 6 PCI_AD<18>	31	32		
77 74 73 6 PCI_DEVSEL_L	33	34	PCI_TRDY_L	6 73 74 77
	35	36		
76 8 _PCI_CLK33M_AIRPORT	37	38	PCI_CBE_L<2>	6 73 74 77
77 74 73 6 PCI_STOP_L	39	40	PCI_AD<16>	6 73 74 75 77
77 75 74 73 6 PCI_AD<12>	41	42		
77 74 73 6 PCI_PAR	43	44		
	45	46		
77 75 74 73 6 PCI_AD<8>	47	48	PCI_AD<14>	6 73 74 75 77
77 75 74 73 6 PCI_AD<9>	49	50	PCI_AD<13>	6 73 74 75 77
77 74 73 6 PCI_CBE_L<0>	51	52		
	53	54	PCI_AD<10>	6 73 74 75 77
77 75 74 73 6 PCI_AD<7>	55	56	PCI_AD<15>	6 73 74 75 77
77 75 74 73 6 PCI_AD<3>	57	58	AP_ALT_ANT	
77 75 74 73 6 PCI_AD<6>	59	60	PCI_CBE_L<1>	6 73 74 77
	61	62	PCI_AD<4>	6 73 74 75 77
77 75 74 73 6 PCI_AD<1>	63	64		
77 75 74 73 6 PCI_AD<5>	65	66	PCI_AD<11>	6 73 74 75 77
77 75 74 73 6 PCI_AD<0>	67	68	ROM_WE_L	6 74 75
	69	70	PCI_AD<2>	6 73 74 75 77
	71	72		
91 USB2_P<4> 6 USB_BT_P	73	74	PCI_SLOTA_INT_L	6 25
91 USB2_N<4> 6 USB_BT_N	75	76	ROM_OE_L	6 74 75
MAKE_BASE=TRUE	77	78	ROM_ONBOARD_CS_L	6 75
MAKE_BASE=TRUE	79	80	ROM_CS_L	6 74 75

516S0285

R7650 1 2 10K 5% 1/16W MF-LF 402

R7651 1 2 22 5% 1/16W MF-LF 402
77 76 75 74 73 6 PCI_AD<17>

R7660 1 2 15K 5% 1/16W MF-LF 402

R7661 1 2 15K 5% 1/16W MF-LF 402

7 _PP3V3_PWRON_BT
91 USB2_OC<4>

C7660 1 2 1UF 10% 6.3V CERM 402

SDF7601
STDOFF-3MMOD5MMH-TH1

AIRPORT & BLUETOOTH			
SYNC_MASTER=N/A	SYNC_DATE=N/A		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6772	REV. E
	SCALE NONE	SHT 76 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

=PCI_CLK33M_USB2 8 77

Page Notes

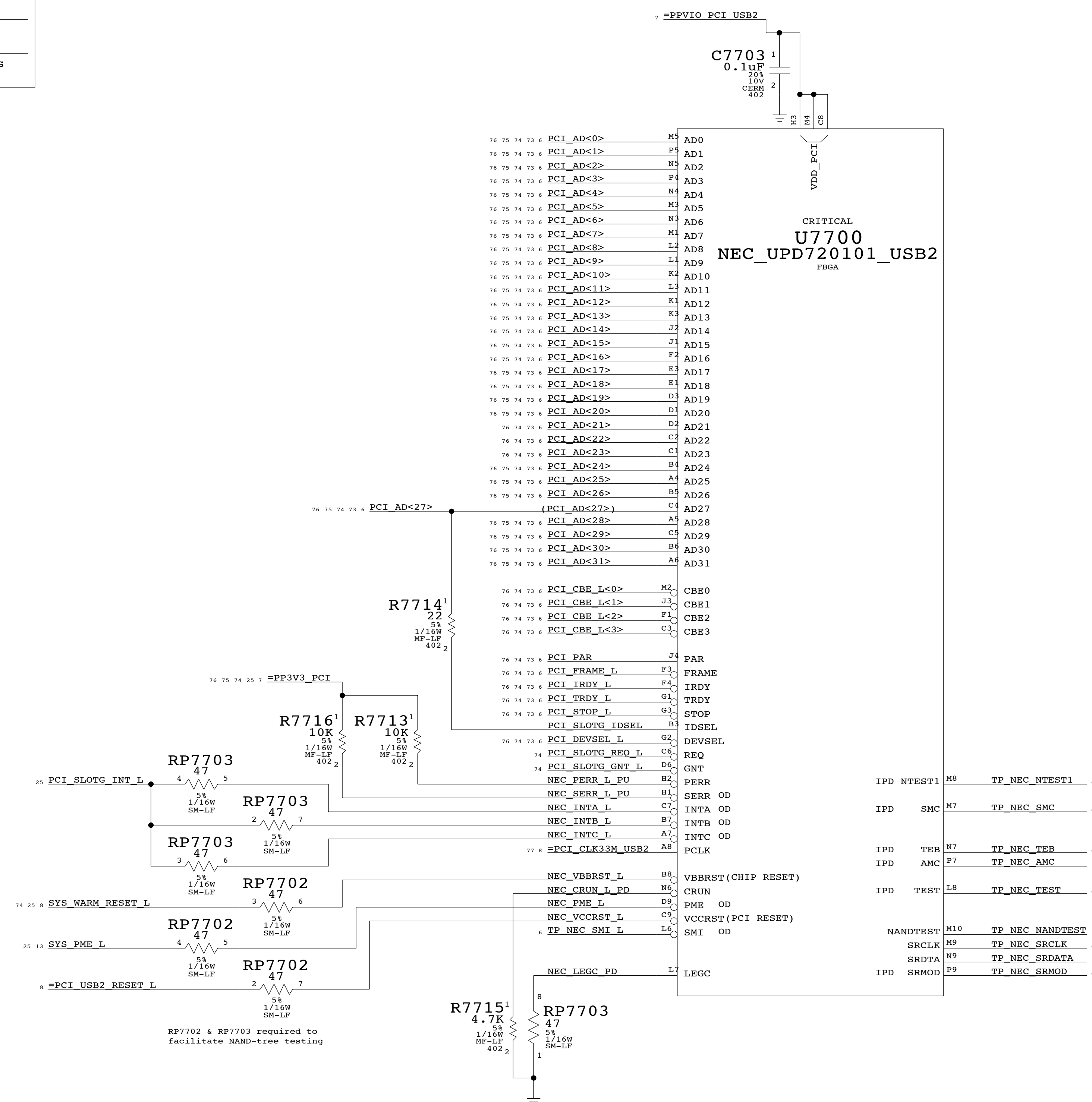
Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.



USB 2.0 PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE NONE	SHT 77	OF 102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD				UATA_DD<15..8>
UATA_DD7				UATA_DD<7>
UATA_DD				UATA_DD<6..0>
UATA_HOST				UATA_DA<2..0>
UATA_HOST				UATA_CS0_L
UATA_HOST				UATA_CS1_L
UATA_HOST				UATA_HSTROBE
UATA_HOST				UATA_STOP
UATA_HOST_R				UATA_DMACK_L
UATA_HOST_R				UATA_RESET_L
UATA_DEV_R_C				UATA_DSTROBE
UATA_DEV_R				UATA_DMARQ
UATA_DEV_R				UATA_INTRQ

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

=PP1V2_PWRON_DISK_SB

R8010 0 5% 1/8W MF-LF 805

SATA_VDD x 5

PP1V2_PWRON_DISK_SB_R
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

C8000 1UF 10% 6.3V CERM 402
C8001 1UF 10% 6.3V CERM 402
C8002 1UF 10% 6.3V CERM 402
C8003 1UF 10% 6.3V CERM 402
C8004 1UF 10% 6.3V CERM 402

AB14 AB17 T14 W15 Y18

SATA_VDD

U2300 SHASTA V1.0 BGA (5 OF 8) OMIT

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>
UD_IDEDD_1_H	H7	UATA_DD_R<1>
UD_IDEDD_2_H	H6	UATA_DD_R<2>
UD_IDEDD_3_H	E2	UATA_DD_R<3>
UD_IDEDD_4_H	C1	UATA_DD_R<4>
UD_IDEDD_5_H	C2	UATA_DD_R<5>
UD_IDEDD_6_H	E3	UATA_DD_R<6>
UD_IDEDD_7_H	G6	UATA_DD_R<7>
UD_IDEDD_8_H	G5	UATA_DD_R<8>
UD_IDEDD_9_H	D4	UATA_DD_R<9>
UD_IDEDD_10_H	G7	UATA_DD_R<10>
UD_IDEDD_11_H	F6	UATA_DD_R<11>
UD_IDEDD_12_H	C3	UATA_DD_R<12>
UD_IDEDD_13_H	F5	UATA_DD_R<13>
UD_IDEDD_14_H	E5	UATA_DD_R<14>
UD_IDEDD_15_H	D5	UATA_DD_R<15>
UD_IDEDA0_H	E6	UATA_DA_R<0>
UD_IDEDA1_H	C4	UATA_DA_R<1>
UD_IDEDA2_H	D6	UATA_DA_R<2>
UD_IDECS1FX_L	B3	UATA_CS0_L_R
UD_IDECS3FX_L	B4	UATA_CS1_L_R
UD_IDEDMACK_L	E8	UATA_DMACK_L_R
UD_IDERD_L	E4	UATA_HSTROBE_R
UD_IDEWR_L	D3	UATA_STOP_R
UD_IDERST_L	E7	UATA_RESET_L_R

DSTROBE aka: IORDY/HDMARDY*

HSTROBE aka: DIOR*

STOP aka: DIOW*

UATA_DSTROBE	F9	UD_IDECHRDY_H
UATA_DMARQ	D7	UD_IDEDMARQ_H
UATA_INTRQ	C5	UD_IDEINTRQ_H

SATA_RXD_P1_C	Y17	RXDP1	TXDP1 AA16 SATA_TXD_P1
SATA_RXD_N1_C	Y16	RXDN1	TXDN1 AB16 SATA_TXD_N1
SATA_RXD_P2_C	AB15	RXDP2	TXDP2 Y15 SATA_TXD_P2
SATA_RXD_N2_C	AA15	RXDN2	TXDN2 Y14 SATA_TXD_N2

SATA 0 SATA 1

SATA_GND

AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/16W MF-LF 402

UATA_DD_R<0>	RP8000 33 5% 1/16W SM-LF	UATA_DD<0>
UATA_DD_R<1>	RP8000 33 5% 1/16W SM-LF	UATA_DD<1>
UATA_DD_R<2>	RP8000 33 5% 1/16W SM-LF	UATA_DD<2>
UATA_DD_R<3>	RP8003 33 5% 1/16W SM-LF	UATA_DD<3>
UATA_DD_R<4>	RP8001 33 5% 1/16W SM-LF	UATA_DD<4>
UATA_DD_R<5>	RP8001 33 5% 1/16W SM-LF	UATA_DD<5>
UATA_DD_R<6>	RP8003 33 5% 1/16W SM-LF	UATA_DD<6>
UATA_DD_R<7>	RP8002 33 5% 1/16W SM-LF	UATA_DD<7>
UATA_DD_R<8>	RP8002 33 5% 1/16W SM-LF	UATA_DD<8>
UATA_DD_R<9>	RP8003 33 5% 1/16W SM-LF	UATA_DD<9>
UATA_DD_R<10>	RP8000 33 5% 1/16W SM-LF	UATA_DD<10>
UATA_DD_R<11>	RP8002 33 5% 1/16W SM-LF	UATA_DD<11>
UATA_DD_R<12>	RP8001 33 5% 1/16W SM-LF	UATA_DD<12>
UATA_DD_R<13>	RP8002 33 5% 1/16W SM-LF	UATA_DD<13>
UATA_DD_R<14>	RP8004 33 5% 1/16W SM-LF	UATA_DD<14>
UATA_DD_R<15>	RP8003 33 5% 1/16W SM-LF	UATA_DD<15>
UATA_DA_R<0>	RP8004 33 5% 1/16W SM-LF	UATA_DA<0>
UATA_DA_R<1>	RP8001 33 5% 1/16W SM-LF	UATA_DA<1>
UATA_DA_R<2>	RP8004 33 5% 1/16W SM-LF	UATA_DA<2>
UATA_RESET_L_R	RP8004 33 5% 1/16W SM-LF	UATA_RESET_L
UATA_CS0_L_R	R8000 33 5% 1/16W MF-LF 402	UATA_CS0_L
UATA_CS1_L_R	R8001 33 5% 1/16W MF-LF 402	UATA_CS1_L
UATA_HSTROBE_R	R8002 22 5% 1/16W MF-LF 402	UATA_HSTROBE
UATA_STOP_R	R8003 22 5% 1/16W MF-LF 402	UATA_STOP
UATA_DMACK_L_R	R8004 22 5% 1/16W MF-LF 402	UATA_DMACK_L

Shasta Disk

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 80 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
UATA_DD<15..8>	UATA_DD		
UATA_DD<7>	UATA_DD7		
UATA_DD<6..0>	UATA_DD		
UATA_DA<2..0>	UATA_HOST		
UATA_CS0_L	UATA_HOST		
UATA_CS1_L	UATA_HOST		
UATA_HSTROBE	UATA_HOST		
UATA_STOP	UATA_HOST		
UATA_DMACK_L	UATA_HOST_R		
UATA_RESET_L	UATA_HOST_R		
UATA_DSTROBE	UATA_DEV_R_C		
UATA_DMARQ	UATA_DEV_R		
UATA_INTRQ	UATA_DEV_R		

SATA CONNECTORS

J8300
LD18077-S04
M-ST-TH
518-0157

C8304 0.1UF 20% 10V CERM 402
C8305 0.1UF 20% 10V CERM 402
C8307 0.1UF 20% 10V CERM 402
C8308 0.1UF 20% 10V CERM 402

SATA_TXD_P1_C → SATA_TXD_P1
SATA_TXD_N1_C → SATA_TXD_N1
SATA_RXD_N1 → SATA_RXD_N1_C
SATA_RXD_P1 → SATA_RXD_P1_C

SATA_TXD_P2 → TP_SATA_TXD_P2 (MAKE_BASE=TRUE)
SATA_TXD_N2 → TP_SATA_TXD_N2 (MAKE_BASE=TRUE)
SATA_RXD_N2_C → TP_SATA_RXD_N2_C (MAKE_BASE=TRUE)
SATA_RXD_P2_C → TP_SATA_RXD_P2_C (MAKE_BASE=TRUE)

HD POWER

CRITICAL
J8303
S05B-XA
M-ST-TH
518-0144

=PP5V_DISK
=PP12V_DISK
=PP3V3_DISK

PATA CONNECTOR

=PP5V_PATA
=PP3V3_PATA

ATA-6 spec does not call out R8180 or R8182

NO STUFF R8313 10K 5% 1/16W MF-LF 402
NO STUFF R8311 10K 5% 1/16W MF-LF 402
R8314 4.7K 5% 1/16W MF-LF 402 Per ATA Spec
R8312 1K 5% 1/16W MF-LF 402 Obsolete

CRITICAL
J8301
804RVS-050505R
F-ST-SM

Sourced by drive
Terminate near connector

	NC 1	2	NC
		4	NC
UATA_RESET_L	5	6	UATA_DD<8>
UATA_DD<7>	7	8	UATA_DD<9>
UATA_DD<6>	9	10	UATA_DD<10>
UATA_DD<5>	11	12	UATA_DD<11>
UATA_DD<4>	13	14	UATA_DD<12>
UATA_DD<3>	15	16	UATA_DD<13>
UATA_DD<2>	17	18	UATA_DD<14>
UATA_DD<1>	19	20	UATA_DD<15>
UATA_DD<0>	21	22	
	23	24	UATA_HSTROBE
UATA_STOP	25	26	
UATA_DSTROBE_R	27	28	UATA_DMACK_L
UATA_INTRQ_R	29	30	UATA_IOCS16_PU
UATA_DA<1>	31	32	NC
UATA_DA<0>	33	34	UATA_DA<2>
UATA_CS0_L	35	36	UATA_CS1_L
UATA_DASP_L	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
UATA_CSEL_PD	47	48	
	NC 49	50	NC

516S0235

R8315 82 5% 1/16W MF-LF 402 (UATA_DSTROBE)
R8316 82 5% 1/16W MF-LF 402 (UATA_INTRQ)
NO STUFF C8301 10pF 5% 50V CERM 402
R8320 82 5% 1/16W MF-LF 402 (UATA_DMARQ → UATA_DMARQ_R)

ATA-6 spec does not call out C8177

=PP5V_PATA
DEVELOPMENT R8321 499 1% 1/16W MF-LF 402 Per ATA Spec
R8319 5.6K 5% 1/16W MF-LF 402 Per ATA Spec
R8318 0 5% 1/16W MF-LF 402 Per ATA Spec
R8317 6.2K 5% 1/16W MF-LF 402 PER ATA7 SPEC

DEVELOPMENT LED8301 GREEN 2.0X1.25A
UATA_DASP_L_DS

"UATA ACTIVE"

DISK CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 83 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK		P25MM	
ENET_RX_CLK		P25MM	
ENET_GBE_REF		P25MM	
ENET_TX_CLK		P25MM	
ENET_RX			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_TX			
ENET_TX_CTL			
ENET_TX_CTL			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_MDC			
ENET_MDIO			

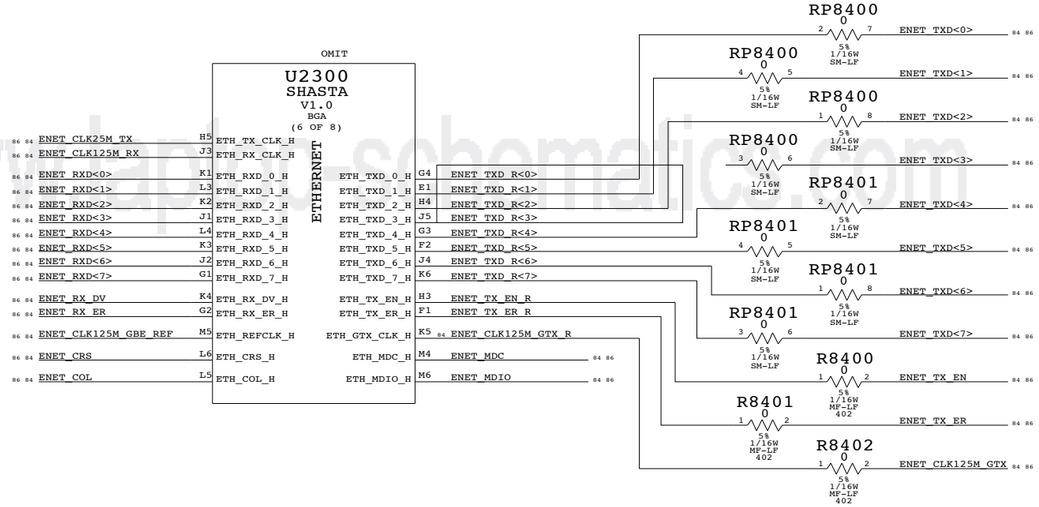
ENET_CLK25M_TX 84 86
ENET_CLK125M_RX 84 86
ENET_CLK125M_GBE_REF 84 86
ENET_CLK125M_GTX 84 86
ENET_CLK125M_GTX_R 84
ENET_RXD<7..0> 84 86
ENET_RX_DV 84 86
ENET_RX_ER 84 86
ENET_TXD<7..0> 84 86
ENET_TX_EN 84 86
ENET_TX_ER 84 86
ENET_CRS 84 86
ENET_COL 84 86
ENET_MDC 84 86
ENET_MDIO 84 86

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Shasta Ethernet

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE: NONE

SHT 84 OF 102

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	P25MM			ENET_CLK125M_GBE_REF_R
	P25MM			ENET_CLK125M_RX_R
	P25MM			ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTAL	P25MM			VESTA_CLK25M_XTALI
	P25MM			VESTA_CLK25M_XTALO
	P25MM			VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38 mms
Length Tolerance: 50 mils
Primary Max Sep: 5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

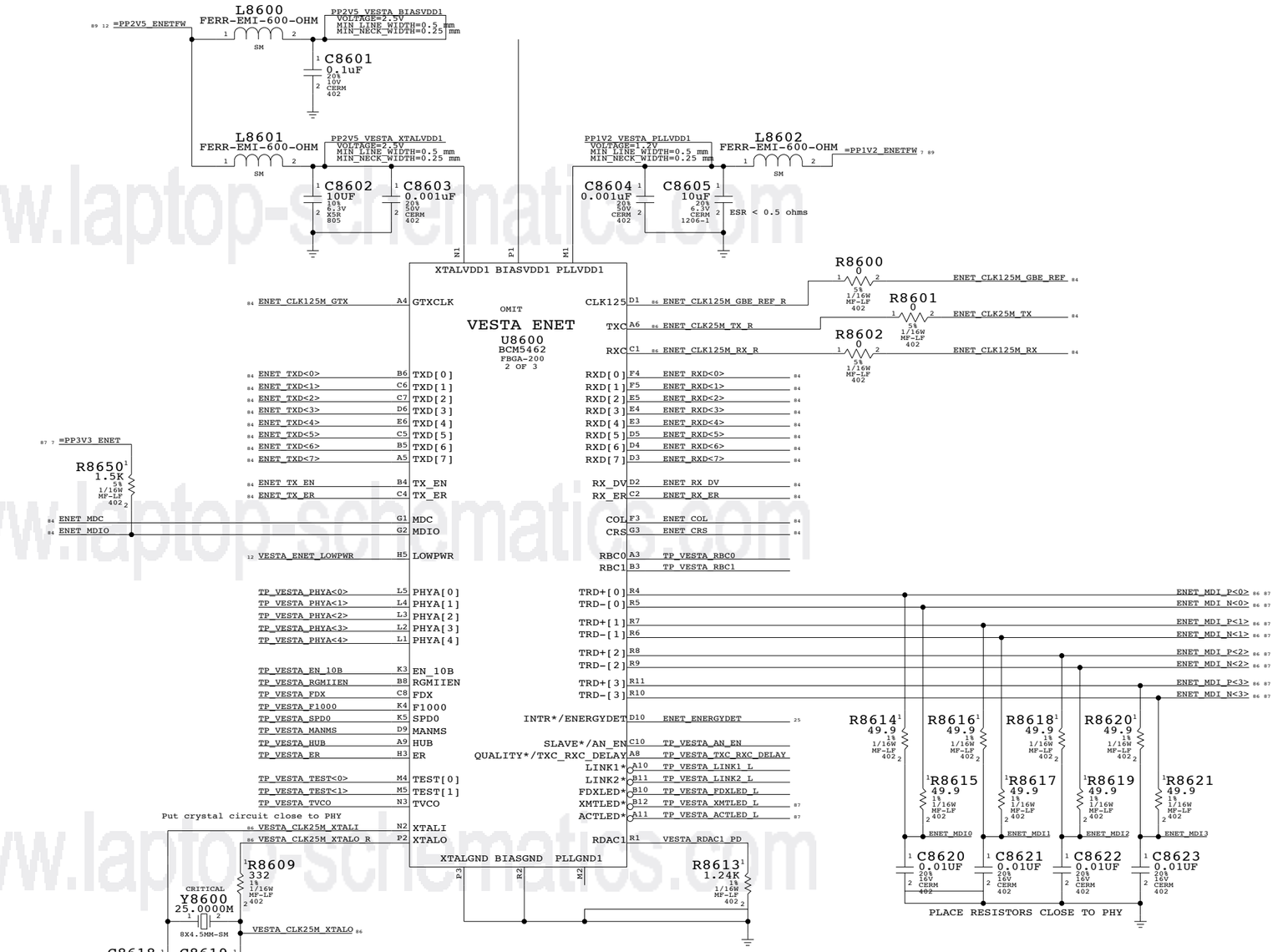
HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

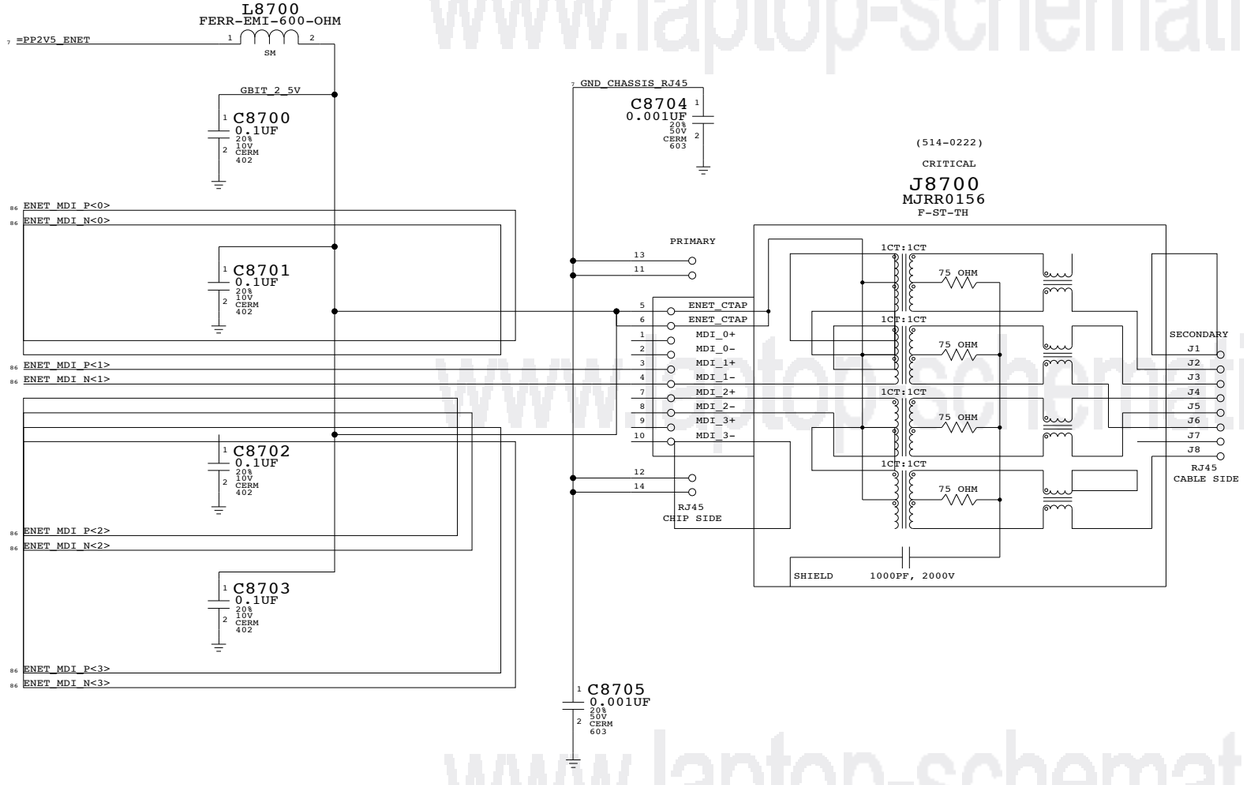


Vesta Ethernet PHY

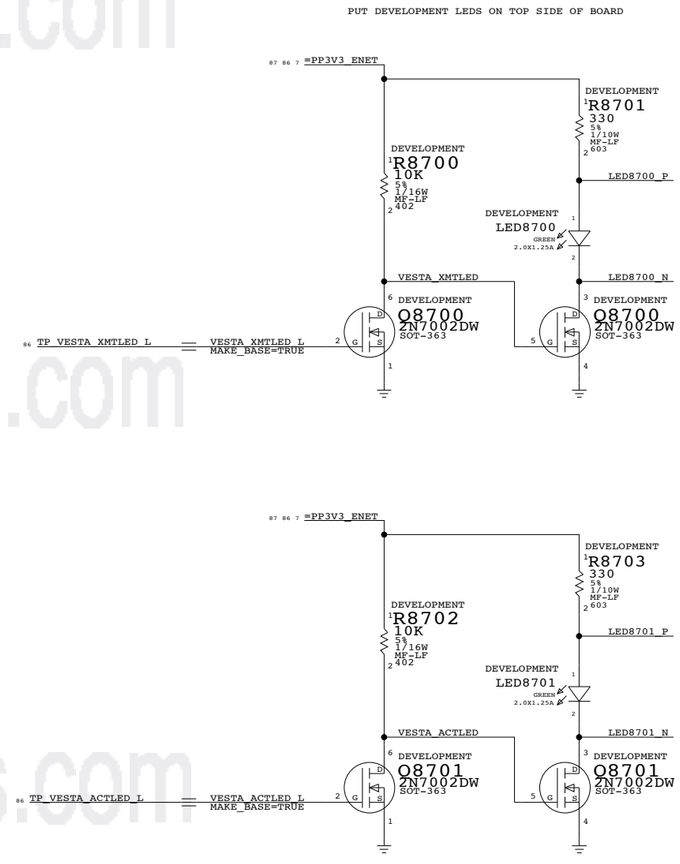
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 86 OF 102	



PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD



ETHERNET CONNECTOR

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 87 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FW				FW_DATA<7..0> 88 89
FW				FW_CTL<1..0> 88 89
FW_LPS				FW_LPS 88 89
FW_LREQ				FW_LREQ 88 89
FW_PINT				FW_PINT 88 89
FW_LCLK		P25MM		FW_CLK98M_LCLK 88 89
FW_PCLK		P25MM		FW_CLK98M_PCLK 88 89
		P25MM		FW_CLK98M_LCLK_R 88

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

74 25 23 7 =PP2V5_PWRON_SB

C8800 0.1uF 20% 10V CERM 402
C8801 0.1uF 20% 10V CERM 402
C8802 0.1uF 20% 10V CERM 402

N5 J7 A4 FWVDDP

U2300 OMIT
SHASTA
V1.0
BGA
(7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	88 89
PHY_DATA_1_H	P5	FW_DATA<1>	88 89
PHY_DATA_2_H	N1	FW_DATA<2>	88 89
PHY_DATA_3_H	M7	FW_DATA<3>	88 89
PHY_DATA_4_H	N6	FW_DATA<4>	88 89
PHY_DATA_5_H	L1	FW_DATA<5>	88 89
PHY_DATA_6_H	M3	FW_DATA<6>	88 89
PHY_DATA_7_H	L2	FW_DATA<7>	88 89
PHY_CTL_0_H	N2	FW_CTL<0>	88 89
PHY_CTL_1_H	N3	FW_CTL<1>	88 89
PHY_LPS_H	P6	FW_LPS	88 89
PHY_LREQ_H	P1	FW_LREQ	88 89
PHY_LCLK_H	R1	FW_CLK98M_LCLK_R	88
PHY_LINKON_L	N7	FW_LINKON	89

89 88 FW_CLK98M_PCLK P2 PHY_SCLK_H
89 88 FW_PINT P3 PHY_PINT_L

R8800 22 5% 1/16W MF-LF 402
FW_CLK98M_LCLK 88 89

Shasta FireWire

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 88 OF 102	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	P38MM	CLOCKS		FW_CLK98M_PCLK_R
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_P<0>
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_N<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_P<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_N<0>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_P<1>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_N<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_P<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_N<1>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_P<2>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_N<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_P<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_N<2>
VESTA_CLK24M_XTALI	P38MM			VESTA_CLK24M_XTALI
	P38MM			VESTA_CLK24M_XTALO
	P38MM			VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

Line To Line:	0.38 mms
Length Tolerance:	100 mils
Primary Max Sep:	7.5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

L8900 FERR-EMI-600-OHM SM — PP1V2_VESTA_PLLVDD2 VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP1V2_ENETFW
C8900 10uF 20% 6.3V CERM 1206-1 (ESR < 0.5 ohms) — C8901 0.001uF 20% 50V CERM 402

L8901 FERR-EMI-600-OHM SM — PP2V5_VESTA_BIASVDD2 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP2V5_ENETFW
C8903 0.1uF 20% 10V CERM 402

L8902 FERR-EMI-600-OHM SM — PP2V5_VESTA_XTALVDD2 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
C8904 10UF 10% 6.3V X5R 805 — C8905 0.001uF 20% 50V CERM 402

L8906 FERR-EMI-600-OHM SM — PP3V3_VESTA_FAVDDH VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP3V3_ENETFW
C8906 0.1uF 20% 10V CERM 402 — C8907 0.1uF 20% 10V CERM 402 — C8908 0.1uF 20% 10V CERM 402 — C8917 10UF 10% 6.3V X5R 805

L8909 FERR-EMI-600-OHM SM — PP2V5_VESTA_FAVDDM VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP2V5_ENETFW
C8909 0.1uF 20% 10V CERM 402 — C8911 0.1uF 20% 10V CERM 402 — C8918 10UF 10% 6.3V X5R 805

L8913 FERR-EMI-600-OHM SM — PP1V2_VESTA_FAVDDL VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP1V2_ENETFW
C8913 0.1uF 20% 10V CERM 402 — C8914 0.1uF 20% 10V CERM 402 — C8915 0.1uF 20% 10V CERM 402 — C8919 10UF 10% 6.3V X5R 805

=PPFW_PHY — R8914 390K 5% 1/16W MF-LF 402

RP8900 22 5% 1/16W SM-LF
FW_DATA<0> — RP8900 pin 1
FW_DATA<1> — RP8900 pin 3
FW_DATA<2> — RP8900 pin 2
FW_DATA<3> — RP8901 pin 4
FW_DATA<4> — RP8901 pin 2
FW_DATA<5> — RP8901 pin 1
FW_DATA<6> — RP8901 pin 3
FW_DATA<7> — RP8900 pin 4

R8900 22 5% 1/16W MF-LF 402 — FW_CTL<0>
R8901 22 5% 1/16W MF-LF 402 — FW_CTL<1>

=PP3V3_FW — VESTA_DS_ONLY_EN0 — R8911 1K 5% 1/16W MF-LF 402
VESTA_PWR_CLASS_0 — R8912 1K 5% 1/16W MF-LF 402

Put crystal circuit close to PHY
CRITICAL Y8920 24.576M 8X4.5MM-SM — VESTA_CLK24M_XTALO
R8921 332 1% 1/16W MF-LF 402
C8920 22pF 5% 50V CERM 402 — C8921 22pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 12PF

R8903 1K 1% 1/16W MF-LF 402 — R8904 10K 1% 1/16W MF-LF 402

R8931 1K 5% 1/16W MF-LF 402 (VESTA_PORT1_DISABLE, VESTA_BILINGUAL_EN12)
R8933 1K 5% 1/16W MF-LF 402 (VESTA_PORT2_DISABLE)
R8935 1K 5% 1/16W MF-LF 402
VESTA_BILINGUAL_EN12_L
VESTA_PORT1_DISABLE_L
VESTA_PORT2_DISABLE_L

VESTA FW U8600 BCM5462 FBGA-200 3 OF 3 — OMIT

		R13	CPS
(Int PU)	VESTA_BILINGUAL_EN12_L	C11	ESDET0
(Int PU)	VESTA_PORT1_DISABLE_L	C12	ESDET1
(Int PU)	VESTA_PORT2_DISABLE_L	C13	ESDET2
	FW_CLK98M_LCLK	D15	PLI_LCLK
	FW_DATA_R<0>	E12	PLI_DATA[0]
	FW_DATA_R<1>	E11	PLI_DATA[1]
	FW_DATA_R<2>	F11	PLI_DATA[2]
	FW_DATA_R<3>	F12	PLI_DATA[3]
	FW_DATA_R<4>	F13	PLI_DATA[4]
	FW_DATA_R<5>	G13	PLI_DATA[5]
	FW_DATA_R<6>	G12	PLI_DATA[6]
	FW_DATA_R<7>	G11	PLI_DATA[7]
	FW_CTL_R<0>	E14	PLI_CTL[0]
	FW_CTL_R<1>	E13	PLI_CTL[1]
	FW_LPS	D11	PLI_LPS
	FW_LREQ	D12	PLI_LREQ
	FW_LOWPWR	J3	LPWR_1394
	VESTA_DS_ONLY_EN0	A13	DS_ONLY_EN0 Internal Pull-Down
	VESTA_PWR_CLASS	A12	PWR_CLASS Internal Pull-Up
	TP_VESTA_TEST_1394<0>	J5	TEST_1394[0]
	TP_VESTA_TEST_1394<1>	J4	TEST_1394[1]
	TP_VESTA_TVCO_24	N13	TVCO_24
	VESTA_CLK24M_XTALI	P14	XTALI_24
	VESTA_CLK24M_XTALO_R	P13	XTALO_24

XTALVDD2 N15 — BIASVDD2 R14 — PLLVDD2 P15 — BIASGND P12 — PLLGND2 N14
FAVDDH K11 K12 K13 — FAVDDM L11 L12 M11 M12 — FAVDDL L10 M10 N11 N12

TDBL[0]	A14	TP_VESTA_TDBL<0>
TDBL[1]	B13	TP_VESTA_TDBL<1>
TDBL[2]	B14	TP_VESTA_TDBL<2>
PLI_PCLK	E15	FW_CLK98M_PCLK_R
PLI_INT	D13	FW_PINT
PLI_LINK	D14	FW_LINKON
TPBIAS[0]	L13	FW_TPBIAS<0> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[0]	L15	FW_TPA_P<0>
TPAN[0]	L14	FW_TPA_N<0>
TPBP[0]	M15	FW_TPB_P<0>
TPBN[0]	M14	FW_TPB_N<0>
TPBIAS[1]	J13	FW_TPBIAS<1> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[1]	J15	FW_TPA_P<1>
TPAN[1]	J14	FW_TPA_N<1>
TPBP[1]	K15	FW_TPB_P<1>
TPBN[1]	K14	FW_TPB_N<1>
TPBIAS[2]	H13	FW_TPBIAS<2> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[2]	G15	FW_TPA_P<2>
TPAN[2]	G14	FW_TPA_N<2>
TPBP[2]	H15	FW_TPB_P<2>
TPBN[2]	H14	FW_TPB_N<2>
SDC	H1	I2C_VESTA_SCL
SDA	H2	I2C_VESTA_SDA
RDAC2	R15	VESTA_RDAC2_PD

R8902 22 5% 1/16W MF-LF 402 — FW_CLK98M_PCLK
R8909 2.0K 1% 1/16W MF-LF 402
=PP3V3_FW — R8915 10K 5% 1/16W MF-LF 402 — R8916 10K 5% 1/16W MF-LF 402
(I2C_VESTA_SDA) (I2C_VESTA_SCL)

Vesta FireWire PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 89 OF 102	

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
R401 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	90
R400 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	90
R402 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	90
R404 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	90
R403 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	90
R405 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	90
R407 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	90
R406 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	90

8 WATTS MAX

24 VOLTS

PP24V_RUN

R9056 1.3 20% 1W FF 2512

PP24V_FW MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V MAKE_BASE=TRUE

=PPFW_PHY 89

CRITICAL

D9000 MURS320XXG SMC

C9009 0.1UF 20% 50V CERM 805

R9002 1.3 20% 1W FF 2512

PP24V_FW_D MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

PP24V_FW_R MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

L9001 FERR-160-OHM 1206

FW_VP VOLTAGE=24V MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM

F9002 0.5AMP SM

PPFW_PORT0_VP VOLTAGE=33V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

F9000 1.5AMP-33V SM

PPFW_PORT1_VP 90 VOLTAGE=33V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

Termination

Place close to FireWire PHY

89 FW_TPBIAS<1>

89 FW_TPBIAS<0>

C9050 1uF 10% 6.3V CERM 402

C9060 1uF 10% 6.3V CERM 402

R9050 56.2 1% 1/16W MF-LF 402

R9051 56.2 1% 1/16W MF-LF 402

R9060 56.2 1% 1/16W MF-LF 402

R9061 56.2 1% 1/16W MF-LF 402

89 FW_TPA_P<0> — 90 FW_PORT0_TPA_P MAKE_BASE=TRUE

89 FW_TPA_N<0> — 90 FW_PORT0_TPA_N MAKE_BASE=TRUE

89 FW_TPB_P<0> — 90 FW_PORT0_TPB_P MAKE_BASE=TRUE

89 FW_TPB_N<0> — 90 FW_PORT0_TPB_N MAKE_BASE=TRUE

89 FW_TPA_P<1> — 90 FW_PORT1_TPA_P MAKE_BASE=TRUE

89 FW_TPA_N<1> — 90 FW_PORT1_TPA_N MAKE_BASE=TRUE

89 FW_TPB_P<1> — 90 FW_PORT1_TPB_P MAKE_BASE=TRUE

89 FW_TPB_N<1> — 90 FW_PORT1_TPB_N MAKE_BASE=TRUE

R9052 56.2 1% 1/16W MF-LF 402

R9053 56.2 1% 1/16W MF-LF 402

R9062 56.2 1% 1/16W MF-LF 402

R9063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0>

FW_TPA_C<1>

C9054 270pF 5% 25V CERM 402

R9054 4.99K 1% 1/16W MF-LF 402

C9064 270pF 5% 25V CERM 402

R9064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

89 FW_TPBIAS<2> — NC_FW_TPBIAS2 MAKE_BASE=TRUE NO_TEST=YES

89 FW_TPA_P<2> — NC_FW_TPA_P2 MAKE_BASE=TRUE NO_TEST=YES

89 FW_TPA_N<2> — NC_FW_TPA_N2 MAKE_BASE=TRUE NO_TEST=YES

89 FW_TPB_P<2> — FW_TPB2_PD MAKE_BASE=TRUE NO_TEST=YES

89 FW_TPB_N<2>

R9070 1K 5% 1/16W MF-LF 402

ESD Rail

89 7 =PP3V3_FW — R9090 665 1% 1/16W MF-LF 402 — PP3V3_FW_ESD_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm — L9090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 90 VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

D9090 SOT23 BZX84C2V7-X-F

"Snapback" & "Late VG" Protection

90 PP3V3_FW_ESD

DP9010 BAV99DW-X-F SOT-363

C9010 0.001uF 20% 50V CERM 402

C9011 0.001uF 20% 50V CERM 402

90 FW_PORT0_TPA_P

90 FW_PORT0_TPA_N

90 FW_PORT0_TPB_P

90 FW_PORT0_TPB_N

DP9011 BAV99DW-X-F SOT-363

C9012 0.001uF 20% 50V CERM 402

C9013 0.001uF 20% 50V CERM 402

FL9010 165-OHM SM SYM_VER-1

FL9011 165-OHM SM SYM_VER-1

R9010 0 5% 1/8W MF-LF 805

PORT 0 1394A

CRITICAL J9000 FWS22 F-ST-TH

90 FW_PORT0_TPA_P_FL — TPO (TPA+)

90 FW_PORT0_TPA_N_FL — TPO# (TPA-)

90 FW_PORT0_TPB_P_FL — TPI (TPB+)

90 FW_PORT0_TPB_N_FL — TPI# (TPB-)

(PPFW_PORT0_VP) — VP

VGND

GND_FW_PORT0_VG VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

C9015 0.01uF 20% 16V CERM 402

C9016 0.01uF 20% 16V CERM 402

514-0202

GND_CHASSIS_FIREWIRE 7 90

"Snapback" & "Late VG" Protection

90 PP3V3_FW_ESD

DP9020 BAV99DW-X-F SOT-363

C9020 0.001uF 20% 50V CERM 402

C9021 0.001uF 20% 50V CERM 402

90 FW_PORT1_TPA_P

90 FW_PORT1_TPA_N

90 FW_PORT1_TPB_P

90 FW_PORT1_TPB_N

DP9021 BAV99DW-X-F SOT-363

C9022 0.001uF 20% 50V CERM 402

C9023 0.001uF 20% 50V CERM 402

FL9020 165-OHM SM SYM_VER-1

FL9021 165-OHM SM SYM_VER-1

R9020 0 5% 1/8W MF-LF 805

PPFW_PORT1_VP 90

PORT 1 1394A

CRITICAL J9001 FWS22 F-ST-TH

90 FW_PORT1_TPA_P_FL — TPO (TPA+)

90 FW_PORT1_TPA_N_FL — TPO# (TPA-)

90 FW_PORT1_TPB_P_FL — TPI (TPB+)

90 FW_PORT1_TPB_N_FL — TPI# (TPB-)

(PPFW_PORT1_VP) — VP

VGND

GND_FW_PORT1_VG VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

C9025 0.01uF 20% 16V CERM 402

C9026 0.01uF 20% 16V CERM 402

514-0202

GND_CHASSIS_FIREWIRE 7 90

FIREWIRE CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	90	102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 91 92
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 91 92
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 76 91
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 76 91
USB2_NEC_XTAL		P25MM		NEC_CLK30M_XT1 91
		P25MM		NEC_CLK30M_XT2 91
		P25MM		NEC_CLK30M_XT2_R 91

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

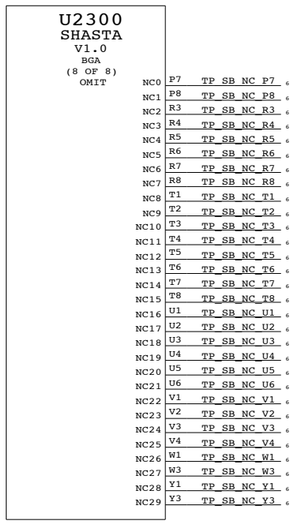
Signal aliases required by this page:
(NONE)

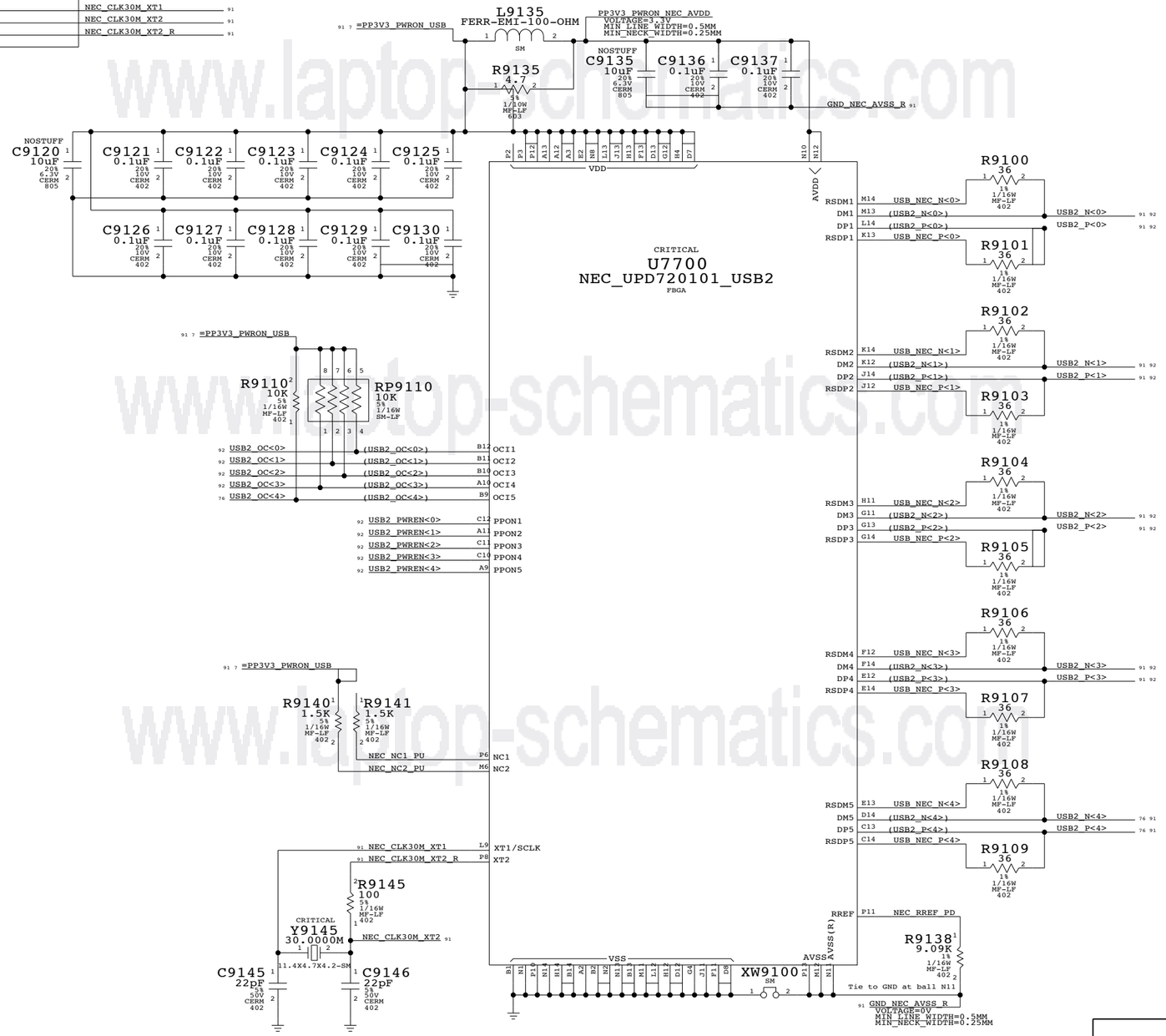
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





USB Host Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 91 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F 6 92
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F 6 92
USB CONTROLLER	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 6 92
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 6 92
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 6 92
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 6 92

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

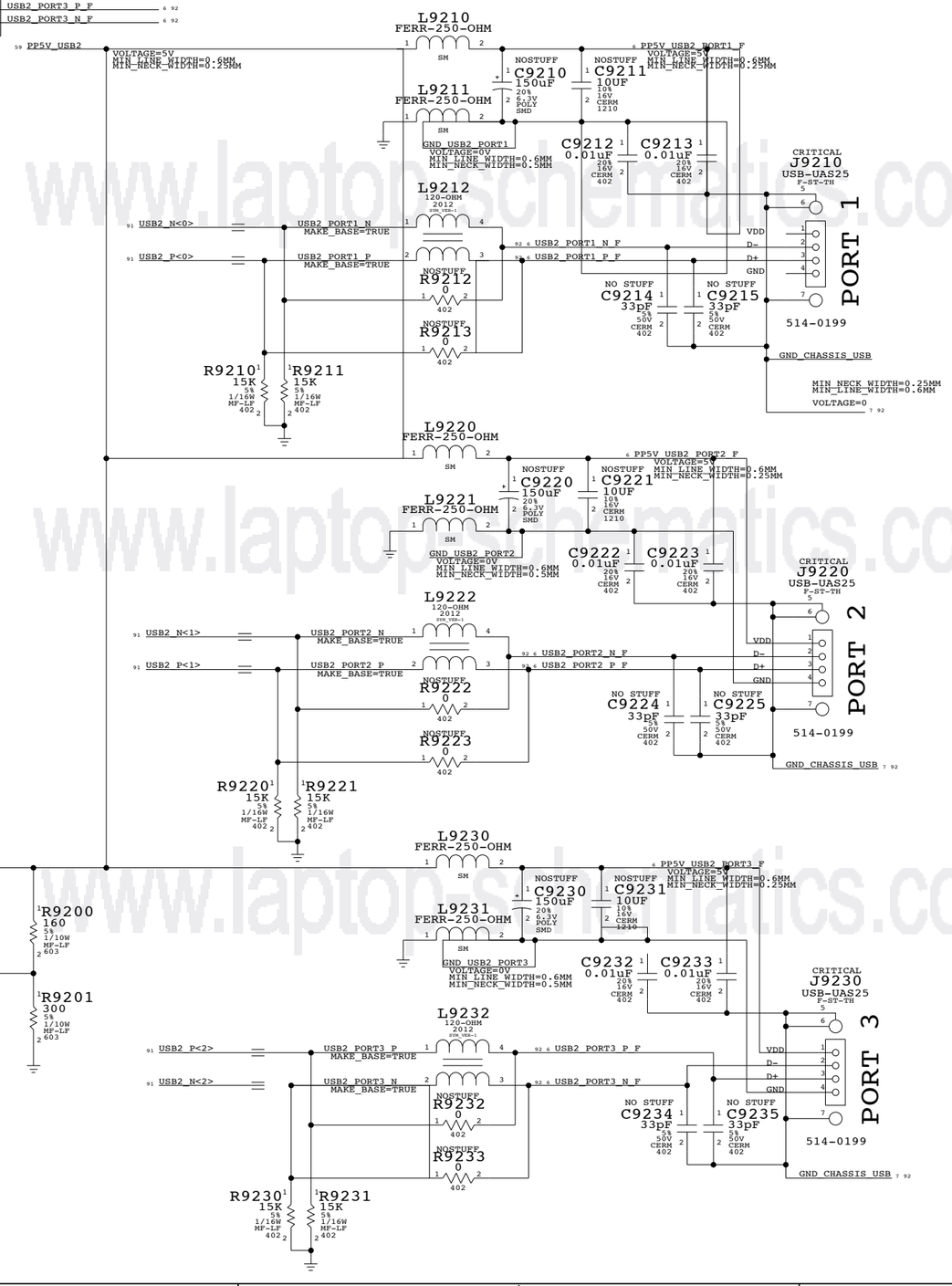
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

91 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
91 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
91 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
91 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
91 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

External USB Ports



UNUSED PORT

91 USB2_N<3>
91 USB2_P<3>
R9250 15K 5% 1/16W MF-LF 402
R9251 15K 5% 1/16W MF-LF 402

USB Device Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 92 OF 102	

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

25 UDASH_SDOWN ── TP_UDASH_SDOWN
                ── MAKE_BASE=TRUE

Q52 Modem Connector

SDF9400
STDOFF-4MM-9MMH-TH

CRITICAL
J9401
C104A-H9.0
F-ST-SM

94 7 _PP3V3_PWRON_MODEM

C9450 10UF 20% 6.3V CERM 805

C9451 0.1UF 20% 10V CERM 402

PP3V3_PWRON_MODEM 7 94

R9451 10K 5% 1/16W MF-LF 402

MODEM_RING2SYS_L 6 25

MODEM_FC_RGDT

I2S1_SYNC 6 25

25 6 I2S1_SB_TO_DEV_DTO

I2S1_DEV_TO_SB_DTI 6 25

25 6 I2S1_RESET_L

25 6 I2S1_MCLK

I2S1_BITCLK 6 25

516S0116

SDF9401
STDOFF-4MM-9MMH-TH

GND_CHASSIS_MODEM

From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

RJ11 CONNECTOR

STUFFED AT FATP
SYMBOL USED FOR PLACEMENT

OMIT

J9402
RJ11-HGT27.5
ST-TH

514-0205

Modem Interface

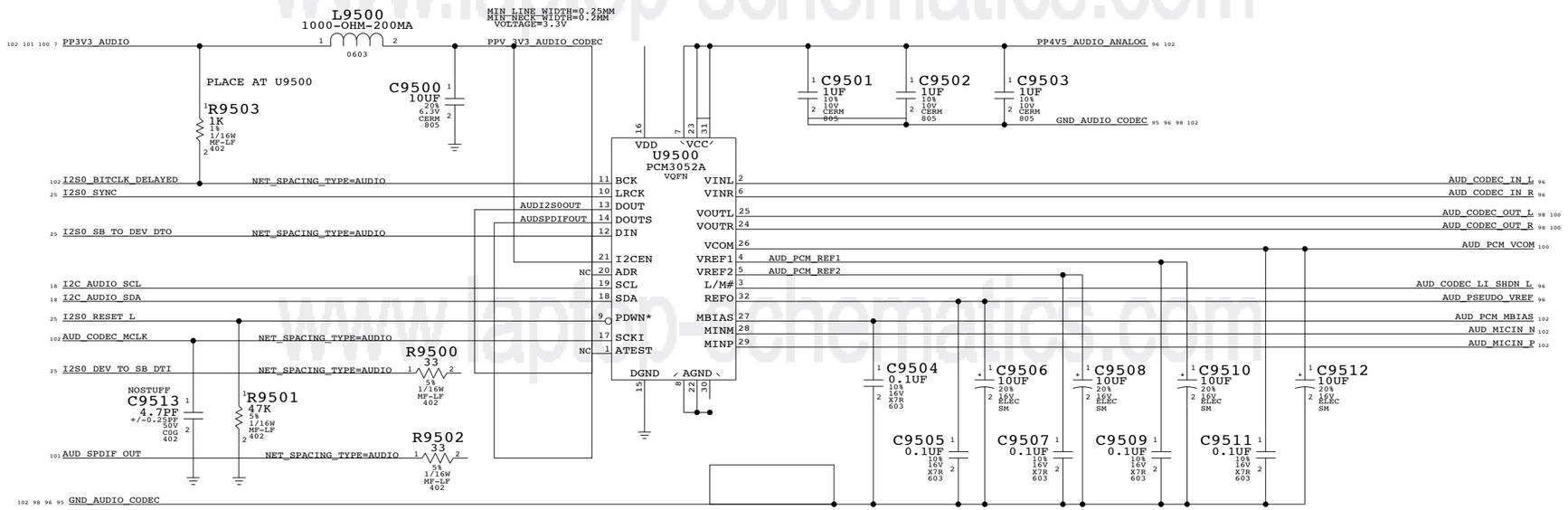
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E

SCALE	SHT	OF
NONE	94	102

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

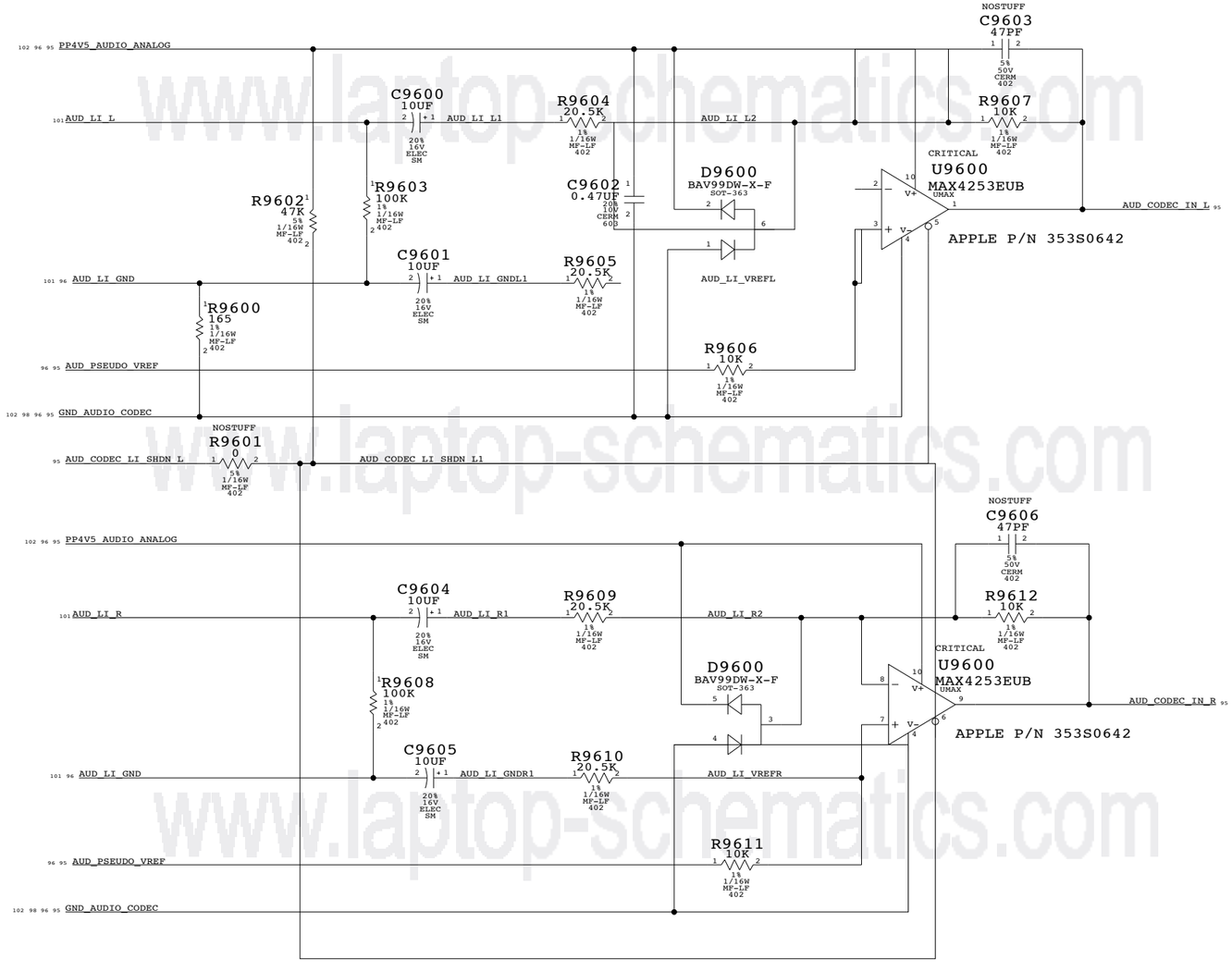
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 95 OF 102	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

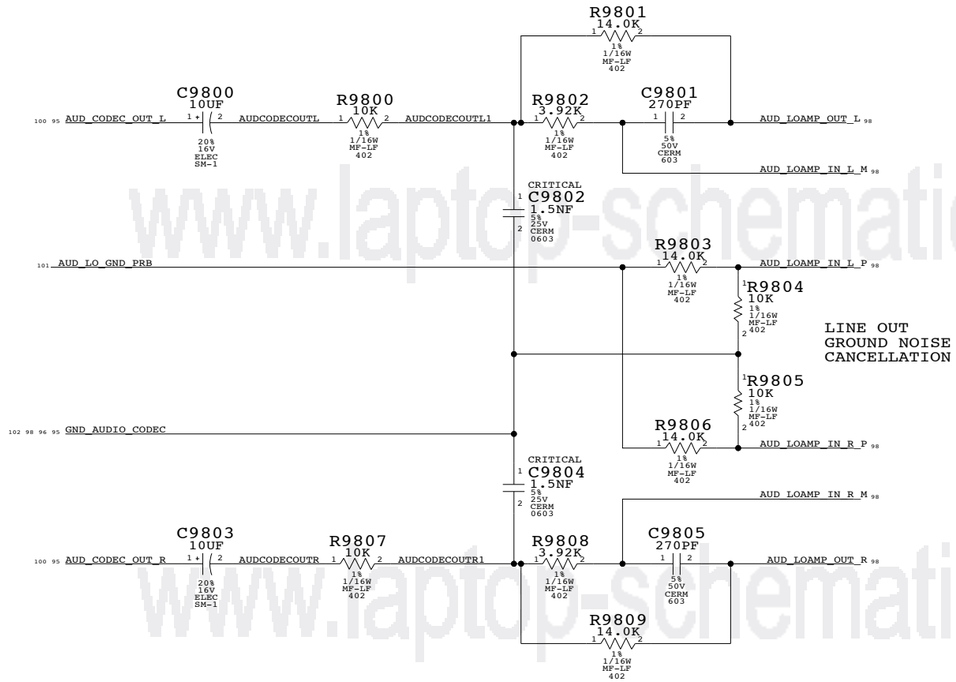
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 96 OF 102	

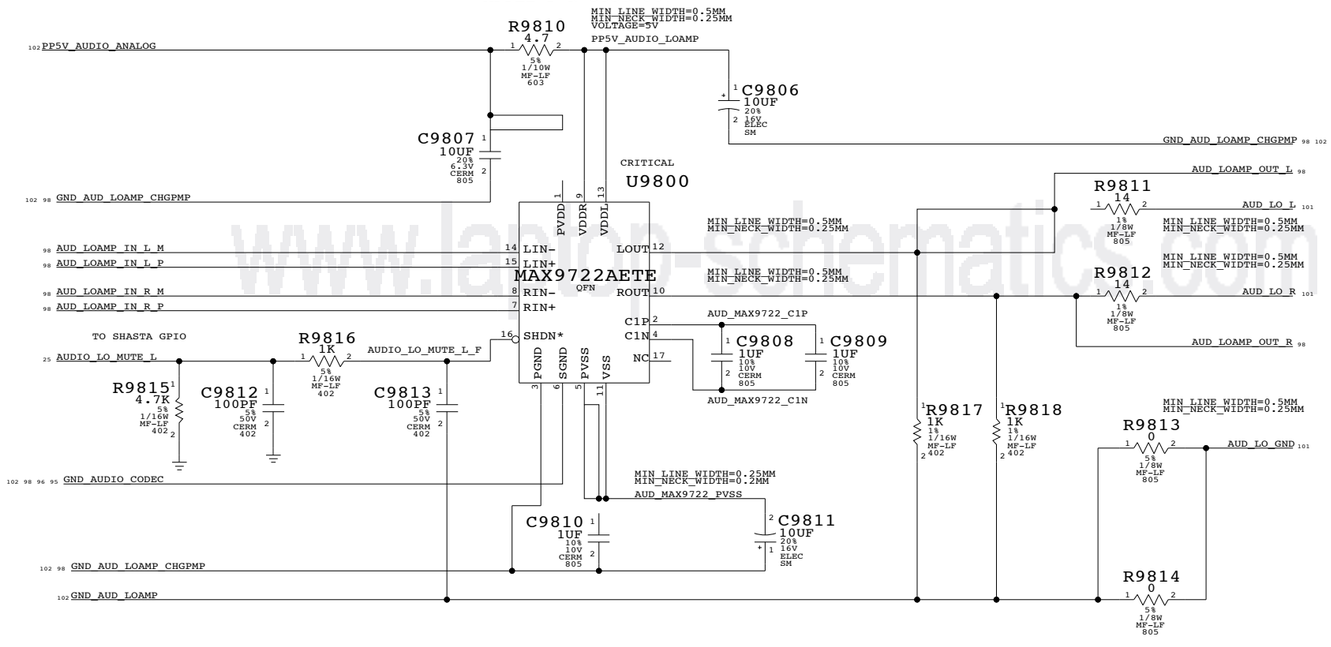
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

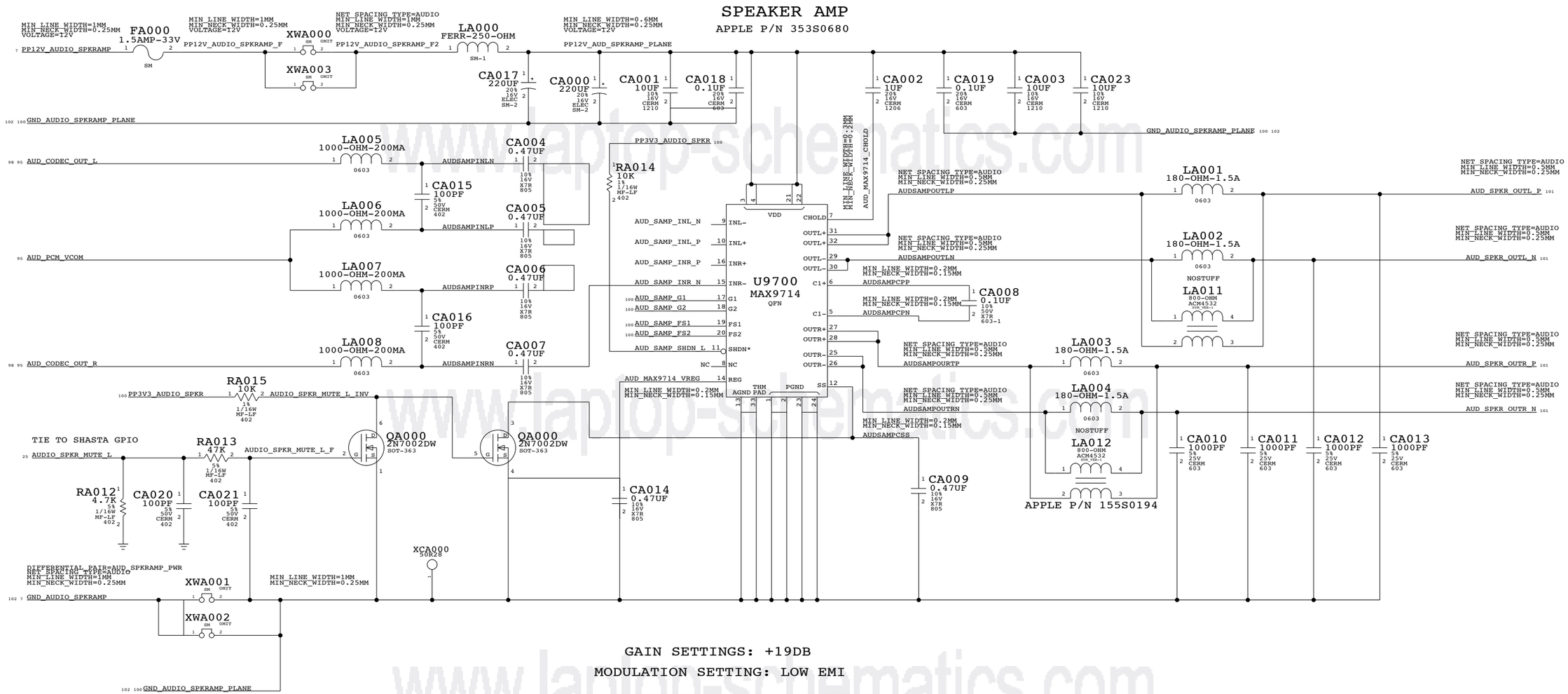
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 98 OF 102	

SPEAKER AMP

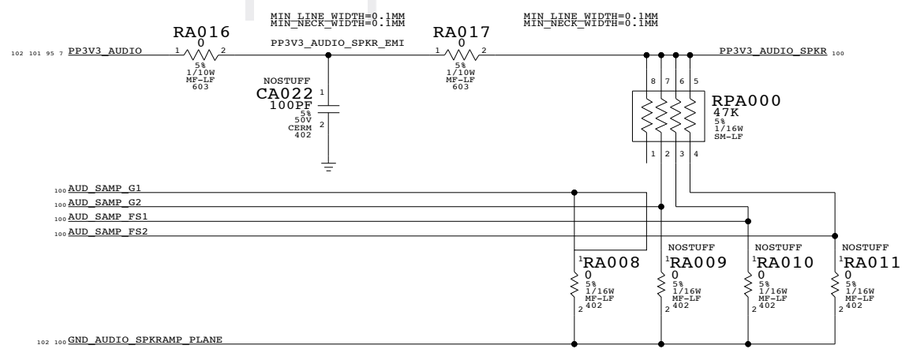
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

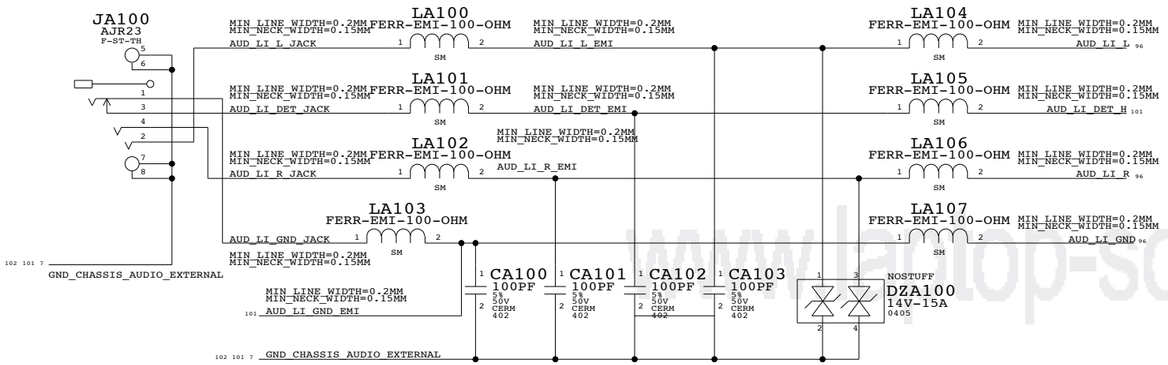
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 100 OF 102	

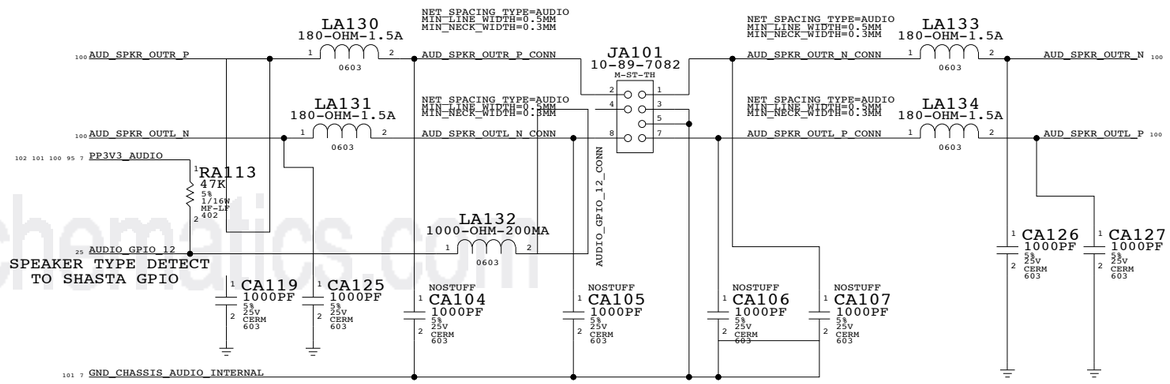
LINE IN JACK

APPLE P/N 514-0203



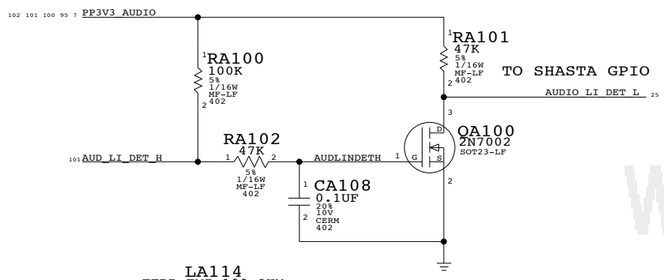
SPEAKER CABLE CONNECTOR

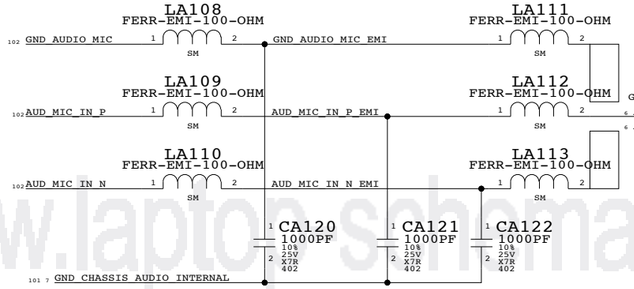
APPLE P/N 518-0138



LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED





JA102
HF28
M-ST-TH
GND_AUDIO_MIC_CONN
AUD_MIC_IN_P_CONN
AUD_MIC_IN_N_CONN

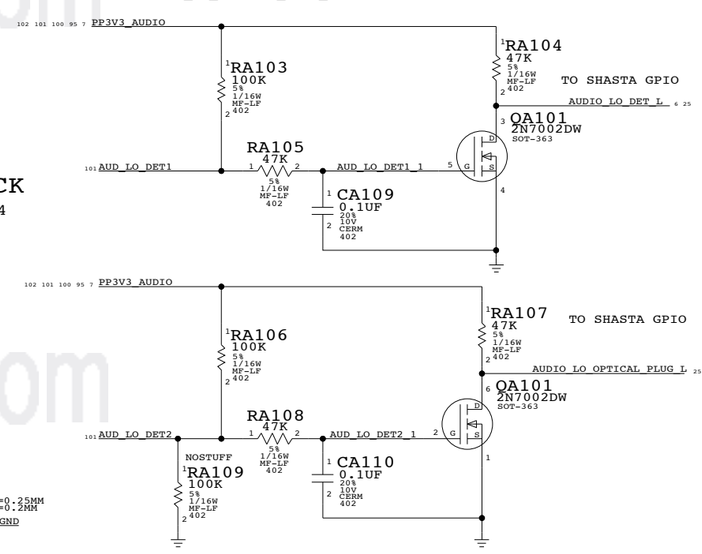
APPLE P/N 518-0034

MIC CABLE CONNECTOR

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0204

AUDIO: Q45 CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

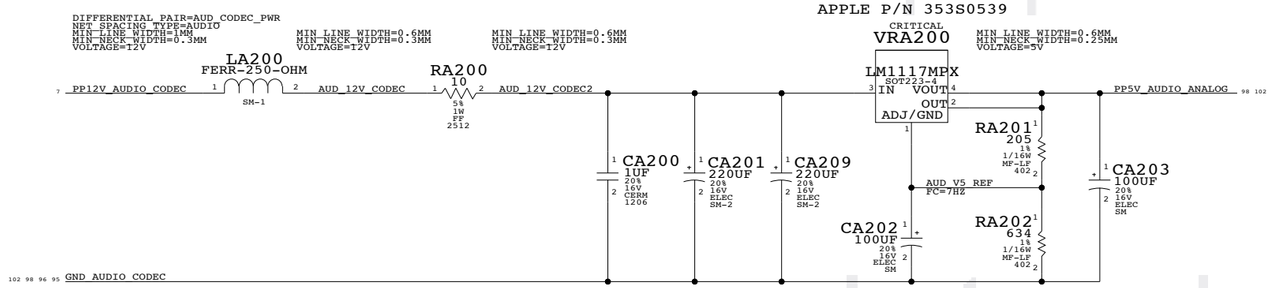
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 101 OF 102	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

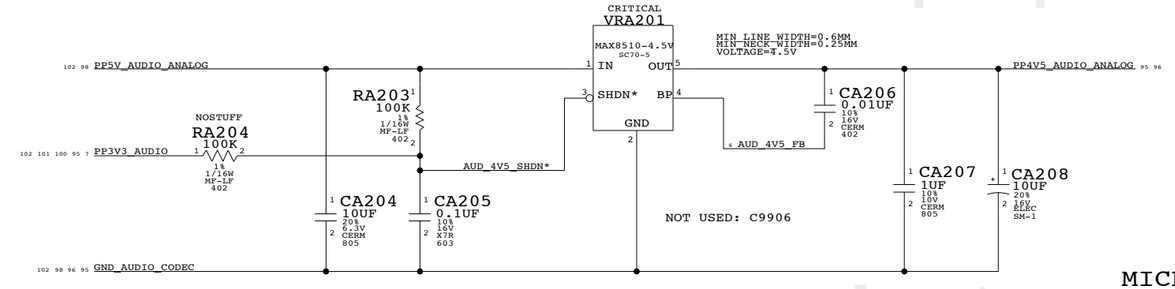
5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP

APPLE P/N 353S0539

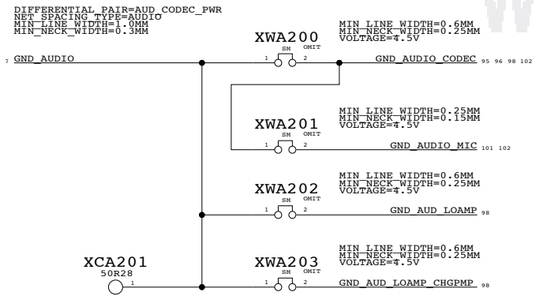


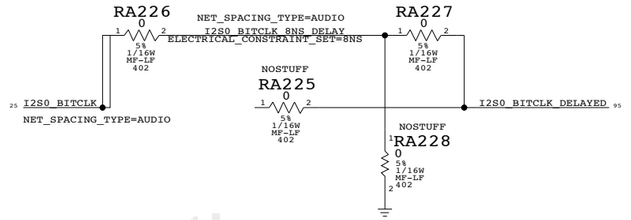
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733

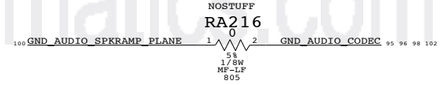


AUDIO GROUND RETURNS

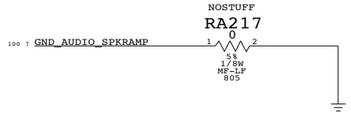




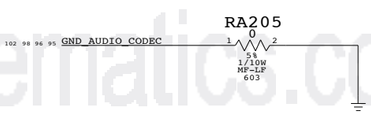
PLACE ACROSS GROUND SPLIT
AT RIGHT SIDE OF CA007



PLACE NEAR ENTRY TO SPEAKER
AMP GROUND PLANE

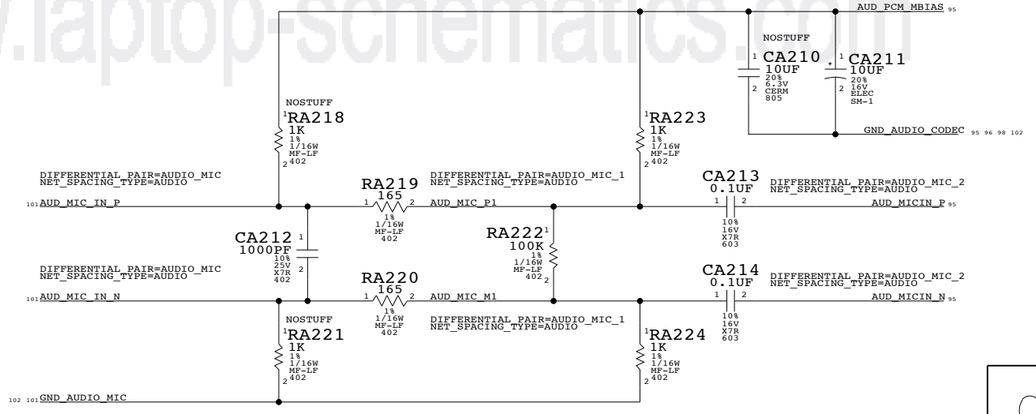


PLACE ACROSS GROUND SPLIT
AT CODEC U9500

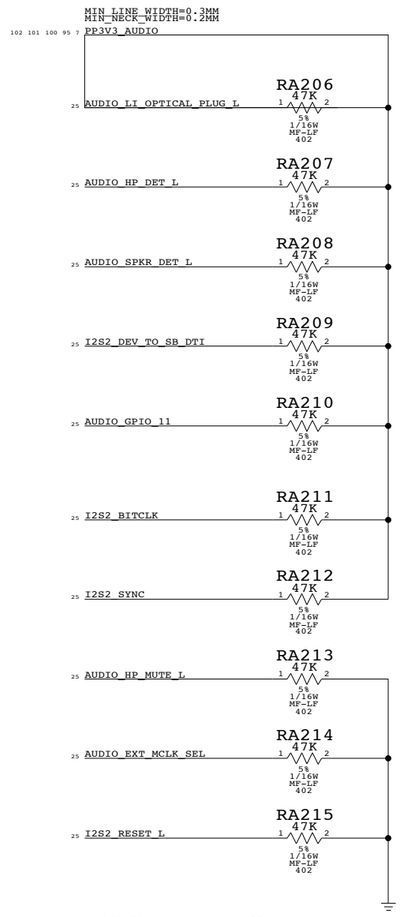


PLACE AT J5903

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



MAKE_BASE=TRUE — I88
TP_I2S2_SB_TO_DEV_DTO — I2S2_SB_TO_DEV_DTO

MAKE_BASE=TRUE — I89
TP_I2S2_MCLK — I2S2_MCLK

MAKE_BASE=TRUE — I116
I2S0_MCLK — AUD_CODEC_MCLK

AUDIO: Q45 POWER SUPPLIES

SYNC_MASTER=AUDIO — SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	E
SCALE: NONE	SHT 102 OF 102	