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<td>IC,KODIAK,V1.2,PBGA,200MM</td>
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**Notes:**
- **PROPRIETARY:**
- **NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**
- **NOT TO REPRODUCE OR COPY IT**
- **CRITICAL**
- **Omit**
PWRON_L

PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

1.2V Vreg

NOTE:
SET OUTPUT=1.22-1.23V
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC
POWER BUDGET CURRENT OF TOTAL RAILS: 3.2A PEAK
2.4A CONTINUOUS

VOLTAGE=0 VMIN_LINE_WIDTH=0.45MMMIN_NECK_WIDTH=0.25MM

PP1V2_PWON FET SWITCH
PEAK CURRENT 1.3A
CONTINUOUS 1.3A

PP1V2_RUN FET SWITCH
PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.2A/M23 IF NOT
NOTE:
- SET OUTPUT=2.5V
- I(VGS=2.5V)=0.5A
- VDD=VREF*(R1581+R1582)=1.45V
- POWER BUDGET CURRENT OF TOTAL RAILS
  - 0.2A PEAK
  - 0.1A CONTINUOUS

- PEAK CURRENT 0.1A
- RDSON=0.04 OHM
- @ VGS=2.5V

- PP2V5_ALL VOLTAGE REGULATOR
- PP2V5_PWRON FET SWITCH
- PEAK CURRENT 0.1A
- PP2V5_RUN FET SWITCH
- PEAK CURRENT 0.1A

- NOSTUFF OPTION TO DELAY 2.5V PWRON TO COME UP WITH 3.3V PWRON
Must power Shasta VCore rail before any Power Sequencing:

BOM options provided by this page:

- NONE

Signal aliases required by this page:

- PCI, otherwise 3.3V.
- VIO1 TO SAME IF 64-BIT

- =PP1V2_PWRON_SB_VCORE
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)

Power aliases required by this page:

Page Notes

NOTE: PCI pads use the VIO supply to meet different drive timing specifications required by the PCI characteristics.

- =PP1V2_PWRON_SB_VCORE
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:
ALL OTHER CLOCK CONSTRAINTS ON THEIR
RESPECTIVE BUS PAGES
ALL JTAG-RELATED PINS
SMU DRIVES 3.3V PUSH-PULL ON

JTAG_NB_TDO
SAME AS Q63
SYS_NORTH_RESET FROM SMU TO NB_PU_RST

3.3V TOLERANT

SHARE CPU AND NB JTAG TMS WITH SMU

=PP3V3_PWRON_SMU

SHARE CPU AND NB JTAG TDI WITH SMU (PRIMARY PLAN)

=PP2V5_PWRON_NB_MISC

NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED
TO AVOID STUBS

LEVEL SHIFTER SMU JTAG TCK TO CPU (BACKUP PLAN)

SMU_JTAG_TCK TO CPU (BACKUP PLAN)

SMU JTAG TDI TO CPU (BACKUP PLAN)

NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)

SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)

SHARE CPU AND NB JTAG TDI WITH SMU

SHAPE CPU AND NB JTAG TCK TO CPU (BACKUP PLAN)

JTAG_NB_TCK_R
JTAG_NB_TDI_R

SMU_SUSPENDREQ_L

LIMITED USE

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APPLE COMPUTER INC.
Q63 USE OF P7.2 IS PWM FAN
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.
M23/M33 DOESN'T USE P1.4. NC ON PG 7.
M23/M33 DOESN'T HAVE THIS FAN (P7.4)
M23/M33 DOESN'T HAVE THIS FAN.
M23/M33 DOESN'T HAVE THOSE FANS.
Q63 USE OF P9.1 IS TACH 8.

SMU ALIASES

SMU SUPPLEMENTAL (4)

SMU SUPPLEMENTAL (4)
NOTICE OF PROPRIETARY PROPERTY

I agree to the following:

I will not maintain the document in confidence.
I will not reveal or publish in whole or part.
I will not reproduce or copy it.

The information contained herein is the proprietary property of Apple Computer, Inc. the possessor.

Fan 0, 1 & System Temp

Fan 0:
- SMU_FAN_TACH0
- FAN_0_PWR
- FAN_0_OUT
- MIN_LINE_WIDTH=0.5MM
- MIN_NECK_WIDTH=0.25MM
- F0_DRV
- F0_VOLTAGE
- F0_GATESLOWDN
- F0_RCFEEDBK
- F0_RCFEEDBK
- F0_DRV

Fan 1:
- SMU_FAN_TACH1
- FAN_1_PWR
- FAN_1_OUT
- MIN_LINE_WIDTH=0.5MM
- MIN_NECK_WIDTH=0.25MM
- F1_DRV
- F1_VOLTAGE
- F1_GATESLOWDN
- F1_RCFEEDBK
- F1_RCFEEDBK
- F1_DRV

Sync Date: 08/26/2005
Sync Master: FINO-M23
Q63: SEE P.28 FOR MORE DECOUPLING CAPS FOR THESE PINS.
GROUND VIAS FOR SIGNAL LAYER TRANSITIONS

MIN_LINE_WIDTH = 0.5MM

VOLTAGE = 0.9V

SYNC_DATE = 10/07/2005

NOTICE OF PROPRIETARY PROPERTY
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<td>HT_MB_TO_NB_CAD_N&lt;0&gt;</td>
</tr>
<tr>
<td>HT_MB_TO_NB_CLK_P&lt;0&gt;</td>
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<td>HT_MB_TO_NB_CLK_P&lt;0&gt;</td>
<td>HT_MB_TO_NB_CLK_N&lt;0&gt;</td>
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<tr>
<td>HT_NB_TO_SB_CAD_P&lt;0&gt;</td>
<td>HT_NB_TO_SB_CAD_N&lt;0&gt;</td>
<td>HT_NB_TO_NB_CAD_P&lt;0&gt;</td>
<td>HT_NB_TO_NB_CAD_N&lt;0&gt;</td>
</tr>
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<td>HT_MB_TO_NB_CAD_N&lt;3&gt;</td>
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<tr>
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<td>HT_NB_TO_NB_CAD_P&lt;1&gt;</td>
<td>HT_NB_TO_NB_CAD_N&lt;1&gt;</td>
</tr>
<tr>
<td>HT_MB_TO_NB_CAD_P&lt;0&gt;</td>
<td>HT_MB_TO_NB_CAD_N&lt;0&gt;</td>
<td>HT_MB_TO_NB_CAD_P&lt;0&gt;</td>
<td>HT_MB_TO_NB_CAD_N&lt;0&gt;</td>
</tr>
<tr>
<td>HT_MB_TO_NB_CLK_P&lt;0&gt;</td>
<td>HT_MB_TO_NB_CLK_N&lt;0&gt;</td>
<td>HT_MB_TO_NB_CLK_P&lt;0&gt;</td>
<td>HT_MB_TO_NB_CLK_N&lt;0&gt;</td>
</tr>
</tbody>
</table>
ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

PLACE CLOSE TO SHASTA

AD<27> IS IDSEL FOR USB
AD<17> IS IDSEL FOR AIRPORT
NOTE: This AirPort implementation does not support PME.

PCI Devices implemented on this page:

- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

Signal aliases required by this page:

- _PP3V3_PCI

Power aliases required by this page:

- ELECTRICAL_CONSTRAINT_SET
- DIFFERENTIAL_PAIRNET_SPACING_TYPE
- PCI_CLK33M_AIRPORT,CLOCKSPCI_CLK_AIRPORT

COMPONENTS

- RC150
- MF-LF
- 402
- 1/16W
- 5%
- 6.3V
- 10%
- 1UF
- CERM
- X5R
- 6.3V
- 10%
- 1UF
- CERM2
- 6.3V
- 10%

- CC150
- 516S0347
- CRITICAL
AD27 (Slot "G") - USB2 (0x1033/0x0035)

PCI Devices implemented on this page:
- PCI_CLK33M_USB2 (33MHz PCI clock)

Power aliases required by this page:
- CLOCKS = PCI_CLK33M_USB2

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN
**Page Notes**

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q3.
SATA PINs WERE REMAPPED FOR BETTER ROUTING AROUND SATA CONNECTOR.
PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

VESTA -> SHASTA

ENET SERIES TERM
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO GROUND RETURNS

UNUSED GPIO TERMINATIONS

AUDIO: POWER SUPPLIES

APPLE COMPUTER INC.