Table 1: Capacitance Values

- All capacitance values are in microfarads.

Table 2: Resistance Values

- All resistance values are in ohms, 0.1 watt +/- 5%.

Legend:
- CPU AVDD VREG
- CPU aliasses & Misc
- Kodiak Memory Dq/Ctl
- Parallel Term
- Main Memory Clock Buffers
- Memory Addr Branching
- Memory Dimm A
- MBl Mem Series Term
- On-Board DDR SDRAM
- On-Board DDR SDRAM
- Kodiak PCI-E X16
- GPU PCIe
- Graphics Vregs
- CPU Core Power
- GPU Frame Buffer
- FB Series Termination
- GPU GDDR SDRAM A
- GPU GDDR SDRAM B
- GPU Straps
- GPU DVI & DACs
- TMDs/Inverter/ExtVGA
- Kodiak PCI-E CONST
- HT ALIASES
- HyperTransport
- Shasta PCI Interface
- PCI Series Termination
- AIRPORT & BLUETOOTH
- USB 2.0 PCI Interface
- BootROM
- Shasta Disk
- Disk Connectors
- Ethernet Series Term
- Shasta Ethernet

Apple Computer Inc.

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
SCH, MLB, IMG5, 17

SA A 
11/01/05

PDF CSA CONTENTS

System Block Diagram
Power Block Diagram
Table Items
FUNC TEST 1 OF 2
Power Conn/Alias
Signal Alias
FUNC TEST 2 OF 2
1.8V Vreg
1.5V Vreg
1.2V Vreg
2.5V Vreg
5V & 3.3V Fets
Vesta Core/Misc
KODIAK CORE & BYPASS
KODIAK & SHASTA MISC
Shasta Core Power
Shasta Serial/Misc
PULSAR2 POWER
PULSAR2 CLOCKS
Pulsar Aliasses
System Management Unit
SMU SUPPLEMENTAL (2)
SMU SUPPLEMENTAL (3)
SMU SUPPLEMENTAL (4)
Fan 1 & 4 System Temp
Fan 0 & HD Temp
IZC Connections
KODIAK E1 PWR & CAPS
KODIAK E1 A
CPU E1 AND IO
KODIAK E1 B
CPU STRAPS
CPU POWER AND BYPASS
PROC DECOUPLING
CPU VCORE VREG
CPU VCORE MORE BYPASS
### Processors

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ASICS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>ALTERNATE FOR</th>
<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Misc Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>ALTERNATE FOR</th>
<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Alternates

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>ALTERNATE FOR</th>
<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NOTES FROM TOM FUSSELMAN
PLACE TWO TEST POINTS ON TOP SIDE
FOR PPV3, ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACKS

FUNC TEST NETS

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROPRIETARY
AND MAY NOT BE REPRODUCED OR DISCLOSED TO ANY OTHER PERSON OR ENTITY
IN ANY FORM OR MANNER WITHOUT THE PRIOR WRITTEN CONSENT OF APPLE COMPUTER INC.
1.8V VOLTAGE REGULATOR

NOTE:

1. POWER BUDGET CURRENT OF TOTAL RAILS
   VOUT=VREF*(R903+R905)/R905=1.85VDC
   IRU3037ACS VREF=0.8VDC
   SET OUTPUT=1.85V FOR FRAMEBUFFER.
   NOTE:

2. POWER BUDGET CURRENT OF FET
   IRF7413PBF
   4.5A CONTINUOUS
   7.4A PEAK

3. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
   THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
   NOTICE OF PROPRIETARY PROPERTY
   III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
   NOT TO REPRODUCE OR COPY IT

4. SYNCH Master=M23-PC
PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

NOTE:

- SET OUTPUT=1.22-1.23V
- VDD=VREF*(R1005+R1003)/R1005=1.22-1.23VDC
- POWER BUDGET CURRENT OF TOTAL RAILS 3.1A PEAK
- 2.4A CONTINUOUS

PP1V2_ALL VOLTAGE REGULATOR

PP1V2_PWRON FET SWITCH
PEAK CURRENT 1.3A
1.0A CONTINUOUS

PP1V2_RUN FET SWITCH
PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT

NOTE:

1.2V Vreg

NOTICE OF PROPRIETARY PROPERTY
The information contained here is the proprietary information of Apple Computer, Inc. The possession of this document and the information contained herein may not be disclosed to any other person or entity.

DEVELOPMENT

CRITICAL
NOTE:
PEAK CURRENT 0.1A

0.2A PEAK

POWER BUDGET CURRENT OF TOTAL RAILS
0.1A CONTINUOUS

1.02K

1K

32

7 6 5

1 4

3 2 1

402

0.01UF

1/16W

5%

C1580

C1581

C1582

R1508

R1509

R1510

R1511

R1512

R1513

C1583

R1508

R1509

R1510

R1511

R1512

R1513

C1580

C1581

C1582

R1508

R1509

R1510

R1511

R1512

R1513

C1583

MIC39102

SOP-8-LF

PP2V5_PWRON FET SWITCH

PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

PEAK CURRENT 0.1A
NOTICE OF PROPRIETARY PROPERTY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III NOT TO REPRODUCE OR COPY IT

AGREES TO THE FOLLOWING

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

12345678

REV.
APPLE COMPUTER INC.
The regulator will be in continuous mode. If both options are off the regulator will be in continuous mode.

BOM options provided by this page:

- M23: PP3V3_ENETFW
- 132
- 7
- PULLUPS MAY BE NO
- STUFFED IN EVT.

- MF-LF402
- 132
- 354
- 9
- 9
- 0
- 138
- TP_JTAG_VESTA_TRST_L
- TP_JTAG_VESTA_TMS
- TP_JTAG_VESTA_TCK

- VESTA JTAG
-
- R1741
- R1742
- R1743

- R1750
- 47K
- 1/16W
- 5%
- 10%
= PP3V3_ENETFW

- Q1750
- 2N7002DW-X-F

- R1741
- MF-LF
- 1/16W
- 5%

- R1752
- SOT-363
- 805
- X5R
- 6.3V
- 10%
= PP3V3_ENETFW

- C1720
- 0.1uF
- 0.1uF
- 0.1uF
- 10V
- CERM

- C1721
- 0.1uF
- 0.1uF
- 0.1uF
- 10V
- CERM

- C1722
- 0.1uF
- 0.1uF
- 0.1uF
- 10V
- CERM

- C1724
- 0.1uF
- 0.1uF

- C1725
- 0.1uF
- 0.1uF

- C1726
- 0.1uF
- 0.1uF

- C1727
- 0.1uF
- 0.1uF

- C1728
- 0.1uF
- 0.1uF

- C1729
- 0.1uF
- 0.1uF

- C1730
- 0.1uF
- 0.1uF

- C1731
- 0.1uF
- 0.1uF

- C1732
- 0.1uF
- 0.1uF

- C1733
- 0.1uF
- 0.1uF

- C1734
- 0.1uF
- 0.1uF

- C1735
- 0.1uF
- 0.1uF

- C1736
- 0.1uF
- 0.1uF

- C1737
- 0.1uF
- 0.1uF

- C1738
- 0.1uF
- 0.1uF

- C1739
- 0.1uF
- 0.1uF

- C1740
- 0.1uF
- 0.1uF

- C1741
- 0.1uF
- 0.1uF

- C1742
- 0.1uF
- 0.1uF

- C1743
- 0.1uF
- 0.1uF

- C1744
- 0.1uF
- 0.1uF

To keep Vesta from being held in reset when system is off

NOTE: Reset GPIO is active HIGH
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:
ALL OTHER CLOCK CONSTRAINTS ON THEIR RESPECTIVE BUS PAGES

Pulsar Aliases

www.laptop-schematics.com
IN TERM-OFF MODE THIS RESISTOR IS HERE TO FIX A KODIAK BUG.
EI OUTPUT FROM CPU B

EI INPUT TO CPU B

EI_BUS_SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M3/M33

WE MAY NEED A DIFFERENT ELECTRICAL_INTERFACE_SET FOR CPU_B AND CPU_B.

PLAYOUT AGREES TO THE FOLLOWING SCALE:

NET_SPACING_TYPE: NONE

DRAWING NUMBER: 051-6790 E

SYNC_DATE: 08/01/2005

SYNC_MASTER: Q63

FULL SCALE LIMITS TO

12345678

12345678

12345678

12345678

www.laptop-schematics.com

KODIAK EI B

APPLE COMPUTER INC.

051-6790 E

PAGE

0

1

2

3

4

5

6

7

8

D

C

B

A
CONNECT PULSAR CLKS TO CPU/NB

CONNECT SHASTA KI A TO/from CPU

CONNECT CPU TO SHASTA INT A0, NC OTHERWISE

CONNECT CPU TO SHASTA SRCOM A0, NC OTHERWISE

CONNECT CPU TO SHASTA QACK A0, NC OTHERWISE

CONNECT CPU TO SHASTA SYSCLK N, NC OTHERWISE

CONNECT CPU TO SHASTA QSYNC CPU A, NC OTHERWISE

CONNECT CPU TO SHASTA QSYNC R, NC OTHERWISE

CONNECT CPU TO SHASTA INT/CLKS, NC OTHERWISE

CONNECT CPU TO SHASTA INT A, NC OTHERWISE

CONNECT CPU TO SHASTA CHKSTOP OR MCP TO NB

CONNECT CPU TO SHASTA CPU/CLKS, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/CLK, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/RESET, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/RESET, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT/INT/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT/INT/INT/INT/INT, NC OTHERWISE

CONNECT CPU TO SHASTA CPU/INT/CLK/RESET/INT/CLK/RESET/INT/INT/CLK/RESET/INT/INT/INT/INT/INT/INT/INT, NC OTHERWISE


On-Board DDR SDRAM

APPLE COMPUTER INC.

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

NOTICE OF PROPRIETARY PROPERTY

SCALE

DRAWING NUMBER

12345678
## KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

<table>
<thead>
<tr>
<th>COL_NAME</th>
<th>ELECTRICAL_CONSTANT</th>
<th>DIFFERENTIAL_GAIN</th>
<th>PHYSICAL_GAIN</th>
<th>UNIT_LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

## KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

<table>
<thead>
<tr>
<th>COL_NAME</th>
<th>ELECTRICAL_CONSTANT</th>
<th>DIFFERENTIAL_GAIN</th>
<th>PHYSICAL_GAIN</th>
<th>UNIT_LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

---

**NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**NOT TO REPRODUCE OR COPY IT**

**TO MAINTAIN THE DOCUMENT IN CONFIDENCE**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING**

---

APPLE COMPUTER INC. 051-6790
ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

PLACE CLOSE TO SHASTA

---

**PCI_SB_PAR PCI_PAR**

**PCI_SB_STOP_L PCI_STOP_L**

**PCI_SB_TRDY_L PCI_TRDY_L**

**PCI_SB_IRDY_L PCI_IRDY_L**

**PCI_SB_FRAME_L PCI_FRAME_L**

**PCI_SB_DEVSEL_L PCI_DEVSEL_L**

**PCI_SB_CBE_L<3> PCI_CBE_L<3>**

**PCI_SB_CBE_L<2> PCI_CBE_L<2>**

**PCI_SB_CBE_L<1> PCI_CBE_L<1>**

**PCI_SB_CBE_L<0> PCI_CBE_L<0>**

**PCI_SB_AD<31> PCI_AD<31>**

**PCI_SB_AD<30> PCI_AD<30>**

**PCI_SB_AD<29> PCI_AD<29>**

**PCI_SB_AD<28> PCI_AD<28>**

**PCI_SB_AD<27> PCI_AD<27>**

**PCI_SB_AD<26> PCI_AD<26>**

**PCI_SB_AD<25> PCI_AD<25>**

**PCI_SB_AD<24> PCI_AD<24>**

**PCI_SB_AD<23> PCI_AD<23>**

**PCI_SB_AD<22> PCI_AD<22>**

**PCI_SB_AD<21> PCI_AD<21>**

**PCI_SB_AD<20> PCI_AD<20>**

**PCI_SB_AD<19> PCI_AD<19>**

**PCI_SB_AD<18> PCI_AD<18>**

**PCI_SB_AD<17> PCI_AD<17>**

**PCI_SB_AD<16> PCI_AD<16>**

**PCI_SB_AD<14> PCI_AD<14>**

**PCI_SB_AD<13> PCI_AD<13>**

**PCI_SB_AD<12> PCI_AD<12>**

**PCI_SB_AD<11> PCI_AD<11>**

**PCI_SB_AD<10> PCI_AD<10>**

**PCI_SB_AD<8> PCI_AD<8>**

**PCI_SB_AD<7> PCI_AD<7>**

**PCI_SB_AD<6> PCI_AD<6>**

**PCI_SB_AD<5> PCI_AD<5>**

**PCI_SB_AD<4> PCI_AD<4>**

**PCI_SB_AD<3> PCI_AD<3>**

**PCI_SB_AD<2> PCI_AD<2>**

**PCI_SB_AD<0> PCI_AD<0>**
NOTE: This AirPort implementation does not support PME.

PCI Devices implemented on this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
- _PCI_CLK33M_AIRPORT

Signal aliases required by this page:
- _PP3V3_PCI

Power aliases required by this page:

Page Notes

ELECTRICAL_CONSTRAINT_SET

PCI_CLK_AIRPORT CLOCKS PCI_CLK33M_AIRPORT

NET_SPACING_TYPE DIFFERENTIAL_PAIR

PRELIMINARY
NOTE: This USB2 implementation supports AD27 (Slot "G") - USB2 (0x1033/0x0035) PCI Devices implemented on this page:

Page Notes

=PPVIO_PCI_USB2

RC250, RC251 & RPC203 REQUIRED TO RC251

MF-LF 1/16W 47 21 5%

SM-LF 1/16W 47 47 5%

RC216 72 MF-LF 1/16W 402 47 5%

RC213 10K MF-LF 402 21

RC214 5% 2 1 MF-LF

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

PPC201

P4MM

PP_VIOPCIUSB2_C2

PPC203

APPLE COMPUTER INC.

SYNC_MASTER=Q63  
SYNC_DATE=08/01/2005

II NOT TO REPRODUCE OR COPY IT 
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE 
AGREES TO THE FOLLOWING 
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY 
NOTICE OF PROPRIETARY PROPERTY 
SCALE
Allows ROM override module to intercept ROM chip select

Q63 APPLICATION IS RUN

NOTE: This page does not specify a BootROM

Power aliases required by this page: (NONE)

Signal aliases required by this page:

SOM options provided by this page:

CC501 2.2UF 6.3V CERM 20% 603
CC500 10V 0.1uF CERM 402 20% 2
RC503 1/16W 5% 402 MF-LF 10K 2
RC504 10K MF-LF 402 5% 1/16W 2
RC500 10K MF-LF 402 5% 1/16W 2

www.laptop-schematics.com
SATA data pairs is 100 ohms.

Secondary Length:  12.70mm
Line To Line:       0.38mm

Signal aliases required by this page:

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901
ATA-6 spec does not call out C8177.

UATA_INTRQ

Notes for shared page 127:
For M23/M33 create a wide shape for FFV2, SATA, VDD and then neck down to the default value when necessary. The width/neck properties on page 127 are set by G63 for schematic sharing.

LC700 changed to 1550U240 (600 ohm, 0.2 ohm DCR, 1A)
Previous one was 1550S011 (600 ohm, 6.6 ohm DCR, 0.2A)
Per Tokin America PN: N2012Z601.

4-11-05: Board file has physical/spacing name assignment already for SATA diff pairs (cap to SHASTA), but not for the SATA cap to connector routes, which the above are added for this purpose.

UATA trace impedance route to 50 ohms.

4-8-05:
Note for shaded page 127:
For M23/M33 create a wide shape for FFV2, SATA, VDD and then neck down to the default value when necessary. The width/neck properties on page 127 are set by G63 for schematic sharing.

FFV2, SATA, VDD and then neck down to the default value when necessary. The width/neck properties on page 127 are set by G63 for schematic sharing.

Updated AC coupling caps for SATA J9000.
Added decoupling caps for J9000 PP5V, SATA NET.

4-12-05:
Note for shaded page 127:
For M23/M33 create a wide shape for FFV2, SATA, VDD and then neck down to the default value when necessary. The width/neck properties on page 127 are set by G63 for schematic sharing.

FFV2, SATA, VDD and then neck down to the default value when necessary. The width/neck properties on page 127 are set by G63 for schematic sharing.

Updated AC coupling caps for SATA J9000.
Added decoupling caps for J9000 PP5V, SATA NET.
Page Notes

This page contains a schematic diagram of the Shasta Ethernet network interface. The diagram shows the connections and signals for the Ethernet TX and RX lines. The annotations indicate specific parts and their connections.

The schematic includes components such as the Ethernet controller, TX and RX pins, and associated clocks and signals. Detailed labels indicate the function of each part and the flow of data.

The page also contains a table with parts and their specifications, which can be referenced for more information.

The diagram is preliminary and may change as the design evolves. The parts listed in the table include resistor values, part numbers, and other relevant technical details.

For a more detailed understanding, please refer to the full schematic and the accompanying documentation.
EXTRA CONSTRAINTS TO SUPPLEMENT THE MISSING NET PHYSICAL FROM EARLIER PAGE

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PLACE THESE PARTS NEAR VESTA

Spare GND vias for layer traversals during routing
Termination
Place close to Firewire PHY

ESD Rail
CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.6 mm