<table>
<thead>
<tr>
<th>PDF</th>
<th>CONTENTS</th>
<th>SYNC</th>
<th>MASTER</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td>FINO-DD</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td>FINO-PC</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Table Items</td>
<td>FINO-M23</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>FUNC TEST 1 OF 2</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Power Conn / Alias</td>
<td>M23-PC</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Signal Alias</td>
<td>FINO-DD</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>FUNC TEST 2 OF 2</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1.8V Vreg</td>
<td>M23-PC</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>1.5V Vreg</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>1.2V Vreg</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>3V &amp; 3.3V Fets</td>
<td>FINO-PC</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Vesta Core / Misc</td>
<td>FINO-DC</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>KODIAC CORE &amp; BYPASS</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>KODIAC &amp; SHASTA MISC</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Shasta Core Power</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Shasta Serial / Misc</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PULSAR2 POWER</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>PULSAR2 CLOCKS</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Pulsar Aliases</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>System Management Unit</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>SMU SUPPLEMENTAL (2)</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>SMU SUPPLEMENTAL (3)</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>SMU SUPPLEMENTAL (4)</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Fan 0, 1 &amp; System Temp</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Fan 2 &amp; HD Temp</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>I2C Connections</td>
<td>FINO-ME</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>KODIAC E1 PWR &amp; CAPS</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>KODIAC E1 A</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>CPU E1 AND IO</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>KODIAC E1 B</td>
<td>q63</td>
<td>08/01/2005</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>CPU STRAPS</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>CPU POWER AND BYPASS</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>PROC DECOUPLING</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>CPU VCORE VREG</td>
<td>M23-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>CPU VCORE MORE BYPASS</td>
<td>FINO-HS</td>
<td>06/20/2005</td>
<td></td>
</tr>
</tbody>
</table>

**IMG5 17" REV F 11/15/05**
### Processors

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
<th>PART NUMBER BOM</th>
<th>OPTION REF</th>
<th>DES</th>
<th>COMMENTS</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>DRAWING NUMBER</th>
<th></th>
</tr>
</thead>
</table>

---

### ASICS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S) BOM</th>
<th>OPTION</th>
<th>VALUE</th>
<th>VOLT.</th>
<th>WATT.</th>
<th>TOL.</th>
<th>PART #</th>
<th>PACKAGE</th>
<th>DEVICE</th>
</tr>
</thead>
</table>

---

### MISC PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S) BOM</th>
<th>OPTION</th>
<th>VALUE</th>
<th>VOLT.</th>
<th>WATT.</th>
<th>TOL.</th>
<th>PART #</th>
<th>PACKAGE</th>
<th>DEVICE</th>
</tr>
</thead>
</table>

---

### ALTERNATES

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>OPTION</th>
<th>PART #</th>
<th>PACKAGE</th>
<th>DEVICE</th>
</tr>
</thead>
</table>

---

---
PP1V2_ALL VOLTAGE REGULATOR

NOTE:
- SET OUTPUT=1.22-1.23V
- IR(DS)SS=2.0mOhm
- VDD7=VREF*(R1003+R1005)/R1005=1.22-1.23VDC
- POWER BUDGET CURRENT OF TOTAL RAILS

1.2A PEAK
2.4A CONTINUOUS

PP1V2_PWRON FET SWITCH
PEAK CURRENT 1.3A
1.2A CONTINUOUS

PP1V2_RUN FET SWITCH
PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT

NOTE:
- SS comes up before GPU POWERUP.L so that SHASTA CORES GET POWER BEFORE ANYTHING ELSE
PP2V5_ALL VOLTAGE REGULATOR

NOTE:
- SET OUTPUT=2.5V
- VD05_VREG = VERR=1.24VDC
- VD07=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS:
- 0.1A PEAK
- 0.1A CONTINUOUS

REV. 551-6790 F
SYNC_MASTER=FINO-PC
SYNC_DATE=06/20/2005

PP2V5_PWRON FET SWITCH
- PEAK CURRENT 0.1A

PP2V5_RUN FET SWITCH
- PEAK CURRENT 0.1A

NOSTUFF OPTION TO DELAY 2.5V PWRON TO COME UP WITH 3.3V PWRON

PP2V5_ALL VOLTAGE REGULATOR
- 10UF 20% 1206 CERM 6.3V2
- 1UF 20% 0.01UF 2 1 C1580
- 0.01UF 402 CERM 16V 20%
- 21 R1512
- 21 R1513
- 1.02K 402 1/16W MF-LF 1%
- 1K 402 1/16W MF-LF 5%
- 100K 402 1/16W MF-LF 5%
- 402
- 5% MF-LF 1/16W 0
other Shasta supplies.

Must power Shasta VCore rail before any Power Sequencing:

BOM options provided by this page:

- =PP1V2_PWRON_SB_VCORE
- =PP2V5_PWRON_SB
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)

Power aliases required by this page:

Page Notes

=PP3V3_PWRON_SB

=PP2V5_PWRON_SB

=PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:

ALL OTHER CLOCK CONSTRAINTS ON THEIR RESPECTIVE BUS PAGES

www.laptop-schematics.com
SMU ALIASES

SMU ALIASES

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHEN THEY DIFFER FROM Q63.

Q63 USES P7.2 AS IT WAS A RES.

M23/M33 SIGNALS DIFFER FROM P7.2.

M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.

M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.

M23/M33 DOESN'T USE P1.4. NC ON PG 7.

M23/M33 DOESN'T HAVE THOSE FANS.

M23/M33 HAS NO SLOTS.

SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.

SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.

SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.

M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.

M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.

Q63 USES P7.2 AS IT WAS A RES.

NOTE: SC2642 VID PINS HAVE LEAKAGE TO GND.

SO PULLUPS MUST BE 1K FOR CPU VRM10.

NOTE: PULL UP CPU_VID<5> TO 2.2V FOR CPU VRM10.

NOTE: CPU VID<0:5> CONTROLLED BY SMU

NOTE: VIDS CONTROLLED BY SMU

NOTE: VIDS CONTROLLED BY SMU

NOTE: VIDS CONTROLLED BY SMU

FEATURES MAY BE 1K FOR CPU VID<5>

MIN_NECK_WIDTH=0.2MM

SMU SUPPLEMENTAL (4)
NOTICE OF PROPRIETARY PROPERTY

I agree to the following:

1. Not to disclose the document in confidence.
2. Not to publish in whole or part.
3. Not to reproduce or copy it.

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the above.

Fan 0, 1 & System Temp

SMU_FAN_TACH0
SMU_FAN_RPM0
SMU_FAN_TACH1
SMU_FAN_RPM1

Sync master = FINO-HS
Sync date = 06/20/2005

Fan 0, 1 & System Temp

SMU_FAN_TACH0
SMU_FAN_RPM0
SMU_FAN_TACH1
SMU_FAN_RPM1

Sync master = FINO-HS
Sync date = 06/20/2005
Q63: SEE P.28 FOR MORE DECOUPLING CAPS FOR THESE PINS.
ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAM CARD VERSION A

DIFFERENTIAL_PAIR=RAM_DQS_R_5_DP
DIFFERENTIAL_PAIR=RAM_DQS_R_3_DP

RAM_DQS_P_R<4>RAM_DQS_P<4>
RAM_DQS_N_R<3>RAM_DQS_N<3>
RAM_DQS_P_R<3>RAM_DQS_P<3>
RAM_DQS_N_R<2>RAM_DQS_N<2>
RAM_DQS_N_R<1>RAM_DQS_N<1>
RAM_DQS_N_R<0>
RAM_DQS_P_R<0>

RAM_DQ_R<61>RAM_DQ<61>
RAM_DQ_R<60>RAM_DQ<60>
RAM_DQ_R<59>RAM_DQ<59>
RAM_DQ_R<58>RAM_DQ<58>
RAM_DQ_R<56>RAM_DQ<56>
RAM_DQ_R<46>RAM_DQ<46>
RAM_DQ_R<43>RAM_DQ<43>
RAM_DQ_R<37>RAM_DQ<37>
RAM_DQ_R<36>RAM_DQ<36>
RAM_DQ_R<32>RAM_DQ<32>
RAM_DQ_R<28>RAM_DQ<28>
RAM_DQ_R<25>RAM_DQ<25>
RAM_DQ_R<24>RAM_DQ<24>
RAM_DQ_R<21>RAM_DQ<21>
RAM_DQ_R<20>RAM_DQ<20>
RAM_DQ_R<18>RAM_DQ<18>
RAM_DQ_R<17>RAM_DQ<17>
RAM_DQ_R<16>RAM_DQ<16>
RAM_DQ_R<14>RAM_DQ<14>
RAM_DQ_R<13>RAM_DQ<13>
RAM_DQ_R<12>RAM_DQ<12>
RAM_DQ_R<11>RAM_DQ<11>
RAM_DQ_R<10>RAM_DQ<10>

RAM_WE_L
RAM_CAS_L RAM_CAS_L_R
RAM_RAS_L RAM_RAS_L_R
RAM_BA<2> RAM_BA_R<2>
RAM_A<15> RAM_A_R<15>
RAM_A<12> RAM_A_R<12>
RAM_A<9> RAM_A_R<9>
RAM_A<7> RAM_A_R<7>
RAM_A<5> RAM_A_R<5>
RAM_A<0> RAM_A_R<0>
Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN
ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

PLACE CLOSE TO SHASTA
NOTE: Target differential impedance for
Secondary Length:  12.70mm
Primary Max Sep:    0.25mm outer
Line To Line:       0.38mm

Signal aliases required by this page:

Power aliases required by this page:

Page Notes

Net Spacing Type: SATA

See Table

SYNC_MASTER=M23-DC  SYNC_DATE=06/20/2005

APPLE COMPUTER INC.
arie 10pF
DEVELOPMENT
CERM
50V5%

129
MF-LF
499
RC916

2
127 6
127 6
127 6

MF-LF
1/16W
402
402

SATA_RXD_P2_C NC_SATA_RXD_P2_C

UATA_INTRQ_R
UATA_DMARQ_R
UATA_STOP
UATA_DD<3>
UATA_DD<2>
UATA_DD<7>
UATA_DA<0>

MAKE_BASE=TRUE
NC_SATA_TXD_N2
MAKE_BASE=TRUE
NO STUFF

CC904
1
1

402
16V
10%

CERM

516S0327
F-ST-SM
RC912

UATA_IOCS16_PU
UATA_HSTROBE
UATA_DD<15>
UATA_DD<9>

5%

NO CLOSER THAN 0.152MM TO DIFF PAIRS. ONE GND VIA PER HOLE-VIA-P5RP25

PLACE CC909/CC910 CLOSE TO JC901 FOR PP5V_PATA.

4-8-05
NOTES FOR SHADED PAGE 127
FOR M23/M33 CREATE A MIDDLE SHAPE
FOR PPV2_SATA_VDD AND THEN HECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDT/NECK PROPERTIES ON PAGE 127
ARE SET BY G63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM, 0.2 OHM DCR, 1A)
PREVIOUS ONE WAS 155S0231 (600 OHM, 0.2 OHM DCR, 1A)
PER TOKIN AMERICA PN: M201224001

4-11-05
BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR DATA DIFF PAIRS (CAP TO SHASTA).
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR DATA DIFF PAIRS (CAP TO SHASTA).
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

DATA FROM SHASTA U2300 TO RP4S

DATA FROM RP4S TO JC901

4-12-05: ADD THREE GROUND VIA PAIR
THIS LAYER JUMP FOR THE DATA
DIFF PAIRS. ONE VIA PER SIGNAL VIA, AND PLACE ON VIA
NO CLOSER THAN 0.132MM TO SIGNAL VIA.

4-12-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR DATA DIFF PAIRS (CAP TO SHASTA).
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A MIDDLE SHAPE
FOR PPV2_SATA_VDD AND THEN HECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDT/NECK PROPERTIES ON PAGE 127
ARE SET BY G63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM, 0.2 OHM DCR, 1A)
PREVIOUS ONE WAS 155S0231 (600 OHM, 0.2 OHM DCR, 1A)
PER TOKIN AMERICA PN: M201224001

4-11-05
PPV2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSSES ACROSS THE Q1306 ET
S132106V.

4-12-05
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.
PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

<table>
<thead>
<tr>
<th>SHASTA → VESTA</th>
<th>ENET_TXD&lt;0&gt;</th>
<th>ENET_TXD&lt;2&gt;</th>
<th>ENET_TXD&lt;1&gt;</th>
<th>ENET_TXD&lt;3&gt;</th>
<th>ENET_TXD&lt;5&gt;</th>
<th>ENET_TXD&lt;4&gt;</th>
<th>ENET_TXD&lt;7&gt;</th>
<th>ENET_TXD&lt;6&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
</tr>
</tbody>
</table>

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

<table>
<thead>
<tr>
<th>VESTA → SHASTA</th>
<th>ENET_TXD&lt;0&gt;</th>
<th>ENET_TXD&lt;2&gt;</th>
<th>ENET_TXD&lt;1&gt;</th>
<th>ENET_TXD&lt;3&gt;</th>
<th>ENET_TXD&lt;5&gt;</th>
<th>ENET_TXD&lt;4&gt;</th>
<th>ENET_TXD&lt;7&gt;</th>
<th>ENET_TXD&lt;6&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
</tr>
</tbody>
</table>

www.laptop-schematics.com
CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

FW_TPB1_FL FW FW FW_PORT1_TPB_N_FL

FW_TPA1_FL FW FW FW_PORT1_TPA_N_FL

FW_TPA_P<1> FW_TPB_N<1> FW_TPA_N<1>

FW_TPB_P<0> FW_TPBIAS<1>

MIN_LINE_WIDTH=0.38 mm VOLTAGE=3.3V

NC_FW_TPA_N2 NC_FW_TPA_P2

MAKE_BASE=TRUE NO_TEST=YES MAKE_BASE=TRUE

VOLTAGE=24V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

CE064 270pF CERM2

RE062 1/16W 1% CERM

BZX84C2V7-X-F FW_PORT1_TPB_P FW_PORT1_TPB_N

VOLTAGE=12V MIN_NECK_WIDTH=0.25MM

CE022 CERM 50V 10% 1/16W

CE016 603-1 0.001UF 10% 4

CE013 0.001UF 10% 4

LE010 1206-LF

SYM_VER-1 32

FLE011 120-OHM

SYM_VER-1 2012

120-OHM PP12V_ALL_FW

PPFW_PORT0_VP

PPFW_PORT1_VP_FL

VOLTAGE=24V

MIN_LINE_WIDTH=0.8MM 10%

CERM 50V 2 1

CERM 50V 2 1

DPE020 DPE010

BAV99DW-X-F BAV99DW-X-F

CON, 1394A 7 DEGREES 20_INCH_LCD514-0251 JE000 CRITICAL1

MIN_NECK_WIDTH=0.8MM

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.8MM

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm
BOM options provided by this page:

- PP3V3_PWRON_BT
- PP5V_PWRON_UDASH

USB pairs to their appropriate termination nodes so they are not needed here:

- USB_BT_P
- USB_BT_N

USB HUB implements 15K pull downs internally:

- PORT 1
- PORT 2
- PORT 3

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB port controllers will provide the appropriate constraints to apply to unused USB D+/D- XNets.

USB controller outputs to indicate control on USB ports 2-4. Rename these properties for M23/M33 placed on this page.

NOTE: This design does not provide power to apply to entire USB D+/D- XNets.

External USB Ports