# Table of Contents

1. **Table Of Contents**

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2. **Board Information**

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3. **System Block Diagram**

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6. **i2C Connections**

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7. **i2C Connections**

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9. **Microcontroller Interface**

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10. **Microcontroller Interface**

    | CONTENTS | SYNC MASTER | DATE |
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    | Sudden Motion Sensor | N/A | N/A |
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    | Memory Interface | N/A | N/A |
    | Memory Interface | N/A | N/A |
Enhanced MAC-1 Test Coverage

Functional test points use a P4 pad placed on bottom side.
Page Notes

Power aliases required by this page:
- PMU

Signal aliases required by this page:
- I2C

NOTE: Neither option is necessary when PMU unstead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.

Selects whether MMU is powered all time or only when the system is on.

Mus devices are connected directly to PMU instead. Use ADT7467 connects to NB I2C bus 1 to resolve address conflict.

EXT TMDS/S
(Write: 0x72 Read: 0x73)

EXT TMDS/S
(Write: 0x70 Read: 0x71)

I2C Connections

SouthBridge I2C Bus

PMU I2C Bus

PMU SMBus

Battery Conn

GPU I2C Bus

Audio Board

NorthBridge I2C Bus

DIMMs

SDS

Codec

SPDIF

Apple Computer Inc.

Model: Apple MacBook Pro

Sync Date: N/A

Rev.: D

Drawiing Number: 115

Spacing:

Electrical ConstraintSet:

PowerAliases:
- PMU

SignalAliases:
- I2C

Apple Computer Inc.
ADAPTER INPUT/INRUSH LIMITER

Power Inputs

BATTERY INPUT/CURRENT SENSE
1.5V/1.8V SWITCHER

Vout = 1.0V * (1 + Ra/Rb)
Page Notes

General notes required by this page:
- PWR_CTRL: System supply for two power
- PWR_CTRL: Charging 24V power

Notes:
- All options provided by this page.
- Omitting SBUS / LIPWR / SBUS options.
- If both options are off the
  resistor will be in terminated mode.

- VESTA1V2_BURST / VESTA1V2_PULSE

BOM options provided by this page:

Signal aliases required by this page:
- =PP3V3_RUN_FWPORTPWRSW
- =PPBUS_FW (system supply for bus power)

Power aliases required by this page:

Page Notes
Bis at least one 10uF cap per rail. If aliased together, make sure there is no separate routing of the output using the same power rails.

Page Notes

3.3V I/O DECOUPLING
(40 balls on I2)

12 Power
Power Sequencing

1. **Power-Up**: GPUVCORE_PGOOD
2. **Wake**: GPUVCORE_PGOOD
3. **Shutdown**: GPUVCORE_PGOOD

- **SYS_PWRSEQ_FINAL**: ANALOG INPUT, SENSE > 1.7V
- **SYS_PWRSEQ_6_L**: ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
- **SYS_PWRSEQ_5**: I2VCORE_PGOOD
- **SYS_PWRSEQ_4**: ACTIVE-HIGH, OUTPUT, PUSH-PULL
- **SYS_PWRSEQ_3_L**: ACTIVE-HIGH, OUTPUT, PUSH-PULL
- **PMU_POWER_UP_L**: ACTIVE-LOW, OUTPUT, OPEN-COLLECTOR

Additional notes:
- **100K pull-up to 3.3V_ALL on pg 13**
- **2N7002DW-X-F**
- **Q2900, R2949, R2935, R2913**: 100K, MF-LF, 1/16W
- **MAKE_BASE=TRUE**
- **PP5V_RUN_PWRSEQ**
- **PP3V3_PWRON_PWRSEQ**
- **PP3V_All_PWRSEQ**
- **PP5V_PWRON_PWRSEQ**
- **2N7002DW-X-F**, **Q2940, R2969**, **Q2941, R2965**: 100K, MF-LF, 1/16W
- **MAKE_BASE=TRUE**
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<td>D2+</td>
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<tr>
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<td></td>
<td>3.3V</td>
</tr>
<tr>
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</tr>
<tr>
<td>MIN_NECK_WIDTH</td>
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**Notes:**
- Keep stuffing resistors close to ADT7467 controller.
- **Fan Controller**
- Fan Controller is connected so as to be backward compatible with the ADT7460.
- I2C READ ADDR = 0x5C, WRITE ADDR = 0x5D
- (Device is connected so as to be backward compatible with the ADT7460.)
ADAPTER CONNECTOR

RIGHT USB BOARD

BACKUP BATTERY CONNECTOR

PBUS HOLD-UP CAPS

LEFT ALS CONNECTOR

CPU FAN

GPU FAN

STYLE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

Q16C Internal I/O II
SLOT "B"

UPPER SLOT

CUSTOMER SLOT

ONE 0.1UF PER SLOT

0.1uF

0.1uF

CERM402

10V20%

603 X5R 6.3V 20%

SLOT "B"

CUSTOMER SLOT
<table>
<thead>
<tr>
<th>I</th>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>B1</td>
<td>LED1</td>
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<tr>
<td>B2</td>
<td>LED2</td>
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<td>B3</td>
<td>LED3</td>
<td>3</td>
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<td>B4</td>
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### Electrical Constraints

- **Spacing**
  - Differential Pair: 48
  - Physical: 48
  - Electrical: 48

---

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---

### Scale

- **D**
  - 45.1
  - 45.1
  - 45.1
  - 45.1

---

### Drawing Number

- **12345678**

---

### Mill Frame Buffer Constraints

- **Unlock**
- **Unlock**
- **Unlock**

---

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NOTE: AGP 8x signals are not provided (NONE)

BOM options provided by this page:
- "=AGP_VREF" - VRef divider output for Signal aliases required by this page:
- "=PP1V5_AGP"
- "=PP3V3_AGP"

Power aliases required by this page:
- "ELECTRICAL_CONSTRAINT_SET"
- "SPACING_PHYSICAL_DIFFERENTIAL_PAIR"
- "NET_TYPE"

PLACE C5731 AT GPU
PLACE C5732 AT NB
PLACE RESISTORS MIDWAY BETWEEN CONNECT TO GPU AGP REF
0.1uF X5R 16V 10%

APPLE COMPUTER INC.
NOTE: Implements a low-swing DVO bus only
- DVO_1V5
- =PP1V5_GPU_DVO
- =PP1V8R2V5_GPU_FB_VIO

FERR-220-OHM
L6050

- GPU_LVDDR_2V8
- GPU_LVDDR_2V5
- =PP1V8_GPU_LVDS_PLL
- =PP1V5_AGP
- =PP1V8_GPU_PANEL_IO

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V

APPLE COMPUTER INC.
NOTE: This AirPort implementation does not support PME.

PCI Devices implemented on this page:
- =USB_BT_N (Bluetooth USB D-)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =PP3V3_PCI (802.11g Power)

**PCI Devices**

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**Q85 Connector**

Q56C/51600341/F-010-MM
Q56C/51600342/F-010-MM-IP
NOTE: This USB2 implementation supports AD27 (Slot "G") - USB2 (0x1033/0x0035)
unique ECSet name to allow this.

violation on I2. May want to provided by the PHY page or a (NONE) This page does not provide a pull-up or pull-down resistor.

NOTE: All I2 GPIOs should have a schematic page.

signals, should be provided by the PHY page or a non-shared termination, including clock

Any NOTE: This page does not provide any BOM options provided by this page:

Signal aliases required by this page:

- =PP2V5R3V3_PWRON_I2_ENET

Page Notes

I2 Ethernet Interface

Note: Any device should have a pull-up or pull-down resistor.
This page does not provide a resistor for J22[0]. It must be provided by the PHY page or a non-shared schematic page.

Note: ENET_MDIO has a pull-down
initiated on J2. Any user to
provide a 1.5K pull-down on J2.

These signals are referenced to the Ethernet I/O rail
ABBREV=DRAWING

1394b implementation based on Apple
assumed that FireWire PHY page will
constrained on this page. It is
properly terminate unused signals.
appropriate connectors and/or to
necessary aliases to map the

NOTE: This page is expected to contain the

-GND_CHASSIS_FW_PORT2
-GND_CHASSIS_FW_PORT1
-PPFW_PORT2

Power aliases required by this page:

Page Notes

SPACING

NET_TYPE

CERM

FW FW_PORT2_TPB_FLFW FW_PORT2_TPB_N_FL
FW FW_PORT1_TPB_FLFW FW_PORT1_TPB_N_FL

2

1

DIFFERENTIAL_PAIR

PHYSICAL

MF-LF

1/16W

604
21

402

21

VOLTAGE=3.3V

1

1

1%

50V

10%

1

1

1%

50V

10%

1

1

1%

50V

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1%
Plane series terminators approximately halfway between Vesta and NB. (They should probably be slightly closer to Vesta than the NB.)

**R9100**
- RP9100
- RP9100
- RP9100
- RP9100
- RP9101
- RP9101
- RP9101
- RP9101
- RP9102
- RP9102
- RP9103
- RP9103

FW_LREQ_R
FW_LPS_R
FW_LPS
FW_CTL_R<0>
FW_CTL<0>
FW_CTL_R<1>
FW_CTL<1>
USB2 data pairs is 90 ohms.

Signal aliases required by this page:

Net spacing type: USB2

Page Notes

Page: B

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Page dimensions: 1224.0x792.0
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---

**Spacing & Physical Constraints 2**

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**Rev.**

APPLE COMPUTER INC.

**Scale**

NONE

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